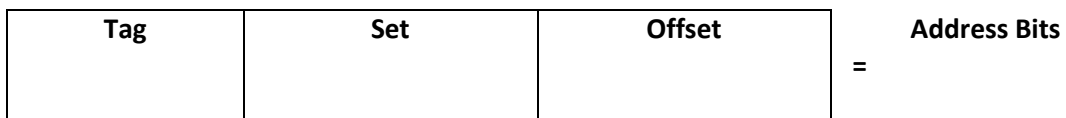


1. Fully associative caches

a. Example

- i. Same cache parameters as before, except now a FA cache
- ii. 8-byte FA cache with line size of 2, and 4-bit address



2. Cache mapping example

- a. Use same addresses and data from DM cache example previously

Address	Data
0110	0x1B
0111	0x59
1000	0xFE
1001	0x3D
1110	0x0C
1111	0x3A
1010	0x25
1011	0x98

- b. Load addresses into cache in same fashion

Memory Access	Tag	Offset	Access Type	Data	Hit or Miss
0110			Read		
1000			Read		
1110			Read		
1010			Write	0xBE	
1011			Write	0xEF	

- c. Place values from first three accesses into table below

Line in Cache	Tag	Byte 0	Byte 1
00			
01			
10			
11			

- d. Now we introduce writes

Line in Cache	Tag	Byte 0	Byte 1
00			
01			
10			
11			

3. Set associative caches

- a. Example

- Same cache parameters as before, except now a 2-way SA cache
- 8-byte 2-way SA cache with line size of 2, and 4-bit address

Tag	Set	Offset	= Address Bits

4. Cache mapping example

- a. Use same addresses and data from previous two examples

Address	Data
0110	0x1B
0111	0x59
1000	0xFE
1001	0x3D
1110	0x0C
1111	0x3A
1010	0x25
1011	0x98

- b. Load addresses into cache into same fashion

Memory Access	Tag	Set	Offset	Access Type	Hit or Miss
0110				Read	
1000				Read	
1110				Read	
1010				Read	

- c. Place values from accesses into table below
- i. How do we know which line in set 1 to evict?

Set	Line in Cache	Tag	Byte 0	Byte 1
0	0			
	1			
1	2			
	3			

5. Cache replacement algorithms

- a. How do we evict lines from a given set for non-DM caches?

6. Cache write policies

- a. If we change values that reside in main memory, we make changes in cache first
- b. What happens when we need to evict a line?
- c. Write-through

- d. Write-back