1. Cache mapping example
    a. Continued from the previous notes
    b. Current cache: 8-byte 2-way SA cache with line size of 2, and a 4-bit address

Tag	Set	Offset		Address Bits
4 – 2 – 0 = 2 bits	$\log_2 S = \log_2 2 = 1$ bit	$\log_2 LS = \log_2 2 = 1$ bit	=	4 bits

    c. Use same addresses and data from previous two examples

Address	Data
0110	0x1B
0111	0x59
1000	0xFE
1001	0x3D
1110	0x0C
1111	0x3A
1010	0x25
1011	0x98

    d. Load addresses into cache into same fashion

Memory Access	Tag	Set	Offset	Access Type	Data	Hit or Miss
0110						
1000						
1110						
1010						
1110						

    e. Place values from accesses into table below
        i. How do we know which line in set 1 to evict?

Set	Line in Cache	Tag	Byte 0	Byte 1	Dirty
0	0				
	1				
1	2				
	3				

2. Cache replacement algorithms
    a. How do we evict lines from a given set for non-DM caches?
        i. Why do we not need a replacement policy for DM caches?

3. Cache write policies

    a. Write-through

    b. Write-back