

DEPARTAMENTO DE ENGENHARIA ELECTROTÉCNICA -FCT/UNL CONVERSORES DE SINAL –NYQUIST RATE ADCS (Nuno Paulino, DEEC, 2023)

Analysis of an ADC using a high-level model

The objective of this work is to develop a high-level model for an *nbit* SAR-Pipeline ADC. This model should accurately describe the behaviour of the ADC circuit described in the paper, "A 12-Bit, 300-MS/s Single-Channel Pipelined-SAR ADC With an Open-Loop MDAC", Chao Wu and Jie Yuan, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 54, NO. 5, MAY 2019, without requiring electrical simulations. Using this model, it should be possible to obtain the digital output code of the ADC for any given input voltage. The model should include capacitor mismatch errors, residue amplifier gain errors and comparator offset errors.

- a) Carefully read the paper to understand the correct operation of the circuit. If necessary, obtain and read papers cited by this paper.
- b) Analyse the capacitor array circuit (shown in Fig. 6 in the paper) to obtain the expression of $(V_{CP} V_{CN})$ as a function of Δv_{in} , the control bits and the capacitors values. Use the charge conservation principle in your analysis. Note that this capacitor circuit uses a modified monotonic switching scheme.
- c) Using the previous expression, write a Matlab/Octave model of the behaviour of this sub SAR ADC, including the offset error of the comparator (or comparators). Note that the SAR ADC uses two capacitor arrays and fully differential signals. Include random errors into the capacitors' values and into the comparator's offset voltages.
- d) Model the complete pipeline ADC, composed by 2 stages with 1 residue amplifiers in between stages, as shown in Fig. 4. Include an error into the residue amplifiers gain.
- e) Use the previous model to calculate the transfer function of the ADC ($d_{out}(v_{in})$) and compute the transition voltages of the ADC for a given set of errors.
- f) Use the model to obtain measure the linearity of the ADC.
- g) Run Monte Carlo analysis of the ADC model to determine the sensitivity of the ADC to mismatch errors between the different components.
- h) Compare your results with the results reported in paper.
- i) (optional) Model the distortion introduced by the residue amplifier including dynamic effects.