

Abstraction As A Practical Debugging Tool

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Broad Motivation

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In current industrial practice, formal is quite isolated from traditional functional verification tool flows.

How can we achieve closer and synergistic integration of these two complementary techniques?

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Focus: RTL implementations of pipelines and hardware communication protocols.

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- The tool is parameterized by the amount of abstraction desired.
- Abstraction parameters are user-controlled to target various design facets.

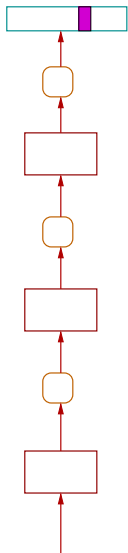
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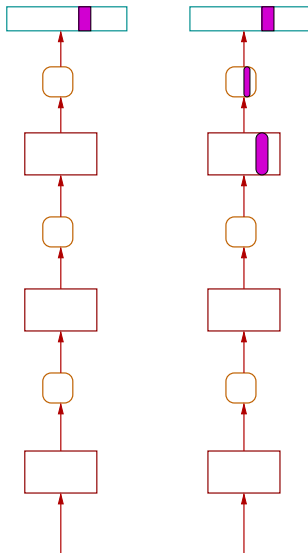
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Tool used to abstract RTL implementations of pipelined transaction queues.

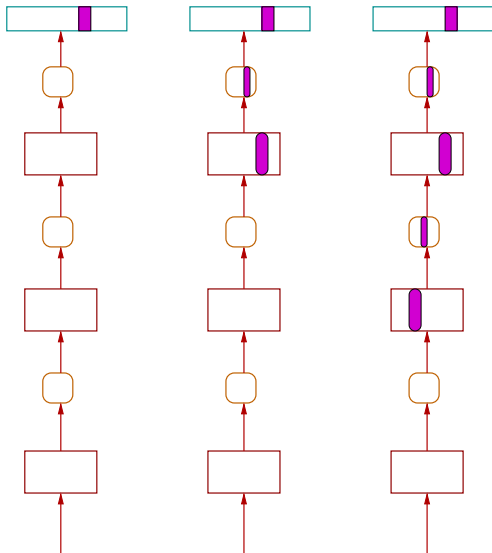
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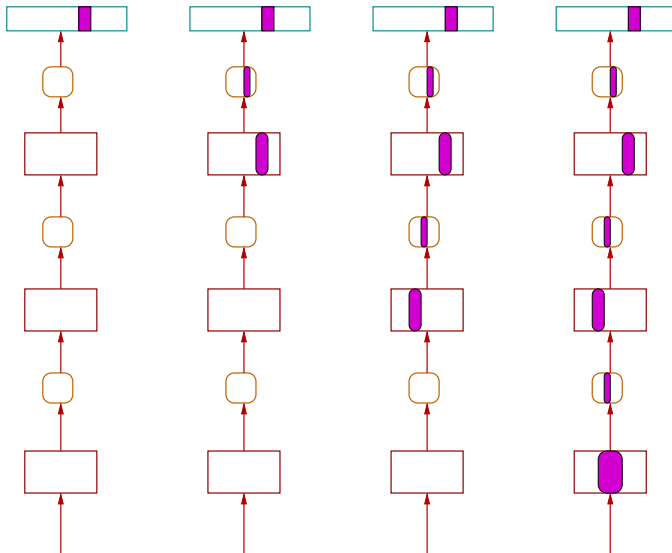
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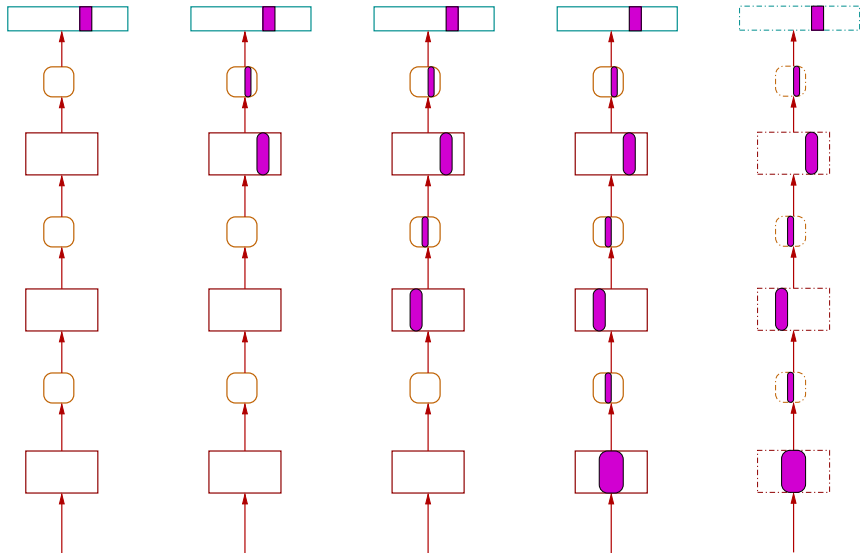
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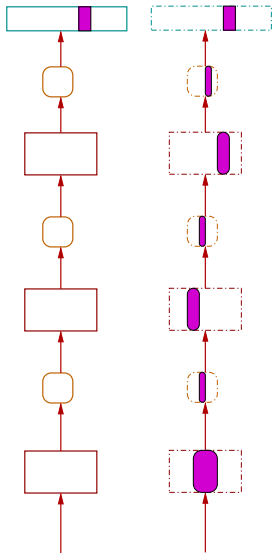
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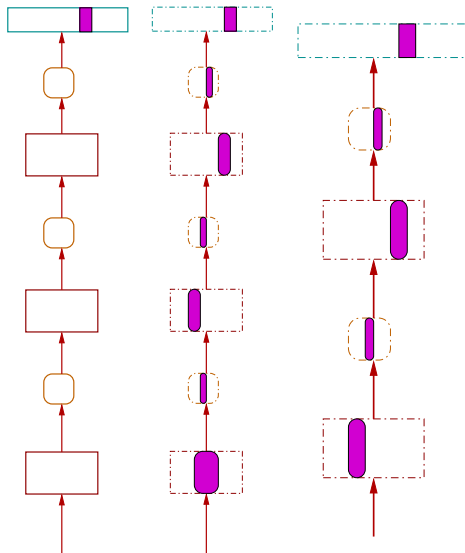
Yes, in principle, but with some important differences.

- These are not just syntactic checks of variables. We must comprehend the semantics of operations.
- Since the goal is to help simulation, not target formal correctness, the abstraction generation requirements are different.

How Much Do We abstract?



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The answer is driven by which stage simulation wishes to target.

Similar questions arise in dealing with non-determinism.

It is critical for the tool to be configurable for generating a range of abstractions.

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Our current procedure works well in practice.

- Generated over 500 abstractions of OR1200 instruction pipeline in a few seconds.

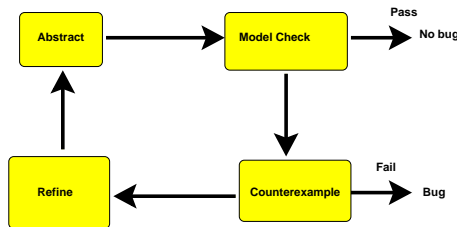
We are currently looking to apply the approach on cache coherence and other protocols.

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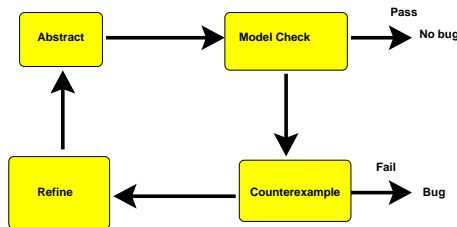
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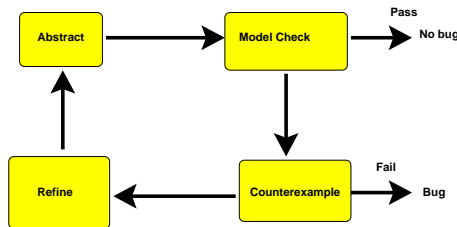


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But the focus of these abstractions is on constructing a formal proof, not models for simulation.

Our tool is a fast, configurable, but not necessarily complete.

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I believe it is by such synergistic combination of formal and dynamic that we can reach the target of a scalable and efficient verification paradigm.

Questions?

Thank You!