Cache Controller FSM

IDLE

comp = Rd | Wr
offset_out = offset_in
write_cache = Wr
done = (Rd | Wr) & (hit & valid_in)
cache_hit = hit & valid_in
stall_out = 1'b0

WB0

write_mem = 1
address = {tag_out, index_in, 000}
offset_out = 000

WB1

write_mem = 1
address = {tag_out, index_in, 010}
offset_out = 010

WB2

write_mem = 1
address = {tag_out, index_in, 100}
offset_out = 100

WB3

write_mem = 1
address = {tag_out, index_in, 110}
offset_out = 110

ALLOC0

read_mem = 1
address = {tag_in, index, 000}

ALLOC1

read_mem = 1
address = {tag_in, index, 010}

ALLOC2

read_mem = 1
address = {tag_in, index, 100}
write_cache = 1
offset_out = 000

ALLOC3

read_mem = 1
address = {tag_in, index, 110}
write_cache = 1
offset_out = 010

ALLOC4

write_cache = 1
offset_out = 100

ALLOC5

write_cache = 1
offset_out = 110
valid_out = 1

CACHE_HANDLER

write_cache = Wr
comp = 1
offset_out = offset_in

FINAL

done = 1
offset_out = offset_in

Transitions:
- (~(Rd | Wr)) | ((Rd | Wr) & valid_in & hit)
- rst
- (Rd | Wr) & (valid_in & ~hit & dirty)
- ((Rd | Wr) & (valid_in & ~hit & ~dirty)) | ((Rd | Wr) & ~valid_in)
- ~stall
- stall

Default Outputs & State

nxt_state = curr_state
stall_out = 1
write_cache = 0
read_mem = 0
address = 0000
offset_out = 000
err = 0
write_mem = 0
enable = 1
cache_hit - 0
valid_out = 0
done = 0
comp = 0