Program NeuRA SS25

Day 1 (29.09.2025 – Start 9:00 – Room 07.150-113):

Session FPGA (HLS & NoC):

- **Hemkendreis, Jonas**: FPGA HLS Today: Successes, Challenges, and Opportunities
- **Potsch, Philipp**: AutoBridge - Coupling Coarse-Grained Floorplanning and Pipelining for High-Frequency HLS Design
- **Egelmeier, Maximilian**: AXI HyperConnect - A Predictable, Hypervisor-level Interconnect for Hardware Accelerators in FPGA SoC
- **Heither, Dustin**: Flexible and Efficient QoS Provisioning in AXI4-Based Network-on-Chip Architecture

Session Machine Learning Hardware:

- **Kalchuk, Illya**: The Design Process for Google's Training Chips: TPUv2 and TPUv3
- **Warter, Cedric**: TPU v4: An Optically Reconfigurable Supercomputer for Machine Learning with Hardware Support for Embeddings
- **Döring, Paul**: Cerebras Architecture Deep Dive: First Look inside the Hardware/Software Co-Design for Deep Learning
- **Schmidt, Leonard**: Approximate Computing: A Survey

Day 2 (30.09.2025 – Start 9:30 – Room 07.150-113):

Session In-Memory Computing:

- **Wiegel, Bela**: Memory Devices and Applications for In-Memory Computing
- **Rußer, Sebastian**: Algorithm Hardware Co-Design for ADC-Less Compute-In-Memory Accelerator
- **Bhuiyan, Md Nur Hossain**: A Logic-Compatible eDRAM Compute-In-Memory with Embedded ADCs for Processing Neural Networks
- **Ramachandran, Aswin**: ISAAC - A Convolutional Neural Network Accelerator with In-Situ Analog Arithmetic in Crossbars