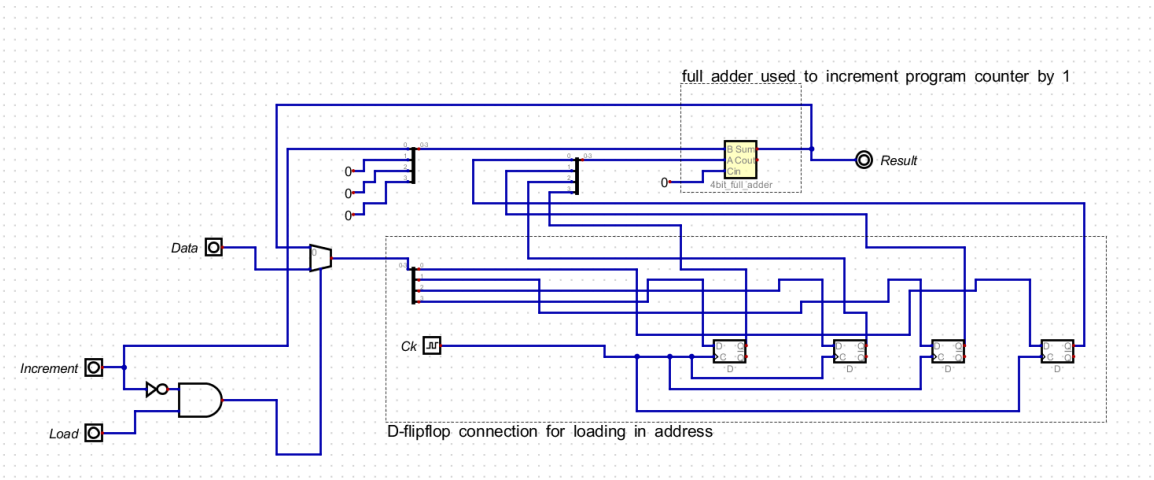
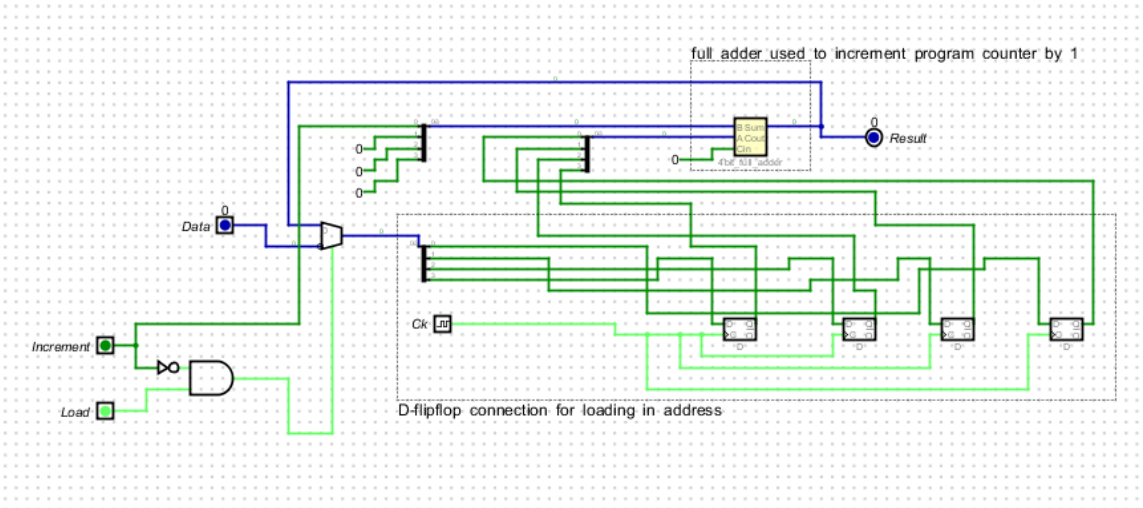
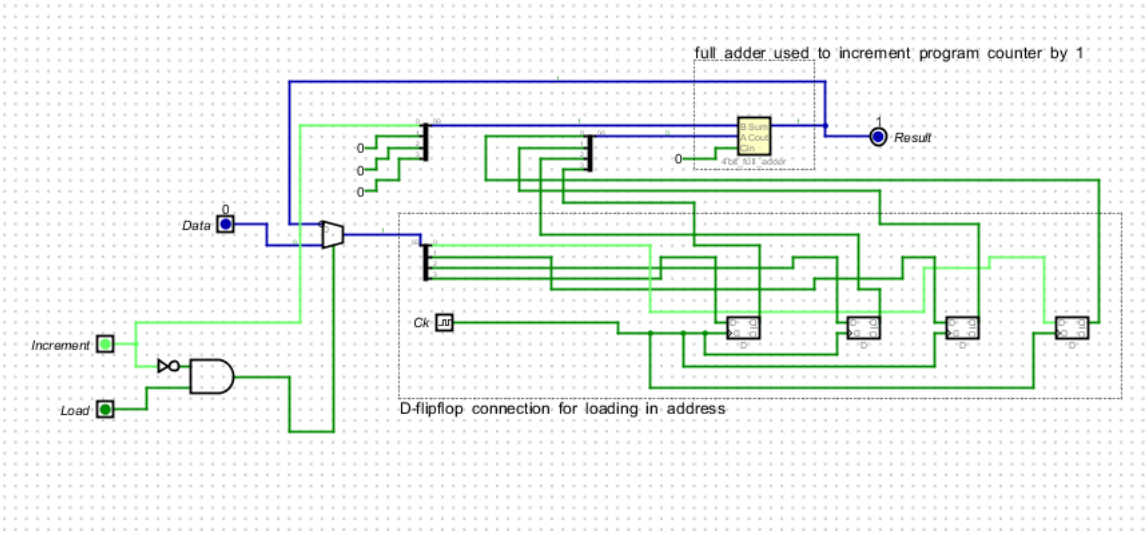
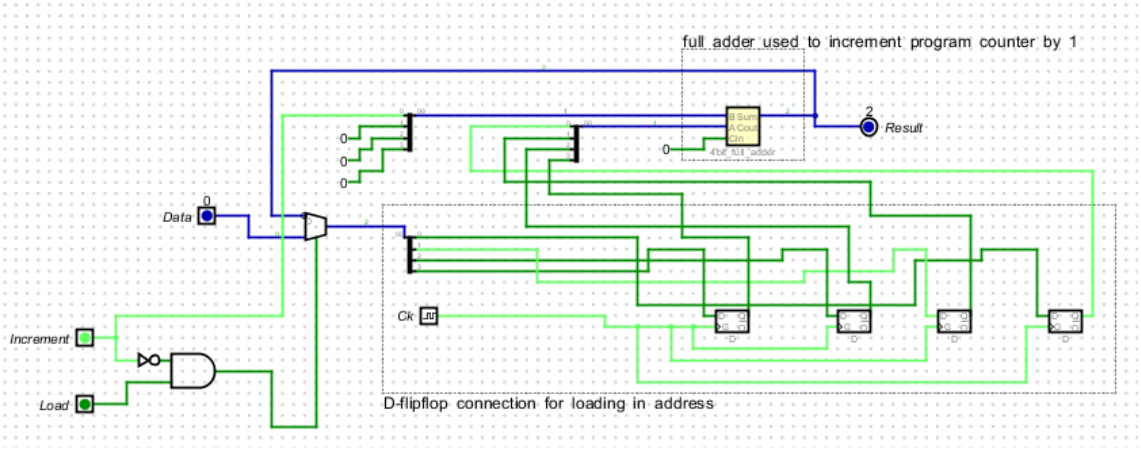
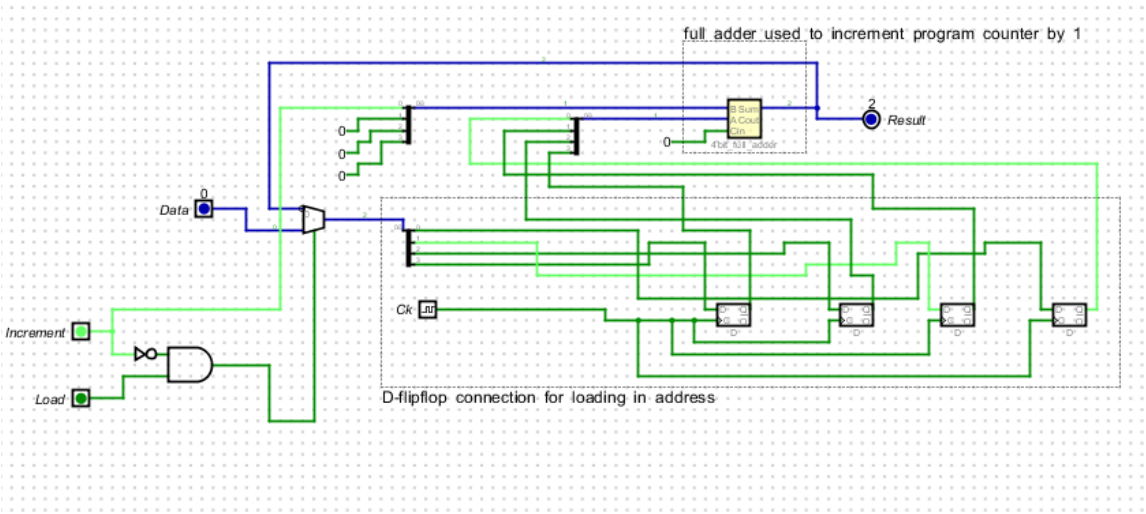
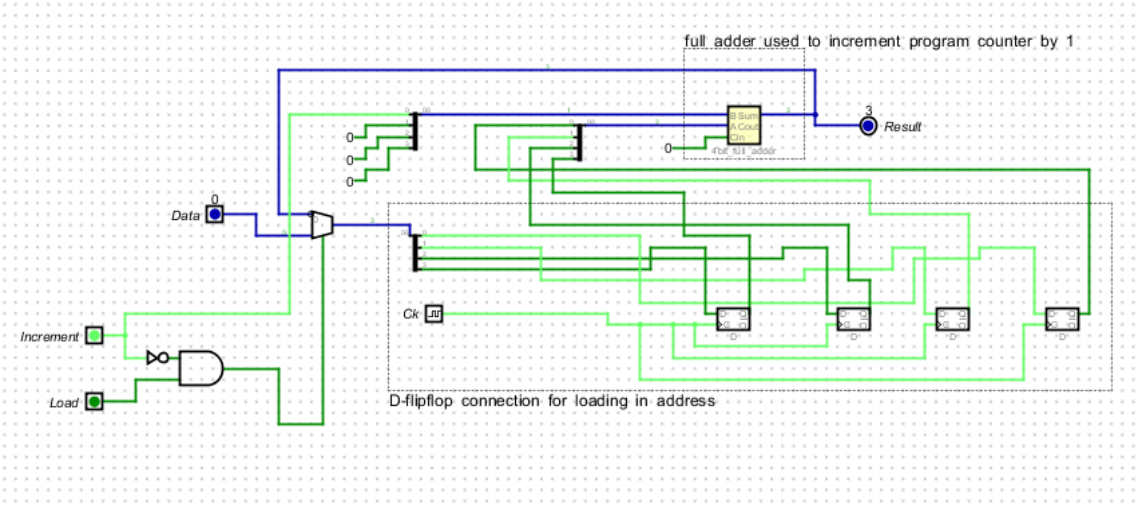
Test Tables

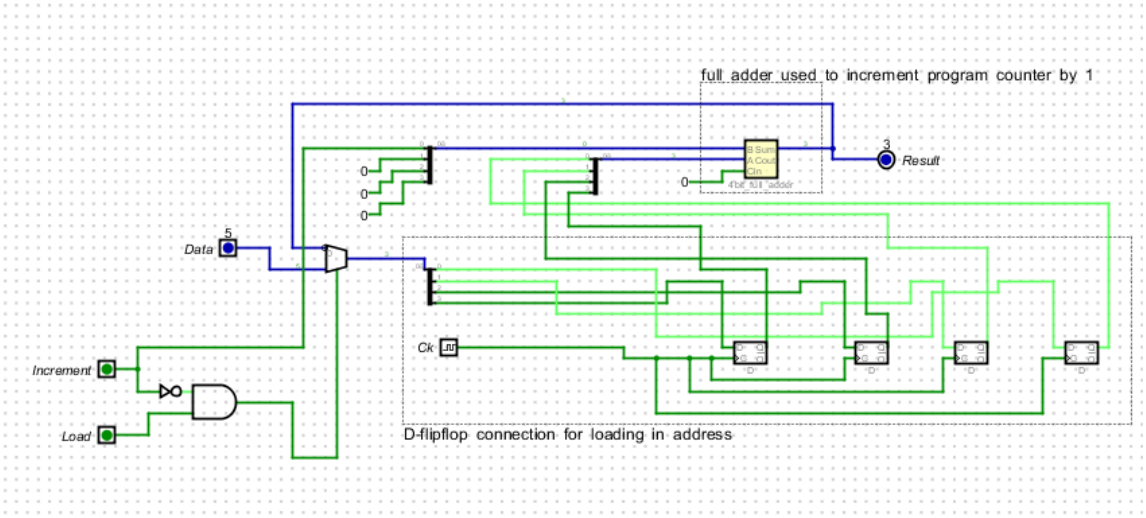
Program Counter Circuit	
Program Counter load turned on	
Program counter Increment turned on	Clock Cycle 1:



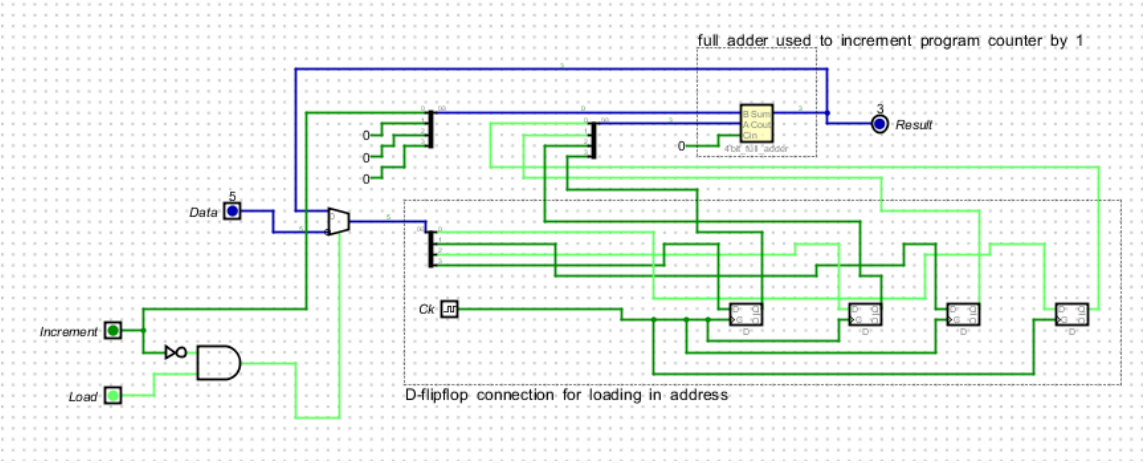


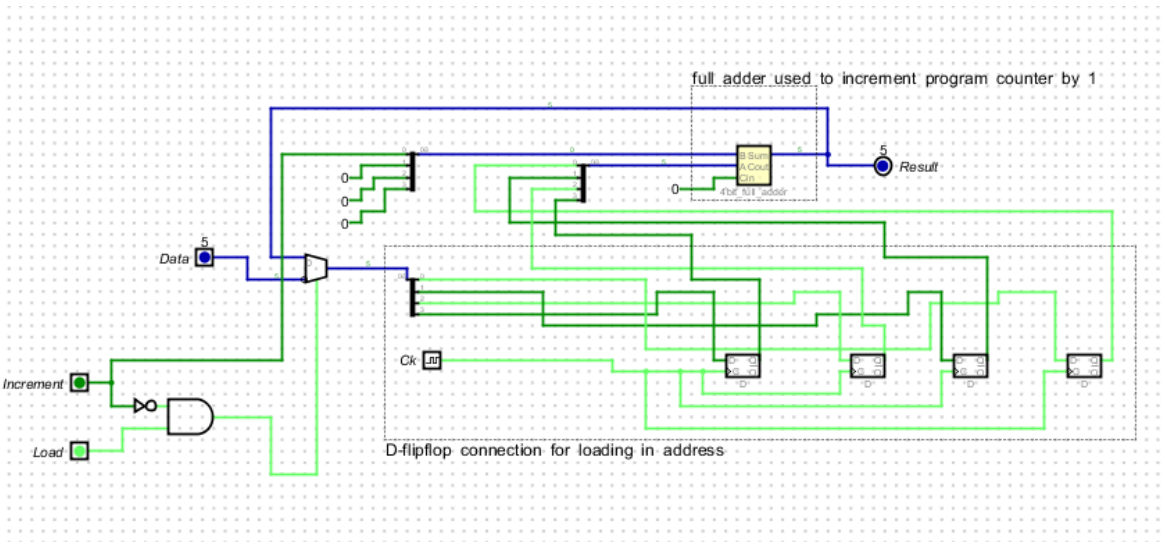
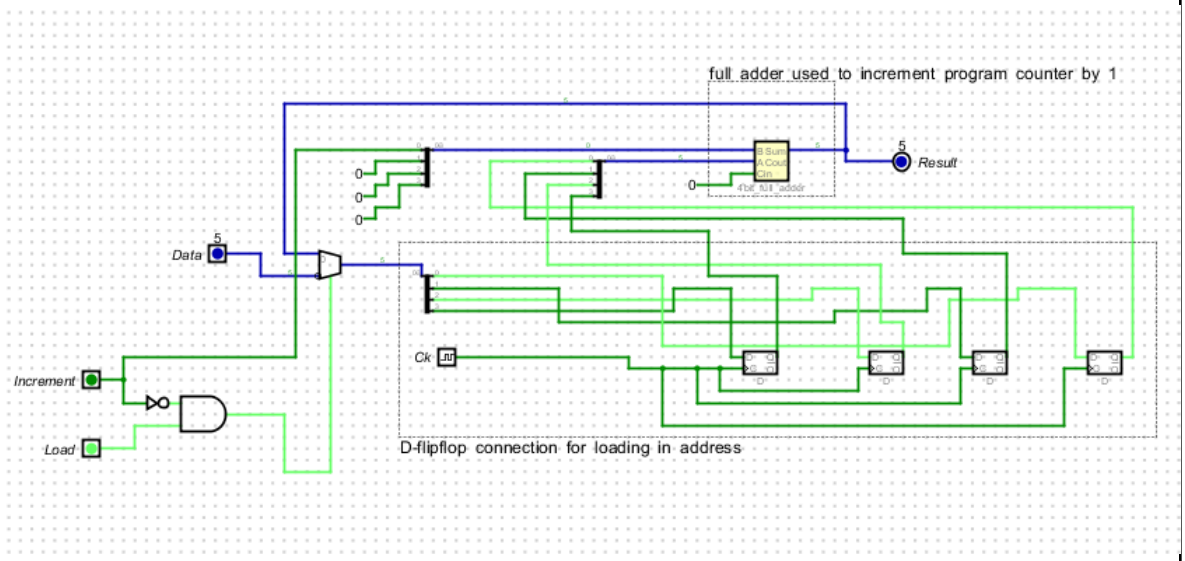
Clock Cycle 2:

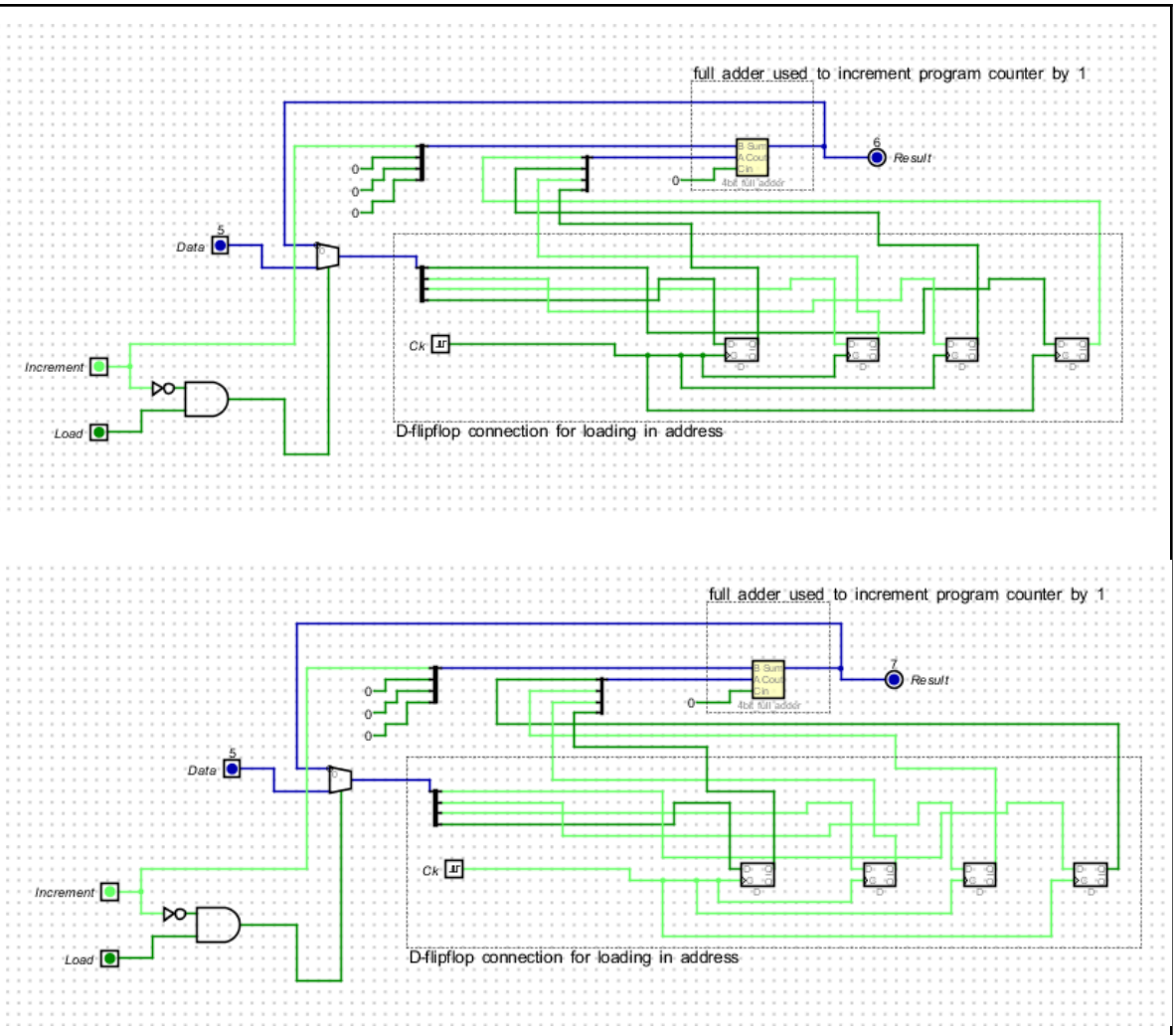
	 
New Data Entry Load	start:

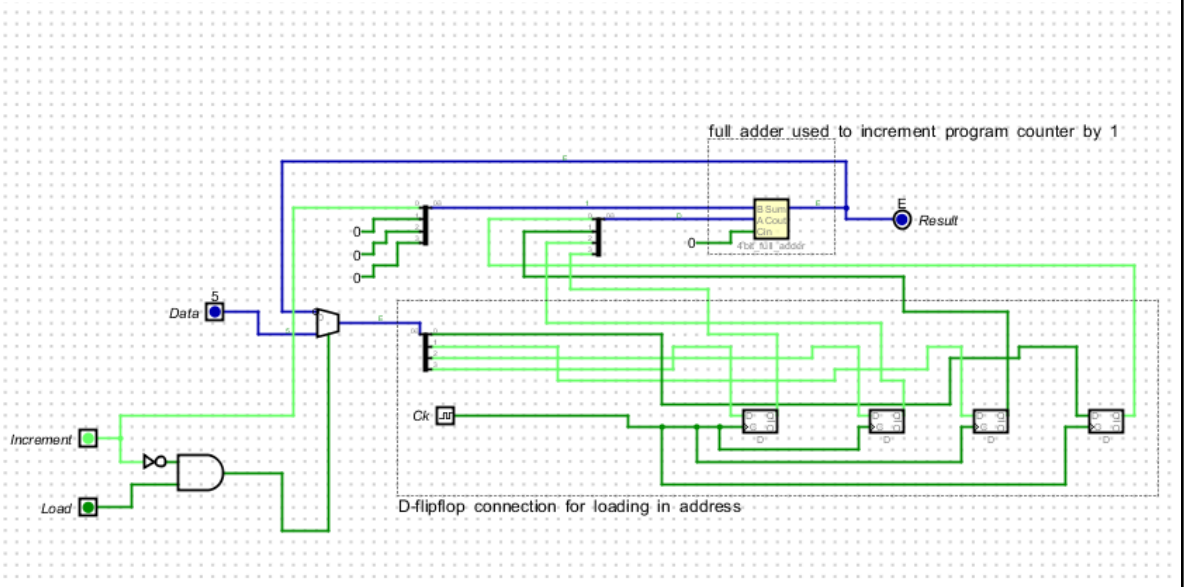


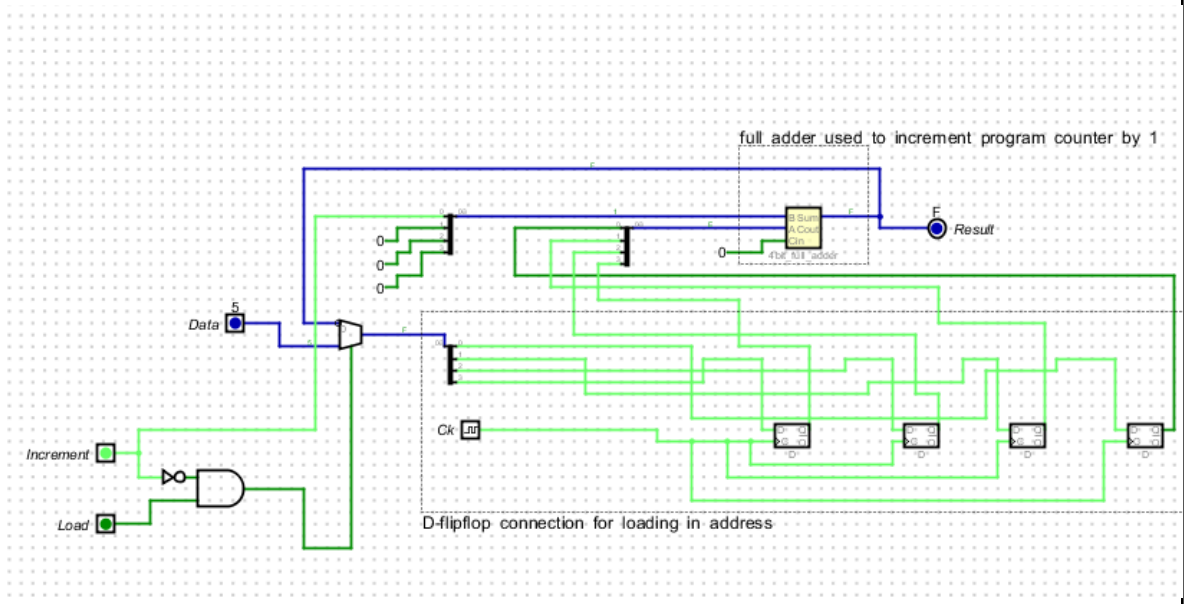
Clock Cycle 1:



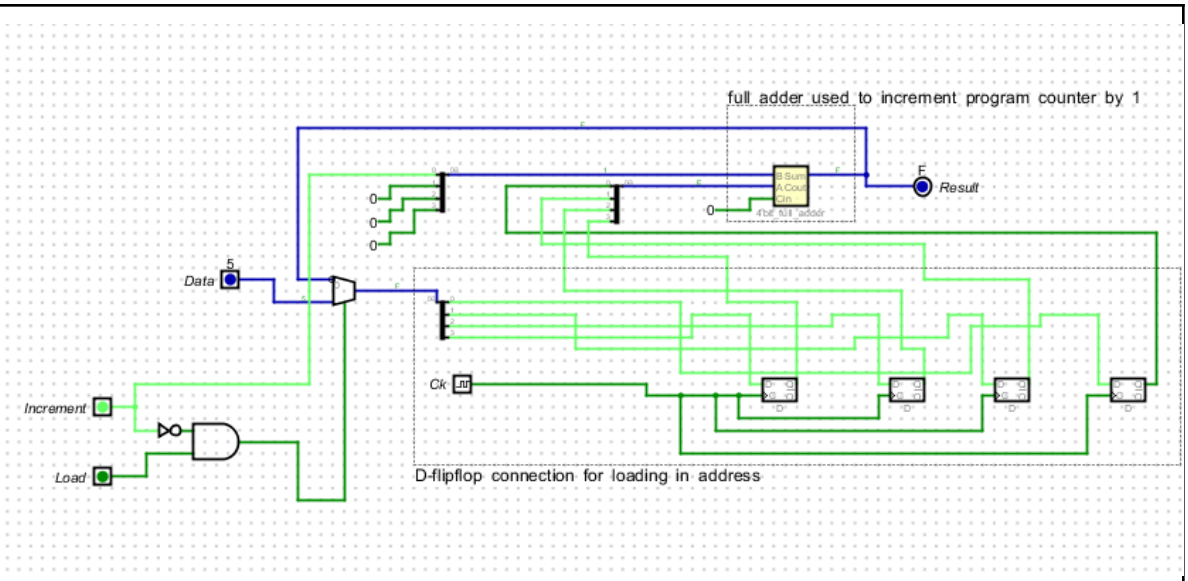
	 end: 
New entry Increment	Clock Cycle 1:

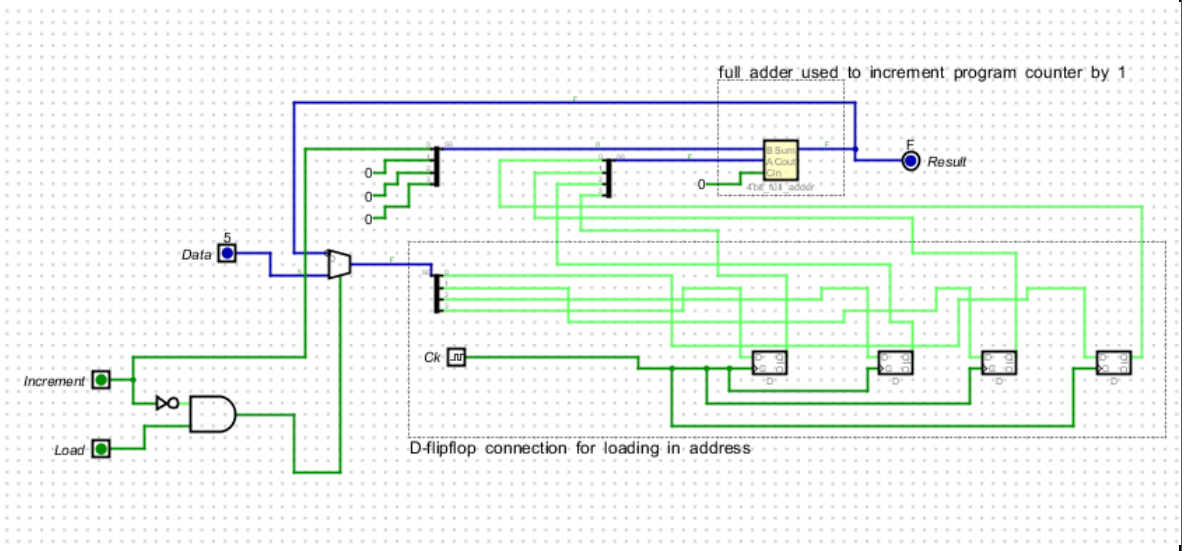
	
Pointer Counter bounded at 16 (increment)	Clock Cycle 1:

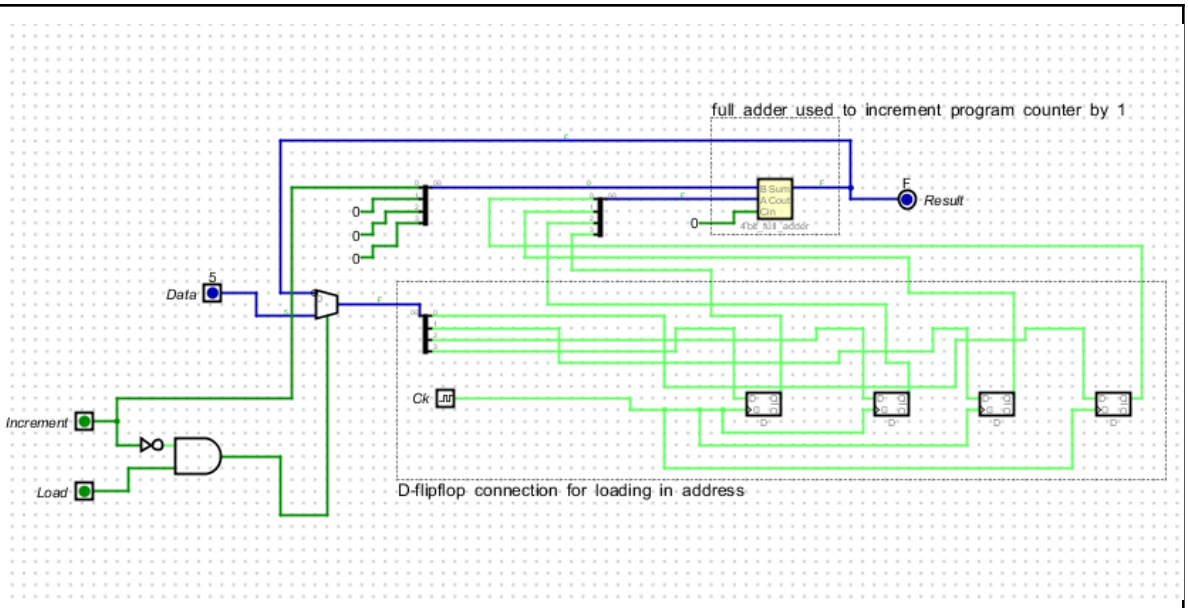




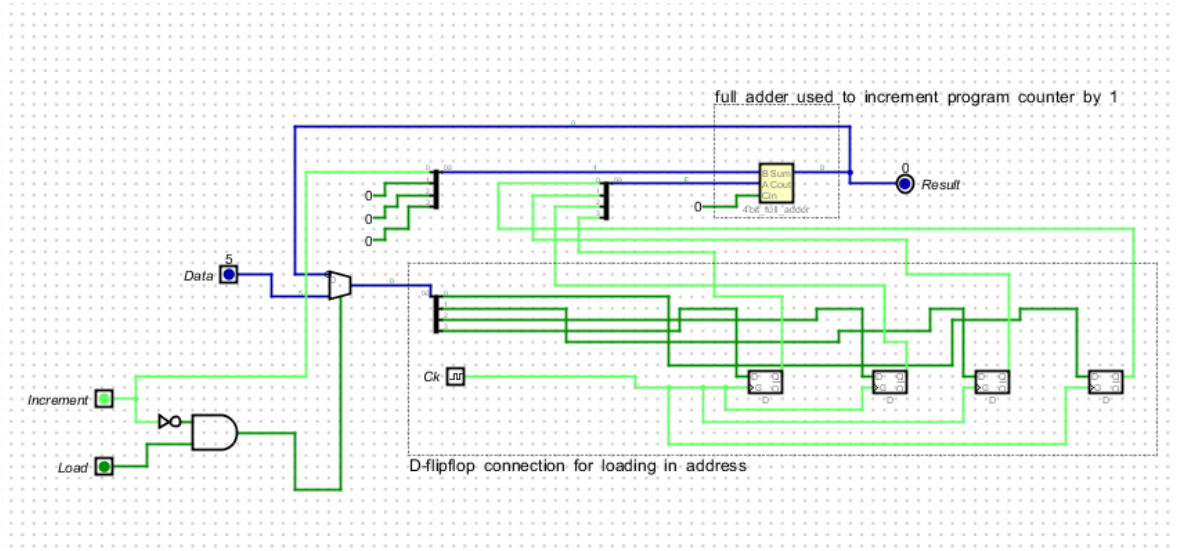
Clock Cycle 2:

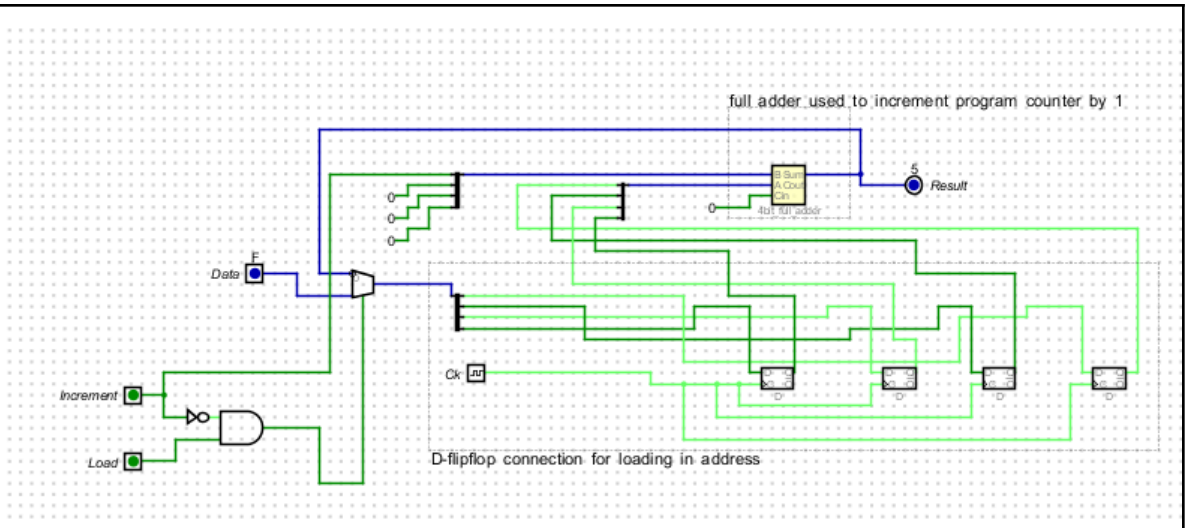
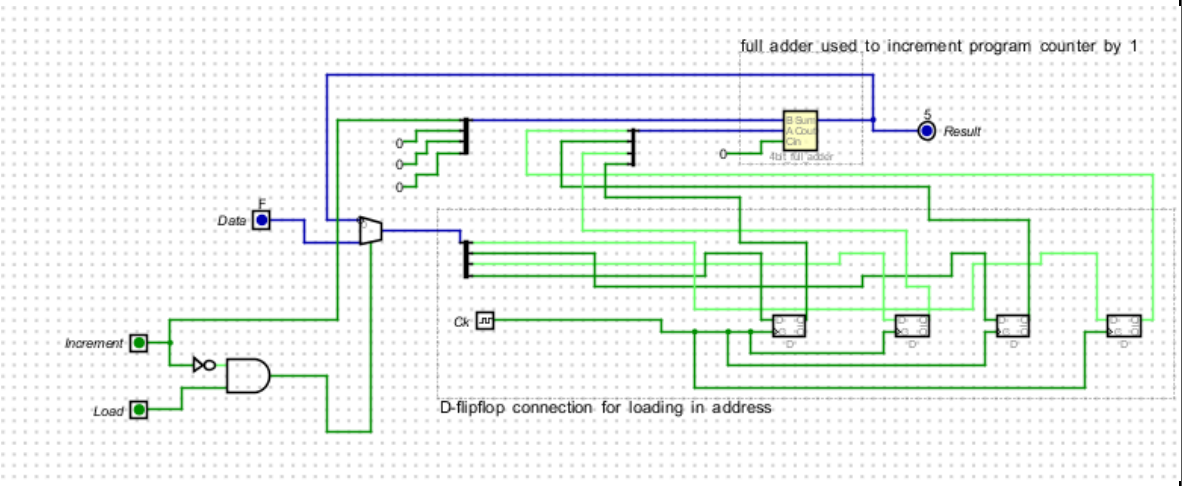

full adder used to increment program counter by 1
Result
Data
Increment
Load
Ck
D-flipflop connection for loading in address

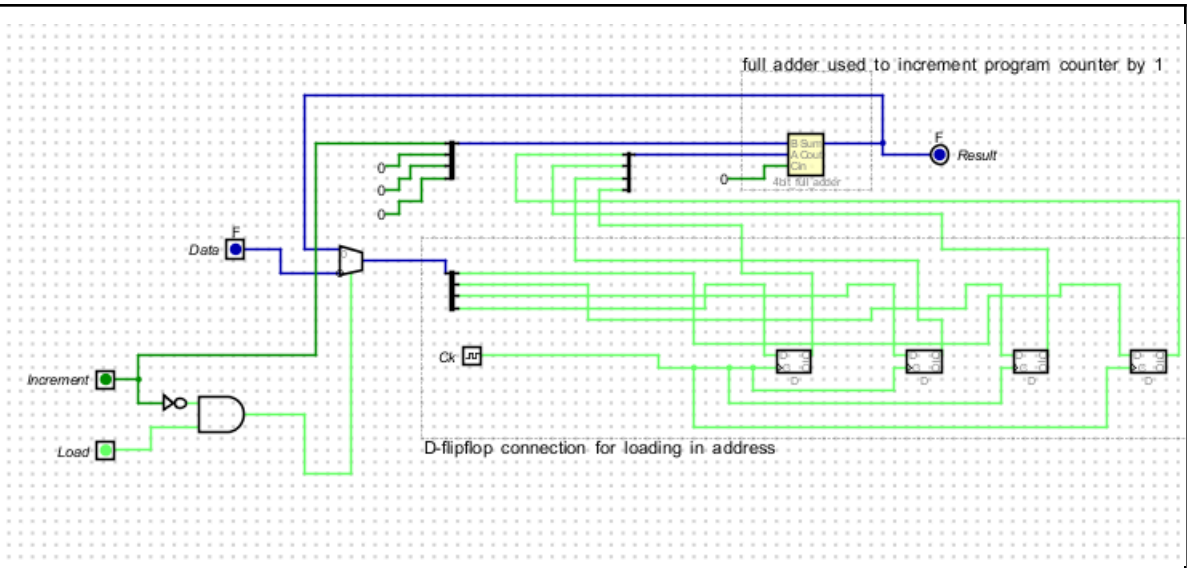

full adder used to increment program counter by 1
Result
Data
Increment
Load
Ck
D-flipflop connection for loading in address

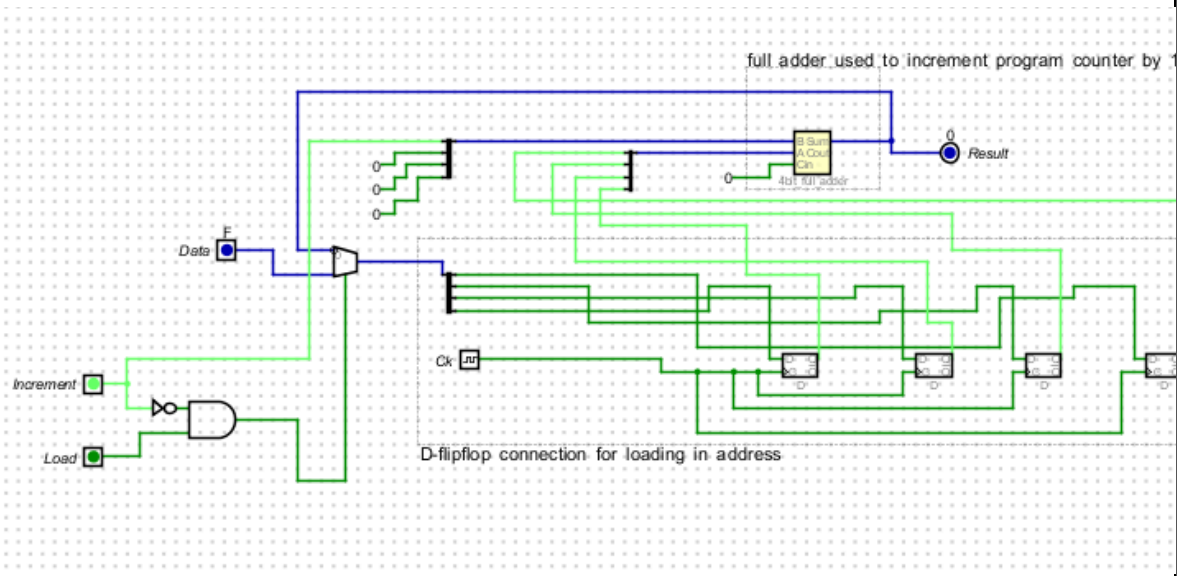


Clock Cycle 3:

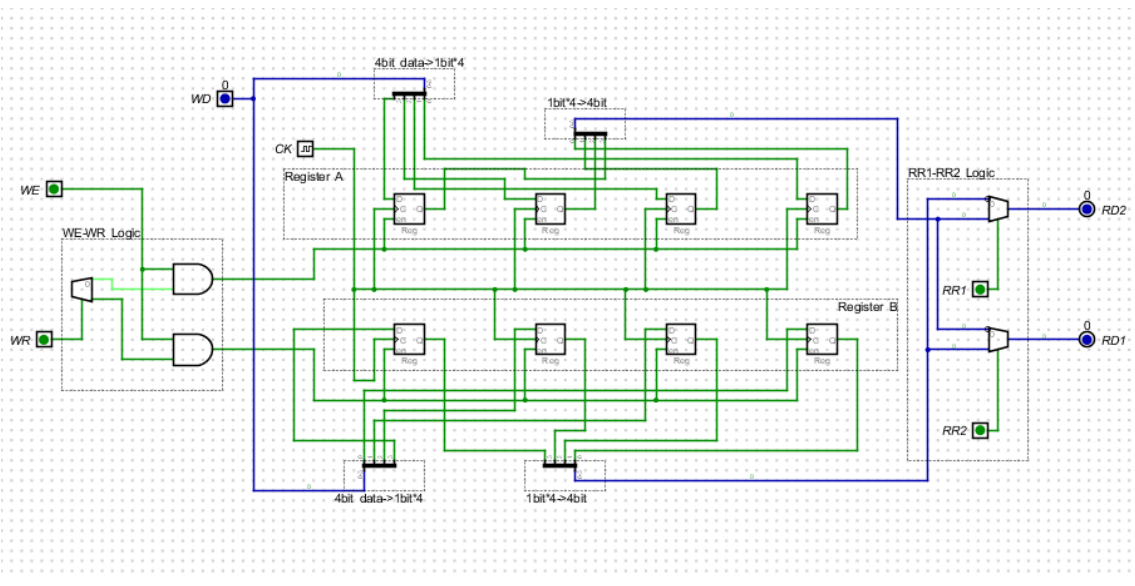
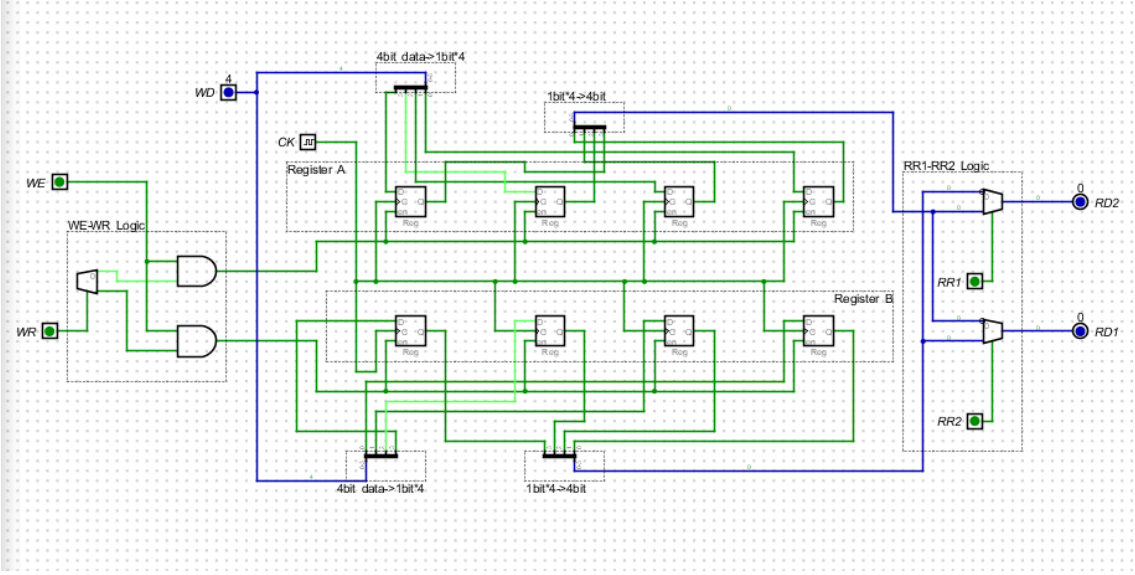


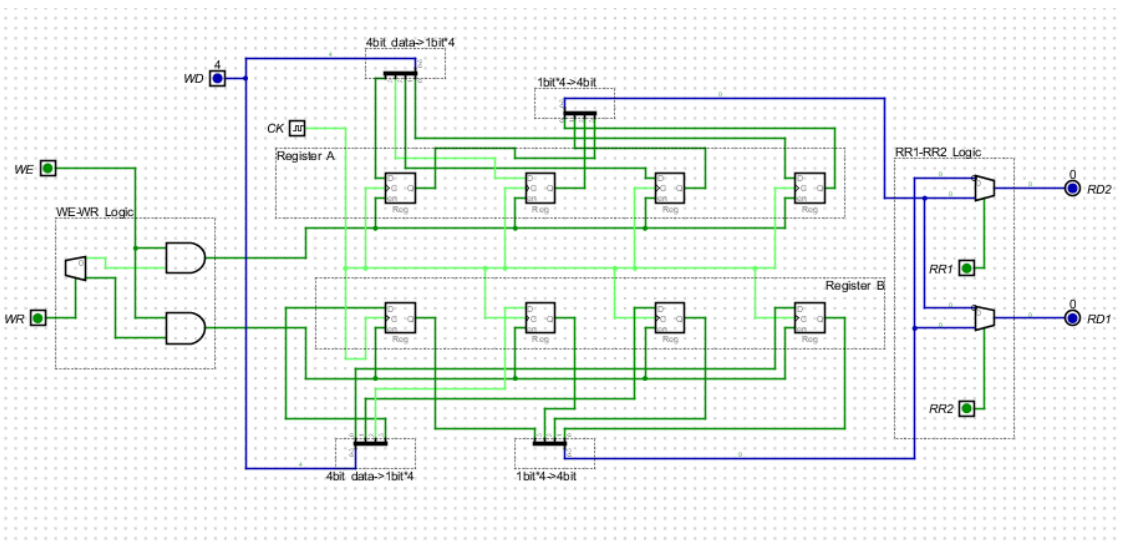
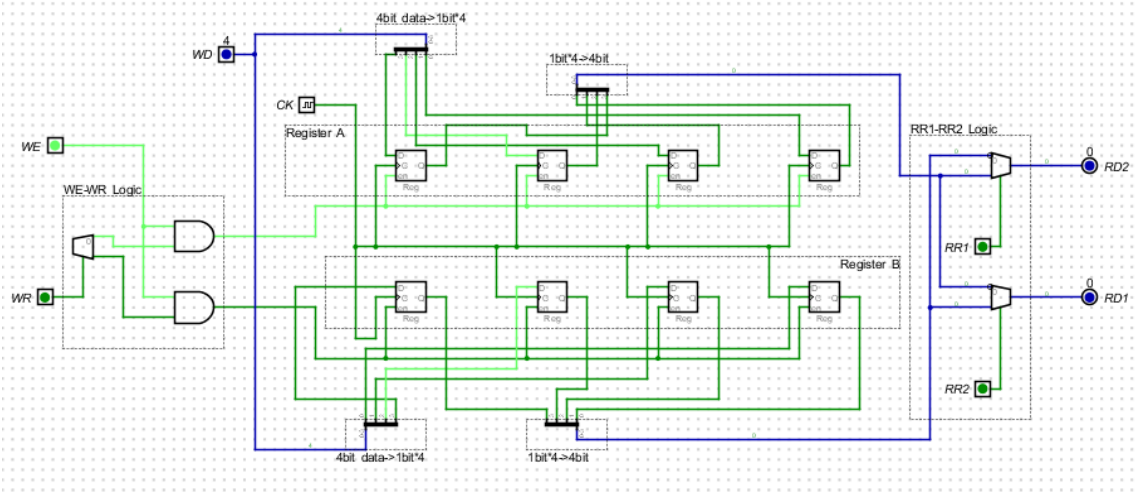
Pointer Counter bounded at 16 (Load)	 Clock Cycle 1: 

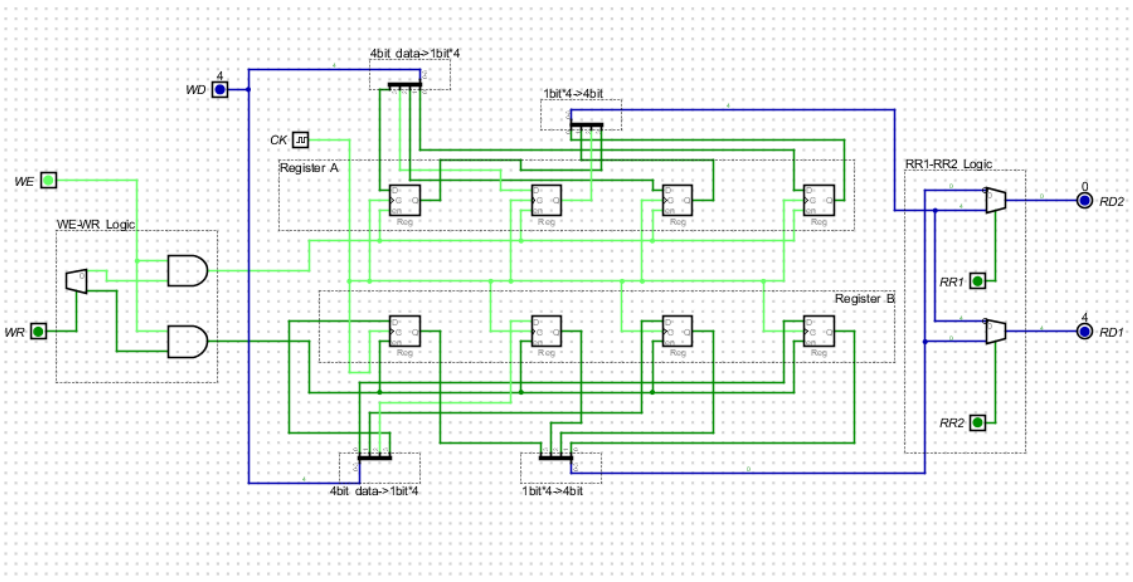
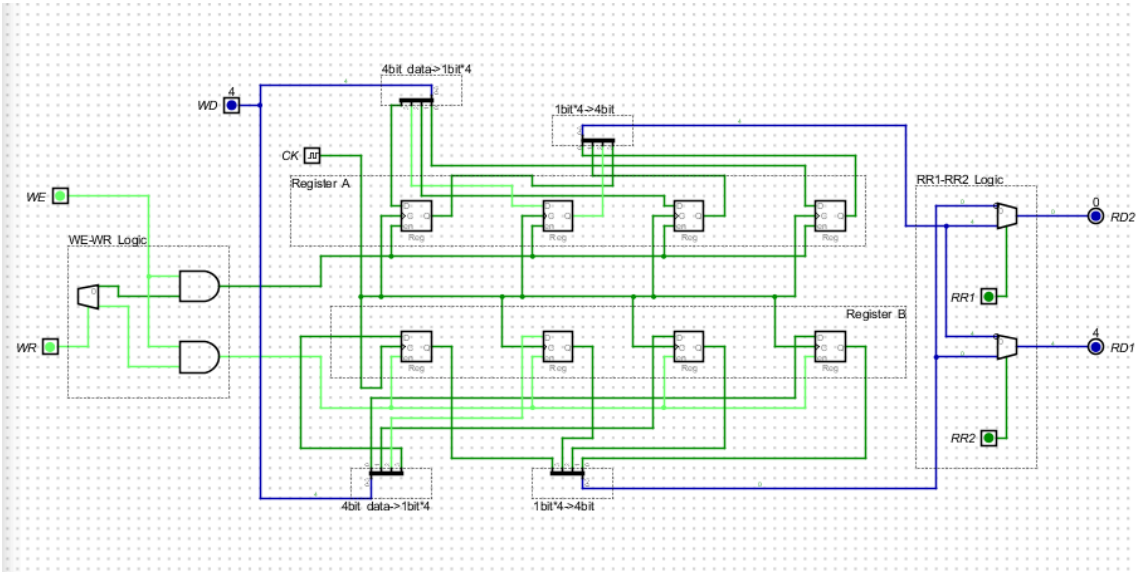


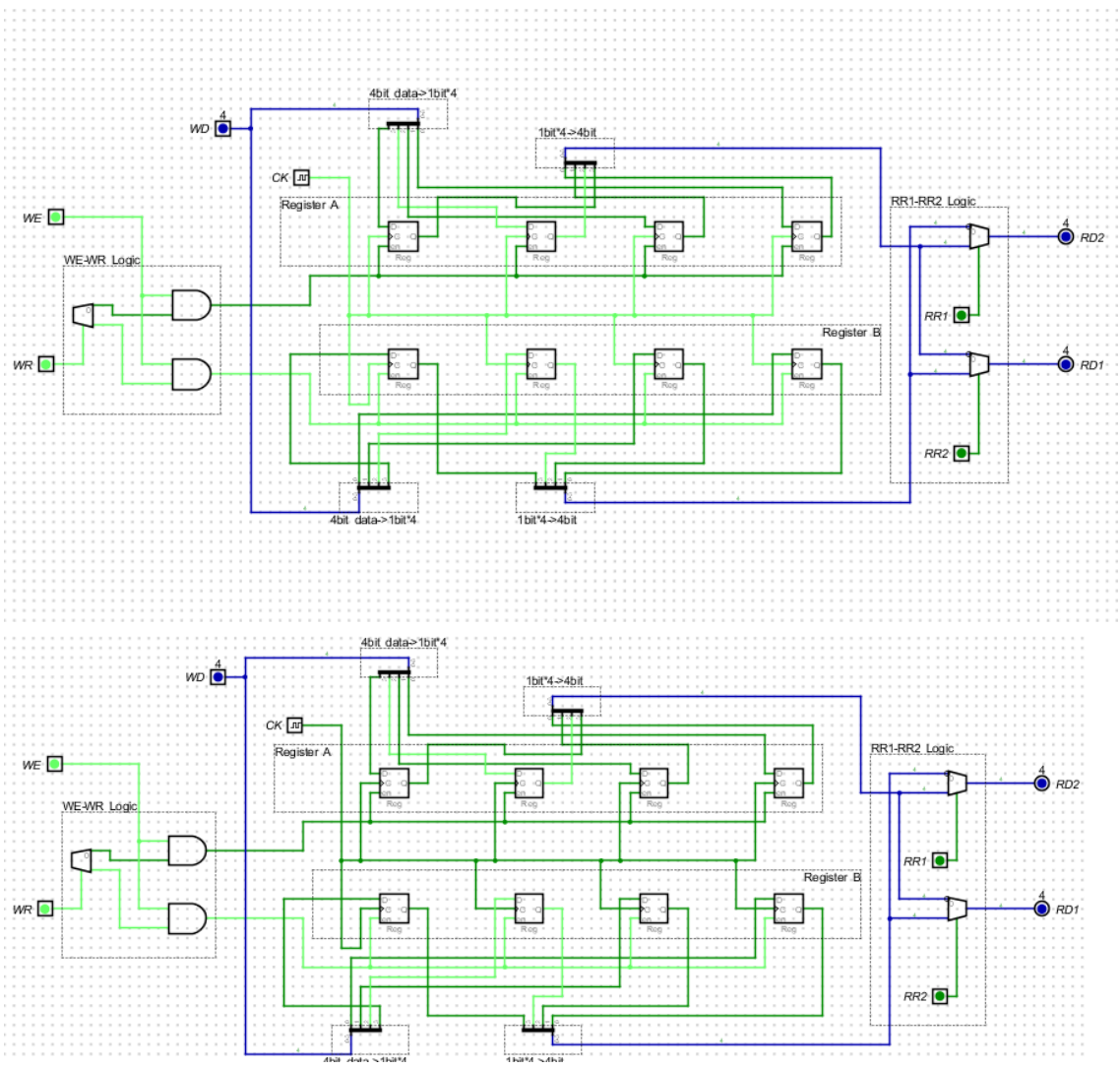
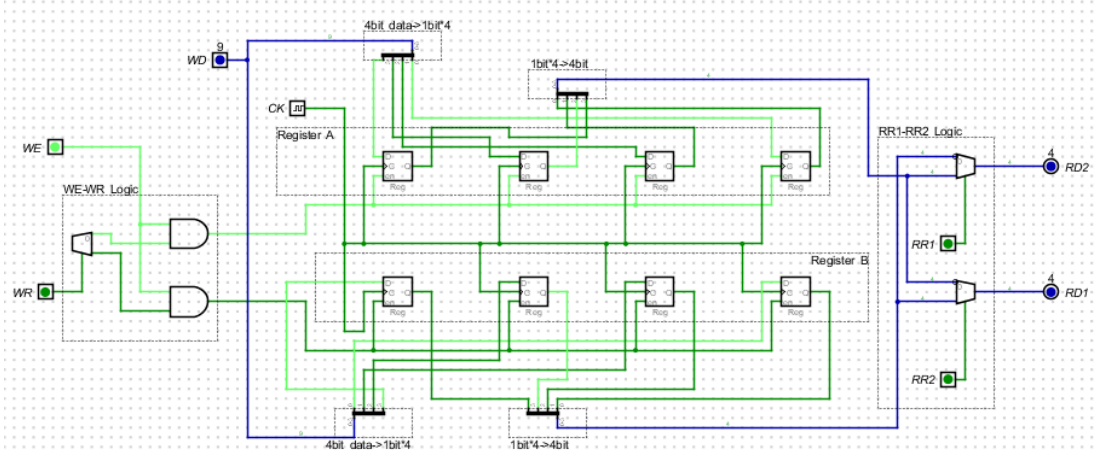


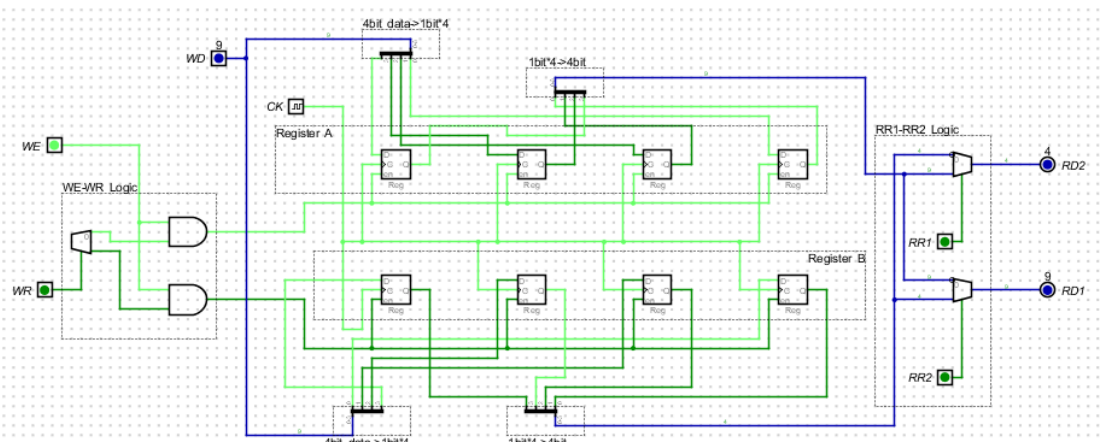
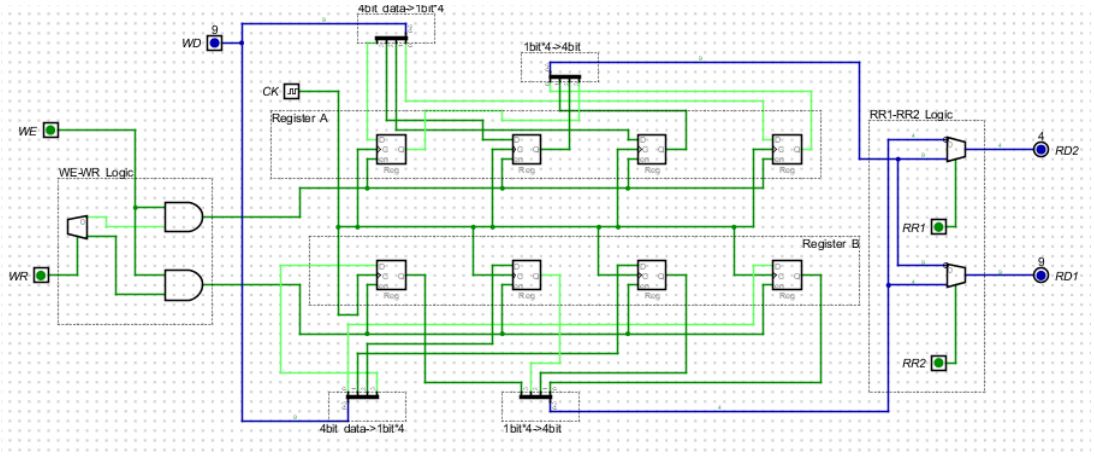
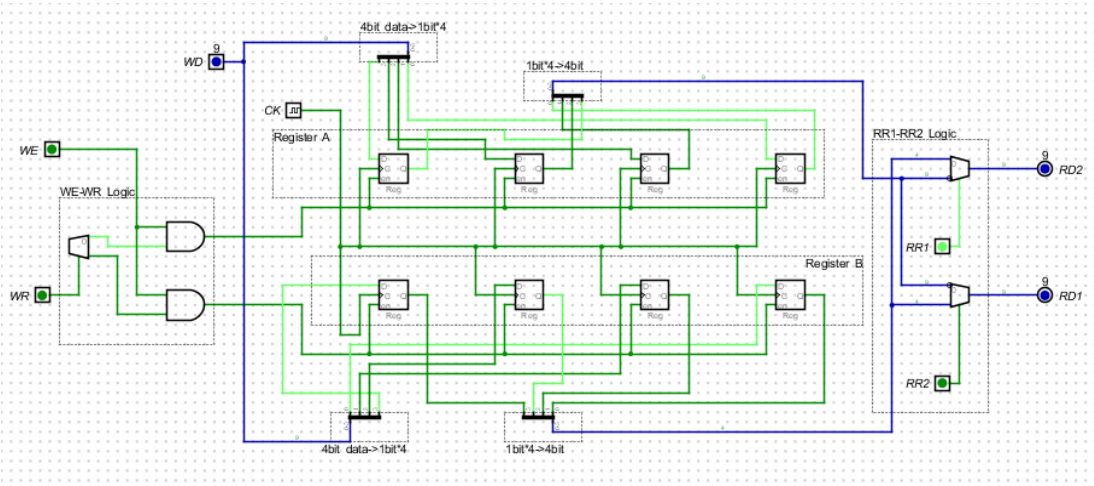
Register File:

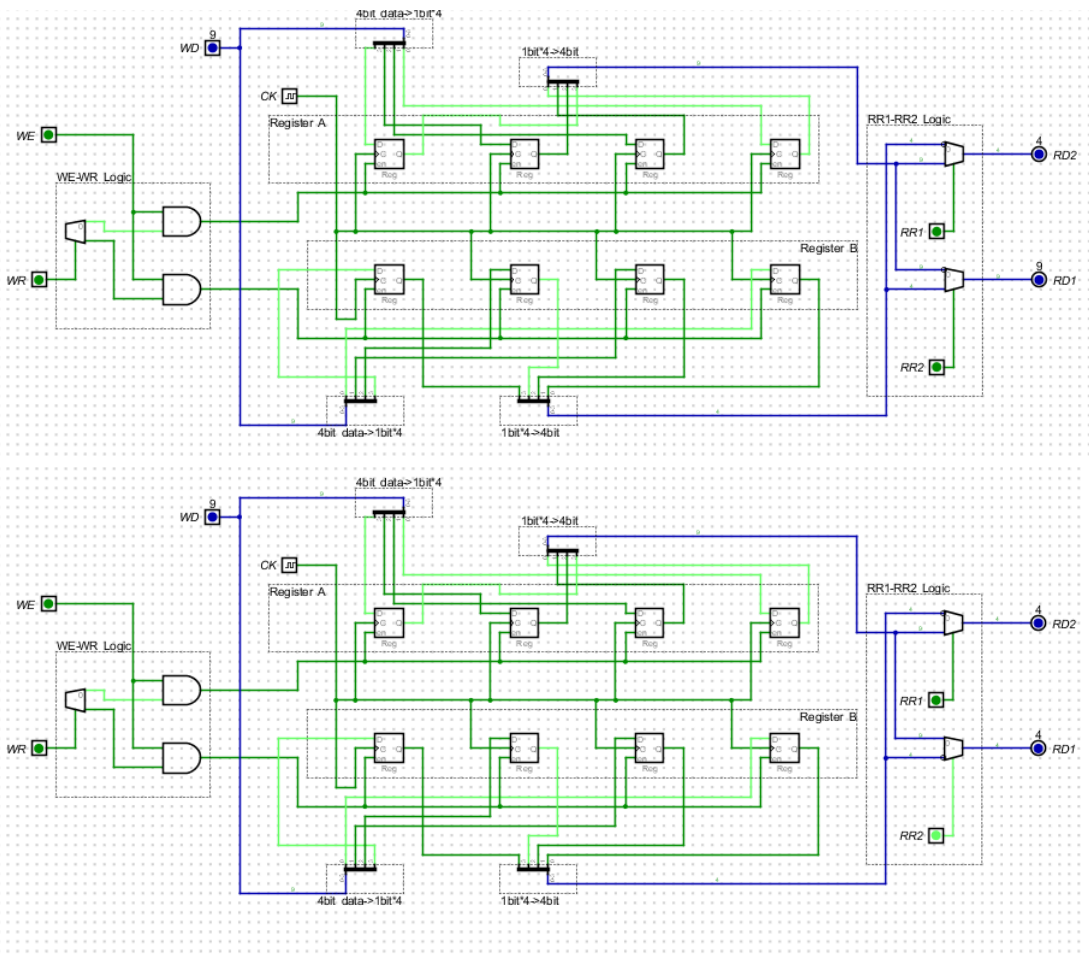
The circuit working	
Inputting data into Write Data	Clock Cycle 1: 

	
Turning on Write enable	Clock Cycle 1: 

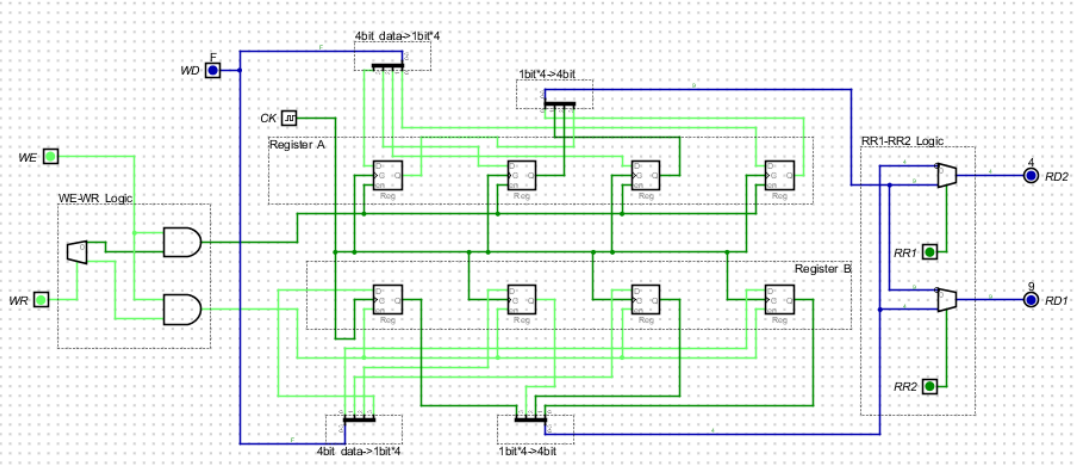
	
Turning on Write register and write enable	Clock Cycle 1: 

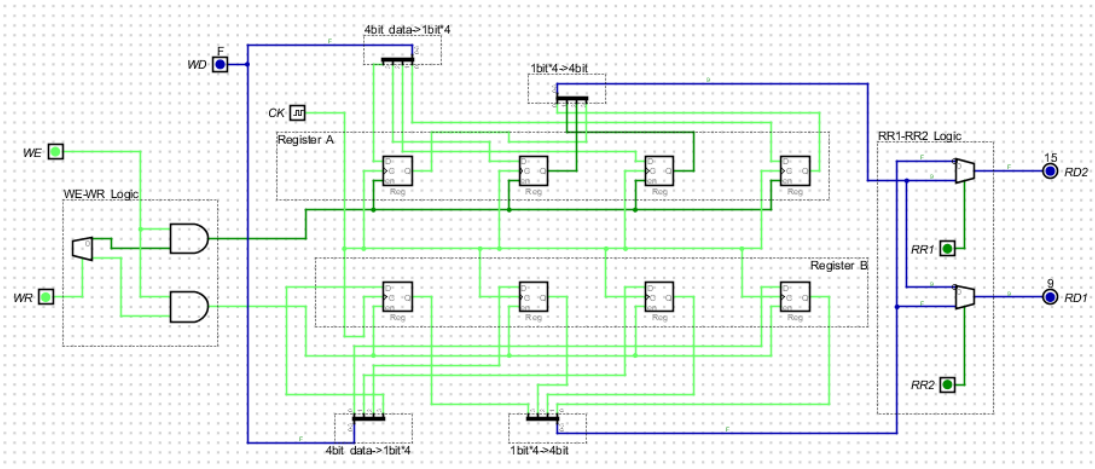
	
Inputting new data into Write Data	Clock Cycle 1: 

	
Read Register 1 is turned on:	 Clock Cycle 1: 
Read Register 2 is turned on:	Clock Cycle 1:

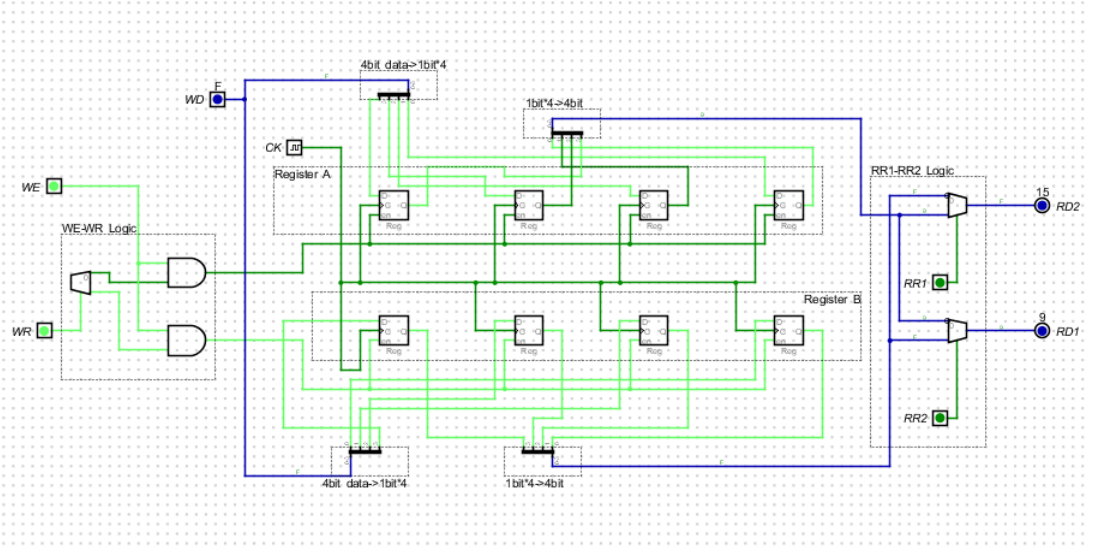


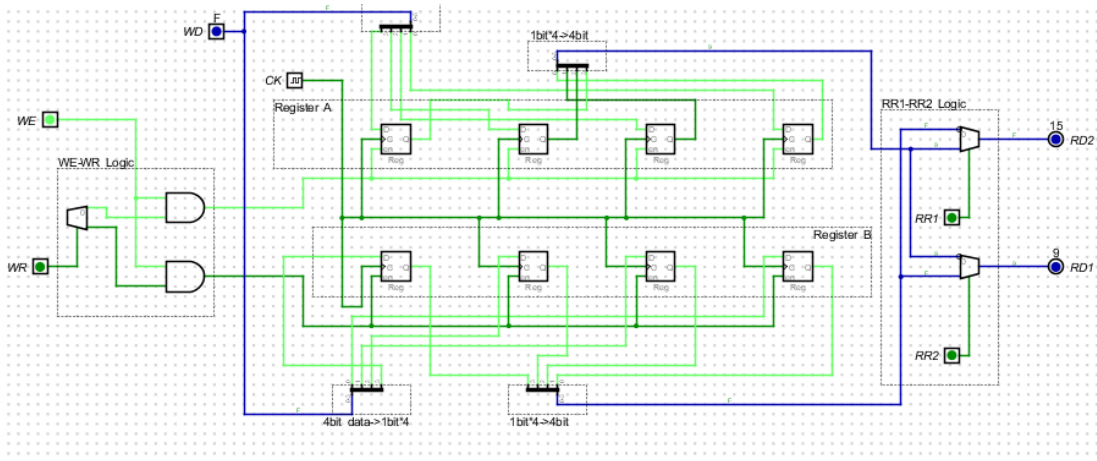
Clock Cycle 1(Register B - Write register enabled):

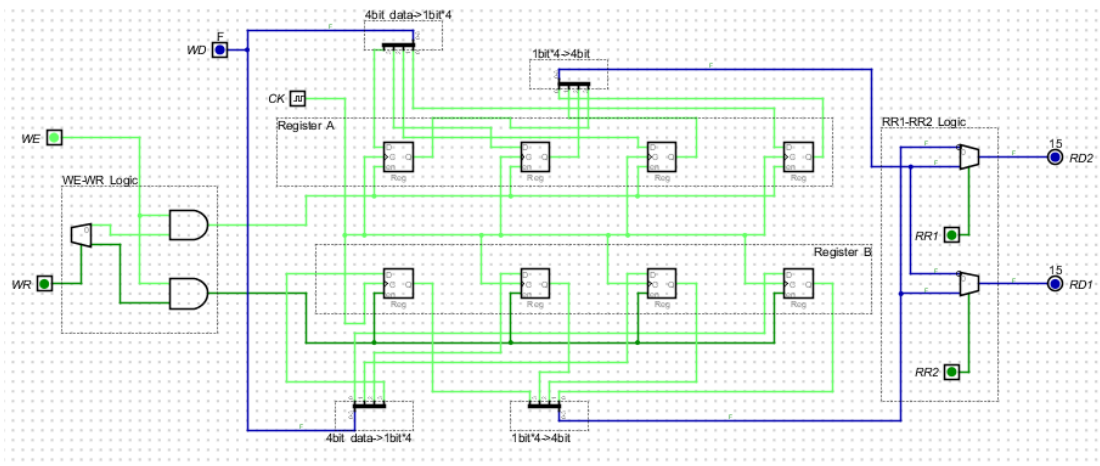




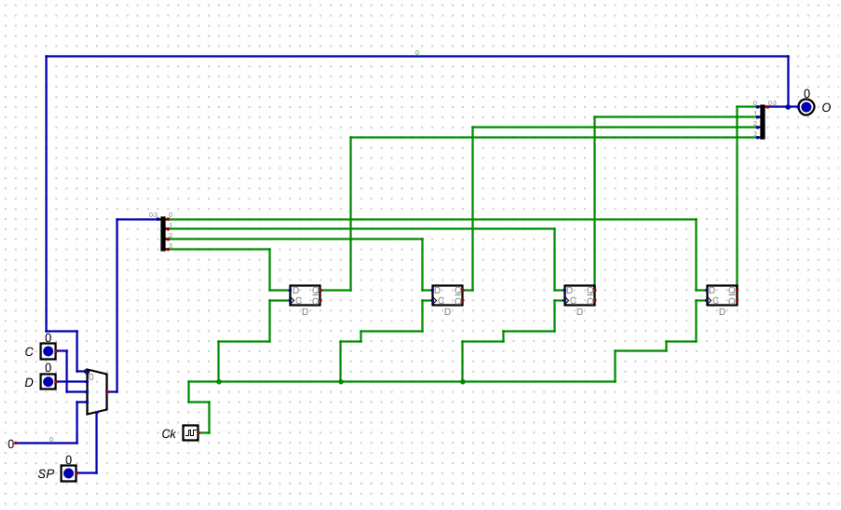
Clock Cycle 2(Register A - Write register not enabled):

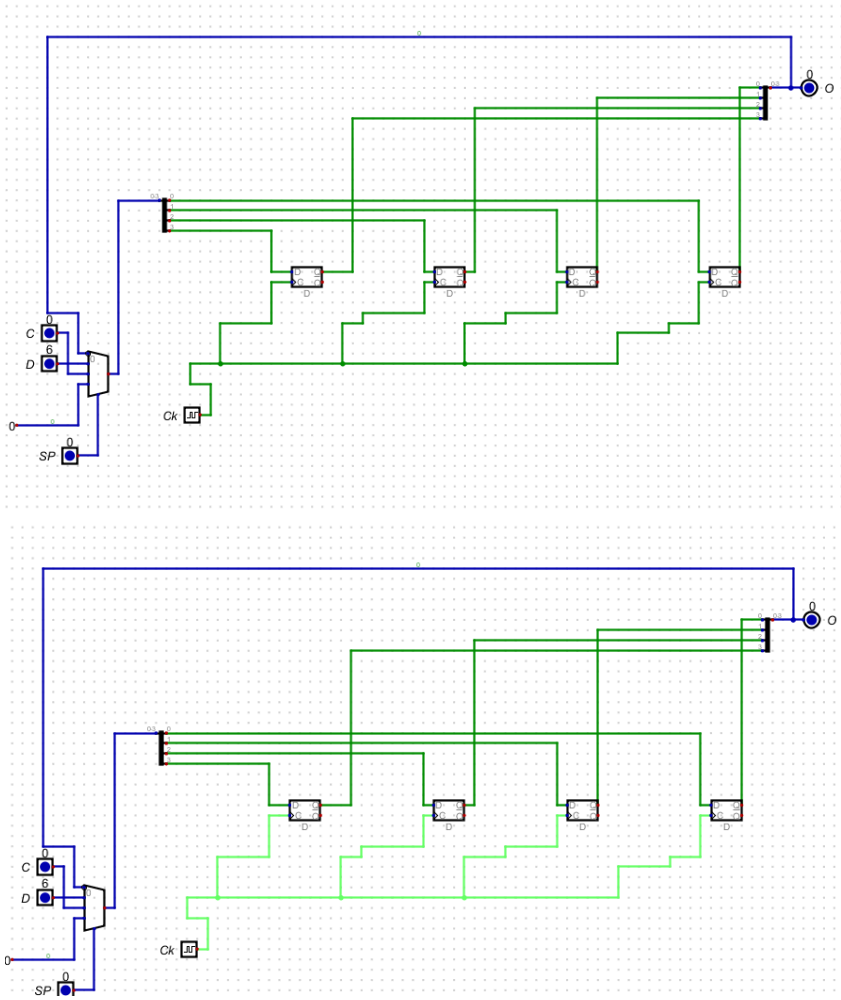




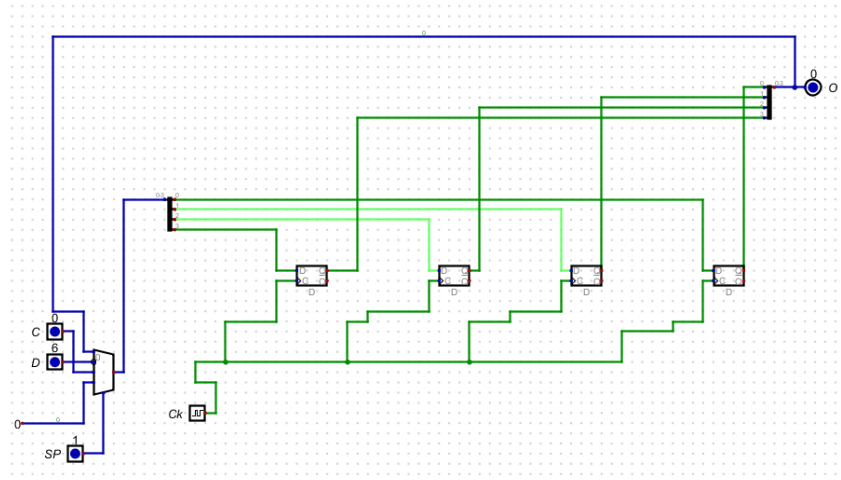
	

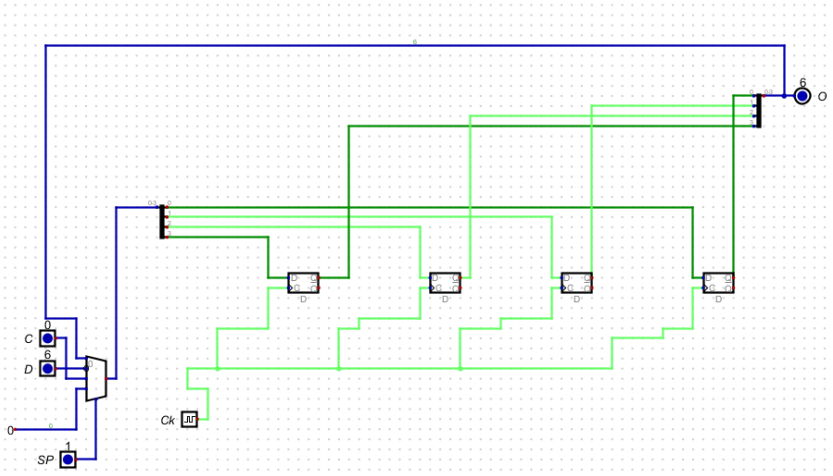
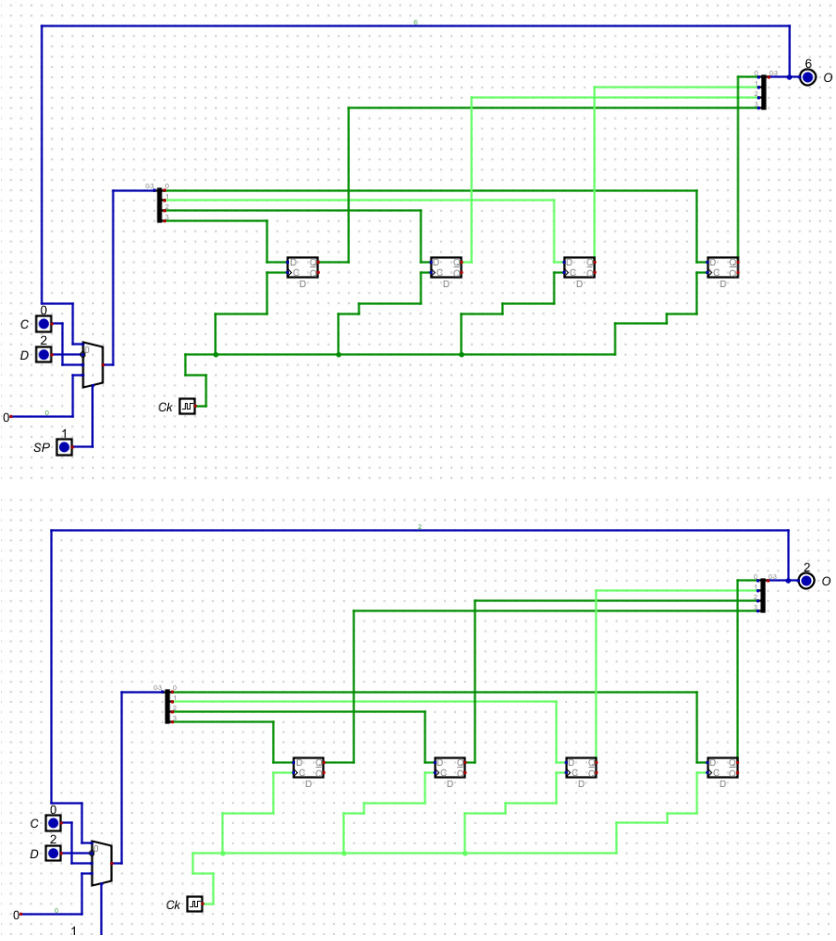
IR Register - A / B Register

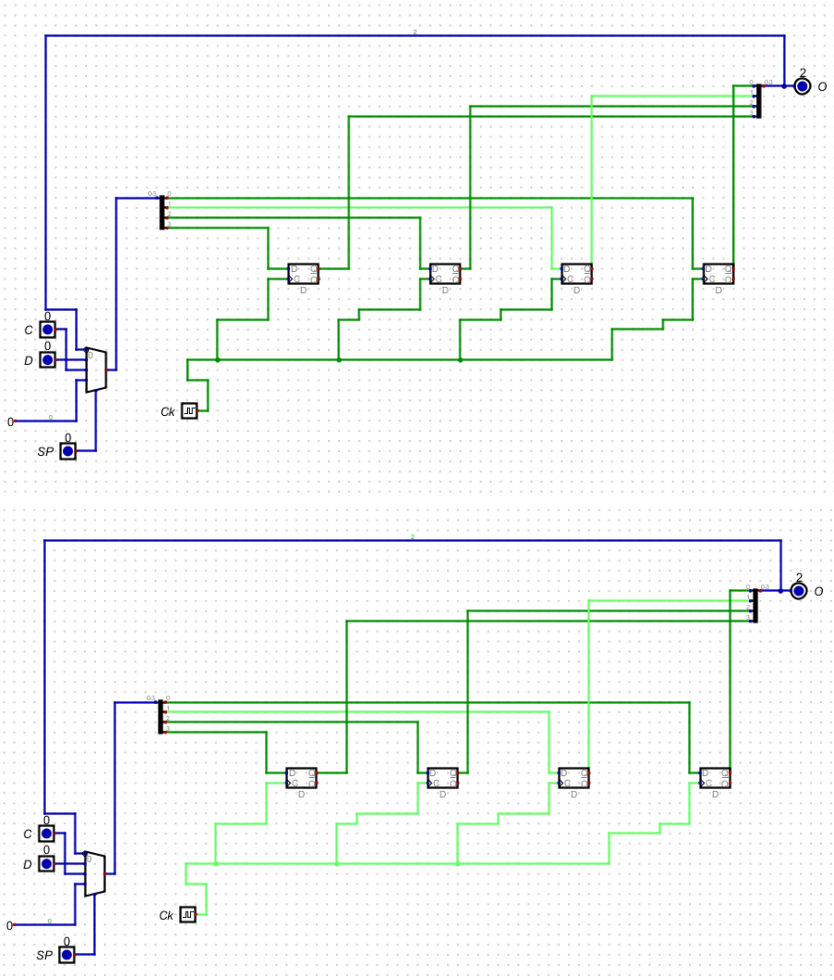
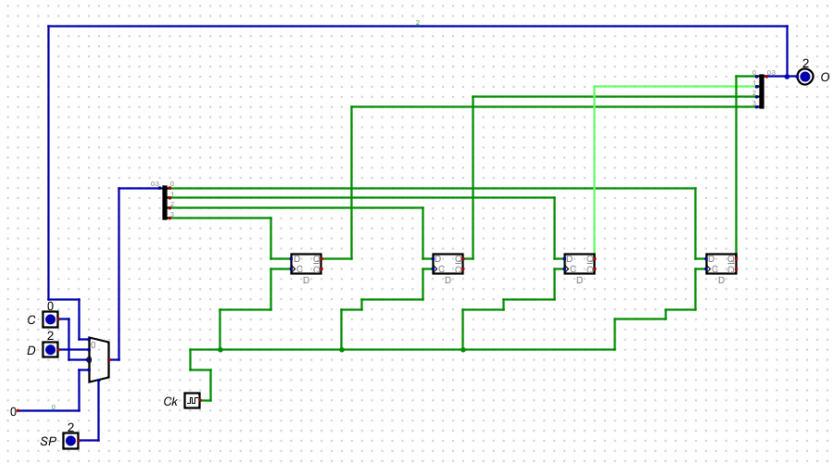
Register on	
Inputting data, signal pin	Clock Cycle 1:

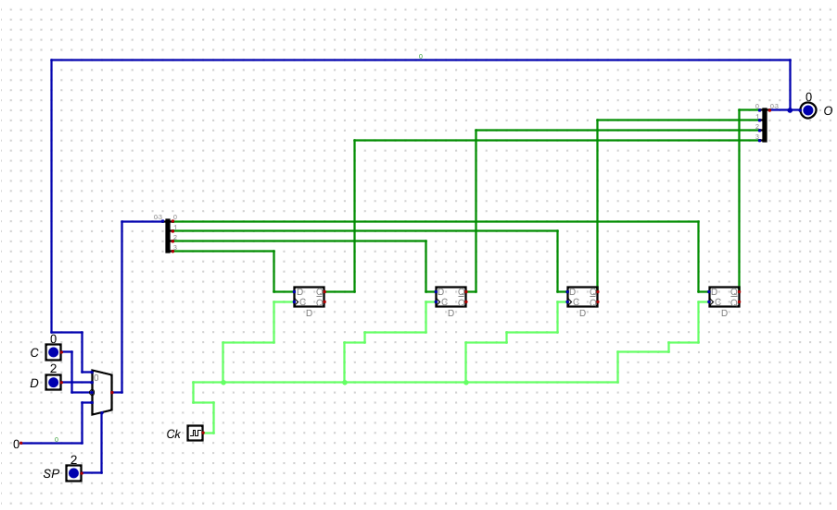
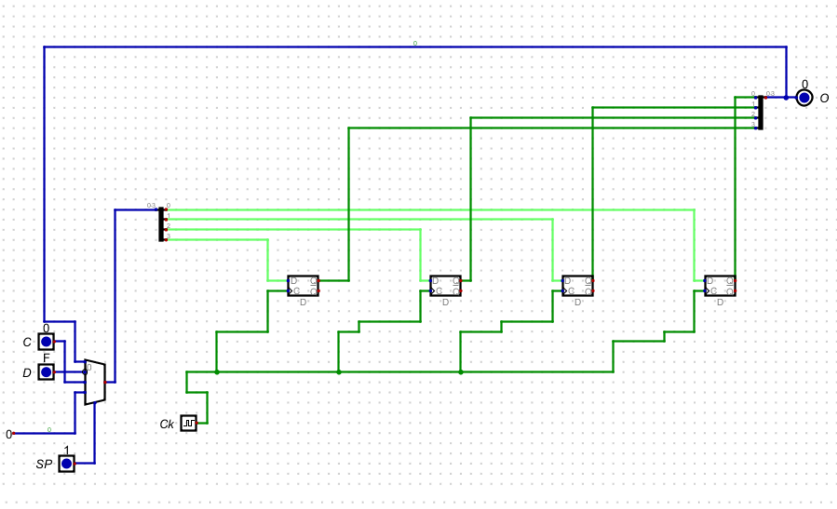
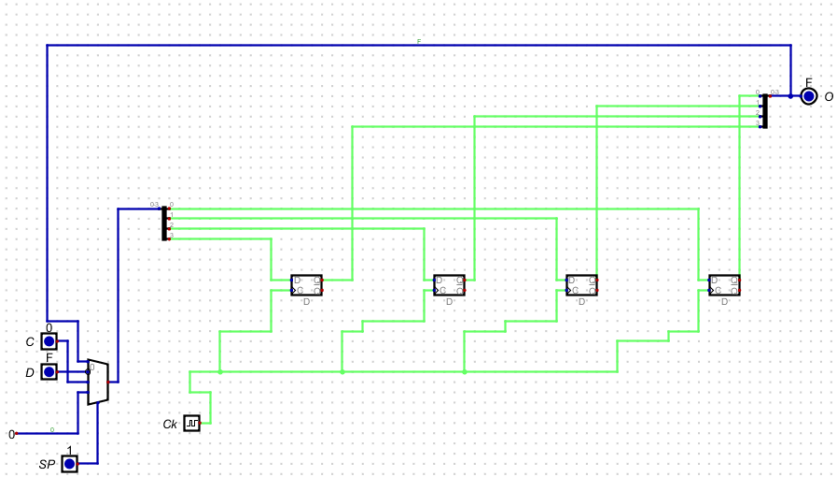


Clock Cycle 2:

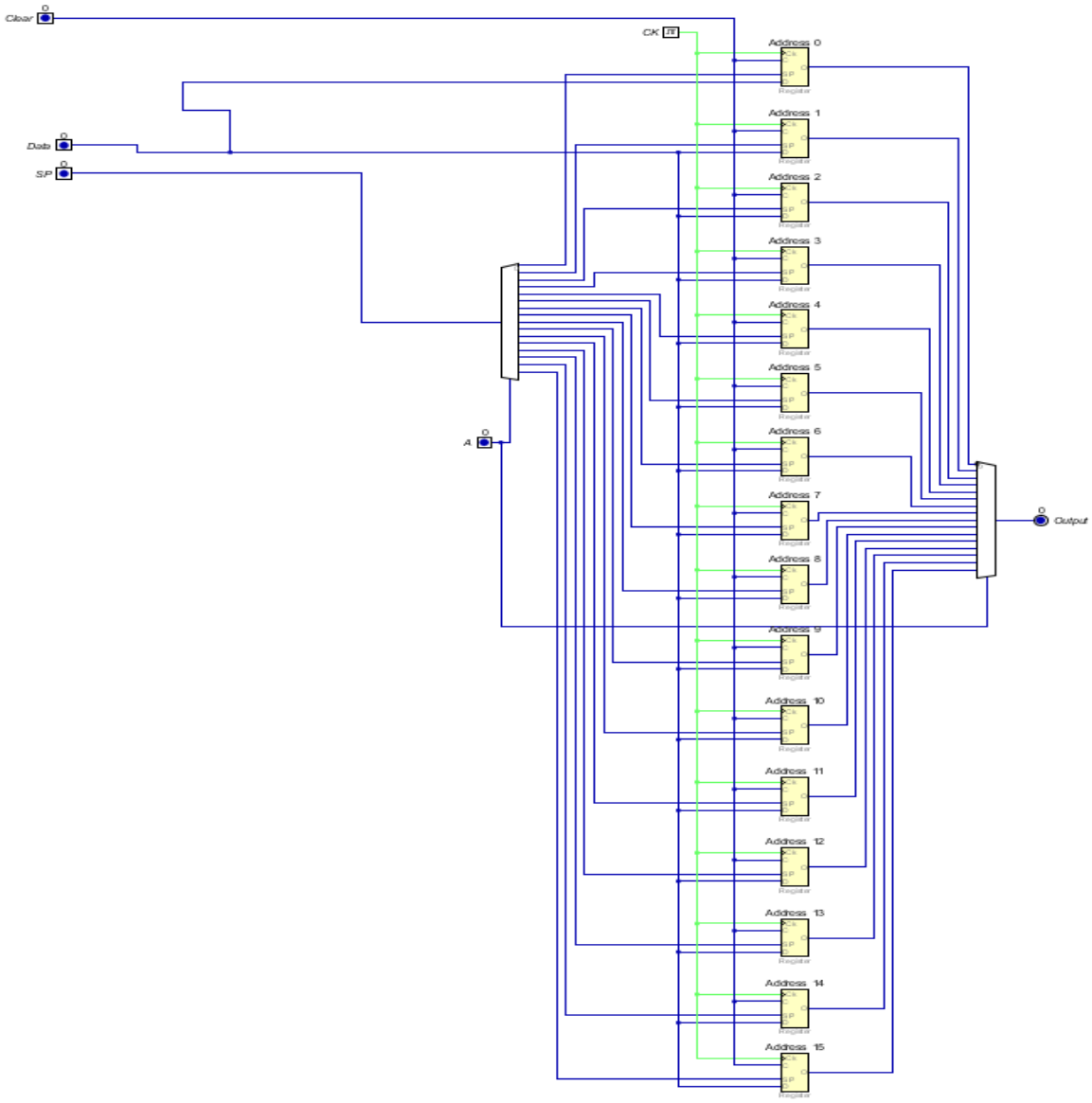


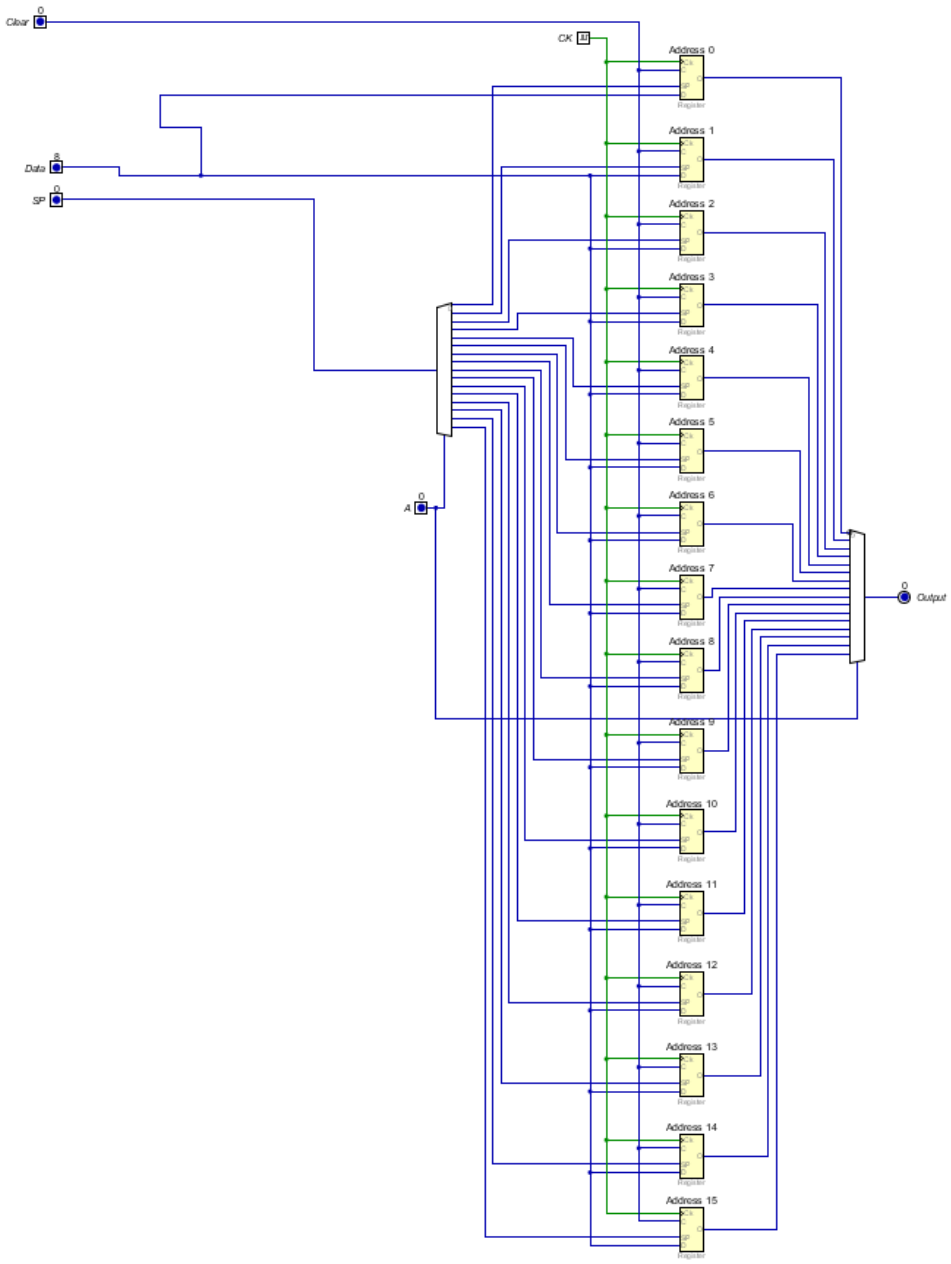
	
Changing data	Clock Cycle 1: 
Reading through register	Clock Cycle 1:

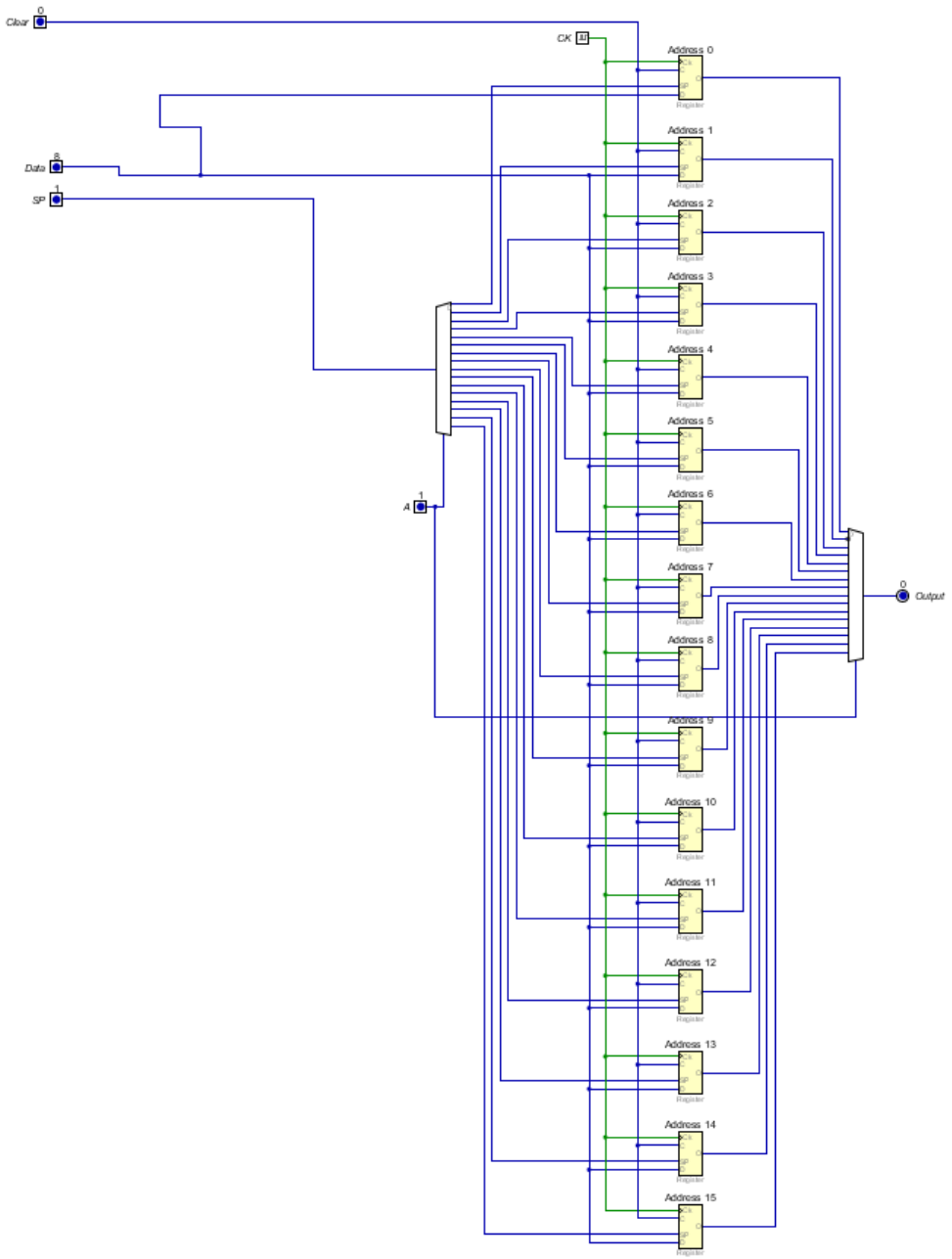
	
Clearing register	Clock Cycle 1: 

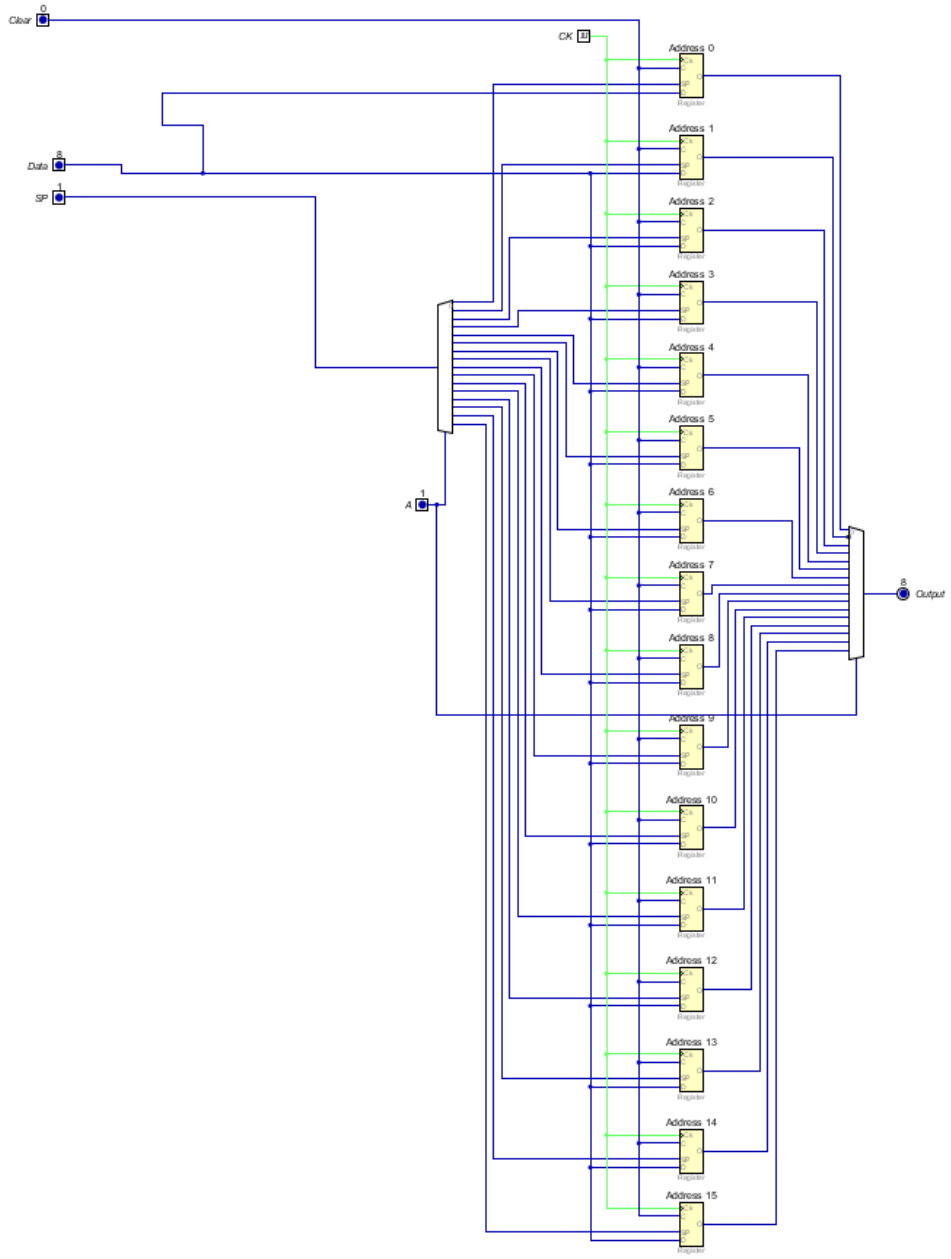
	
Max data that can be stored	Clock Cycle 1:  

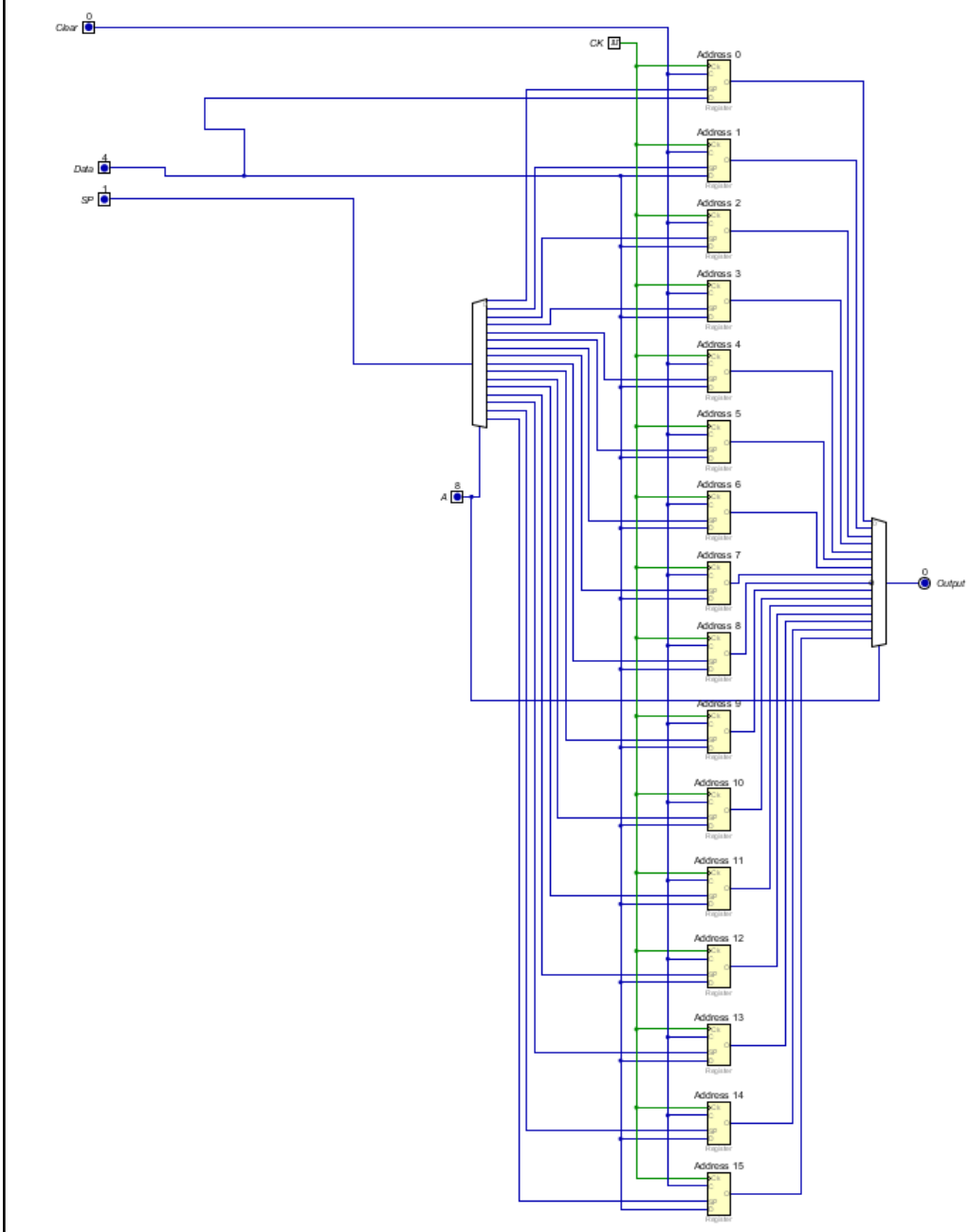
RAM Block:

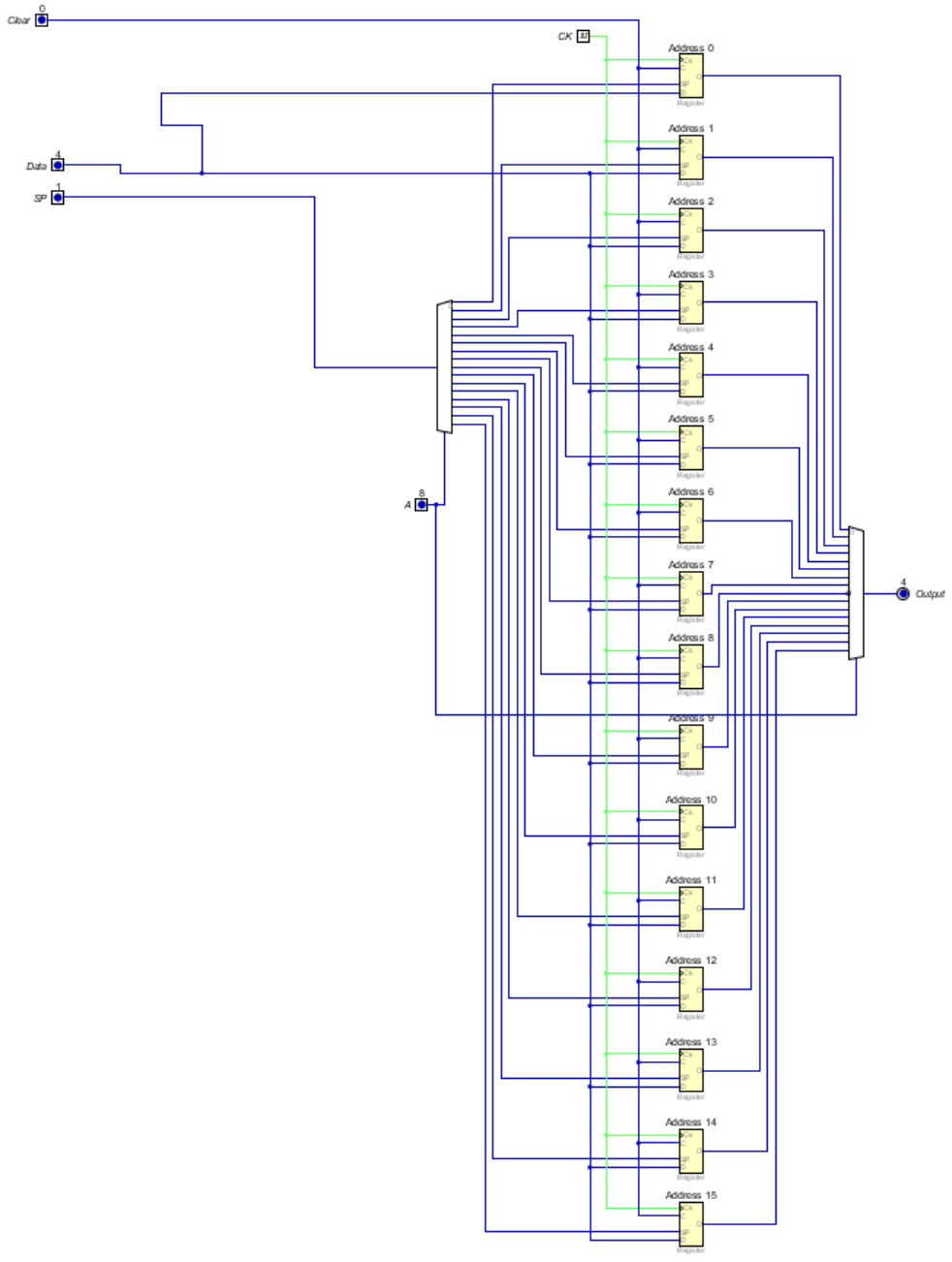

Clear
CK
Data
SP
A
Output
Address 0
Address 1
Address 2
Address 3
Address 4
Address 5
Address 6
Address 7
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15

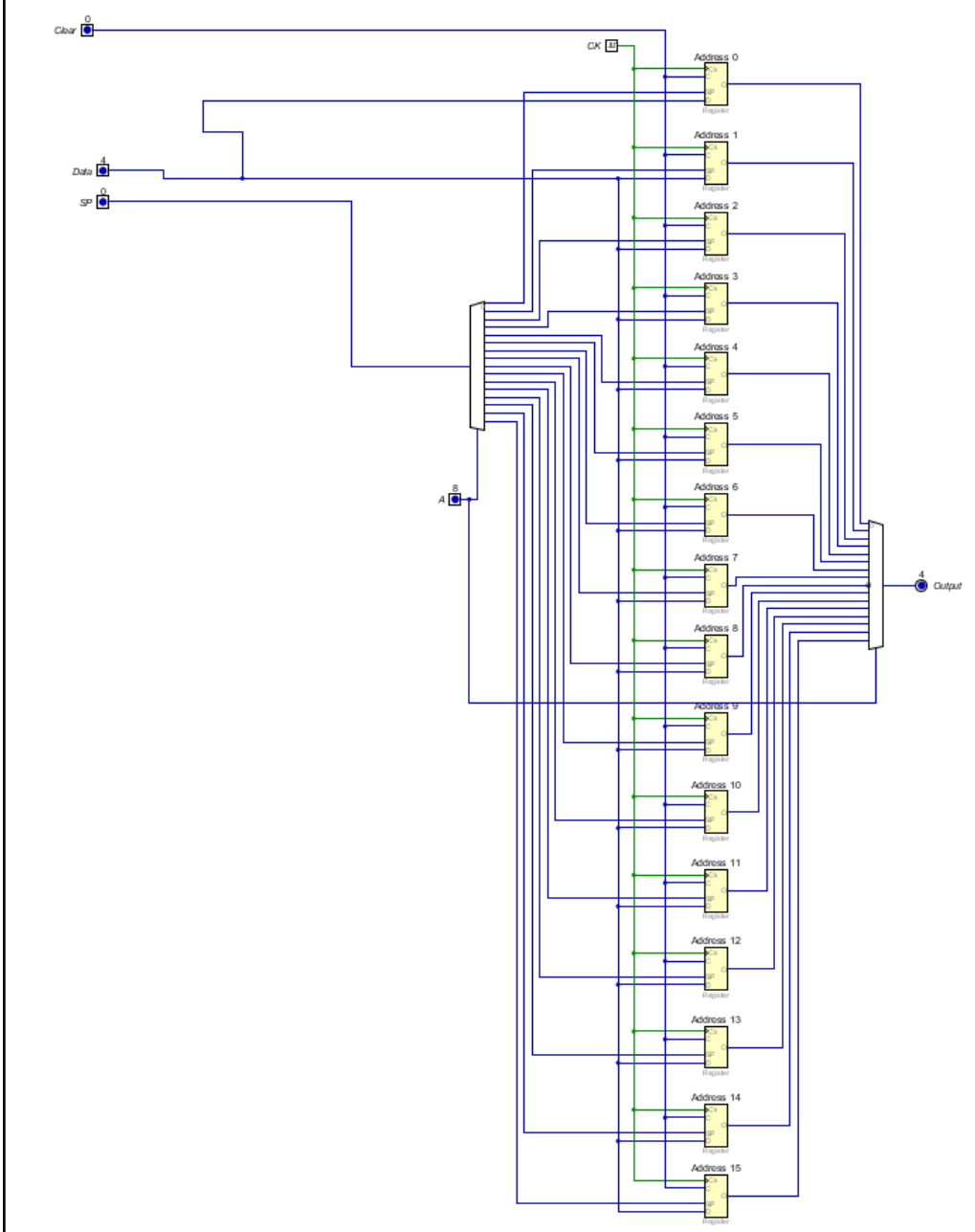
Inputting data into A register	 Clock Cycle 1:

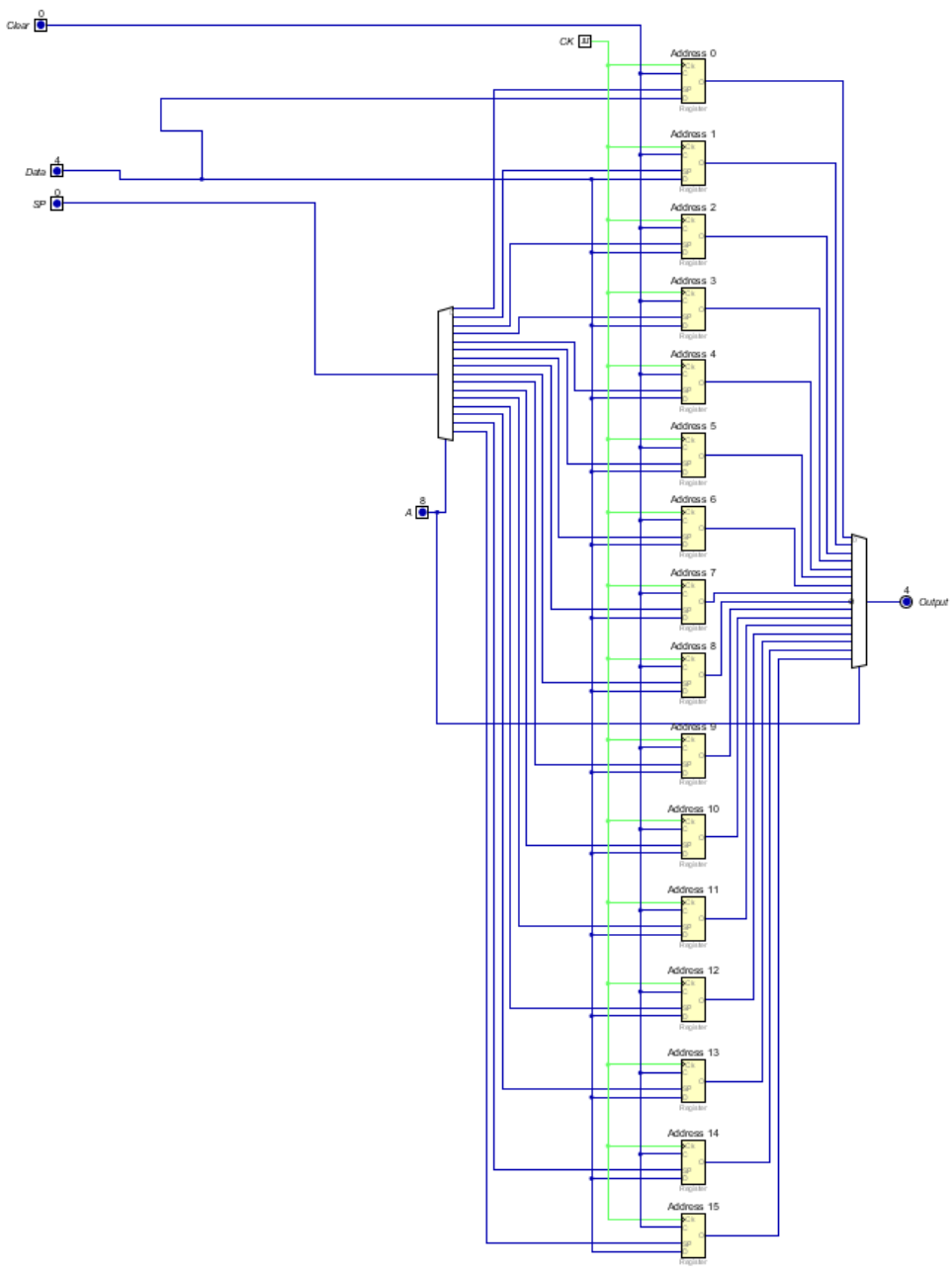

Clear
0
CK
Address 0
Address 1
Address 2
Address 3
Address 4
Address 5
Address 6
Address 7
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15
Register
Data
8
SP
1
A
1
0
Output

	
Inputting new data in a different register	Clock Cycle 1:

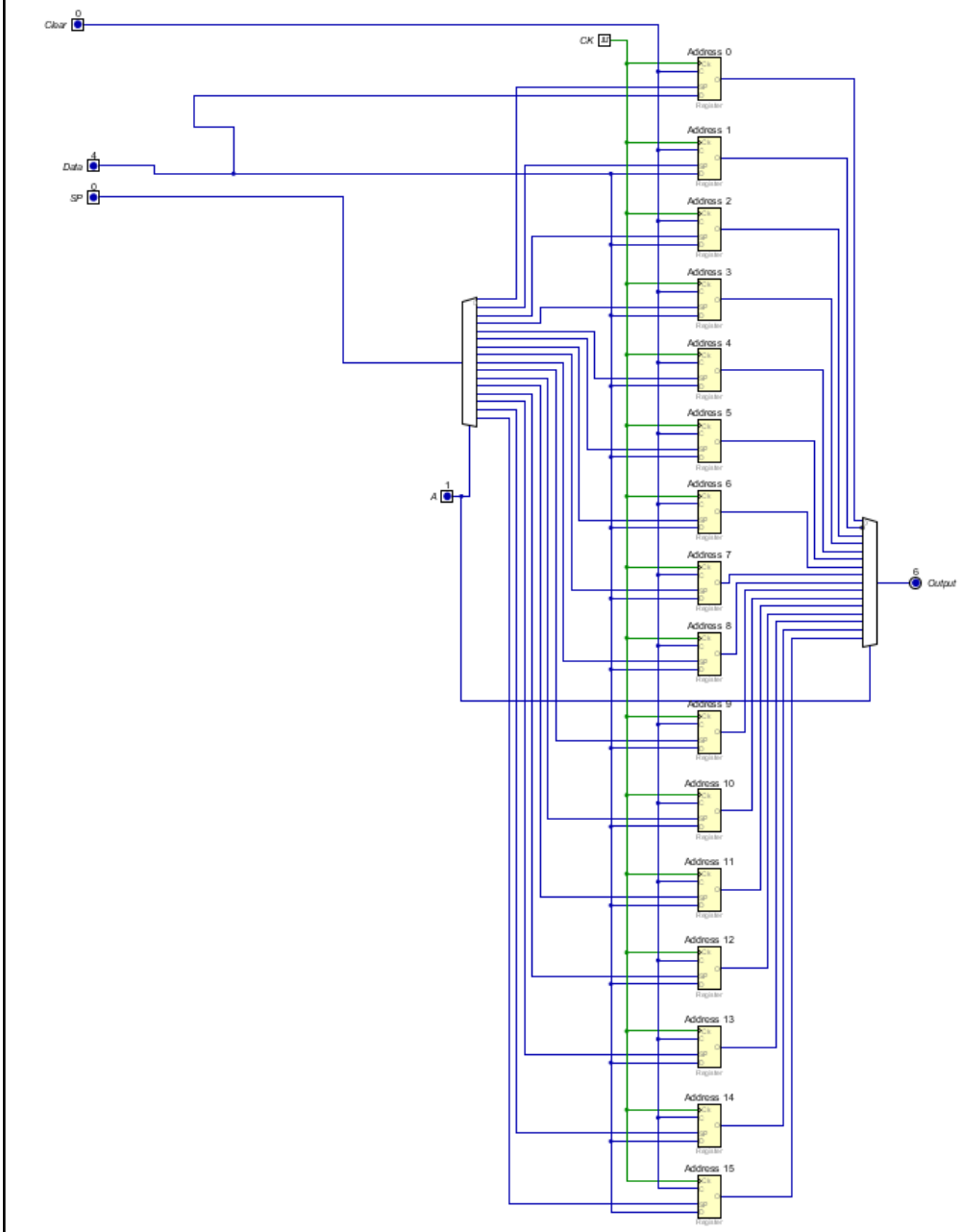

Clear
0
CK
Data
4
SP
1
A
8
Address 0
Address 1
Address 2
Address 3
Address 4
Address 5
Address 6
Address 7
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15
Register
Output
0

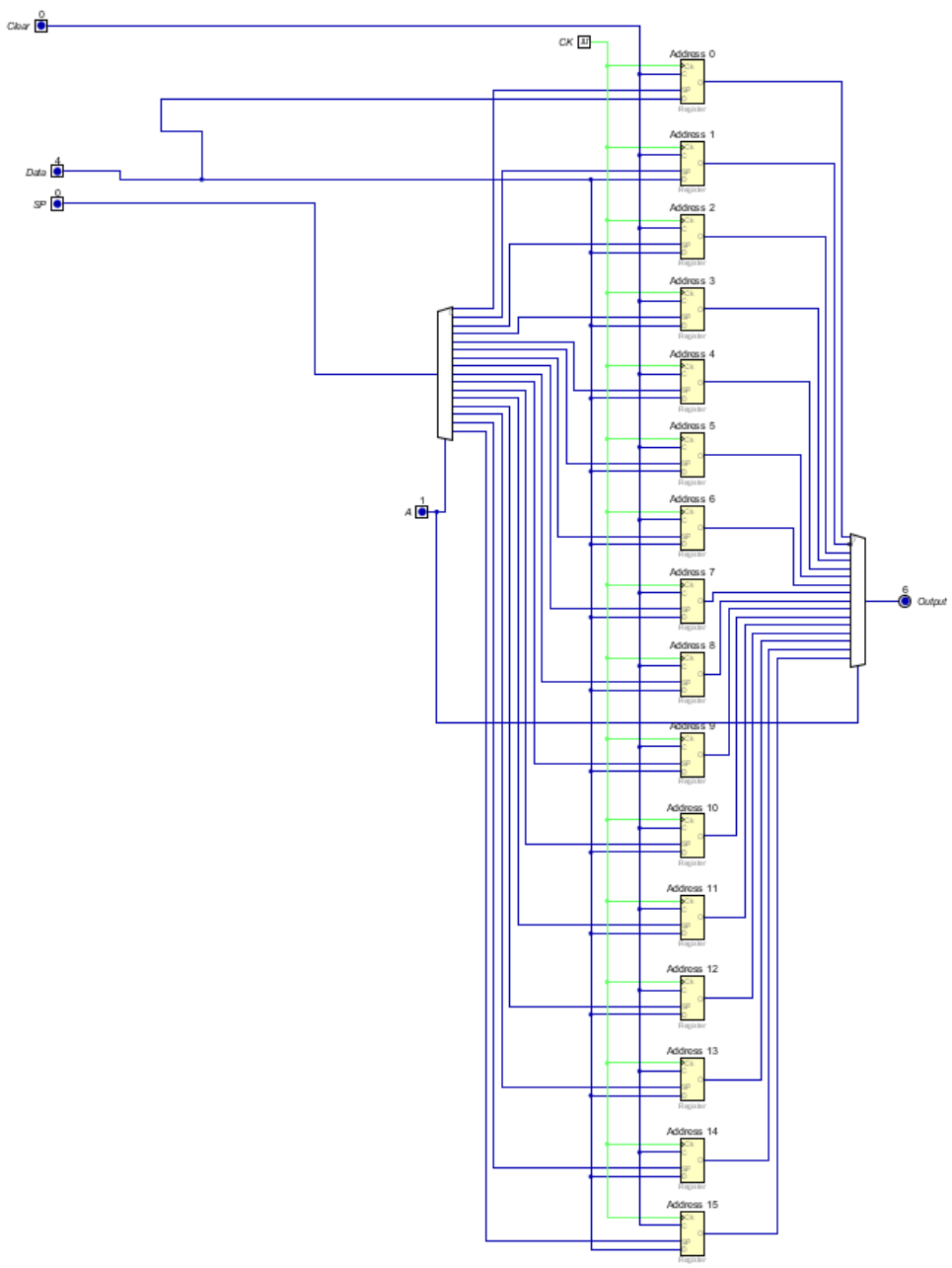
	
Reading registers:	Clock Cycle 1(address 8):

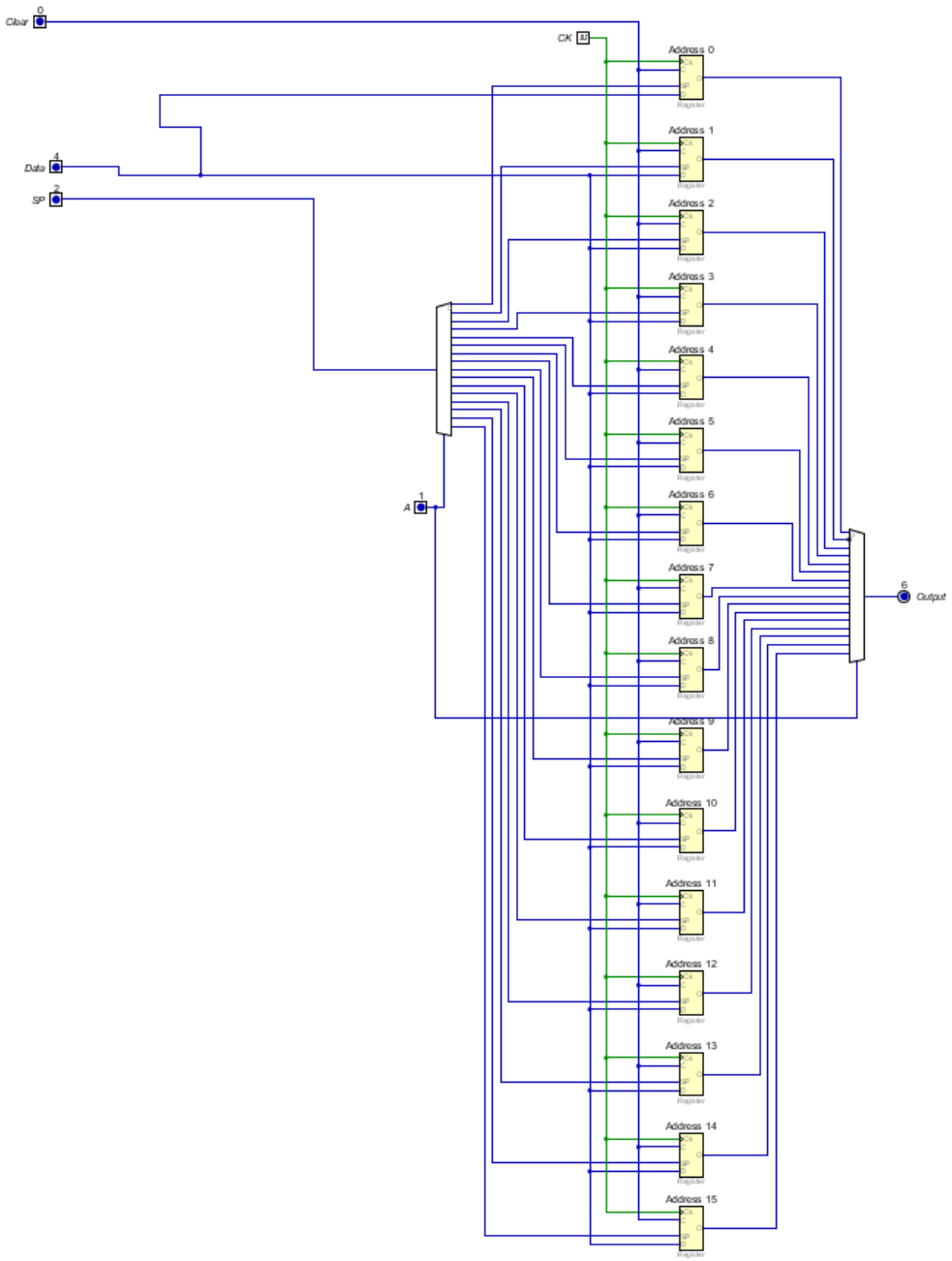

Clear
0
CK
Address 0
Address 1
Address 2
Address 3
Address 4
Address 5
Address 6
Address 7
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15
Register
Data
4
SP
0
A
8
4
Output

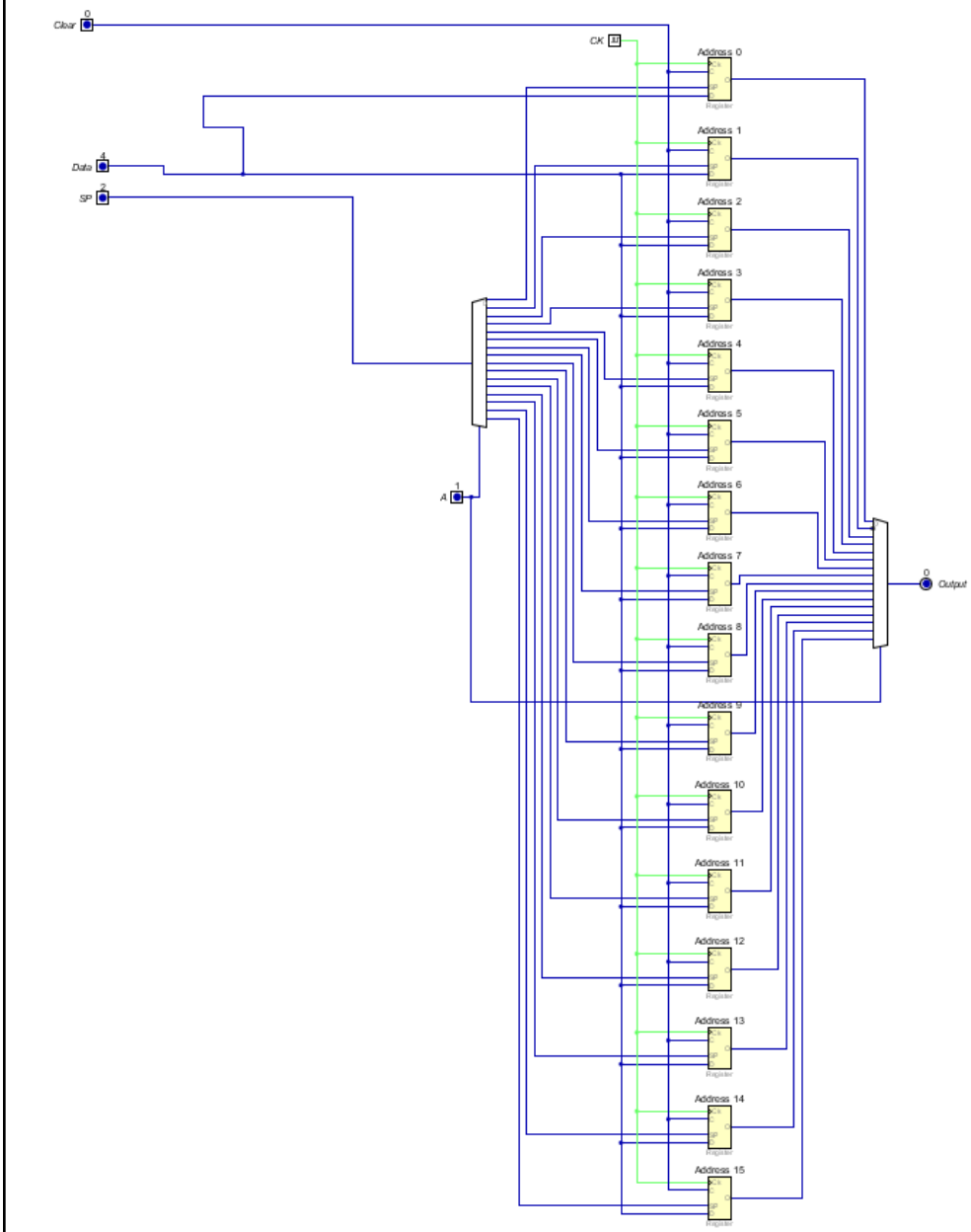


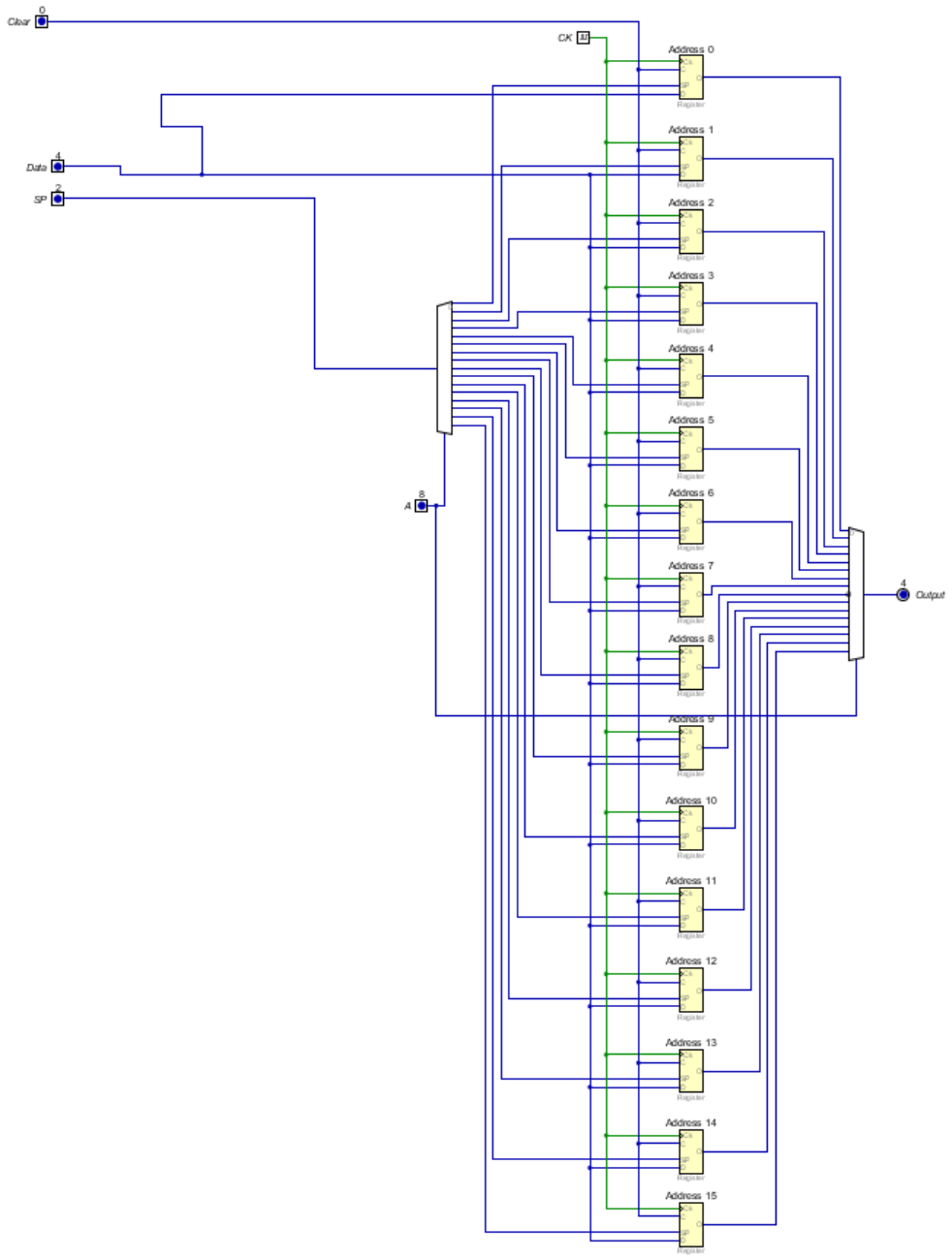
Clock Cycle 1(address 1):

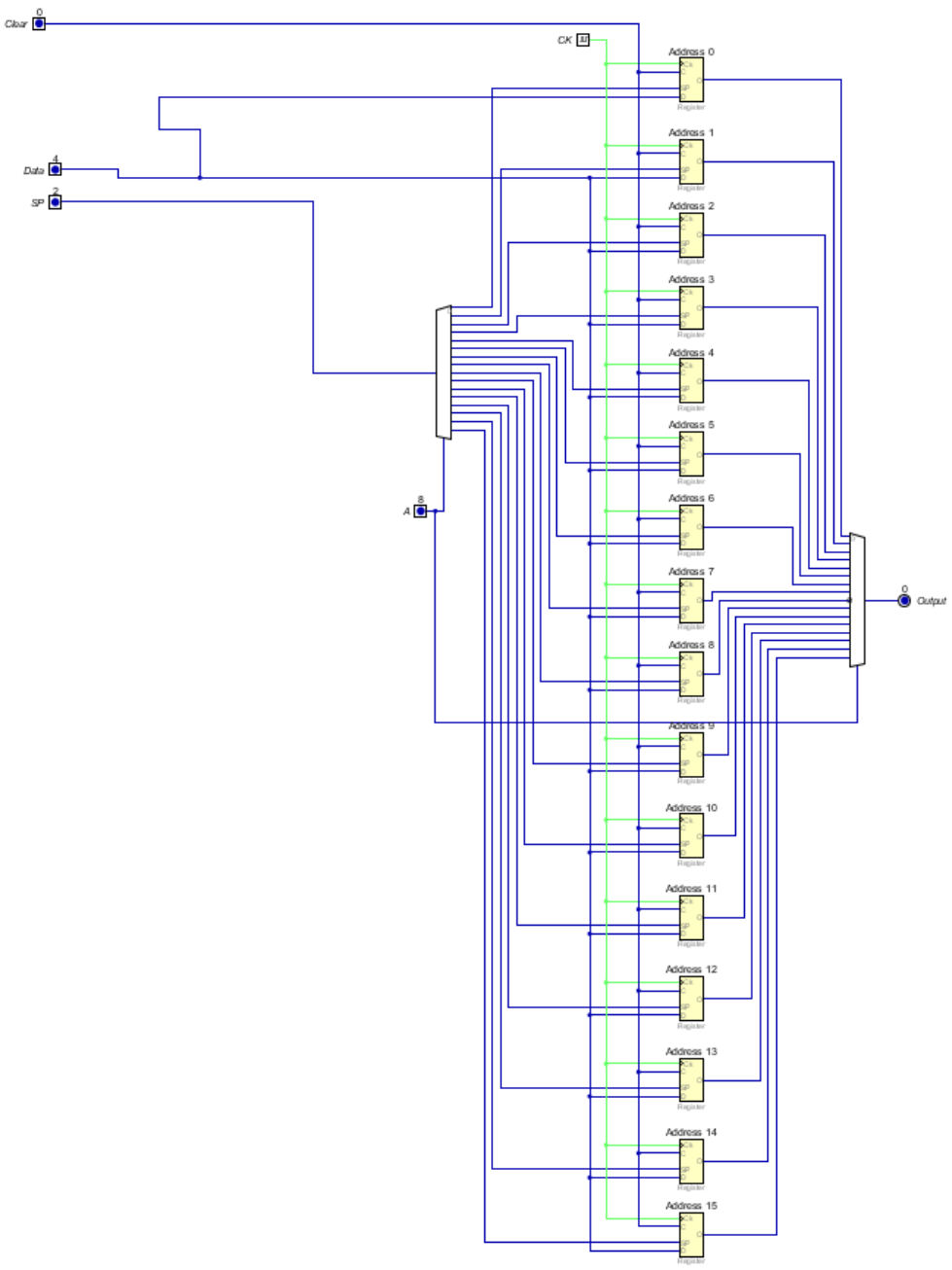

Clear
0
CK
Address 0
Address 1
Address 2
Address 3
Address 4
Address 5
Address 6
Address 7
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15
Register
Data
4
SP
0
A
1
6
Output

	
Clearing registers	Clock Cycle 1(address 1- address 8):

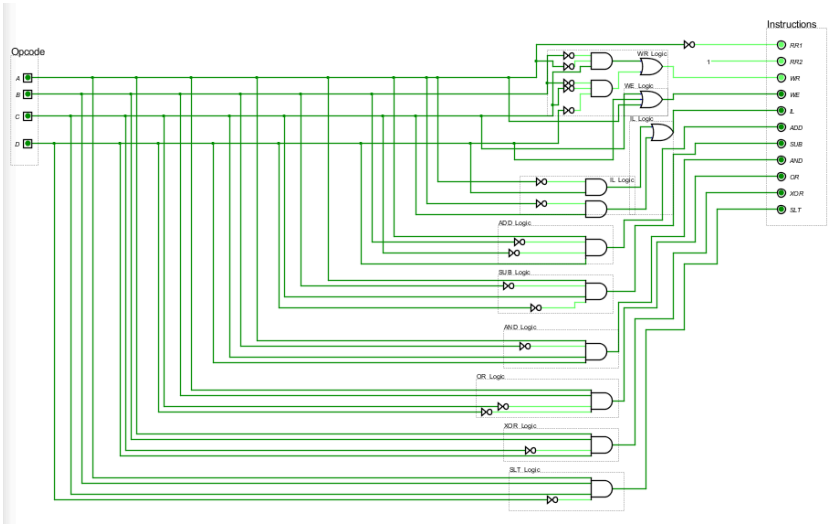
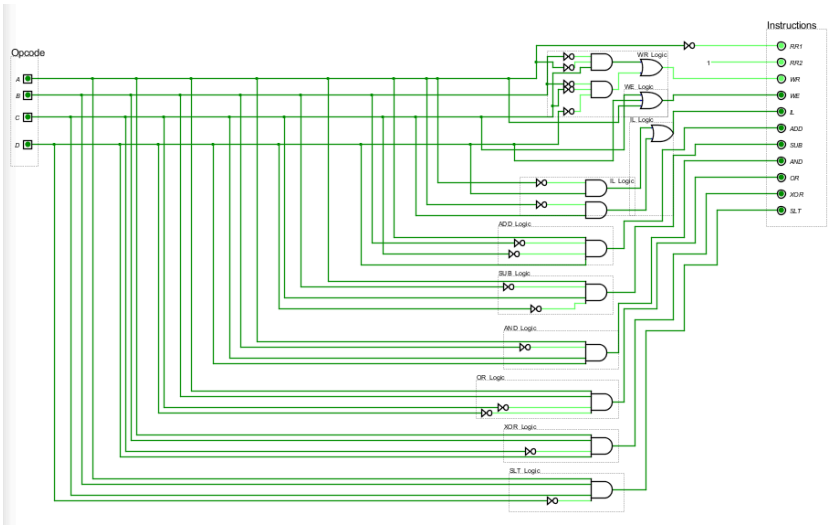

0
Clear
CK
Address 0
Address 1
4
Data
2
SP
Address 2
Address 3
Address 4
Address 5
1
A
Address 6
Address 7
6
Output
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15

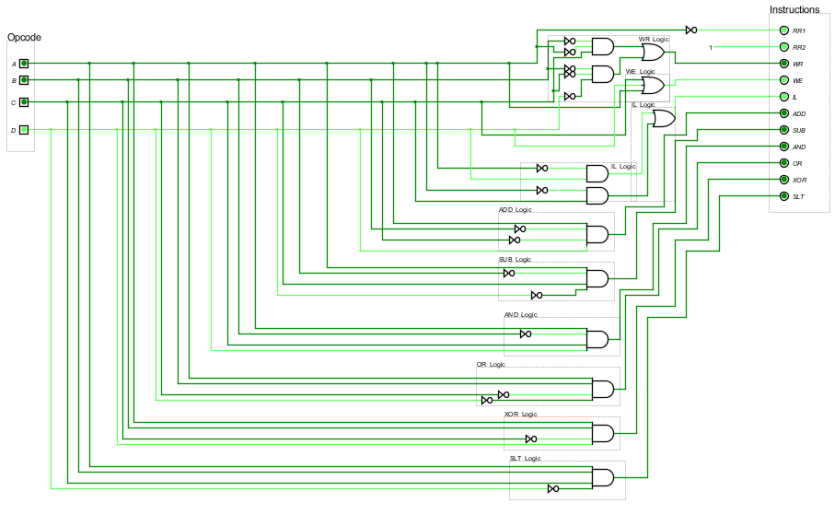
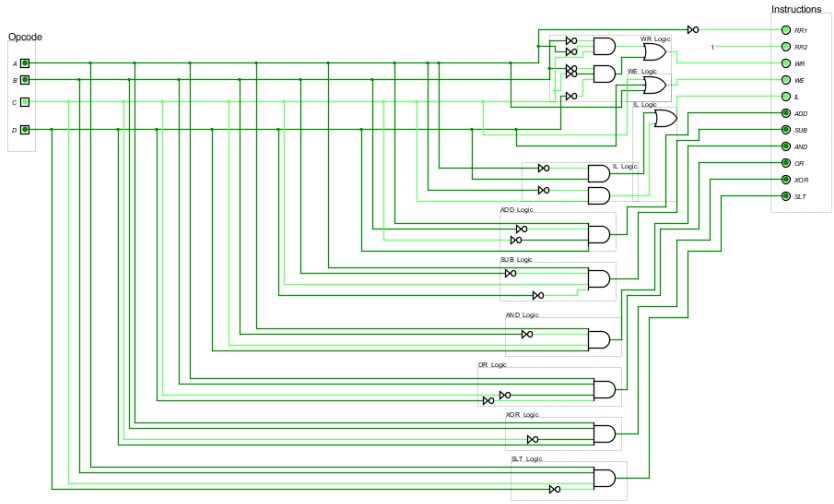
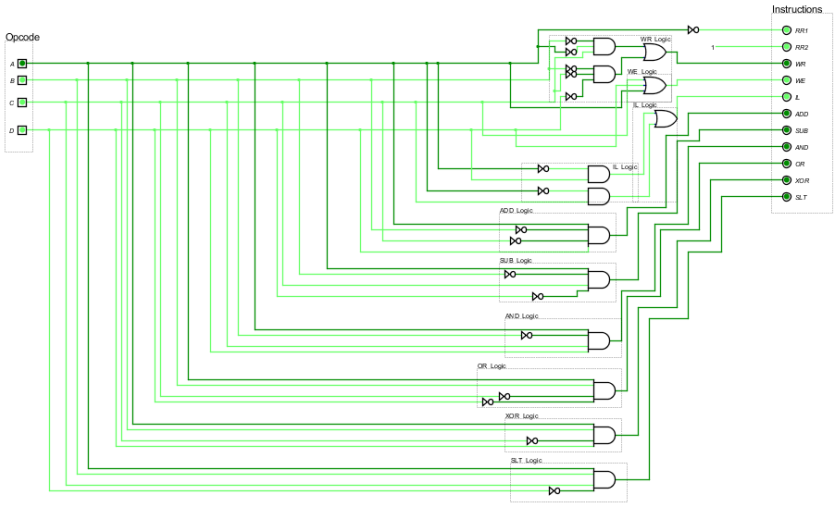

Clear
0
CK
Address 0
Address 1
Data
4
SP
2
Address 2
Address 3
Address 4
Address 5
A
1
Address 6
Address 7
0
Output
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15

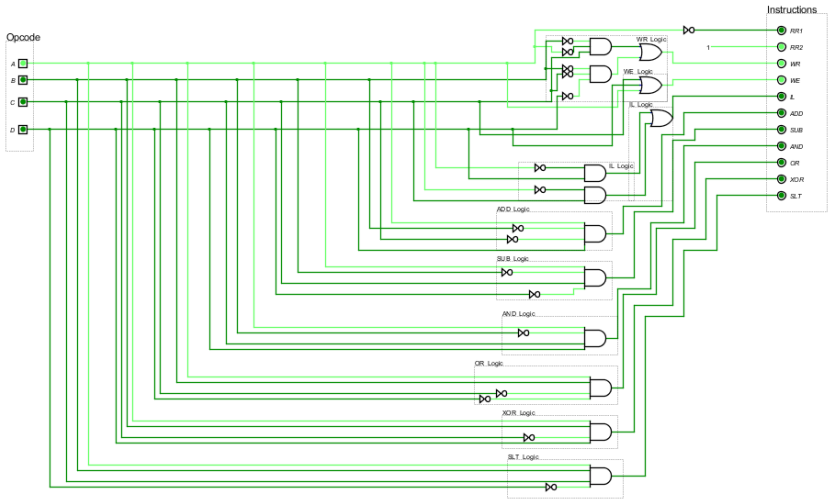
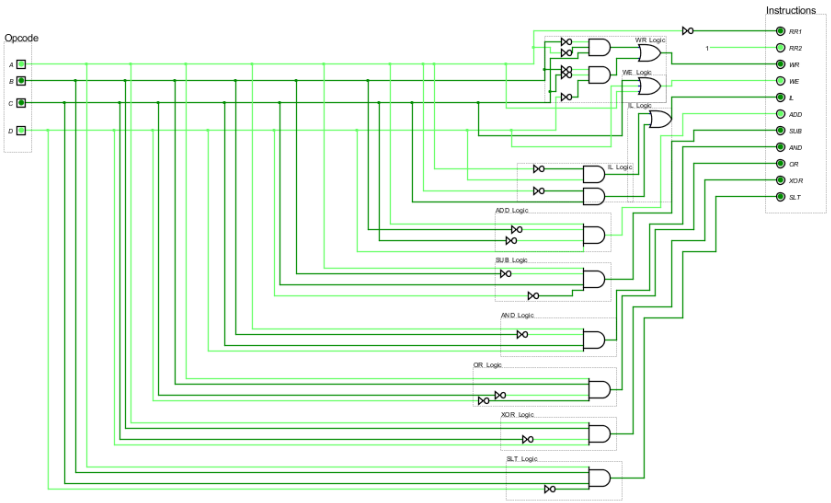
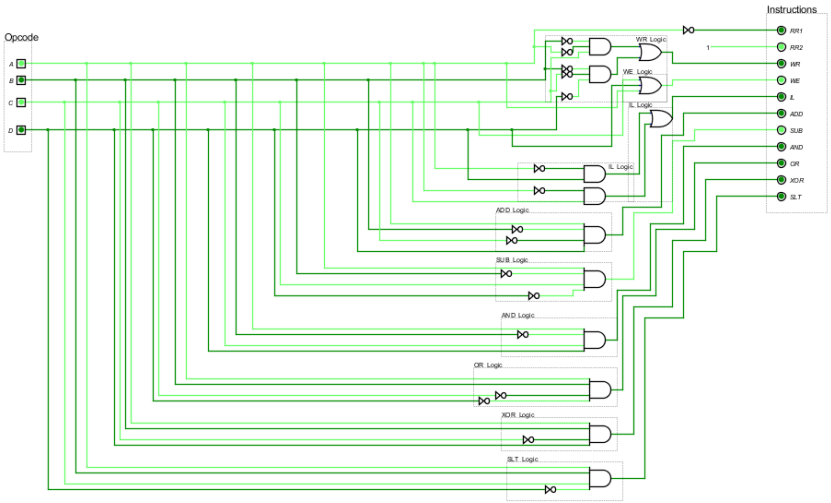

Clear
0
CK
Address 0
Address 1
Data
4
SP
2
Address 2
Address 3
Address 4
Address 5
A
8
Address 6
Address 7
4
Output
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15

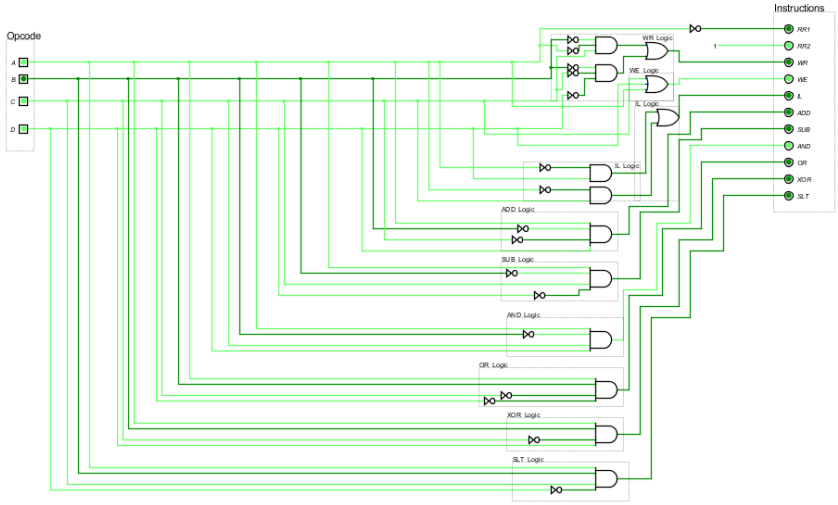
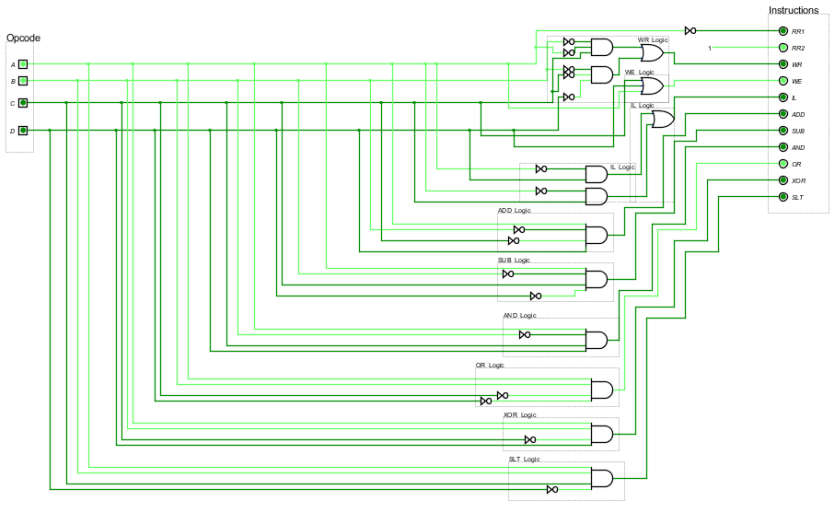
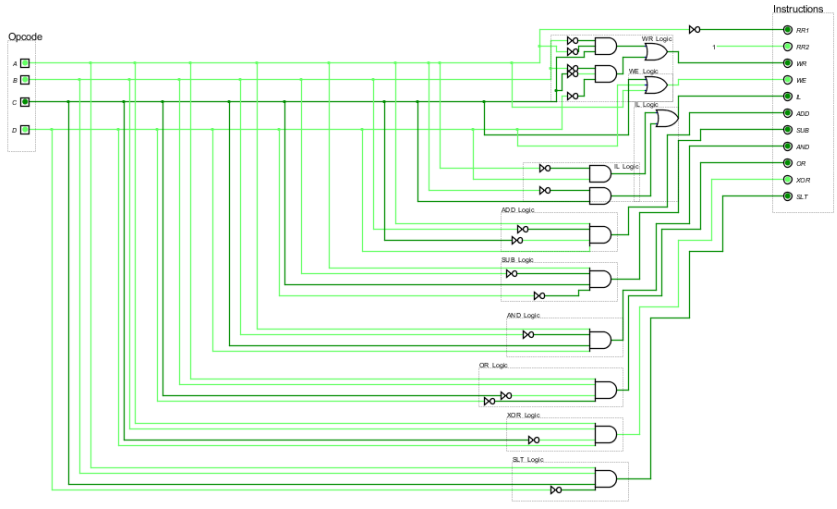

Clear
0
CK
Address 0
Address 1
Data
4
SP
2
Address 2
Address 3
Address 4
Address 5
A
8
Address 6
Address 7
0
Output
Address 8
Address 9
Address 10
Address 11
Address 12
Address 13
Address 14
Address 15

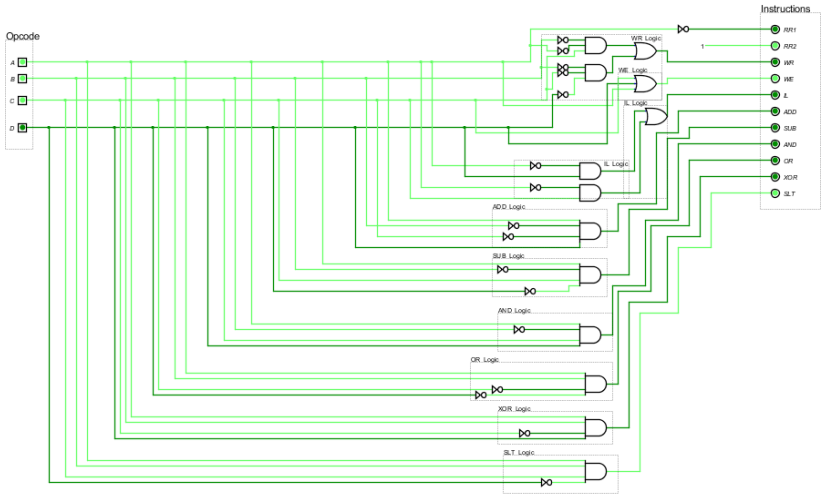
Decoder:

Circuit running	
Opcode 0000	

Opcode 0001	
Opcode 0010	
Opcode 0111	

Opcode 1000	
Opcode 1001	
Opcode 1010	

Opcode 1011	
Opcode 1100	
Opcode 1101	

Opcode 1110	 Opcode A B C D Instructions WR Logic WE Logic IL Logic IL Logic ADD Logic SUB Logic AND Logic OR Logic XOR Logic SLT Logic 1 WR1 RR2 WR WE IL ADD SUB AND OR XOR SLT