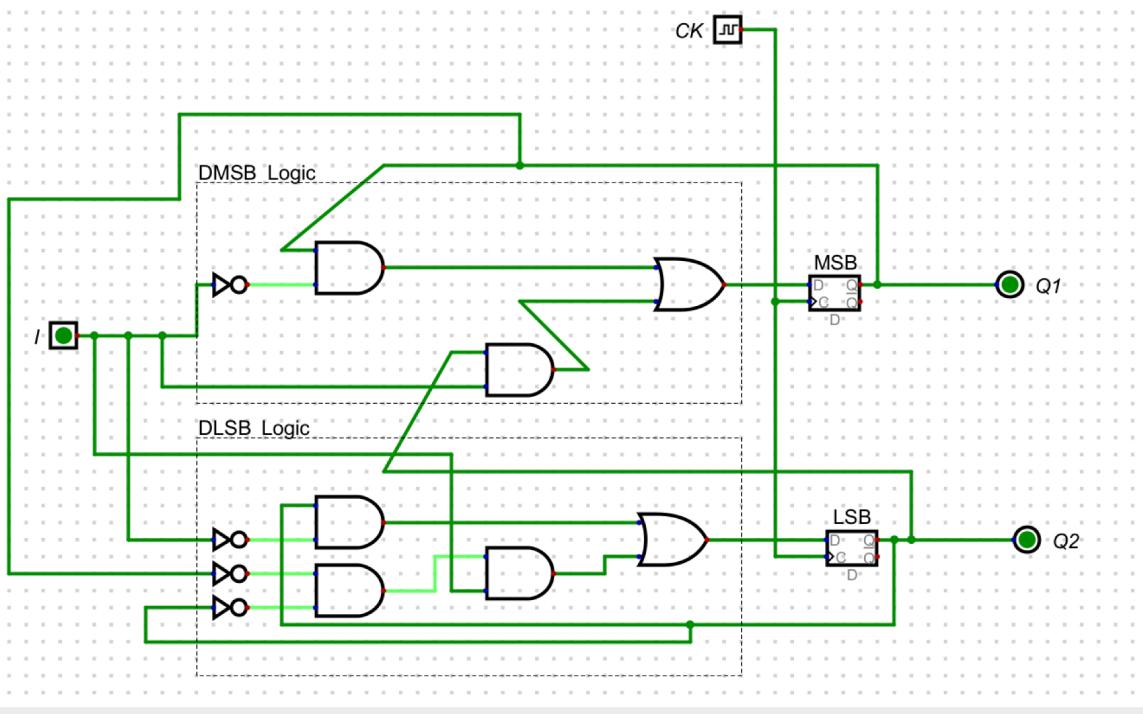


Test Tables:

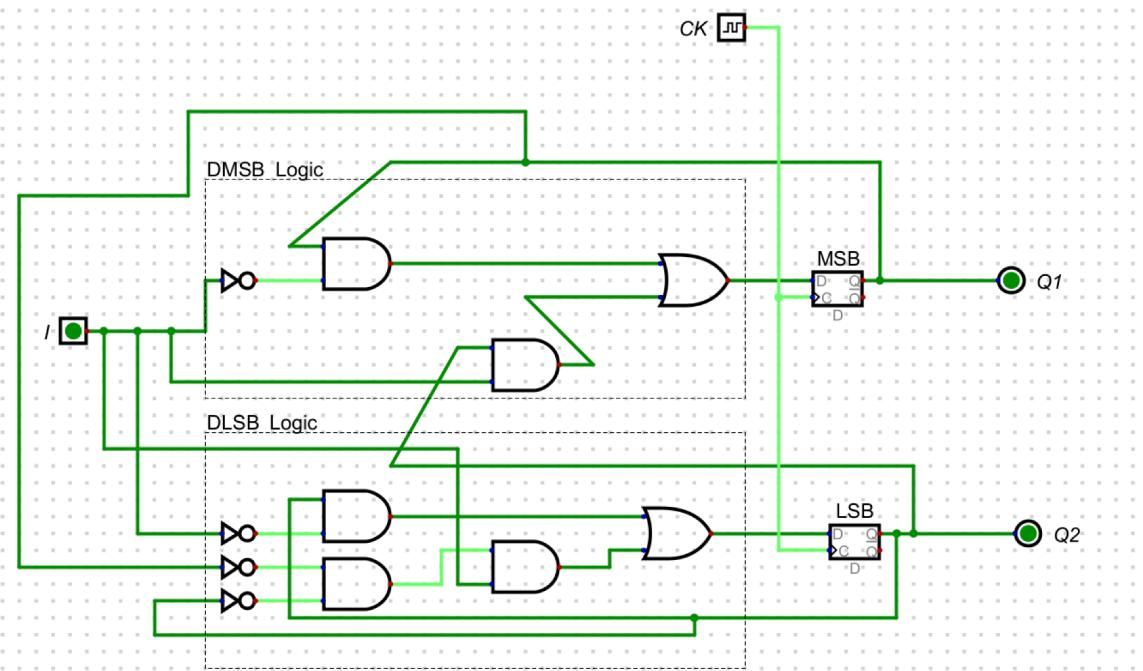
State Machine:

Input = 0, Clock = 0, Q1 = 0, Q2 = 0

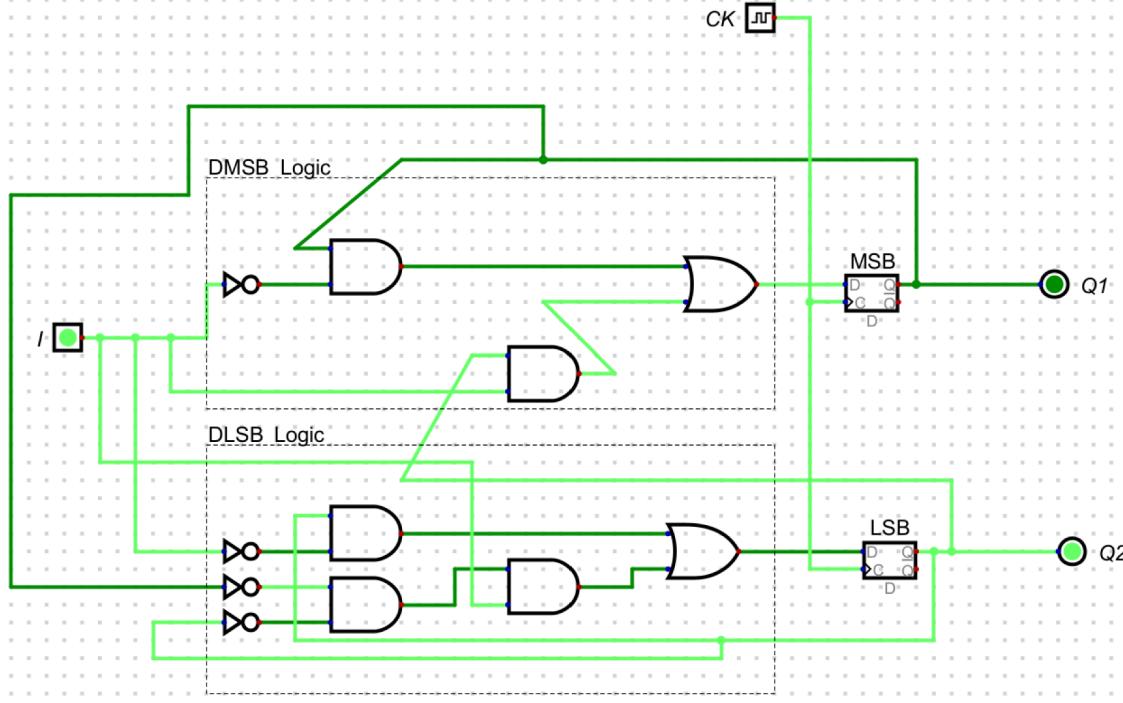


13 nodes

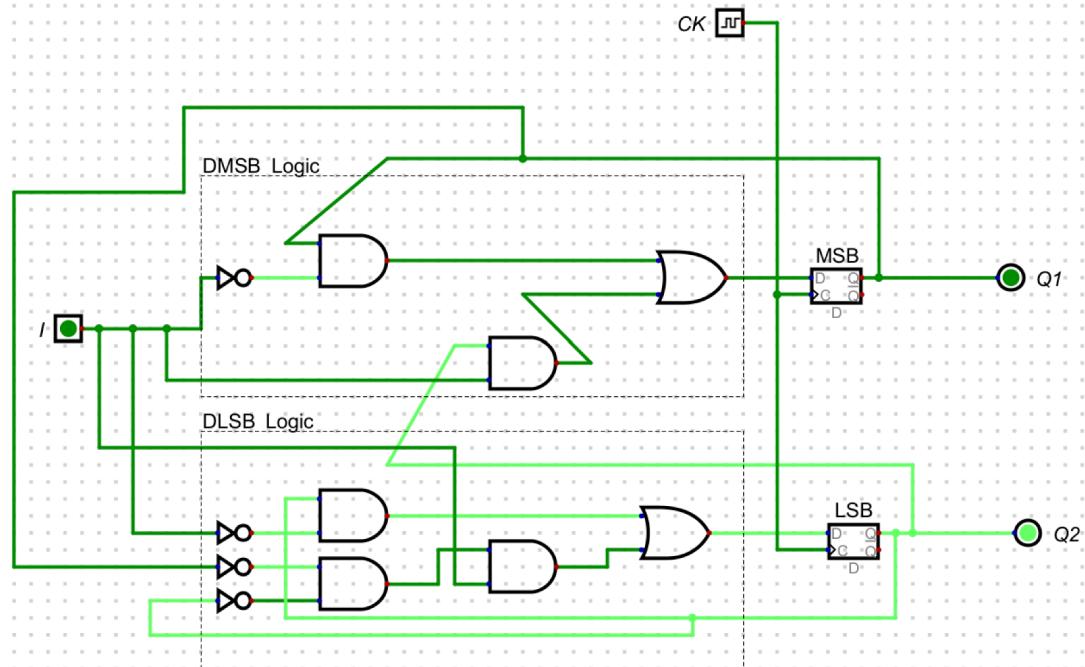
Input = 0, Clock = 1, Q1 = 0, Q2 = 0 (in Fetch cycle)



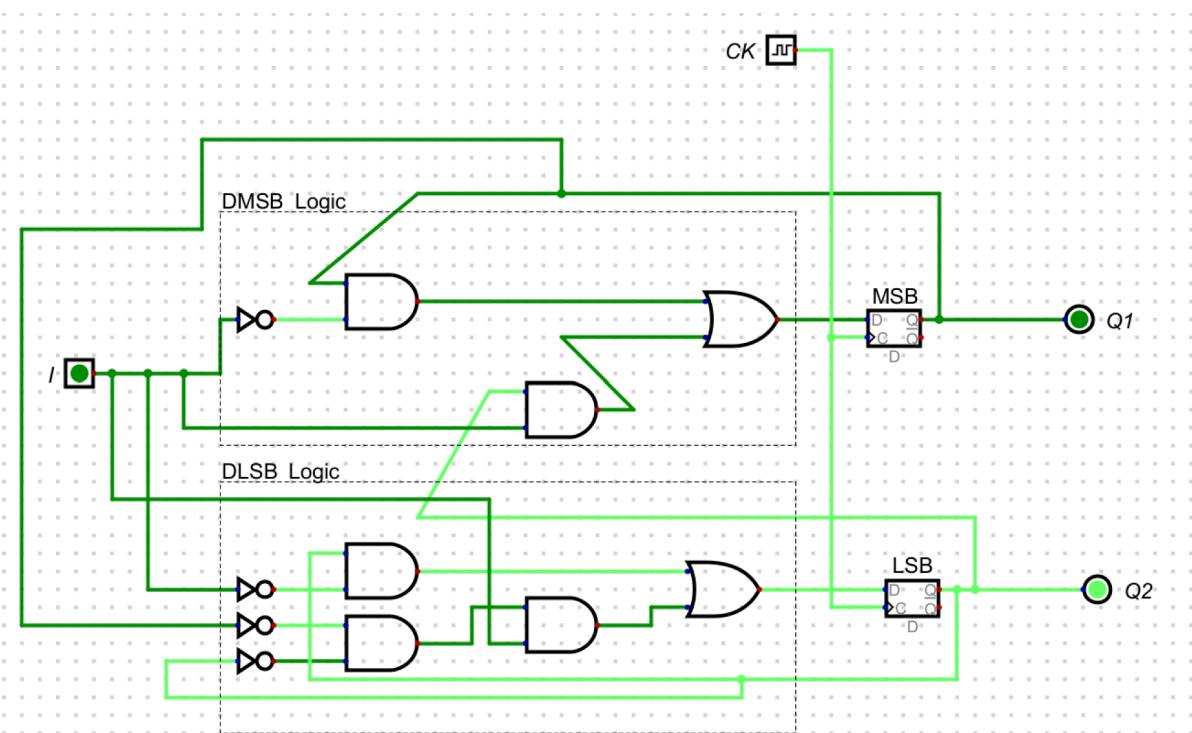
Input = 1, Clock = 1, Q1 = 0, Q2 = 1 (Transitioning to Decode State)



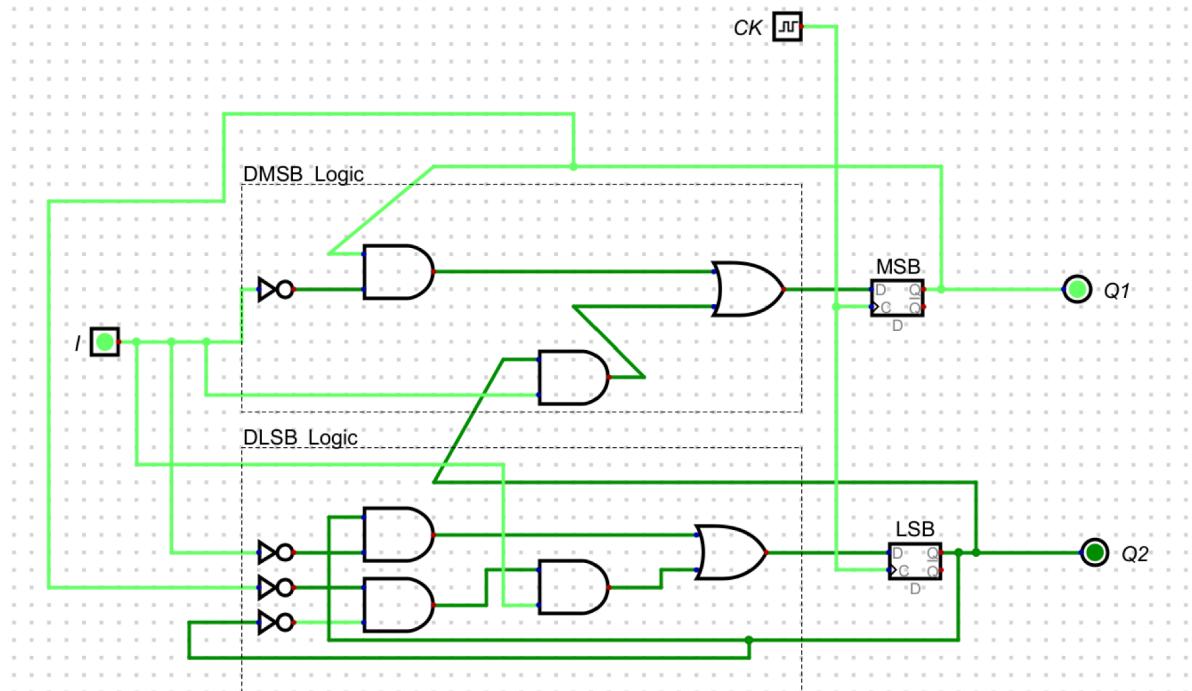
Input = 0, Clock = 0, Q1 = 0, Q2 = 1 (Stays in Decode State)



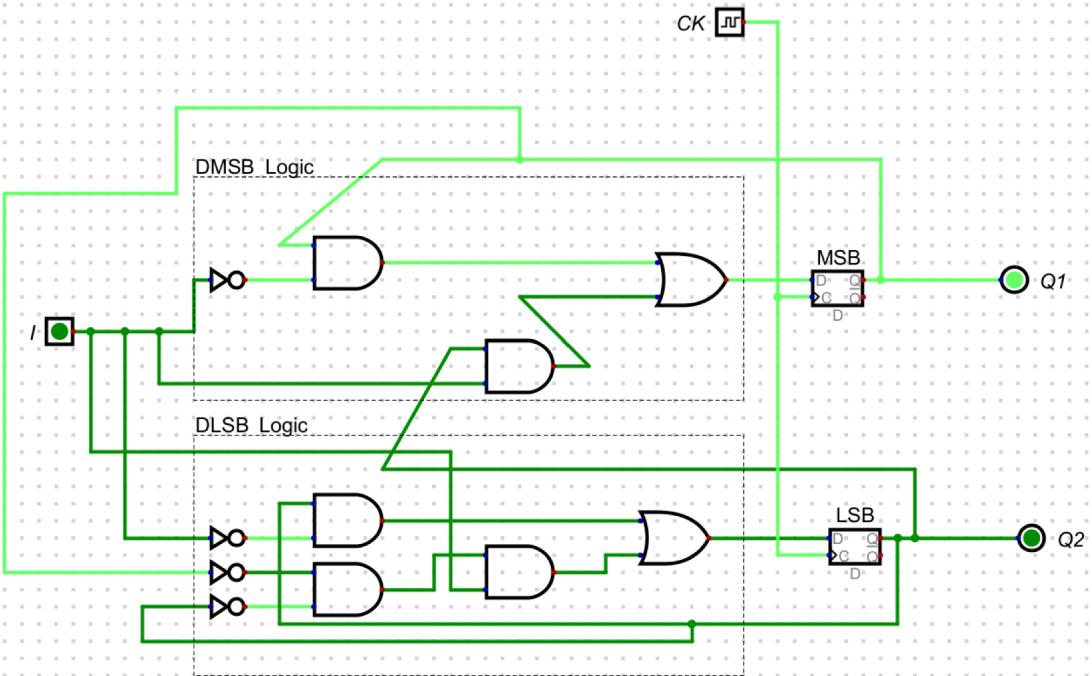
Input = 0, Clock = 1, Q1 = 0, Q2 = 1 (Continue to stay in Decode State)



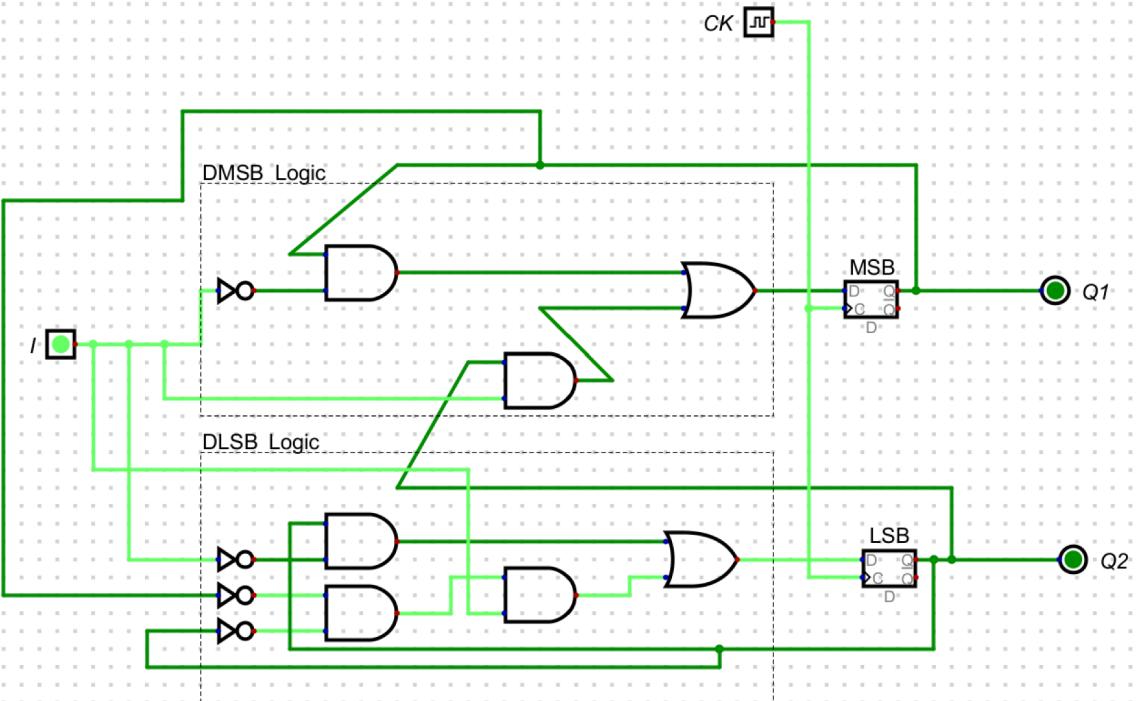
Input = 1, Clock = 1, Q1 = 1, Q2 = 0 (Goes to Execution State)



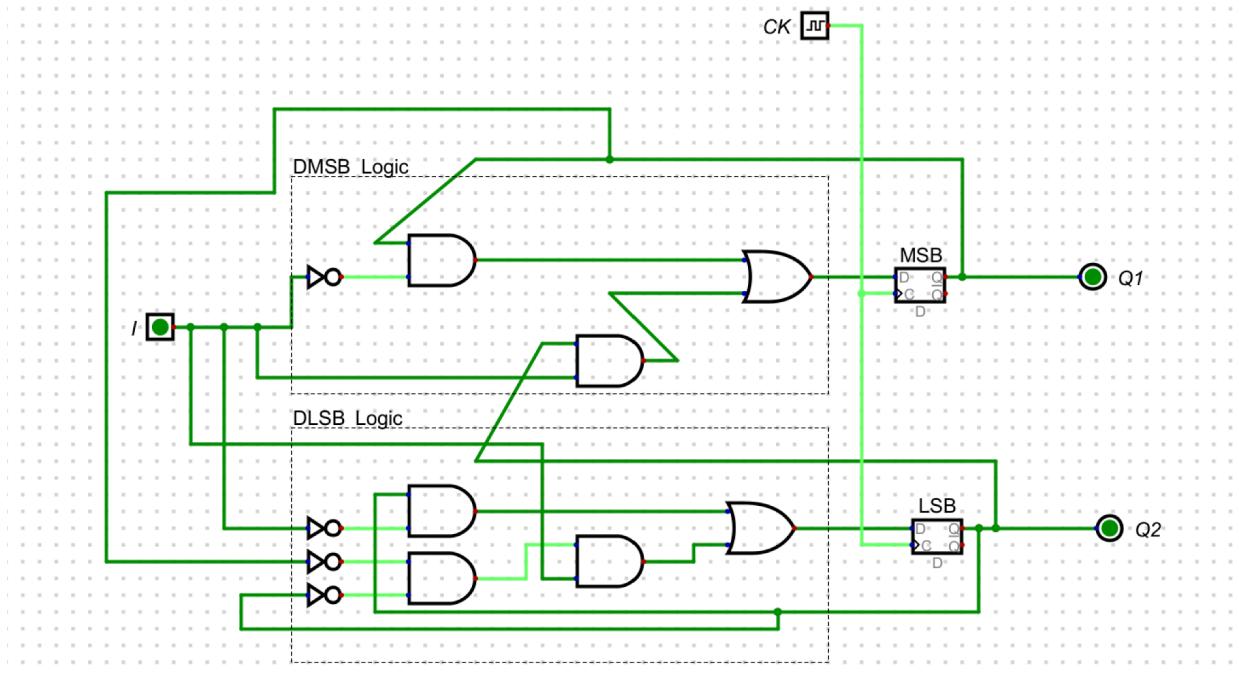
Input = 0, Clock = 1, Q1 = 1, Q2 = 0 (Stays in Execution State)



Input = 1, Clock = 1, Q1 = 0, Q2 = 0 (Goes to back to Fetch state)

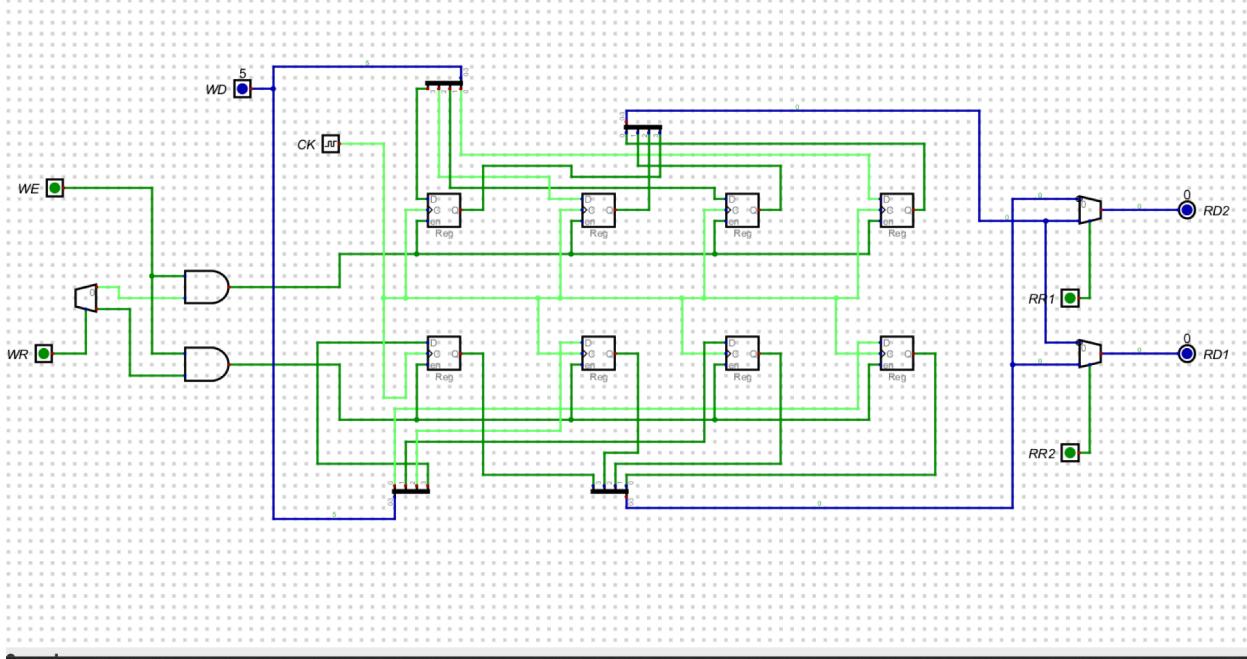


Input = 0, Clock = 1, Q1 = 0, Q2 = 0 (Stays in Fetch state)

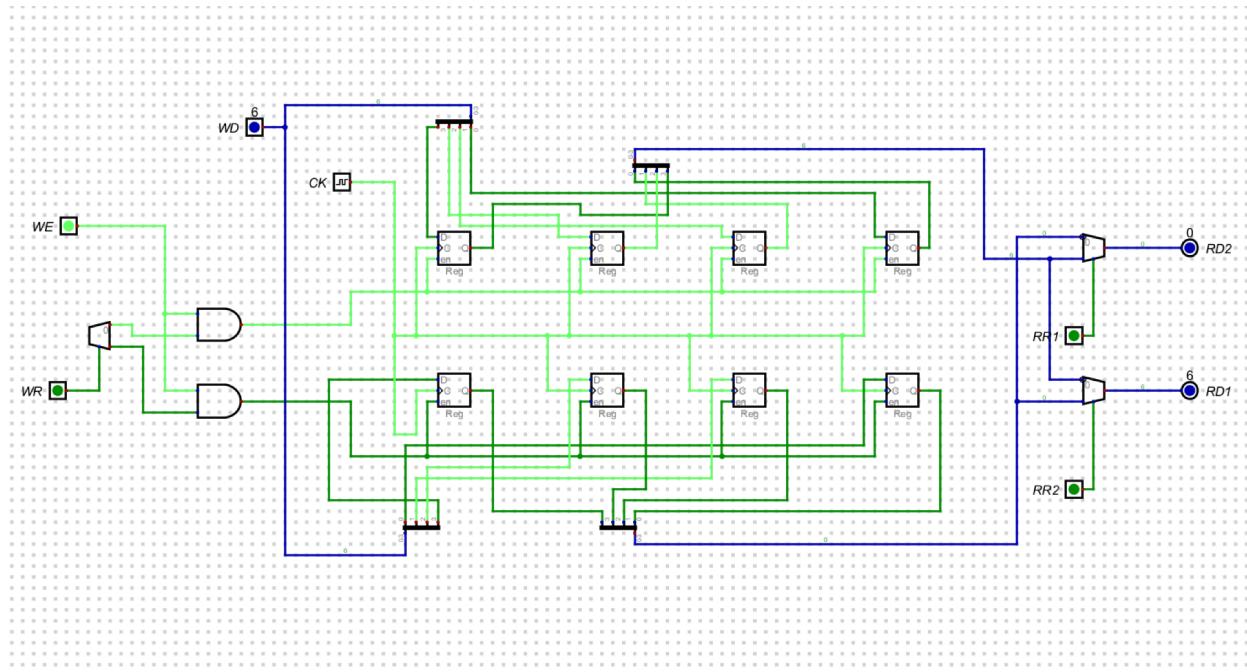


Register File:

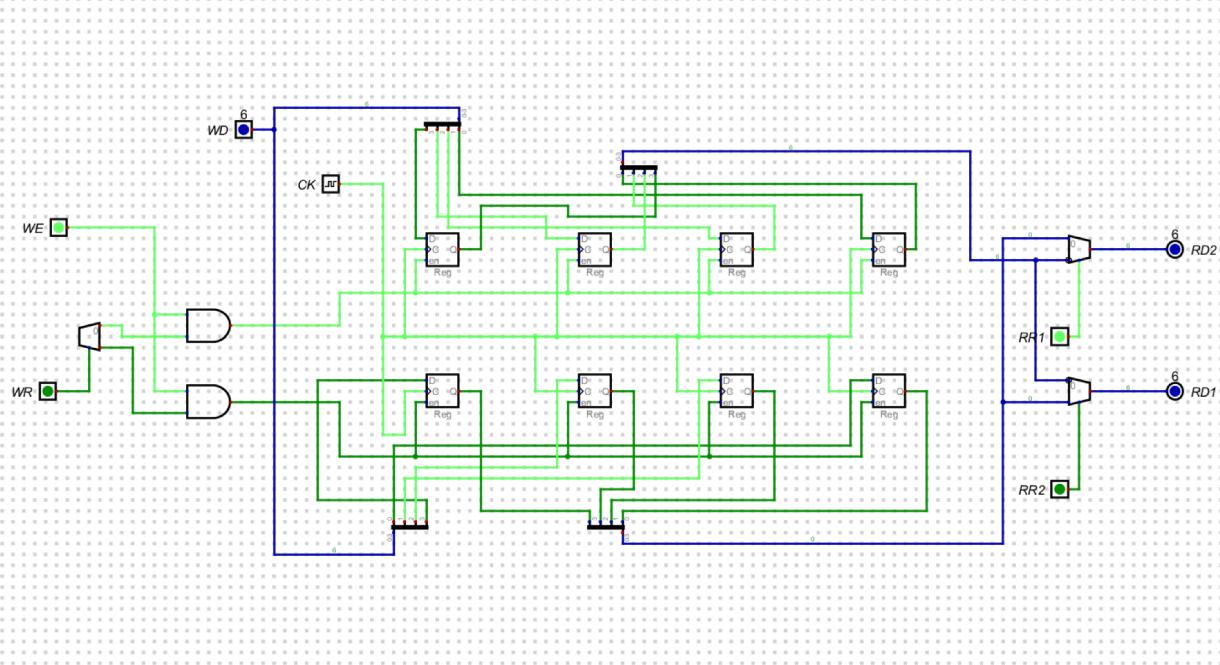
WD=5 WR=0 WE=0 RR1=0 RR2=0, RD1 = 0, RD2 = 0



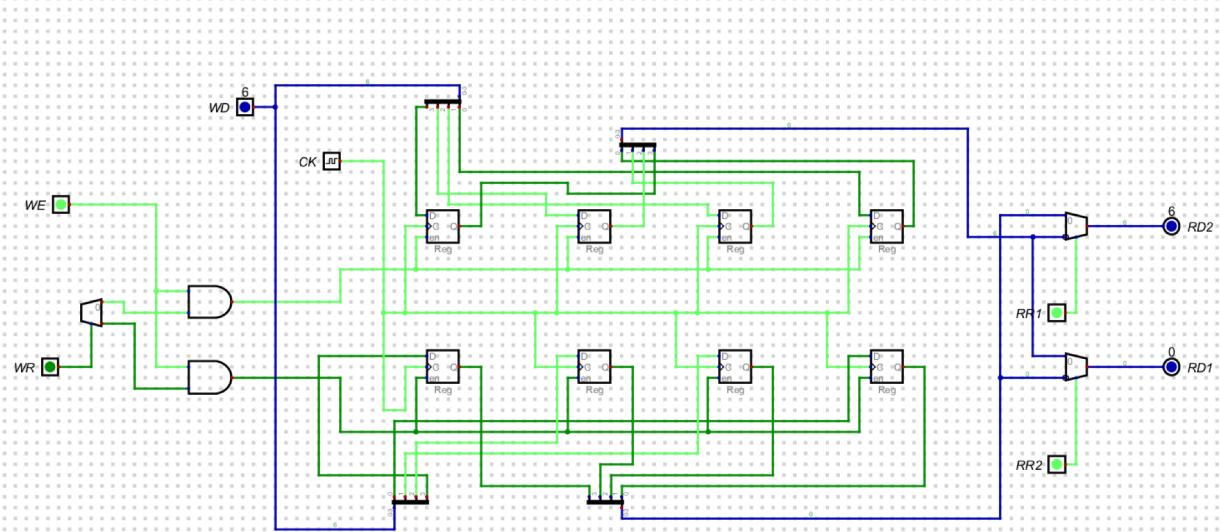
WD=6 WR=0 WE=1 RR1=0 RR2=0, RD1 = 6, RD2 = 0



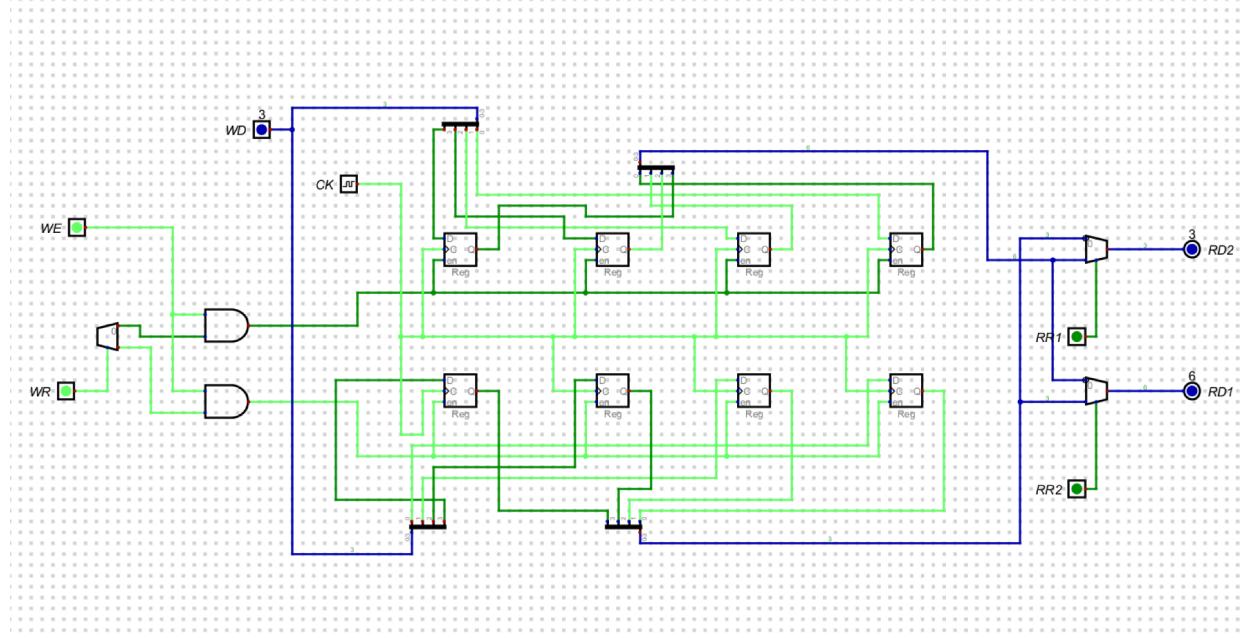
WD=6 WR=0 WE=1 RR1=1 RR2=0, RD1 = 6, RD2 = 6



WD=6 WR=0 WE=1 RR1=1 RR2=1, RD1 = 0, RD2 = 6



WD=3 WR=1 WE=1 RR1=0 RR2=0 , RD1 = 6, RD2 = 3

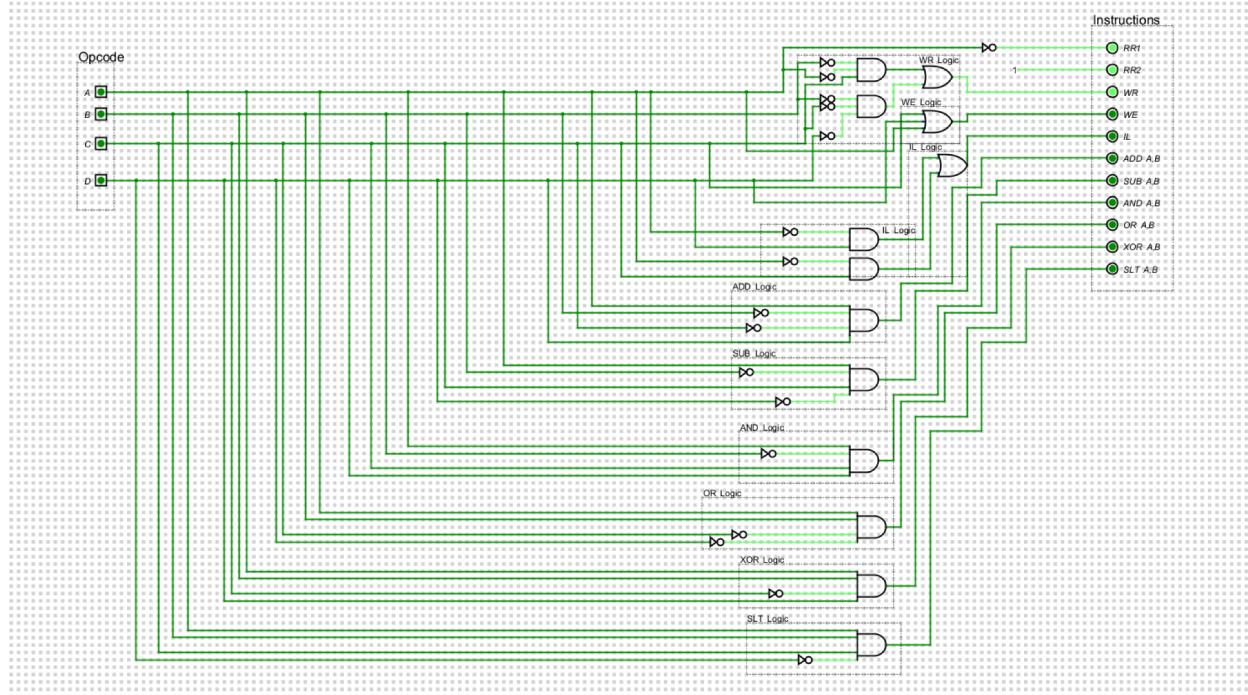


Decoder:

0000

Inputs: A = 0, B = 0, C = 0, D = 0

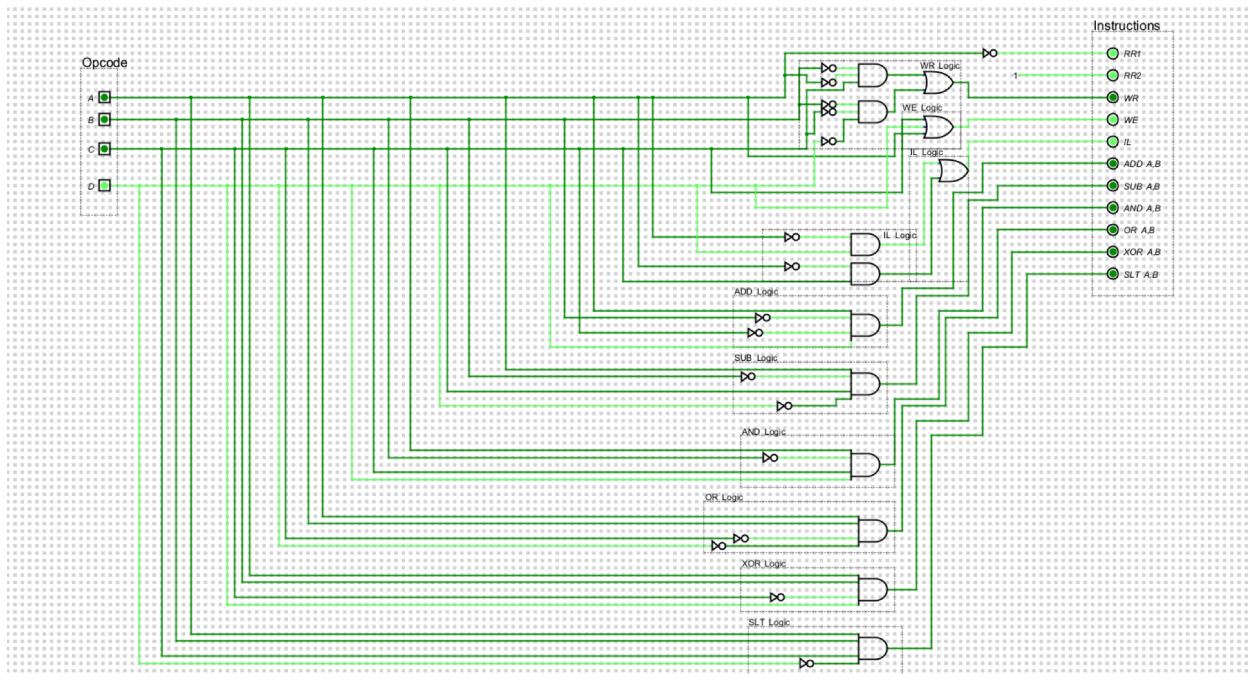
Outputs: RR1 = 1, RR2 = 1, WR = 1, WE = 0, IL = 0, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 0



0001

Inputs: A = 0, B = 0, C = 0, D = 1

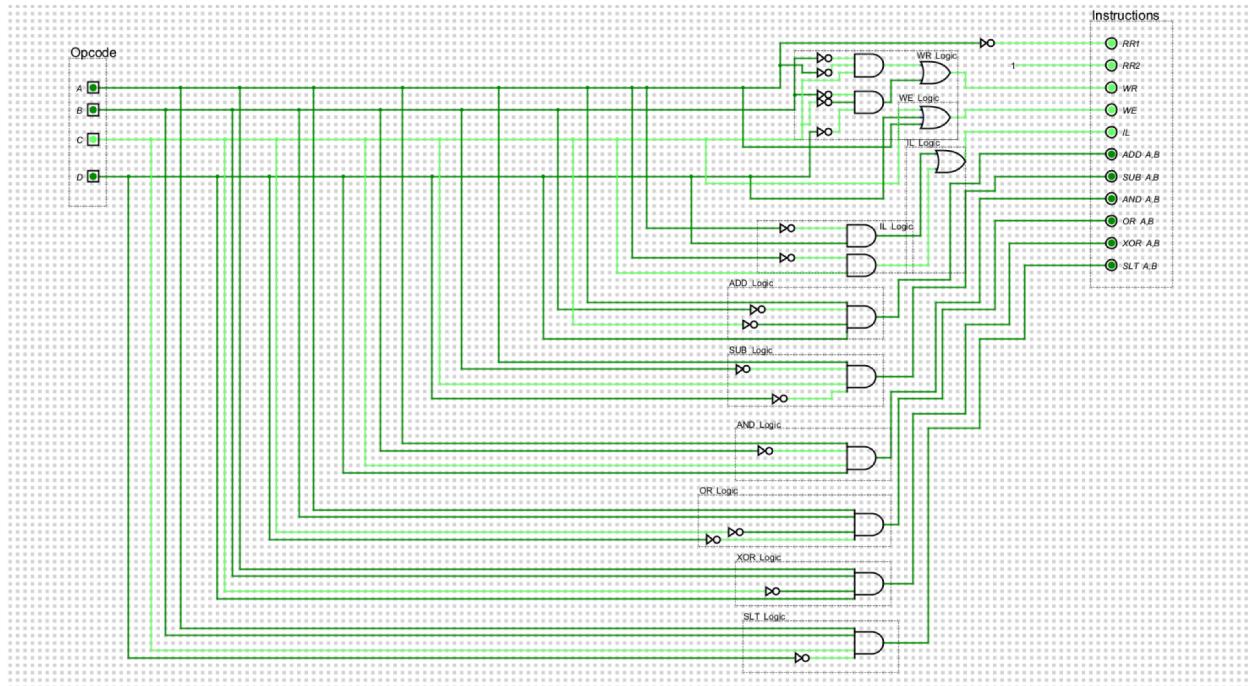
Outputs: RR1 = 1, RR2 = 1, WR = 0, WE = 1, IL = 1, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 0



0010

Inputs: A = 0, B = 0, C = 1, D = 0

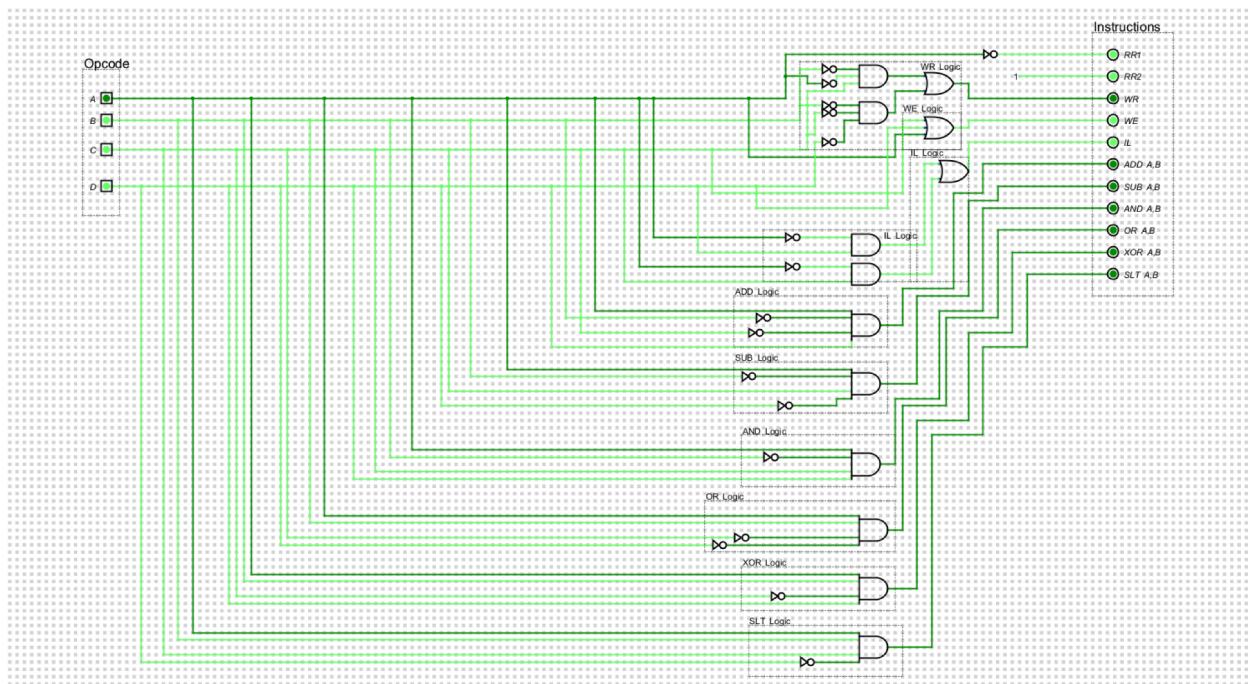
Outputs: RR1 = 1, RR2 = 1, WR = 1, WE = 1, IL = 1, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 0



0111

Inputs: A = 0, B = 1, C = 1, D = 1

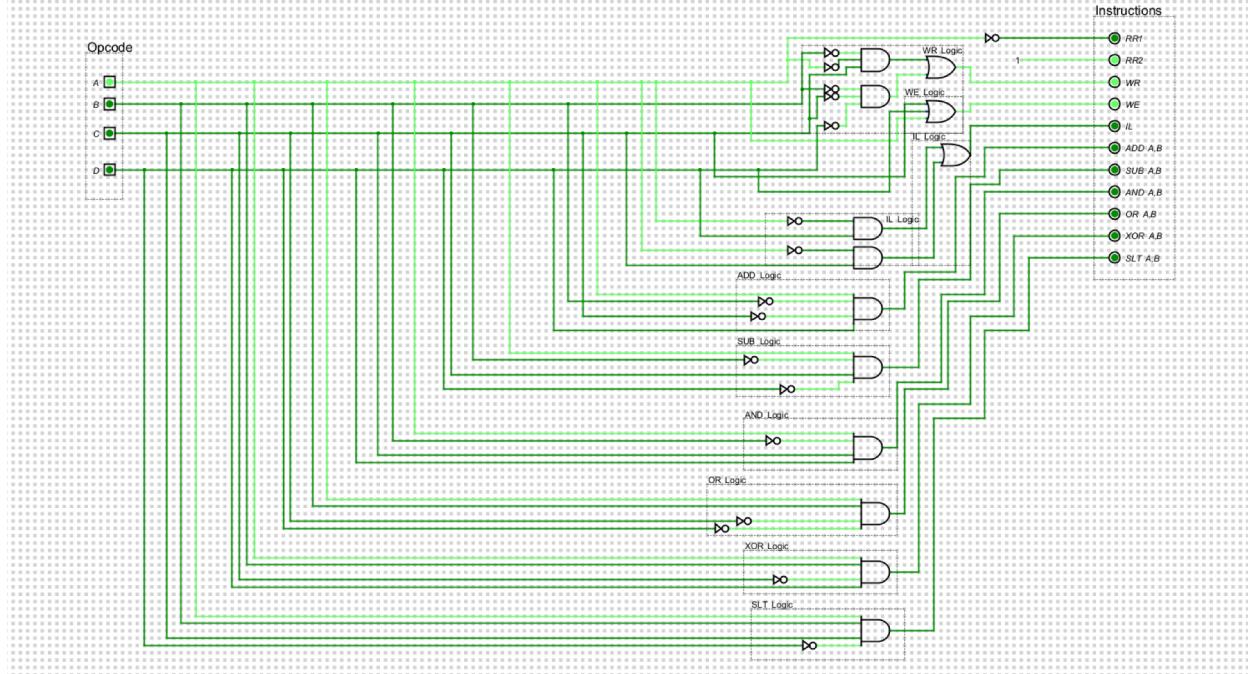
Outputs: RR1 = 1, RR2 = 1, WR = 0, WE = 1, IL = 1, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 0



1000

Inputs: A = 1, B = 0, C = 0, D = 0

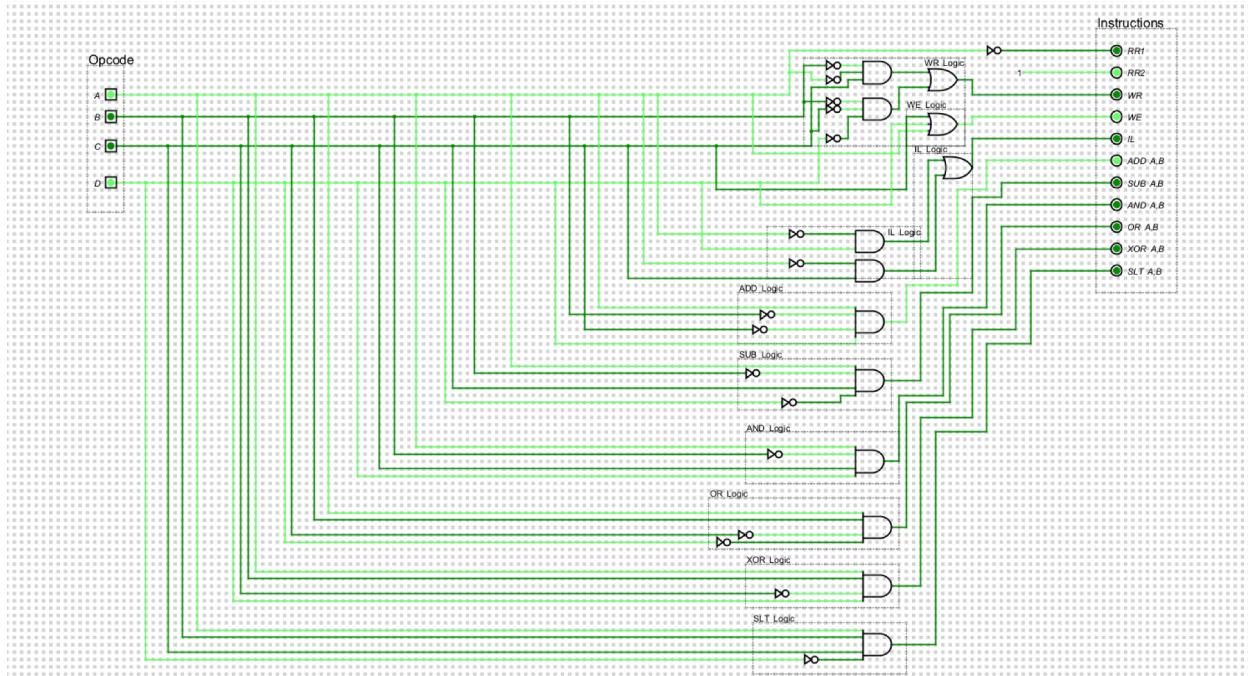
Outputs: RR1 = 0, RR2 = 1, WR = 1, WE = 1, IL = 0, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 0



1001

Inputs: A = 1, B = 0, C = 0, D = 1

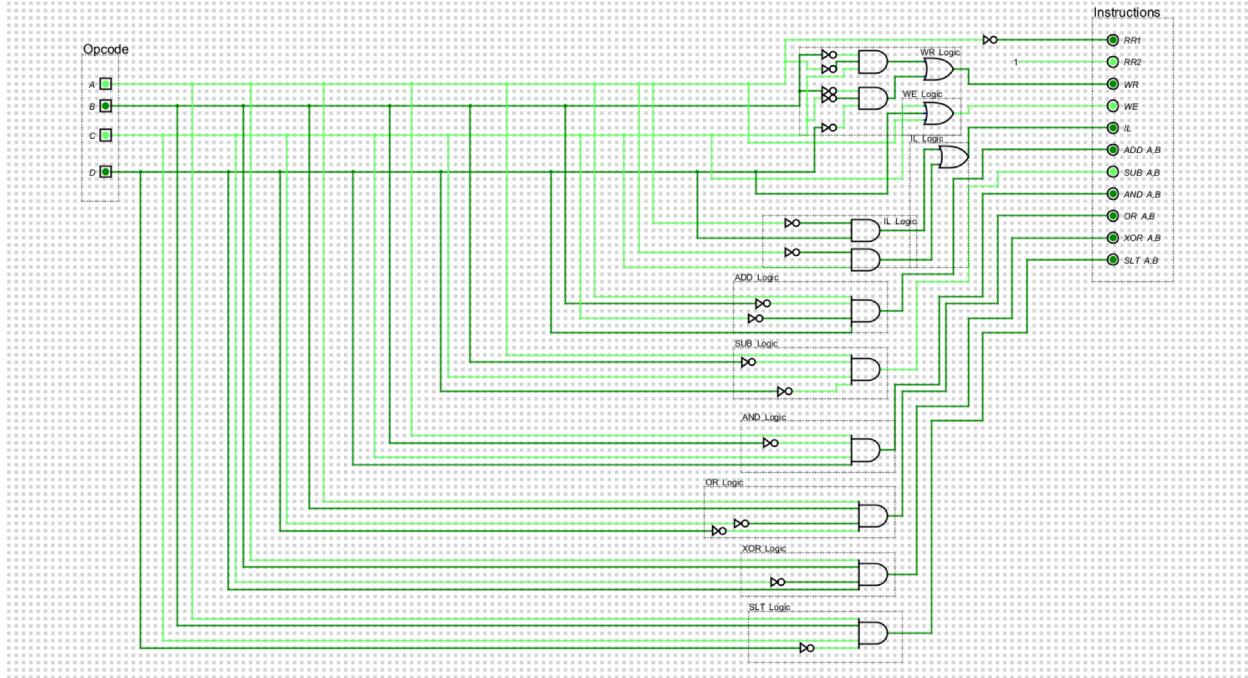
Outputs: RR1 = 0, RR2 = 1, WR = 0, WE = 1, IL = 0, ADD = 1, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 0



1010

Inputs: A = 1, B = 0, C = 1, D = 0

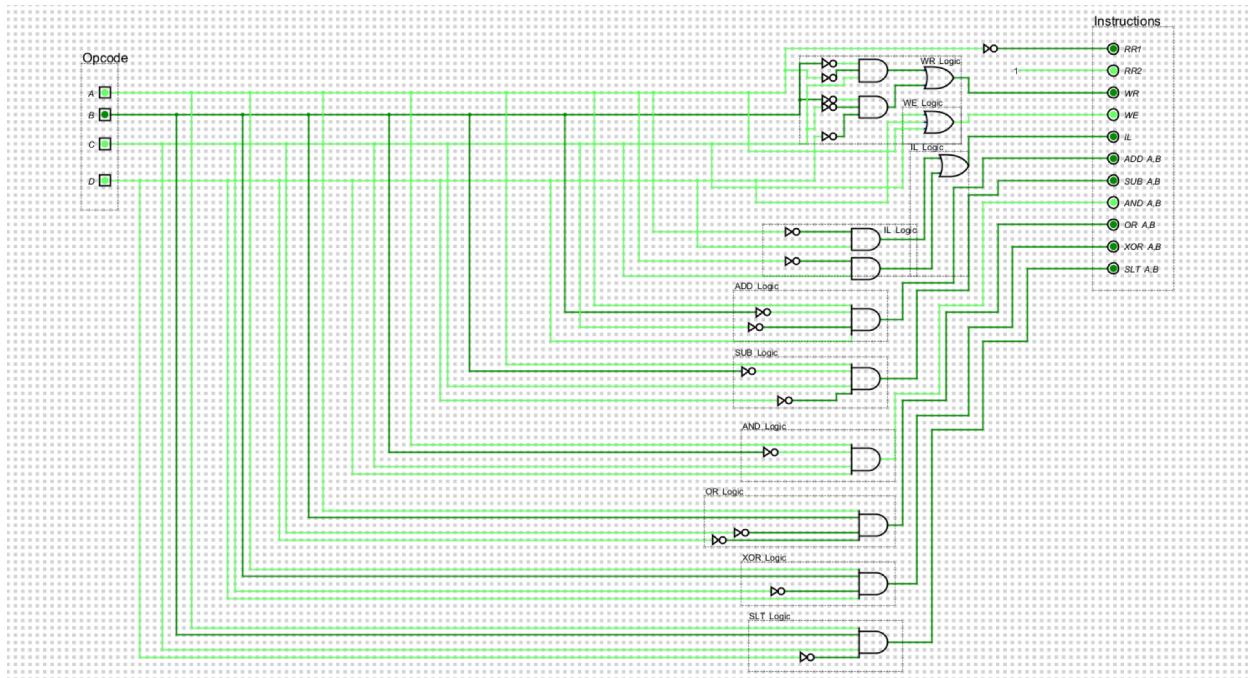
Outputs: RR1 = 0, RR2 = 1, WR = 0, WE = 1, IL = 0, ADD = 0, SUB = 1, AND = 0, OR = 0, XOR = 0, SLT = 0



1011

Inputs: A = 1, B = 0, C = 1, D = 1

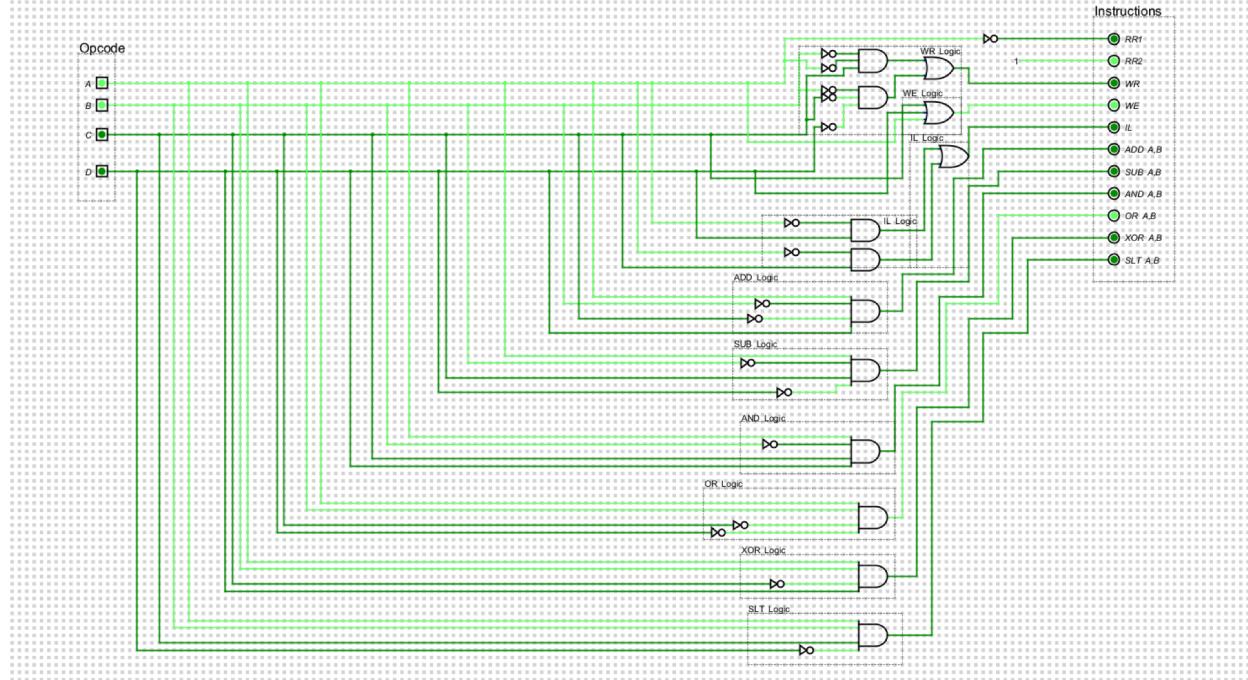
Outputs: RR1 = 0, RR2 = 1, WR = 0, WE = 1, IL = 0, ADD = 0, SUB = 0, AND = 1, OR = 0, XOR = 0, SLT = 0



1100

Inputs: A = 1, B = 1, C = 0, D = 0

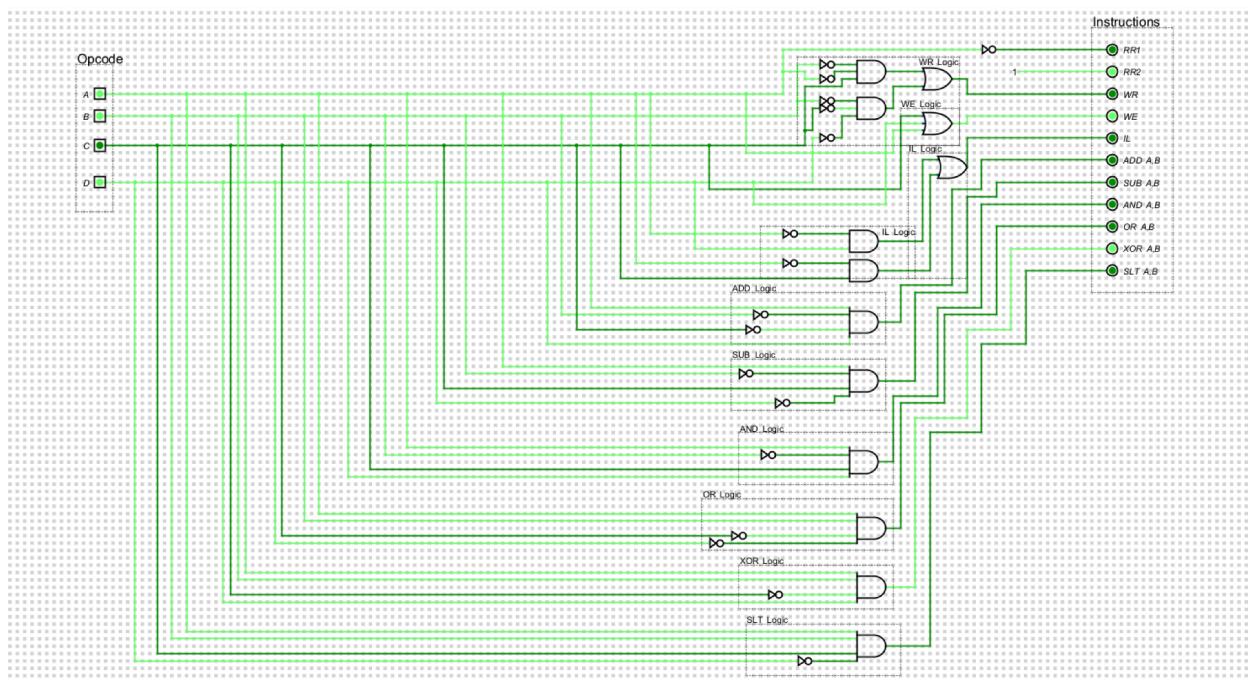
Outputs: RR1 = 0, RR2 = 1, WR = 0, WE = 1, IL = 0, ADD = 0, SUB = 0, AND = 0, OR = 1, XOR = 0, SLT = 0



1101

Inputs: A = 1, B = 1, C = 0, D = 1

Outputs: RR1 = 0, RR2 = 1, WR = 0, WE = 1, IL = 0, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 1, SLT = 0



1110

Inputs: A = 1, B = 1, C = 1, D = 0

Outputs: RR1 = 0, RR2 = 1, WR = 0, WE = 1, IL = 0, ADD = 0, SUB = 0, AND = 0, OR = 0, XOR = 0, SLT = 1

