ESE 330

Cadence Project: Part 3

DUE December 10th

Decoder design

Decoder Design in Dynamic Combinational CMOS Logic

You have to design 8-bit row decoder that converts 8 address bits into 256 wordlines with minimum possible delay using the logic effort. The maximum allowed capacitance on any address input is limited to 20.5 fF. The load capacitance at the wordline is $C_{wordline}$ = 8.5 pF.
You can implement the decoder with either 4 or 6 stages using domino logic, as shown in Figure 1 and Figure 2. Size the logic gates for the optimal delay from the rising edge of the clock using logic effort method and simulate the designed decoder in Cadence. How the delay compares to the delay obtained using static CMOS implementation?
In calculations, assume that the gate capacitance is C_g = 1.9 fF/μm, intrinsic delay of the inverter is t_{po} = 38 ps and γ = 1.

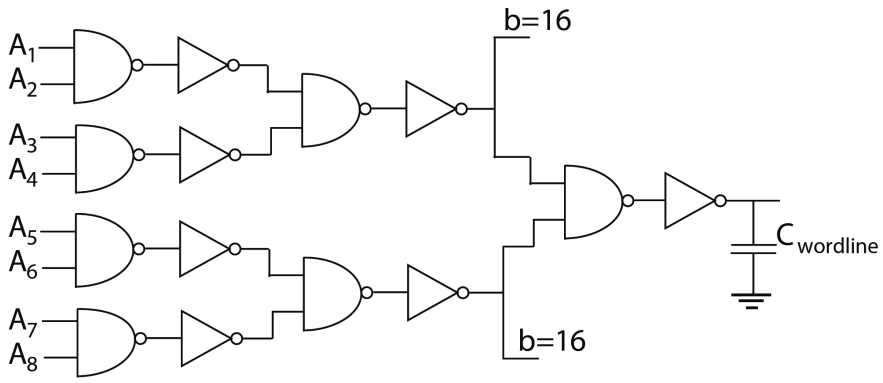

Figure 1. 6-stage implementation

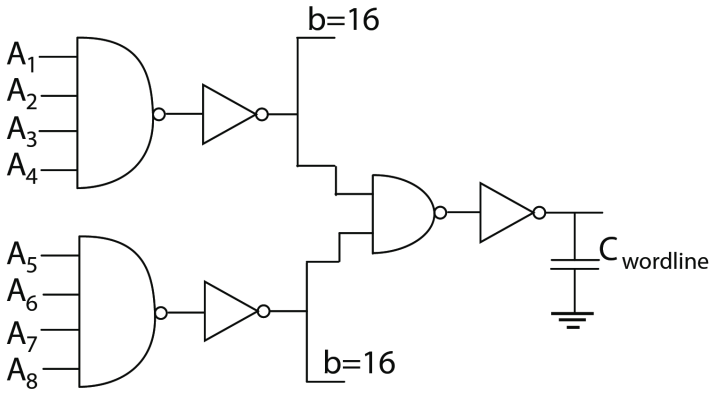

Figure 2. 4-stage implementation

REPORT

Please include in your report schematic plots with annotated transistor sizes. Include timing diagrams from Cadence that clearly demonstrate that your claimed results are true.