ESE 330

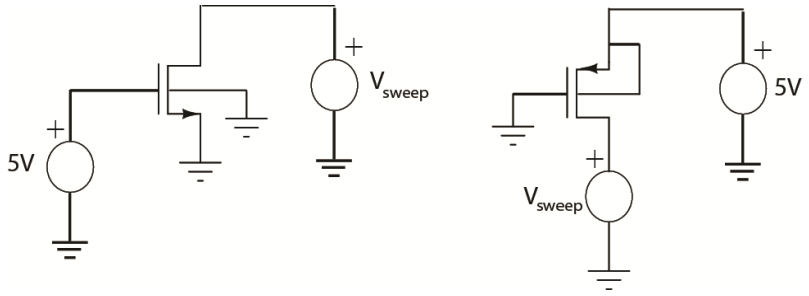
Cadence Project: Part 1

DUE October 31st

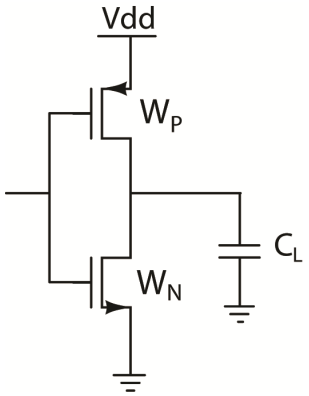
In both problems use the following parameters for 0.5 μm CMOS technology:
Vdd = 5V, $V_{Tn0} = 0.73V$, $k'_n = \mu_n C_{ox} = 115\mu A/V^2$, $V_{Tp0} = -0.94V$ and $k'_p = \mu_p C_{ox} = 37\mu A/V^2$.
You can use the long channel transistor characteristics.
To calculate transistor capacitances use the following parameters:
$C_{ox}=2.5\times10^{-3}F/m^2$, $L_S = L_D = 1.5$ μm
NMOS: $C_j = 4.16\times10^{-4}F/m^2$, $C_{jsw} = 3.26\times10^{-10}F/m$, $C_{GD0} = C_{GS0} = 1.93\times10^{-10}F/m$.
PMOS: $C_j = 7.1\times10^{-4}F/m^2$, $C_{jsw} = 2.18\times10^{-10}F/m$, $C_{GD0} = C_{GS0} = 2.28\times10^{-10}F/m$.
Assume $K_{eq} = 1$ and $K_{eqsw} = 1$ for both NMOS and PMOS transistor.

Problem 1:

a. Plot the I_d vs. V_{ds} characteristics of minimum sized NMOS and PMOS transistors ($W_N = 1.8\mu m$, $W_P=1.8\mu m$, $L_N=L_P=L=0.6\mu m$) and from these plots estimate R_{eqn} and R_{eqp} for 0.5 μm CMOS technology. R_{eq} is estimated as the average of $R_{on(Vout=Vdd)} = V_{dd}/I_{d(Vout=Vdd)}$ and $R_{on(Vout=Vdd/2)} = (V_{dd}/2)/I_{d(Vout=Vdd/2)}$. To plot I_d vs. V_{ds} of NMOS transistor use the following schematic and DC analysis. From R_{eqn} and R_{eqp} calculate R_{sqn} and R_{sqp}.



b. Use the values of R_{sqn} and R_{sqp} obtained from a. to calculate pull-down and pull-up times (t_{pHL} and t_{pLH}) when the inverter shown in Figure ($W_N = 1.8\mu m$, $W_P=3.6\mu m$, $L_N=L_P=L=0.6\mu m$) drives a capacitive load of 5pF (*note that the load capacitance is much greater than internal capacitance of the inverter, so the propagation delay can be estimates as only the external delay*). Simulate the inverter shown below using transient analysis (*assume an ideal step input voltage*) and obtain t_{pHL} and t_{pLH}. How these values compare to calculated ones?



c. Using the capacitance values for 0.5μm CMOS technology calculate the value of the internal capacitance of the inverter. Calculate the propagation delay of the inverter that drives a capacitive load of 10fF (*note that the load capacitance is comparable to the internal capacitance of the inverter, so in the calculation of the propagation delay both capacitances have to be included*). Simulate the inverter and compare the simulated propagation delays to calculated.

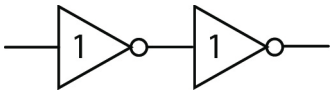
Problem 2: Chain of Inverters

a. First, we have to derive the important technology parameters that are essential in our propagation delay analysis. In the class, we derived the following expression for the delay:

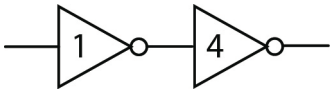
$$t_p = t_{p0}\,(1+f/\gamma)$$

where t_{p0} is the intrinsic delay of an inverter, f is the fanout, and $\gamma = C_{intrinsic}/C_{gate}$ is the ratio of the input intrinsic to the input gate capacitance.

We will determine the parameters of this equation (t_{po} and γ) through measurements of the propagation delay of the minimum size inverter (W_N =1.8μm, W_P=3.6μm, L_N=L_P=L=0.6μm) with two different loads. For the first circuit, measure a propagation delay of the minimum sized inverter with a load of the minimum sized inverter.

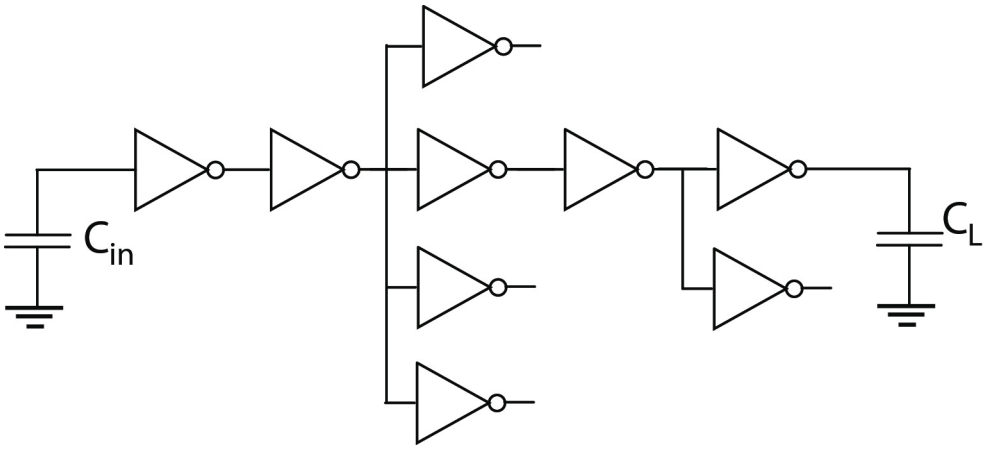


Then, measure a delay of the first inverter where the first inverter is the minimum sized and the second one is 4 times minimum size.



Using these two times, calculate t_{po} and γ.

b. Using calculated t_{po} and γ, optimize the circuit given in Figure below. Assume that the first inverter is the minimum size inverter (W_N =1.8μm, W_P=3.6μm, L_N=L_P=L=0.6μm) and that C_L = 256 C_{in} (C_{in} in the input capacitance of the minimum size inverter).



First, find the sizing of all the other inverters in the chain (W_N and W_P) to achieve the minimum delay D_{min} from the input to output. What is the value of D_{min} normalized to t_{p0}?

Using Cadence SpectreS, verify the result of your optimizations. How different is measured t_p from what the calculated value?

REPORT

Please include in your report schematic plots with annotated transistor sizes. Include timing diagrams from Cadence that clearly demonstrate that your claimed results are true. The project is done in a group of two students and only one report per group is required.