Digital System Design

ESE 218 – Section: L03

Lab 12. Direct Digital Synthesis

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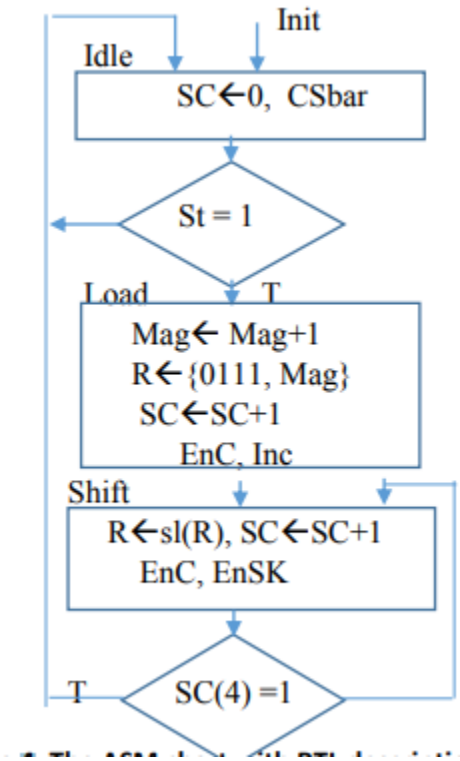
Objective:

The goal of this lab is to generate a saw-wave via Digital-to-Analog converter (DAC). This system design is composed of 2 counters: 1 being the magnitude counter and another being the serial clock counter, a 12-bit parallel-in-serial-out shift register and a controller. After the system is designed and tested via simulated waveforms, it was implemented using a FPGA (Ice40HX1k) and a DAC (MCP4801).

Description of the Design:

To obtain the system, first we needed each individual parts of the system. The Verilog code for the counter, PISO, and D- flip flop was given. We had to design the controller given the ASM chart. The ASM chart is as follows:



To design the controller, first the state diagram had to be obtained. Which was then used to find the state table. Using the state table, the excitation equations and the equations for the outputs were obtained. K-map was not used in this case. If there is one “1” in next state, it is an AND/NOR operation, if there are two “1” in the next state, it is a XOR/XNOR operation and if there are three ”1” in the next state, it is a OR/NAND operation. Using this logic, excitation equations as well as the equations for the outputs were obtained. The process is shown below:

States → R, I, S

Inputs → St, C

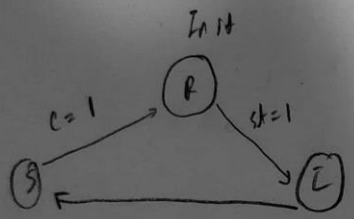
outputs → Cs_bar

Sclk ← EnSk

← Clk

EnC

InC



Q	Q_1	Q_0	Cs_bar	EnSk	EnC	InC
R	0	0	1	0	0	0
I	0	1	0	0	1	1
S	1	0	0	1	1	0
X	1	1	X	X	X	X

C = SC(1)

St, C = 00

Q^*	Q_1^*	Q_0^*
R	0	0
S	1	0
S	1	0
X	X	X

St, C = 01

Q^*	Q_1^*	Q_0^*
R	0	0
S	1	0
R	0	0
X	X	X

St, C = 10

Q^*	Q_1^*	Q_0^*
I	0	1
S	1	0
S	1	1
X	X	X

St, C = 11

Q^*	Q_1^*	Q_0^*
I	0	1
S	1	0
R	0	0
X	X	X

one 1 : AND, NOR

two 1's : XOR, XNOR, 1 b.0

three 1's : OR, NAND

$$Q_1^* = \bar{S}\bar{C}(Q_1 + Q_0) + \bar{S}CQ_0 + S\bar{C}(Q_1 + Q_0) + SCQ_0$$

$$= \bar{C}(Q_1 + Q_0)\underbrace{(\bar{S} + S)}_{=1} + CQ_0\underbrace{(S + \bar{S})}_{=1}$$

$$= \bar{C}Q_1 + \bar{C}Q_0 + CQ_0$$

$$Q_1^* = \bar{C}Q_1 + Q_0$$

$$Q_0^* = 0 + 0 + S\bar{C}(\overline{Q_0 \oplus Q_1}) + SC(\overline{Q_0 \oplus Q_1})$$

$$= S(\overline{Q_1 \oplus Q_0})$$

$$C_{S\_bar} = \overline{Q_1 \oplus Q_0}$$

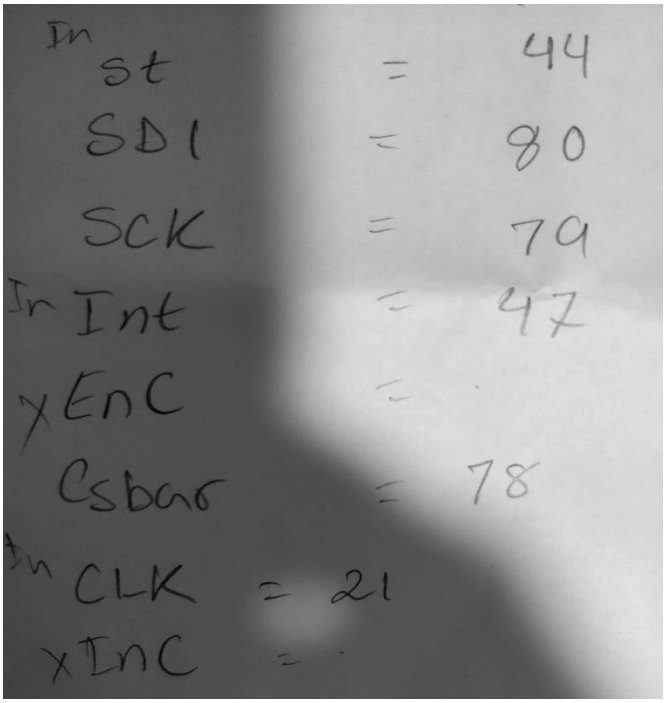
$$EnSk = Q_1$$

$$EnC = Q_1 + Q_0$$

$$EnP = Q_0$$

Description of the Experiment:

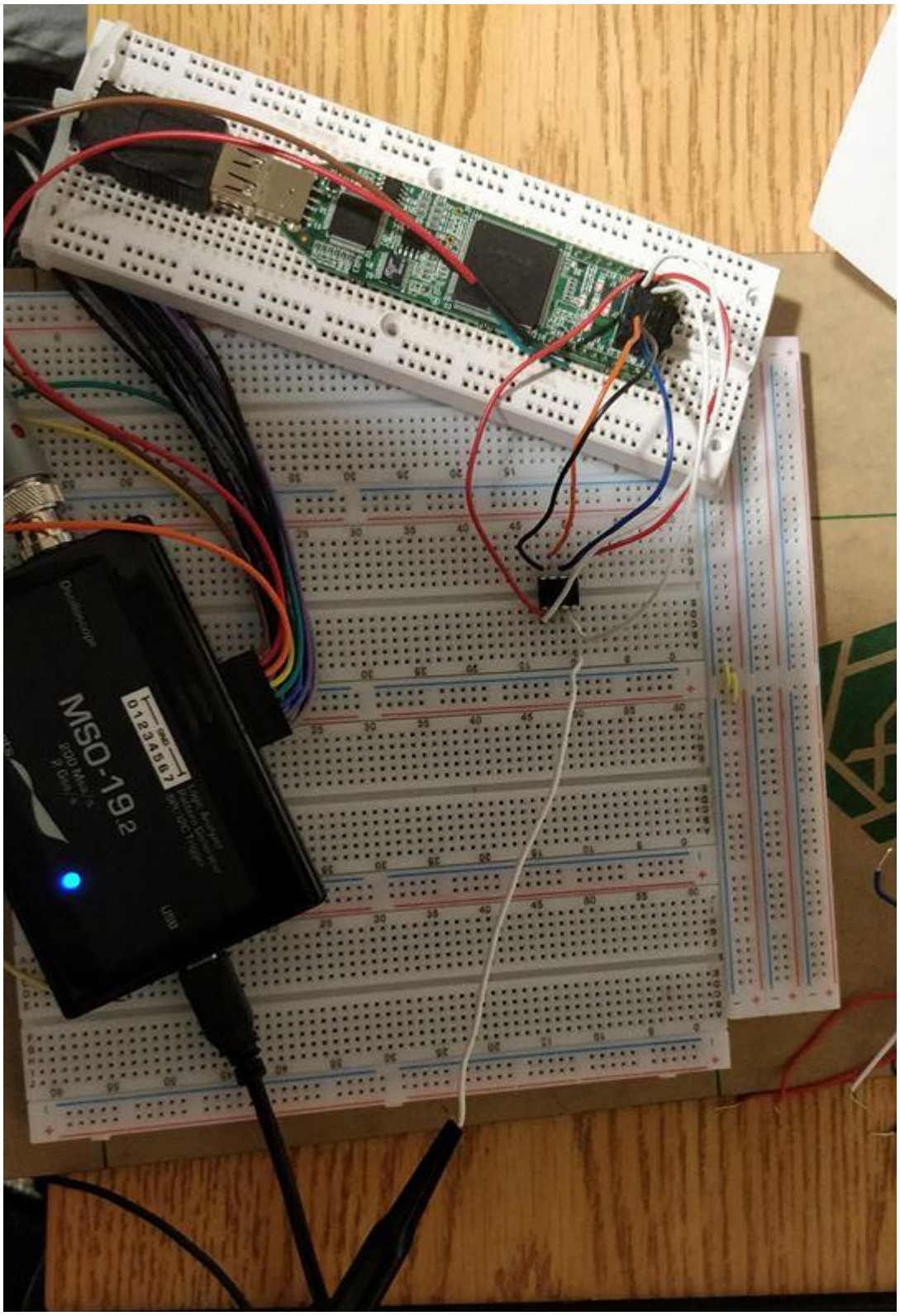
Using the iCEcube2 program, bitmap was generated using the ".v" files. The chosen pin locations for the FPGA are as follows:



The bitmap was then sent to Diamond programmer to program it. The next task was to connect the FPGA and DAC chip. For the DAC chip, the pin layouts are as follow

8	7	6	5
Vout	Gnd	Vdd	Gnd
1	2	3	4
Vdd	CSbar	SCK	SDI

The illustration of the circuit is as follows:



Data and Results:

Objective to approximate analog signal by concept of Direct Digital Synthesis using the help of an 8-bit DAC was carried out in this laboratory experiment. Preliminary set-up for laboratory experiment was done in prelab portion of this lab. Following instruction provided in lab manual a bitmap of Top level schematic was obtained to program FPGA unit. DAC: MCP4801 was connected to appropriate pin layouts setup from FPGA. Signal generator MS0-19 provided Start and Initial signals to be used as inputs to the system and internal clock of FPGA was accessed from pin 21 to be used as system Clock. Followings are the waveform obtained from DAC output using analog probe.

Figure 1 : Saw-Wave obtained from DAC output terminal.

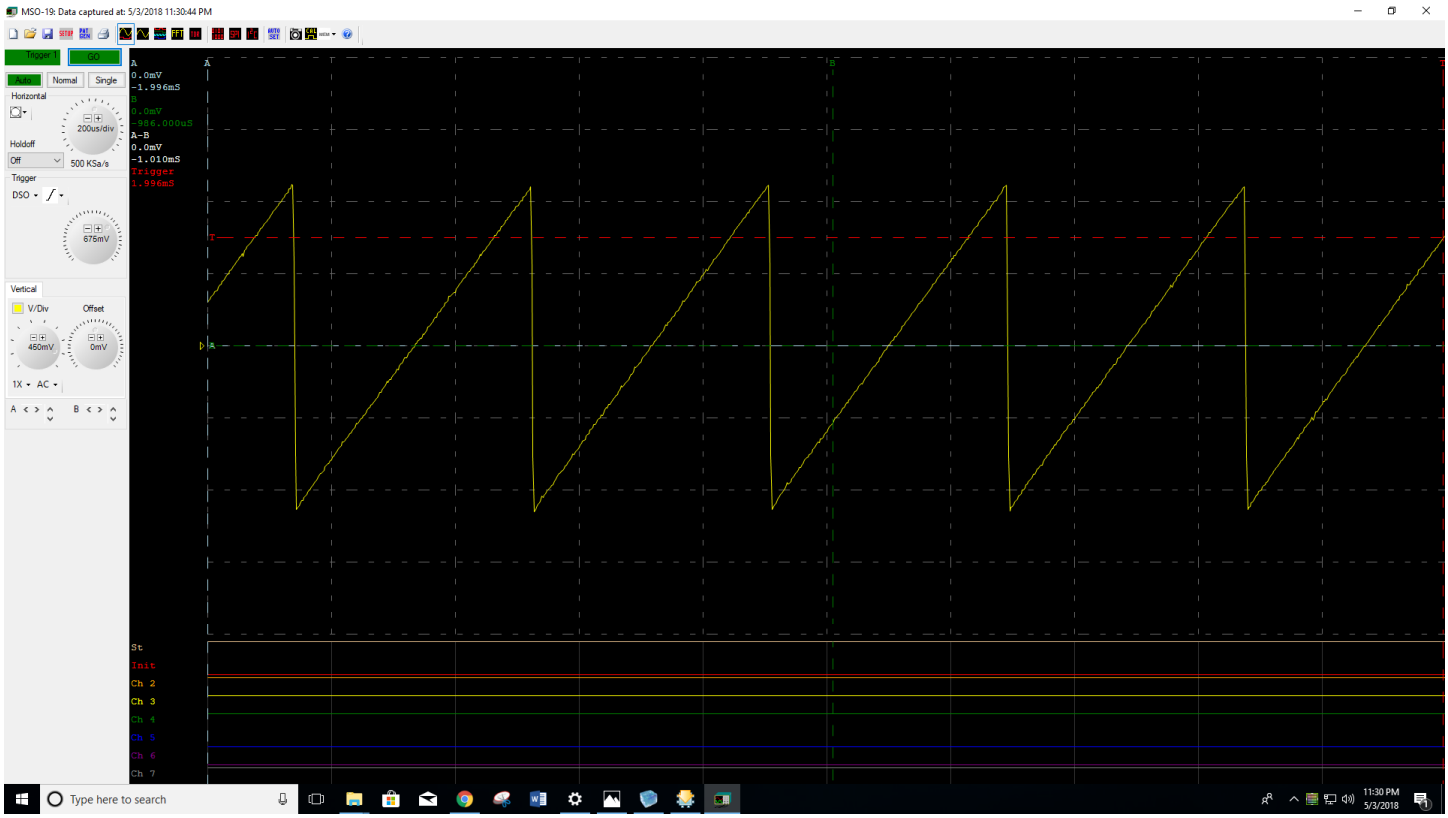


Figure 2: A closer look at waveform obtained from DAC Output terminal.

Using pattern generator, St = 1 and Init = 1→0 was obtained as input signals to the system. Clock was accessed from internal pin 21 from FPGA. All outputs from FPGA such as CSbar, SDI and SCK was connected appropriately to DAC: MCP4801. Output waveforms from pin 8 of DAC was observed on windows software provided by MSO-19 signal generator.

Above analog signal resembles a saw, hence the Saw-wave. By analyzing the wave, we can denote that a repetitive process taking place. From start of the signal a constant positive slope goes to “peak” then performs a vertical drop. This process occurs over again for each cycle of SCK clock, generating a Saw-Wave. The goal of this lab was successfully implemented using the help of Hardware descriptive Language, FPGA and a DAC.