Cadence Project

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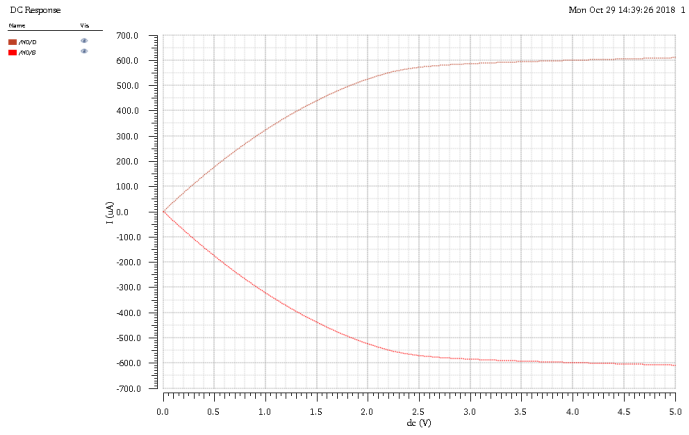
ESE 330.01 - Integrated Electronics

1 Problem 1

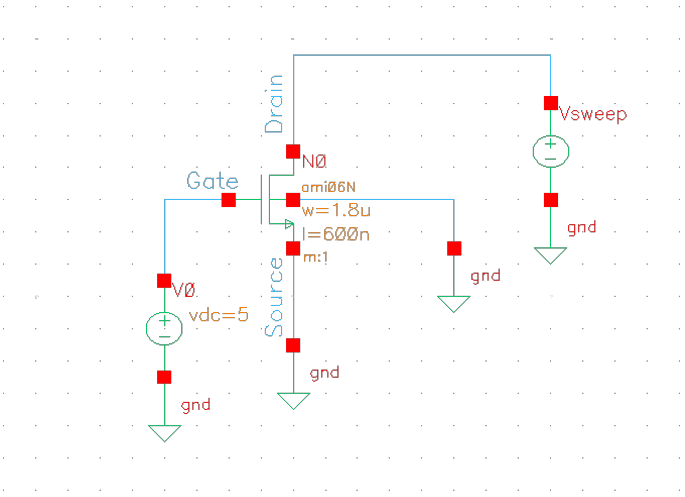
1.1 Part a

The values implemented in the calculations throughout secion 1.1 are as follows:

$$
\begin{aligned}
W_n &= W_p = 1.8\mu m \\
L_N &= L_P = 0.6\mu m \\
R_{on(Vout=Vdd)} &= V_{dd}/I_{d(Vout=Vdd)} \\
R_{on(Vout=Vdd/2)} &= (V_{dd}/2)/I_{d(Vout=Vdd/2)} \\
R_{eq} &= \frac{R_{on(Vout=Vdd)} + R_{on(Vout=Vdd/2)}}{2}
\end{aligned}
$$



(a) I_d vs. V_{ds}



(b) NMOS schematic

Figure 1: Data from NMOS circuit

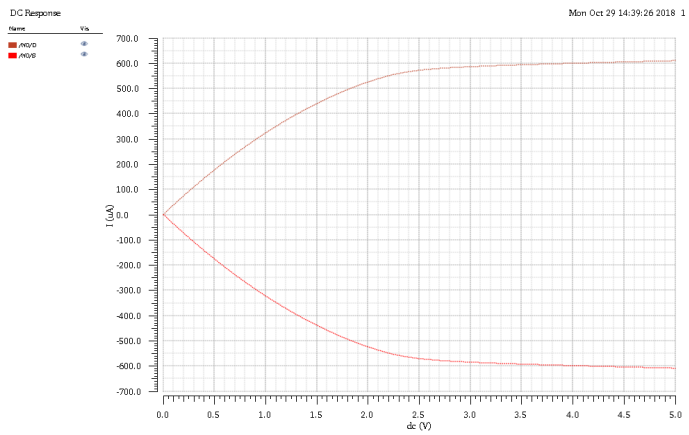
1.1.1 NMOS calculations

(Values from figure 1a)

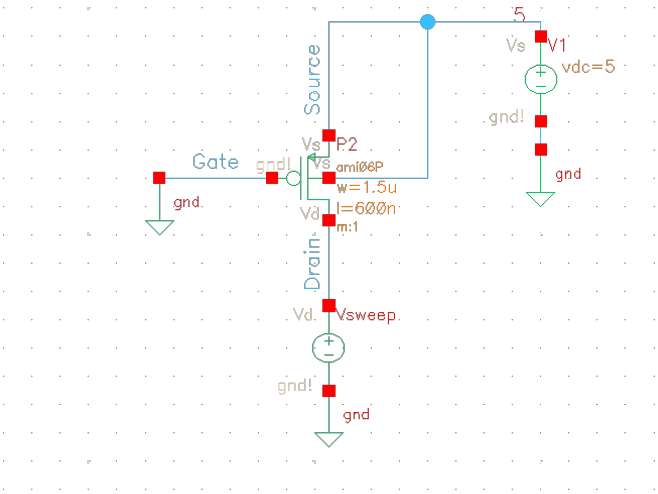
$$\begin{aligned} R_{on(Vout=Vdd)} &= \frac{V_{dd}}{I_{d(Vout=Vdd)}} \\ &= \frac{5.0V}{610\mu A} \\ &= 8.33k\Omega \end{aligned} \tag{1}$$

$$\begin{aligned} R_{on(Vout=Vdd/2)} &= \frac{V_{dd}/2}{I_{d(Vout=Vdd/2)}} \\ &= \frac{5.0V}{575\mu A} \\ &= 8.70k\Omega \end{aligned} \tag{2}$$

$$\begin{aligned} R_{eqn} &= \frac{R_{on(Vout=Vdd)} + R_{on(Vout=Vdd/2)}}{2} \\ &= \frac{8.70k\Omega + 8.33k\Omega}{2} \\ &= 8.515k\Omega \end{aligned} \tag{3}$$



(a) I_d vs. V_{sd}



(b) PMOS schematic

Figure 2: Data from PMOS circuit

The plots shown in figures 1a and 2a show both the current through the drain (upper curve) and the source (lower curve). This was achieved by sweeping the voltage of V_{sweep} from 0.0V to 5.0V and tracking the response. The resulting current measured at varying voltage was used for resistance calculations.

1.1.2 PMOS calculations

(Values from figure 2a)

$$\begin{aligned} R_{on(Vout=Vdd)} &= \frac{V_{dd}}{I_{d(Vout=Vdd)}} \\ &= \frac{5.0V}{310\mu A} \\ &= 16.13k\Omega \end{aligned} \tag{4}$$

$$\begin{aligned} R_{on(Vout=Vdd/2)} &= \frac{V_{dd}/2}{I_{d(Vout=Vdd/2)}} \\ &= \frac{5.0V}{260\mu A} \\ &= 19.23k\Omega \end{aligned} \tag{5}$$

$$\begin{aligned} R_{eqp} &= \frac{R_{on(Vout=Vdd)} + R_{on(Vout=Vdd/2)}}{2} \\ &= \frac{16.13k\Omega + 19.23k\Omega}{2} \\ &= 17.68k\Omega \end{aligned} \tag{6}$$

1.2 Part b

In this section, we use the following values to simulate the inverter seen in figure 3:

$$\begin{aligned} W_n &= 1.8\mu m \\ W_p &= 3.6\mu m \\ L_N = L_P &= 0.6\mu m \\ C_{load} &= 5pF \end{aligned}$$

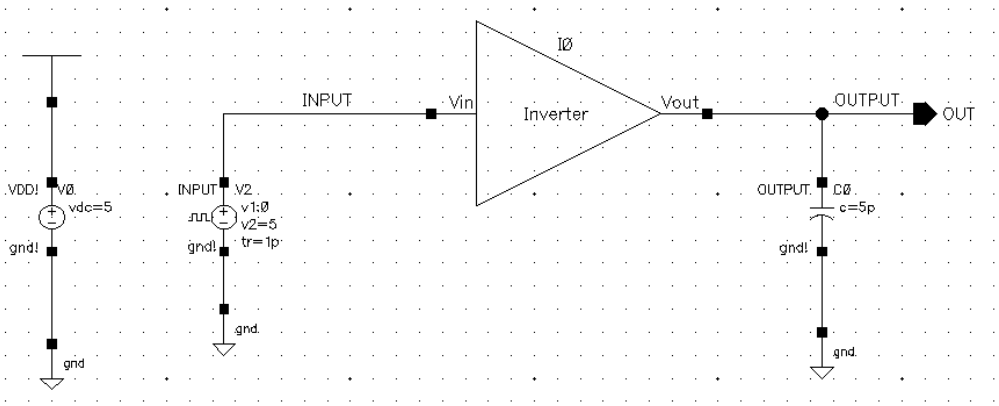


Figure 3: Inverter created using values from equations 6 and 5

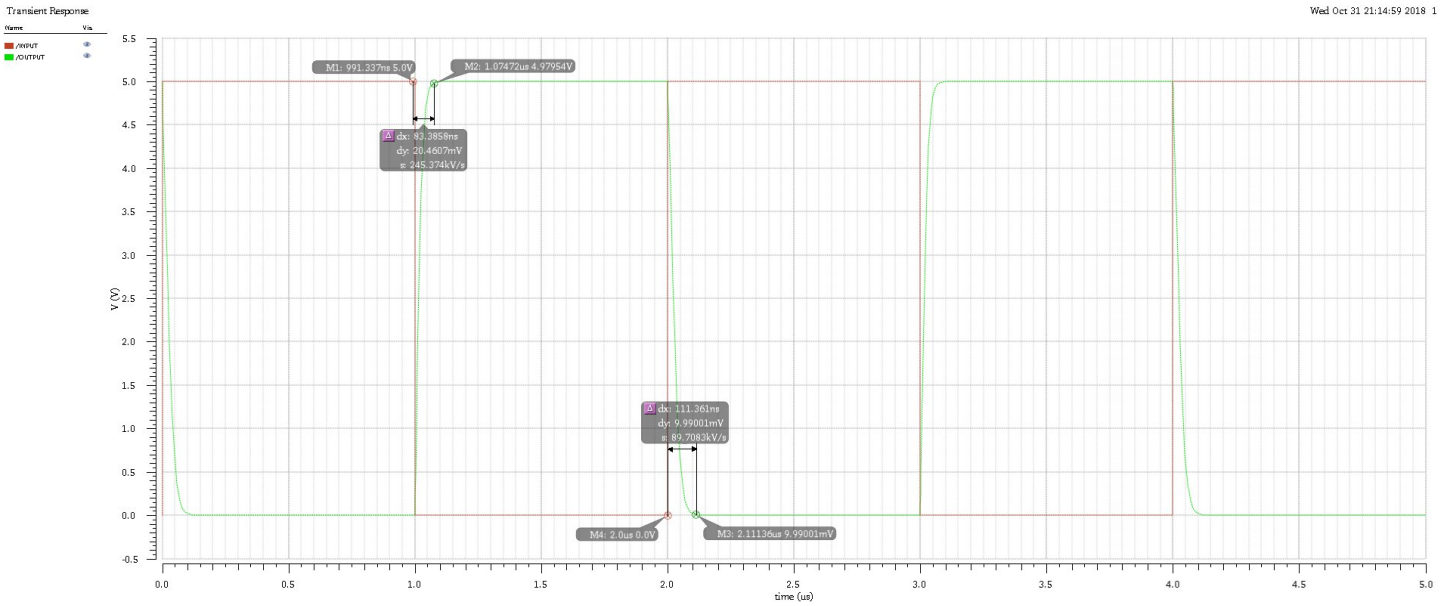


Figure 4: Inverter waveform:
The red signal represents the inverter input and the green represents the output.

1.2.1 Simulation values

By analyzing the waveform (figure 4), we can see clearly the values of t_{pHL} and t_{pLH}.

$$t_{pHL} = 111.36ns$$
$$t_{pLH} = 83.39ns$$

1.2.2 Calculation values

Calculating timing values:

$$\begin{aligned} t_{pHL} &= 0.69 * R_{eqn} * C_{load} \\ &= 0.69 * 8.515k\Omega * 5pF \\ &= 29.38ns \end{aligned} \tag{7}$$

$$\begin{aligned} t_{pLH} &= 0.69 * R_{eqp} * C_{load} \\ &= 0.69 * 17.68k\Omega * 5pF \\ &= 61.00ns \end{aligned} \tag{8}$$

1.3 Part c

C_{load} changes from 5 pF to 10 fF.

1.3.1 Calculated values

Calculating C_{DB1} (PMOS):

$$\begin{aligned} C_{DB} &= K_{eq} * C_j * L_D * W_P + K_{eqsw} * C_{jsw} * (2 * L_D * W_P) \\ &= 1 * (7.1 * 10^{-4} F/m^2) * 1.5\mu m * 3.6\mu m + 1 * (2.18 * 10^{-10} F/m) * (2 * 1.5\mu m * 3.6\mu m) \\ &= 3.83fF \end{aligned} \tag{9}$$

Calculating C_{DB2} (NMOS):

$$\begin{aligned} C_{DB} &= K_{eq} * C_j * L_S * W_N + K_{eqsw} * C_{jsw} * (2 * L_S * W_N) \\ &= 1 * (4.16 * 10^{-4} F/m^2) * 1.5\mu m * 1.8\mu m + 1 * (3.26 * 10^{-10} F/m) * (2 * 1.5\mu m * 1.8\mu m) \\ &= 1.12fF \end{aligned} \tag{10}$$

Calculating internal inverter capacitance:

$$\begin{aligned} C_{internal} = C_{Self} &= 2 * C_{GD01} + 2 * C_{GD02} + C_{DB1} + C_{DB2} \\ &= 2 * 0.228nF + 2 * 0.193nF + 3.83fF + 1.12fF \\ &= 0.842nF \end{aligned} \tag{11}$$

Propagation delay of an inverter with a $C_{internal}$ value of 0.842 nF that drives a 10 fF load:

$$\begin{aligned} t_p &= \frac{t_{pHL} + t_{pLH}}{2} * C_L \\ &= \frac{111.36ns + 83.39ns}{2} * 10fF \\ &= 97.375ns \end{aligned} \tag{12}$$

1.3.2 Simulated values

When the inverter was simulated with a 10fF load (figure), the propagation delay was notably different then the values expected through calculation:

$$\begin{aligned} t_{pHL} &= 470ns \\ t_{pLH} &= 396ns \\ t_p &= 433ns \end{aligned}$$

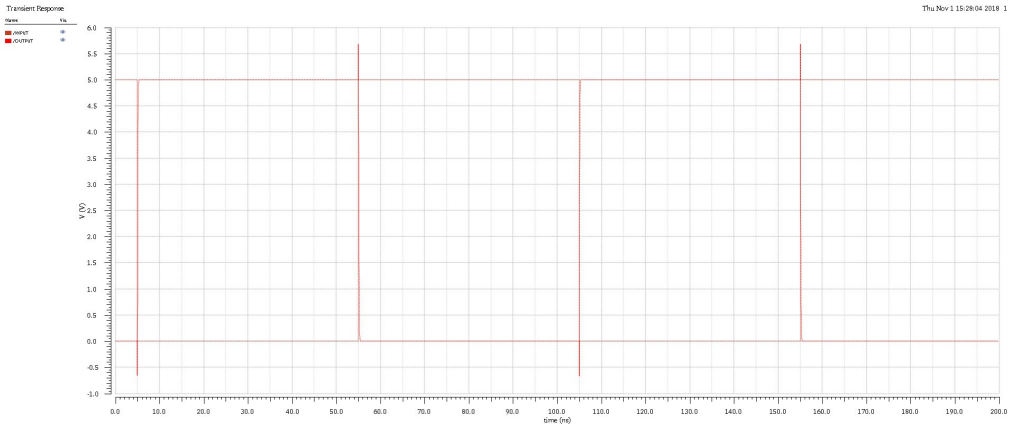


Figure 5: Input and output signals with a 10fF load.

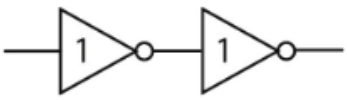
2 Problem 2

2.1 Part a

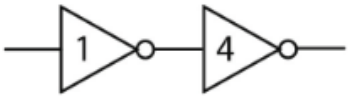
Values used when simulating the inverter chain (figure 7):

$$\begin{aligned} W_{Nmin} &= 1.8\mu m \\ W_{Pmin} &= 3.6\mu m \\ 4 * W_{Nmin} &= 7.2\mu m \\ 4 * W_{Pmin} &= 14.4\mu m \\ L_N = L_P &= 0.6\mu m \\ C_L &= 256 * C_{in} \\ C_{intrinsic} &= 0.842nF \end{aligned}$$

The chain is simulated twice. First with two identical inverters, both sized with the minimum values. The second simulation replaces the second inverter in the chain with an inverter four times the original size. In both simulations (sections 2.1.1 and 2.1.2), the delay of the output of the first inverter is measured.



(a) Two minimum sized inverters



(b) One minimum sized inverter, one four times minimum size inverter

Figure 6: Inverter chain configuration for delay measurement

Delay expression:

$$t_p = t_{p0} * (1 + f/\gamma) \tag{13}$$

where t_{p0} is the intrinsic inverter delay, f is the fanout, and $\gamma = C_{intrinsic}/C_{gate}$. When calculating γ, the value for $C_{intrinsic}$ sill be the value determined in equation 11.

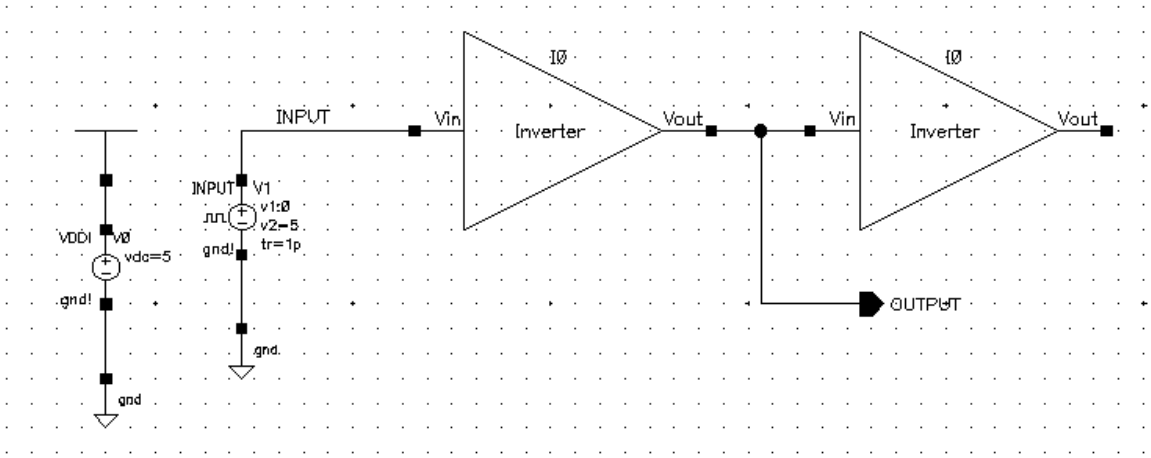
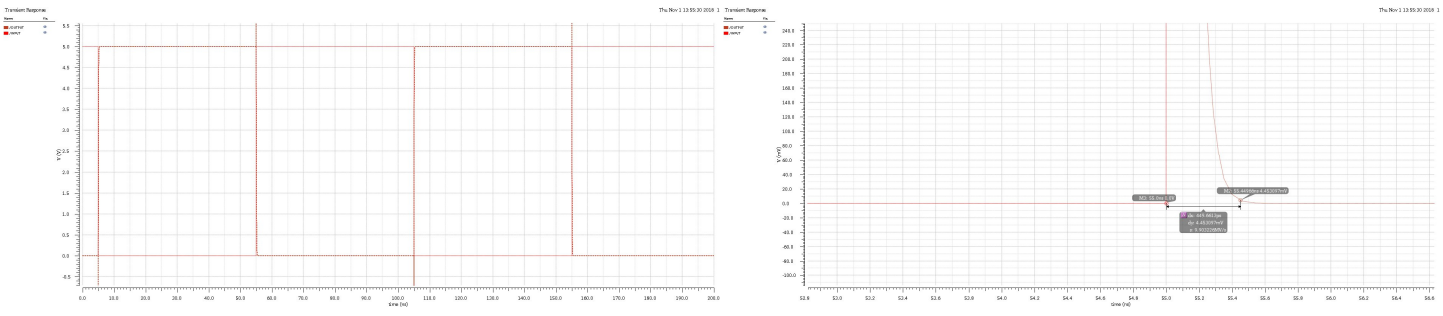


Figure 7: Inverter chain

2.1.1 Minimum sized inverter

The delay simulated for two minimum sized inverters was approximately 0.35 ns.



(a) Input and output of first inverter

(b) Shown: t_{pHL} of Inverter 1 = 0.50 ns

Figure 8: Measurements for inverter chain delay

$$
\begin{aligned}
t_p =& \frac{t_{pHL} + t_{pLH}}{2} \\
t_p =& \frac{0.5ns + 0.35ns}{2} \\
t_p =& 0.35ns
\end{aligned}
\tag{14}
$$

Calculating the value for C_{gate}:

Calculating C_{fanout}:

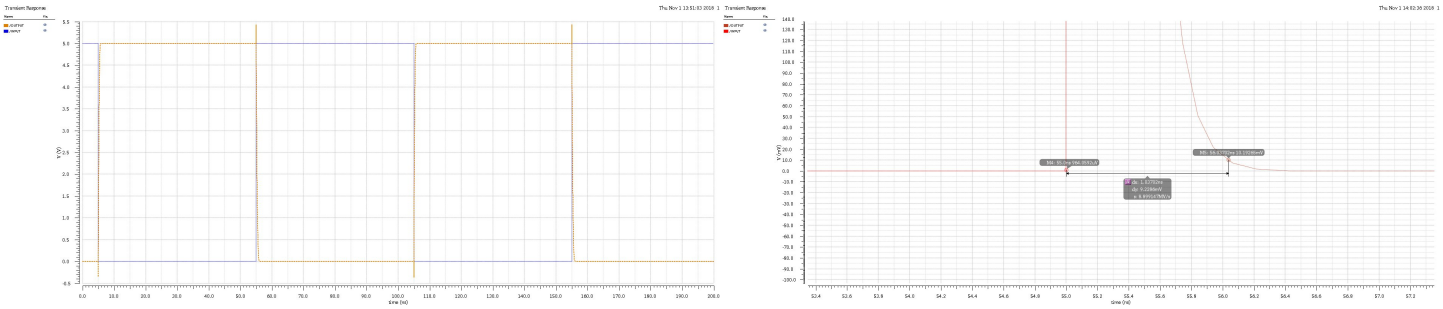
$$
\begin{aligned}
C_{fanout} &= (C_{GS03} + C_{GD03} + W_3 * L_3 * C_{ox}) + (C_{GS04} + C_{GD04} + W_4 * L_4 * C_{ox}) \\
&= ((2.28 * 10^{-10} F/m) + (2.28 * 10^{-10} F/m) + 3.6\mu m * 0.6\mu m * (2.5 * 10^{-3} F/m^2)) \\
&+ ((1.93 * 10^{-10} F/m) + (1.93 * 10^{-10} F/m) + 1.8\mu m * 0.6\mu m * (2.25 * 10^{-3} F)) \\
&= 824pF
\end{aligned}
\tag{15}
$$

Calculating γ:

$$\begin{aligned}\gamma &= C_{intrinsic}/C_{gate} \\ &= 842nF/824pF \\ &= 1.02\end{aligned} \tag{16}$$

2.1.2 Four times minimum size

The simulation was then repeat with the first inverter untouched. The second inverter was replaced with a similar inverter four times the minimum size. The measured delay in this configuration was approximately 0.95 ns.



(a) Input and output of first inverter

(b) Shown: t_{pHL} of Inverter 1 = 1.04 ns

Figure 9: Measurements for inverter chain delay

$$\begin{aligned}t_p =& \frac{t_{pHL} + t_{pLH}}{2} \\ t_p =& \frac{1.04ns + 0.85ns}{2} \\ t_p =& 0.945ns\end{aligned} \tag{17}$$

Calculating the value for C_{gate}:

The equation used here is the same as the one seen in the previous section. The only difference is the value of the width in C_{gate}, which is four times larger than previously seen.

Calculating C_{fanout}:

$$\begin{aligned}C_{fanout} &= (C_{GS03} + C_{GD03} + W_3 * L_3 * C_{ox}) + (C_{GS04} + C_{GD04} + W_4 * L_4 * C_{ox}) \\ &= ((2.28 * 10^{-10}F/m) + (2.28 * 10^{-10}F/m) + 14.4\mu m * 0.6\mu m * (2.5 * 10^{-3}F/m^2)) \\ &+ ((1.93 * 10^{-10}F/m) + (1.93 * 10^{-10}F/m) + 7.2\mu m * 0.6\mu m * (2.25 * 10^{-3}fF)) \\ &= 842pF\end{aligned} \tag{18}$$

Calculating γ:

$$\begin{aligned}\gamma &= C_{intrinsic}/C_{gate} \\ &= 842nF/824pF \\ &= 1.02\end{aligned} \tag{19}$$

We can see here that the change in value of γ when the size of the load inverter is increased is negligible.

Calculating t_{p0}:

When calculating the value of t_{p0}, we need, first, to rearrange equation 13. Doing so, we are left with:

$$t_{p0} = \frac{t_p}{(1 + f/\gamma)} \tag{20}$$

2.2 Part b