Digital System Design

ESE 218 – Section: L03

Bonus Lab: Analog to Digital Converter

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Roni Das : 108378223

Roni Das ESE:218 :L03

ID:108378223 Bonus Lab

The **Objective** of this lab is to Design Master controller based on IceStick FPGA with SPI-compatible protocol for communication with 10-bit ADC MCP3001. Datasheet for MCP3001 was thoroughly revised and requirements noted down.

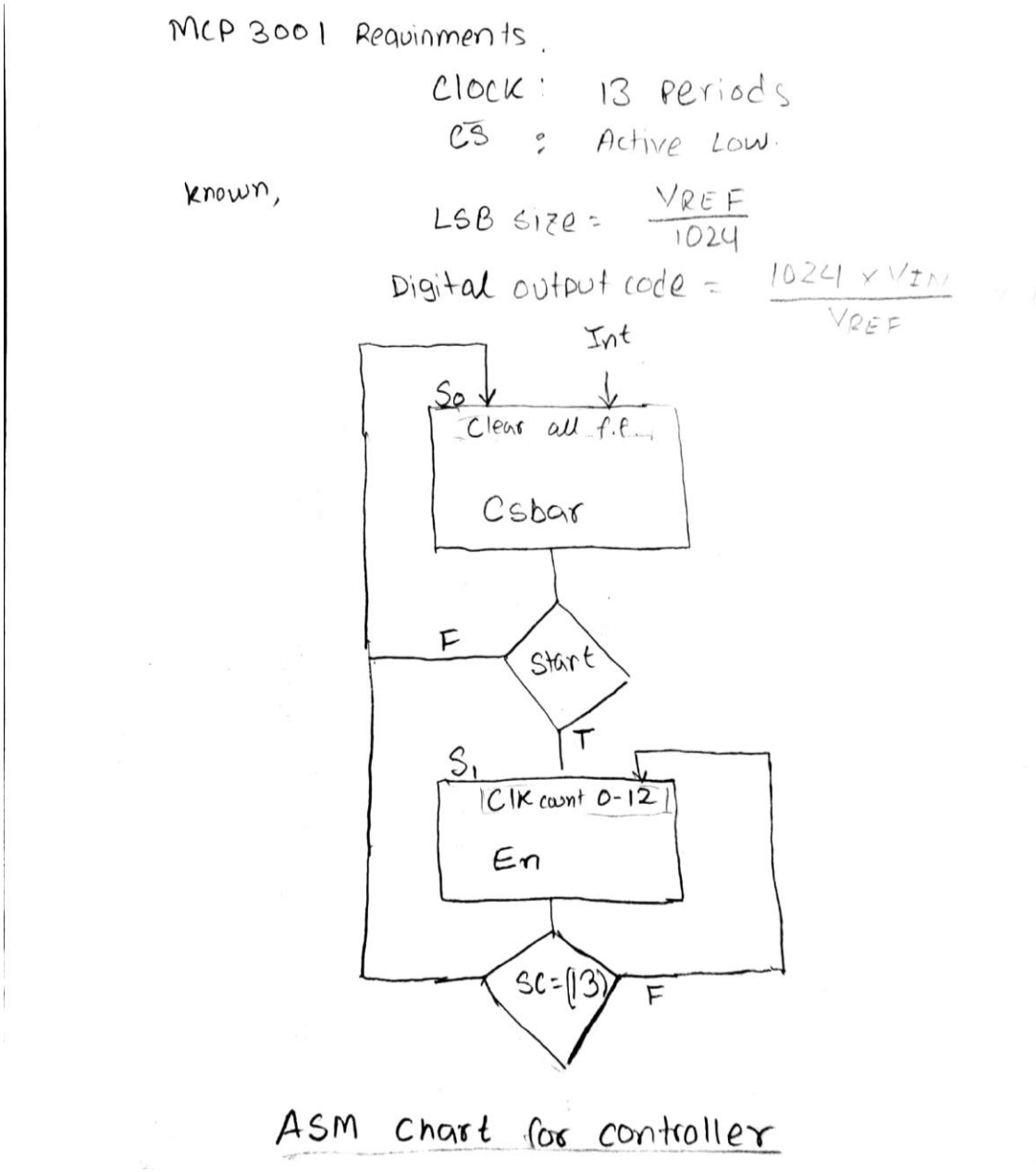
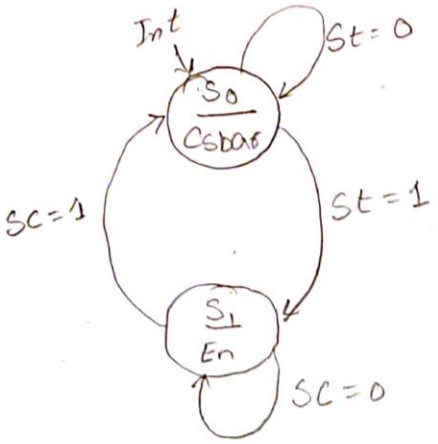


Figure 1: Controller design.

Approaches taken to reach objective as follows:

Design a control unit in Hardware descriptive language which will communicate with MCP3001 via programmable FPGA. From Datasheet of MCP3001 is was noted that It requires 13 clock periods to calculated after CSbar has been pulled down. Our goal is to provide these 13 clock periods to MCP3001 with the help of a counter. ADC provides, MSB first , at falling edge starting from 3rd Clock pulse. Data Out from ADC is then feed into a 10-bit Serial In Parallel Out Shift Register to observe ADC values.

SPI Master consists of Controller, a 10-bit SIPO SR and a 4-bit Up counter. System starts upon initialization = 1; Before initialization states of the flip flops are unknown. With Int= 1, CSbar goes Hight clearing all flips flops incident to system. CSbar is also applied to ADC, putting it into high impedance mode. System idles at this state (S0) , until Starts = 1. With St=1 ; Csabar goes down and Enable set to High. With Enable =1 , Counter starts counting from 0 as clock pulses are provided to ADC and other components of the system. With SC= 1 at 13 ; Csbar goes High and count stops, En = 0 ; setting the state back to S0. Visualization of these processes can be derived form Schematics of the circuit and its simulated waveforms (presented below). Note that Clock for ADC is function of both Enable and Clock. In this lab, Clock to ADC is named MCLK. Same Clock periods, MCLK is also given to SIPO as it does not need more to push out data. One key difference of the operation of ADC (provides Serial in for SIPO), and SIPO SR is that One same Clock period they work on different edges of the clock; ADC provides data on Falling edge of the clock while SIPO takes in on the Rising edge of the Clock. Therefore, as soon as the data is available at ADC output, immediate rising edge of next MCLK data is processed through SIPO.



State diagram for controller.

Present state variable	present state	INPUTS			Next state	outputs	
S_0/S_1	G_0	St	Int	SC	G_0^*	En	Csbar
?	?	X	0	X	X	X	X
S_0	0	X	1	X	0	0	1
S_0	0	0	X	X	0	0	1
S_0	0	1	X	X	1	0	1
S_1	1	X	X	0	1	1	0
S_1	1	X	X	1	0	1	0

① $G_0^* = \bar{G_0}\,St + G_0\,\bar{SC}$

② $En = G_0\,\bar{SC} + G_0\,SC$

③ $Csbar = \bar{G_0}\,Int + \bar{G_0}\,\bar{St} + \bar{G_0}\,St$

Figure 2: State Diagram and Table for Controller.

Since, it's a one variable state , only a single D- flip flop is required to cycle through the states.

For convenience of error free operation, all Verilog models and Schematics from HDL was verified in Simulation mode. Following presents those results

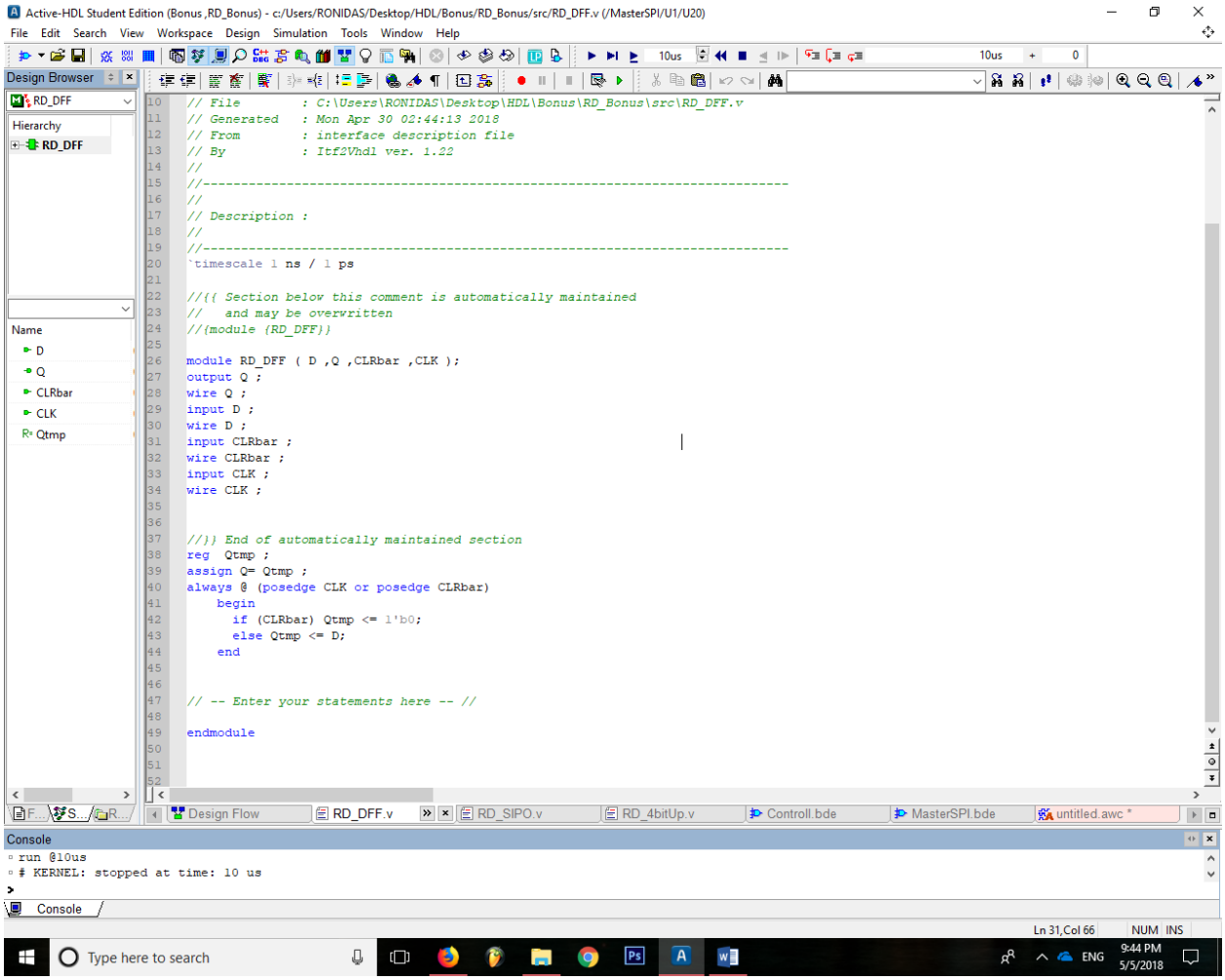


Figure 3: Verilog model for D-Flip Flop.

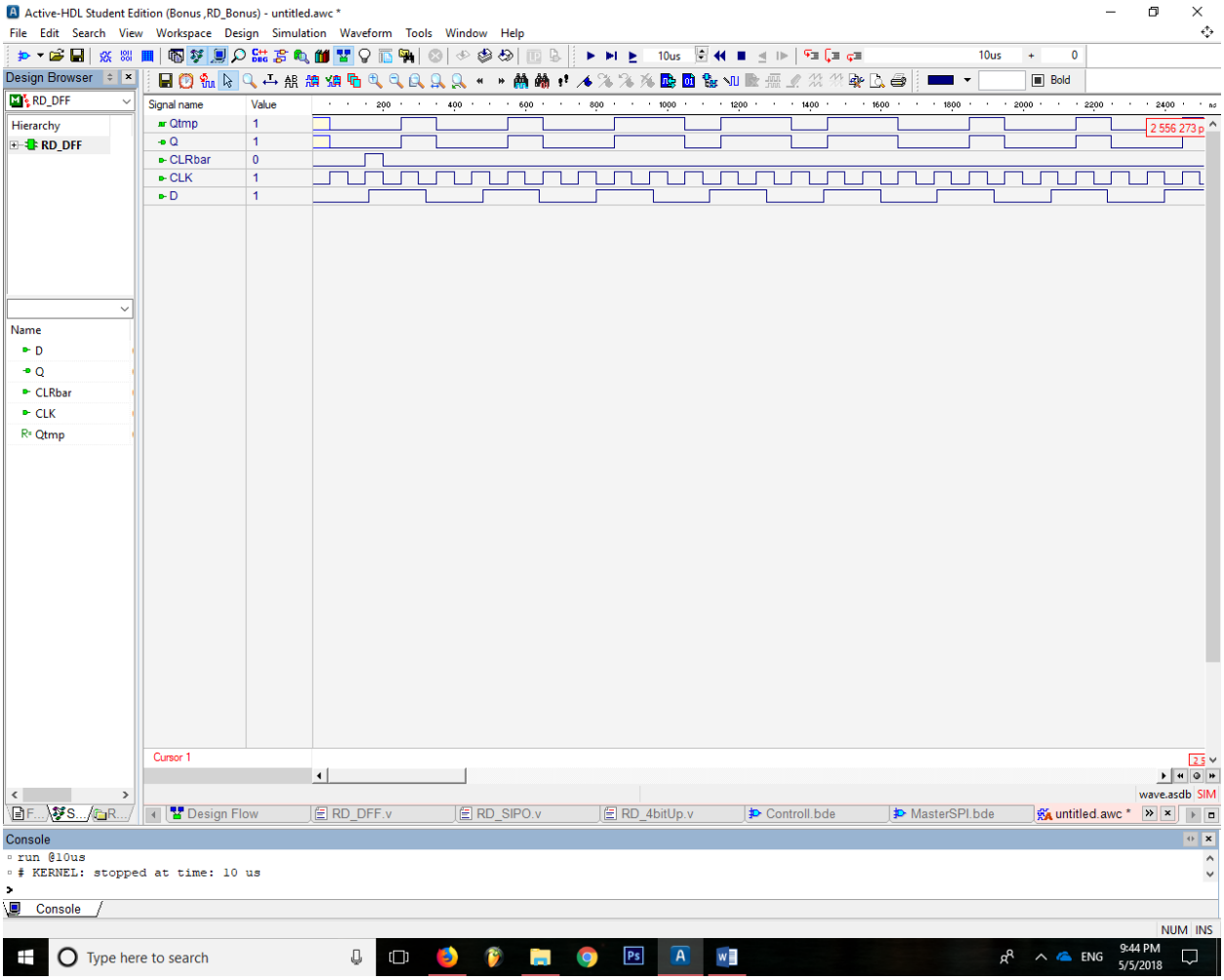


Figure 4: Operation of D-Flip Flop Verified.

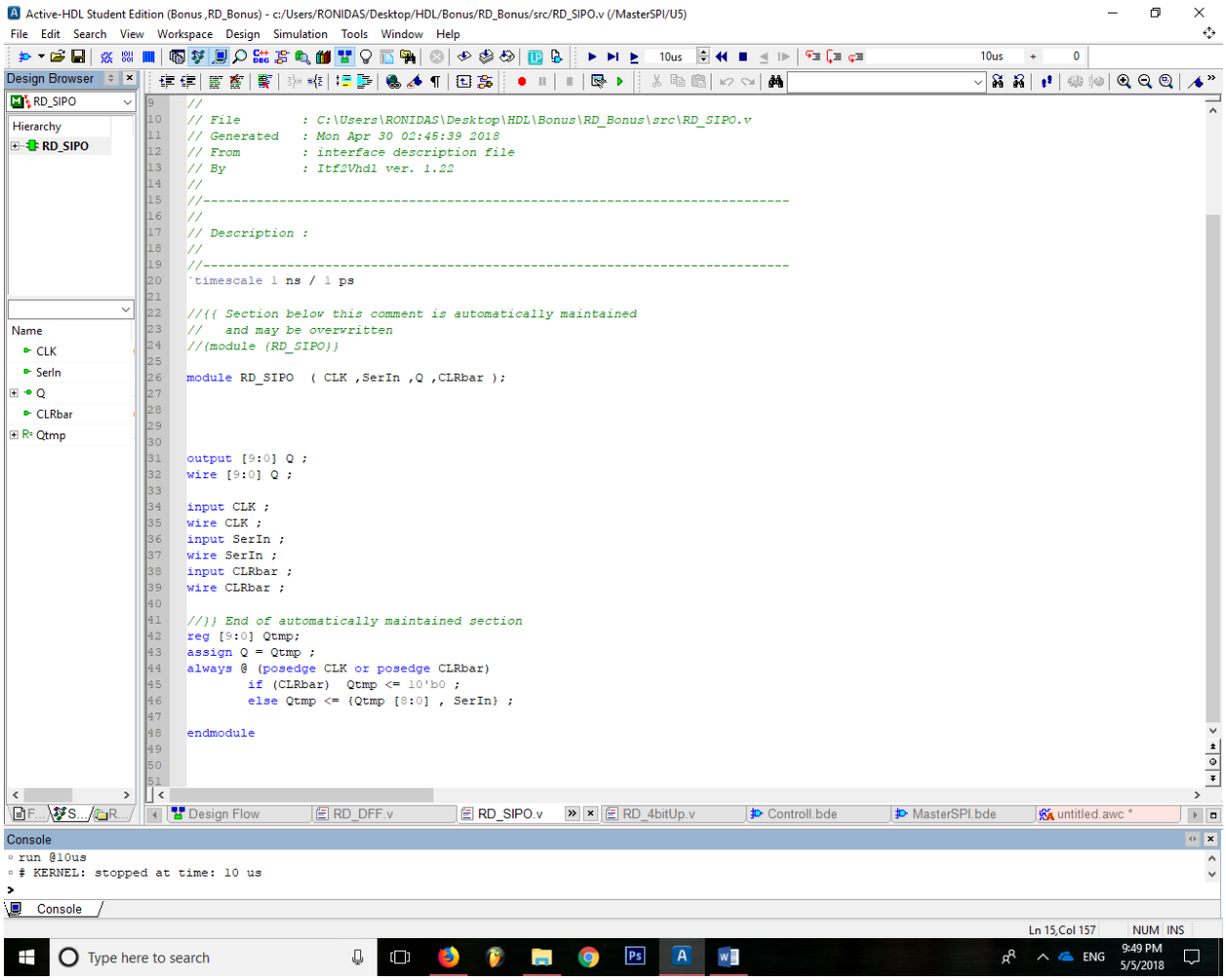


Figure 5: Verilog model for Serial in Parallel Out Shift Register.

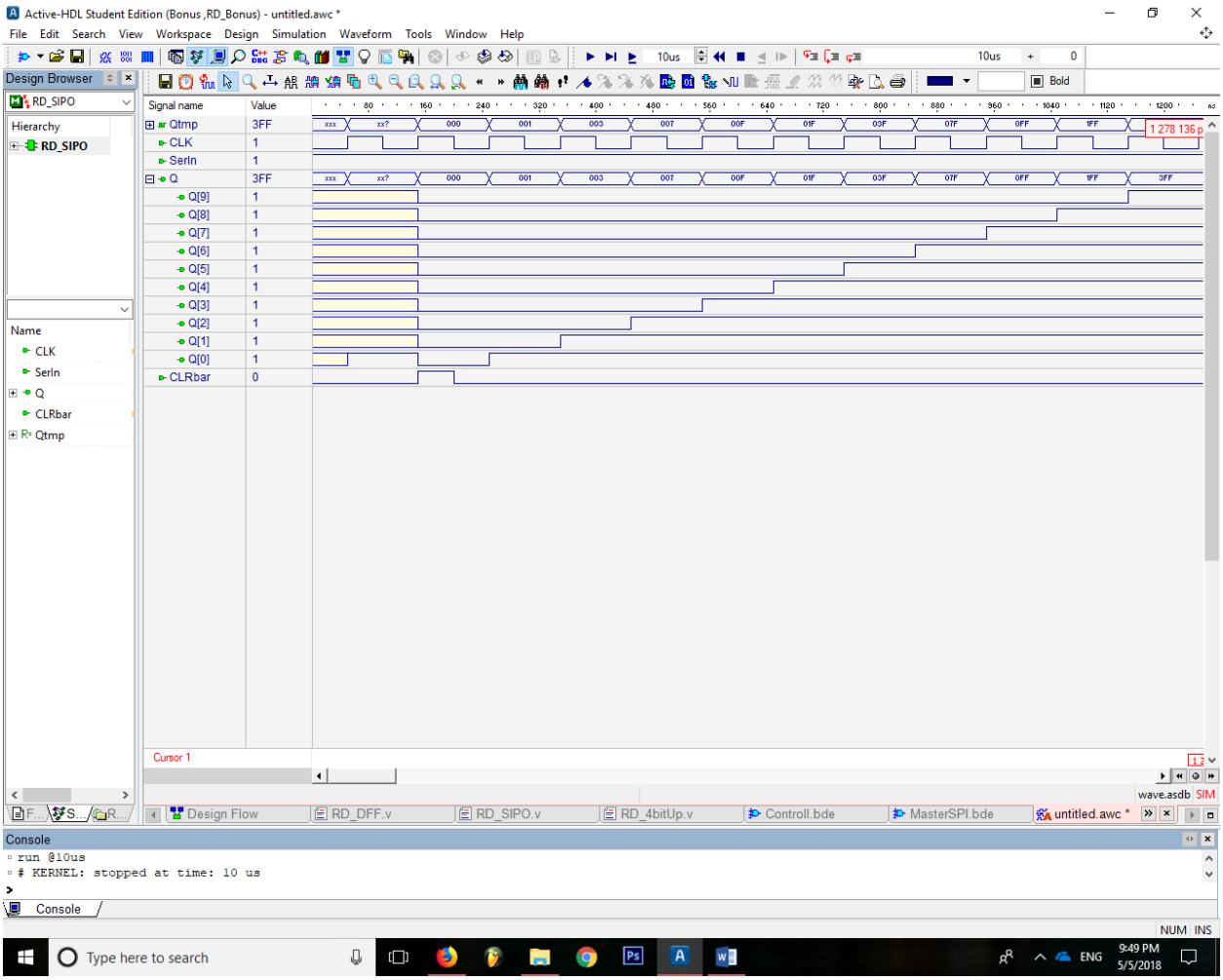


Figure 6 : Operation of SIPO SR verified.

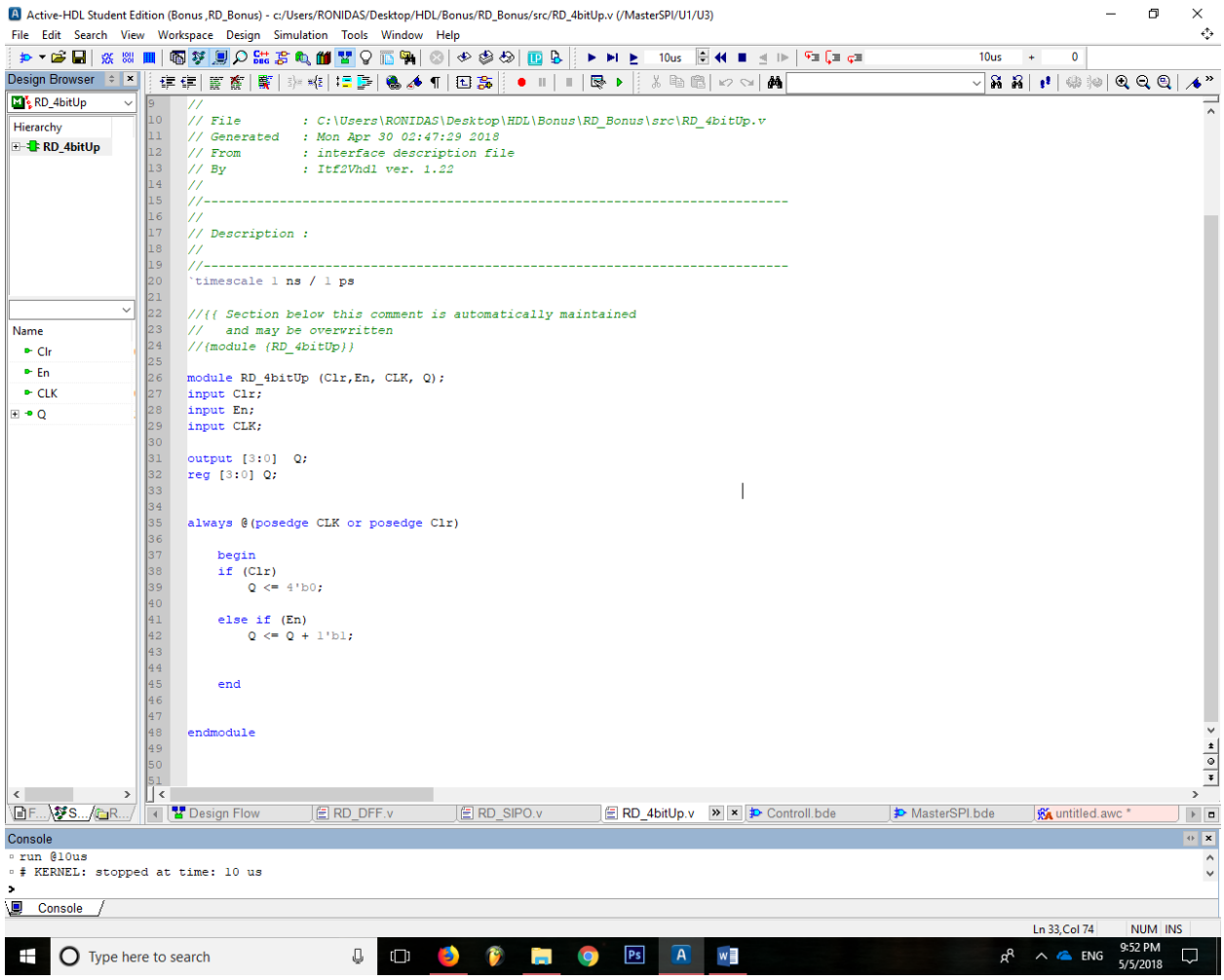


Figure 7: Verilog model for 4-bit Up Counter.

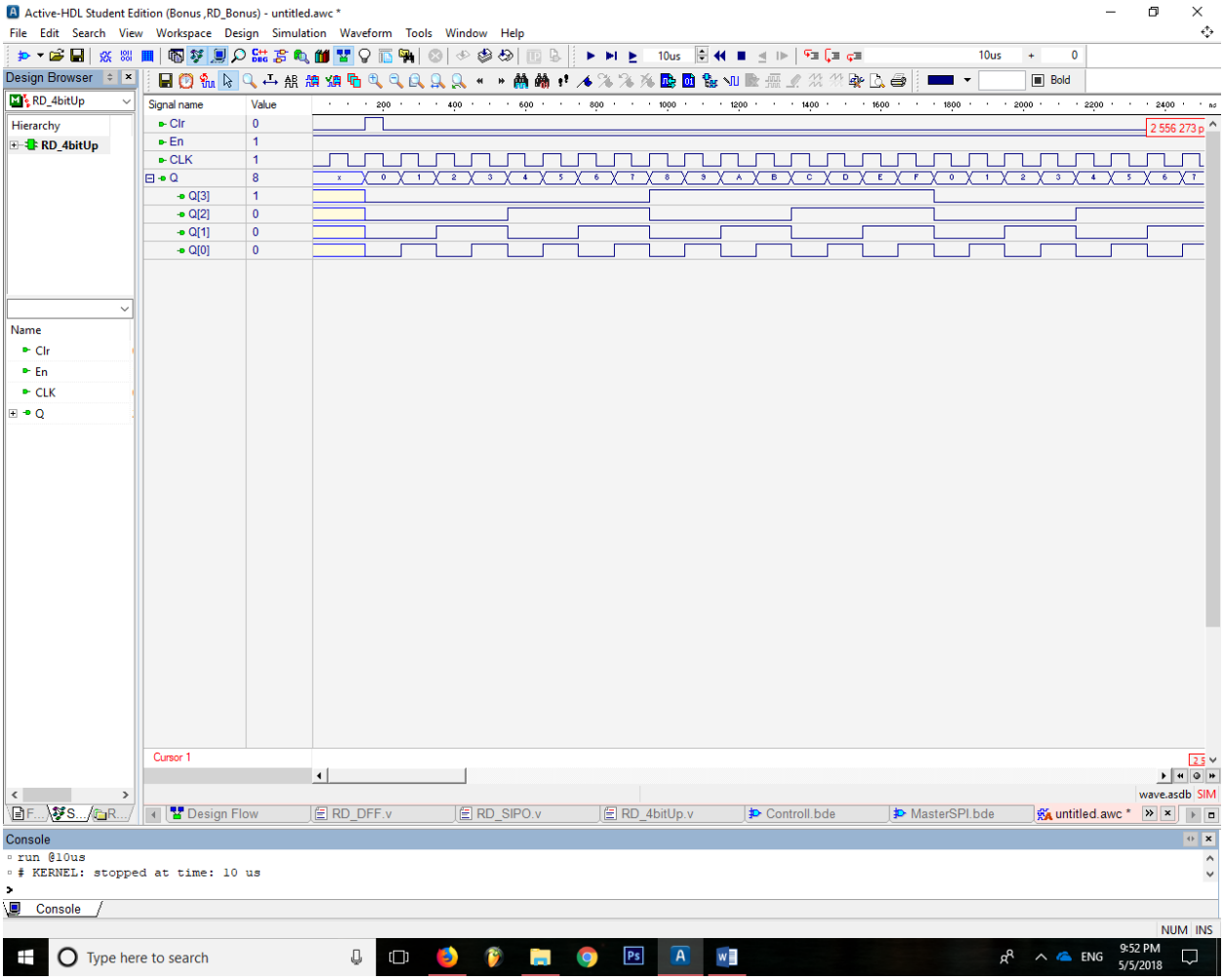


Figure 8 : Operation of 4-bit Up Counter verified using simulation.

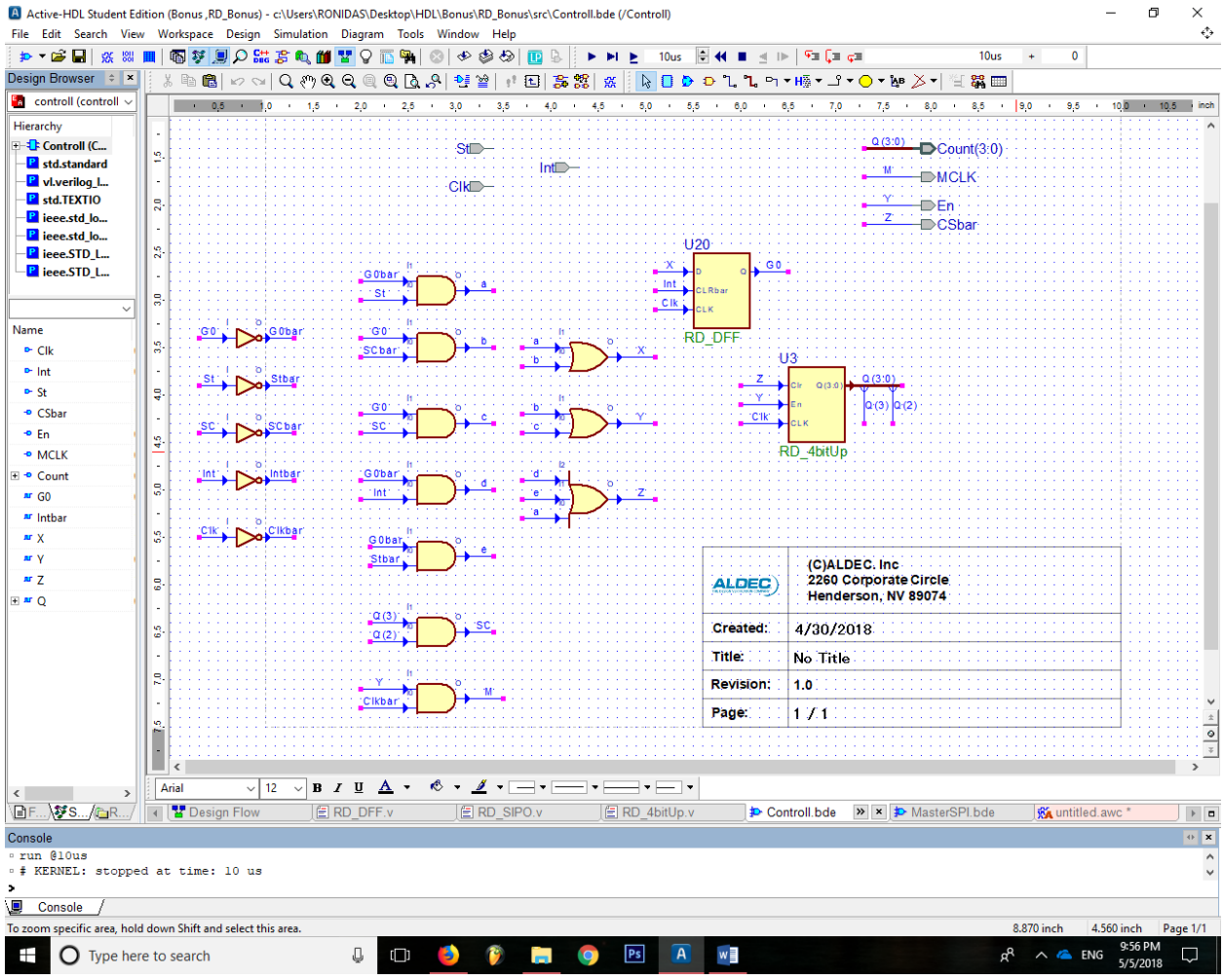


Figure 9 : Schematic for Control Logic.

With the help of the counter, Controller counts 13 Clock periods and repeats as long as Start = 1; En and Csbar are decode from given state. Controller was converted into a single unit for future uses.

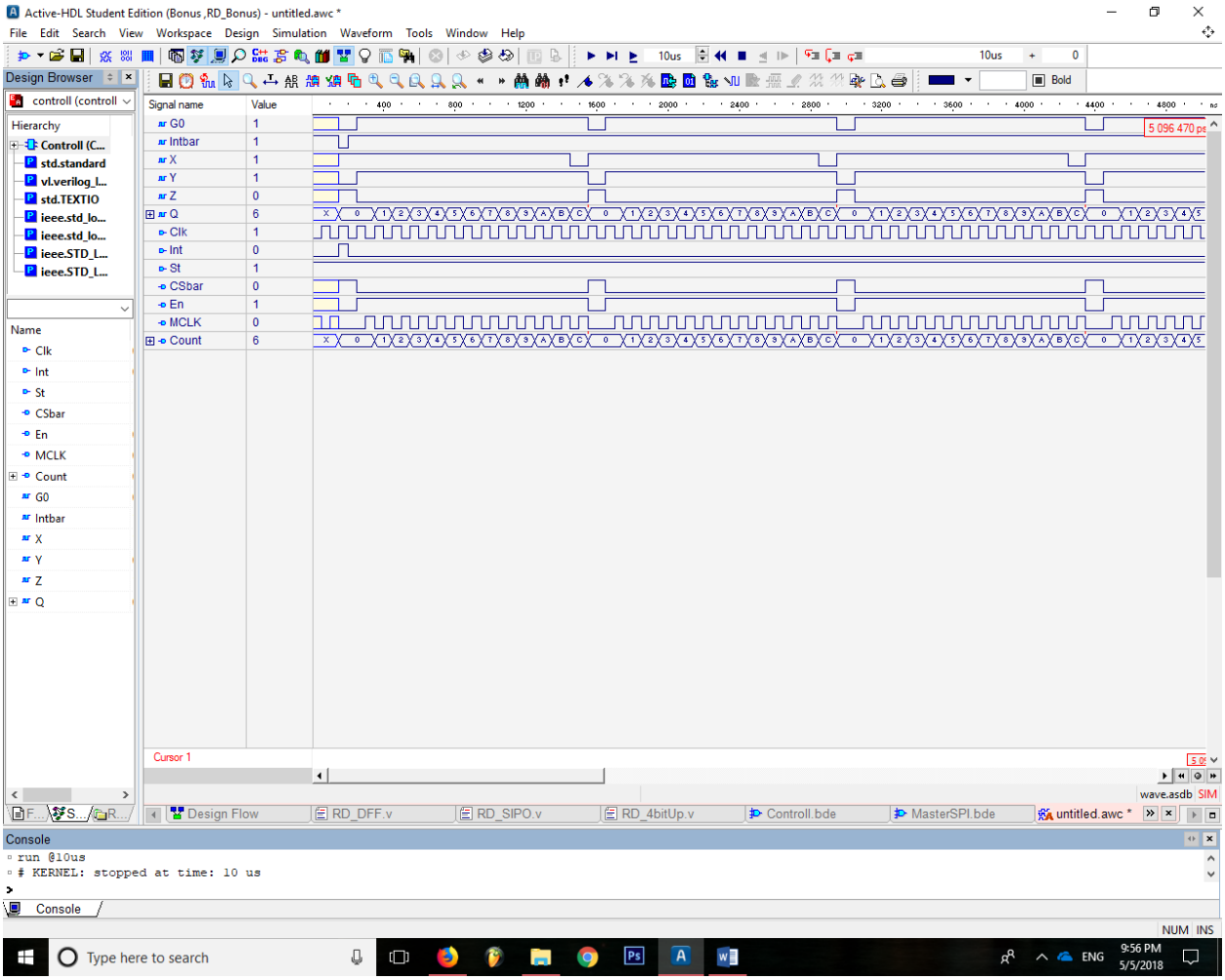


Figure 10 : Operation of Controller and Counter verified from simulation.

From waveforms above, we can denote that MCLK = 13 clock periods. On the last falling edge of MCLK CSbar changes to 1 ; Waveforms of CSbar and MCLK was compared against MCP3001 datasheet and verified.

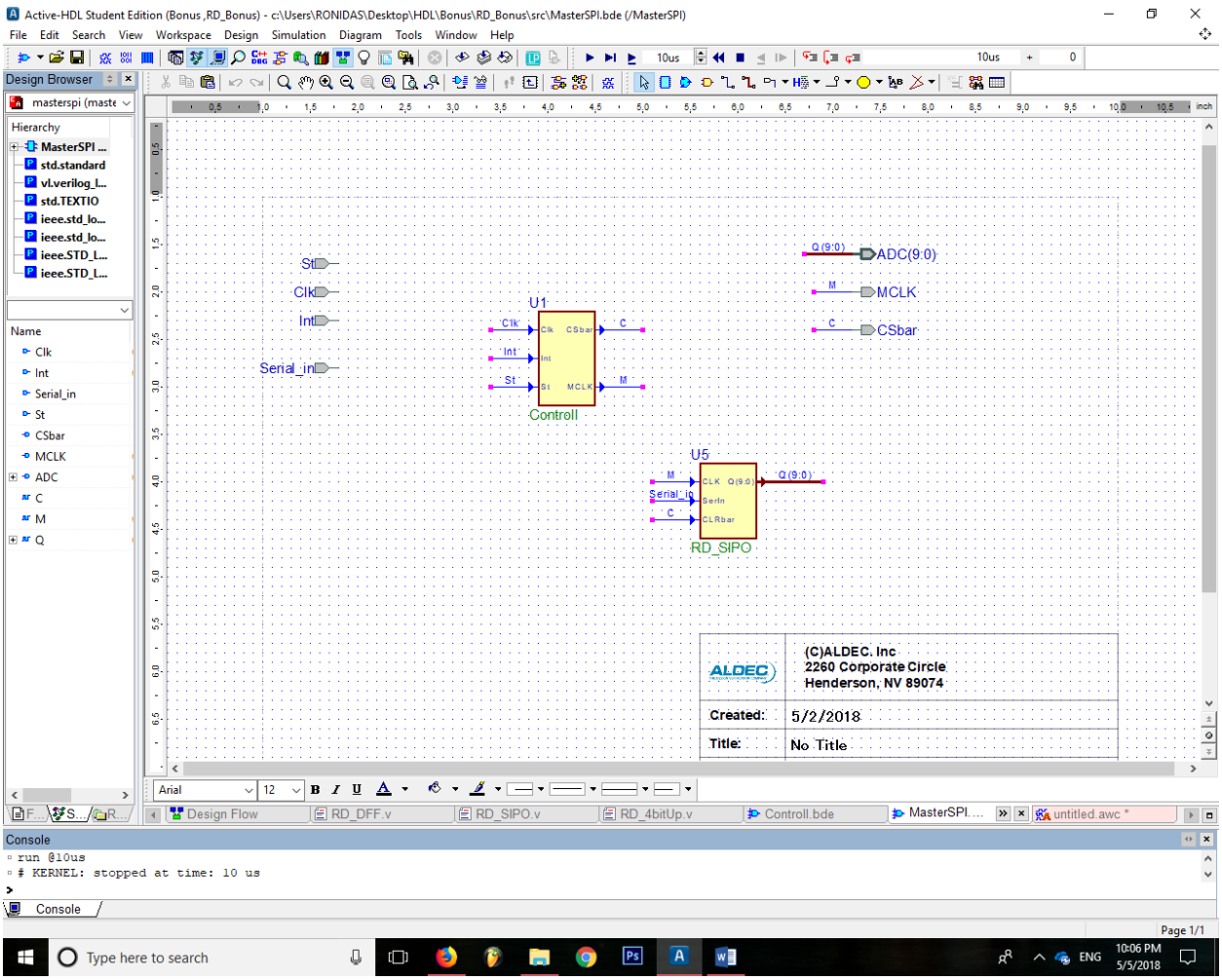


Figure 11 : Schematic for Master SPI for communication with 10-bit ADC.

4-bit up Counter is situated inside the unit “Controll” (described in Figure 9). SIPO takes in data from ADC output and show us the results in parallel . For simulation purposes Serial_in was set to 1.

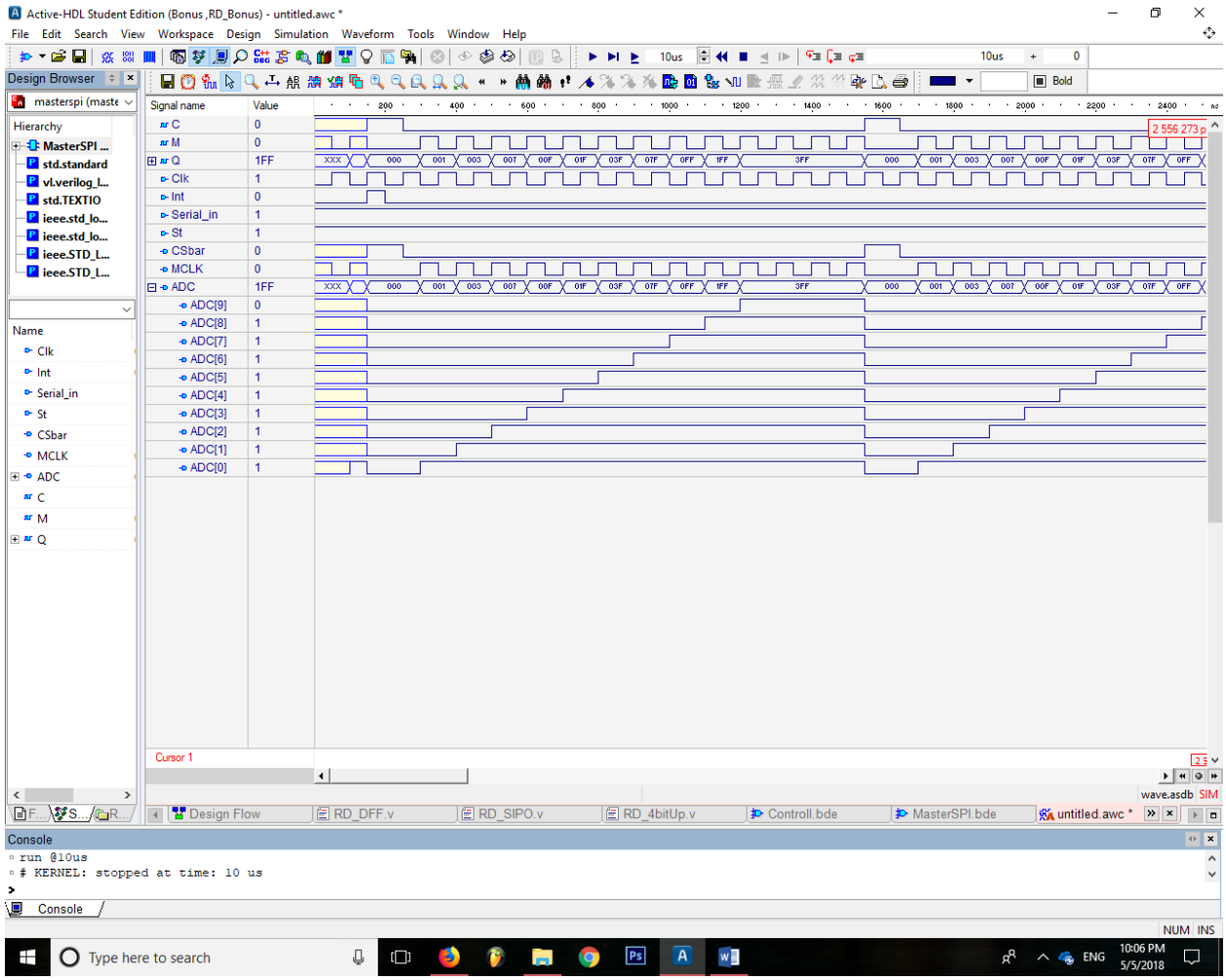


Figure 12 : Waveforms for Master SPI.

As shown above, all the requirements for communication with ADC MCP3001 is met. The Verilog models and code generated from schematic was processed through IceCube2 for purpose of Bitmap generation. Using the help of Diamond Programmer, FPGA was programmed with Master SPI to communicated with 10-bit ADC MCP3001. Pin layouts on FPGA are shown below. Clock was accessed from pin 21 of FPGA device.

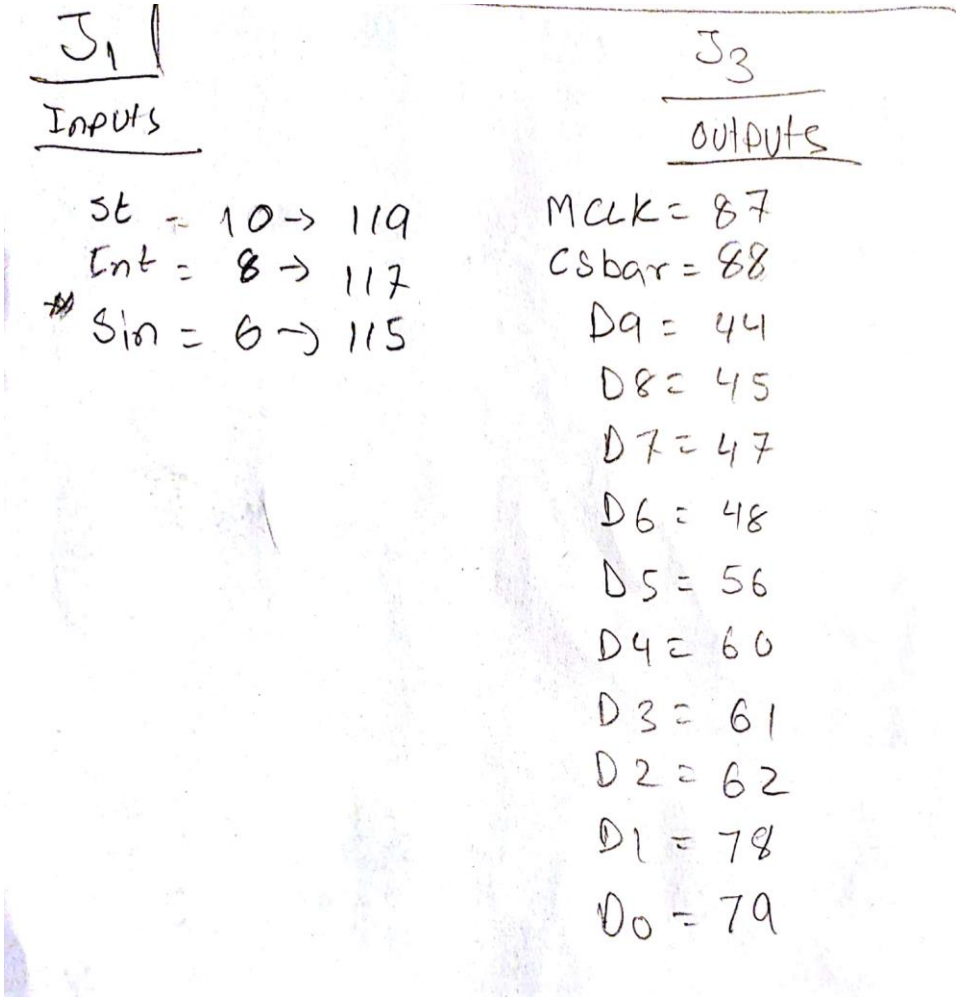


Figure 13: Pin layouts selected using IceCube2.

Clock was accessed from pin 21 of FPGA device. Therefore, no external clock was applied to the system .

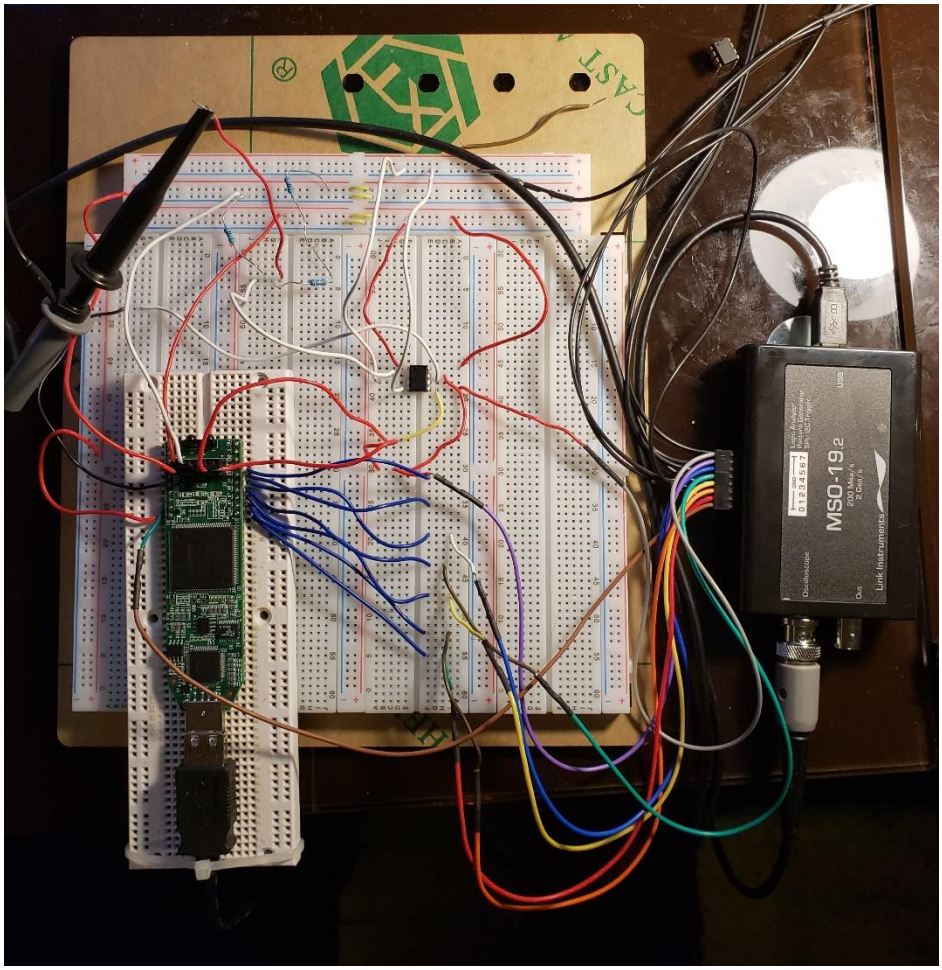
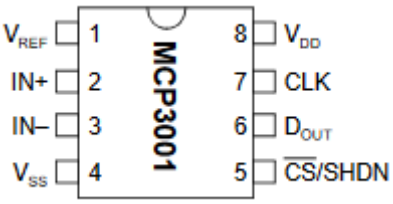


Figure 14 : Experimental set-up for the System.



Once again, datasheet of MCP3001 was used as reference and pins were connected appropriately. Due to limited availability of logical probes from MSO-19, Bit : D9 – D5 was captured on the screen (5 MSB). Last two probes were used to monito CSbar and Clock applied to ADC. Probe 1 from MSO-19 provided Initiation for the circuit. ADC was powered and grounded from FPGA unit. Data and Results follows below.

Data and results:

Vref = 3.3 V
IN+ = 3.3 V
IN- = GND

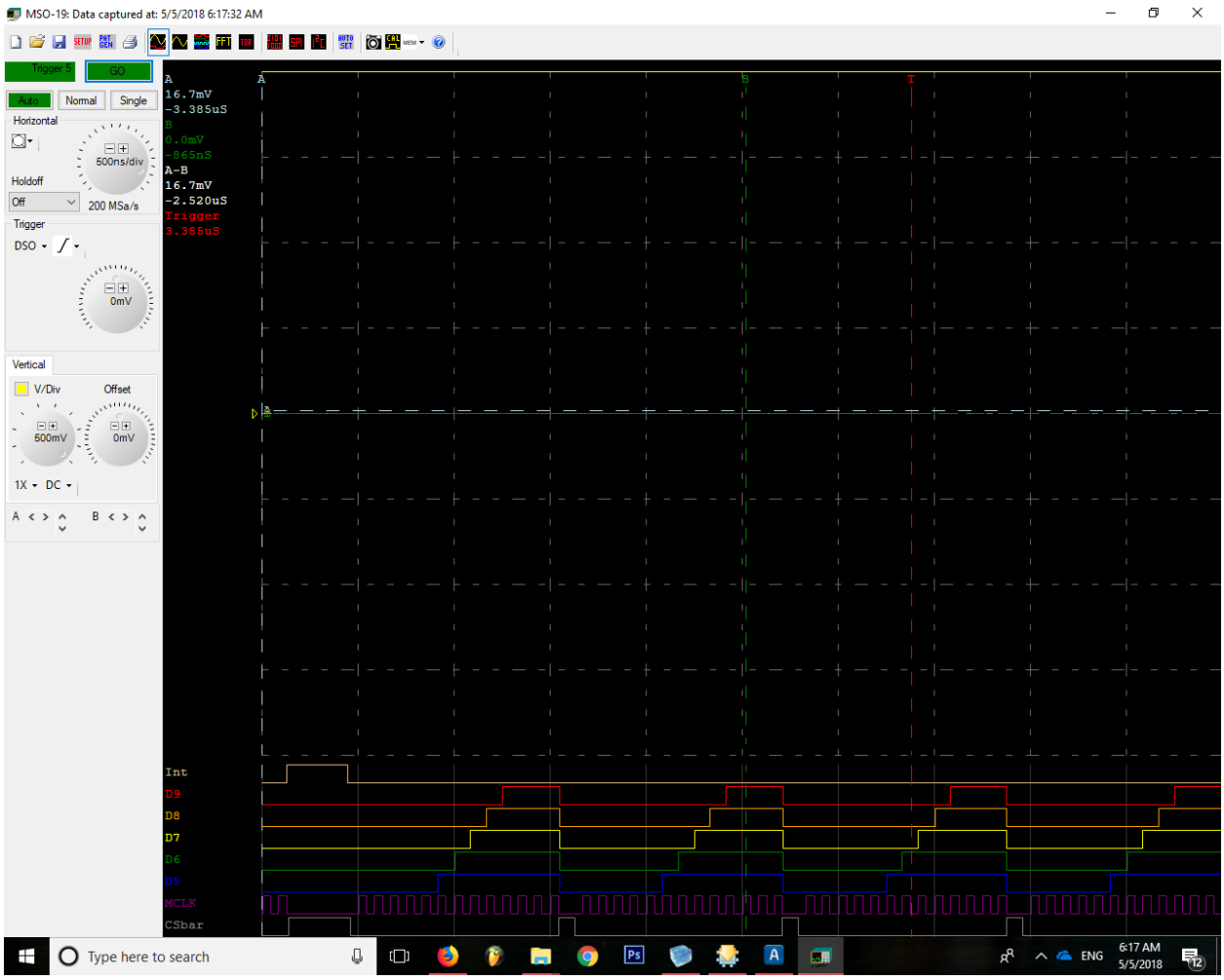


Figure 15: Waveforms obtained ADC for Vref = 3.3 V and Vin = 3.3 (approx.)

With 10-bit resolution ADC, max voltage converts to decimal value = 1024; +/- 1 LSB in each tier of DC value. Using, we can calucated expected Digital output of when Vin = 3.3 V.

$$Digital\ Output\ Code\ = \frac{1024 * V_{IN}}{V_{REF}}$$

$$\text{Digital Output Code} = \frac{1024 * 3.3V}{3.3V} = 1024$$

Above results D9-D5 = 1 on last clock periods just before CSbar = 1 ; correspond decimal 1023 if we consider +1 LSB for D9 output.

Vref = 3.3 V
IN+ = 1.61 V
IN- = GND

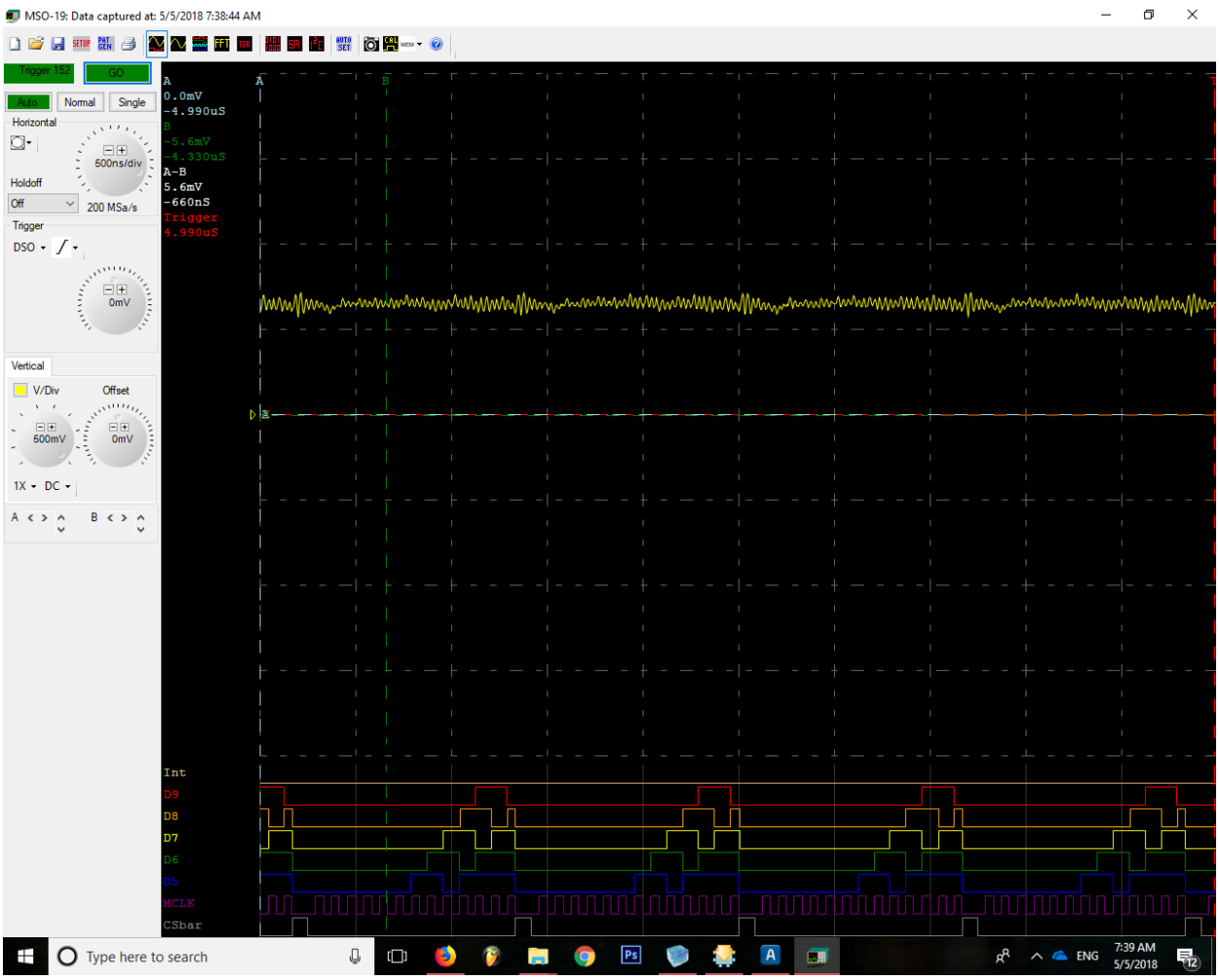


Figure 16 : Output waveforms for ADC for Vref= 3.3 V ; Vin= 1.61 V. (MSB : D9-D5 shown)

Using Voltage division, by using two resistors of 10K each, an intermediate voltage was obtained at IN+ node of MCP3001. IN- node(pin 3) of ADC was ground for an accurate conversion. Noise from IN- subtracts from IN+ to provide Vin. However, we can approximate conversion using.

$$Digital\ Output\ Code\ = \frac{1024 * V_{IN}}{V_{REF}}$$

Digital Output Code = $\frac{1024 * 1.61V}{3.3V}$ = 499 ; Bin = 0111110011 ;

Vref = 3.3 V
IN+ = GND
IN- = GND

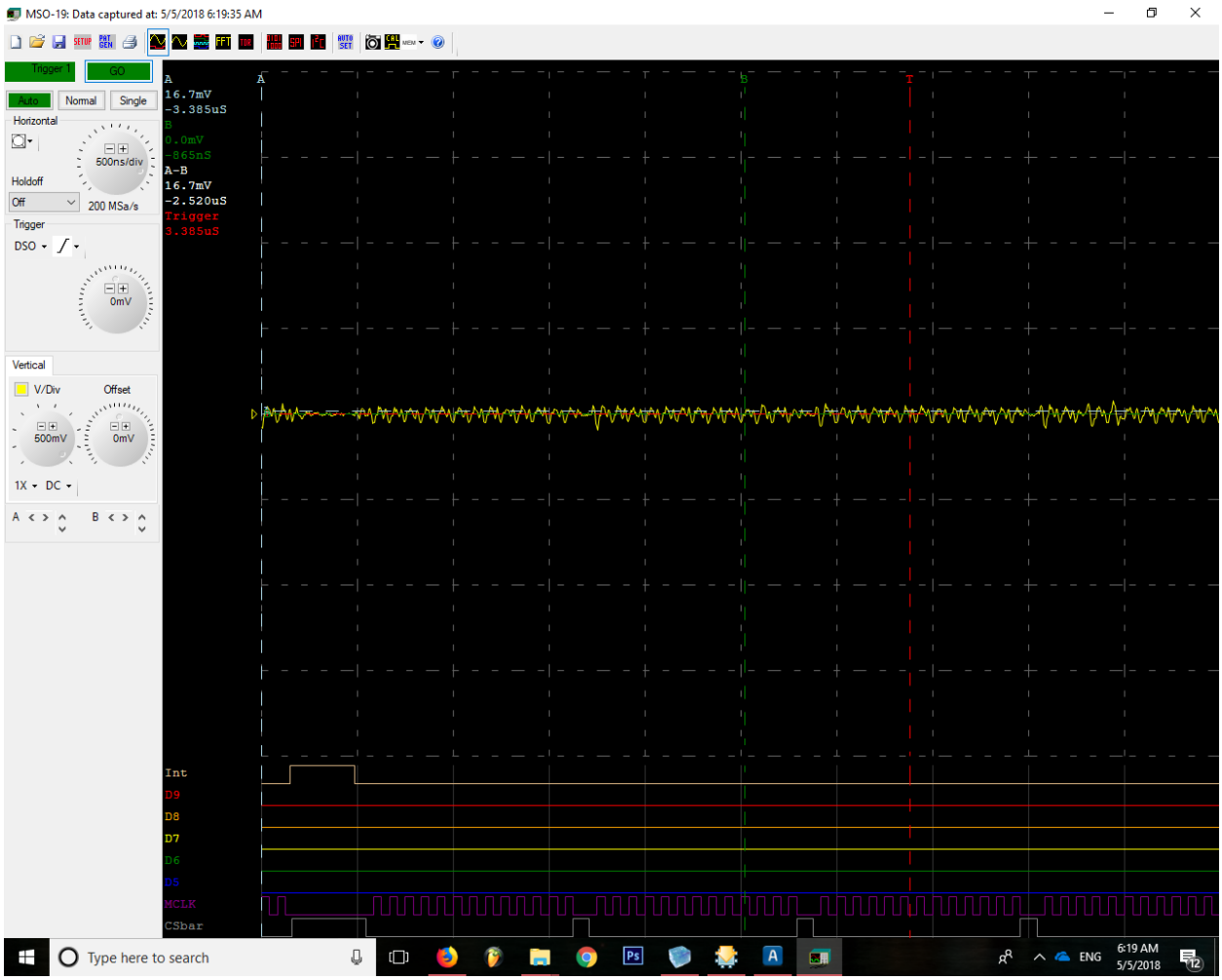


Figure 17 : Output waveforms for ADC for Vref= 3.3 V ; Vin= 0V(approx.).(MSB : D9-D5 shown)

$$\text{Digital Output Code} = \frac{1024 * 0V}{3.3V} = 0$$

As expected differential voltage between IN+ and IN- is very close to 0. Therefore, Digital output code for Analog value of 0 V is 0 (from D9-D0).

Conclusion : Design the Master controller based on IceStick FPGA with SPI-compatible protocol for communication with 10-bit ADC MCP3001 was carried out in this laboratory experiment. Using the knowledge of HDL an FPGA was programmed to carry out all operations to reach objective successfully. ADC paves a meaningful way for processing information in today's digital realm.