Quartus+ModelSim-Altera 联合仿真（Verilog 版）

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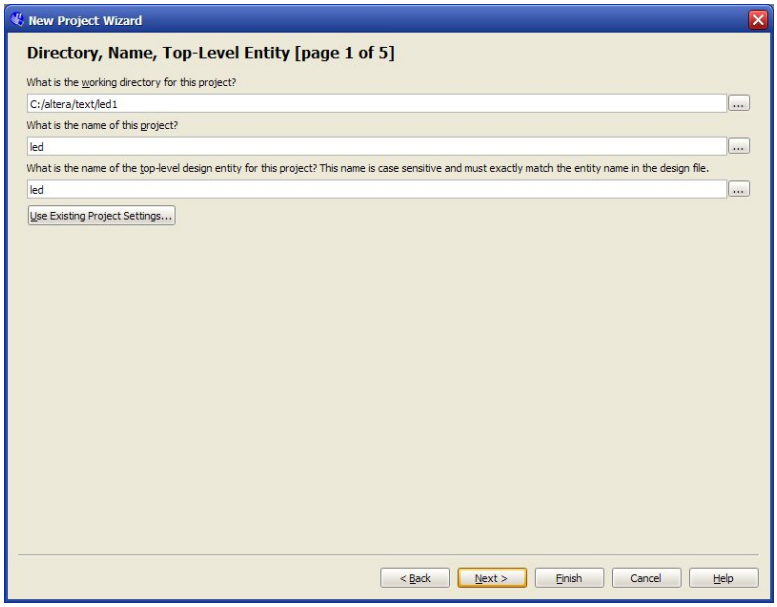
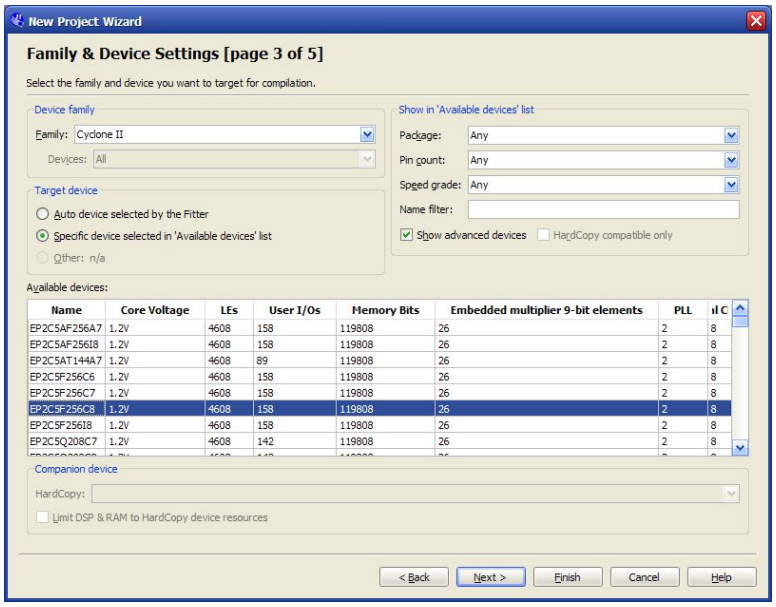
（注：默认 Next/OK/Finish）

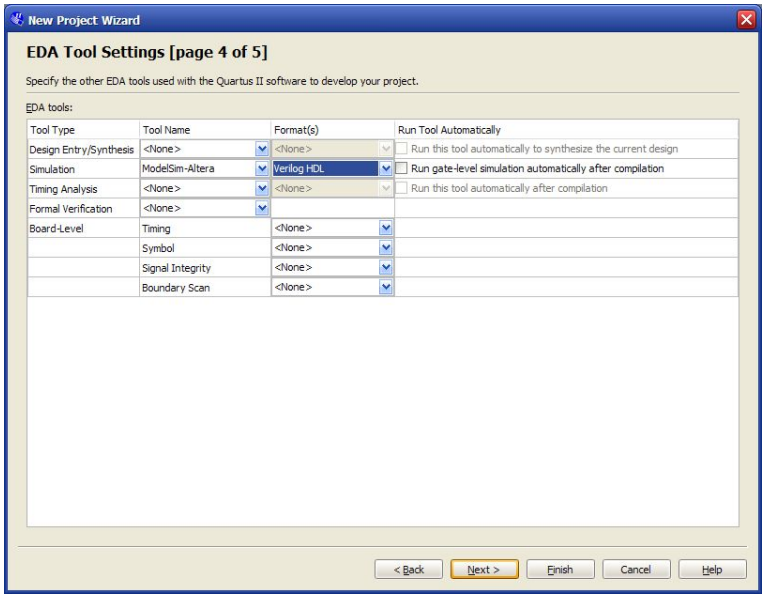
Step1：新建工程 New Project Wizard...设置路径+工程名+entity 名（project、entity 必须同名）；



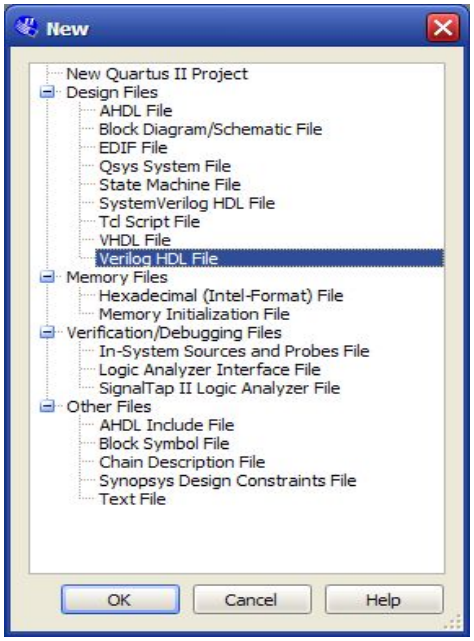
Step2：选择器件：Cyclone II　EP2C5F26C8（例如）；



Step3：Simulation 设置：ModelSim-Altera + Verilog HDL；



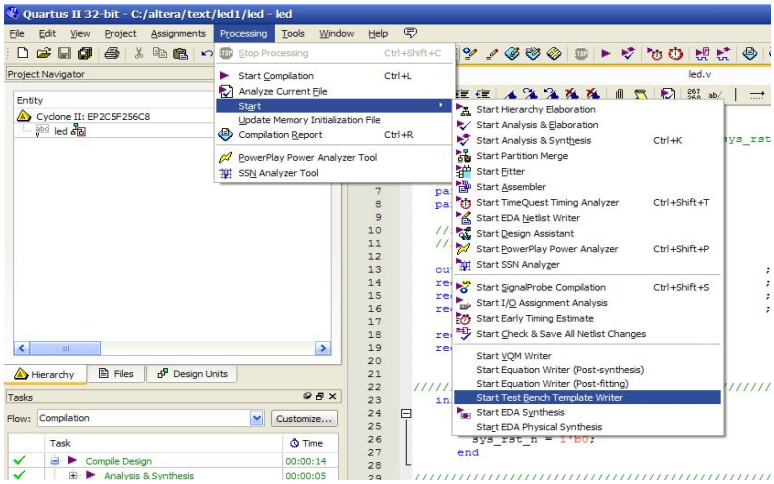
Step4：新建文件，选 Verilog HDL File；



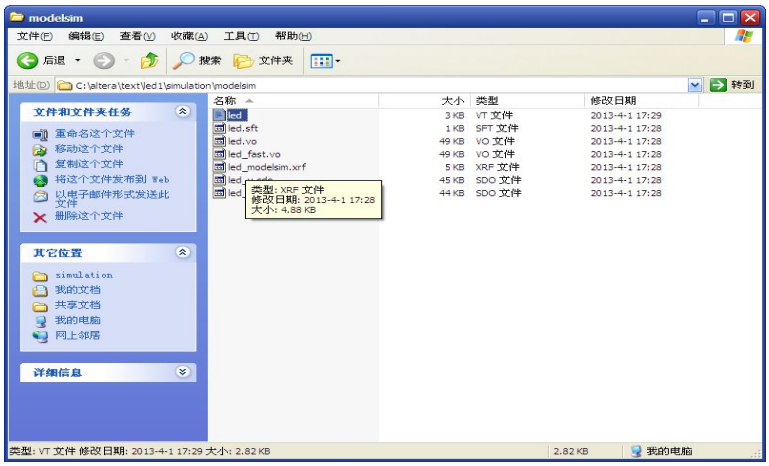
Step5：输入代码，并保存为 led（.v 文件）；

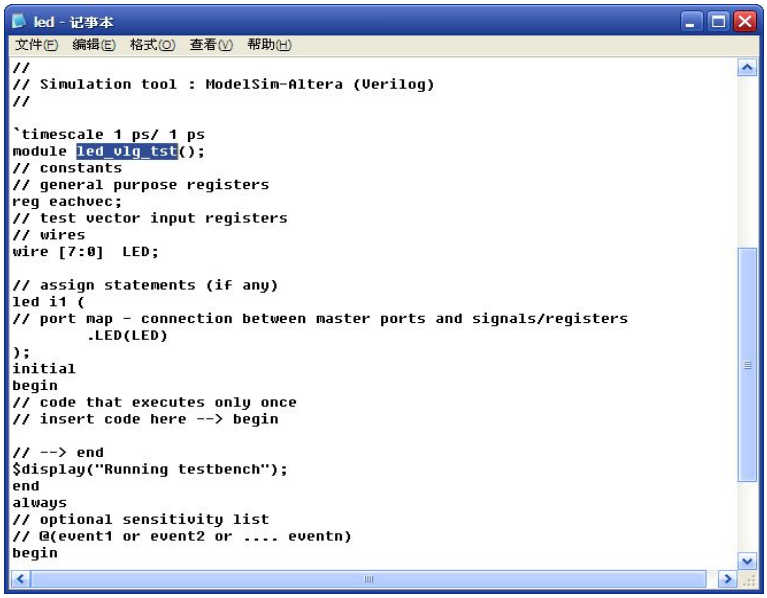
Step6：调试，修改直到没有 Error 为止（工程目录下同时自动生成了 simulation 文件）；

Step7：生成 Test Bench 文件（.vt）：Processing -> Start -> Start Test Bench Template Writer；

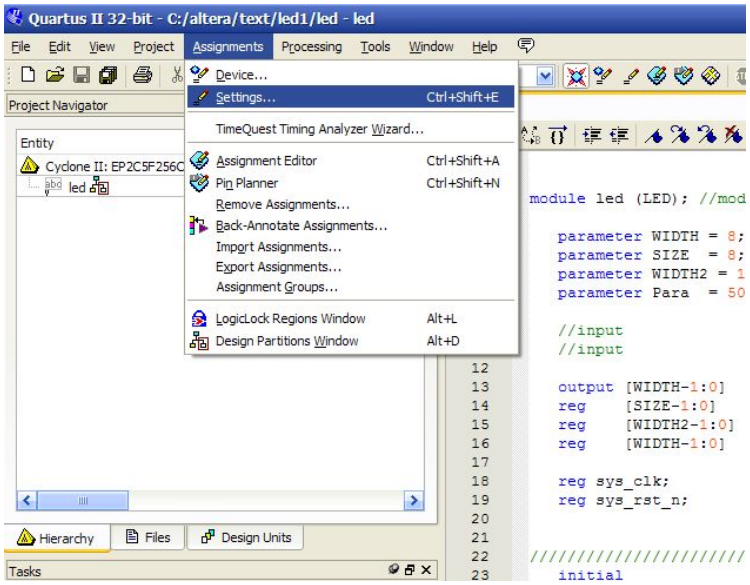


Step8：工程目录下 C:\altera\text\led1\simulation\modelsim 打开 led.vt 文件，并复制“led_vlg_tst”；

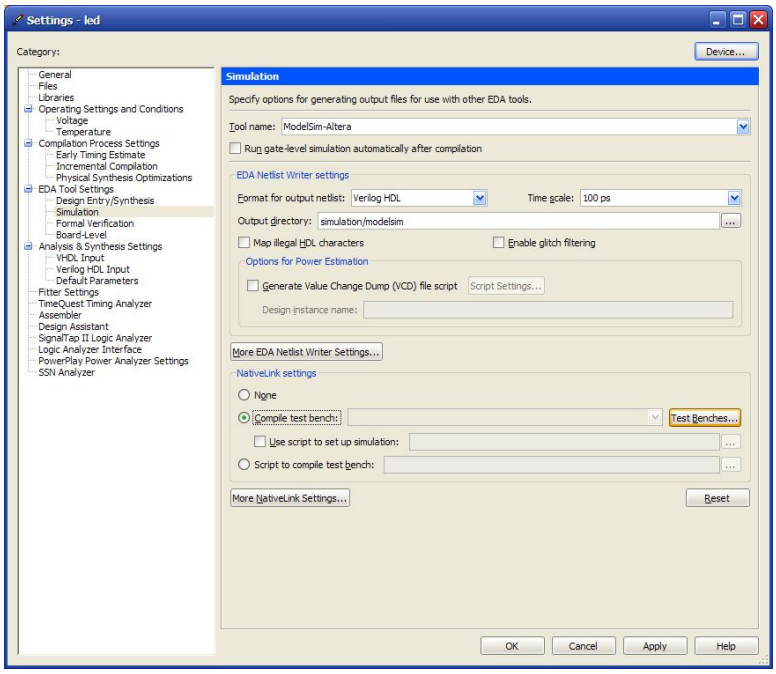




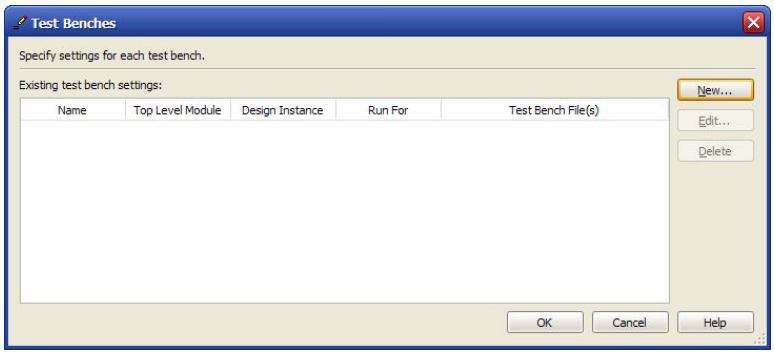
Step9：设置 Simulation：Assignments+Settings；



Step10：Simulation -> 仿真扫描时间 Time scale:100ps（或其它值），Comple test bench -> Tset Benchse...；

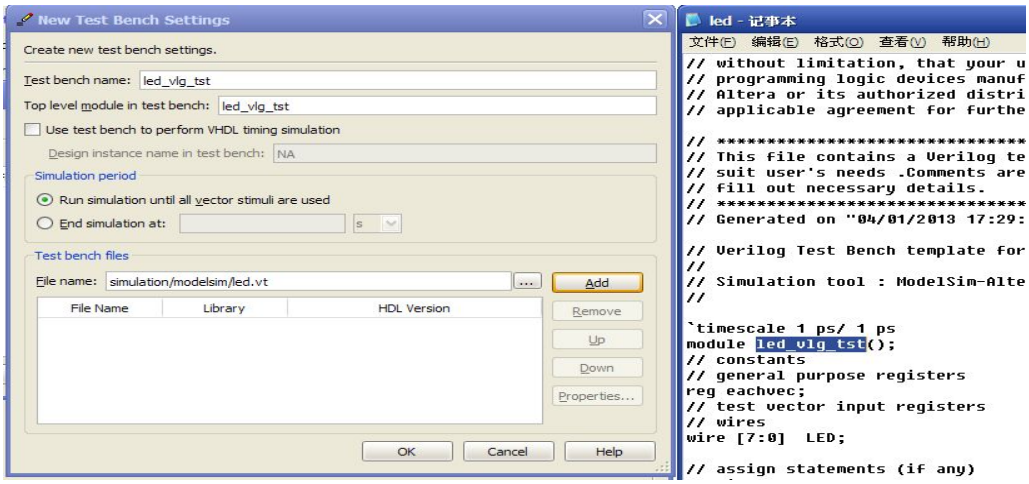


Step11：点击 New...；

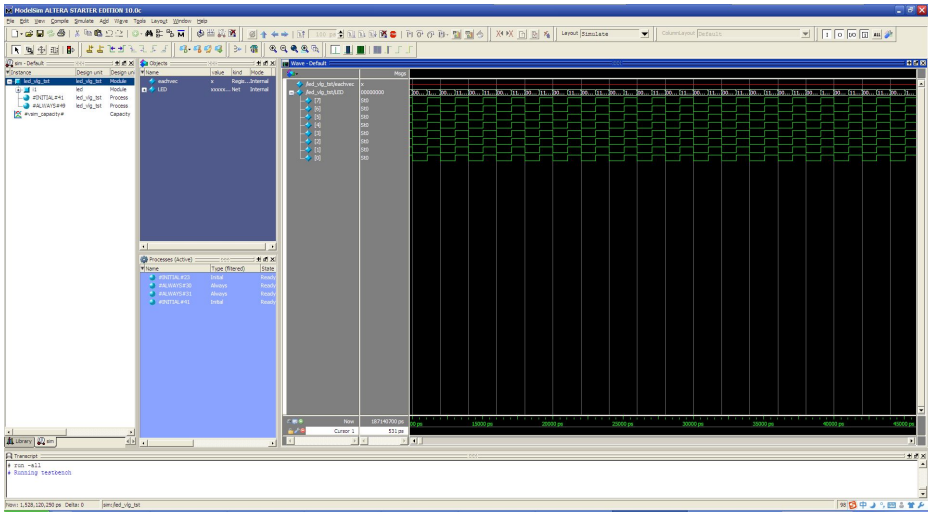


Step12：粘贴 Test bench name：led_vlg_tst（Step8 中已复制），Top level module in test bench：led_vlg_tst（必须和.vt 文件里的 module 名一致）；

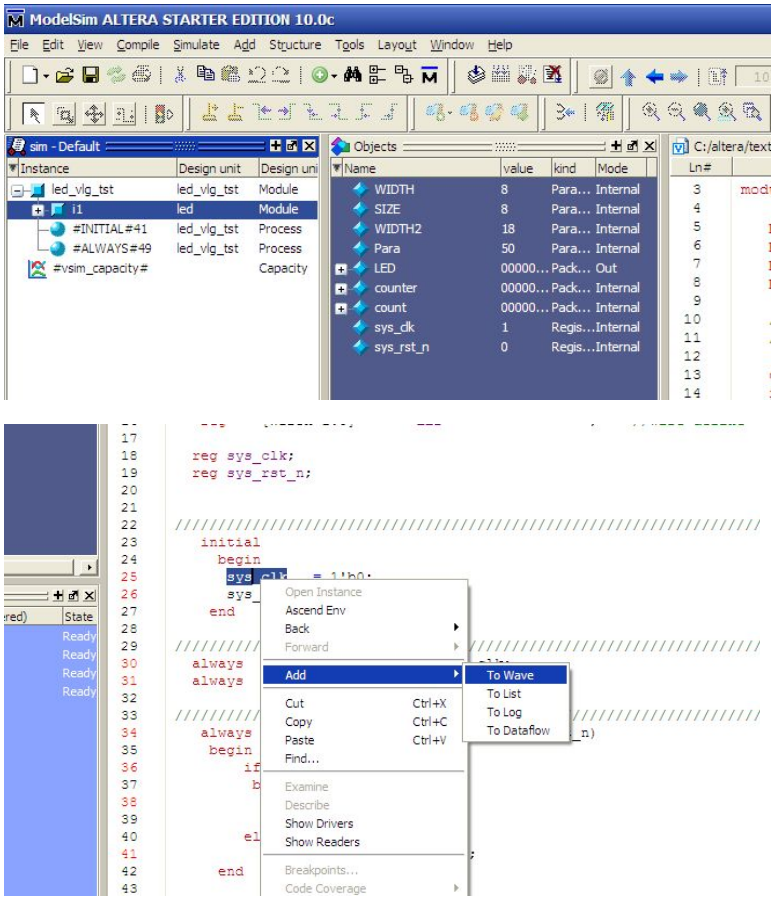
Step13：添加 Test bench files：simulation/modelsim/led.vt，并点击 Add；



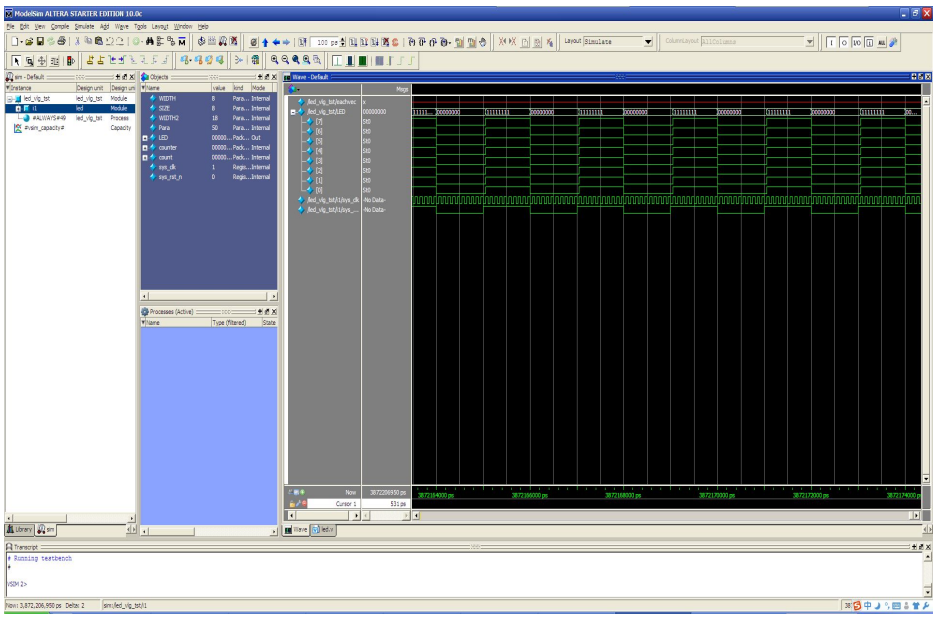
Step14：点击  ，即启动 ModelSim 进入仿真；



Step14：工作区中双击打开 i1 文件，并将所需要的信号添加到仿真波形图中：Add -> To Wave；



Step15：点击  ，便可看到完整的波形图了。完成仿真。



——2013.04.02 杭州