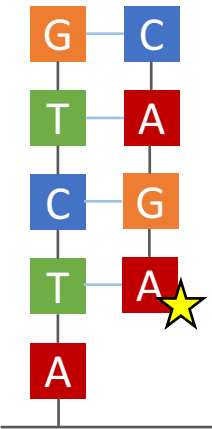
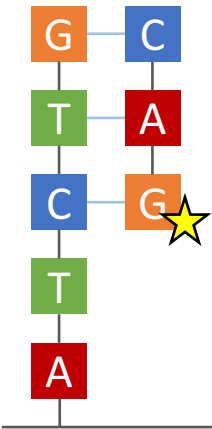
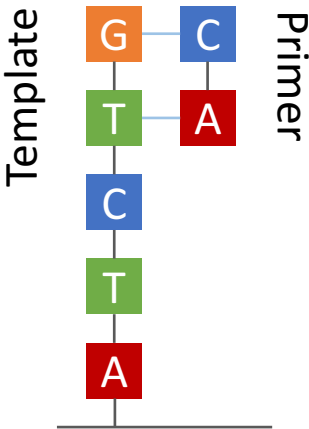


Cycle 0

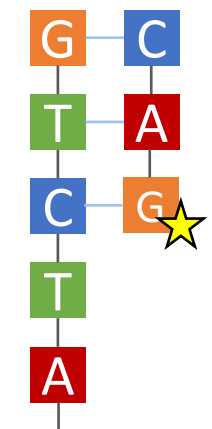
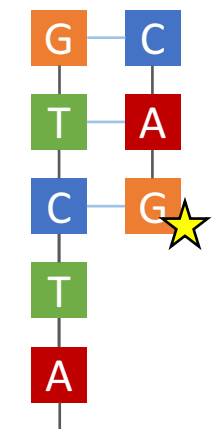
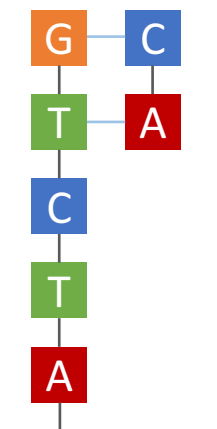
Cycle 1

Cycle 2

Normal

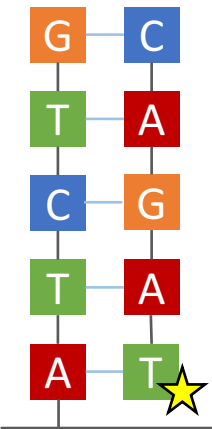
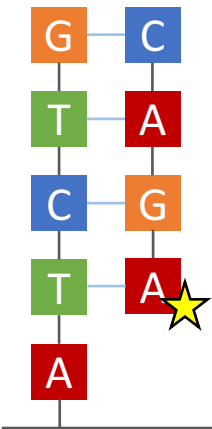
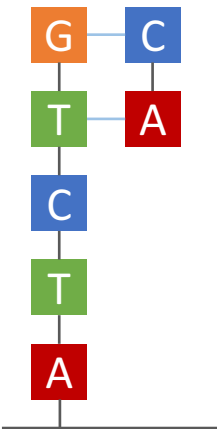


Lagging



Reverse termination fails

Leading



dGTP instead of ddGTP