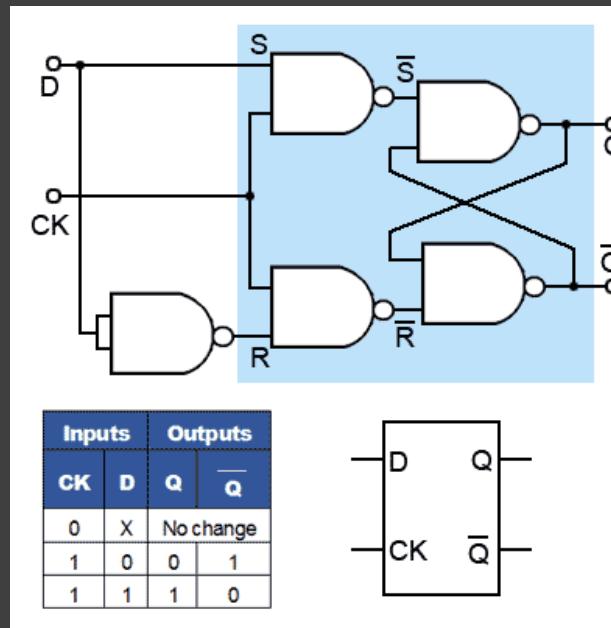


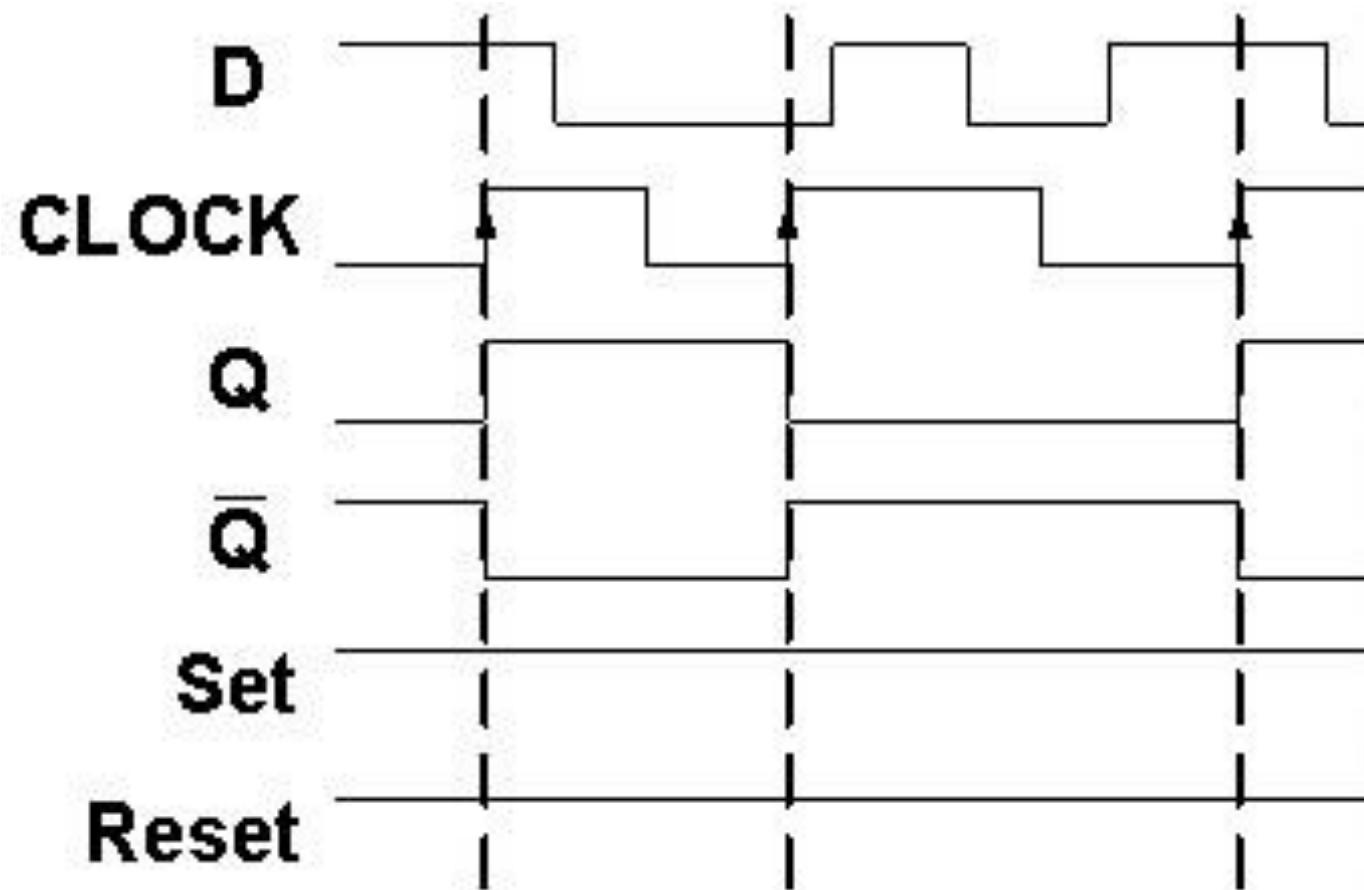
Design of low power and high  
speed Cmos D Flip flop using  
Self Voltage Level(SVL)  
method

# D flip-flop

- In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset. However, this would be pointless since the output of the flip flop would always change on every pulse applied to this data input.
- The "CLOCK" or "ENABLE" input is used to avoid this for isolating the data input from the flip flop's latching circuitry. When the clock input is set to true, the D input condition is only copied to the output Q. This forms the basis of another sequential device referred to as **D Flip Flop**.



## Time diagram of d-flip flop



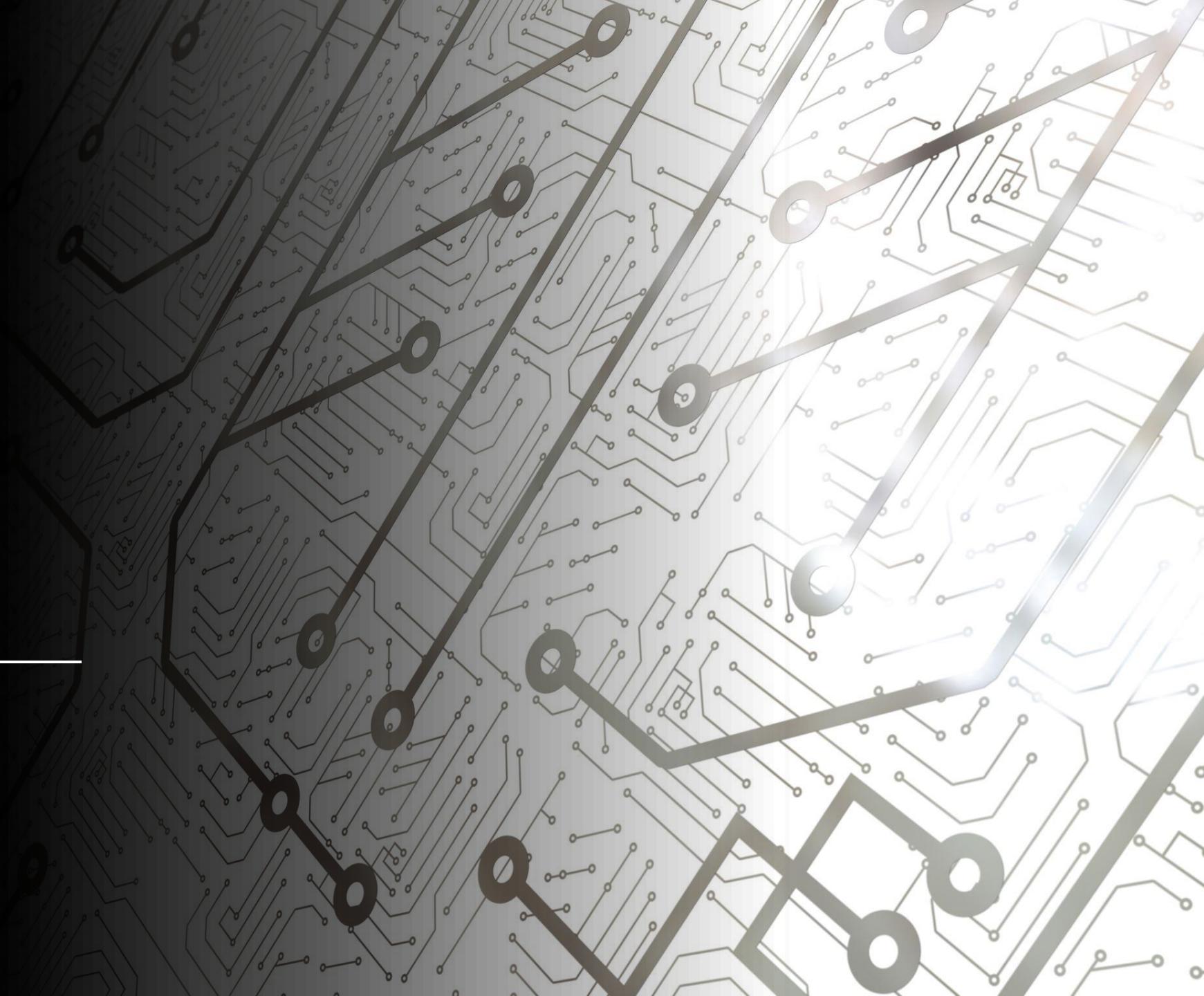
# SVL method



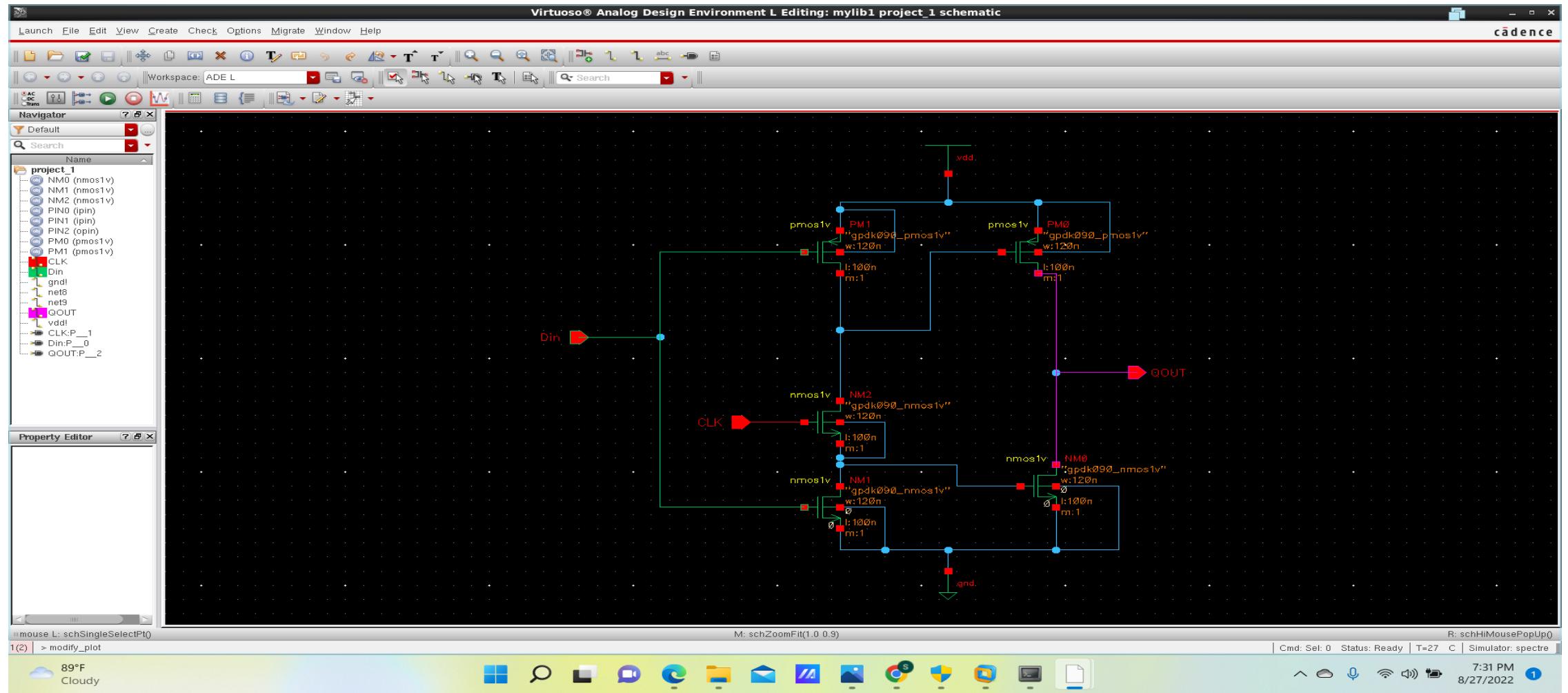
- SVL is the acronym for ‘Self-Voltage Level’.
- SVL technique is used to reduce leakage power in clocked systems like flip flops circuitry during a standby mode of operation i.e; when  $\text{clock}=0$ . SVL method utilizes PMOS and NMOS transistors in equivalent as pull up network or pull down system. Pull-up transistors gate is connected with the complement of clock signal and pull-down transistors gate terminal is connected with clock .
- This technique to reduce leakage power and delay time through voltage swing, uses a clock signal as the control signal to control supply voltage to D flip flop. Hence the name ‘Self-voltage level’ is justified.

# CIRCUIT-1

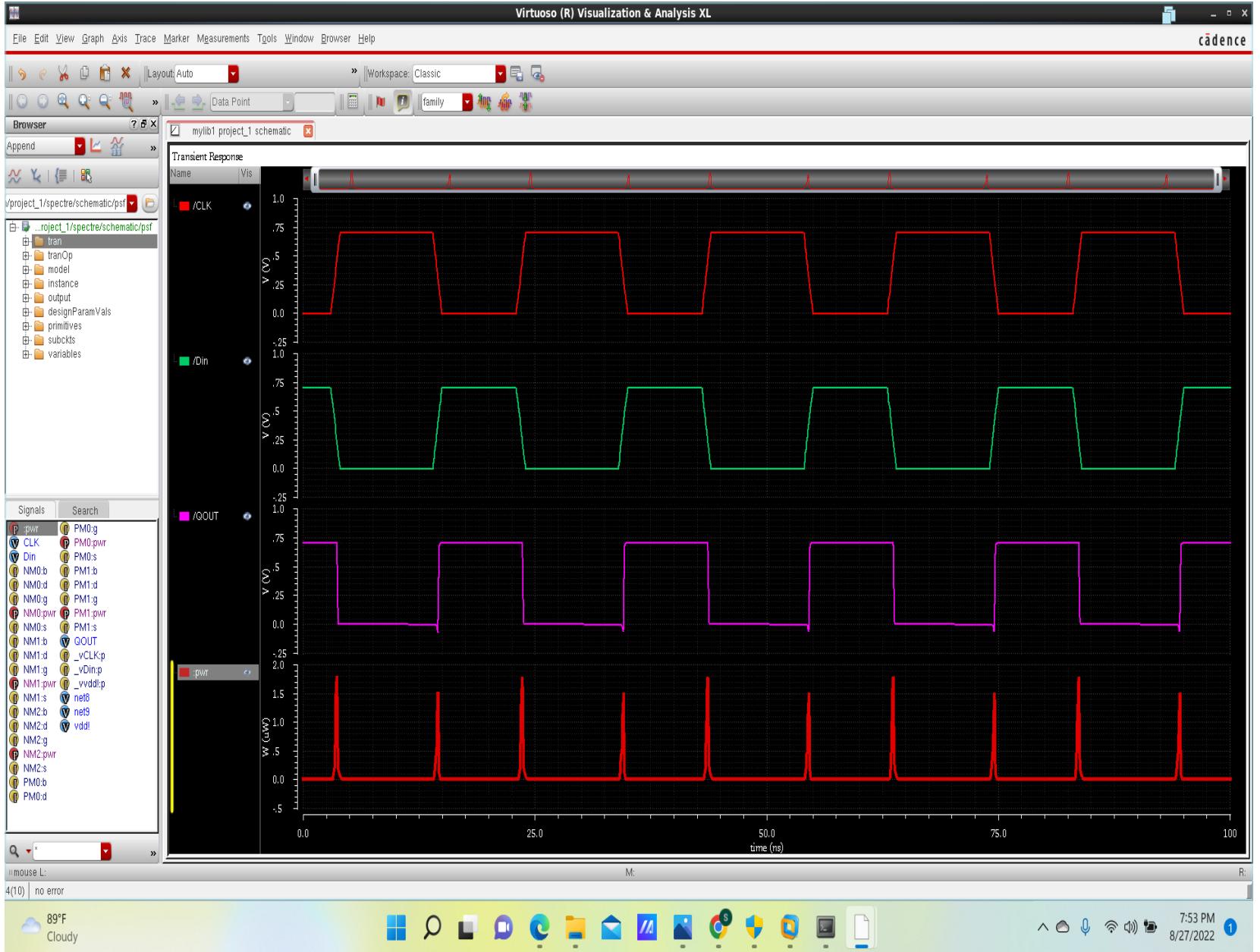
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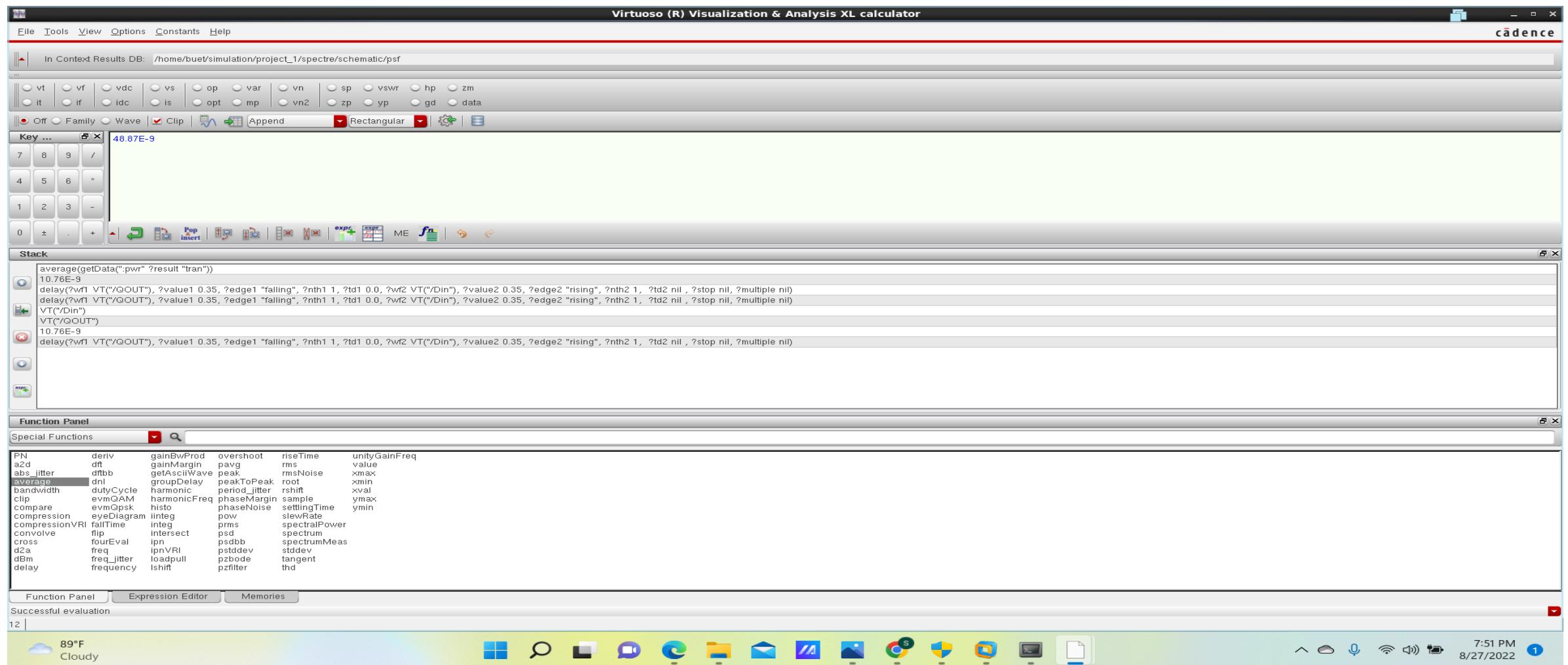
# Schematic



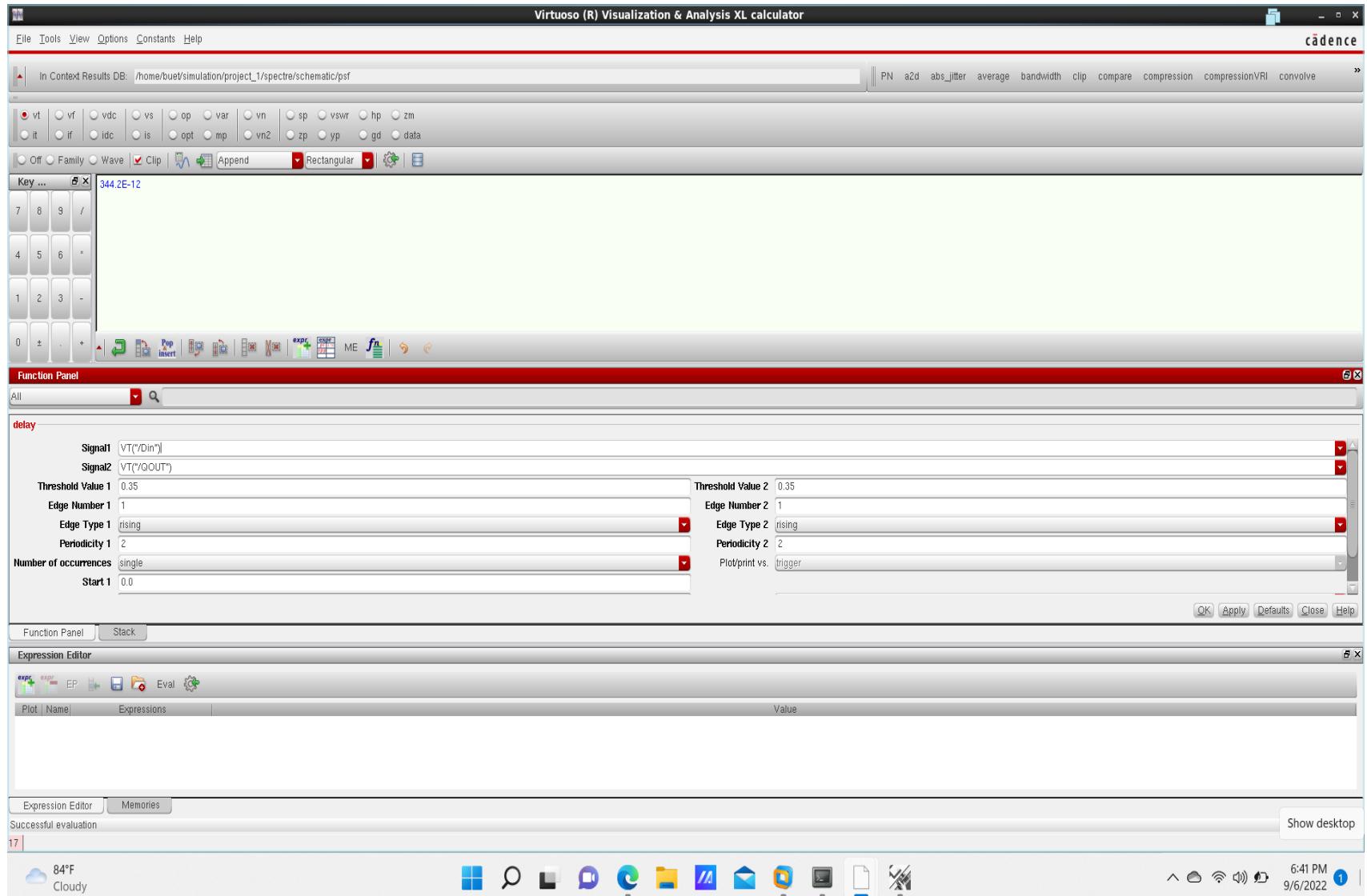
# Output



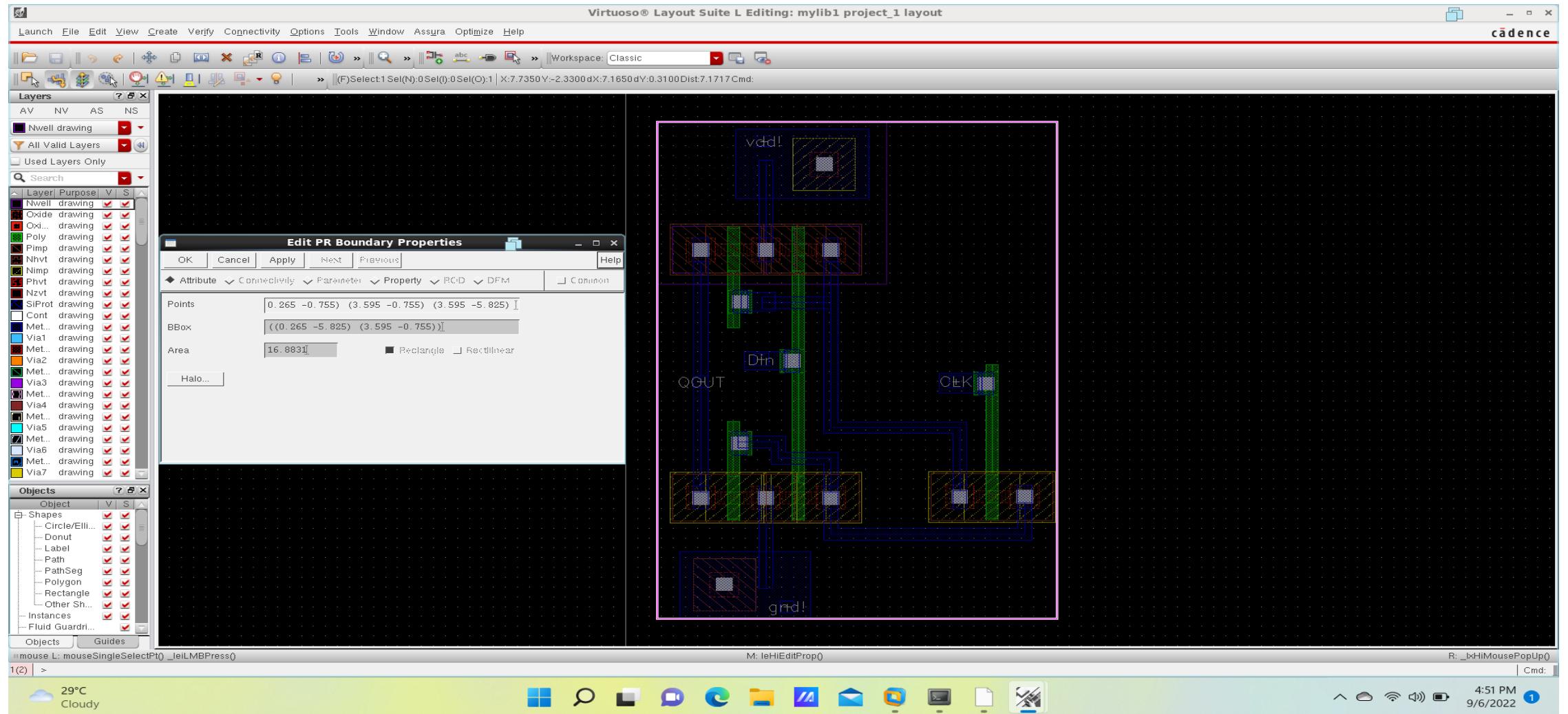
# Power



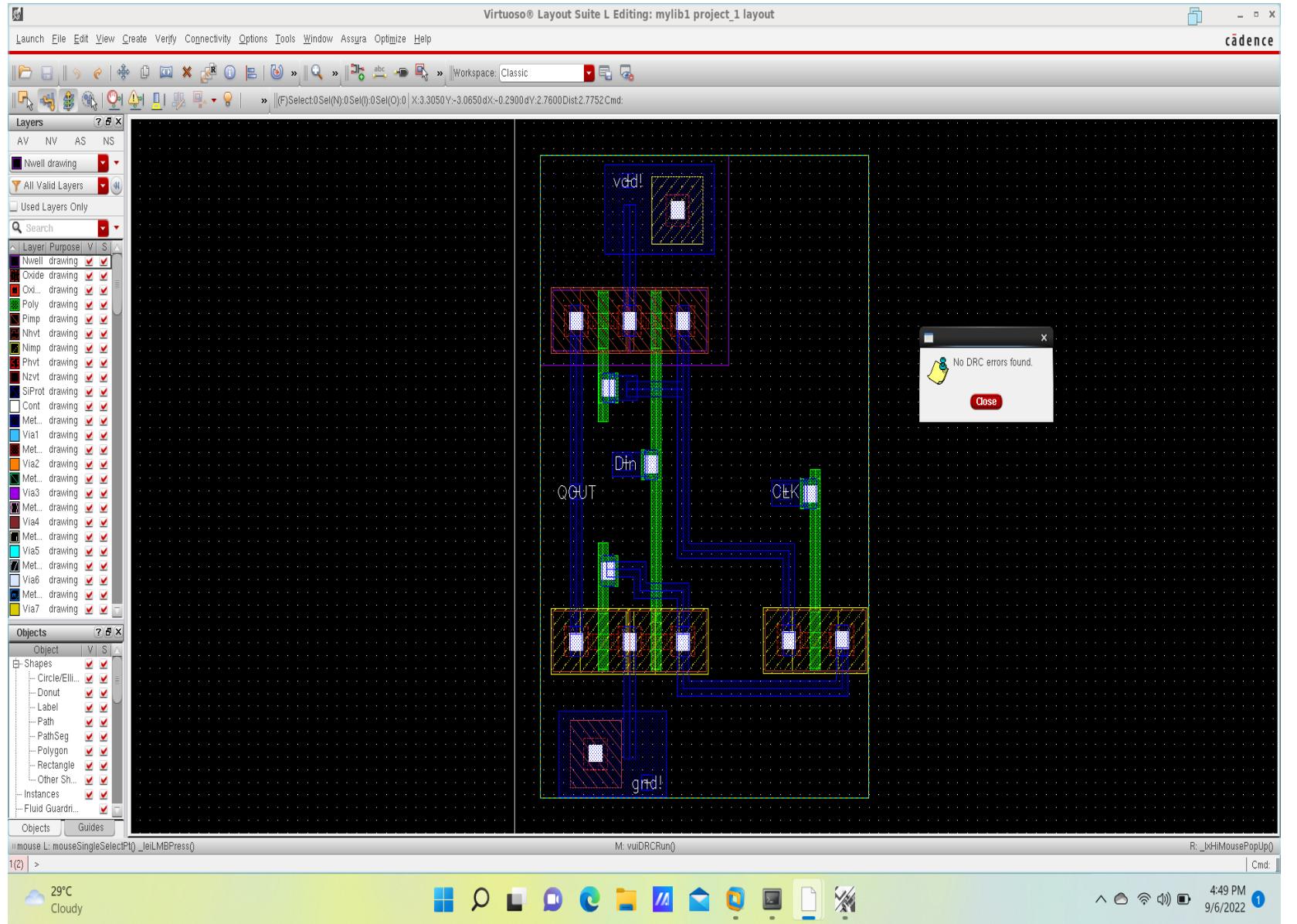
# Delay



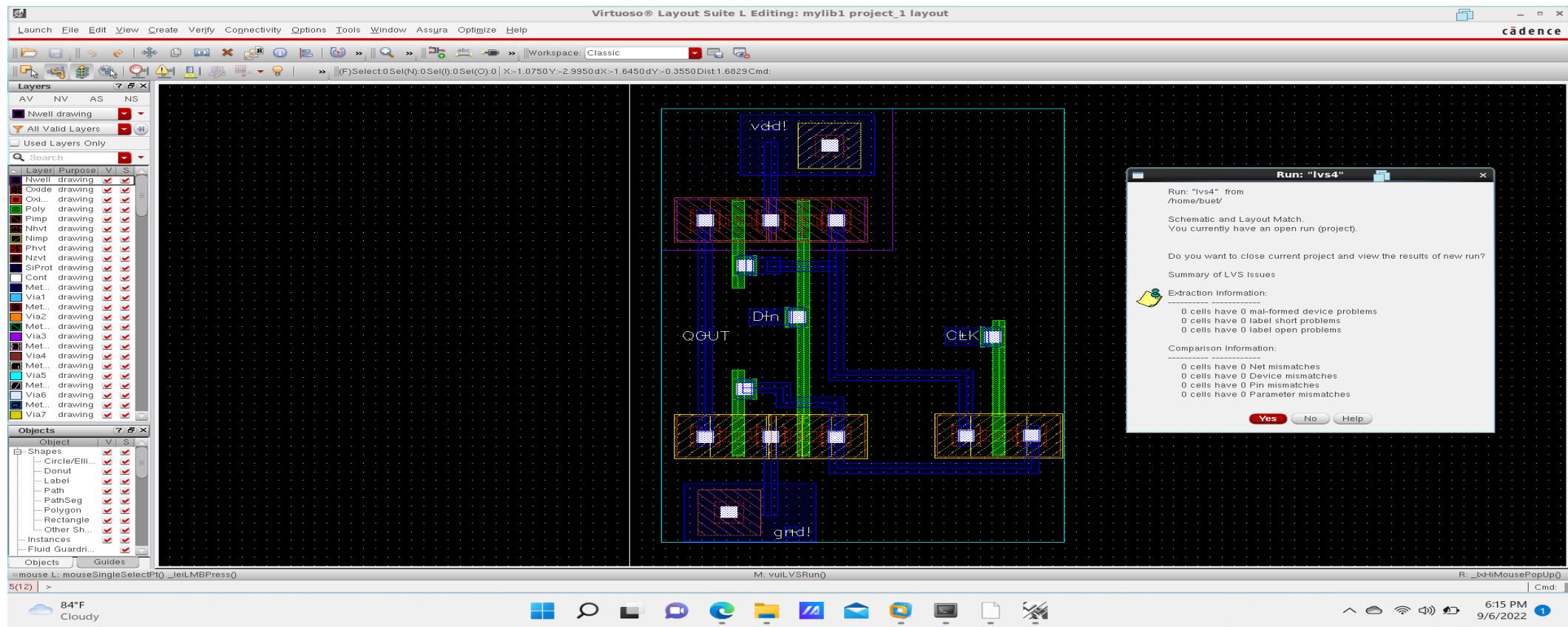
# Area



## No DRC

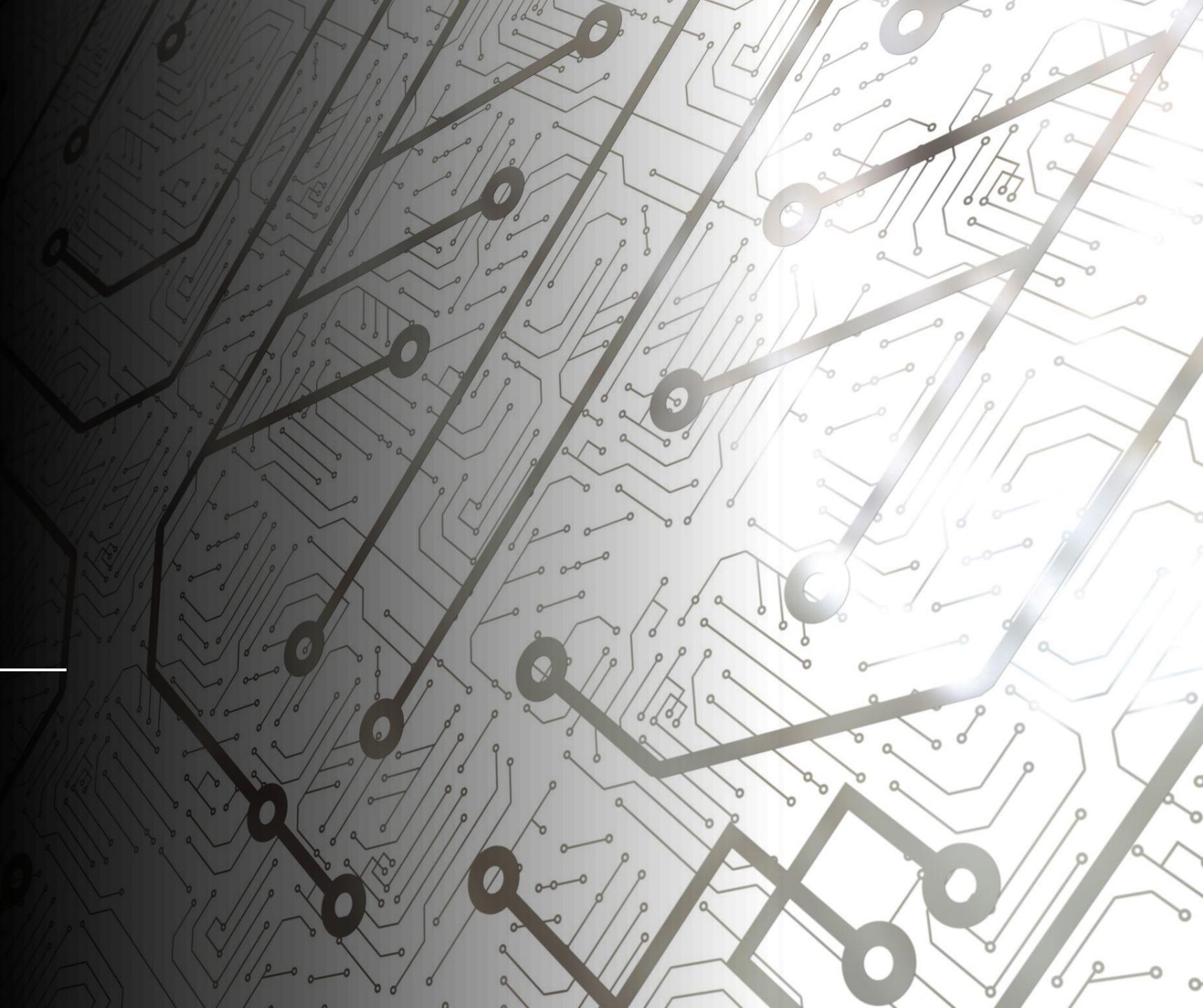


# LVS match

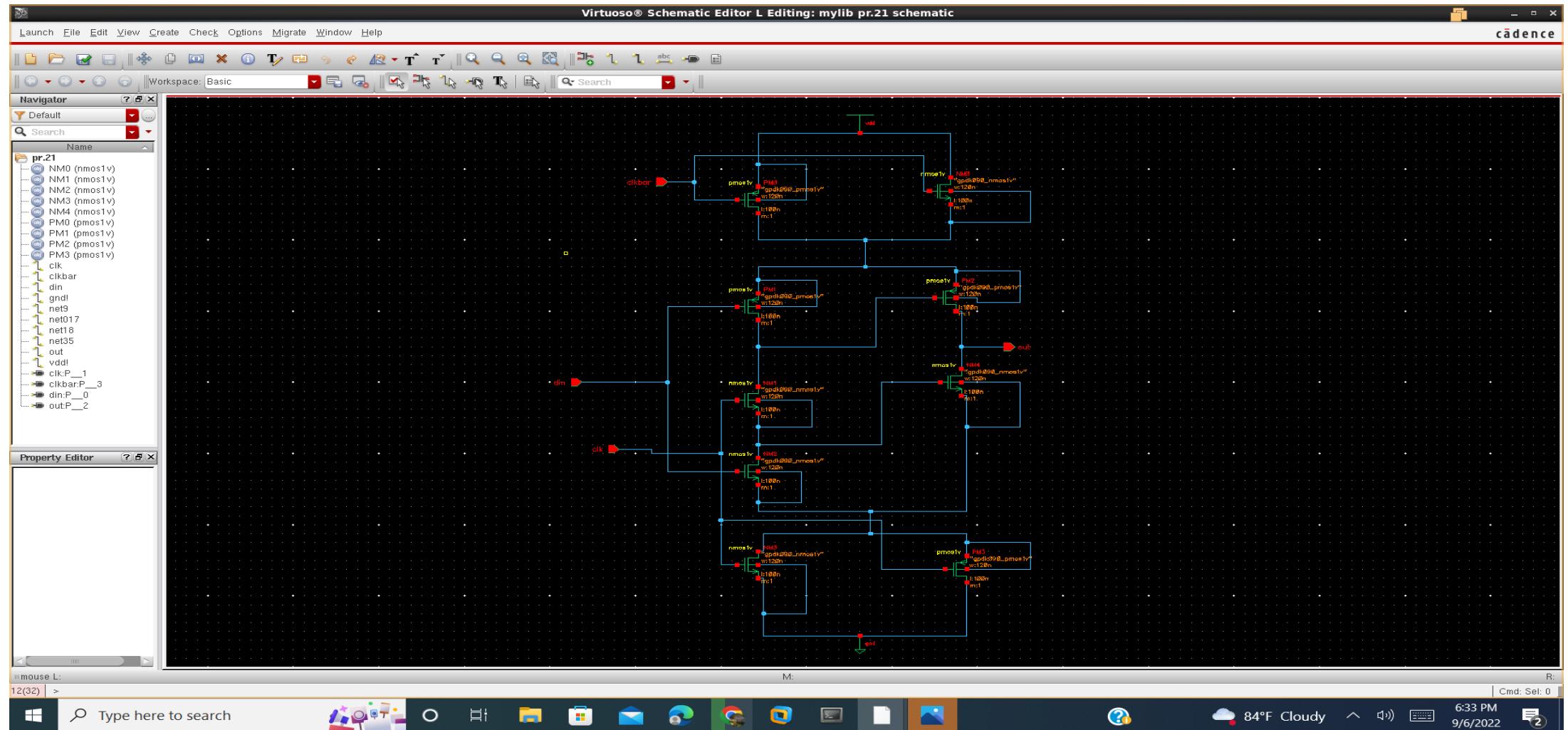


## Circuit-2

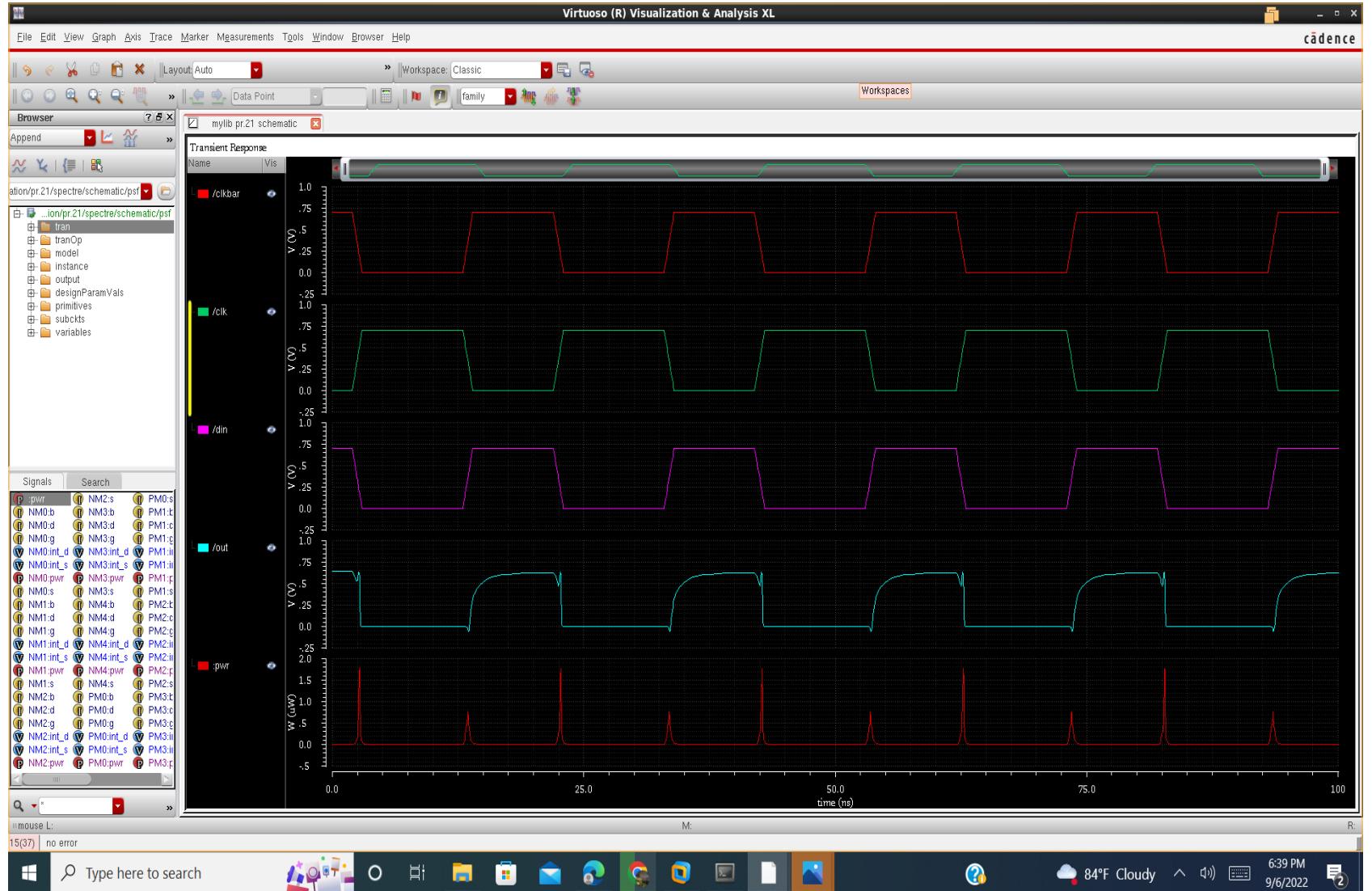
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# Schematic



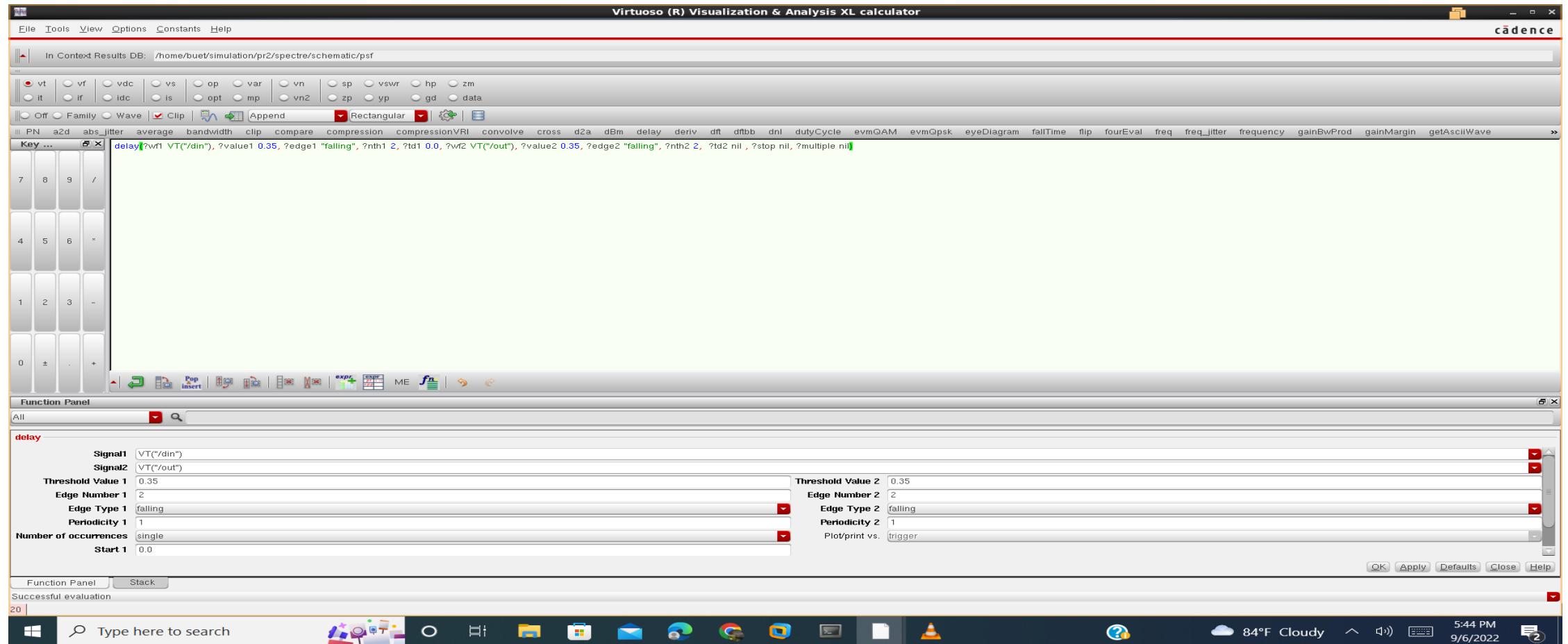
# Output



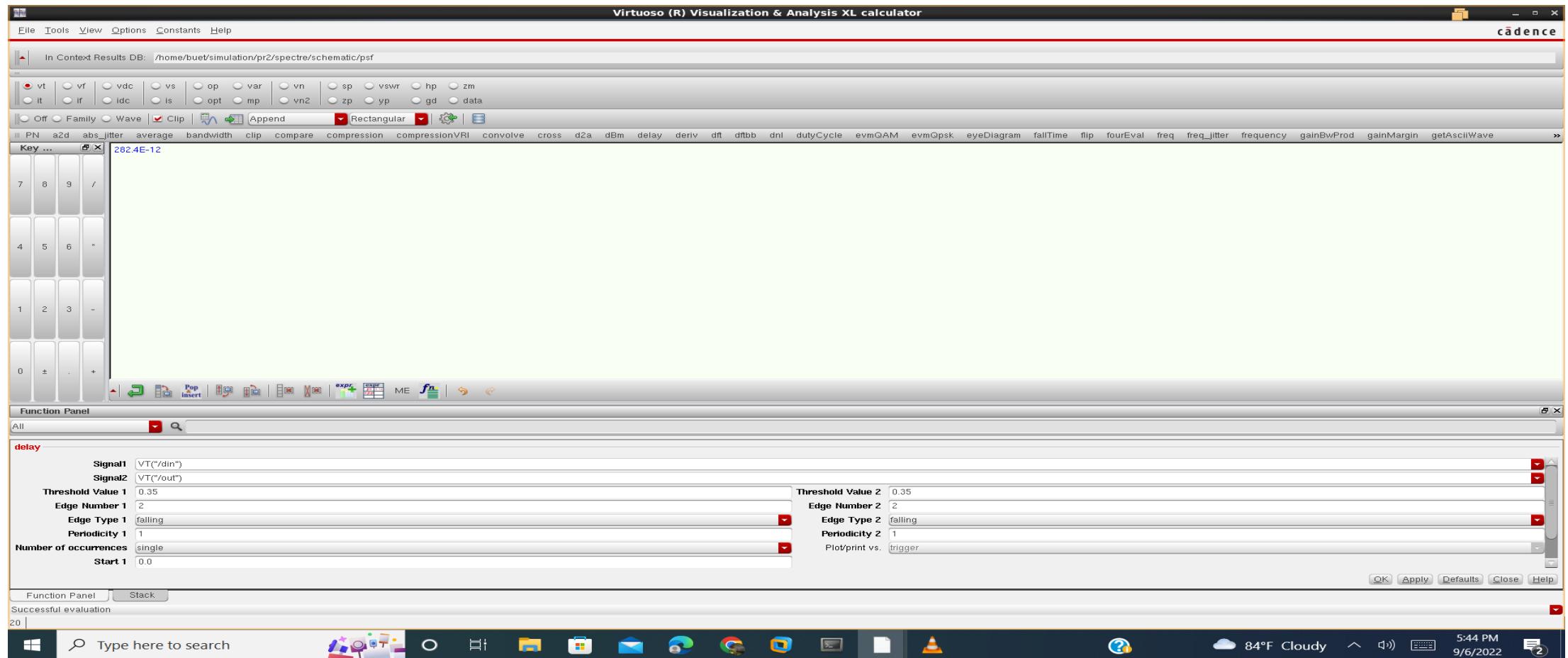
# Output curve



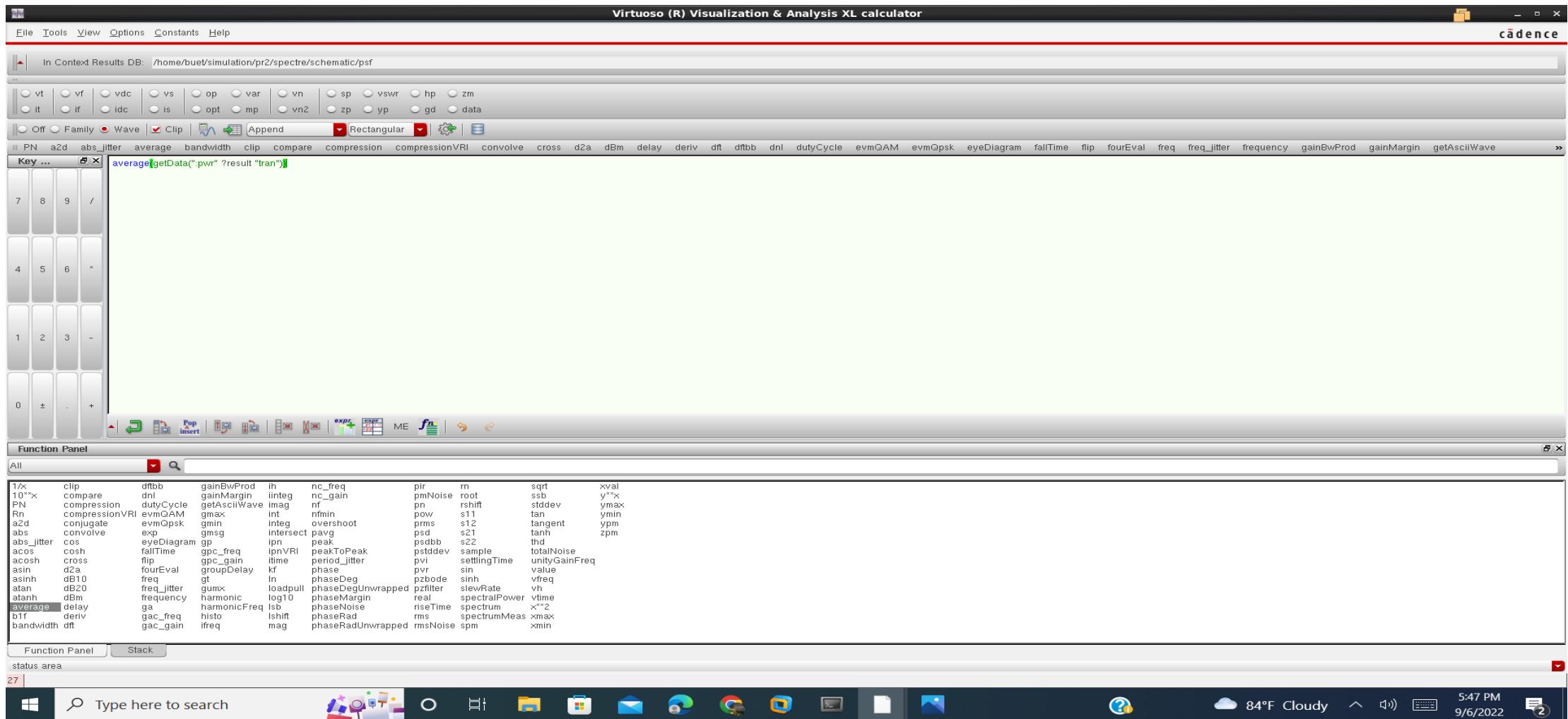
# Delay



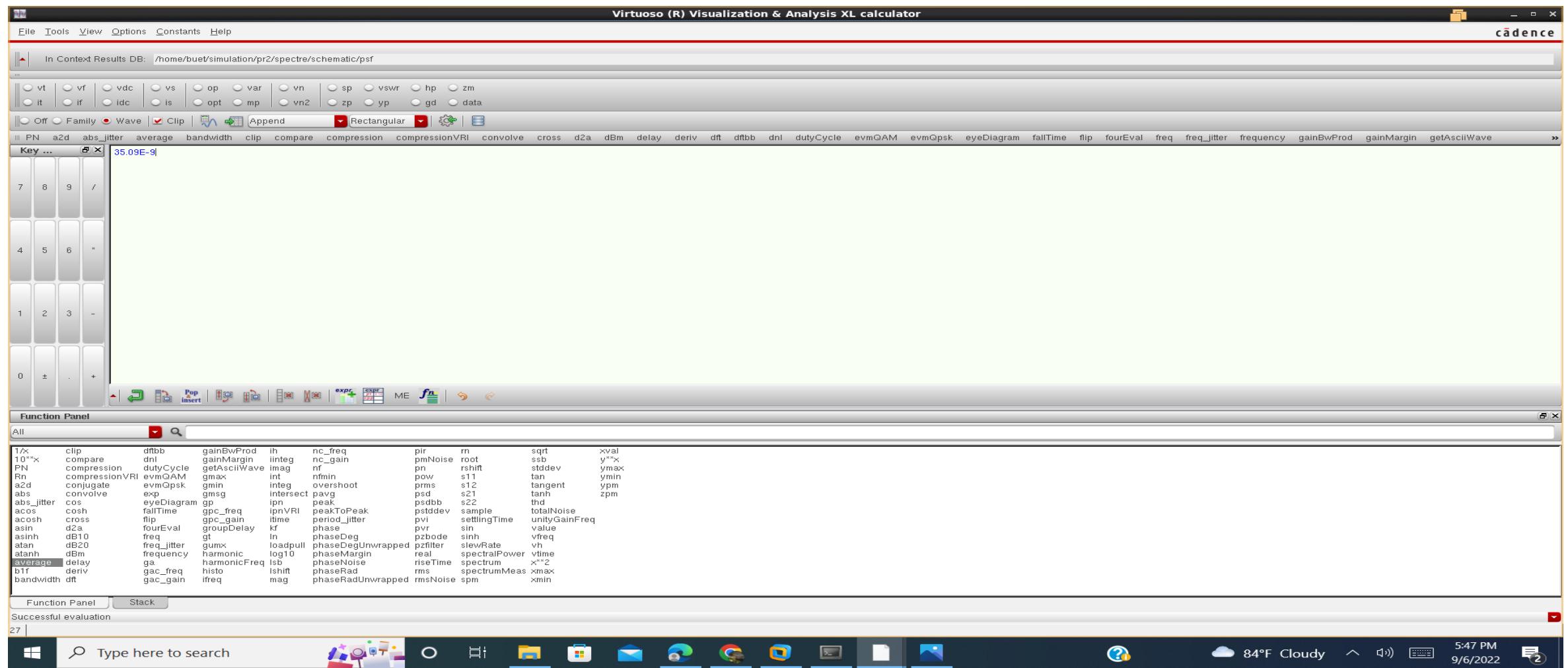
# Delay

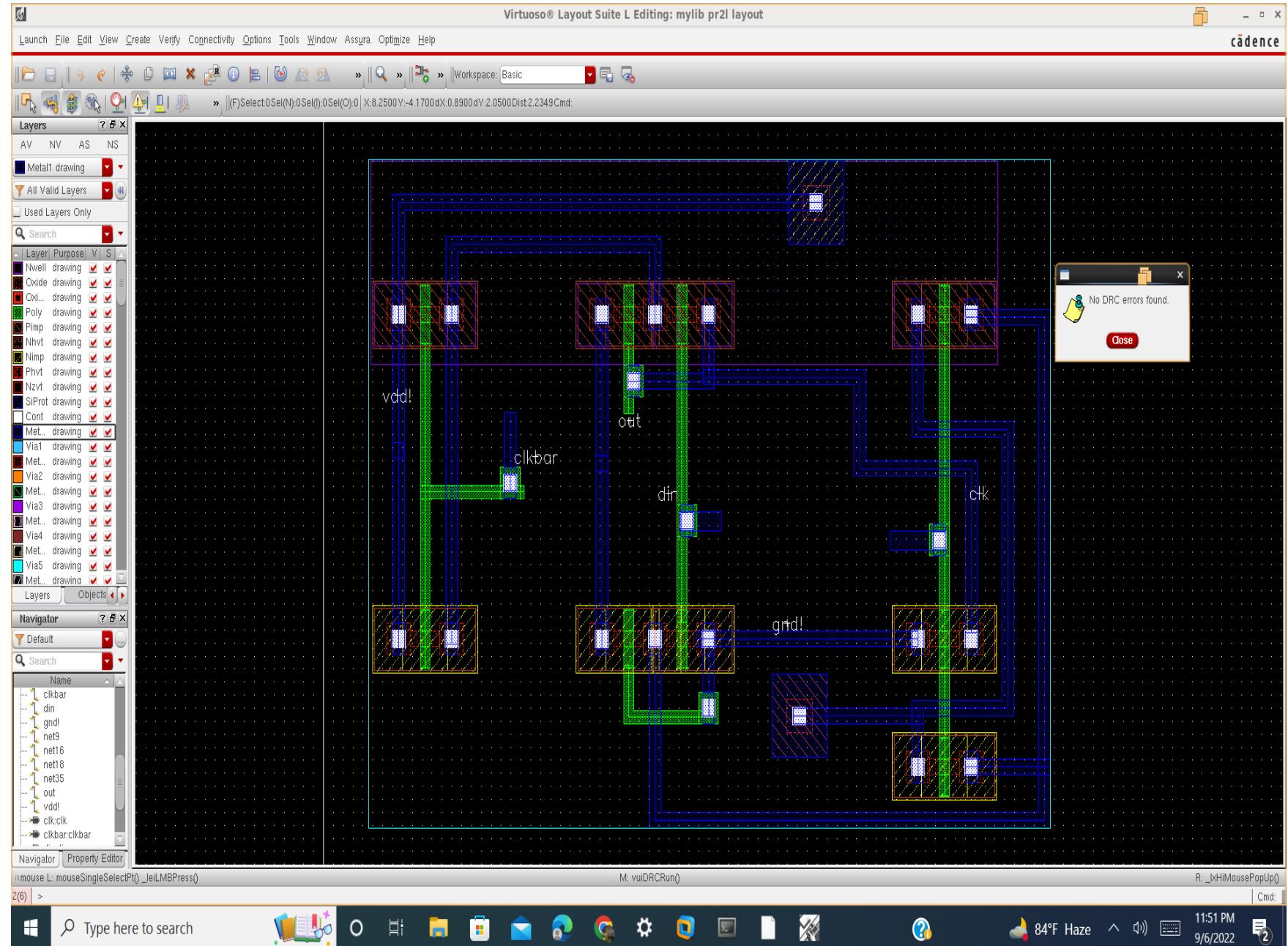
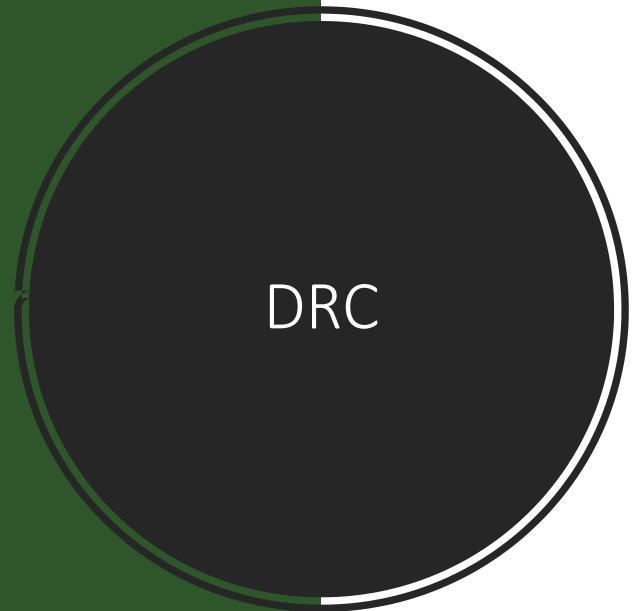


# Power

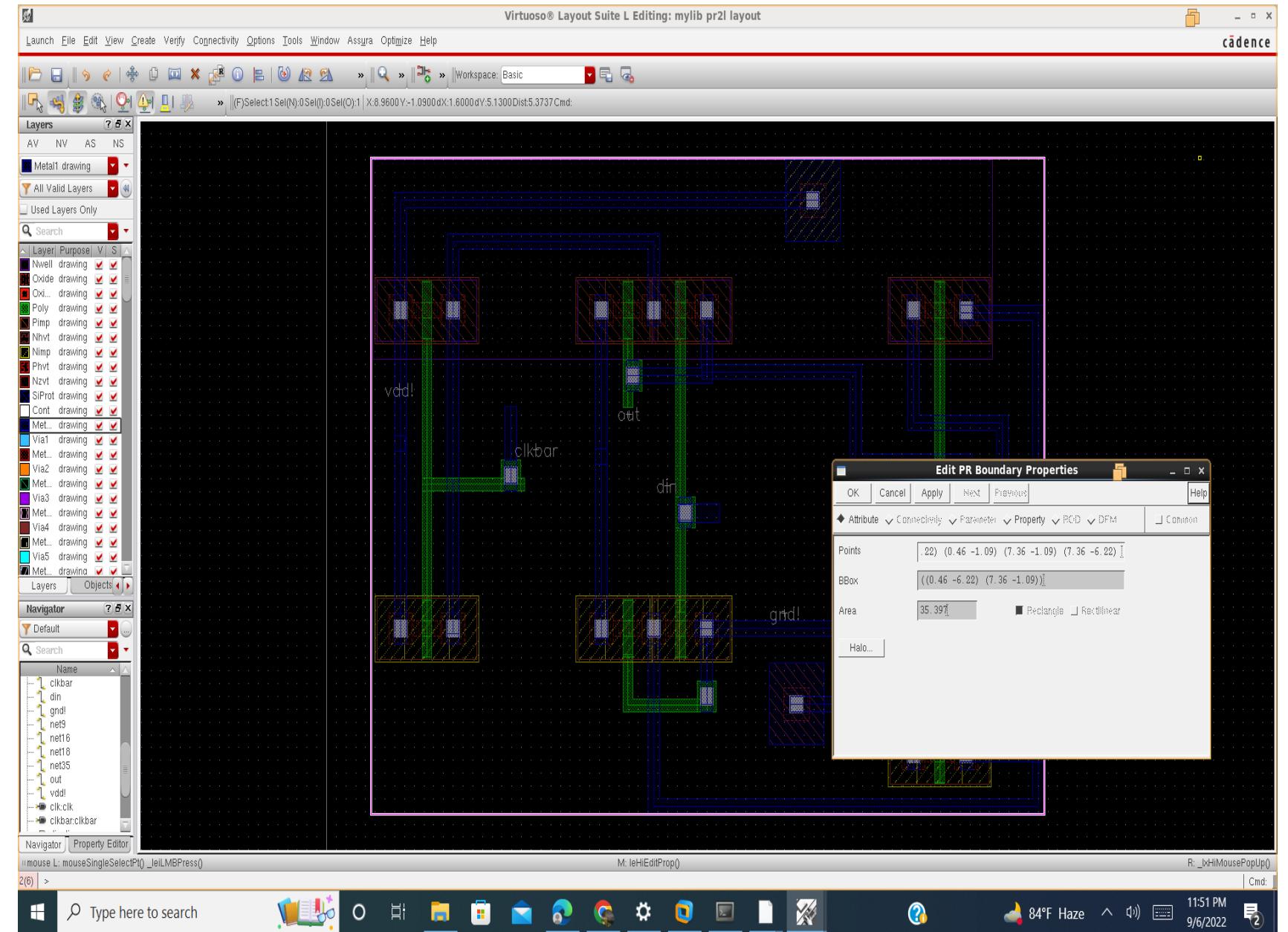


# Power

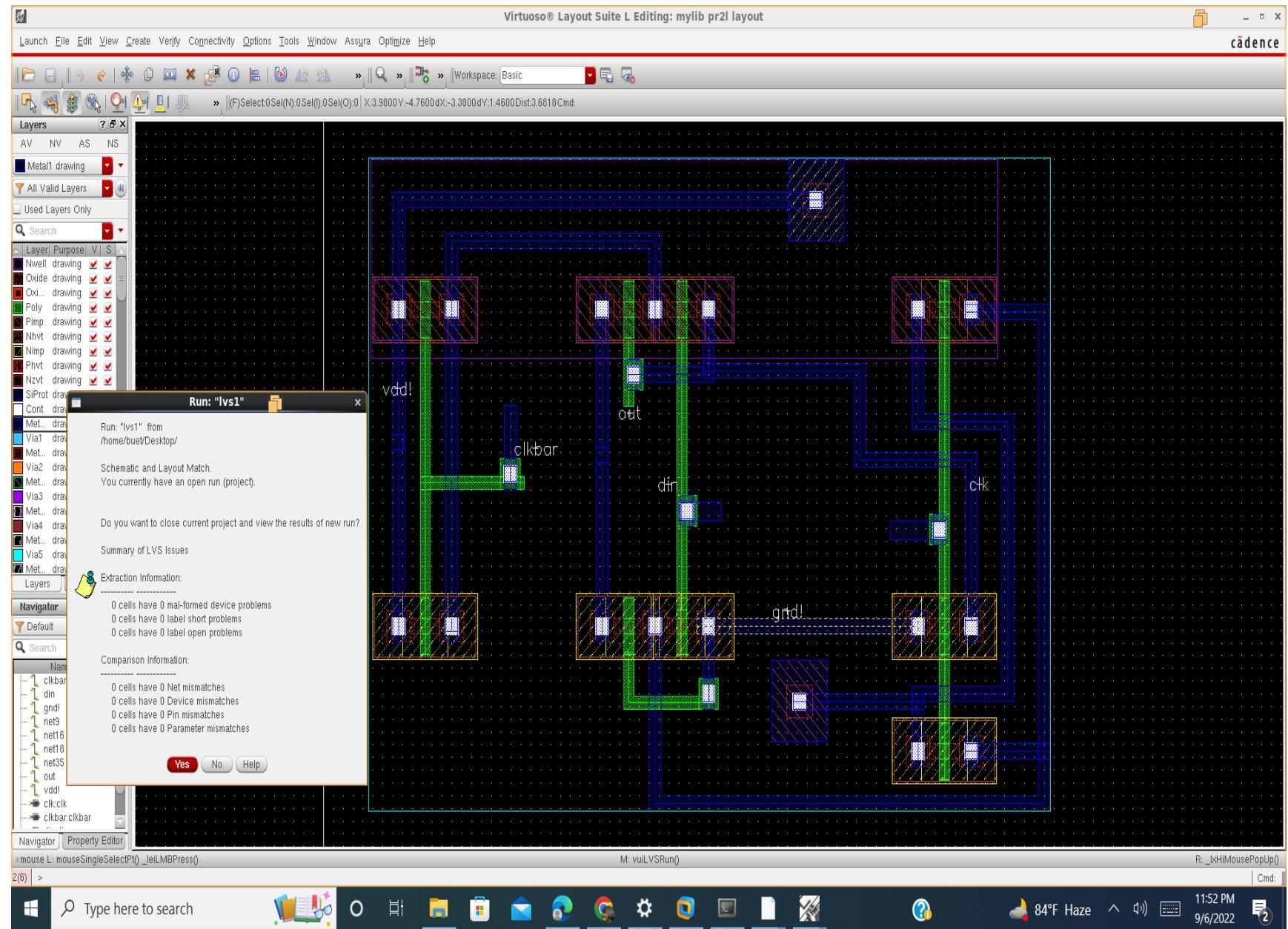


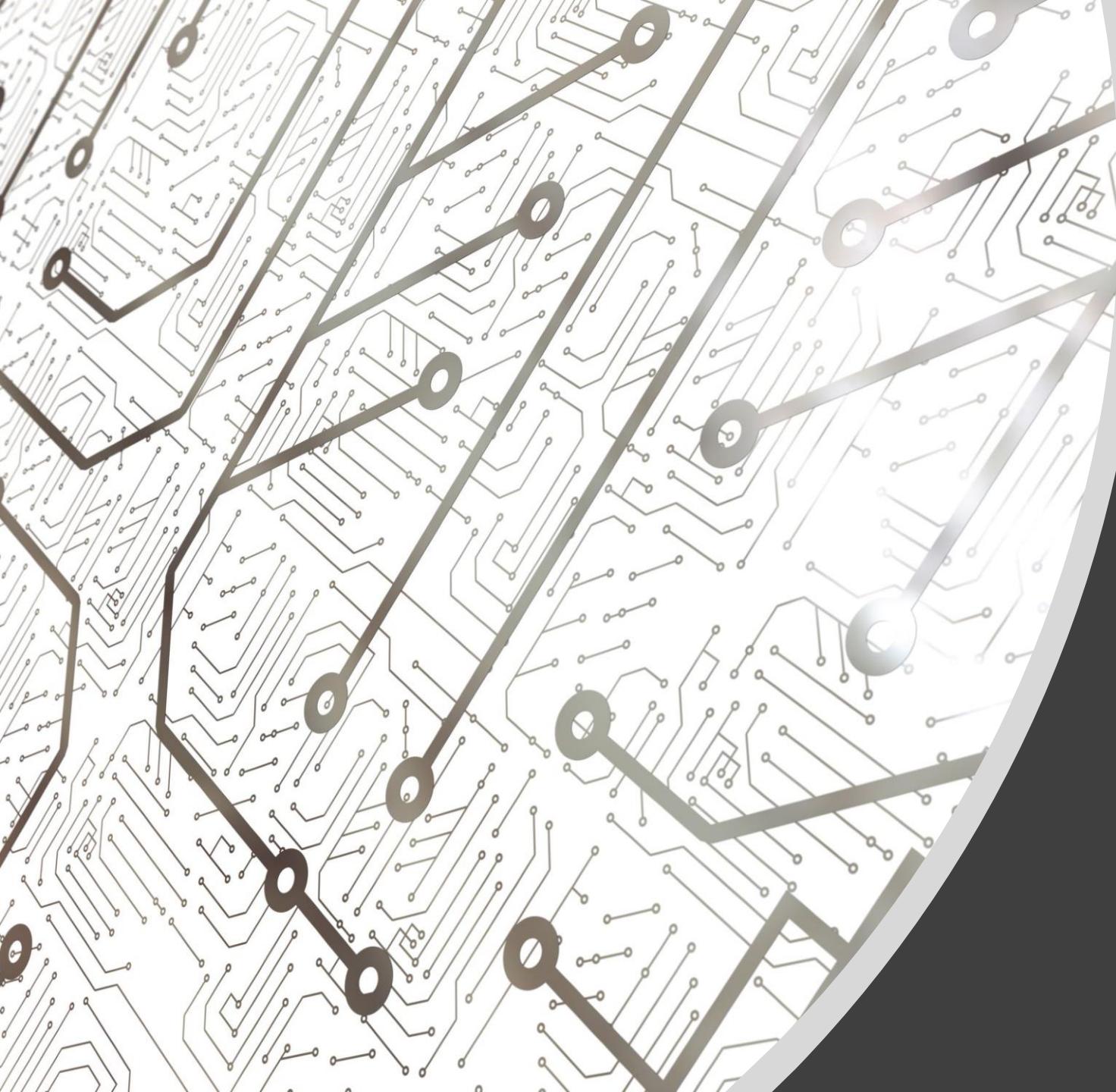


Area



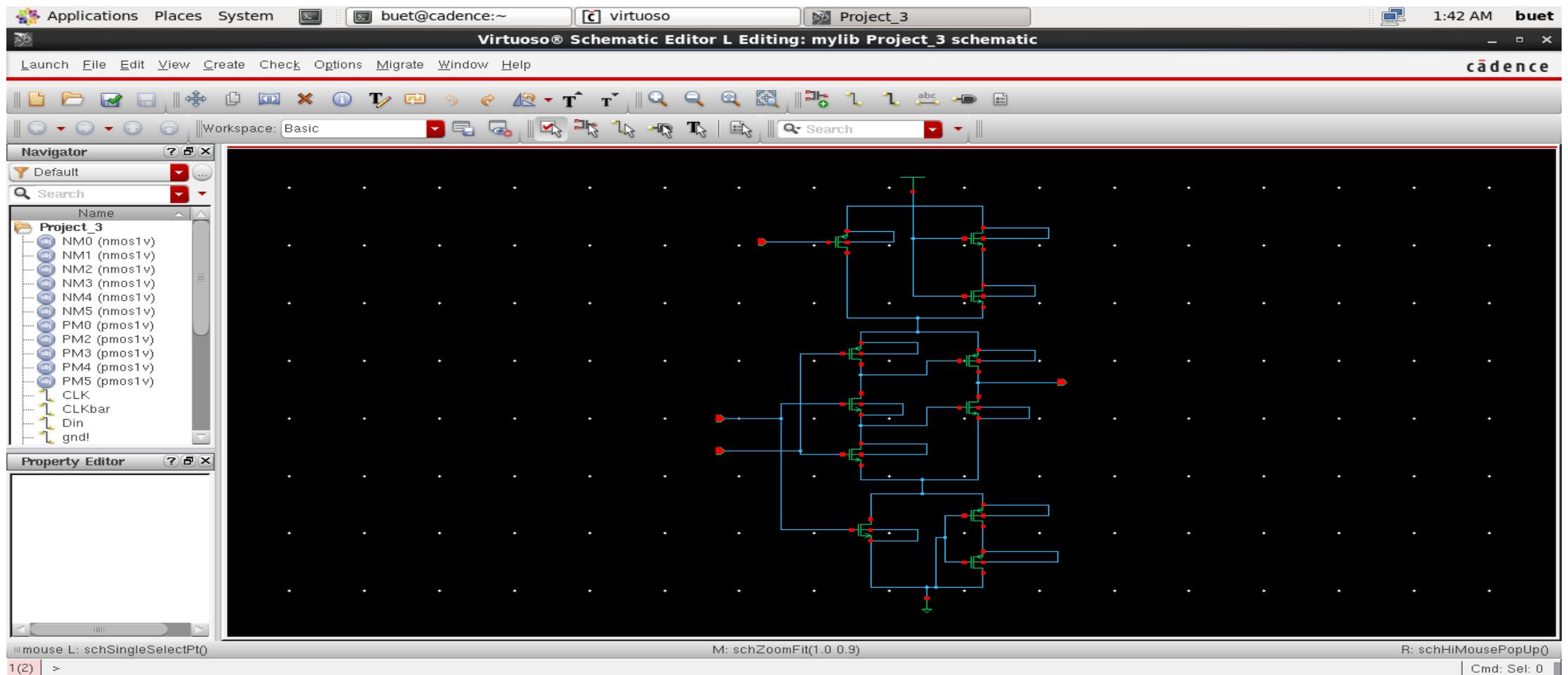
# LVS



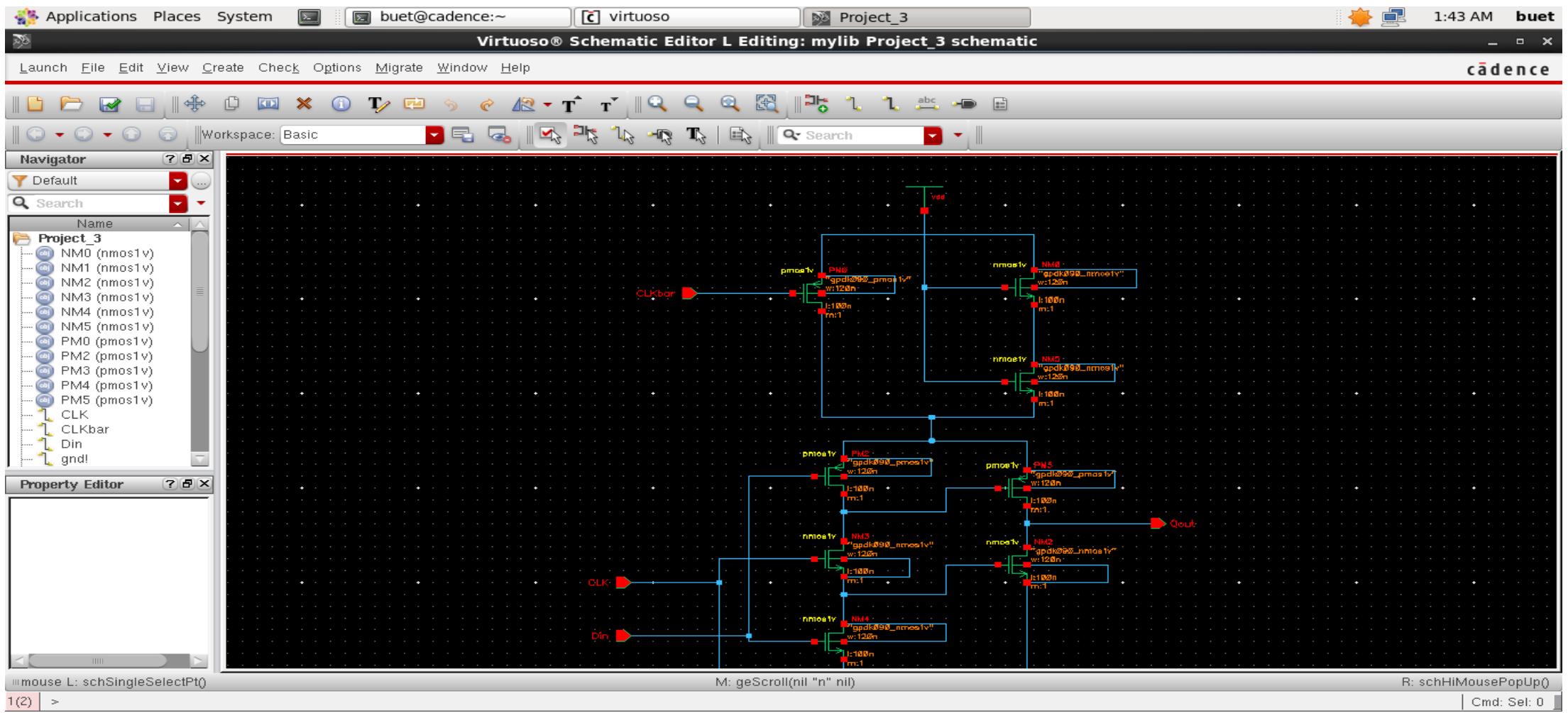


# Circuit-3

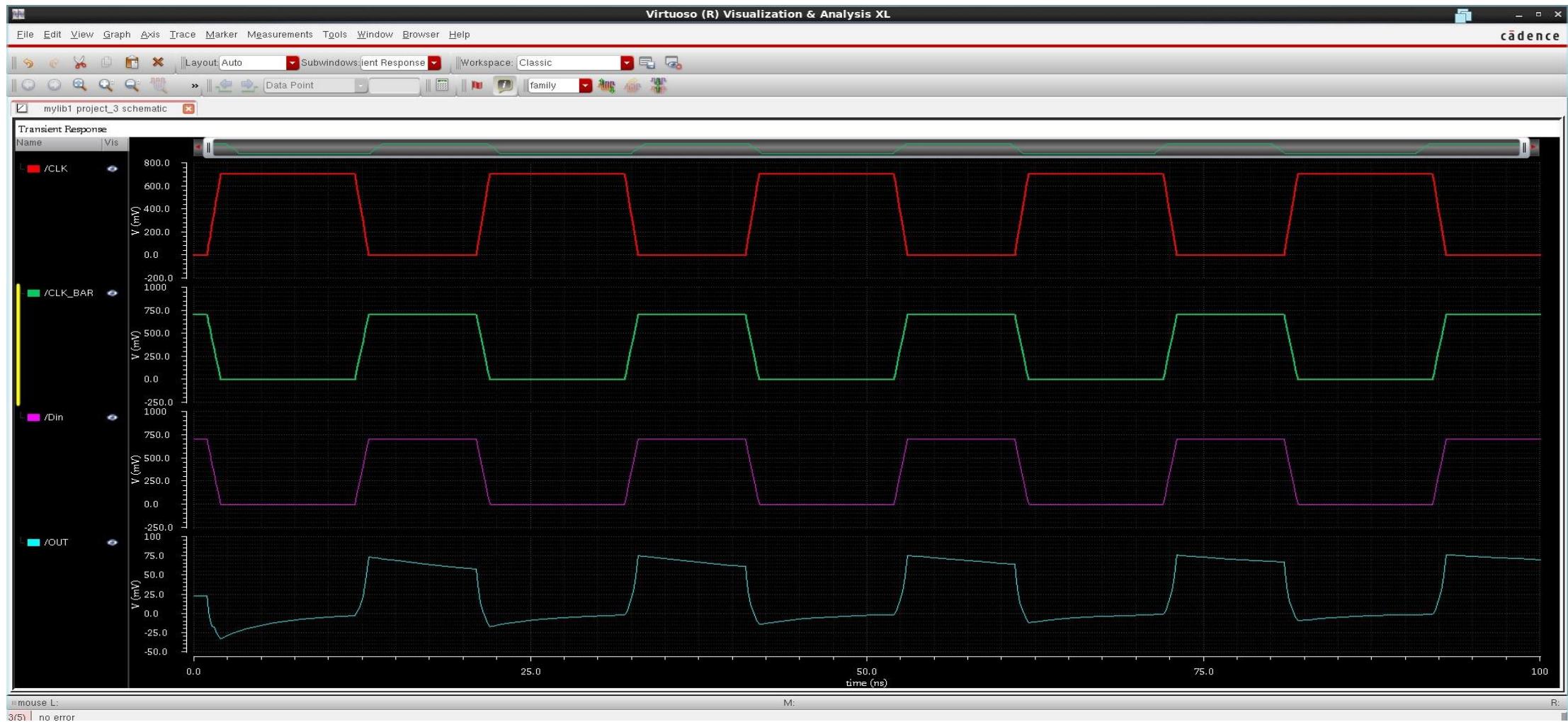
# Schematic



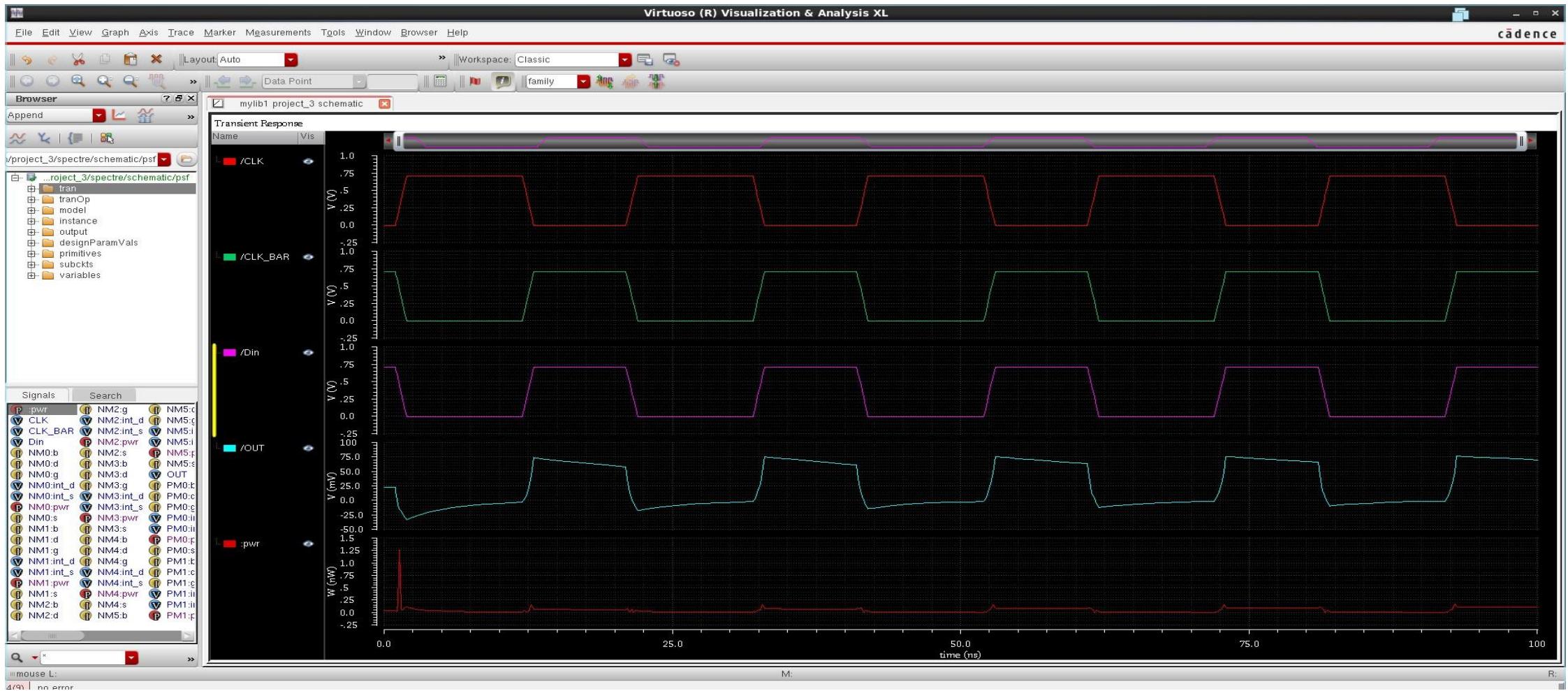
# Schematic



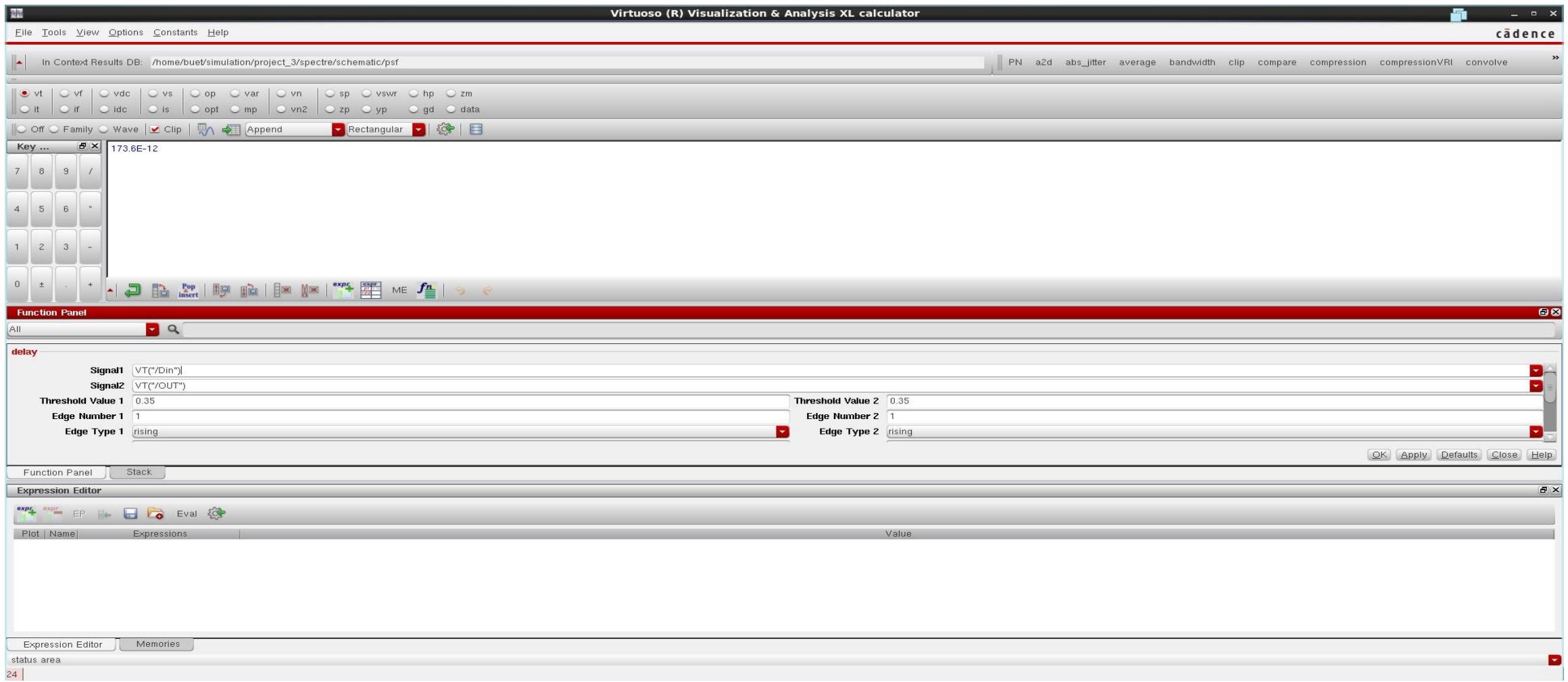
# Output response



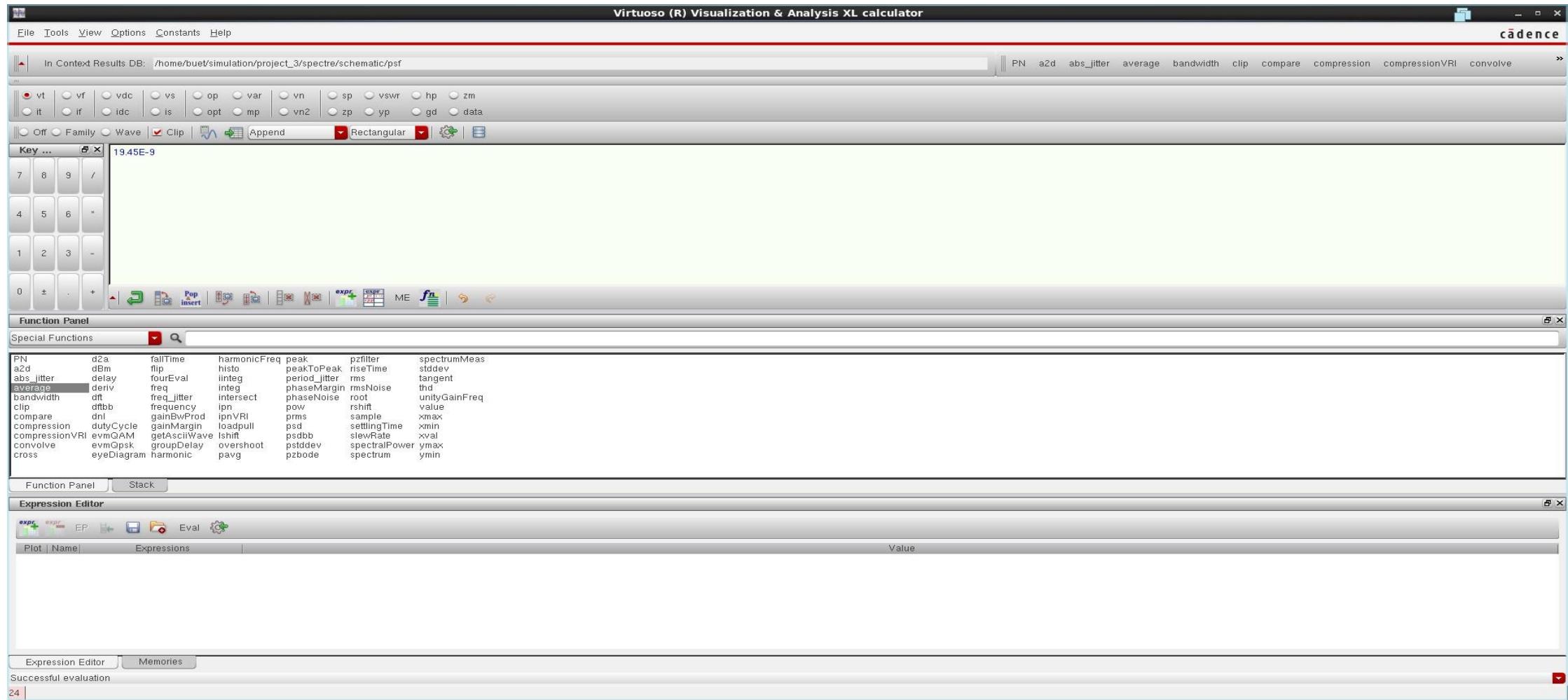
# Output response with PWR

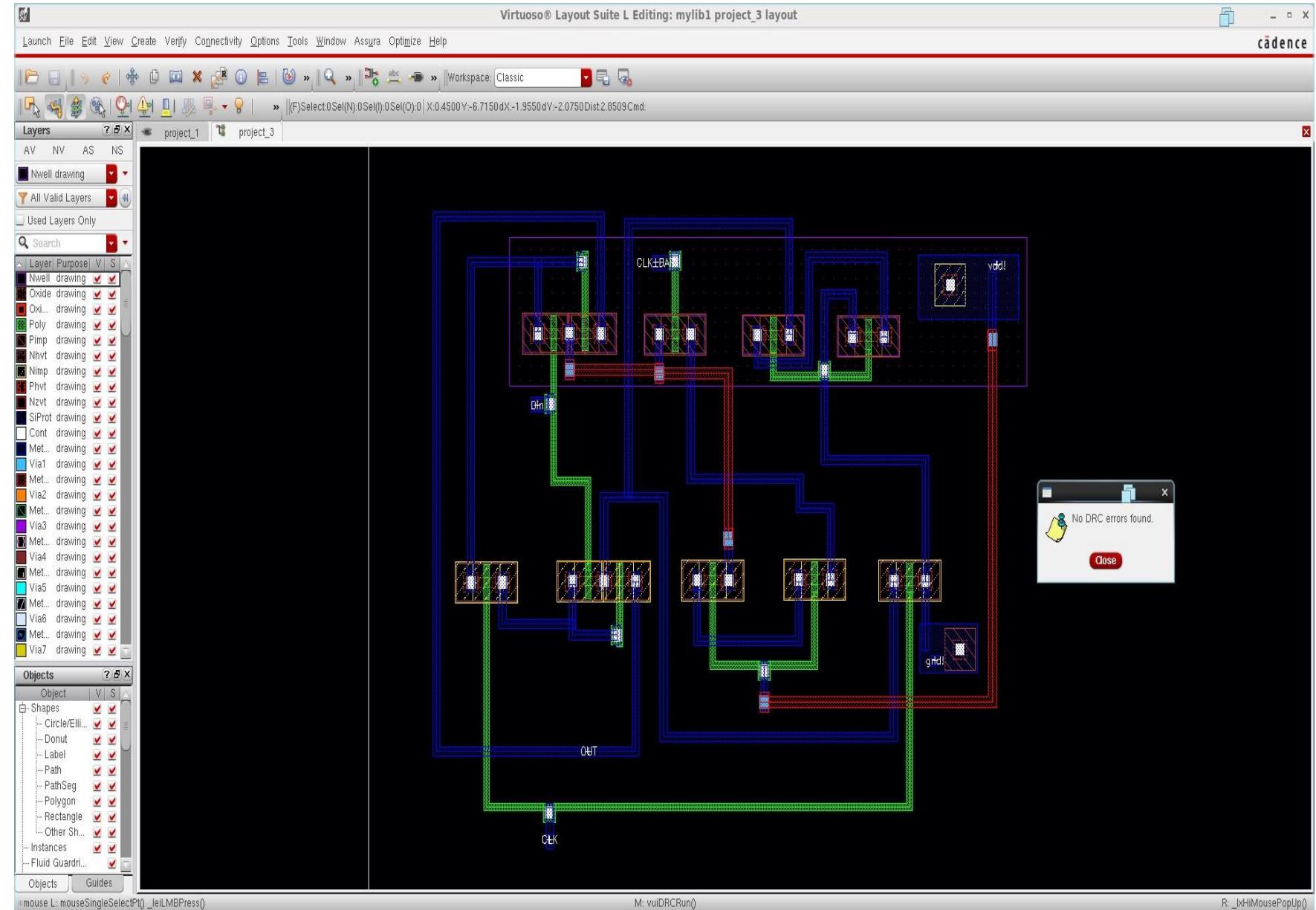
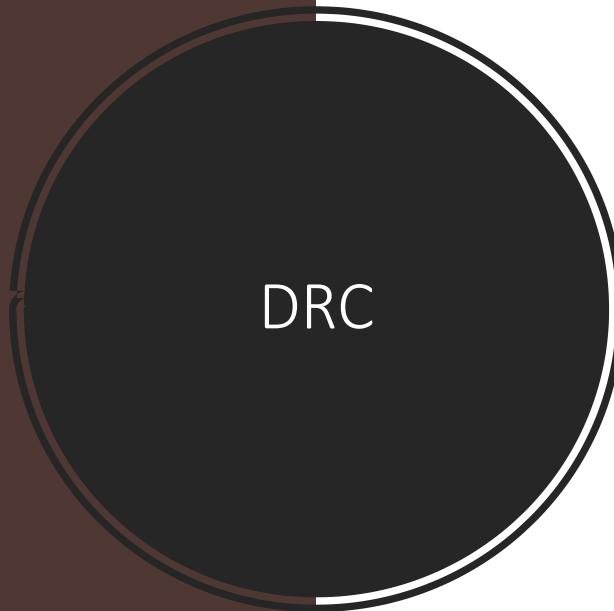


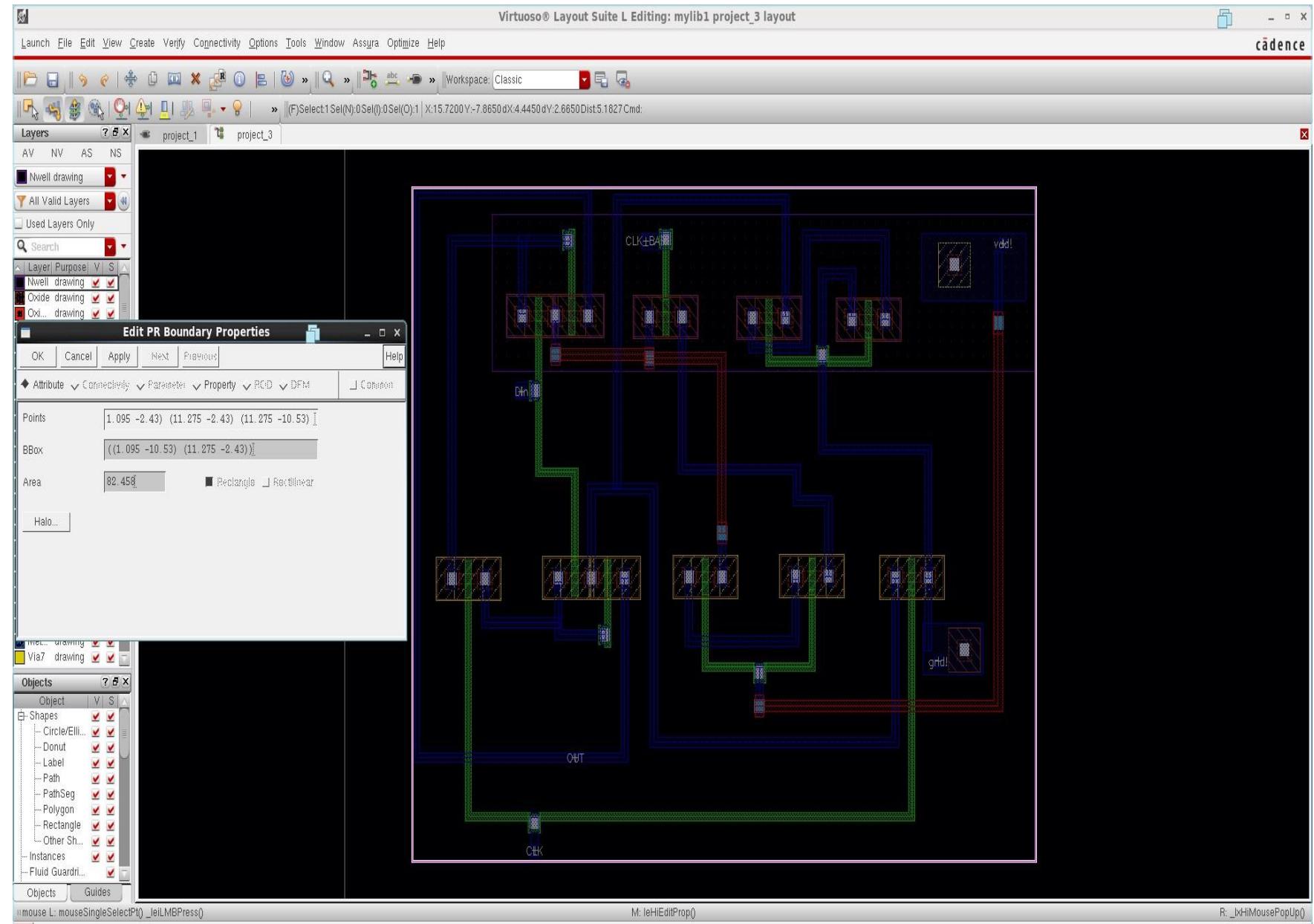
# Delay

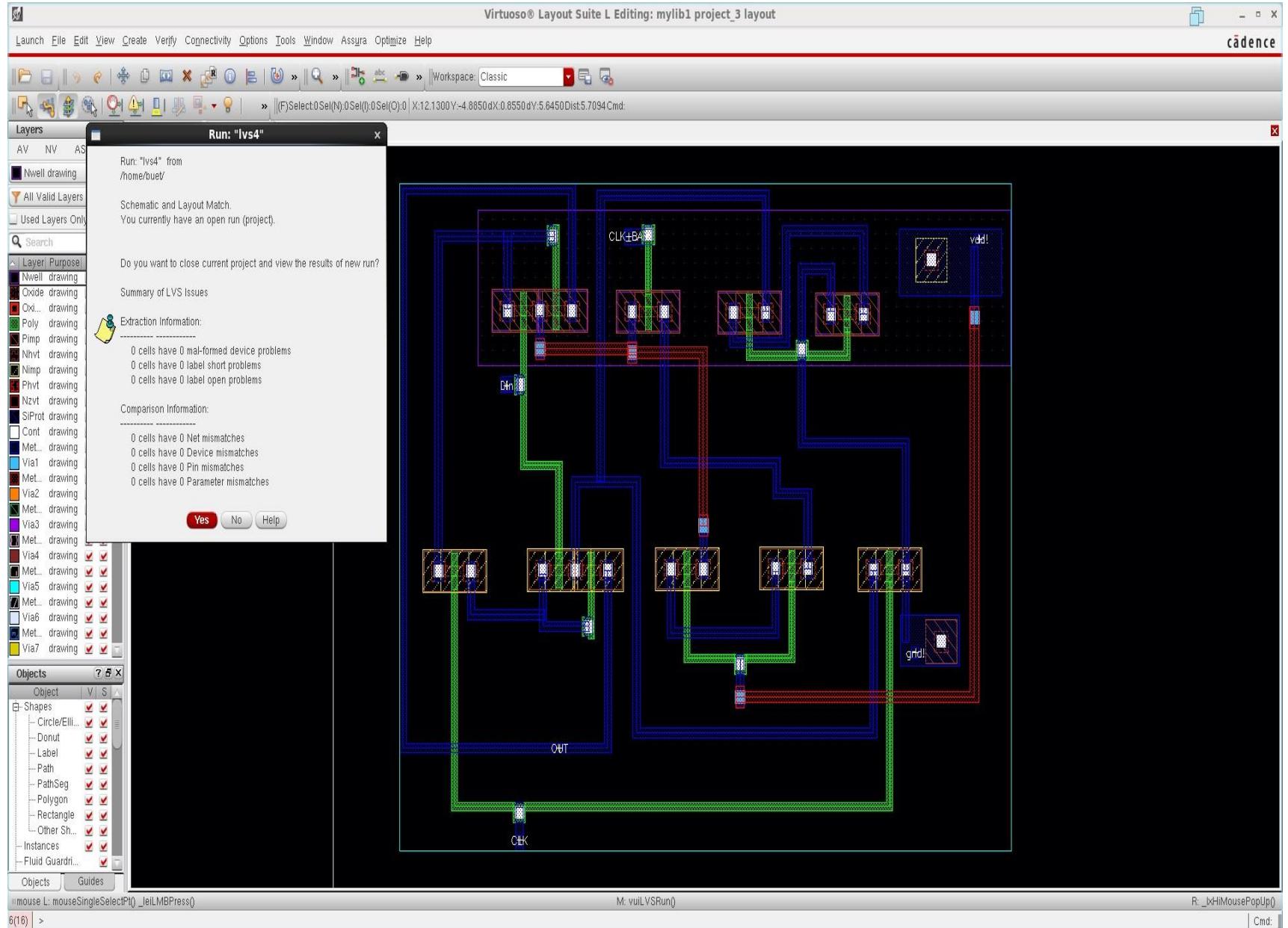


# Power









# Comparison between the circuits

- In this SVL method we want to decrease the delay time. Here we get lower delay time in circuit 1 to circuit 3. and dissipated power also lower from circuit 1 to circuit 3 .
- So, delay and power dissipation between three circuits are circuit 1>circuit 2>circuit 3. As a result, we can say that in our process for the d flipflop circuits, SVL is used properly.

|           | Propagation delay<br>(ps) | Average Power<br>(ps) | Power Delay Product<br>(ps) | Cell Area<br>(um^2) | No. of DRC errors | No. of LVS Mismatches |
|-----------|---------------------------|-----------------------|-----------------------------|---------------------|-------------------|-----------------------|
| Circuit-1 | 344.2                     | 48.87                 | $1.682 \times 10^{-17}$     | 16.8831             | 0                 | 0                     |
| Circuit-2 | 282.4                     | 35.09                 | $9.90 \times 10^{-18}$      | 35.397              | 0                 | 0                     |
| Circuit-3 | 173.6                     | 19.45                 | $3.38 \times 10^{-18}$      | 82.458              | 0                 | 0                     |