AC701 EVALUATION BOARD HW-A7-AC701
(XC7A200T-FBG676)

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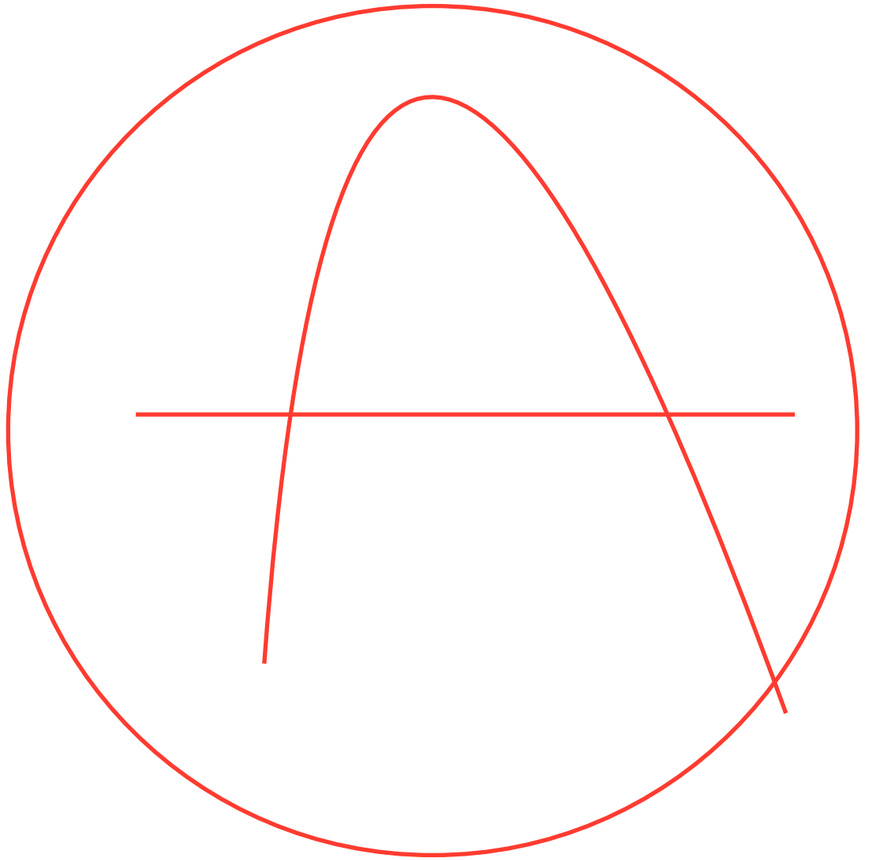

REV. 2.0

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PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DISCLAIMER		
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IRONWOOD FGG/FBG676 SOCKET
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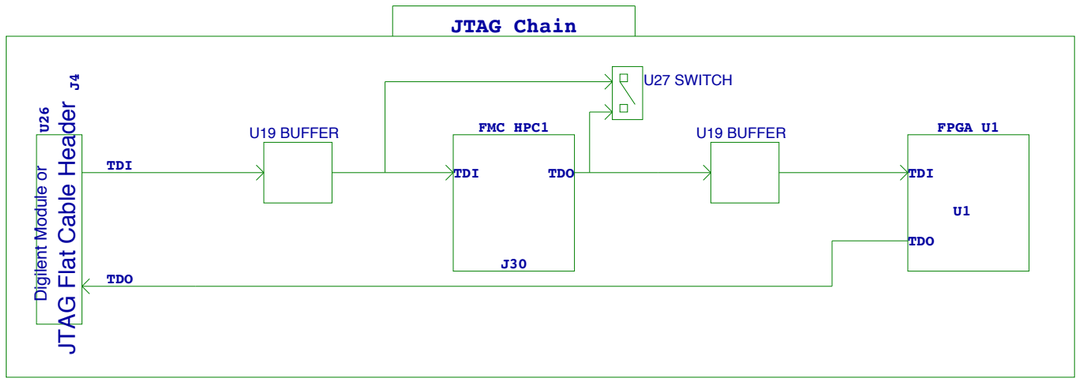
JTAG Chain



IIC Addressing

0b1110100	PCA9548a
0b1011101	SI570
0bxxxxx00	FMC HPC 1
0b1010100	IIC EEPROM
0b1010000	SFP+
0b0111001	ADV7511
0b1010000 0b0011000	DDR3 SODIMM
0b1010000	SI5324

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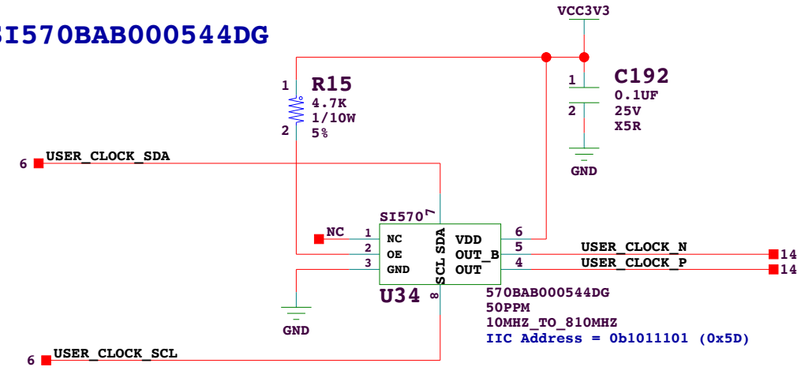
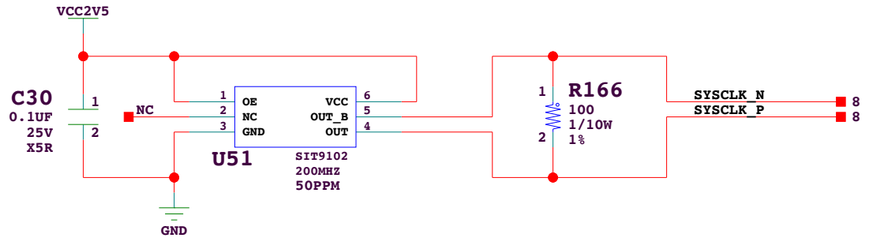
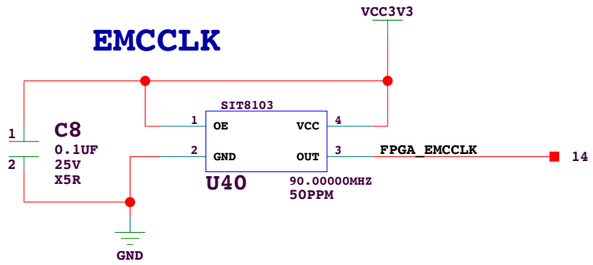
SI570BAB000544DG

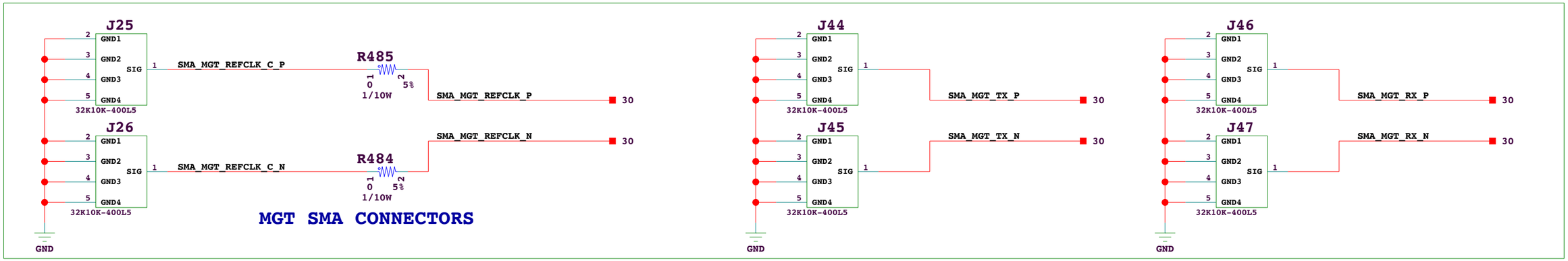


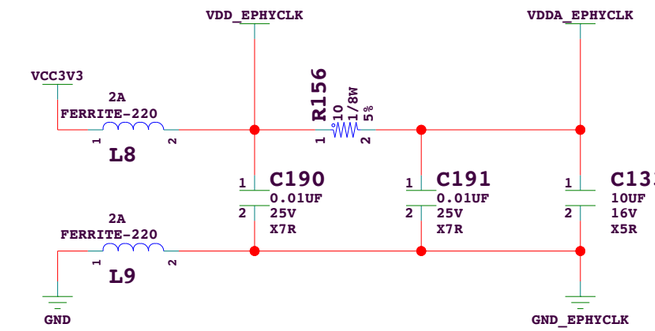
SIT9102AI-243N25E200.0000

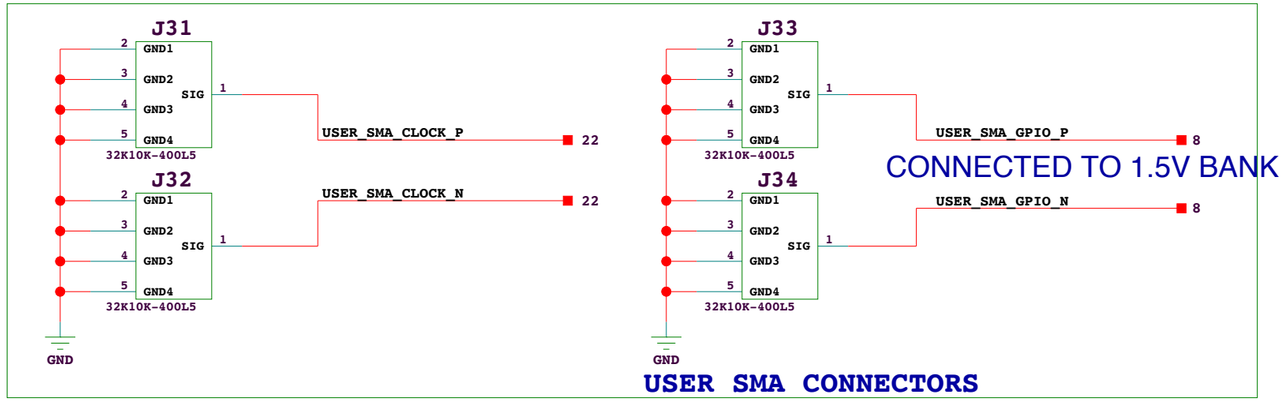


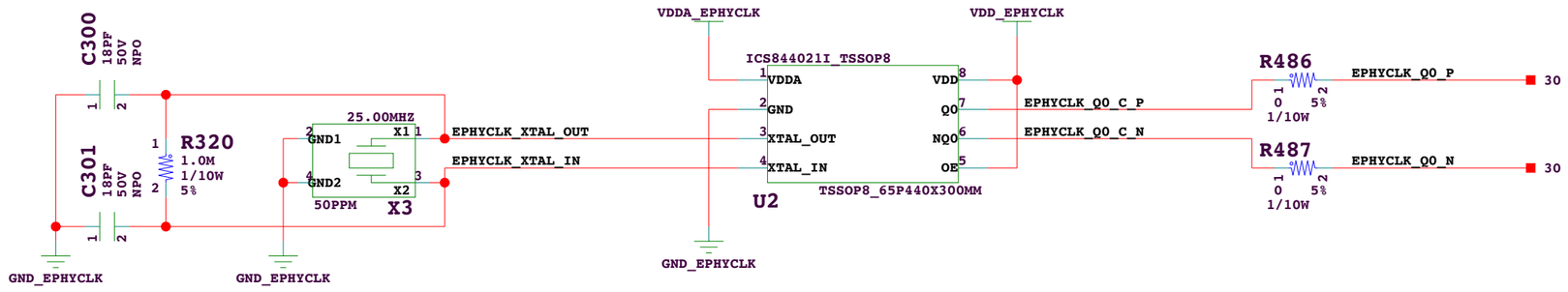
EMCCLK











Clocks

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Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
CLOCKS

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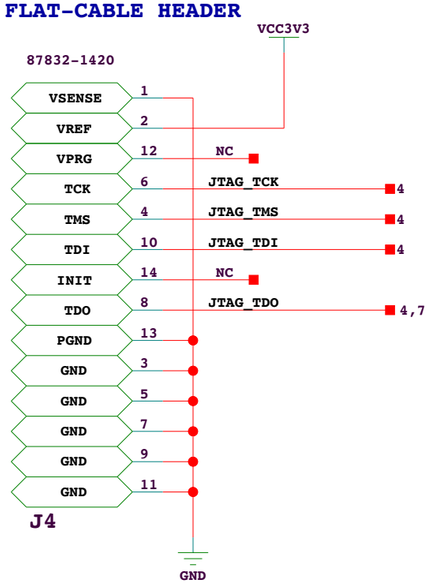
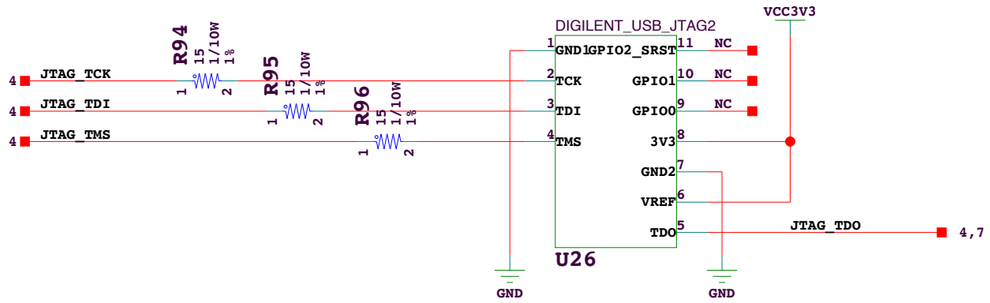
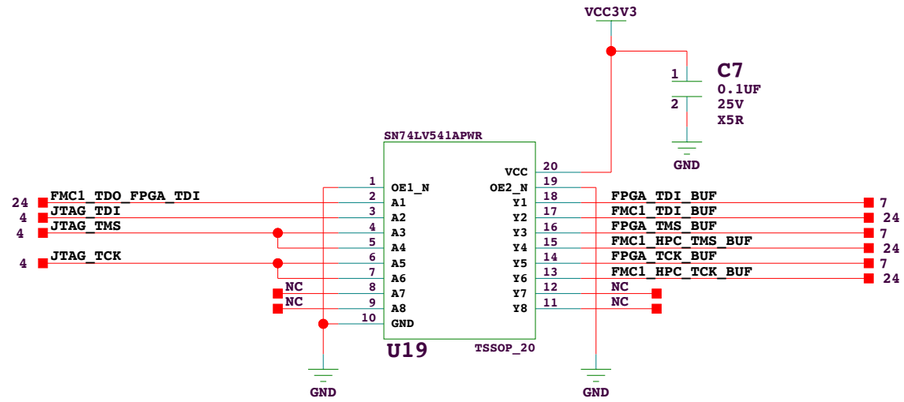
JTAG FLAT-CABLE HEADER

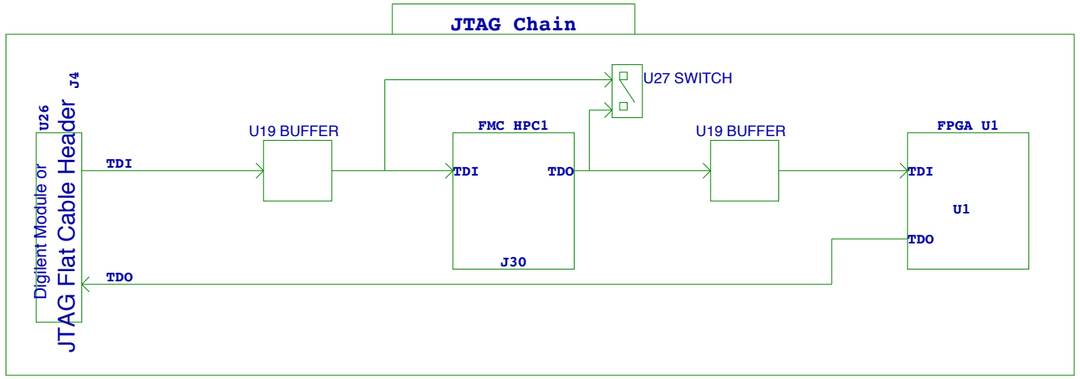


USB JTAG DIGILENT MODULE





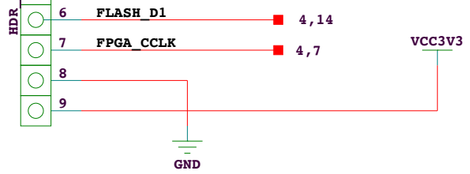
JTAG Chain



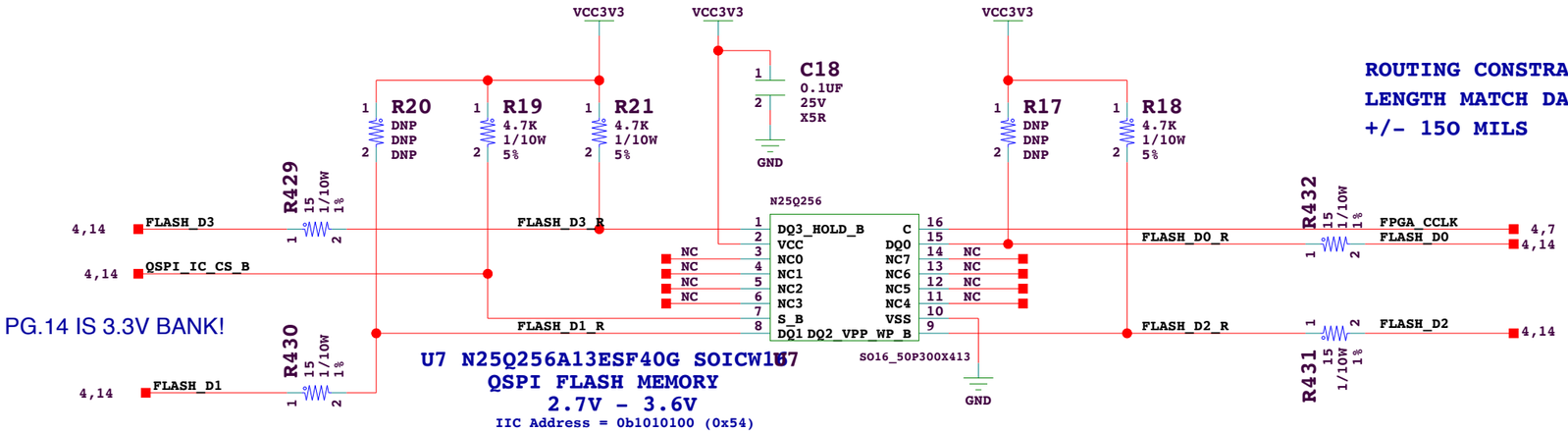
ON = SPI DEVICE

OFF = SPI EXTERNAL

SPI SELECT JUMPER



SPI EXTERNAL
PROGRAMMING HEADER



PG.14 IS 3.3V BANK!

U7 N25Q256A13ESF40G SOICW16
QSPI FLASH MEMORY
2.7V - 3.6V
IIC Address = 0b1010100 (0x54)

ROUTING CONSTRAINT:
LENGTH MATCH DATA AND CLOCK
+/- 150 MILS

FPGA Configuration Options

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Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD CONFIGURATION		
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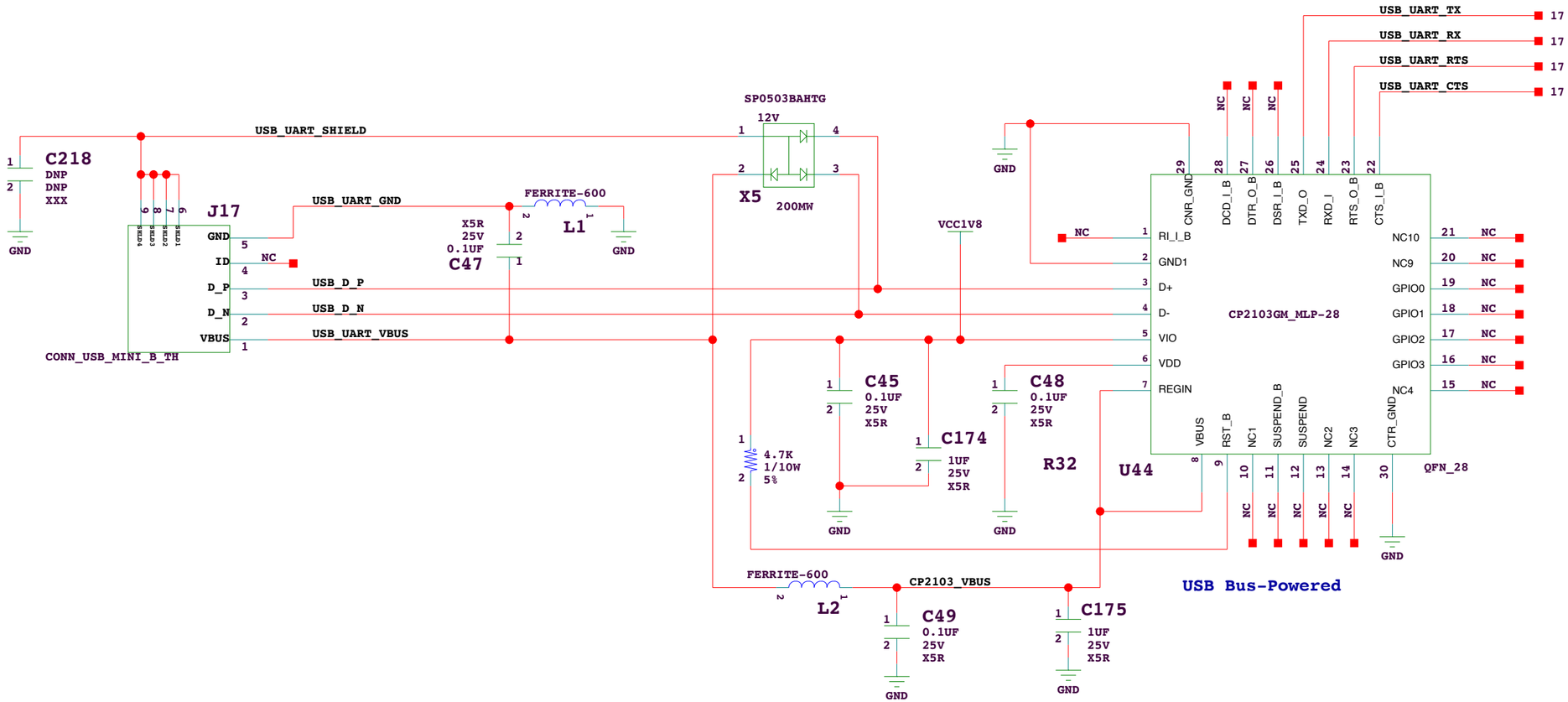

USB UART

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PCB P/N: 1280669
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Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD USB-to-UART BRIDGE	
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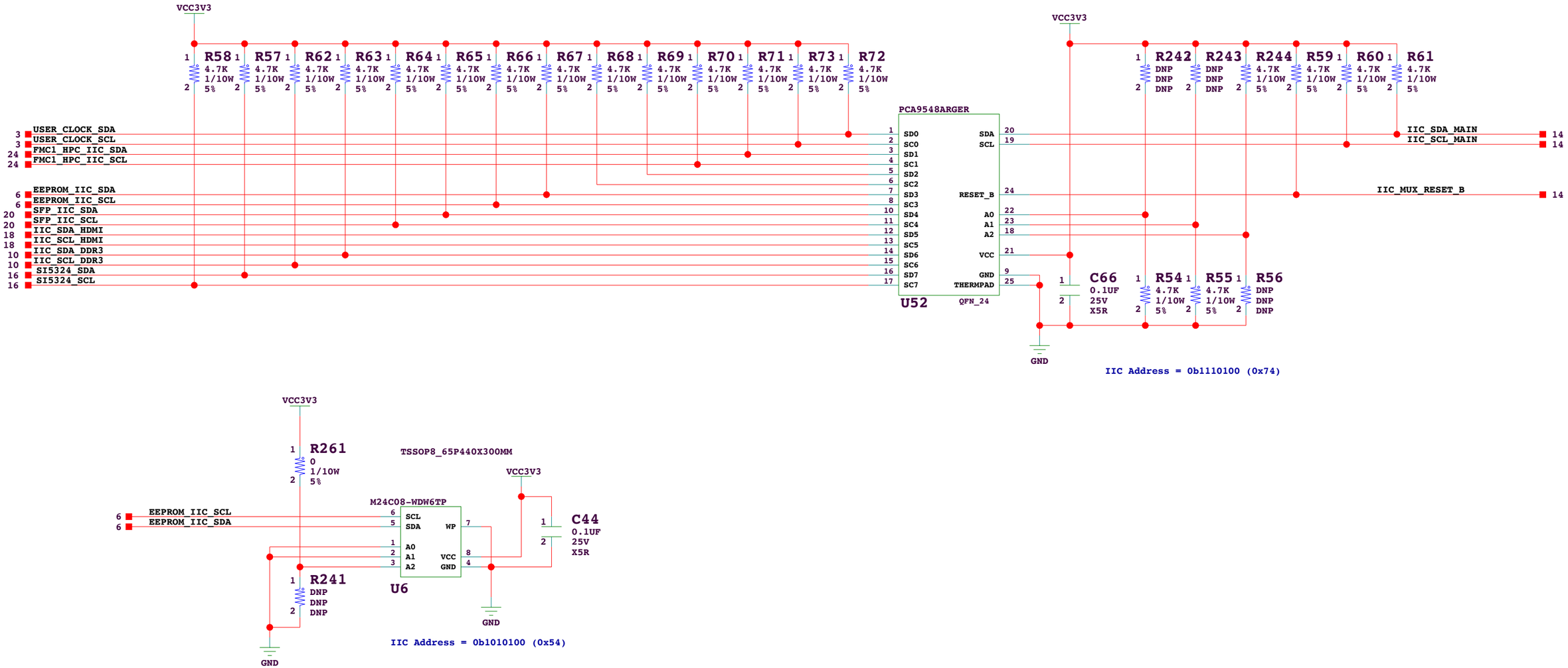

IIC MUX, EEPROM

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TP FOR INT, DONE TIMING MEASUREMENT

SOC_IRON_FG676

BANK 0
XC7A200TFBG676

DXN_0_R11 R11
VCCADC_0_M12 M12
GNDADC_0_M11 M11
DXP_0_R12 R12
VREFN_0_N11 N11
VREFP_0_P12 P12
VP_0_N12 N12
VN_0_P11 P11
VCCBATT_0_G14 G14
CCLK_0_H13 H13
TCK_0_H12 H12
TMS_0_H11 H11
TDO_0_J10 J10
TDI_0_H10 H10
INIT_B_0_V11 V11
PROGRAM_B_0_AE16 AE16
CFGBVS_0_AB15 AB15
DONE_0_W10 W10
M2_0_W9 W9
M0_0_AB7 AB7
M1_0_Y9 Y9

XADC_DXN 29
XADC_VCC 29
XADC_DXP 29
XADC_VREFP 29
XADC_VP_R_P 29
XADC_VN_R_N 29
FPGA_VBATT 7
FPGA_CCLK 4
FPGA_TCK_BUF 4
FPGA_TMS_BUF 4
JTAG_TDO 4
FPGA_TDI_BUF 4
FPGA_INIT_B 7
FPGA_PROG_B 4,7
CFGBVS
FPGA_DONE 7
FPGA_M2 7
FPGA_M0 7
FPGA_M1 7

U1

FPGA_3V3
Y14 VCCO_0_Y14
W11 VCCO_0_W11

HDR_1X2 J52

C1 0.1UF 25V X5R
C2 0.1UF 25V X5R
C163 100UF 6.3 X5R
R233 DNP DNP DNP
C217 DNP DNP XXX

XADC_AGND
GND

FPGA_3V3 R42 4.7K 1/10W 5%
4,7 FPGA_PROG_B
Pushbutton TL3301EF100QG
SW9
GND

FPGA_3V3 R469 4.7K 1/10W 5%
7 FPGA_INIT_B
SN74AVC1T45 U66 SC70_6
VCCB VCCA DIR GND
VCC3V3
R306 261 1/10W 1%
R307 261 1/10W 1%
DS1 RED GRN LED-GRN-RED

VCC3V3 R396 261 1/10W
7 FPGA_DONE
LED-GRN-SMT DS10

D6 BAT40-04 40V 200MW NC
VCC1V5
R83 4.7K 1/10W 5%
7 FPGA_VBATT
B1 1.5V SEIKO TS518FE_FL35E

SW1 SDA03H1SBD NC
R339 1.21K 1/10W 1%
R337 1.21K 1/10W 1%
R338 1.21K 1/10W 1%

Encryption Key Battery B1
FPGA Bank 0, Prog. PB, INIT LED

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PCB P/N: 1280669
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Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK0, PROG.PB,INIT LED		
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SOC_IRON_FG676

BANK 34
XC7A200TFBG676

IO_0_34_N8	N8	DDR3_RESET_B	10
IO_L1P_T0_34_K3	K3	DDR3_A9	10
IO_L1N_T0_34_J3	J3	DDR3_A1	10
IO_L2P_T0_34_M7	M7	DDR3_A5	10
IO_L2N_T0_34_L7	L7	DDR3_A12	10
IO_L3P_T0_DQS_34_M4	M4	DDR3_A0	10
IO_L3N_T0_DQS_34_L4	L4	DDR3_A3	10
IO_L4P_T0_34_L5	L5	DDR3_A11	10
IO_L4N_T0_34_K5	K5	DDR3_A4	10
IO_L5P_T0_34_N7	N7	DDR3_A10	10
IO_L5N_T0_34_N6	N6	DDR3_A13	10
IO_L6P_T0_34_M6	M6	DDR3_A7	10
IO_L6N_T0_VREF_34_M5	M5		
IO_L7P_T1_34_K1	K1	DDR3_A6	10
IO_L7N_T1_34_J1	J1	DDR3_A2	10
IO_L8P_T1_34_L3	L3	DDR3_A14	10
IO_L8N_T1_34_K2	K2	DDR3_A15	10
IO_L9P_T1_DQS_34_N1	N1	DDR3_BA0	10
IO_L9N_T1_DQS_34_M1	M1	DDR3_BA1	10
IO_L10P_T1_34_H2	H2	DDR3_BA2	10
IO_L10N_T1_34_H1	H1	DDR3_A8	10
IO_L11P_T1_SRCC_34_M2	M2	DDR3_CLK0_P	10
IO_L11N_T1_SRCC_34_L2	L2	DDR3_CLK0_N	10
IO_L12P_T1_MRCC_34_N3	N3	DDR3_CLK1_P	10
IO_L12N_T1_MRCC_34_N2	N2	DDR3_CLK1_N	10
IO_L13P_T2_MRCC_34_R3	R3	SYSCLK_P	3
IO_L13N_T2_MRCC_34_P3	P3	SYSCLK_N	3
IO_L14P_T2_SRCC_34_P4	P4	DDR3_CKE0	10
IO_L14N_T2_SRCC_34_N4	N4	DDR3_CKE1	10
IO_L15P_T2_DQS_34_R1	R1	DDR3_WE_B	10
IO_L15N_T2_DQS_34_P1	P1	DDR3_RAS_B	10
IO_L16P_T2_34_T4	T4	DDR3_CAS_B	10
IO_L16N_T2_34_T3	T3	DDR3_S0_B	10
IO_L17P_T2_34_T2	T2	DDR3_S1_B	10
IO_L17N_T2_34_R2	R2	DDR3_ODT0	10
IO_L18P_T2_34_U2	U2	DDR3_ODT1	10
IO_L18N_T2_34_U1	U1	DDR3_TEMP_EVENT	10
IO_L19P_T3_34_P6	P6	GPIO_SW_N	21
IO_L19N_T3_VREF_34_P5	P5		
IO_L20P_T3_34_T5	T5	GPIO_SW_S	21
IO_L20N_T3_34_R5	R5	GPIO_SW_W	21
IO_L21P_T3_DQS_34_U6	U6	GPIO_SW_C	21
IO_L21N_T3_DQS_34_U5	U5	GPIO_SW_E	21
IO_L22P_T3_34_R8	R8	GPIO_DIP_SW0	21
IO_L22N_T3_34_P8	P8	GPIO_DIP_SW1	21
IO_L23P_T3_34_R7	R7	GPIO_DIP_SW2	21
IO_L23N_T3_34_R6	R6	GPIO_DIP_SW3	21
IO_L24P_T3_34_T8	T8	USER_SMA_GPIO_P	3
IO_L24N_T3_34_T7	T7	USER_SMA_GPIO_N	3
IO_25_34_U4	U4	CPU_RESET	21

VTTVREF

C462 (0.1UF, 25V, X5R) — 1: VTTVREF, 2: GND

C491 (0.1UF, 25V, X5R) — 1: VTTVREF, 2: GND

FPGA_1V5

T6	VCCO_34_T6	
P2	VCCO_34_P2	
N5	VCCO_34_N5	
M8	VCCO_34_M8	
L1	VCCO_34_L1	
K4	VCCO_34_K4	

U1

SOC_IRON_FG676

FPGA_1V5

C158 (100UF, 6.3, X5R) — 1: FPGA_1V5, 2: GND

SOC_IRON_FG676

BANK 35
XC7A200TFBG676

IO_0_35_J8	J8	NC	
IO_L1P_T0_AD4P_35_E6	E6	DDR3_D63	10,12
IO_L1N_T0_AD4N_35_D6	D6	DDR3_D62	10,12
IO_L2P_T0_AD12P_35_H8	H8	DDR3_D61	10,12
IO_L2N_T0_AD12N_35_G8	G8	DDR3_D60	10,12
IO_L3P_T0_DQS_AD5P_35_H7	H7	DDR3_DQS7_P	10,12
IO_L3N_T0_DQS_AD5N_35_G7	G7	DDR3_DQS7_N	10,12
IO_L4P_T0_35_F8	F8	DDR3_D59	10,12
IO_L4N_T0_35_F7	F7	DDR3_D58	10,12
IO_L5P_T0_AD13P_35_H6	H6	DDR3_D57	10,12
IO_L5N_T0_AD13N_35_G6	G6	DDR3_D56	10,12
IO_L6P_T0_35_H9	H9	DDR3_DM7	10
IO_L6N_T0_VREF_35_G9	G9		
IO_L7P_T1_AD6P_35_J6	J6	DDR3_D55	
IO_L7N_T1_AD6N_35_J5	J5	DDR3_D54	10,12
IO_L8P_T1_AD14P_35_L8	L8	DDR3_D53	10,12
IO_L8N_T1_AD14N_35_K8	K8	DDR3_D52	10,12
IO_L9P_T1_DQS_AD7P_35_J4	J4	DDR3_DQS6_P	10,12
IO_L9N_T1_DQS_AD7N_35_H4	H4	DDR3_DQS6_N	10,12
IO_L10P_T1_AD15P_35_K7	K7	DDR3_D51	10,12
IO_L10N_T1_AD15N_35_K6	K6	DDR3_D50	10,12
IO_L11P_T1_SRCC_35_G4	G4	DDR3_D49	10,12
IO_L11N_T1_SRCC_35_F4	F4	DDR3_D48	10,12
IO_L12P_T1_MRCC_35_G5	G5	DDR3_DM6	10
IO_L12N_T1_MRCC_35_F5	F5	NC	
IO_L13P_T2_MRCC_35_E5	E5	DDR3_D47	
IO_L13N_T2_MRCC_35_D5	D5	DDR3_D46	10,12
IO_L14P_T2_SRCC_35_D4	D4	DDR3_D45	10,12
IO_L14N_T2_SRCC_35_C4	C4	DDR3_D44	10,12
IO_L15P_T2_DQS_35_B5	B5	DDR3_DQS5_P	10,12
IO_L15N_T2_DQS_35_A5	A5	DDR3_DQS5_N	10,12
IO_L16P_T2_35_B4	B4	DDR3_D43	10,12
IO_L16N_T2_35_A4	A4	DDR3_D42	10,12
IO_L17P_T2_35_D3	D3	DDR3_D41	10,12
IO_L17N_T2_35_C3	C3	DDR3_D40	10,12
IO_L18P_T2_35_F3	F3	DDR3_DM5	10
IO_L18N_T2_35_E3	E3	NC	
IO_L19P_T3_35_C2	C2	DDR3_D39	10,12
IO_L19N_T3_VREF_35_B2	B2		
IO_L20P_T3_35_A3	A3	DDR3_D38	
IO_L20N_T3_35_A2	A2	DDR3_D37	10,12
IO_L21P_T3_DQS_35_C1	C1	DDR3_DQS4_P	10,12
IO_L21N_T3_DQS_35_B1	B1	DDR3_DQS4_N	10,12
IO_L22P_T3_35_F2	F2	DDR3_D36	10,12
IO_L22N_T3_35_E2	E2	DDR3_D35	10,12
IO_L23P_T3_35_E1	E1	DDR3_D34	10,12
IO_L23N_T3_35_D1	D1	DDR3_D33	10,12
IO_L24P_T3_35_G2	G2	DDR3_D32	10,12
IO_L24N_T3_35_G1	G1	DDR3_DM4	10
IO_25_35_H3	H3	NC	

VTTVREF

C463 (0.1UF, 25V, X5R) — 1: VTTVREF, 2: GND

C492 (0.1UF, 25V, X5R) — 1: VTTVREF, 2: GND

FPGA_1V5

J7	VCCO_35_J7	
G3	VCCO_35_G3	
F6	VCCO_35_F6	
D2	VCCO_35_D2	
C5	VCCO_35_C5	
A1	VCCO_35_A1	

U1

SOC_IRON_FG676

FPGA_1V5

C402 (100UF, 6.3, X5R) — 1: FPGA_1V5, 2: GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANKS34,35 DDR3 SODIMM IF		
Date:	2-14-2014_14:52	Ver:	2.0
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XC7A200T-FBG676 ONLY

SOC_IRON_FG676

BANK 33
XC7A200TFBG676

IO_0_33_V4	V4	NC	
IO_L1P_T0_33_V1	V1	DDR3_D31	10,11
IO_L1N_T0_33_W1	W1	DDR3_D30	10,11
IO_L2P_T0_33_W5	W5	DDR3_D29	10,11
IO_L2N_T0_33_W4	W4	DDR3_D28	10,11
IO_L3P_T0_DQS_33_V3	V3	DDR3_DQS3_P	10,11
IO_L3N_T0_DQS_33_V2	V2	DDR3_DQS3_N	10,11
IO_L4P_T0_33_V6	V6	DDR3_D27	10,11
IO_L4N_T0_33_W6	W6	DDR3_D26	10,11
IO_L5P_T0_33_W3	W3	DDR3_D25	10,11
IO_L5N_T0_33_Y3	Y3	DDR3_D24	10,11
IO_L6P_T0_33_U7	U7	DDR3_DM3	10
IO_L6N_T0_VREF_33_V7	V7		
IO_L7P_T1_33_AB1	AB1	DDR3_D23	
IO_L7N_T1_33_AC1	AC1	DDR3_D22	10,11
IO_L8P_T1_33_Y2	Y2	DDR3_D21	10,11
IO_L8N_T1_33_Y1	Y1	DDR3_D20	10,11
IO_L9P_T1_DQS_33_AD1	AD1	DDR3_DQS2_P	10,11
IO_L9N_T1_DQS_33_AE1	AE1	DDR3_DQS2_N	10,11
IO_L10P_T1_33_AE2	AE2	DDR3_D19	10,11
IO_L10N_T1_33_AF2	AF2	DDR3_D18	10,11
IO_L11P_T1_SRCC_33_AB2	AB2	DDR3_D17	10,11
IO_L11N_T1_SRCC_33_AC2	AC2	DDR3_D16	10,11
IO_L12P_T1_MRCC_33_AA3	AA3	DDR3_DM2	10
IO_L12N_T1_MRCC_33_AA2	AA2	NC	
IO_L13P_T2_MRCC_33_AA4	AA4	DDR3_D15	10,11
IO_L13N_T2_MRCC_33_AB4	AB4	DDR3_D14	10,11
IO_L14P_T2_SRCC_33_AC3	AC3	DDR3_D13	10,11
IO_L14N_T2_SRCC_33_AD3	AD3	DDR3_D12	10,11
IO_L15P_T2_DQS_33_AD5	AD5	DDR3_DQS1_P	10,11
IO_L15N_T2_DQS_33_AE5	AE5	DDR3_DQS1_N	10,11
IO_L16P_T2_33_AE3	AE3	DDR3_D11	10,11
IO_L16N_T2_33_AF3	AF3	DDR3_D10	10,11
IO_L17P_T2_33_AF5	AF5	DDR3_D9	10,11
IO_L17N_T2_33_AF4	AF4	DDR3_D8	10,11
IO_L18P_T2_33_AC4	AC4	DDR3_DM1	10
IO_L18N_T2_33_AD4	AD4	NC	
IO_L19P_T3_33_Y7	Y7	DDR3_D7	10,11
IO_L19N_T3_VREF_33_AA7	AA7		
IO_L20P_T3_33_Y6	Y6	DDR3_D6	10,11
IO_L20N_T3_33_Y5	Y5	DDR3_D5	10,11
IO_L21P_T3_DQS_33_V8	V8	DDR3_DQS0_P	10,11
IO_L21N_T3_DQS_33_W8	W8	DDR3_DQS0_N	10,11
IO_L22P_T3_33_AA5	AA5	DDR3_D4	10,11
IO_L22N_T3_33_AB5	AB5	DDR3_D3	10,11
IO_L23P_T3_33_Y8	Y8	DDR3_D2	10,11
IO_L23N_T3_33_AA8	AA8	DDR3_D1	10,11
IO_L24P_T3_33_AB6	AB6	DDR3_D0	10,11
IO_L24N_T3_33_AC6	AC6	DDR3_DM0	10
IO_25_33_V9	V9	NC	

U1

SOC_IRON_FG676

VTTVREF

C461 0.1UF 25V X5R

C490 0.1UF 25V X5R

GND

FPGA_1V5

Y4	VCCO_33_Y4
W7	VCCO_33_W7
U2	VCCO_33_U3
AD2	VCCO_33_AD2
AC5	VCCO_33_AC5
AA1	VCCO_33_AA1

FPGA_1V5

C157 100UF 6.3 X5R

GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
BANK33, DDR3 SODIMM IF

Date:	2-14-2014_14:52	Ver:	2.0
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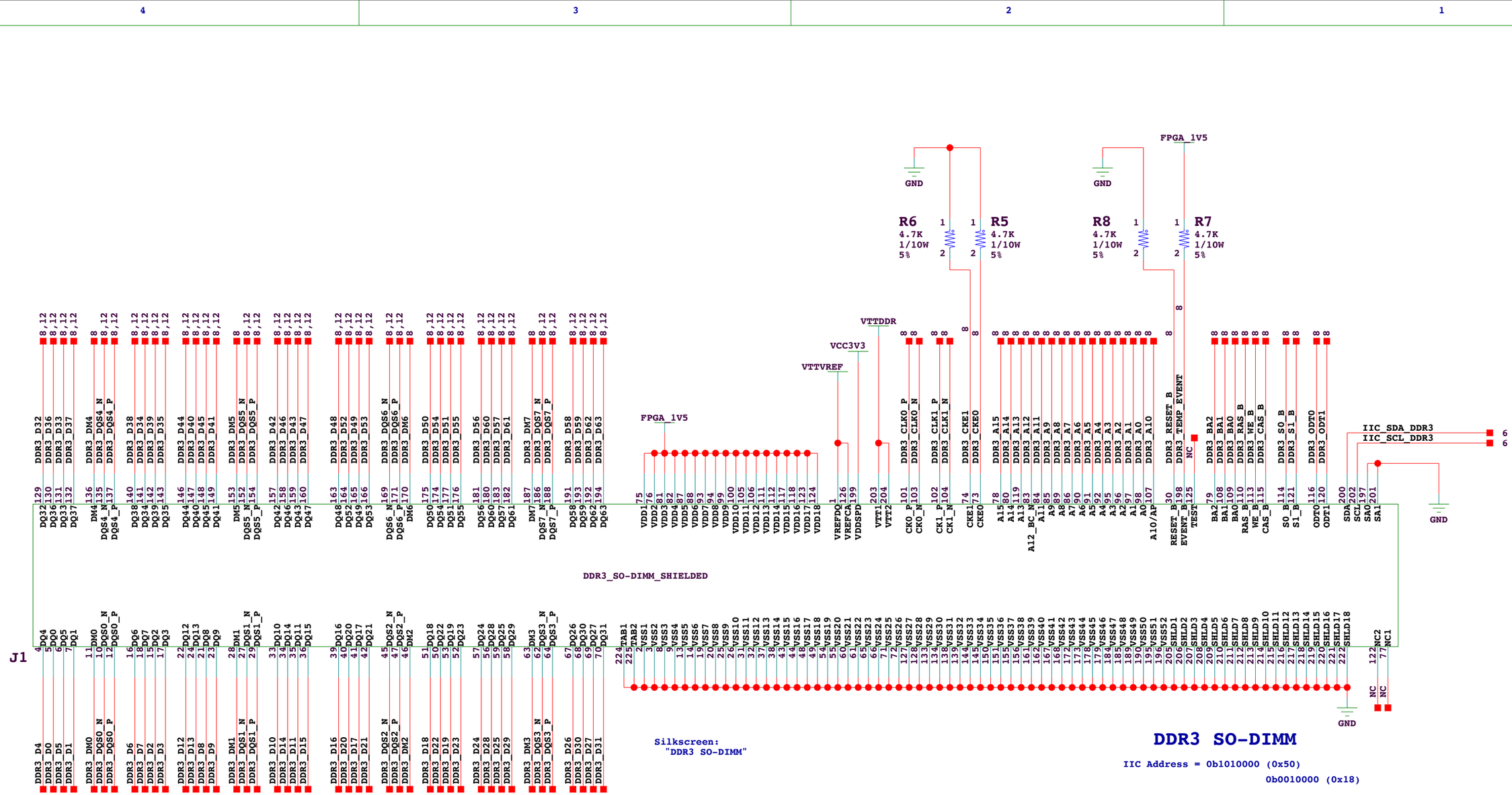

PCB P/N:	1280669
SCH P/N:	0381502
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM SOCKET J1
Date:	2-14-2014_14:52
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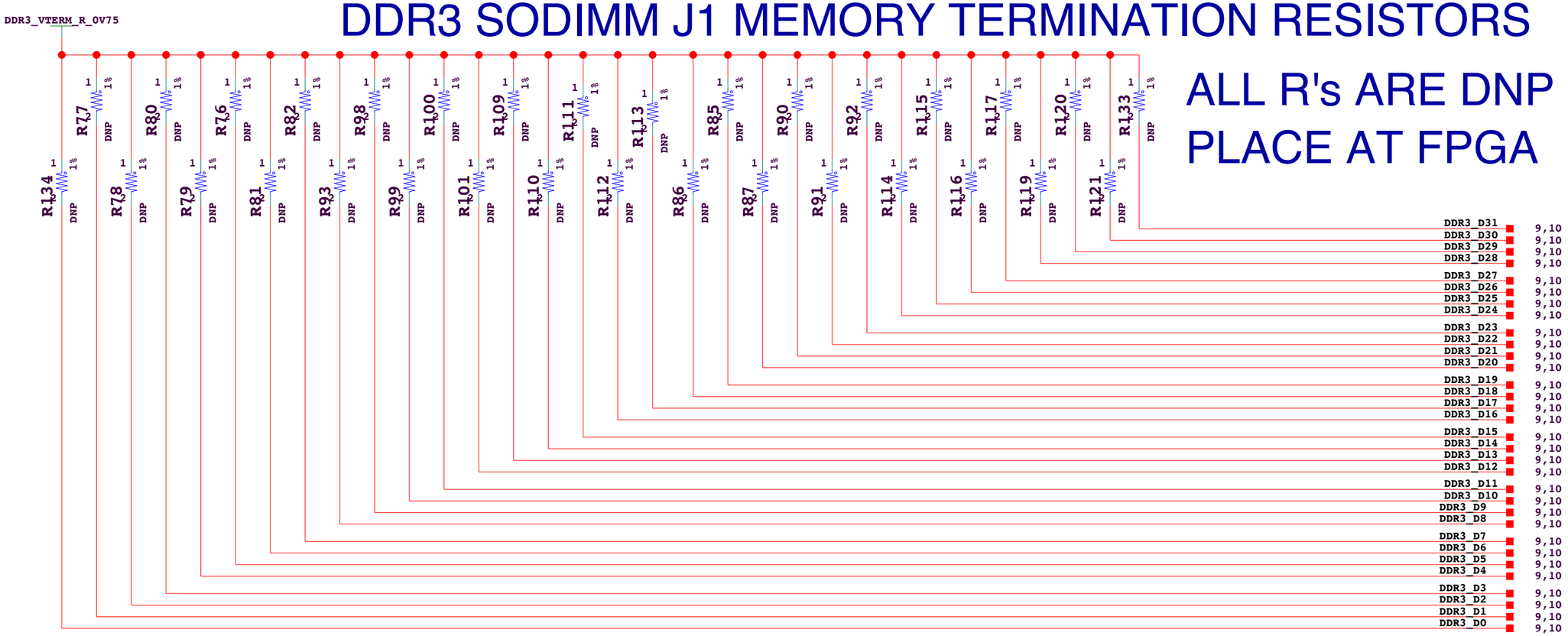
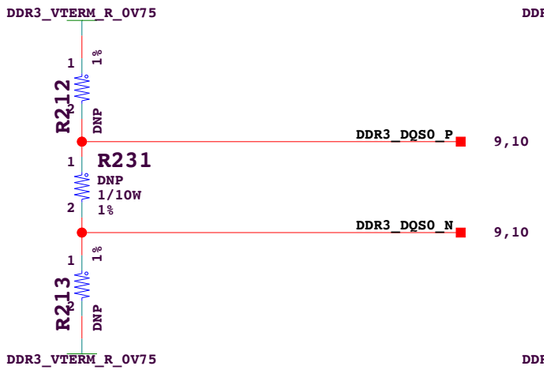
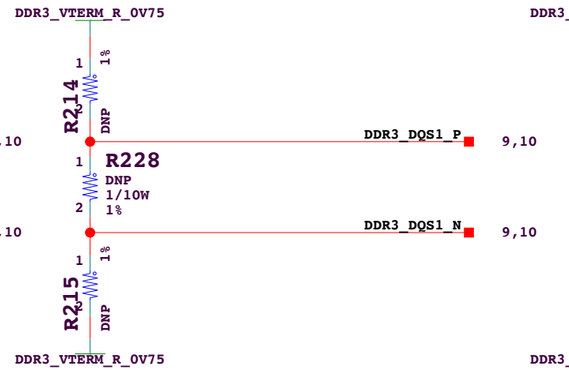
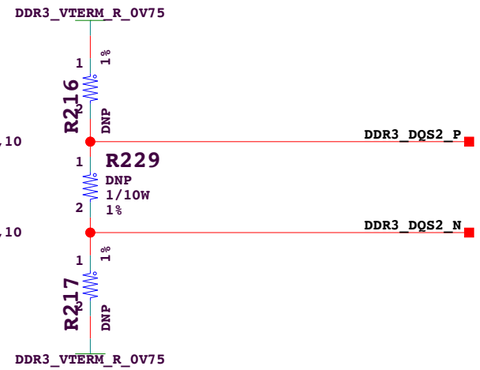
DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

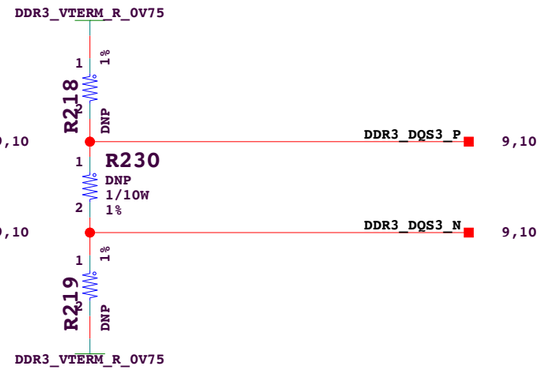
ALL R's ARE DNP
PLACE AT FPGA

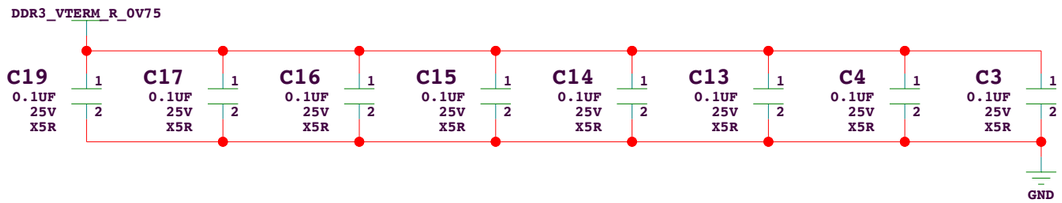












XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS		
Date:	2-14-2014_14:52	Ver:	2.0
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DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

DDR3_VTERM_R_0V75

R139 R144 R135 R146 R175 R172 R173 R174 R159 R155 R161 R163 R164 R168 R169 R170
R136 R142 R143 R145 R171 R176 R177 R178 R157 R158 R160 R162 R182 R181 R180 R179
1 1% DNP

ALL R's ARE DNP
PLACE AT FPGA

DDR3_D63	8,10
DDR3_D62	8,10
DDR3_D61	8,10
DDR3_D60	8,10
DDR3_D59	8,10
DDR3_D58	8,10
DDR3_D57	8,10
DDR3_D56	8,10
DDR3_D55	8,10
DDR3_D54	8,10
DDR3_D53	8,10
DDR3_D52	8,10
DDR3_D51	8,10
DDR3_D50	8,10
DDR3_D49	8,10
DDR3_D48	8,10
DDR3_D47	8,10
DDR3_D46	8,10
DDR3_D45	8,10
DDR3_D44	8,10
DDR3_D43	8,10
DDR3_D42	8,10
DDR3_D41	8,10
DDR3_D40	8,10
DDR3_D39	8,10
DDR3_D38	8,10
DDR3_D37	8,10
DDR3_D36	8,10
DDR3_D35	8,10
DDR3_D34	8,10
DDR3_D33	8,10
DDR3_D32	8,10

DDR3_VTERM_R_0V75

R220 DNP
R237 DNP 1/10W 1%
R221 DNP

DDR3_DQS4_P 8,10
DDR3_DQS4_N 8,10

DDR3_VTERM_R_0V75

R222 DNP
R238 DNP 1/10W 1%
R223 DNP

DDR3_DQS5_P 8,10
DDR3_DQS5_N 8,10

DDR3_VTERM_R_0V75

R224 DNP
R239 DNP 1/10W 1%
R225 DNP

DDR3_DQS6_P 8,10
DDR3_DQS6_N 8,10

DDR3_VTERM_R_0V75

R226 DNP
R240 DNP 1/10W 1%
R227 DNP

DDR3_DQS7_P 8,10
DDR3_DQS7_N 8,10

DDR3_VTERM_R_0V75

C40 C39 C38 C37 C27 C26 C21 C20
0.1UF 25V X5R

GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
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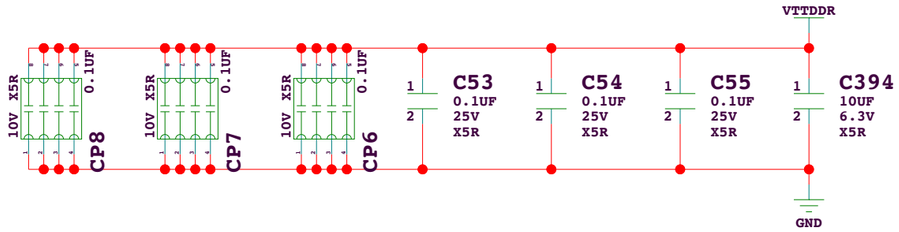
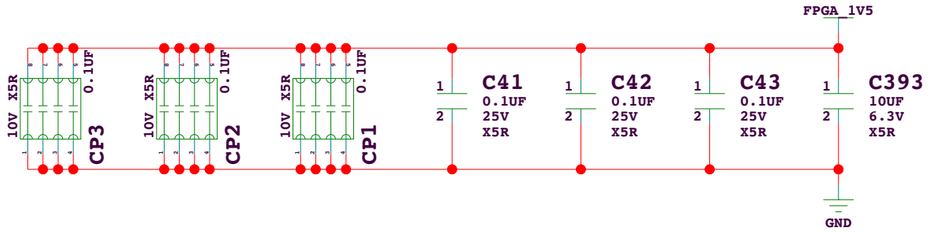
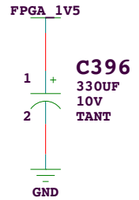
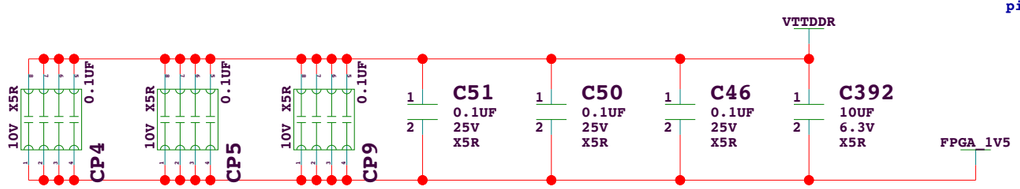
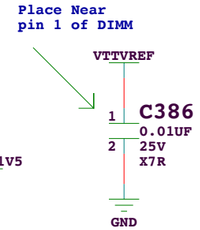
DDR3 SODIMM J1 MEMORY DECOUPLING CAPACITORS

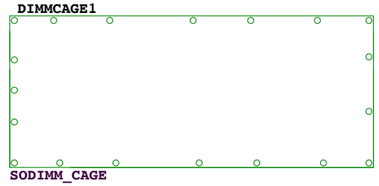












XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM DECOUPLING	
Date:	2-14-2014_14:52	Ver: 2.0
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SOC_IRON_FG676

BANK 14
XC7A200TFBG676

IO_0_14_M19	M19	SI5324_INT_ALM_B	16
IO_L1P_T0_D00_MOSI_14_R14	R14	FLASH_D0	4
IO_L1N_T0_D01_DIN_14_R15	R15	FLASH_D1	4
IO_L2P_T0_D02_14_P14	P14	FLASH_D2	4
IO_L2N_T0_D03_14_N14	N14	FLASH_D3	4
IO_L3P_T0_DQS_PUDC_B_14_P15	P15	CTRL2_PWRGOOD	24,39,45
IO_L3N_T0_DQS_EMCCLK_14_P16	P16	FPGA_EMCCLK	3
IO_L4P_T0_D04_14_N16	N16	FMC1_HPC_PRSNT_M2C_B	24,26
IO_L4N_T0_D05_14_N17	N17	FMC1_HPC_PG_M2C	25
IO_L5P_T0_D06_14_R16	R16	FMC_VADJ_ON_B	45
IO_L5N_T0_D07_14_R17	R17	IIC_MUX_RESET_B	6
IO_L6P_T0_FCS_B_14_P18	P18	QSPI_IC_CS_B	4
IO_L6N_T0_D08_VREF_14_N18	N18	IIC_SCL_MAIN	6
IO_L7P_T1_D09_14_K25	K25	IIC_SDA_MAIN	6
IO_L7N_T1_D10_14_K26	K26	PCIE_WAKE_B	28
IO_L8P_T1_D11_14_M20	M20	PCIE_PERST	28
IO_L8N_T1_D12_14_L20	L20	LCD_E_LS	14
IO_L9P_T1_DQS_14_L24	L24	LCD_RW_LS	14
IO_L9N_T1_DQS_D13_14_L25	L25	LCD_DB4_LS	14
IO_L10P_T1_D14_14_M24	M24	LCD_DB5_LS	14
IO_L10N_T1_D15_14_M25	M25	LCD_DB6_LS	14
IO_L11P_T1_SRCC_14_L22	L22	LCD_DB7_LS	14
IO_L11N_T1_SRCC_14_L23	L23	LCD_RS_LS	14
IO_L12P_T1_MRCC_14_M21	M21	USER_CLOCK_P	3
IO_L12N_T1_MRCC_14_M22	M22	USER_CLOCK_N	3
IO_L13P_T2_MRCC_14_N21	N21	ROTARY_PUSH	21
IO_L13N_T2_MRCC_14_N22	N22	ROTARY_INCA	21
IO_L14P_T2_SRCC_14_P20	P20	ROTARY_INCB	21
IO_L14N_T2_SRCC_14_P21	P21	SDIO_CD_DAT3	14
IO_L15P_T2_DQS_RDWR_B_14_N23	N23	SDIO_CMD	14
IO_L15N_T2_DQSOUT_CSO_B_14_N24	N24	SDIO_CLK	14
IO_L16P_T2_CSI_B_14_P19	P19	SDIO_DAT0	14
IO_L16N_T2_A15_D31_14_N19	N19	SDIO_DAT1	14
IO_L17P_T2_A14_D30_14_P23	P23	SDIO_DAT2	14
IO_L17N_T2_A13_D29_14_P24	P24	SDIO_SDDET	14
IO_L18P_T2_A12_D28_14_R20	R20	SDIO_SDWP	14
IO_L18N_T2_A11_D27_14_R21	R21	PMBUS_CLK_LS	14
IO_L19P_T3_A10_D26_14_R25	R25	PMBUS_DATA_LS	14
IO_L19N_T3_A09_D25_VREF_14_P25	P25	PMBUS_CTRL_LS	14
IO_L20P_T3_A08_D24_14_N26	N26	PMBUS_ALERT_LS	14
IO_L20N_T3_A07_D23_14_M26	M26	GPIO_LED_0	21
IO_L21P_T3_DQS_14_T24	T24	GPIO_LED_1	21
IO_L21N_T3_DQS_A06_D22_14_T25	T25	GPIO_LED_2	21
IO_L22P_T3_A05_D21_14_R26	R26	GPIO_LED_3	21
IO_L22N_T3_A04_D20_14_P26	P26	PMOD_0	21
IO_L23P_T3_A03_D19_14_T22	T22	PMOD_1	21
IO_L23N_T3_A02_D18_14_R22	R22	PMOD_2	21
IO_L24P_T3_A01_D17_14_T23	T23	PMOD_3	21
IO_L24N_T3_A00_D16_14_R23	R23	SFP_LOS	20
IO_25_14_R18	R18	SFP_TX_DISABLE	20

FPGA_3V3

R19	VCCO_14_R19
P22	VCCO_14_P22
N25	VCCO_14_N25
N15	VCCO_14_N15
L21	VCCO_14_L21
K24	VCCO_14_K24

U1

SOC_IRON_FG676

PWRCTL1_VCC4B_PG
CTRL2_PWRGOOD from TI controller U9 indicates both VCC3V3 and VCCO_VADJ FMC power rails are OK

VCC5V0

J23 HDR_2X7

14 LCD_DB7	1	2	LCD_DB6 14
14 LCD_DB5	3	4	LCD_DB4 14
NC	5	6	NC
NC	7	8	NC
14 LCD_E	9	10	LCD_RW 14
14 LCD_RS	11	12	LCD_VEE
	13	14	

GND

6.81K 1/10W 1%
R118
LCD Contrast Pot
R232 2K 1/2W 20% POT_3352W

VCC5V0

GND

FPGA_3V3

C473 0.1UF 25V X5R

VCC5V0

C472 0.1UF 25V X5R

GND

TXS0108E U45 TSSOP_20

14 LCD_E_LS	2 VCCA	VCCB 19	LCD_E 14
14 LCD_RW_LS	1 A1	B1 20	LCD_RW 14
14 LCD_DB4_LS	3 A2	B2 18	LCD_DB4 14
14 LCD_DB5_LS	4 A3	B3 17	LCD_DB5 14
14 LCD_DB6_LS	5 A4	B4 16	LCD_DB6 14
14 LCD_DB7_LS	6 A5	B5 15	LCD_DB7 14
14 LCD_RS_LS	7 A6	B6 14	LCD_RS 14
NC	8 A7	B7 13	
	9 A8	B8 12	NC
	10 OE	GND 11	

GND

VCC3V3

PMBUS Isolation

R313 2.00K
R315 2.00K
R314 2.00K
R316 2.00K

Q14 NDS331N			
38,39,45 PMBUS_CLK	3	2	PMBUS_CLK_LS 14
Q15 NDS331N			
38,39,45 PMBUS_DATA	3	2	PMBUS_DATA_LS 14
Q19 NDS331N			
38,39 PMBUS_CTRL	3	2	PMBUS_CTRL_LS 14
Q20 NDS331N			
38,39,45 PMBUS_ALERT	3	2	PMBUS_ALERT_LS 14

FPGA_3V3

C155 100UF 6.3 X5R

GND

VCC3V3

C52 0.1UF 25V X5R

GND

R325 R322 R323 R324 R319 R321 R318 R317 51.1K1%

SD Card Connector
67840-8001 U29

14 SDIO_CD_DAT3	1 CD_DAT3	IOGND2 18	
14 SDIO_CMD	2 CMD	IOGND1 17	
	3 VSS1	GNDTAB4 16	
14 SDIO_CLK	4 VDD	GNDTAB3 15	
	5 CLK	GNDTAB2 14	
14 SDIO_DAT0	6 VSS2	GNDTAB1 13	
14 SDIO_DAT1	7 DAT0		
14 SDIO_DAT2	8 DAT1		
	9 DAT2		
14 SDIO_SDDET	10 DETECT		
14 SDIO_SDWP	11 PROTECT		
	12 DETECT_PROTECT		

GND GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD GPIO BANK14, SD SOCKET, LCD IF
Date: 2-14-2014_14:52	Ver: 2.0
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CONFIGURATION MAPPING

PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=1	RGMII_RX=0
	EPHY_LED1	RGMII_TX=0	RGMII_RX=1
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1

GEM / MDIO - POWER & DECOUPLING

VCC1V8 — L12 (FERRITE-220) — VCC1V8_FILT

MAGNETICS / RJ45

VCC1V8_FILT: C400 4.7UF 10V; C90 0.1UF 25V → GND

AVDDX, AVDDR, AVDDC

VCC1V8_FILT: C398 4.7UF 10V; C86, C87, C85, C84, C88, C83 0.1UF 25V → GND

AVDD

VCC1V8_FILT: C397 4.7UF 10V; C81, C82, C80, C79, C89, C64 0.1UF 25V → GND

VDDO, VDDOR

VCC1V8: C403 4.7UF 10V; C98, C99, C97, C96, C100 0.1UF 25V → GND

J35 HDR_1X3: 1 → VCC1V8; 2 → R274 1.00K 1/16W → VCC1V8; 3 → GND

J37 HDR_1X3: 1 → PHY_LED1 15; 2 → VCC1V8; 3 → PHY_LED0 15

J36 HDR_1X3: 1 → VCC1V8; 2; 3 → PHY_LED0 15

2 → J35, J37, J36

J5 HDR_1X2: 1 → R271 1.00K 1/16W → GND; 2 → VCC1V8

R2 4.7K 1/10W: 1 → VCC1V8; 2 → PHY_MDIO

88E1116R (QFN_64) — U12

17	PHY_MDIO	45	MDIO	MGMT
17	PHY_MDC	48	MDC	
15,17	PHY_TX_CLK	60	TX_CLK	RGMII
15,17	PHY_TX_CTRL	63	TX_CTRL	
15,17	PHY_TXD3	62	TXD3	
15,17	PHY_TXD2	61	TXD2	
15,17	PHY_TXD1	59	TXD1	
15,17	PHY_TXD0	58	TXD0	
17	PHY_RX_CLK	53	RX_CLK	
17	PHY_RX_CTRL	49	RX_CTRL	
17	PHY_RXD3	55	RXD3	
17	PHY_RXD2	54	RXD2	
17	PHY_RXD1	51	RXD1	
17	PHY_RXD0	50	RXD0	
	PHY_CONFIG3	3	CONFIG3	
	PHY_CONFIG2	2	CONFIG2	
	PHY_LED0	1	CONFIG1	
15		64	CONFIG0	
15	PHY_XTAL_IN	38	XTAL_IN	
15	PHY_XTAL_OUT	39	XTAL_OUT	
		4	COMA_B	
	PHY_VREF	57	VREF	
17	PHY_RESET_B	10	RESET_B	

VCC1V8 → R272 1.00K 1/16W → PHY_VREF; VCC1V8 → R273 1.00K 1/16W → GND

MDI: MDIO_P/N, MDI1_P/N, MDI2_P/N, MDI3_P/N

MDIO_P	31	PHY_MDIO_P
MDIO_N	30	PHY_MDIO_N
MDI1_P	26	PHY_MDI1_P
MDI1_N	25	PHY_MDI1_N
MDI2_P	24	PHY_MDI2_P
MDI2_N	23	PHY_MDI2_N
MDI3_P	20	PHY_MDI3_P
MDI3_N	19	PHY_MDI3_N
RSET	33	PHY_RSET
CTRL18	17	NC
DIS_REG12	12	
LED0	6	PHY_LED0 15
LED1	8	PHY_LED1 15
LED2	9	PHY_LED2 15
TEST: HSDAC_P	36	PHY_HSDAC_P
HSDAC_N	35	PHY_HSDAC_N
TSTPT	32	NC
	11	PHY_TRST_B
JTAG: TCK	42	NC
TMS	41	NC
TDI	43	NC
TDO	44	NC

R291 4.99K 1/10W: 1 → PHY_LED0; 2 → GND

R1 4.7K 1/10W: 1 → PHY_TRST_B; 2 → GND

R3, R10 DNP 2 PLACES: 1 → PHY_HSDAC_P; 2 → PHY_HSDAC_N

J24 DNP: 1 → PHY_TRST_B; 2 → GND

VCC1V8_FILT: C56 0.1UF 25V; C395 1000PF 50V X7R → GND

RJ45 P4 — 10/100/1000 RJ45 AND MAGNETICS

1	TDO_P	PHY_MDIO_P	
2	TDO_N	PHY_MDIO_N	
3	TD1_P	PHY_MDI1_P	
6	TD1_N	PHY_MDI1_N	
4	TD2_P	PHY_MDI2_P	
5	TD2_N	PHY_MDI2_N	
7	TD3_P	PHY_MDI3_P	
8	TD3_N	PHY_MDI3_N	
9	VCC		
10	GND		
SH2	SH2		
SH1	SH1		

L11 FERRITE-220

VCC1V8 → R448, R449, R447, R445, R443, R438; R450, R451, R446, R444, R442, R441 100 1/10W 1% → GND

15,17	PHY_TX_CLK
15,17	PHY_TX_CTRL
15,17	PHY_TXD3
15,17	PHY_TXD2
15,17	PHY_TXD1
15,17	PHY_TXD0

VCC3V3 → R281, R280, R279 261 1/10W → LED-GRN-SMT DS13, DS12, DS11 → NDS331N Q4, Q3, Q1 → GND

15	PHY_LED0
15	PHY_LED1
15	PHY_LED2

25.00MHZ 50PPM — X1: NC 3, NC 2, 4, 1 → PHY_XTAL_OUT 15; PHY_XTAL_IN 15

R275 DNP; C405, C406 18PF 50V NPO 2 PLACES → GND

PHY POWER SYMBOL & CAPS MOVED TO PG. 16

1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESITORS ON HSDAC_P AND HSDAC_N.

2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

GEM / MDIO

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD 10/100/1000 PHY		
Date:	2-14-2014_14:52	Ver:	2.0
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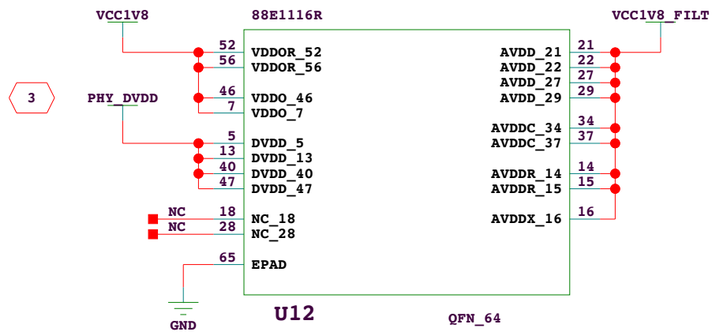
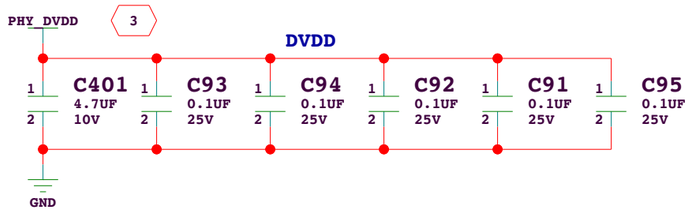
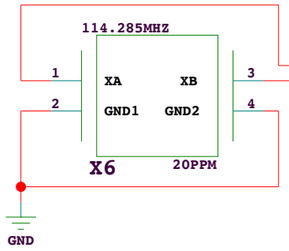
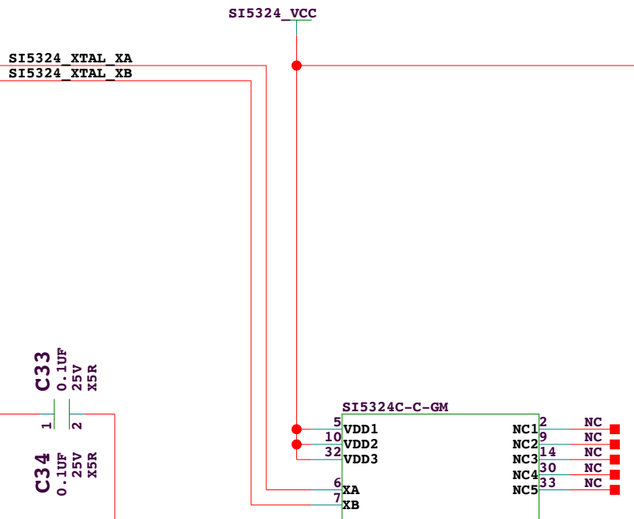




3 DVDD 1.2V IS SUPPLIED INTERNALLY. DVDD PINS 5,13,40,47 ARE FOR EXTERNAL CAPS





5324 Clock Recovery

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SI5324 CLOCK RECOVERY		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
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SOC_IRON_FG676

BANK 13
XC7A200TFBG676

IO_0_13_U24	U24	HDMI_R_D21	19
IO_L1P_T0_13_U25	U25	HDMI_R_D16	19
IO_L1N_T0_13_U26	U26	HDMI_R_D11	19
IO_L2P_T0_13_V26	V26	HDMI_R_D7	19
IO_L2N_T0_13_W26	W26	HDMI_R_D8	19
IO_L3P_T0_DQS_13_AB26	AB26	HDMI_R_DE	19
IO_L3N_T0_DQS_13_AC26	AC26	HDMI_R_VSYNC	19
IO_L4P_T0_13_W25	W25	HDMI_R_D9	19
IO_L4N_T0_13_Y26	Y26	HDMI_R_D6	19
IO_L5P_T0_13_Y25	Y25	HDMI_R_D5	19
IO_L5N_T0_13_AA25	AA25	HDMI_R_D29	19
IO_L6P_T0_13_V24	V24	HDMI_R_D17	19
IO_L6N_T0_VREF_13_W24	W24	HDMI_R_D10	19
IO_L7P_T1_13_AA24	AA24	HDMI_R_D4	19
IO_L7N_T1_13_AB25	AB25	HDMI_R_D30	19
IO_L8P_T1_13_AA22	AA22	HDMI_R_HSYNC	19
IO_L8N_T1_13_AA23	AA23	HDMI_R_D28	19
IO_L9P_T1_DQS_13_AB24	AB24	HDMI_R_D32	19
IO_L9N_T1_DQS_13_AC24	AC24	HDMI_R_D31	19
IO_L10P_T1_13_V23	V23	HDMI_R_D23	19
IO_L10N_T1_13_W23	W23	HDMI_R_D19	19
IO_L11P_T1_SRCC_13_Y22	Y22	HDMI_R_D33	19
IO_L11N_T1_SRCC_13_Y23	Y23	HDMI_R_D34	19
IO_L12P_T1_MRCC_13_U22	U22	PHY_TX_CLK	15
IO_L12N_T1_MRCC_13_V22	V22	HDMI_R_D35	19
IO_L13P_T2_MRCC_13_U21	U21	PHY_RX_CLK	15
IO_L13N_T2_MRCC_13_V21	V21	HDMI_R_CLK	19
IO_L14P_T2_SRCC_13_W21	W21	HDMI_INT	18
IO_L14N_T2_SRCC_13_Y21	Y21	HDMI_R_SPDIF	19
IO_L15P_T2_DQS_13_T20	T20	HDMI_SPDIF_OUT_LS	17
IO_L15N_T2_DQS_13_U20	U20	HDMI_R_D18	19
IO_L16P_T2_13_W20	W20	HDMI_R_D20	19
IO_L16N_T2_13_Y20	Y20	HDMI_R_D22	19
IO_L17P_T2_13_T19	T19	USB_UART_TX	5
IO_L17N_T2_13_U19	U19	USB_UART_RX	5
IO_L18P_T2_13_V19	V19	USB_UART_RTS	5
IO_L18N_T2_13_W19	W19	USB_UART_CTS	5
IO_L19P_T3_13_V18	V18	PHY_RESET_B	15
IO_L19N_T3_VREF_13_W18	W18	PHY_MDC	15
IO_L20P_T3_13_T14	T14	PHY_MDIO	15
IO_L20N_T3_13_T15	T15	PHY_TX_CTRL	15
IO_L21P_T3_DQS_13_T17	T17	PHY_TXD3	15
IO_L21N_T3_DQS_13_T18	T18	PHY_TXD2	15
IO_L22P_T3_13_U15	U15	PHY_TXD1	15
IO_L22N_T3_13_U16	U16	PHY_TXD0	15
IO_L23P_T3_13_U14	U14	PHY_RX_CTRL	15
IO_L23N_T3_13_V14	V14	PHY_RXD3	15
IO_L24P_T3_13_V16	V16	PHY_RXD2	15
IO_L24N_T3_13_V17	V17	PHY_RXD1	15
IO_25_13_U17	U17	PHY_RXD0	15

FPGA_1V8

Y24	VCCO_13_Y24
V20	VCCO_13_V20
U23	VCCO_13_U23
T26	VCCO_13_T26
T16	VCCO_13_T16
AC25	VCCO_13_AC25

U1

SOC_IRON_FG676

FPGA_1V8

C60
0.1UF
25V
X5R

GND

VCC3V3

C59
0.1UF
25V
X5R

GND

SN74AVC1T45

1	VCCA	VCCB	6
17 HDMI_SPDIF_OUT_LS	3 A	B 4	HDMI_SPDIF_OUT 18
2	GND	DIR	5

SC70_6

U38

GND

GND

FPGA_1V8

C156
100UF
6.3
X5R

GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK13 HDIM/EPHY IF		
Date:	2-14-2014_14:52	Ver:	2.0
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IIC Address = 0b0111001 (0x39)

VCC3V3
VCC1V8

R104 2.43K 1/10W 1%
R105 2.43K 1/10W 1%
R106 2.43K 1/10W 1%

HDMI_INT
IIC_SCL_HDMI
IIC_SDA_HDMI
HDMI_VSYNC
HDMI_HSYNC
HDMI_CLK
HDMI_HEAC_C_N
HDMI_D35 HDMI_D34 HDMI_D33 HDMI_D32 HDMI_D31 HDMI_D30 HDMI_D29 HDMI_D28
NC NC NC NC
HDMI_D23 HDMI_D22 HDMI_D21 HDMI_D20 HDMI_D19 HDMI_D18 HDMI_D17 HDMI_D16
NC NC NC NC
HDMI_D11 HDMI_D10 HDMI_D9 HDMI_D8 HDMI_D7 HDMI_D6 HDMI_D5 HDMI_D4
NC NC NC NC
HDMI_DE
HDMI_SPDIF

INT PD SCL SDA VSYNC HSYNC CLK HPD D35 D34 D33 D32 D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 DE SPDIF

GND

HDMI_D0_P HDMI_D0_N HDMI_D1_P HDMI_D1_N HDMI_D2_P HDMI_D2_N HDMI_CLK_P HDMI_CLK_N
HDMI_DDCSDA HDMI_DDCSCL HDMI_HEAC_P HDMI_HEAC_N HDMI_CEC

To HDMI Connector

TX0_P TX0_N TX1_P TX1_N TX2_P TX2_N TXC_P TXC_N DDCSDA DDCSCL HEAC_P HEAC_N CEC

CEC_CLK HDMI_CEC_12MHZ_CLK
SPDIF_OUT HDMI_SPDIF_OUT

PVDD1 PVDD2 PVDD3 HDMI_PLVDD HDMI_AVDD
AVDD1 AVDD2 AVDD3 HDMI_AVDD
DVDD1 DVDD2 DVDD3 DVDD4 DVDD5 HDMI_DVDD
DVDD_3V HDMI_DVDD_3V
BGVDD HDMI_PLVDD
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND

ADV7511

U48

LQFP100_14X14

DSD0 DSD1 DSD2 DSD3 DSD4 DSD5 DSD_CLK MCLK I2S0 I2S1 I2S2 I2S3 SCLK LRCLK R_EXT

R102 887 1/10W 1%

GND

VCC2V5

SIT8102
VCC OE OUT GND
U41 12.00000MHZ 50PPM

C78 0.1UF 25V X5R

GND

HDMI_DVDD_3V

C201 0.01UF 25V X7R
C67 0.1UF 25V X5R
C336 10UF 16V X5R
FERRITE-220 L13

VCC3V3

GND

HDMI_DVDD

C206 0.01UF 25V X7R
C72 0.1UF 25V X5R
C205 0.01UF 25V X7R
C71 0.1UF 25V X5R
C204 0.01UF 25V X7R
C70 0.1UF 25V X5R
C202 0.01UF 25V X7R
C68 0.1UF 25V X5R
C337 10UF 16V X5R
FERRITE-220 L14

VCC1V8

GND

HDMI_PLVDD

C208 0.01UF 25V X7R
C74 0.1UF 25V X5R
C207 0.01UF 25V X7R
C73 0.1UF 25V X5R
C203 0.01UF 25V X7R
C69 0.1UF 25V X5R
C338 10UF 16V X5R
FERRITE-220 L15

VCC1V8

GND

HDMI_AVDD

C210 0.01UF 25V X7R
C76 0.1UF 25V X5R
C211 0.01UF 25V X7R
C77 0.1UF 25V X5R
C209 0.01UF 25V X7R
C75 0.1UF 25V X5R
C339 10UF 16V X5R
FERRITE-220 L16

VCC1V8

GND

ADV7511 HDMI CODEC

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD ADV7511 HDMI CODEC		
Date:	2-14-2014_14:52	Ver:	2.0
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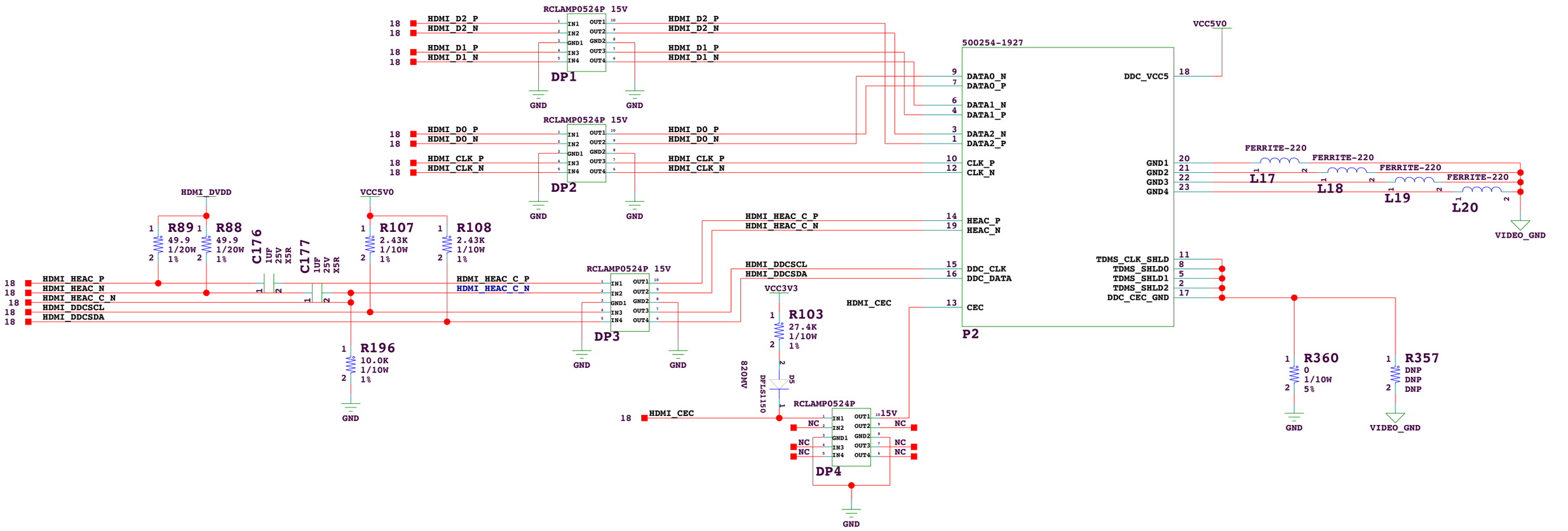
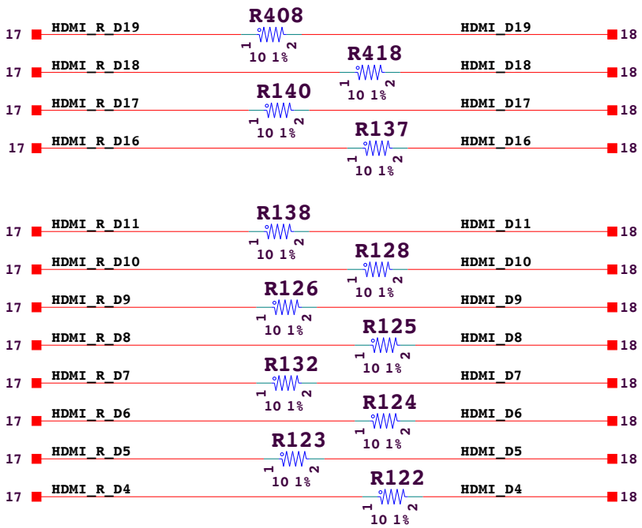
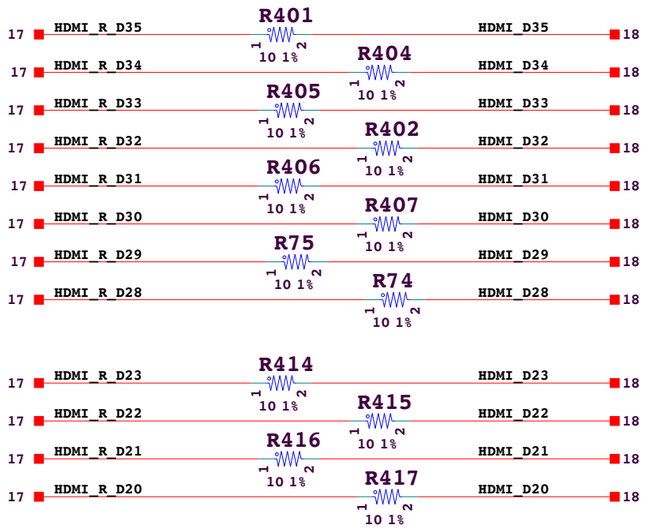
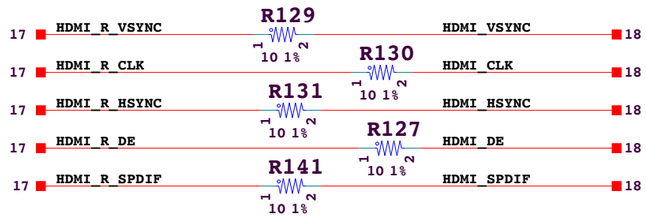


Place series Rs at FPGA







HDMI CONNECTOR

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD HDMI CONN. P2, HDMI SERIES R's		
Date:	2-14-2014_14:52	Ver:	2.0
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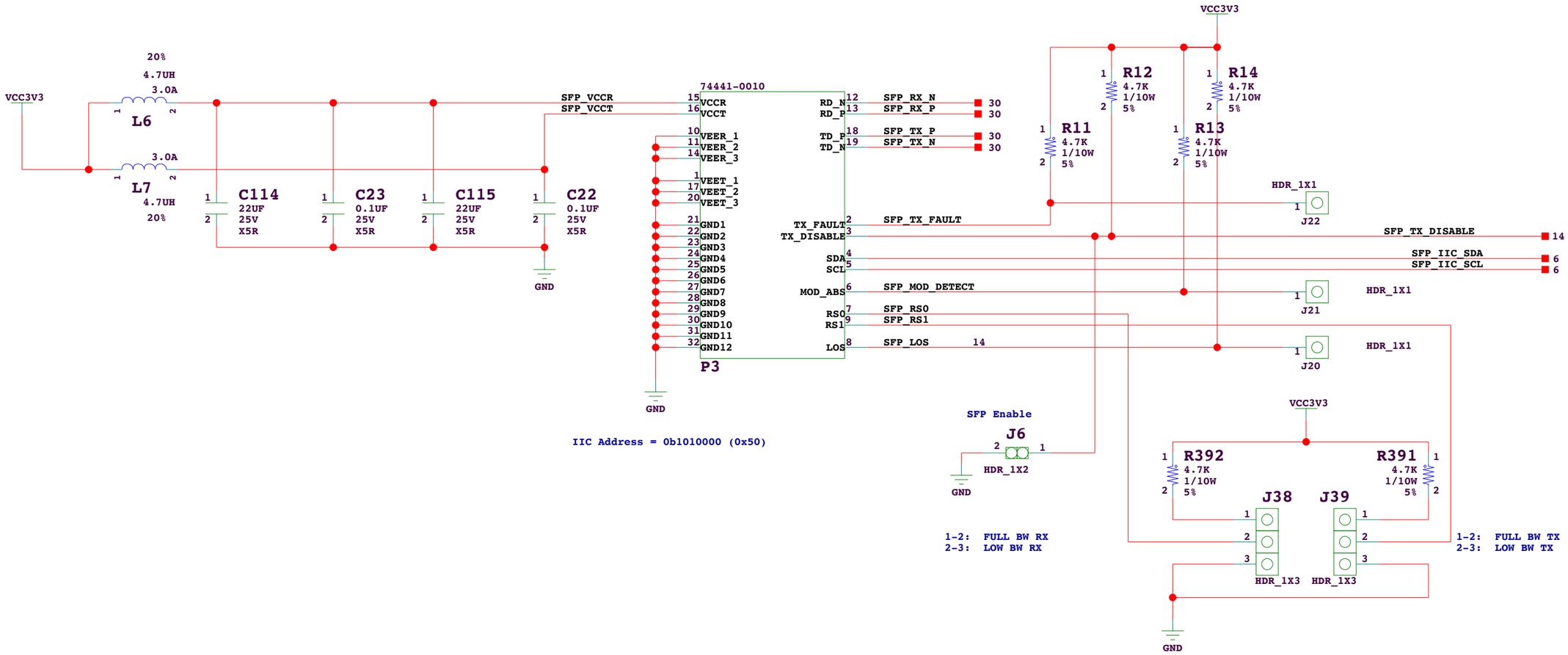

SFP+ Connector and Cage

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SFP+ CONN. P3		
Date:	2-14-2014_14:52	Ver:	2.0
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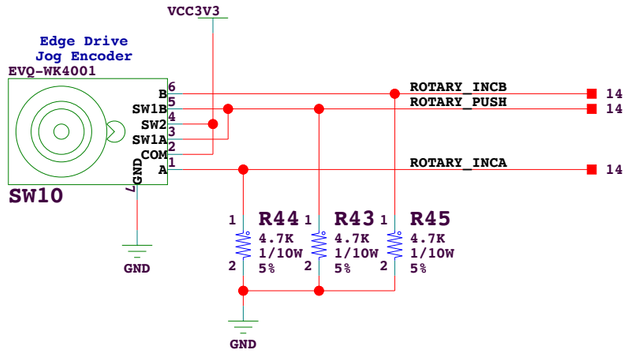
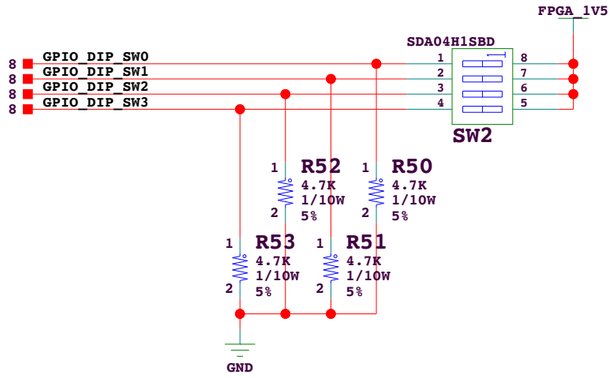
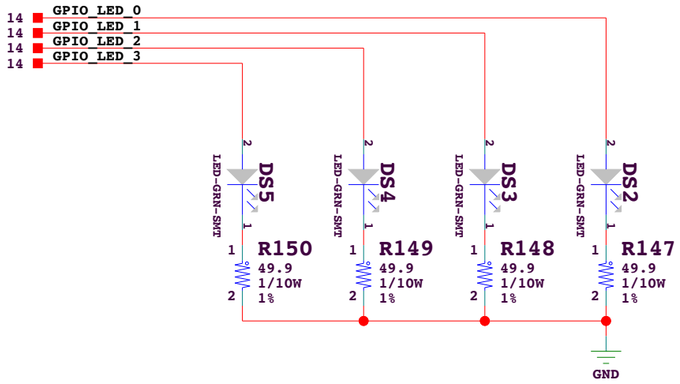
Rotary Switch

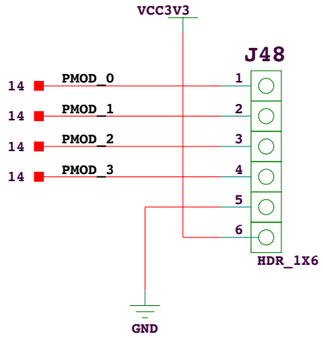


4-Pole DIP Switch

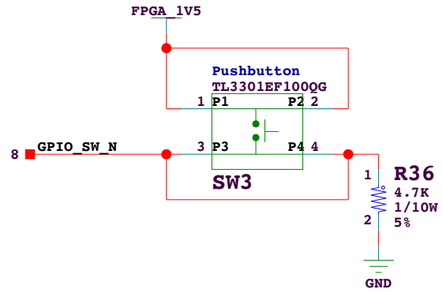


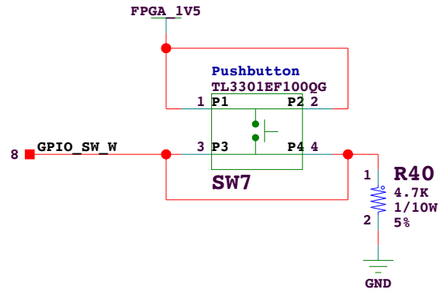
LEDs near top edge

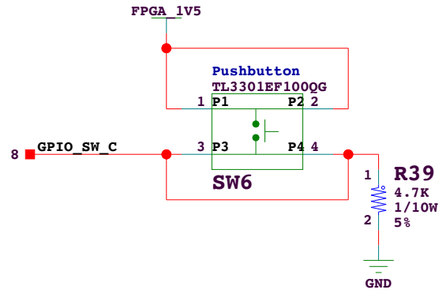


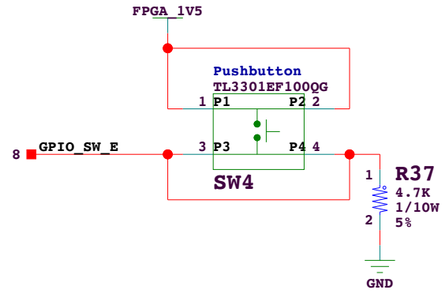


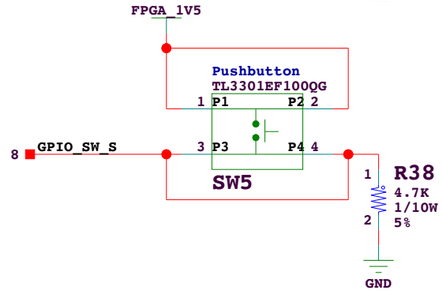
Directional Push-Buttons

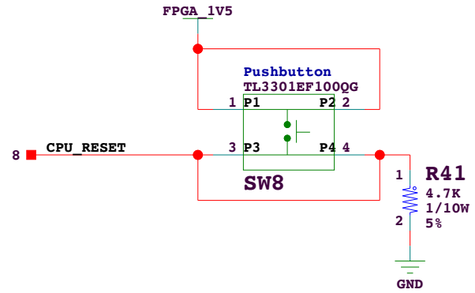












XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD GPIO SWITCHES and LEDs		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
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SOC_IRON_FG676

BANK 16
XC7A200TFBG676

IO_0_16_H17	H17	XADC_GPIO_0	29
IO_L1P_T0_16_H14	H14	FMC1_HPC_LA02_P	26
IO_L1N_T0_16_H15	H15	FMC1_HPC_LA02_N	26
IO_L2P_T0_16_G17	G17	FMC1_HPC_LA03_P	25
IO_L2N_T0_16_F17	F17	FMC1_HPC_LA03_N	25
IO_L3P_T0_DQS_16_F18	F18	FMC1_HPC_LA04_P	26
IO_L3N_T0_DQS_16_F19	F19	FMC1_HPC_LA04_N	26
IO_L4P_T0_16_G15	G15	FMC1_HPC_LA05_P	24
IO_L4N_T0_16_F15	F15	FMC1_HPC_LA05_N	24
IO_L5P_T0_16_G19	G19	FMC1_HPC_LA06_P	24
IO_L5N_T0_16_F20	F20	FMC1_HPC_LA06_N	24
IO_L6P_T0_16_H16	H16	FMC1_HPC_LA07_P	26
IO_L6N_T0_VREF_16_G16	G16	FMC1_HPC_LA07_N	26
IO_L7P_T1_16_C17	C17	FMC1_HPC_LA08_P	25
IO_L7N_T1_16_B17	B17	FMC1_HPC_LA08_N	25
IO_L8P_T1_16_E16	E16	FMC1_HPC_LA09_P	24
IO_L8N_T1_16_D16	D16	FMC1_HPC_LA09_N	24
IO_L9P_T1_DQS_16_A17	A17	FMC1_HPC_LA10_P	24
IO_L9N_T1_DQS_16_A18	A18	FMC1_HPC_LA10_N	24
IO_L10P_T1_16_B19	B19	FMC1_HPC_LA11_P	26
IO_L10N_T1_16_A19	A19	FMC1_HPC_LA11_N	26
IO_L11P_T1_SRCC_16_E17	E17	FMC1_HPC_LA01_CC_P	24
IO_L11N_T1_SRCC_16_E18	E18	FMC1_HPC_LA01_CC_N	24
IO_L12P_T1_MRCC_16_D18	D18	FMC1_HPC_LA00_CC_P	25
IO_L12N_T1_MRCC_16_C18	C18	FMC1_HPC_LA00_CC_N	25
IO_L13P_T2_MRCC_16_D19	D19	FMC1_HPC_CLK0_M2C_P	26
IO_L13N_T2_MRCC_16_C19	C19	FMC1_HPC_CLK0_M2C_N	26
IO_L14P_T2_SRCC_16_E20	E20	FMC1_HPC_LA12_P	25
IO_L14N_T2_SRCC_16_D20	D20	FMC1_HPC_LA12_N	25
IO_L15P_T2_DQS_16_B20	B20	FMC1_HPC_LA13_P	24
IO_L15N_T2_DQS_16_A20	A20	FMC1_HPC_LA13_N	24
IO_L16P_T2_16_C21	C21	FMC1_HPC_LA14_P	24
IO_L16N_T2_16_B21	B21	FMC1_HPC_LA14_N	24
IO_L17P_T2_16_B22	B22	FMC1_HPC_LA15_P	26
IO_L17N_T2_16_A22	A22	FMC1_HPC_LA15_N	26
IO_L18P_T2_16_E21	E21	FMC1_HPC_LA16_P	25
IO_L18N_T2_16_D21	D21	FMC1_HPC_LA16_N	25
IO_L19P_T3_16_C22	C22	NC	
IO_L19N_T3_VREF_16_C23	C23	NC	
IO_L20P_T3_16_B25	B25	XADC_MUX_ADDR0_LS	37
IO_L20N_T3_16_A25	A25	XADC_MUX_ADDR1_LS	37
IO_L21P_T3_DQS_16_A23	A23	XADC_MUX_ADDR2_LS	37
IO_L21N_T3_DQS_16_A24	A24	PCIE_MGT_CLK_SEL0	30
IO_L22P_T3_16_C26	C26	PCIE_MGT_CLK_SEL1	30
IO_L22N_T3_16_B26	B26	SFP_MGT_CLK_SEL0	30
IO_L23P_T3_16_C24	C24	SFP_MGT_CLK_SEL1	30
IO_L23N_T3_16_B24	B24	SI5324_RST_LS_B	22
IO_L24P_T3_16_D23	D23	REC_CLOCK_C_P	16
IO_L24N_T3_16_D24	D24	REC_CLOCK_C_N	16
IO_25_16_E22	E22	XADC_GPIO_1	29

VCCO_VADJ

F16	VCCO_16_F16
E19	VCCO_16_E19
D22	VCCO_16_D22
C25	VCCO_16_C25
B18	VCCO_16_B18
A21	VCCO_16_A21

U1

SOC_IRON_FG676

SOC_IRON_FG676

BANK 15
XC7A200TFBG676

IO_0_15_K18	K18	XADC_GPIO_2	29
IO_L1P_T0_AD0P_15_K15	K15	XADC_VAUX0_R_P	29
IO_L1N_T0_AD0N_15_J16	J16	XADC_VAUX0_R_N	29
IO_L2P_T0_AD8P_15_J14	J14	XADC_VAUX8_R_P	29
IO_L2N_T0_AD8N_15_J15	J15	XADC_VAUX8_R_N	29
IO_L3P_T0_DQS_AD1P_15_K16	K16	XADC_AD1_R_P	37
IO_L3N_T0_DQS_AD1N_15_K17	K17	XADC_AD1_R_N	37
IO_L4P_T0_15_M14	M14	FMC1_HPC_LA19_P	26
IO_L4N_T0_15_L14	L14	FMC1_HPC_LA19_N	26
IO_L5P_T0_AD9P_15_M15	M15	XADC_AD9_R_P	37
IO_L5N_T0_AD9N_15_L15	L15	XADC_AD9_R_N	37
IO_L6P_T0_15_M16	M16	FMC1_HPC_LA20_P	25
IO_L6N_T0_VREF_15_M17	M17	FMC1_HPC_LA20_N	25
IO_L7P_T1_AD2P_15_J19	J19	FMC1_HPC_LA21_P	26
IO_L7N_T1_AD2N_15_H19	H19	FMC1_HPC_LA21_N	26
IO_L8P_T1_AD10P_15_L17	L17	FMC1_HPC_LA22_P	25
IO_L8N_T1_AD10N_15_L18	L18	FMC1_HPC_LA22_N	25
IO_L9P_T1_DQS_AD3P_15_K20	K20	FMC1_HPC_LA23_P	24
IO_L9N_T1_DQS_AD3N_15_J20	J20	FMC1_HPC_LA23_N	24
IO_L10P_T1_AD11P_15_J18	J18	FMC1_HPC_LA24_P	26
IO_L10N_T1_AD11N_15_H18	H18	FMC1_HPC_LA24_N	26
IO_L11P_T1_SRCC_15_G20	G20	FMC1_HPC_LA18_CC_P	24
IO_L11N_T1_SRCC_15_G21	G21	FMC1_HPC_LA18_CC_N	24
IO_L12P_T1_MRCC_15_K21	K21	FMC1_HPC_LA17_CC_P	24
IO_L12N_T1_MRCC_15_J21	J21	FMC1_HPC_LA17_CC_N	24
IO_L13P_T2_MRCC_15_H21	H21	FMC1_HPC_CLK1_M2C_P	25
IO_L13N_T2_MRCC_15_H22	H22	FMC1_HPC_CLK1_M2C_N	25
IO_L14P_T2_SRCC_15_J23	J23	USER_SMA_CLOCK_P	3
IO_L14N_T2_SRCC_15_H23	H23	USER_SMA_CLOCK_N	3
IO_L15P_T2_DQS_15_G22	G22	FMC1_HPC_LA25_P	25
IO_L15N_T2_DQS_ADV_B_15_F22	F22	FMC1_HPC_LA25_N	25
IO_L16P_T2_A28_15_J24	J24	FMC1_HPC_LA26_P	24
IO_L16N_T2_A27_15_H24	H24	FMC1_HPC_LA26_N	24
IO_L17P_T2_A26_15_F23	F23	FMC1_HPC_LA27_P	24
IO_L17N_T2_A25_15_E23	E23	FMC1_HPC_LA27_N	24
IO_L18P_T2_A24_15_K22	K22	FMC1_HPC_LA28_P	26
IO_L18N_T2_A23_15_K23	K23	FMC1_HPC_LA28_N	26
IO_L19P_T3_A22_15_G24	G24	FMC1_HPC_LA29_P	25
IO_L19N_T3_A21_VREF_15_F24	F24	FMC1_HPC_LA29_N	25
IO_L20P_T3_A20_15_E25	E25	FMC1_HPC_LA30_P	26
IO_L20N_T3_A19_15_D25	D25	FMC1_HPC_LA30_N	26
IO_L21P_T3_DQS_15_E26	E26	FMC1_HPC_LA31_P	25
IO_L21N_T3_DQS_A18_15_D26	D26	FMC1_HPC_LA31_N	25
IO_L22P_T3_A17_15_H26	H26	FMC1_HPC_LA32_P	26
IO_L22N_T3_A16_15_G26	G26	FMC1_HPC_LA32_N	26
IO_L23P_T3_FOE_B_15_G25	G25	FMC1_HPC_LA33_P	25
IO_L23N_T3_FWE_B_15_F25	F25	FMC1_HPC_LA33_N	25
IO_L24P_T3_RS1_15_J25	J25	SM_FAN_TACH	38
IO_L24N_T3_RS0_15_J26	J26	SM_FAN_PWM	38
IO_25_15_L19	L19	XADC_GPIO_3	29

VCCO_VADJ

M18	VCCO_15_M18
K14	VCCO_15_K14
J17	VCCO_15_J17
H20	VCCO_15_H20
G23	VCCO_15_G23
F26	VCCO_15_F26

U1

SOC_IRON_FG676

VCCO_VADJ

C159 100UF 6.3 X5R

GND

VCC3V3

C57 0.1UF 25V X5R

GND

SN74AVC1T45

1	VCCA	VCCB	6
16 SI5324_RST_B	3 A	B 4	SI5324_RST_LS_B 22
2	GND	DIR	5

SC70_6 U5

VCCA, VCCB = 1.2V-TO-3.6V
DIR = L => B-TO-A

GND GND

VCCO_VADJ

C58 0.1UF 25V X5R

GND

VCCO_VADJ

C160 100UF 6.3 X5R

GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANKS15,16 HPC FMC and XADC IF		
Date:	2-14-2014_14:52	Ver:	2.0
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XC7A200T-FBG676 ONLY

SOC_IRON_FG676

BANK 12
XC7A200TFBG676

IO_0_12_AB22	AB22	NC	
IO_L1P_T0_12_AE25	AE25	FMC1_HPC_HA02_P	26
IO_L1N_T0_12_AE26	AE26	FMC1_HPC_HA02_N	26
IO_L2P_T0_12_AC22	AC22	FMC1_HPC_HA03_P	26
IO_L2N_T0_12_AC23	AC23	FMC1_HPC_HA03_N	26
IO_L3P_T0_DQS_12_AF24	AF24	FMC1_HPC_HA04_P	25
IO_L3N_T0_DQS_12_AF25	AF25	FMC1_HPC_HA04_N	25
IO_L4P_T0_12_AD25	AD25	FMC1_HPC_HA05_P	25
IO_L4N_T0_12_AD26	AD26	FMC1_HPC_HA05_N	25
IO_L5P_T0_12_AE23	AE23	FMC1_HPC_HA06_P	26
IO_L5N_T0_12_AF23	AF23	FMC1_HPC_HA06_N	26
IO_L6P_T0_12_AD23	AD23	FMC1_HPC_HA07_P	26
IO_L6N_T0_VREF_12_AD24	AD24	FMC1_HPC_HA07_N	26
IO_L7P_T1_12_AD21	AD21	FMC1_HPC_HA08_P	25
IO_L7N_T1_12_AE21	AE21	FMC1_HPC_HA08_N	25
IO_L8P_T1_12_AF19	AF19	FMC1_HPC_HA09_P	25
IO_L8N_T1_12_AF20	AF20	FMC1_HPC_HA09_N	25
IO_L9P_T1_DQS_12_AE22	AE22	FMC1_HPC_HA10_P	26
IO_L9N_T1_DQS_12_AF22	AF22	FMC1_HPC_HA10_N	26
IO_L10P_T1_12_AD20	AD20	FMC1_HPC_HA11_P	26
IO_L10N_T1_12_AE20	AE20	FMC1_HPC_HA11_N	26
IO_L11P_T1_SRCC_12_AB21	AB21	FMC1_HPC_HA01_CC_P	25
IO_L11N_T1_SRCC_12_AC21	AC21	FMC1_HPC_HA01_CC_N	25
IO_L12P_T1_MRCC_12_AA20	AA20	FMC1_HPC_HA17_CC_P	26
IO_L12N_T1_MRCC_12_AB20	AB20	FMC1_HPC_HA17_CC_N	26
IO_L13P_T2_MRCC_12_AA19	AA19	FMC1_HPC_HA00_CC_P	25
IO_L13N_T2_MRCC_12_AB19	AB19	FMC1_HPC_HA00_CC_N	25
IO_L14P_T2_SRCC_12_AC19	AC19	FMC1_HPC_HA12_P	25
IO_L14N_T2_SRCC_12_AD19	AD19	FMC1_HPC_HA12_N	25
IO_L15P_T2_DQS_12_AC18	AC18	FMC1_HPC_HA13_P	25
IO_L15N_T2_DQS_12_AD18	AD18	FMC1_HPC_HA13_N	25
IO_L16P_T2_12_AE18	AE18	FMC1_HPC_HA14_P	25
IO_L16N_T2_12_AF18	AF18	FMC1_HPC_HA14_N	26
IO_L17P_T2_12_Y18	Y18	FMC1_HPC_HA15_P	26
IO_L17N_T2_12_AA18	AA18	FMC1_HPC_HA15_N	25
IO_L18P_T2_12_AE17	AE17	FMC1_HPC_HA16_P	25
IO_L18N_T2_12_AF17	AF17	FMC1_HPC_HA16_N	25
IO_L19P_T3_12_AA17	AA17	FMC1_HPC_HA18_P	25
IO_L19N_T3_VREF_12_AB17	AB17	FMC1_HPC_HA18_N	26
IO_L20P_T3_12_AC17	AC17	FMC1_HPC_HA19_P	26
IO_L20N_T3_12_AD17	AD17	FMC1_HPC_HA19_N	25
IO_L21P_T3_DQS_12_Y16	Y16	FMC1_HPC_HA20_P	25
IO_L21N_T3_DQS_12_Y17	Y17	FMC1_HPC_HA20_N	25
IO_L22P_T3_12_AB16	AB16	FMC1_HPC_HA21_P	25
IO_L22N_T3_12_AC16	AC16	FMC1_HPC_HA21_N	26
IO_L23P_T3_12_Y15	Y15	FMC1_HPC_HA22_P	26
IO_L23N_T3_12_AA15	AA15	FMC1_HPC_HA22_N	26
IO_L24P_T3_12_W14	W14	FMC1_HPC_HA23_P	26
IO_L24N_T3_12_W15	W15	FMC1_HPC_HA23_N	26
IO_25_12_W16	W16	NC	

VCCO_VADJ

W17	VCCO_12_W17
AF26	VCCO_12_AF26
AE19	VCCO_12_AE19
AD22	VCCO_12_AD22
AB18	VCCO_12_AB18
AA21	VCCO_12_AA21

U1

SOC_IRON_FG676

VCCO_VADJ

C161
100UF
6.3
X5R

GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK12 HPC FMC IF		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
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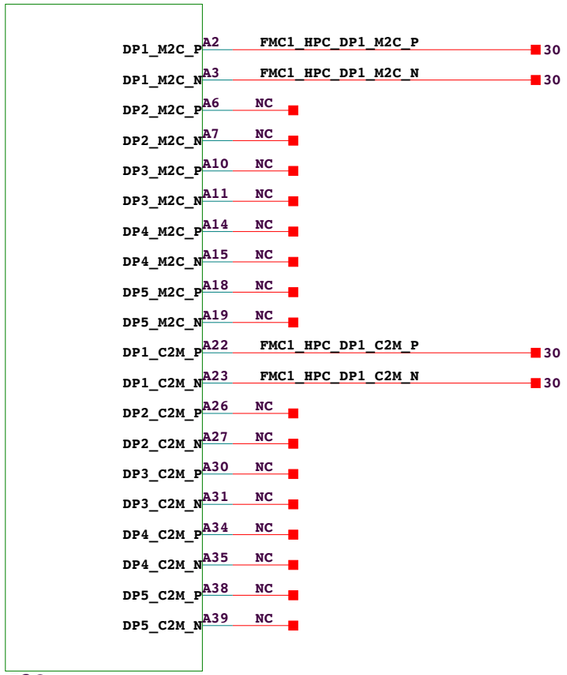
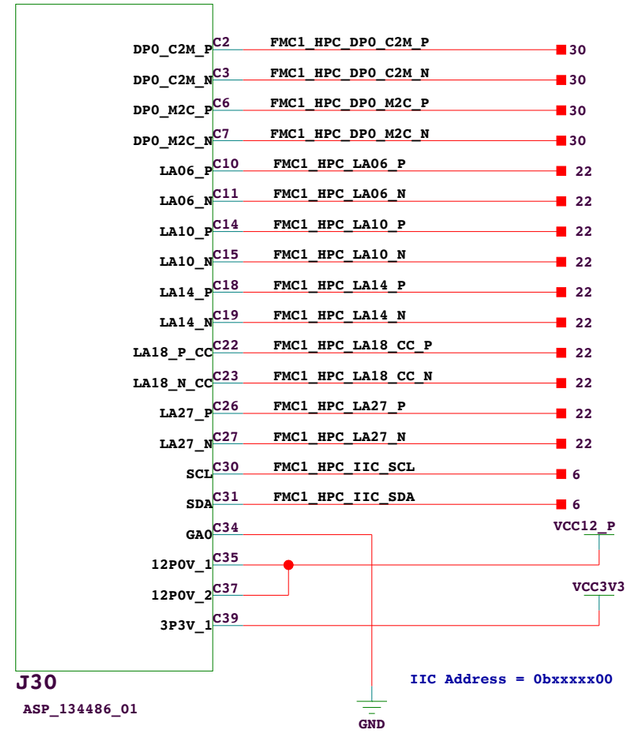
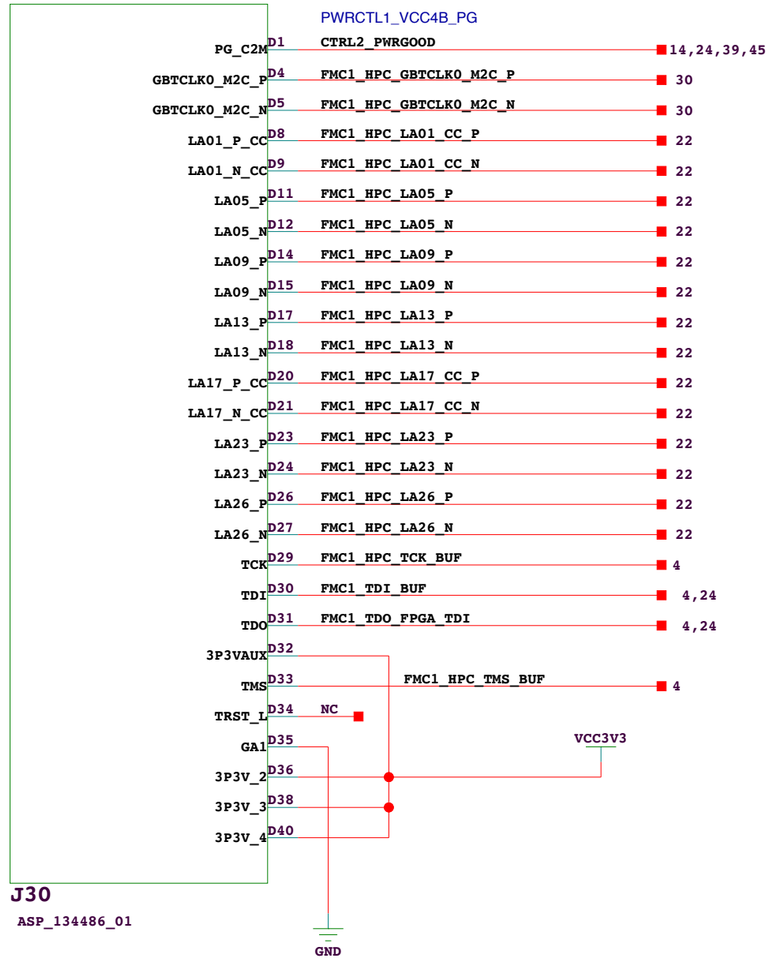
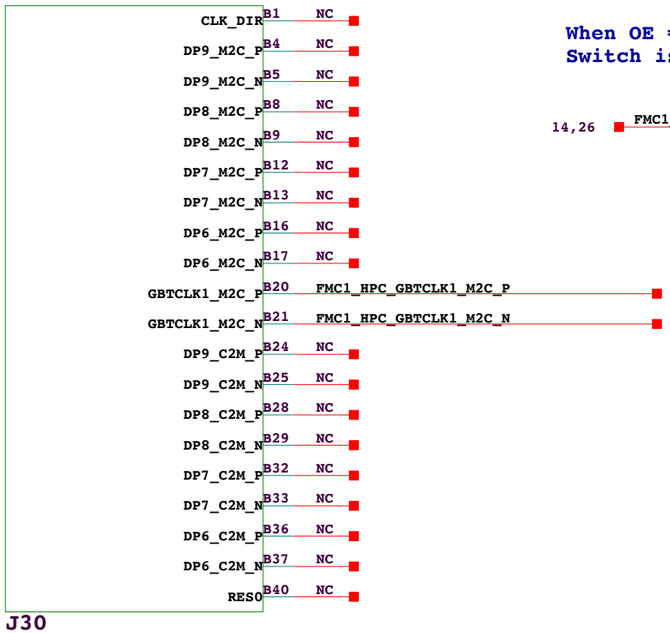
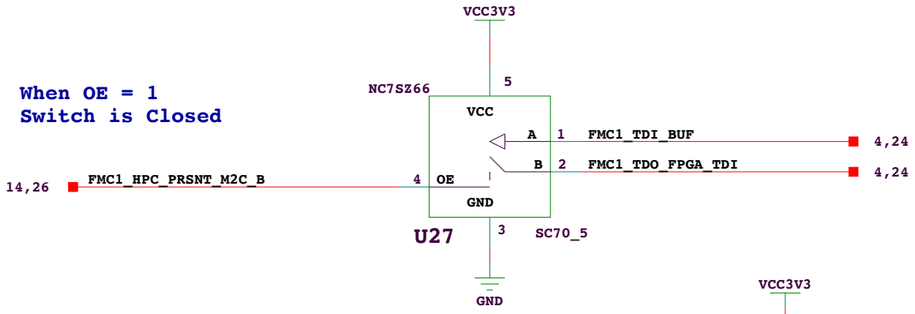




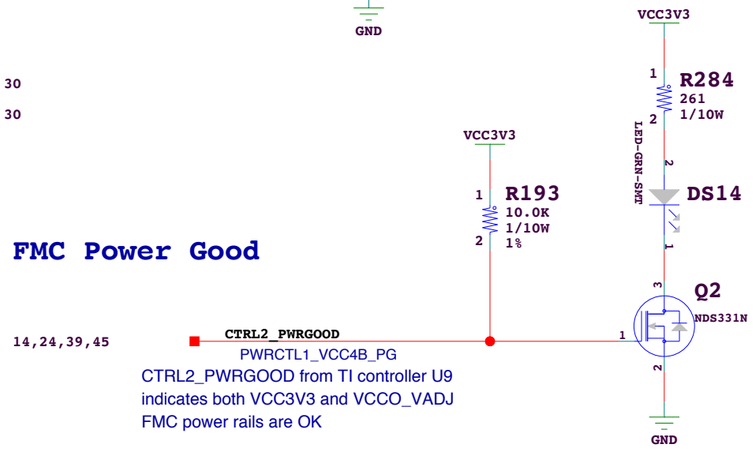




When OE = 1
Switch is Closed



FMC Power Good



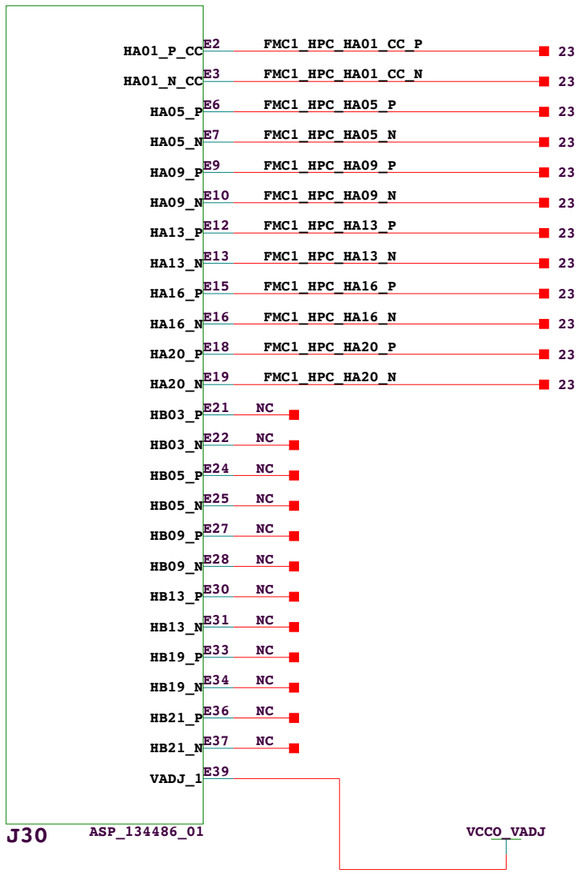
CTRL2_PWRGOOD from TI controller U9 indicates both VCC3V3 and VCCO_VADJ FMC power rails are OK

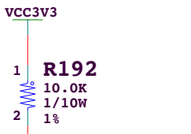
ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows A, B, C, D

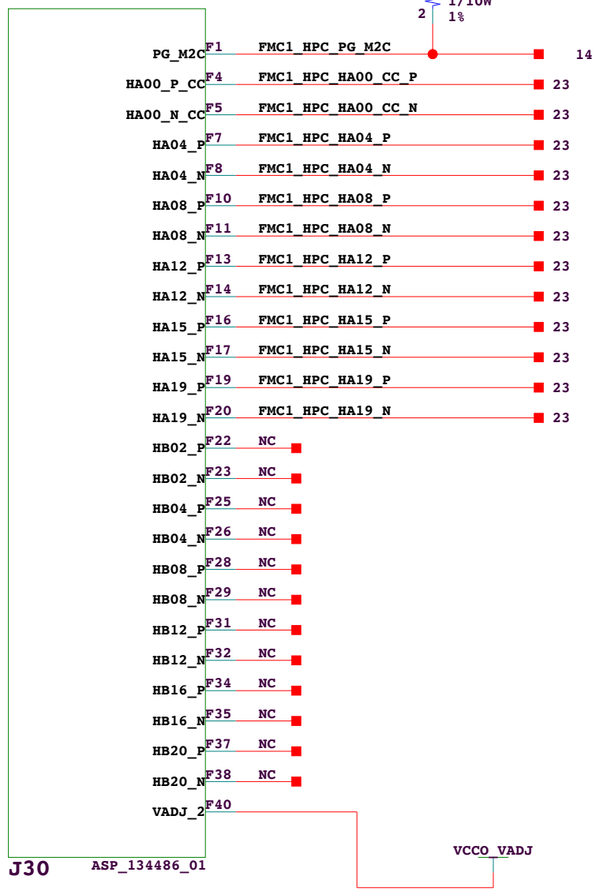
XILINX

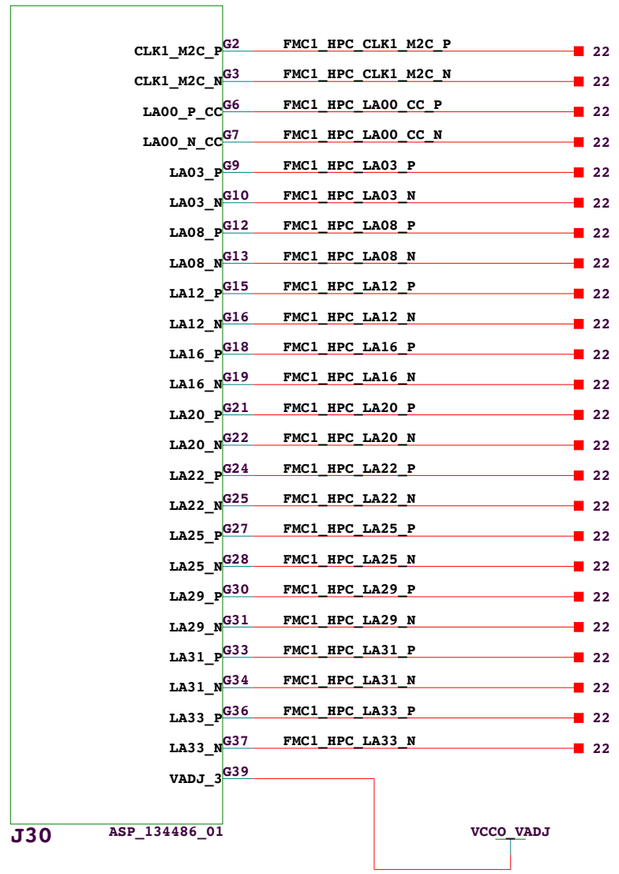
PCB P/N: 1280669
SCH P/N: 0381502

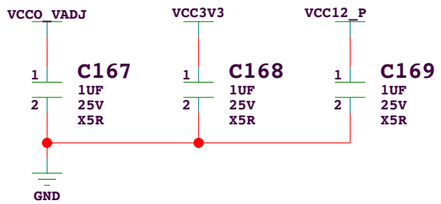
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS A, B, C, D		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	24 of 51	Drawn By	DN









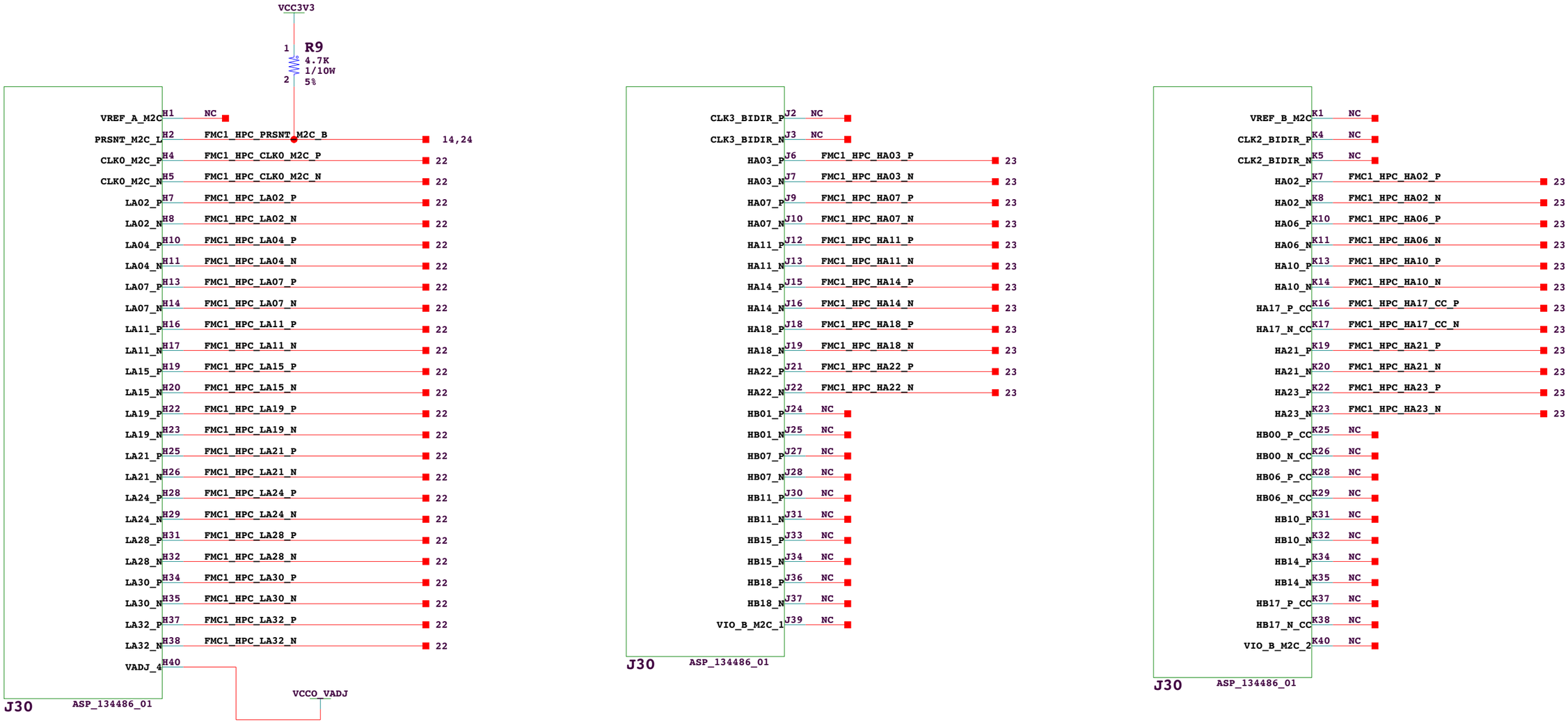


ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows E, F, G

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS E, F, G		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	25 of 51	Drawn By	DN

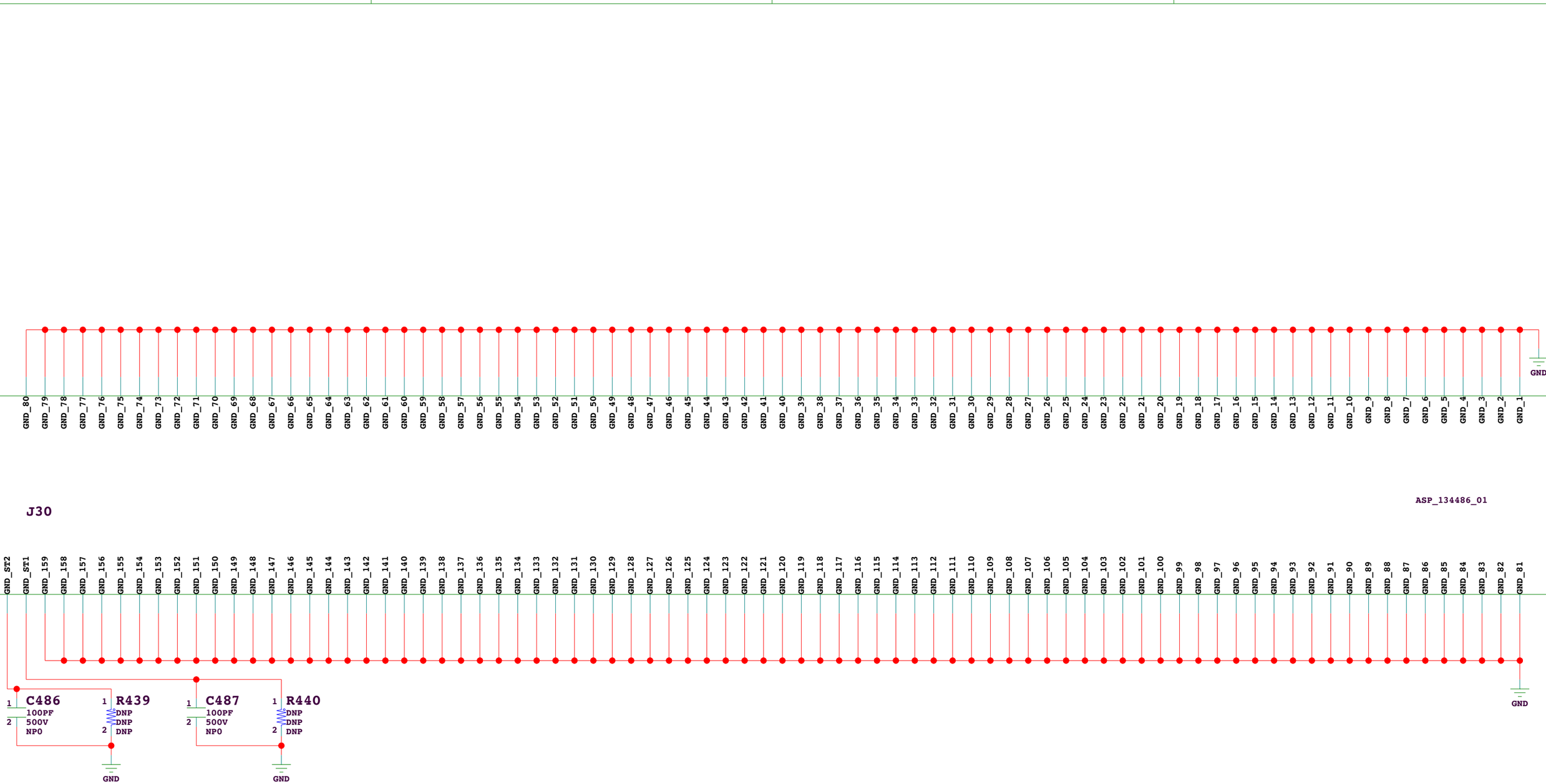


ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows H, J, K

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS H, J, K		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	26 of 51	Drawn By	DN

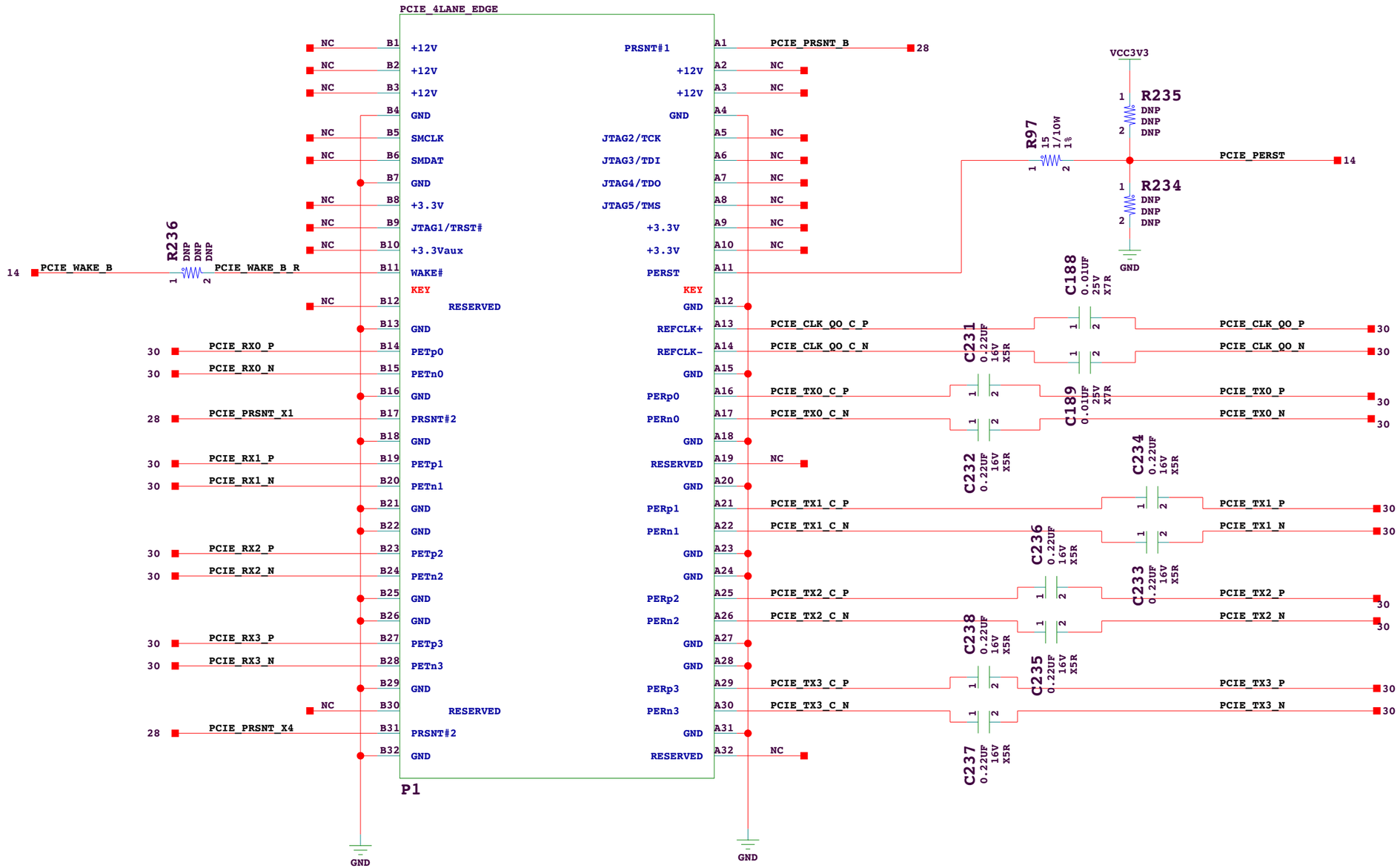


ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS GND		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	27 of 51	Drawn By	DN

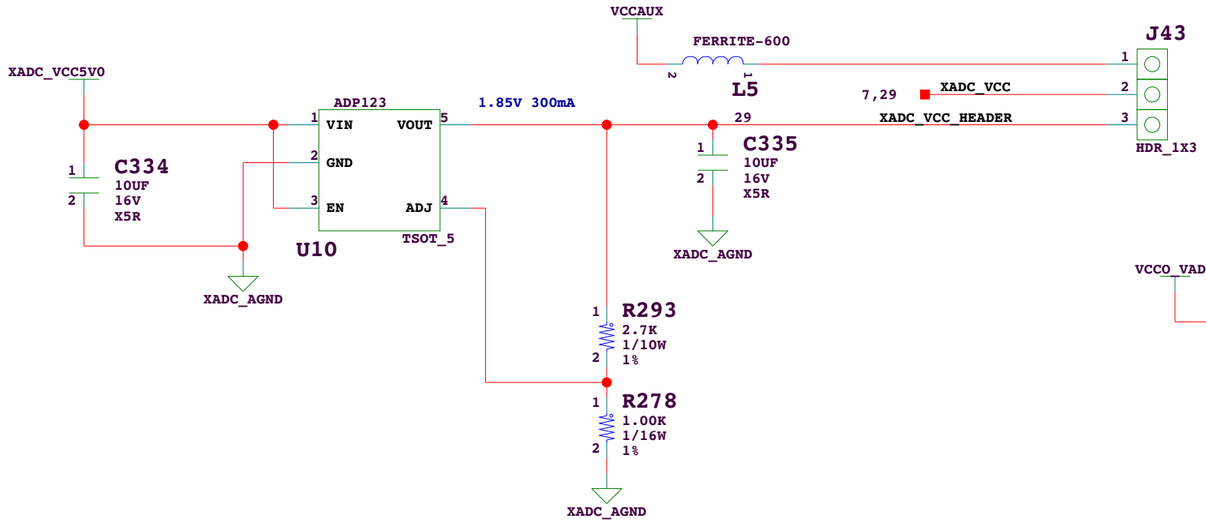


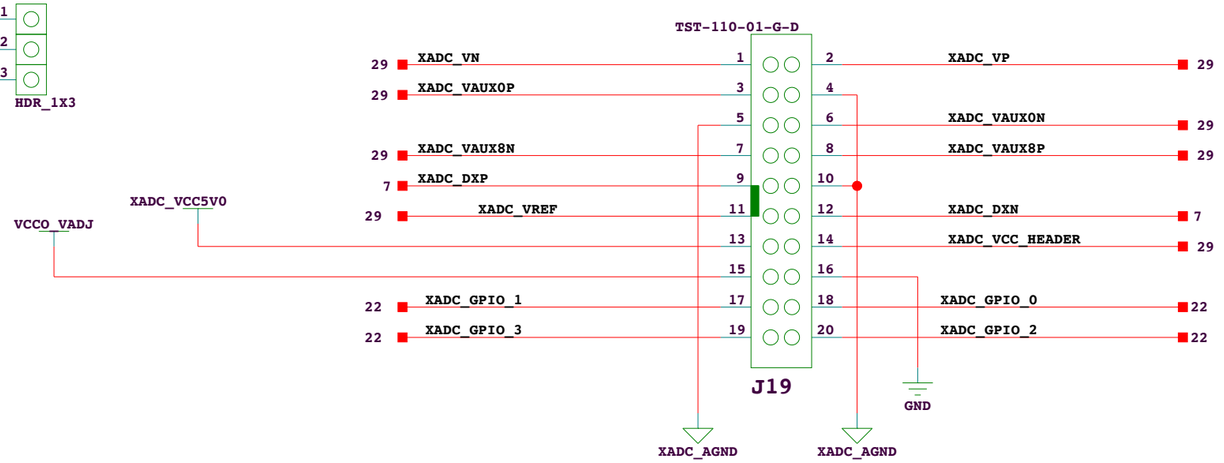
PCIe 4X Card Edge

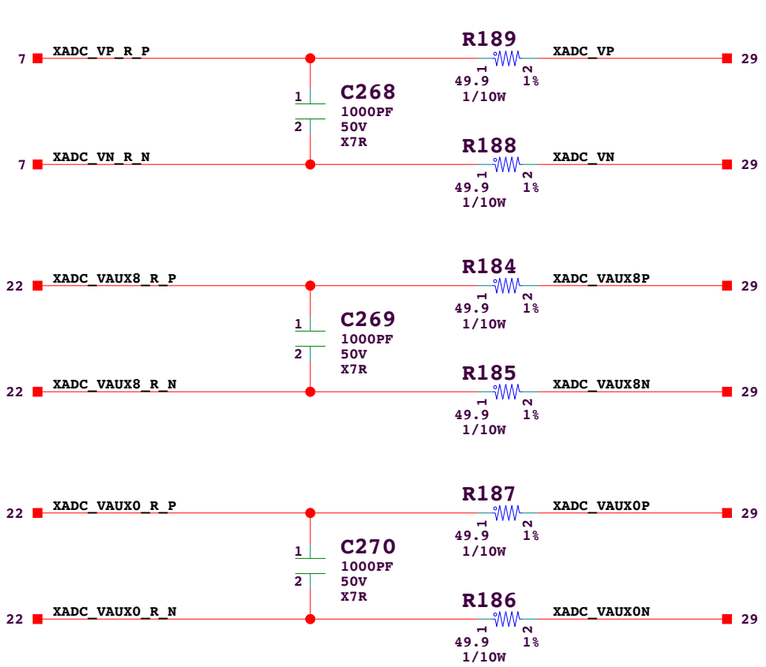
XILINX

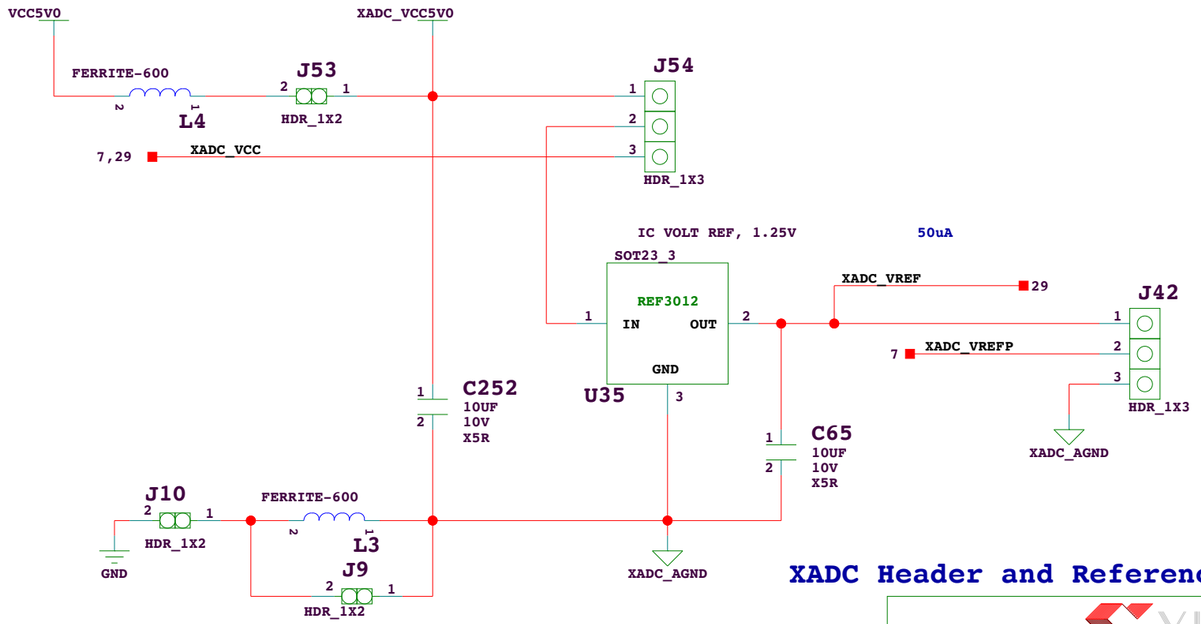
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD PCIe 4X CARD EDGE CONN. P1		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	28 of 51	Drawn By	DN









XADC Header and Reference

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC HDR. J19, XADC VREF.		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	29 of 51	Drawn By	DN

SOC_IRON_FG676

BANK 213
XC7A200TFBG676

MGTPTXP0_213_AC10	AC10	SFP_TX_P
MGTPTXN0_213_AD10	AD10	SFP_TX_N
MGTPRXP0_213_AC12	AC12	SFP_RX_P
MGTPRXN0_213_AD12	AD12	SFP_RX_N
MGTPTXP1_213_AE9	AE9	FMC1_HPC_DP0_C2M_P
MGTPTXN1_213_AF9	AF9	FMC1_HPC_DP0_C2M_N
MGTPRXP1_213_AE13	AE13	FMC1_HPC_DP0_M2C_P
MGTPRXN1_213_AF13	AF13	FMC1_HPC_DP0_M2C_N
MGTPTXP2_213_AC8	AC8	FMC1_HPC_DP1_C2M_P
MGTPTXN2_213_AD8	AD8	FMC1_HPC_DP1_C2M_N
MGTPRXP2_213_AC14	AC14	FMC1_HPC_DP1_M2C_P
MGTPRXN2_213_AD14	AD14	FMC1_HPC_DP1_M2C_N
MGTPTXP3_213_AE7	AE7	SMA_MGT_TX_P
MGTPTXN3_213_AF7	AF7	SMA_MGT_TX_N
MGTPRXP3_213_AE11	AE11	SMA_MGT_RX_P
MGTPRXN3_213_AF11	AF11	SMA_MGT_RX_N
MGTREFCLK0P_213_AA13	AA13	SFP_MGT_CLK0_C_P
MGTREFCLK0N_213_AB13	AB13	SFP_MGT_CLK0_C_N
MGTREFCLK1P_213_AA11	AA11	SFP_MGT_CLK1_C_P
MGTREFCLK1N_213_AB11	AB11	SFP_MGT_CLK1_C_N
MGTRREF_213_AF15	AF15	MGTRREF_213

U1

SOC_IRON_FG676

30 SFP_MGT_CLK1_C_P — C322 0.1UF 25V X5R — SFP_MGT_CLK1_P 30
C321 0.1UF 25V X5R
30 SFP_MGT_CLK1_C_N — SFP_MGT_CLK1_N 30

MGTAVTT — R389 100 1/10W 1%

30 SFP_MGT_CLK0_C_P — C318 0.1UF 25V X5R — SFP_MGT_CLK0_P 30
C320 0.1UF 25V X5R
30 SFP_MGT_CLK0_C_N — SFP_MGT_CLK0_N 30

SOC_IRON_FG676

BANK 216
XC7A200TFBG676

MGTPTXP0_216_B7	B7	PCIE_TX3_P
MGTPTXN0_216_A7	A7	PCIE_TX3_N
MGTPRXP0_216_B11	B11	PCIE_RX3_P
MGTPRXN0_216_A11	A11	PCIE_RX3_N
MGTPTXP1_216_D8	D8	PCIE_TX2_P
MGTPTXN1_216_C8	C8	PCIE_TX2_N
MGTPRXP1_216_D14	D14	PCIE_RX2_P
MGTPRXN1_216_C14	C14	PCIE_RX2_N
MGTPTXP2_216_B9	B9	PCIE_TX1_P
MGTPTXN2_216_A9	A9	PCIE_TX1_N
MGTPRXP2_216_B13	B13	PCIE_RX1_P
MGTPRXN2_216_A13	A13	PCIE_RX1_N
MGTPTXP3_216_D10	D10	PCIE_TX0_P
MGTPTXN3_216_C10	C10	PCIE_TX0_N
MGTPRXP3_216_D12	D12	PCIE_RX0_P
MGTPRXN3_216_C12	C12	PCIE_RX0_N
MGTREFCLK0P_216_F11	F11	PCIE_CLK_QO_P
MGTREFCLK0N_216_E11	E11	PCIE_CLK_QO_N
MGTREFCLK1P_216_F13	F13	NC
MGTREFCLK1N_216_E13	E13	NC
MGTRREF_216_A15	A15	MGTRREF_216

U1

SOC_IRON_FG676

MGTAVTT — R165 100 1/10W 1%

VCC2V5 — U3 SY89544UMG

3 EPHYCLK_QO_P — IN0
NC — VT0
3 EPHYCLK_QO_N — IN0
16 SI5324_OUT0_C_P — IN1
NC — VT1
16 SI5324_OUT0_C_N — IN1
30 FMC1_HPC_GBTCLK0_M2C_C_P — IN2
NC — VT2
30 FMC1_HPC_GBTCLK0_M2C_C_N — IN2
NC — VT3 — IN3
NC — VT3 — IN3
NC

MUX 0 1 2 3 S0 S1
NC1 14 NC
NC2 15 NC
SEL0 6
SEL1 19
PWRPAD 33
GND

VCC3 8 VCC4 17 VCC5 20 VCC6 24 VCC7 28 VCC8 29
C105 0.1UF 25V X5R
GND

SY89544UMG
Q 10 SFP_MGT_CLK0_P 30
Q 11 SFP_MGT_CLK0_N 30

GND1 7 GND2 9 GND3 12 GND4 13 GND5 16 GND6 18

DEFAULT: IN0: EPHYCLK

MGT_CLK0_SEL0
Q24 NDS336P 460MW
22 SFP_MGT_CLK_SEL0
R454 10.0K 1/10W 1%
R455 10.0K 1/10W 1%
VCC2V5
MGT_CLK0_SEL1
R332 10.0K 1/10W 1%
GND
Q25 NDS336P 460MW
22 SFP_MGT_CLK_SEL1
R333 10.0K 1/10W 1%
GND

VCC2V5 — U4 SY89544UMG

3 SMA_MGT_REFCLK_P — IN0
NC — VT0
3 SMA_MGT_REFCLK_N — IN0
16 SI5324_OUT1_C_P — IN1
NC — VT1
16 SI5324_OUT1_C_N — IN1
30 FMC1_HPC_GBTCLK1_M2C_C_P — IN2
NC — VT2
30 FMC1_HPC_GBTCLK1_M2C_C_N — IN2
NC — VT3 — IN3
NC — VT3 — IN3
NC

MUX 0 1 2 3 S0 S1
NC1 14 NC
NC2 15 NC
SEL0 6
SEL1 19
PWRPAD 33
GND

VCC3 8 VCC4 17 VCC5 20 VCC6 24 VCC7 28 VCC8 29
C106 0.1UF 25V X5R
GND

SY89544UMG
Q 10 SFP_MGT_CLK1_P 30
Q 11 SFP_MGT_CLK1_N 30

GND1 7 GND2 9 GND3 12 GND4 13 GND5 16 GND6 18

R493 0 5% 1/10W — 24 FMC1_HPC_GBTCLK0_M2C_P — FMC1_HPC_GBTCLK0_M2C_C_P 30
R492 0 5% 1/10W — 24 FMC1_HPC_GBTCLK0_M2C_N — FMC1_HPC_GBTCLK0_M2C_C_N 30
R494 0 5% 1/10W — 24 FMC1_HPC_GBTCLK1_M2C_P — FMC1_HPC_GBTCLK1_M2C_C_P 30
R495 0 5% 1/10W — 24 FMC1_HPC_GBTCLK1_M2C_N — FMC1_HPC_GBTCLK1_M2C_C_N 30

DEFAULT: IN0: SMA_MGT_RECLK

MGT_CLK1_SEL0
Q23 NDS336P 460MW
22 PCIE_MGT_CLK_SEL0
R452 10.0K 1/10W 1%
R453 10.0K 1/10W 1%
VCC2V5
MGT_CLK1_SEL1
R151 10.0K 1/10W 1%
GND
Q22 NDS336P 460MW
22 PCIE_MGT_CLK_SEL1
R152 10.0K 1/10W 1%
GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD MGT BANKS 213, 216, 2X CLOCK MUX		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	30 of 51	Drawn By	DN

SOC_IRON_FG676

BANK MGTAVCC
XC7A200TFBG676

MGTAVCC_AA10 AA10
MGTAVCC_AC11 AC11
MGTAVCC_AC13 AC13
MGTAVCC_AC9 AC9
MGTAVCC_D11 D11
MGTAVCC_D13 D13
MGTAVCC_D9 D9
MGTAVCC_F10 F10
MGTAVCC_AA12 AA12
MGTAVCC_F12 F12

U1

SOC_IRON_FG676

MGTAVCC

J41 1 YELLOW

J29 1 BLACK

GND

Place scope test points close to FPGA

SOC_IRON_FG676

BANK MGTAVTT
XC7A200TFBG676

MGTAVTT_AE10 AE10
MGTAVTT_AE12 AE12
MGTAVTT_AE14 AE14
MGTAVTT_AE8 AE8
MGTAVTT_AD15 AD15
MGTAVTT_AD7 AD7
MGTAVTT_B10 B10
MGTAVTT_B12 B12
MGTAVTT_B14 B14
MGTAVTT_B8 B8
MGTAVTT_C15 C15
MGTAVTT_C7 C7

U1

SOC_IRON_FG676

MGTAVTT

J40 1 YELLOW

J28 1 BLACK

GND

Place scope test points close to FPGA

MGTAVCC

C228 4.7UF 25V X5R
C101 0.1UF 25V X5R
C102 0.1UF 25V X5R

Spec=4.7uF, 2x0.1uF

C329 DNP 25V X5R
C330 DNP 25V X5R
C331 DNP 25V X5R
C332 DNP 25V X5R

C342 DNP 25V X5R
C341 DNP 25V X5R
C340 DNP 25V X5R
C333 DNP 25V X5R

GND

Place MGT 0.1uF caps within the FPGA via field on the bottom of the board, one for each MGT power pin/GND pin pair

MGTAVTT

C226 4.7UF 25V X5R
C103 0.1UF 25V X5R
C104 0.1UF 25V X5R

Spec=4.7uF, 2x0.1uF

C346 DNP 25V X5R
C345 DNP 25V X5R
C344 DNP 25V X5R
C343 DNP 25V X5R
C352 DNP 25V X5R

C350 DNP 25V X5R
C349 DNP 25V X5R
C348 DNP 25V X5R
C347 DNP 25V X5R
C351 DNP 25V X5R

GND

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD MGT PWR. BANKS AVCC and AVTT		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	31 of 51	Drawn By	DN

SOC_IRON_FG676

BANK VCCINT
XC7A200TFBG676

VCCINT

VCCINT_J11	J11
VCCINT_J13	J13
VCCINT_K10	K10
VCCINT_K12	K12
VCCINT_L11	L11
VCCINT_L13	L13
VCCINT_M10	M10
VCCINT_P10	P10
VCCINT_T10	T10
VCCINT_T12	T12
VCCINT_U11	U11
VCCINT_V10	V10
VCCINT_V12	V12

U1

SOC_IRON_FG676

SOC_IRON_FG676

BANK VCCAUX
XC7A200TFBG676

VCCAUX

VCCAUX_U9	U9
VCCAUX_J9	J9
VCCAUX_L9	L9
VCCAUX_N9	N9
VCCAUX_R9	R9

U1

SOC_IRON_FG676

SOC_IRON_FG676

BANK VCCBRAM
XC7A200TFBG676

VCCBRAM

VCCBRAM_N13	N13
VCCBRAM_R13	R13
VCCBRAM_U13	U13
VCCBRAM_W13	W13

U1

SOC_IRON_FG676

VCCINT

VCCINT

C407 680UF 6.3V TANT
C421 100UF 6.3 X5R
C422 100UF 6.3 X5R
C353 C354 C355 C356 C387 4.7UF 6.3V X5R
C357 C358 C359 C360 C388 4.7UF 6.3V X5R
C365 C366 C367 C368 C389 4.7UF 6.3V X5R
C361 C362 C363 C364 C390 4.7UF 6.3V X5R
C369 C370 C371 C372 C373 4.7UF 6.3V X5R
C374 C375 C376 4.7UF 6.3V X5R

GND

1x680uF, 2x100uF, 28x4.7uF
42x0.47uF on PG.34

VCCAUX

VCCAUX

C213 C214 C215 47UF 25V X5R
C420 C419 C417 C416 0.47UF 10V X5R
C431 C430 C429 C428 0.47UF 10V X5R
C425 C426 C427 0.47UF 10V X5R

GND

3x47uF, 4x4.7uF, 7x0.47uF

VCCBRAM

VCCBRAM

C399 C418 100UF 6.3 X5R
C377 C378 C379 C391 4.7UF 6.3V X5R
C415 C414 C413 C412 0.47UF 10V X5R
C411 C410 C409 C408 0.47UF 10V X5R

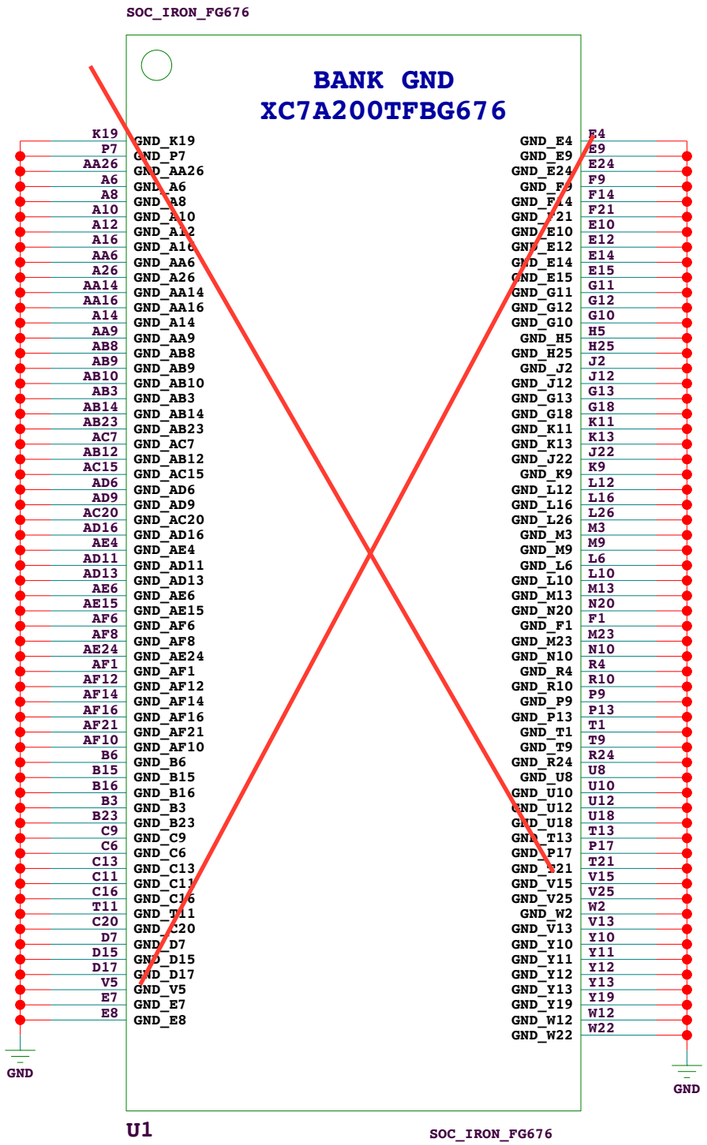
GND

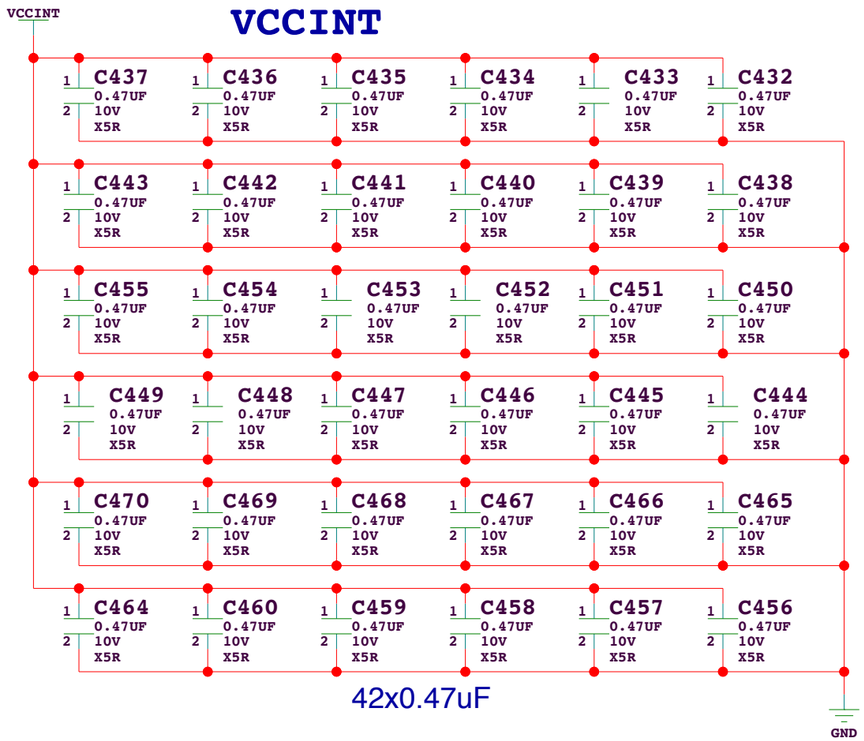
2x100uF, 4x4.7uF, 8x0.47uF

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA CORE PWR. BANKS		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	32 of 51	Drawn By	DN





XILINX

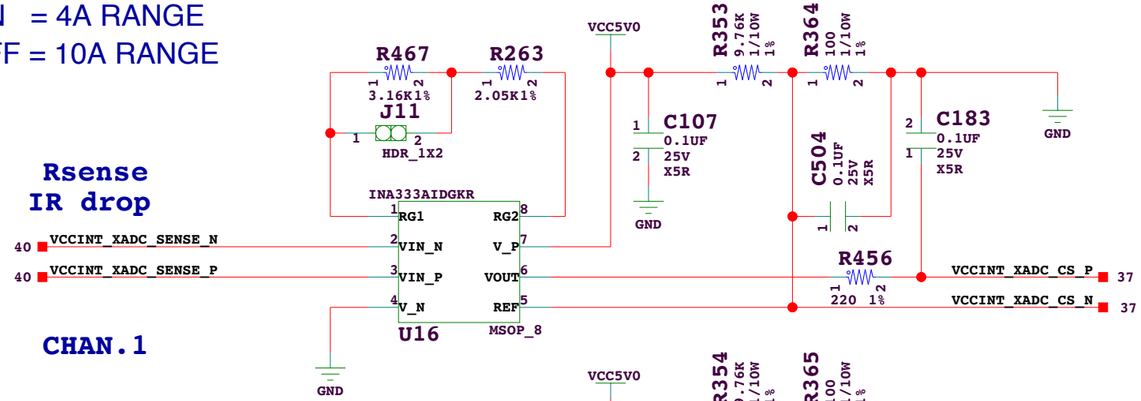
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA PWR. BANK GND		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	33 of 51	Drawn By	DN

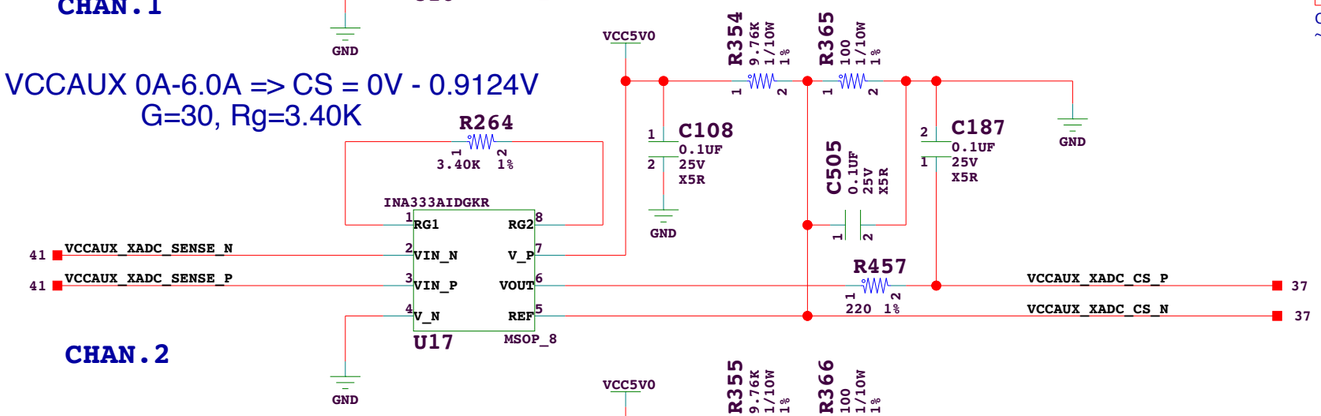
XADC I/F MONITORING CIRCUIT PAGE 1

VCCINT 0A-10A => CS = 0V - 1.009V G=20, Rg=5.21K
VCCINT 0A-4A => CS = 0V - 0.996V G=50, Rg=2.05K

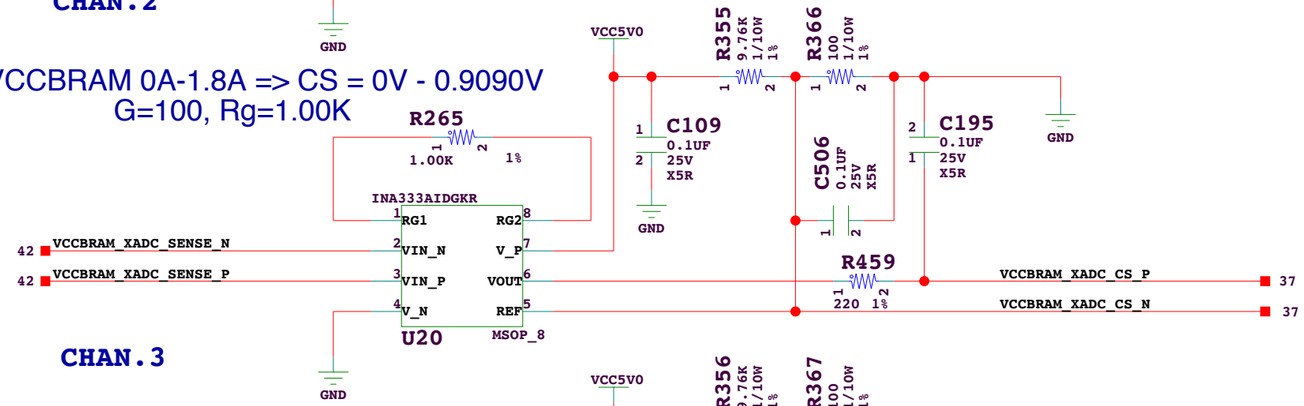
J11 ON = 4A RANGE
J11 OFF = 10A RANGE



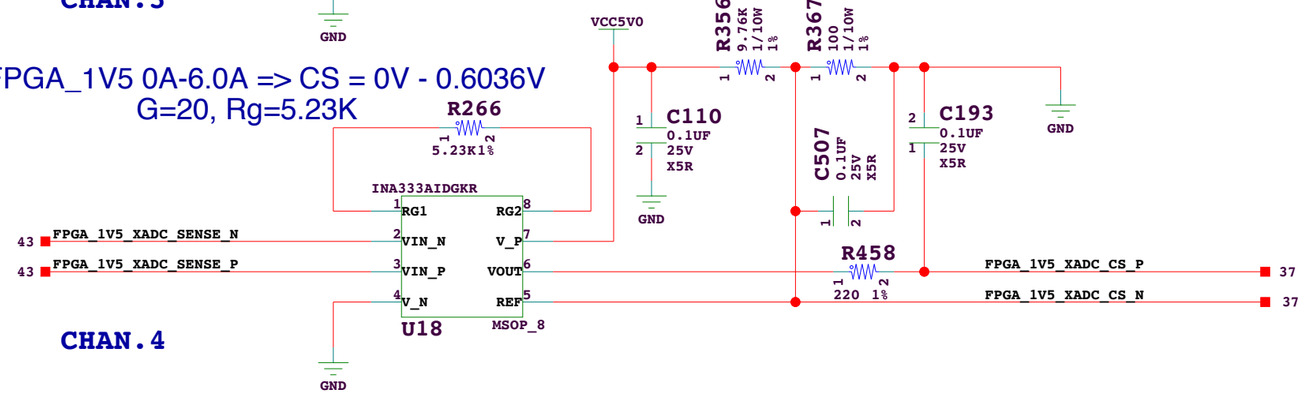
VCCAUX 0A-6.0A => CS = 0V - 0.9124V
G=30, Rg=3.40K



VCCBRAM 0A-1.8A => CS = 0V - 0.9090V
G=100, Rg=1.00K

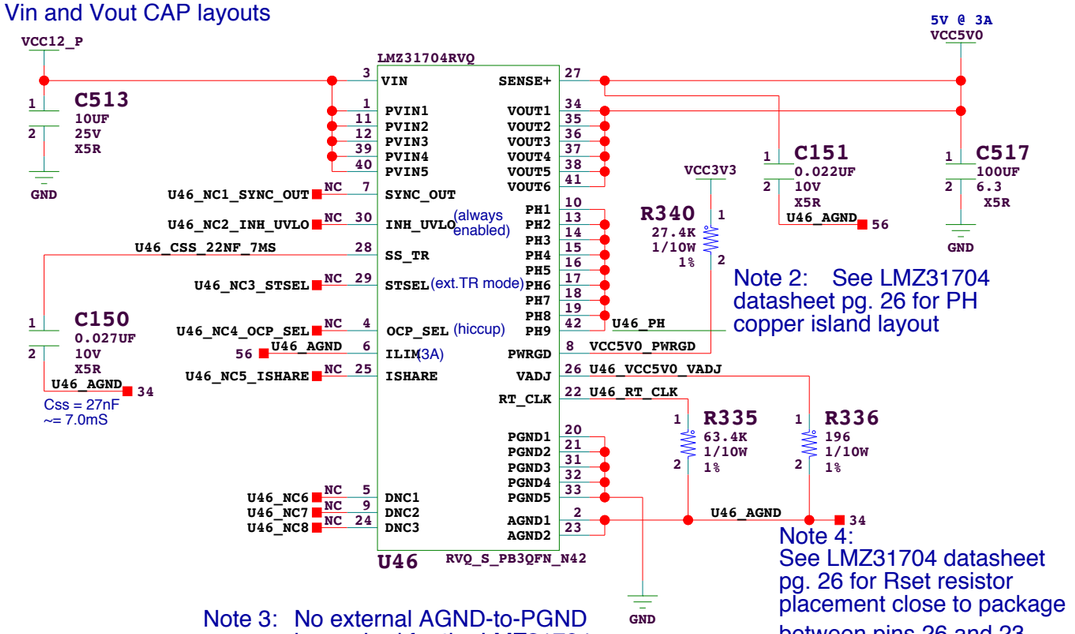


FPGA_1V5 0A-6.0A => CS = 0V - 0.6036V
G=20, Rg=5.23K



CONTROLLER #1&2
OP AMP SUPPLY

Note 1: See LMZ31704 datasheet pg. 26 for Vin and Vout CAP layouts

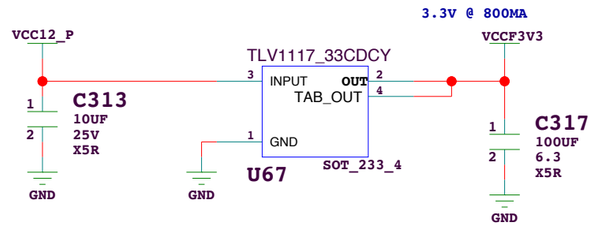


Note 2: See LMZ31704 datasheet pg. 26 for PH copper island layout

Note 3: No external AGND-to-PGND is required for the LMZ31704 per TI on 2-7-2014

Note 4: See LMZ31704 datasheet pg. 26 for Rset resistor placement close to package between pins 26 and 23

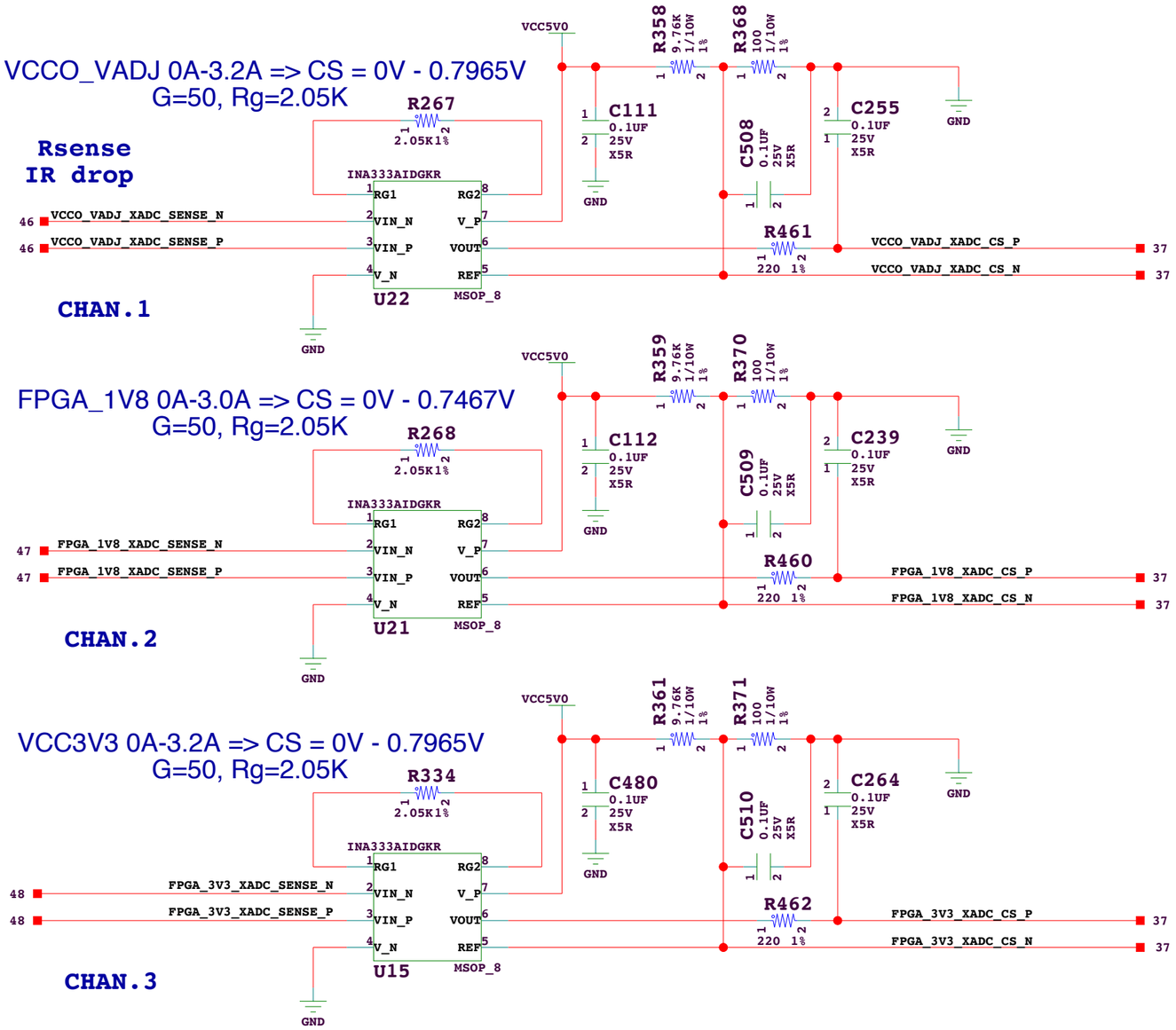
3.3V IMMEDIATE ON FIXED SUPPLY



XILINX		PCB P/N: 1280669 SCH P/N: 0381502	
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	34 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 2

CONTROLLER #2



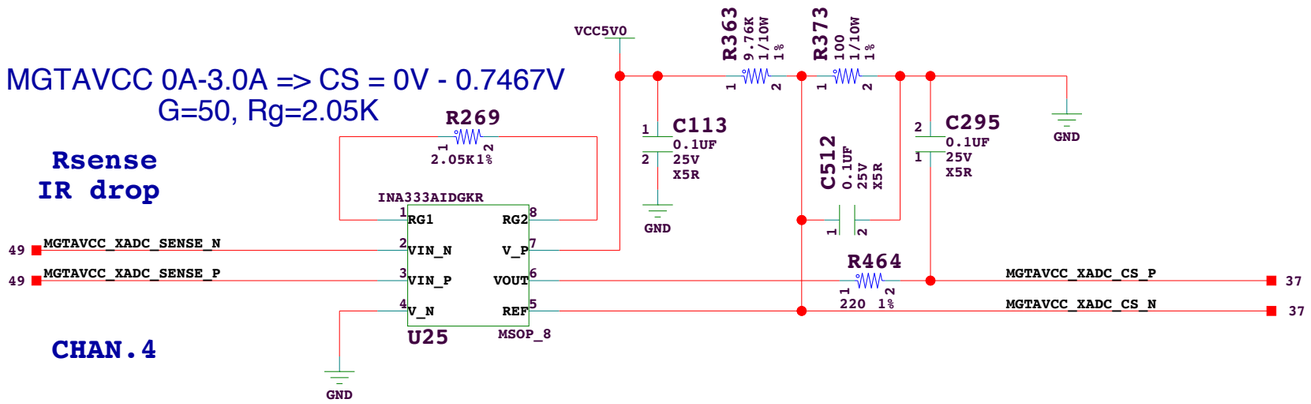
XILINX

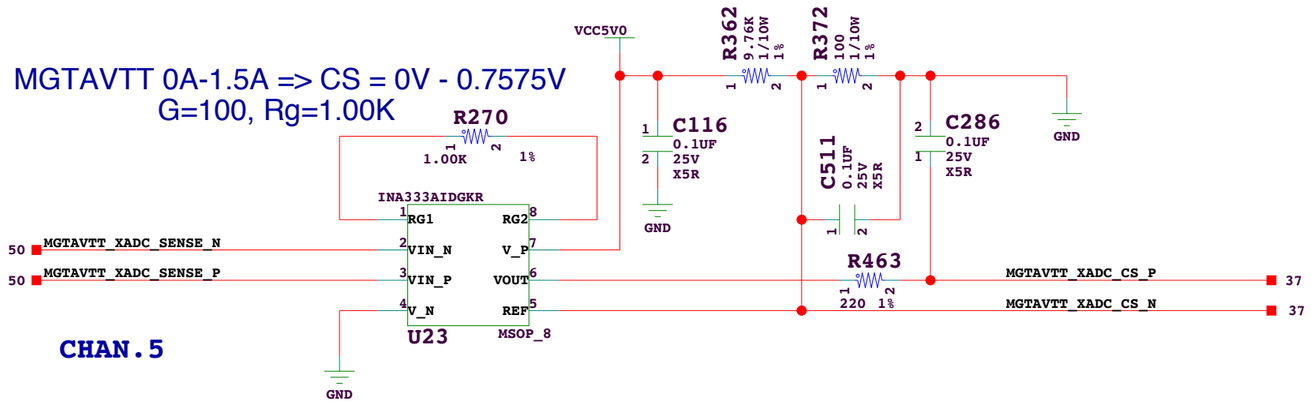
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	35 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 3

CONTROLLER #2



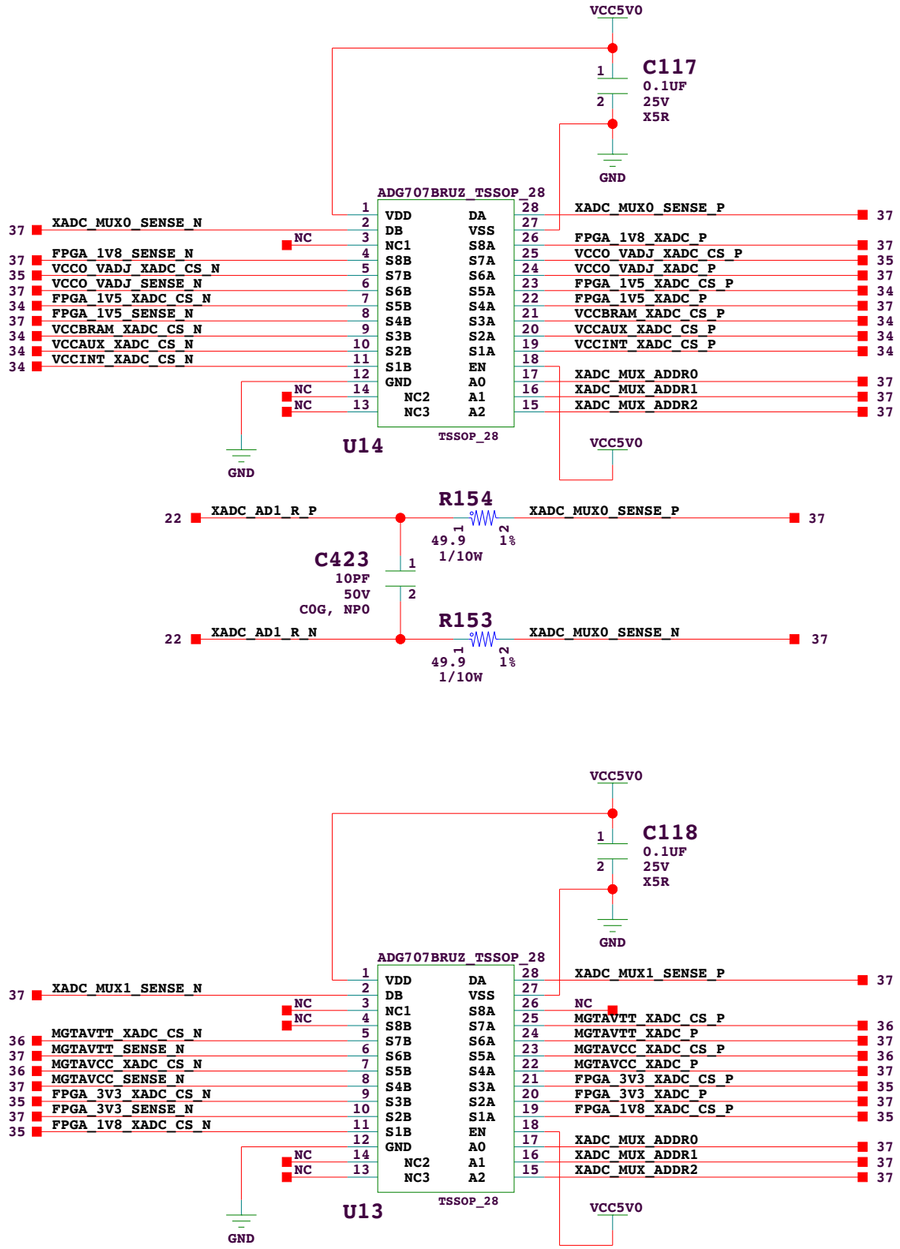


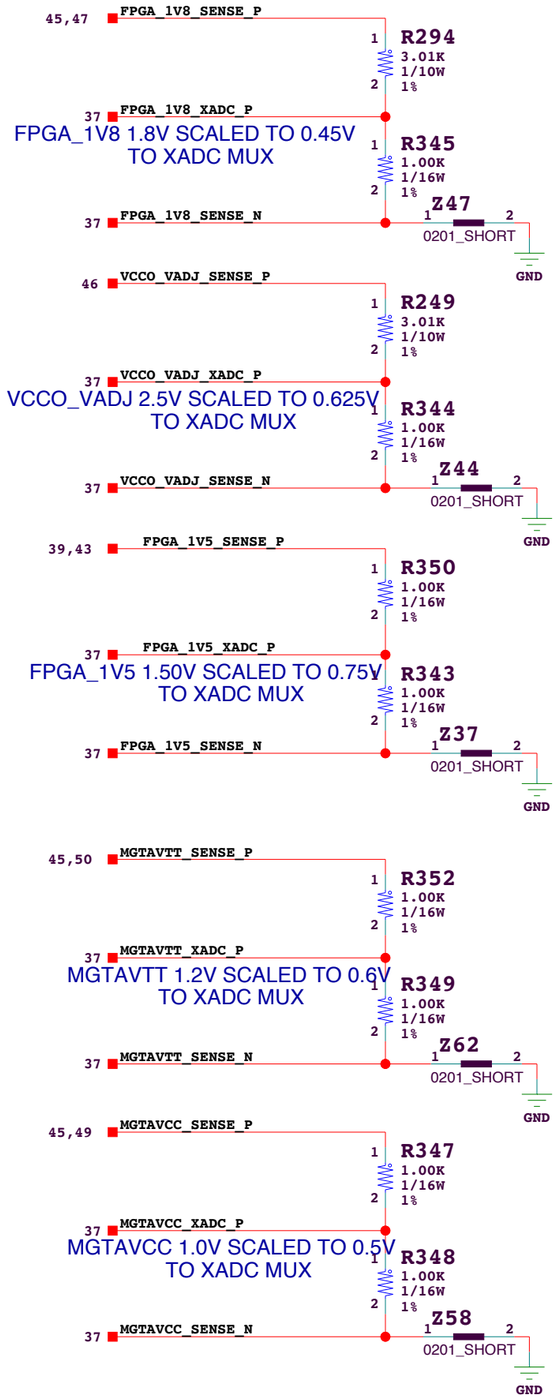
XILINX

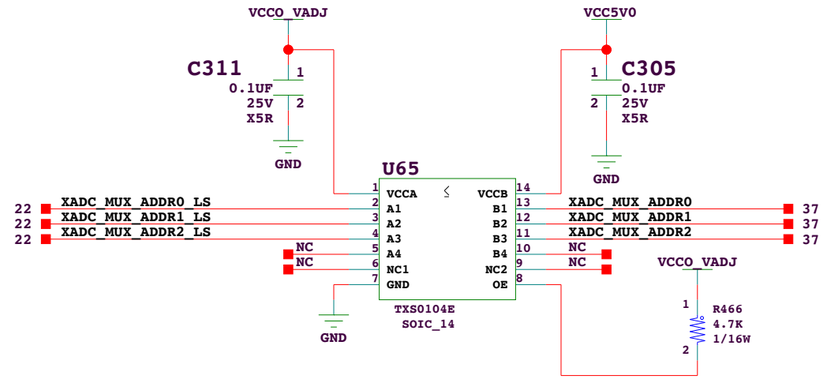
PCB P/N: 1280669
SCH P/N: 0381502

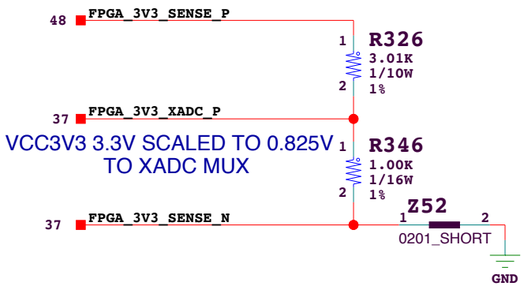
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	36 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 4



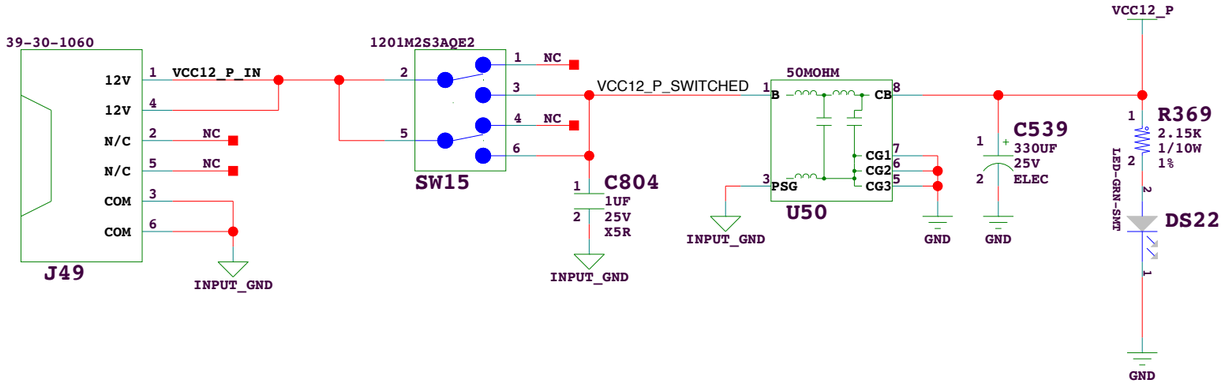






XILINX		PCB P/N: 1280669	
		SCH P/N: 0381502	
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. 2X MUX		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	37 of 51	Drawn By	DN

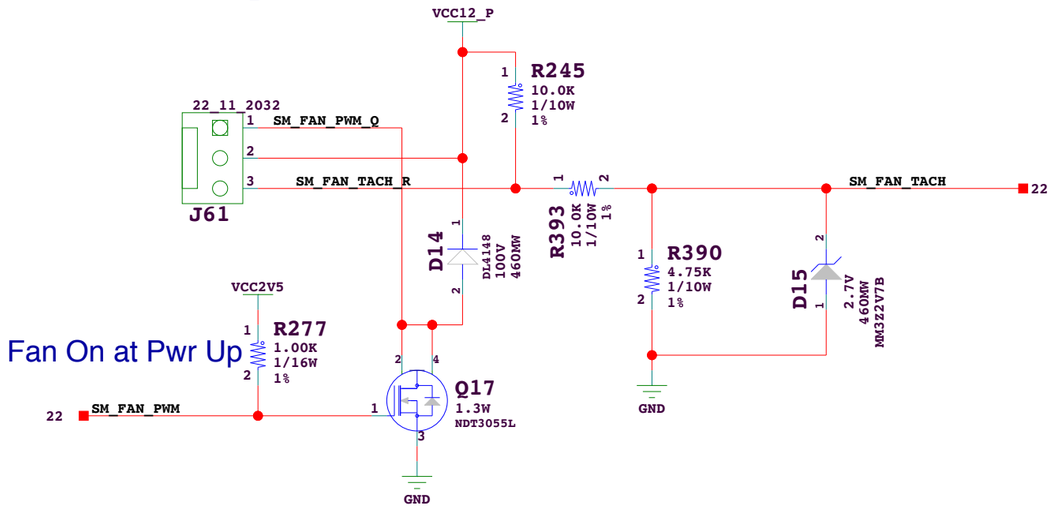
POWER SYSTEM SCHEMATIC STARTS HERE



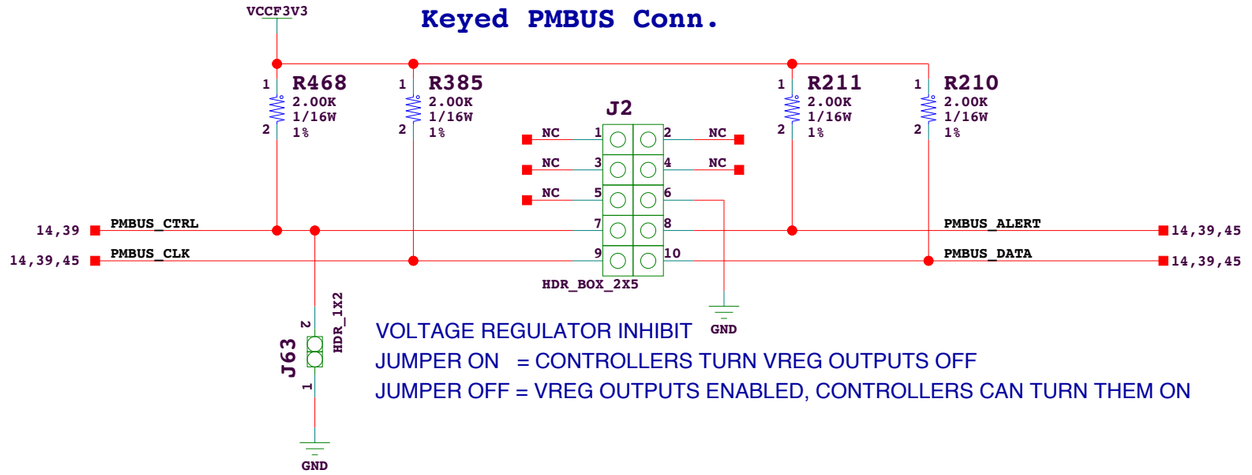
AC701 POWER SYSTEM CONFIGURATION

CTLR	REF	PAGE	PMBUS ADDR/RAIL	NET NAME	VOLTAGE	VREG-TYPE	MAX I
#1	U8	PG 39	101 UCD90120A	4 RAILS:			
		PG 40	101 1	VCCINT	1.0V	LMZ31710 U49	10A
		PG 41	101 2	VCCAUX	1.8V	LMZ31506 U53	6A
		PG 42	101 3	VCCBRAM	1.0V	LMZ31503 U54	3A
		PG 43	101 4	FPGA_1V5	1.5V	LMZ31506 U55	6A
#2	U9	PG 45	102 UCD90120A	5 RAILS:			
		PG 46	102 1	VCCO_VADJ	2.5V	LMZ31506 U56	6A
		PG 47	102 2	FPGA_1V8	1.8V	LMZ31503 U57	3A
		PG 48	102 3	FPGA_3V3	3.3V	LMZ31506 U58	6A
		PG 49	102 4	MGTAVCC	1.0V	LMZ31503 U59	3A
		PG 49	102 5	MGTAVTT	1.2V	LMZ31503 U60	3A

Keyed Fan Header



Keyed PMBUS Conn.



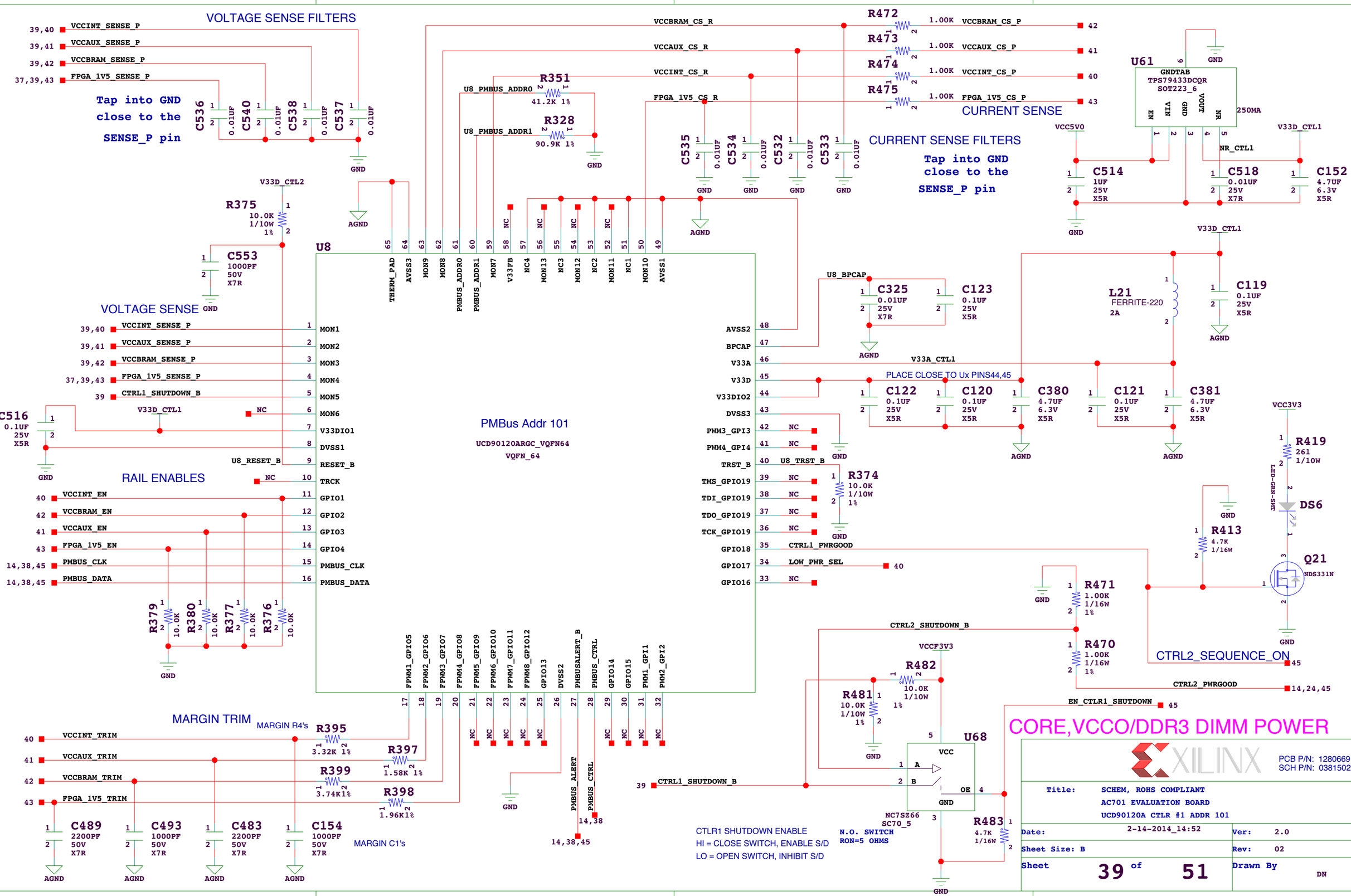
VOLTAGE REGULATOR INHIBIT
JUMPER ON = CONTROLLERS TURN VREG OUTPUTS OFF
JUMPER OFF = VREG OUTPUTS ENABLED, CONTROLLERS CAN TURN THEM ON

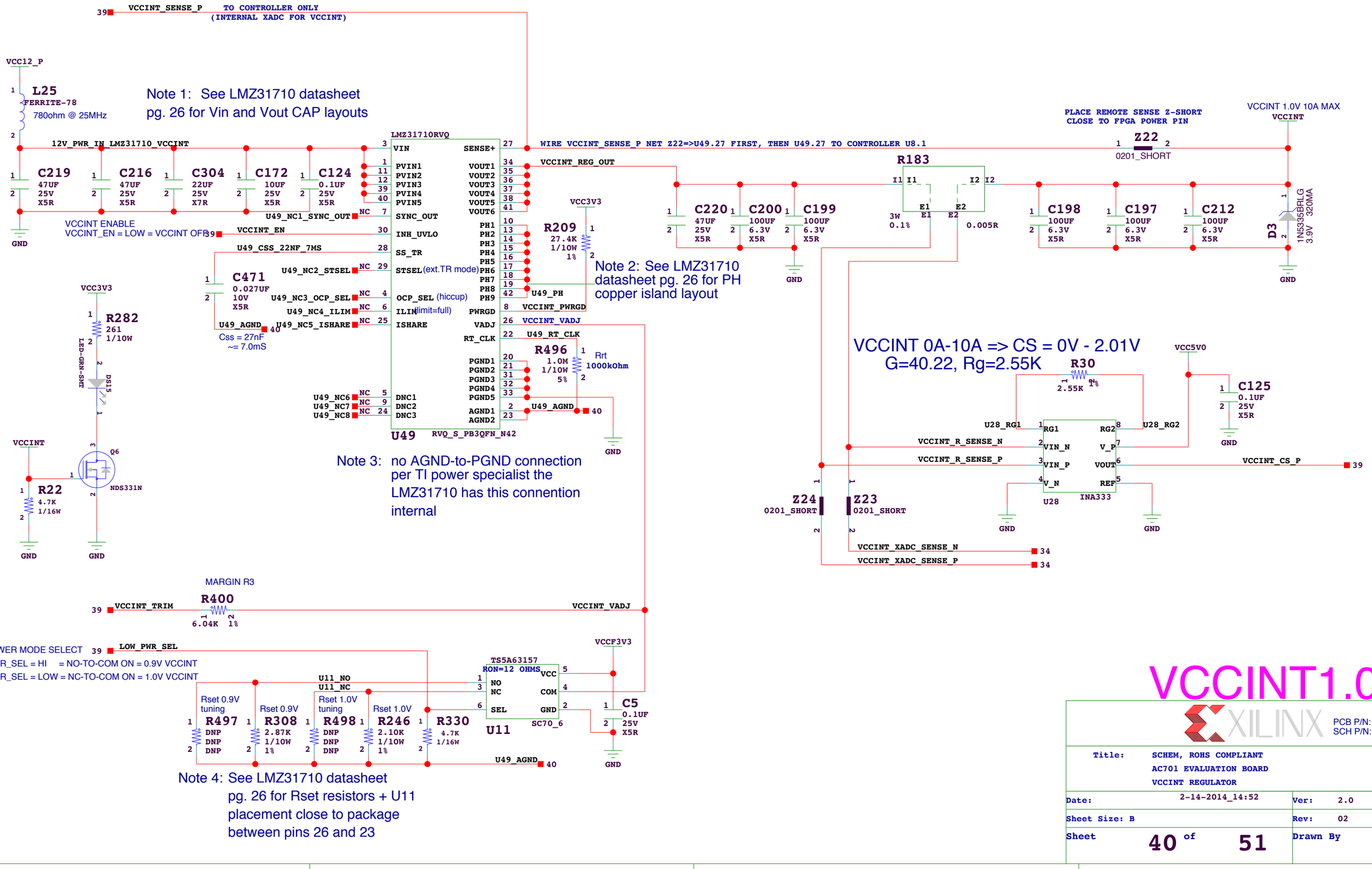
Power Connector and switch, PMBus Header

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD POWER CONN.,SWITCH,PMBUS HEADER,FAN CONTROL		
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	38 of 51	Drawn By	DN


VOLTAGE SENSE FILTERS
39,40 VCCINT_SENSE_P
39,41 VCCAUX_SENSE_P
39,42 VCCBRAM_SENSE_P
37,39,43 FPGA_1V5_SENSE_P
Tap into GND close to the SENSE_P pin
C536 0.01UF
C540 0.01UF
C538 0.01UF
C537 0.01UF
GND
VCCBRAM_CS_R
VCCAUX_CS_R
VCCINT_CS_R
FPGA_1V5_CS_R
R472 1.00K VCCBRAM_CS_P 42
R473 1.00K VCCAUX_CS_P 41
R474 1.00K VCCINT_CS_P 40
R475 1.00K FPGA_1V5_CS_P 43
CURRENT SENSE
CURRENT SENSE FILTERS
Tap into GND close to the SENSE_P pin
C535 0.01UF
C534 0.01UF
C532 0.01UF
C533 0.01UF
U8_PMBUS_ADDR0
R351 41.2K 1%
U8_PMBUS_ADDR1
R328 90.9K 1%
U61
GNDTAB
TPS79433DCQR
SOT223_6
EN VIN GND VOUT NR
250MA
VCC5V0
V33D_CTL1
NR_CTL1
C514 1UF 25V X5R
C518 0.01UF 25V X7R
C152 4.7UF 6.3V X5R
V33D_CTL2
R375 10.0K 1/10W 1%
C553 1000PF 50V X7R
AGND
U8
THERM_PAD AVSS3 MON9 MON8 PMBUS_ADDR0 PMBUS_ADDR1 MON7 V33FB NC4 MON13 NC3 MON12 NC2 MON11 NC1 MON10 AVSS1
AVSS2 BPCAP V33A V33D V33DIO2 DVSS3 PWM3_GPI3 PWM4_GPI4 TRST_B TMS_GPIO19 TDI_GPIO19 TDO_GPIO19 TCK_GPIO19 GPIO18 GPIO17 GPIO16
U8_BPCAP
C325 0.01UF 25V X7R
C123 0.1UF 25V X5R
L21 FERRITE-220 2A
C119 0.1UF 25V X5R
V33A_CTL1
PLACE CLOSE TO Ux PINS44,45
C122 0.1UF 25V X5R
C120 0.1UF 25V X5R
C380 4.7UF 6.3V X5R
C121 0.1UF 25V X5R
C381 4.7UF 6.3V X5R
VOLTAGE SENSE
39,40 VCCINT_SENSE_P
39,41 VCCAUX_SENSE_P
39,42 VCCBRAM_SENSE_P
37,39,43 FPGA_1V5_SENSE_P
39 CTRL1_SHUTDOWN_B
MON1 MON2 MON3 MON4 MON5 MON6 V33DIO1 DVSS1 RESET_B TRCK GPIO1 GPIO2 GPIO3 GPIO4 PMBUS_CLK PMBUS_DATA
C516 0.1UF 25V X5R
V33D_CTL1
NC
U8_RESET_B
PMBus Addr 101
UCD90120ARGC_VQFN64
VQFN_64
RAIL ENABLES
40 VCCINT_EN
42 VCCBRAM_EN
41 VCCAUX_EN
43 FPGA_1V5_EN
14,38,45 PMBUS_CLK
14,38,45 PMBUS_DATA
R379 10.0K
R380 10.0K
R377 10.0K
R376 10.0K
FPWM1_GPIO5 FPWM2_GPIO6 FPWM3_GPIO7 FPWM4_GPIO8 FPWM5_GPIO9 FPWM6_GPIO10 FPWM7_GPIO11 FPWM8_GPIO12 GPIO13 DVSS2 PMBUSALERT_B PMBUS_CTRL GPIO14 GPIO15 PWM1_GPI1 PWM2_GPI2
PMBUS_ALERT
PMBUS_CTRL
14,38
14,38,45
MARGIN TRIM
MARGIN R4's
40 VCCINT_TRIM
41 VCCAUX_TRIM
42 VCCBRAM_TRIM
43 FPGA_1V5_TRIM
R395 3.32K 1%
R397 1.58K 1%
R399 3.74K1%
R398 1.96K1%
C489 2200PF 50V X7R
C493 1000PF 50V X7R
C483 2200PF 50V X7R
C154 1000PF 50V X7R
MARGIN C1's
39 CTRL1_SHUTDOWN_B
CTLR1 SHUTDOWN ENABLE
HI = CLOSE SWITCH, ENABLE S/D
LO = OPEN SWITCH, INHIBIT S/D
N.O. SWITCH
RON=5 OHMS
U8_TRST_B
R374 10.0K 1/10W 1%
CTRL1_PWRGOOD
LOW_PWR_SEL
40
R419 261 1/10W
LED-GRN-SMT
DS6
R413 4.7K 1/16W
Q21
NDS331N
R471 1.00K 1/16W 1%
R470 1.00K 1/16W 1%
CTRL2_SHUTDOWN_B
CTRL2_SEQUENCE_ON
45
CTRL2_PWRGOOD
14,24,45
EN_CTLR1_SHUTDOWN
45
VCCF3V3
R482 10.0K 1/10W 1%
R481 10.0K 1/10W 1%
U68
VCC A B OE GND
NC7SZ66
SC70_5
R483 4.7K 1/16W
CORE,VCCO/DDR3 DIMM POWER
XILINX
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
UCD90120A CTLR #1 ADDR 101
Date: 2-14-2014_14:52
Ver: 2.0
Sheet Size: B
Rev: 02
Sheet 39 of 51
Drawn By DN


VCCINT_SENSE_P
TO CONTROLLER ONLY
(INTERNAL XADC FOR VCCINT)
VCC12_P
L25
FERRITE-78
780ohm @ 25MHz
Note 1: See LMZ31710 datasheet
pg. 26 for Vin and Vout CAP layouts
12V_PWR_IN_LMZ31710_VCCINT
C219 47UF 25V X5R
C216 47UF 25V X5R
C304 22UF 25V X7R
C172 10UF 25V X5R
C124 0.1UF 25V X5R
GND
VCCINT ENABLE
VCCINT_EN = LOW = VCCINT OFF
LMZ31710RVQ
VIN
PVIN1
PVIN2
PVIN3
PVIN4
PVIN5
SYNC_OUT
INH_UVLO
SS_TR
STSEL (ext.TR mode)
OCP_SEL (hiccup)
ILIM (limit=full)
ISHARE
SENSE+
VOUT1
VOUT2
VOUT3
VOUT4
VOUT5
VOUT6
PH1
PH2
PH3
PH4
PH5
PH6
PH7
PH8
PH9
PWRGD
VADJ
RT_CLK
PGND1
PGND2
PGND3
PGND4
PGND5
AGND1
AGND2
DNC1
DNC2
DNC3
RVQ_S_PB3QFN_N42
U49
U49_NC1_SYNC_OUT
VCCINT_EN
U49_CSS_22NF_7MS
U49_NC2_STSEL
U49_NC3_OCP_SEL
U49_NC4_ILIM
U49_NC5_ISHARE
U49_AGND
U49_NC6
U49_NC7
U49_NC8
C471 0.027UF 10V X5R
Css = 27nF
~= 7.0mS
VCC3V3
R209 27.4K 1/10W 1%
Note 2: See LMZ31710
datasheet pg. 26 for PH
copper island layout
WIRE VCCINT_SENSE_P NET Z22=>U49.27 FIRST, THEN U49.27 TO CONTROLLER U8.1
VCCINT_REG_OUT
VCCINT_PWRGD
VCCINT_VADJ
U49_PH
U49_RT_CLK
R496 1.0M 1/10W 5%
Rrt 1000kOhm
U49_AGND
C220 47UF 25V X5R
C200 100UF 6.3V X5R
C199 100UF 6.3V X5R
R183 3W 0.1% 0.005R
PLACE REMOTE SENSE Z-SHORT
CLOSE TO FPGA POWER PIN
Z22 0201_SHORT
VCCINT 1.0V 10A MAX
VCCINT
C198 100UF 6.3V X5R
C197 100UF 6.3V X5R
C212 100UF 6.3V X5R
D3 1N5335BRLG 3.9V 320MA
VCCINT 0A-10A => CS = 0V - 2.01V
G=40.22, Rg=2.55K
R30 2.55K 1%
VCC5V0
C125 0.1UF 25V X5R
U28_RG1
U28_RG2
VCCINT_R_SENSE_N
VCCINT_R_SENSE_P
VCCINT_CS_P
RG1
RG2
VIN_N
VIN_P
V_N
V_P
VOUT
REF
INA333
U28
Z24 0201_SHORT
Z23 0201_SHORT
VCCINT_XADC_SENSE_N
VCCINT_XADC_SENSE_P
R282 261 1/10W
LED-GRN-SMT
DS15
Q6
NDS331N
R22 4.7K 1/16W
Note 3: no AGND-to-PGND connection
per TI power specialist the
LMZ31710 has this connention
internal
MARGIN R3
R400 6.04K 1%
VCCINT_TRIM
LOW-POWER MODE SELECT
LOW_PWR_SEL = HI = NO-TO-COM ON = 0.9V VCCINT
LOW_PWR_SEL = LOW = NC-TO-COM ON = 1.0V VCCINT
LOW_PWR_SEL
TS5A63157
RON=12 OHMS
U11_NO
U11_NC
NO
NC
SEL
VCC
COM
GND
SC70_6
U11
VCCF3V3
Rset 0.9V tuning
R497 DNP
R308 2.87K 1/10W 1%
Rset 1.0V tuning
R498 DNP
R246 2.10K 1/10W 1%
R330 4.7K 1/16W
C5 0.1UF 25V X5R
Note 4: See LMZ31710 datasheet
pg. 26 for Rset resistors + U11
placement close to package
between pins 26 and 23
VCCINT1.0V
XILINX
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
VCCINT REGULATOR
Date: 2-14-2014_14:52
Ver: 2.0
Sheet Size: B
Rev: 02
Sheet 40 of 51
Drawn By DN

VCC12_P

L26
FERRITE-78
12V_PWR_IN_TPS84K_VCCAUX

C127 0.1UF 25V X5R
C230 47UF 25V X5R
C229 47UF 25V X5R
C306 22UF 25V X7R
C179 10UF 25V X5R
GND

Z2
0603_SHORT
See TPS84621 datasheet
pg. 23 for PGND-AGND short

39 VCCAUX_SENSE_P
TO CONTROLLER ONLY
(INTERNAL XADC FOR VCCAUX)
REMOTE SENSE Z-SHORT PLACED
Z26
0201_SHORT
CLOSE TO FPGA POWER PIN
VCCAUX

39 VCCAUX_TRIM
R420
3.16K1%
MARGIN R3
VCCAUX_VADJ

R201
715
1/10W
1%
AGND

VCC3V3
R247
10.0K
1/10W
1%

R302
200K
1/10W
1%
RTCLK_VCCAUX

VCCAUX_POWER_GOOD

39 VCCAUX_EN

LMZ31506RUQ
U53
BQFN_47

1	AGND1	PGND2	37
2	AGND2	PGND1	36
NC 3	DNC1	RT_CLK	35
NC 4	DNC2	AGND3	34
NC 5	DNC3	PWRGD	33
NC 6	SS_TR	DNC13	32 NC
7	STSEL	DNC12	31 NC
8	INH_UVLO1	DNC11	30 NC
9	INH_UVLO2	VOUT7	29
10	PH1	VOUT6	28
11	PH2	VOUT5	27
12	PH3	VOUT4	26
13	PH4	VOUT3	25
14	PH5	VOUT2	24
NC 15	DNC4	DNC10	23 NC

47	46	45	44	43	42	41	40	39	38
VOUT8	PH7	AGND4	SENSE+	VADJ	VIN	PVIN3	PVIN2	PVIN1	PGND3

16	17	18	19	20	21	22			
DNC5	PH6	DNC6	DNC7	DNC8	VOUT1	DNC9			

NC NC NC NC NC
VCCAUX_PH_ISLAND

VCCAUX_REG_OUT
C126 0.1UF 25V X5R
C225 47UF 25V X5R
C224 47UF 25V X5R
C227 47UF 25V X5R
GND

VCC3V3
R283
261
1/10W
LED-GRN-SMT
DS16
VCCAUX
Q7
NDS331N
R23
4.7K
1/16W
GND

AGND

VCCAUX 1.8V 6A MAX
R190
0.005 2W 1%
I1 I1 I2 I2
V1 V1 V2 V2
C221 47UF 25V X5R
C222 47UF 25V X5R
C223 47UF 25V X5R
D4 1N5335BRLG 3.9V 320MA
VCCAUX

VCCAUX 0A-6A => CS = 0V - 2.03V
G=67.67, Rg=1.50K

VCC5V0
R31
1.50K 1%
C128 0.1UF 25V X5R
GND

Z27
0201_SHORT
34 VCCAUX_XADC_SENSE_N
XADC TAP
34 VCCAUX_XADC_SENSE_P
0201_SHORT
Z28

VCCAUX_R_SENSE_N
VCCAUX_R_SENSE_P

1	RG1	RG2	8
2	VIN_N	V_P	7
3	VIN_P	VOUT	6
4	V_N	REF	5

U30 INA333
GND GND

VCCAUX_CS_P 39

VCCAUX 1.8V

XILINX
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCAUX REGULATOR		
Date:	2-14-2014_14:52	Ver:	2.0
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VCC12_P

L24
FERRITE-78
12V_PWR_IN_TPS84K_VCCBRAM

C61 0.1UF 25V X5R
C272 47UF 25V X5R
C273 47UF 25V X5R
C384 22UF 25V X7R
C182 10UF 25V X5R
GND

See TPS84621 datasheet
pg. 23 for PGND-AGND short

Z3
0603_SHORT

39 VCCBRAM_SENSE_P
39 VCCBRAM_TRIM

R421
7.50K1%
MARGIN R3
VCCBRAM_VADJ

R202
5.76K 1%
AGND

TO CONTROLLER ONLY
(INTERNAL XADC FOR VCCBRAM)

VCCBRAM
Z30
0201_SHORT

REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN

VCC3V3
R248
10.0K
1/10W
1%

R465
DNP
DNP
DNP
RTCLK_VCCBRAM

VCCBRAM_POWER_GOOD

LMZ31503RUQ
VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3
47 46 45 44 43 42 41 40 39 38

1 AGND1
2 AGND2
NC 3 DNC1
NC 4 DNC2
NC 5 DNC3
NC 6 SS_TR
7 STSEL
8 INH_UVLO1
9 INH_UVLO2
10 PH1
11 PH2
12 PH3
13 PH4
14 PH5
NC 15 DNC4

37 PGND2
36 PGND1
35 RT_CLK
34 AGND3
33 PWRGD
32NC DNC13
31NC DNC12
30NC DNC11
29 VOUT7
28 VOUT6
27 VOUT5
26 VOUT4
25 VOUT3
24 VOUT2
23NC DNC10

DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9
16 17 18 19 20 21 22
NC NC NC NC NC

U54
BQFN_47

39 VCCBRAM_EN

VCC3V3
R428
261
1/10W
LED-GRN-SMT
DS17

VCCBRAM
Q8
NDS331N
R24
4.7K
1/16W
GND
GND

AGND

VCCBRAM_PH_ISLAND

VCCBRAM_REG_OUT

C131 0.1UF 25V X5R
C241 47UF 25V X5R
C245 47UF 25V X5R
C240 47UF 25V X5R
GND

VCCBRAM 1.0V 3A MAX

R191
0.005
2W 1%
I1 I1 I2 I2
V1 V1 V2 V2

C242 47UF 25V X5R
C243 47UF 25V X5R
C244 47UF 25V X5R

VCCBRAM
D1
1N5335BRLG
3.9V 320MA
GND

VCCBRAM 0A-1.8A => CS = 0V - 1.996V
G=221.7, Rg=453

VCC5V0
R33
453 1%

C129 0.1UF 25V X5R
GND

Z31
0201_SHORT
34 VCCBRAM_XADC_SENSE_N
34 VCCBRAM_XADC_SENSE_P
Z32
0201_SHORT

XADC TAP

VCCBRAM_R_SENSE_N
VCCBRAM_R_SENSE_P

RG1 RG2
VIN_N V_P
VIN_P VOUT
V_N REF
U31
INA333

VCCBRAM_CS_P
39

GND
GND

VCCBRAM 1.0V

XILINX
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCBRAM REGULATOR		
Date:	2-14-2014_14:52	Ver:	2.0
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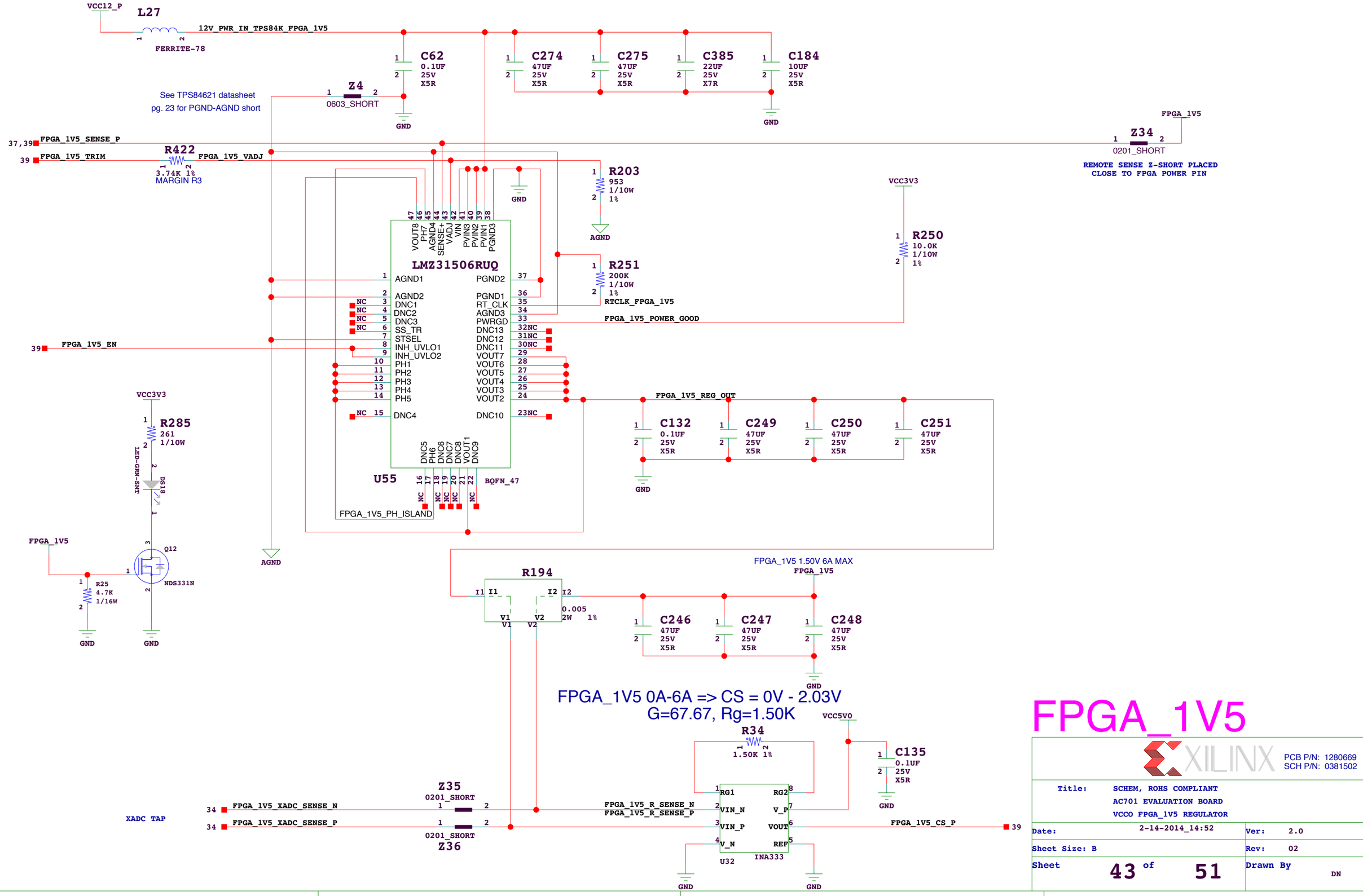
VCC12_P
L27
12V_PWR_IN_TPS84K_FPGA_1V5
FERRITE-78
C62
0.1UF
25V
X5R
C274
47UF
25V
X5R
C275
47UF
25V
X5R
C385
22UF
25V
X7R
C184
10UF
25V
X5R
GND
Z4
0603_SHORT
See TPS84621 datasheet
pg. 23 for PGND-AGND short
FPGA_1V5
Z34
0201_SHORT
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
37,39
FPGA_1V5_SENSE_P
39
FPGA_1V5_TRIM
R422
3.74K 1%
MARGIN R3
FPGA_1V5_VADJ
R203
953
1/10W
1%
AGND
VCC3V3
R250
10.0K
1/10W
1%
LMZ31506RUQ
VOUT8
PH7
AGND4
SENSE+
VADJ
VIN
PVIN3
PVIN2
PVIN1
PGND3
AGND1
AGND2
DNC1
DNC2
DNC3
SS_TR
STSEL
INH_UVLO1
INH_UVLO2
PH1
PH2
PH3
PH4
PH5
DNC4
PGND2
PGND1
RT_CLK
AGND3
PWRGD
DNC13
DNC12
DNC11
VOUT7
VOUT6
VOUT5
VOUT4
VOUT3
VOUT2
DNC10
R251
200K
1/10W
1%
RTCLK_FPGA_1V5
FPGA_1V5_POWER_GOOD
39
FPGA_1V5_EN
VCC3V3
R285
261
1/10W
LED-GRN-SMT
DS18
FPGA_1V5
Q12
NDS331N
R25
4.7K
1/16W
GND
AGND
FPGA_1V5_REG_OUT
C132
0.1UF
25V
X5R
C249
47UF
25V
X5R
C250
47UF
25V
X5R
C251
47UF
25V
X5R
U55
BQFN_47
DNC5
PH6
DNC6
DNC7
DNC8
VOUT1
DNC9
DNC11
DNC12
DNC13
FPGA_1V5_PH_ISLAND
FPGA_1V5 1.50V 6A MAX
R194
0.005
2W
1%
C246
47UF
25V
X5R
C247
47UF
25V
X5R
C248
47UF
25V
X5R
FPGA_1V5 0A-6A => CS = 0V - 2.03V
G=67.67, Rg=1.50K
R34
1.50K 1%
VCC5V0
C135
0.1UF
25V
X5R
Z35
0201_SHORT
Z36
0201_SHORT
34
FPGA_1V5_XADC_SENSE_N
34
FPGA_1V5_XADC_SENSE_P
XADC TAP
FPGA_1V5_R_SENSE_N
FPGA_1V5_R_SENSE_P
RG1
VIN_N
VIN_P
V_N
RG2
V_P
VOUT
REF
INA333
U32
FPGA_1V5_CS_P
39
FPGA_1V5
XILINX
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
VCCO FPGA_1V5 REGULATOR
Date: 2-14-2014_14:52
Ver: 2.0
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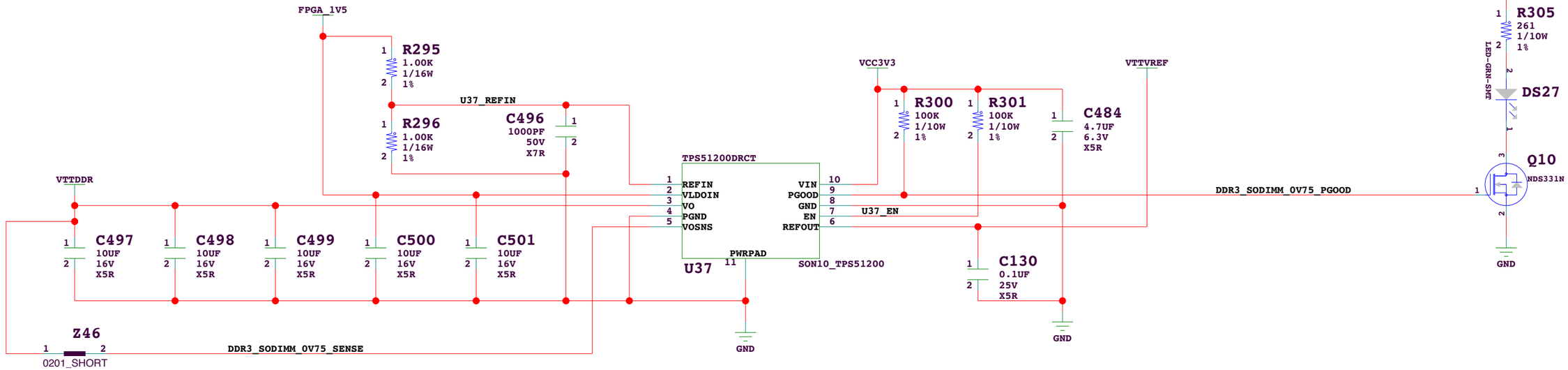
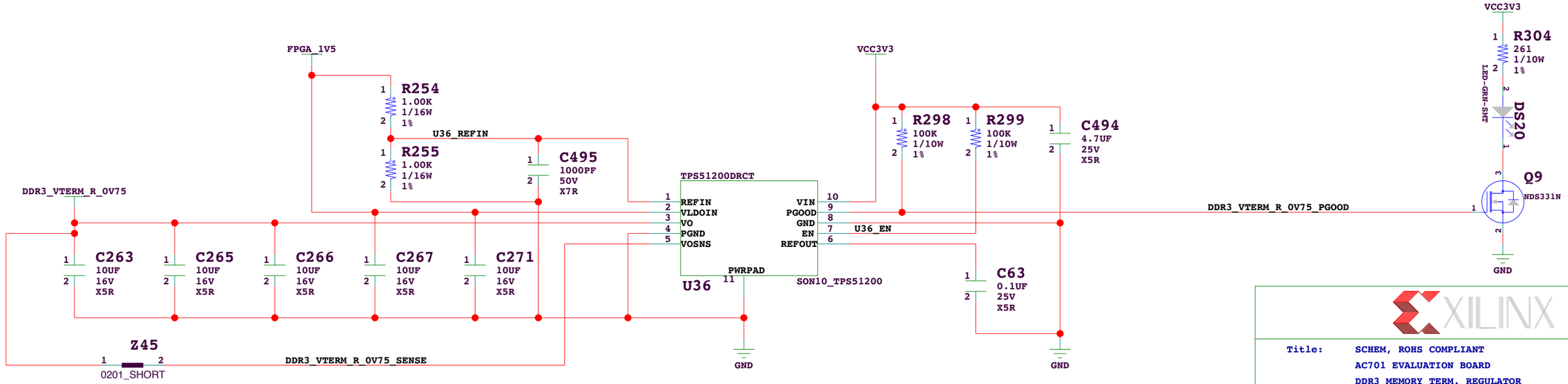
Drawn By DN

DDR3 SODIMM TERM. REGULATOR, 0.75v @ 3A



DDR3 SODIMM MEM. TERM. RESISTOR REGULATOR, 0.75v @ 3A



XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 MEMORY TERM. REGULATOR		
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FPGA 1.8V, FPGA & SYSTEM 3.3V GTP POWER

PMBus Addr 102

UCD90120ARGC_VQFN64
VQFN_64

CURRENT SENSE

CURRENT SENSE FILTERS

Tap into GND close to the SENSE_P pin

VOLTAGE SENSE

Tap into GND close to the SENSE_P pin

RAIL ENABLES

MARGIN TRIM

MARGIN R4's

MARGIN C1's

PLACE CLOSE TO Ux PINS44,45

PCB P/N:	1280669
SCH P/N:	0381502
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD UCD90120A CTLR #2 ADDR 102
Date:	2-14-2014_14:52
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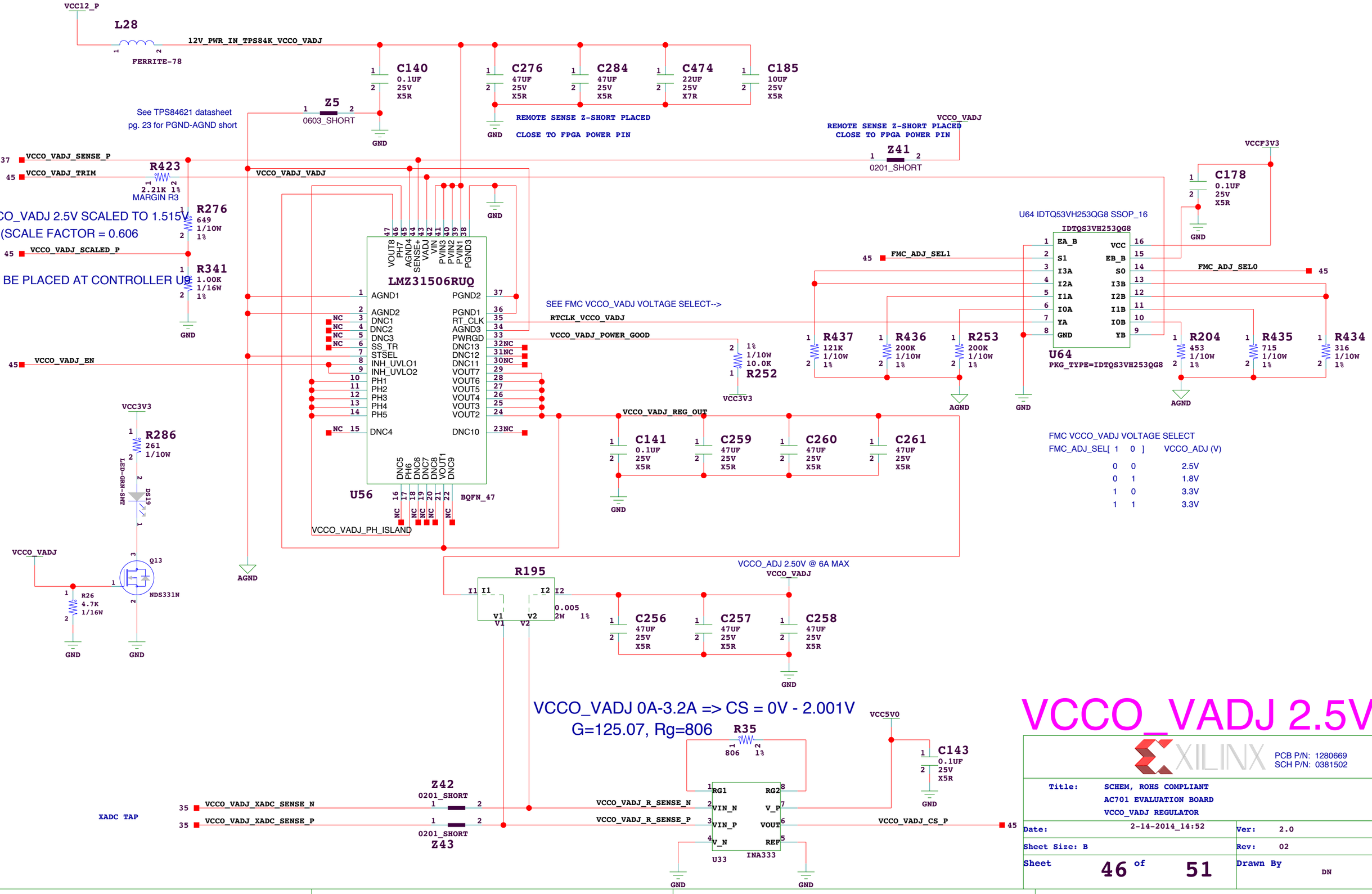
VCC12_P
L28
FERRITE-78
12V_PWR_IN_TPS84K_VCCO_VADJ
C140 0.1UF 25V X5R
C276 47UF 25V X5R
C284 47UF 25V X5R
C474 22UF 25V X7R
C185 10UF 25V X5R
GND
Z5
0603_SHORT
See TPS84621 datasheet
pg. 23 for PGND-AGND short
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
VCCO_VADJ
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
Z41
0201_SHORT
VCCO_VADJ_SENSE_P
VCCO_VADJ_TRIM
R423
2.21K 1%
MARGIN R3
VCCO_VADJ_VADJ
VCCF3V3
C178 0.1UF 25V X5R
VCCO_VADJ 2.5V SCALED TO 1.515V
(SCALE FACTOR = 0.606
R276 649 1/10W 1%
VCCO_VADJ_SCALED_P
R341 1.00K 1/16W 1%
CAN BE PLACED AT CONTROLLER U8
U64 IDTQ53VH253QG8 SSOP_16
IDTQS3VH253QG8
EA_B S1 I3A I2A I1A I0A YA GND
VCC EB_B S0 I3B I2B I1B I0B YB
FMC_ADJ_SEL1
FMC_ADJ_SEL0
R437 121K 1/10W 1%
R436 200K 1/10W 1%
R253 200K 1/10W 1%
R204 453 1/10W 1%
R435 715 1/10W 1%
R434 316 1/10W 1%
U64
PKG_TYPE=IDTQS3VH253QG8
AGND
LMZ31506RUQ
VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3
AGND1 AGND2 DNC1 DNC2 DNC3 SS_TR STSEL INH_UVLO1 INH_UVLO2
PH1 PH2 PH3 PH4 PH5 DNC4
PGND2 PGND1 RT_CLK AGND3 PWRGD DNC13 DNC12 DNC11 VOUT7 VOUT6 VOUT5 VOUT4 VOUT3 VOUT2 DNC10
DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9
U56
BQFN_47
SEE FMC VCCO_VADJ VOLTAGE SELECT-->
RTCLK_VCCO_VADJ
VCCO_VADJ_POWER_GOOD
R252 10.0K 1/10W 1%
VCC3V3
VCCO_VADJ_EN
VCCO_VADJ_REG_OUT
C141 0.1UF 25V X5R
C259 47UF 25V X5R
C260 47UF 25V X5R
C261 47UF 25V X5R
FMC VCCO_VADJ VOLTAGE SELECT
FMC_ADJ_SEL[1 0] VCCO_ADJ (V)
0 0 2.5V
0 1 1.8V
1 0 3.3V
1 1 3.3V
VCC3V3
R286 261 1/10W
LED-GRN-SMT
DS19
VCCO_VADJ
Q13
NDS331N
R26 4.7K 1/16W
VCCO_VADJ_PH_ISLAND
R195
0.005 2W 1%
VCCO_ADJ 2.50V @ 6A MAX
VCCO_VADJ
C256 47UF 25V X5R
C257 47UF 25V X5R
C258 47UF 25V X5R
VCCO_VADJ 0A-3.2A => CS = 0V - 2.001V
G=125.07, Rg=806
R35 806 1%
VCC5V0
C143 0.1UF 25V X5R
Z42
Z43
0201_SHORT
XADC TAP
VCCO_VADJ_XADC_SENSE_N
VCCO_VADJ_XADC_SENSE_P
VCCO_VADJ_R_SENSE_N
VCCO_VADJ_R_SENSE_P
RG1 VIN_N VIN_P V_N RG2 V_P VOUT REF
INA333
U33
VCCO_VADJ_CS_P
VCCO_VADJ 2.5V
XILINX
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
VCCO_VADJ REGULATOR
Date: 2-14-2014_14:52
Ver: 2.0
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Drawn By DN

VCC12_P

L29

12V_PWR_IN_TPS84K_FPGA_1V8

FERRITE-78

C142 0.1UF 25V X5R

C285 47UF 25V X5R

C294 47UF 25V X5R

C475 22UF 25V X7R

C186 10UF 25V X5R

GND

See TPS84621 datasheet
pg. 23 for PGND-AGND short

Z6 0603_SHORT

37,45 FPGA_1V8_SENSE_P

45 FPGA_1V8_TRIM

R424 4.42K 1% MARGIN R3

FPGA_1V8_VADJ

FPGA_1V8

Z48 0201_SHORT

REMOTE SENSE Z-SHORT PLACED CLOSE TO FPGA POWER PIN

R27 1.13K 1/10W 1%

AGND

VCC3V3

R297 10.0K 1/10W 1%

R303 324K 1/10W 1%

RTCLK_FPGA_1V8

FPGA_1V8_POWER_GOOD

LMZ31503RUQ

		VOUT8 47	
		PH7 46	
		AGND4 45	
		SENSE+ 44	
		VADJ 43	
		VIN 42	
		PVIN3 41	
		PVIN2 40	
		PVIN1 39	
		PGND3 38	
1	AGND1	PGND2	37
2	AGND2	PGND1	36
NC 3	DNC1	RT_CLK	35
NC 4	DNC2	AGND3	34
NC 5	DNC3	PWRGD	33
NC 6	SS_TR	DNC13	32NC
7	STSEL	DNC12	31NC
8	INH_UVLO1	DNC11	30NC
9	INH_UVLO2	VOUT7	29
10	PH1	VOUT6	28
11	PH2	VOUT5	27
12	PH3	VOUT4	26
13	PH4	VOUT3	25
14	PH5	VOUT2	24
NC 15	DNC4	DNC10	23NC
	DNC5 16		
	PH6 17		
	DNC6 18		
	DNC7 19		
	DNC8 20		
	VOUT1 21		
	DNC9 22		

U57 BQFN_47

FPGA_1V8_CU_ISLAND

45 FPGA_1V8_EN

SHARED VCC1V8 1.8V 3A SHARED MAX

VCC1V8

C146 0.1UF 25V X5R

C315 47UF 25V X5R

GND

VCC3V3

R287 261 1/10W

LTST-G5RN-SMT

DS26

FPGA_1V8

Q11 NDS331N

R46 4.7K 1/16W

GND

SHARED VCC1V8 1.8V 3A SHARED MAX

FPGA_1V8

R205 0.005 2W 1%

I1 I1 I2 I2

V1 V1 V2 V2

VCC1V8

C145 0.1UF 25V X5R

C307 47UF 25V X5R

C308 47UF 25V X5R

C309 47UF 25V X5R

C310 47UF 25V X5R

C312 47UF 25V X5R

C314 47UF 25V X5R

GND

FPGA_1V8 0A-3.2A => CS = 0V - 2.001V
G=125.07, Rg=806

R197 806 1%

VCC5V0

C144 0.1UF 25V X5R

GND

Z50 0201_SHORT

35 FPGA_1V8_XADC_SENSE_N

XADC TAP

35 FPGA_1V8_XADC_SENSE_P

Z51 0201_SHORT

	RG1 1	RG2	8
FPGA_1V8_R_SENSE_N	VIN_N 2	V_P	7
FPGA_1V8_R_SENSE_P	VIN_P 3	VOUT	6
	V_N 4	REF	5

U39 INA333

FPGA_1V8_CS_P 45

GND GND

VCC1V8 & FPGA_1V8

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA_1V8 REGULATOR		
Date:	2-14-2014_14:52	Ver:	2.0
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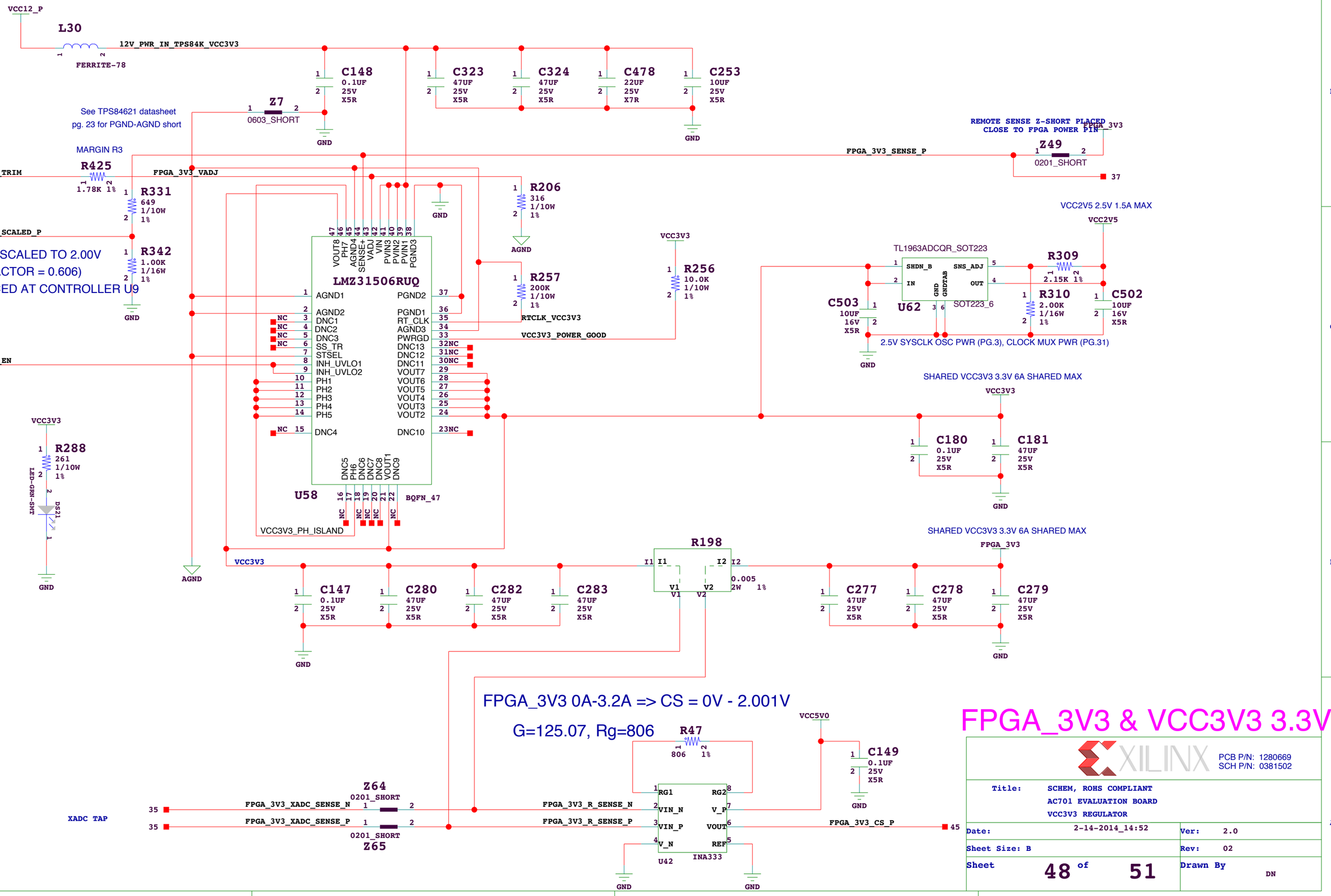
VCC12_P
L30
12V_PWR_IN_TPS84K_VCC3V3
FERRITE-78
C148
0.1UF
25V
X5R
C323
47UF
25V
X5R
C324
47UF
25V
X5R
C478
22UF
25V
X7R
C253
10UF
25V
X5R
GND
Z7
0603_SHORT
See TPS84621 datasheet
pg. 23 for PGND-AGND short
MARGIN R3
R425
1.78K 1%
FPGA_3V3_TRIM
FPGA_3V3_VADJ
FPGA_3V3_SENSE_P
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
FPGA_3V3
Z49
0201_SHORT
R331
649
1/10W
1%
R206
316
1/10W
1%
AGND
FPGA_3V3_SCALED_P
VCC3V3 3.3V SCALED TO 2.00V
(SCALE FACTOR = 0.606)
CAN BE PLACED AT CONTROLLER U9
R342
1.00K
1/16W
1%
LMZ31506RUQ
VOUT8
PH7
AGND4
SENSE+
VADJ
VIN
PVIN3
PVIN2
PVIN1
PGND3
AGND1
AGND2
DNC1
DNC2
DNC3
SS_TR
STSEL
INH_UVLO1
INH_UVLO2
PH1
PH2
PH3
PH4
PH5
DNC4
PGND2
PGND1
RT_CLK
AGND3
PWRGD
DNC13
DNC12
DNC11
VOUT7
VOUT6
VOUT5
VOUT4
VOUT3
VOUT2
DNC10
DNC5
PH6
DNC6
DNC7
DNC8
VOUT1
DNC9
U58
BQFN_47
VCC3V3_PH_ISLAND
R257
200K
1/10W
1%
RTCLK_VCC3V3
VCC3V3_POWER_GOOD
R256
10.0K
1/10W
1%
VCC2V5 2.5V 1.5A MAX
VCC2V5
TL1963ADCQR_SOT223
SHDN_B
IN
GND
GNDTAB
SNS_ADJ
OUT
U62
SOT223_6
R309
2.15K 1%
R310
2.00K
1/16W
1%
C503
10UF
16V
X5R
C502
10UF
16V
X5R
2.5V SYSCLK OSC PWR (PG.3), CLOCK MUX PWR (PG.31)
SHARED VCC3V3 3.3V 6A SHARED MAX
VCC3V3
C180
0.1UF
25V
X5R
C181
47UF
25V
X5R
SHARED VCC3V3 3.3V 6A SHARED MAX
FPGA_3V3
C147
0.1UF
25V
X5R
C280
47UF
25V
X5R
C282
47UF
25V
X5R
C283
47UF
25V
X5R
R198
0.005
2W
1%
C277
47UF
25V
X5R
C278
47UF
25V
X5R
C279
47UF
25V
X5R
FPGA_3V3 0A-3.2A => CS = 0V - 2.001V
G=125.07, Rg=806
R47
806
1%
VCC5V0
C149
0.1UF
25V
X5R
Z64
0201_SHORT
FPGA_3V3_XADC_SENSE_N
FPGA_3V3_XADC_SENSE_P
Z65
0201_SHORT
XADC TAP
RG1
VIN_N
VIN_P
V_N
RG2
V_P
VOUT
REF
INA333
U42
FPGA_3V3_R_SENSE_N
FPGA_3V3_R_SENSE_P
FPGA_3V3_CS_P
R288
261
1/10W
1%
LED-G-RN-SMT
DS21
R288
DS21
FPGA_3V3 & VCC3V3 3.3V
XILINX
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
VCC3V3 REGULATOR
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Drawn By DN

VCC12_P

L31

12V_PWR_IN_TPS84K_MGTAVCC

FERRITE-78

C165 0.1UF 25V X5R

C326 47UF 25V X5R

C327 47UF 25V X5R

C479 22UF 25V X7R

C254 10UF 25V X5R

GND

See TPS84621 datasheet
pg. 23 for PGND-AGND short

Z8 0603_SHORT

MGTAVCC

Z55 0201_SHORT

REMOTE SENSE Z-SHORT PLACED CLOSE TO FPGA POWER PIN

37,45 MGTAVCC_SENSE_P

45 MGTAVCC_TRIM

R426 7.50K1%

MARGIN R3

MGTAVCC_VADJ

R208 5.76K 1%

AGND

VCC3V3

R258 10.0K 1/10W 1%

R259 DNP DNP DNP

RTCLK_MGTAVCC

MGTAVCC_POWER_GOOD

LMZ31503RUQ

1	AGND1	PGND2	37
2	AGND2	PGND1	36
NC 3	DNC1	RT_CLK	35
NC 4	DNC2	AGND3	34
NC 5	DNC3	PWRGD	33
NC 6	SS_TR	DNC13	32NC
7	STSEL	DNC12	31NC
8	INH_UVLO1	DNC11	30NC
9	INH_UVLO2	VOUT7	29
10	PH1	VOUT6	28
11	PH2	VOUT5	27
12	PH3	VOUT4	26
13	PH4	VOUT3	25
14	PH5	VOUT2	24
NC 15	DNC4	DNC10	23NC

VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3

47 46 45 44 43 42 41 40 39 38

DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9

16 17 18 19 20 21 22

NC NC NC NC NC

U59 BQFN_47

MGTAVCC_PH_ISLAND

45 MGTAVCC_EN

VCC3V3

R289 261 1/10W

LED-GRN-SMT

DS24

MGTAVCC

Q16 NDS331N

R28 4.7K 1/16W

GND

AGND

MGTAVCC_REG_OUT

C293 47UF 25V X5R

C292 1UF 16V X5R 0402

C194 1UF 16V X5R 0402

C319 1UF 16V X5R 0402

C162 0.1UF 25V X5R 0402

C287 47UF 6.3V X5R 0805

C288 47UF 6.3V X5R 0805

C289 47UF 6.3V X5R 0805

C290 47UF 6.3V X5R 0805

R199 0.005 2W 1%

I1 I1 I2 I2 V1 V1 V2 V2

C526 0.1UF 25V X5R 0402

C527 0.1UF 25V X5R 0402

C291 47UF 6.3V X5R 0805

C530 100UF 6.3 X5R

C555 100UF 6.3V TANT 0805

MGTAVCC 1.0V 3A MAX

MGTAVCC

D2 1N5335BRLG 3.9V 320MA

TI DERIVED BULK FILTERING TO MEET 10MV MAX RIPPLE

MGTAVCC 0A-3A => CS = 0V - 2.015V
G=134.3, Rg=750

VCC5V0

R48 750 1/10W 1%

C164 0.1UF 25V X5R

GND

Z56 0201_SHORT

Z57 0201_SHORT

XADC TAP

36 MGTAVCC_XADC_SENSE_N

36 MGTAVCC_XADC_SENSE_P

MGTAVCC_R_SENSE_N

MGTAVCC_R_SENSE_P

1	RG1	RG2	8
2	VIN_N	V_P	7
3	VIN_P	VOUT	6
4	V_N	REF	5

U43 INA333

MGTAVCC_CS_P 45

MGTAVCC 1.0V

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

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VCC12_P

L32

12V_PWR_IN_TPS84K_MGTAVTT

FERRITE-78

C171 0.1UF 25V X5R

C382 47UF 25V X5R

C383 47UF 25V X5R

C481 22UF 25V X7R

C262 10UF 25V X5R

GND

See TPS84320 datasheet
pg. 24 for PGND-AGND short

Z9 0603_SHORT

MGTAVTT

Z59 0201_SHORT

REMOTE SENSE Z-SHORT PLACED CLOSE TO FPGA POWER PIN

37,45 MGTAVTT_SENSE_P

45 MGTAVTT_TRIM

R427 6.19K 1%

MARGIN R3

MGTAVTT_VADJ

R207 2.87K 1/10W 1%

AGND

R262 324K 1/10W 1%

RTCLK_MGTAVTT

VCC3V3

R260 10.0K 1/10W 1%

MGTAVTT_POWER_GOOD

LMZ31503RUQ

VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3

47 46 45 44 43 42 41 40 39 38

1	AGND1	PGND2	37
2	AGND2	PGND1	36
NC 3	DNC1	RT_CLK	35
NC 4	DNC2	AGND3	34
NC 5	DNC3	PWRGD	33
NC 6	SS_TR	DNC13	32 NC
7	STSEL	DNC12	31 NC
8	INH_UVLO1	DNC11	30 NC
9	INH_UVLO2	VOUT7	29
10	PH1	VOUT6	28
11	PH2	VOUT5	27
12	PH3	VOUT4	26
13	PH4	VOUT3	25
14	PH5	VOUT2	24
NC 15	DNC4	DNC10	23 NC

DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9

16 17 18 19 20 21 22

NC NC NC NC NC

U60 BQFN_47

MGTAVTT_PH_ISLAND

45 MGTAVTT_EN

VCC3V3

R290 261 1/10W

LED-GRN-SMT DS25

MGTAVTT

Q18 NDS331N

R29 4.7K 1/16W

GND GND

AGND

MGTAVTT_REG_OUT

C296 47UF 25V X5R

C196 1UF 16V X5R 0402

C551 1UF 16V X5R 0402

C552 1UF 16V X5R 0402

C170 0.1UF 25V X5R 0402

C297 47UF 6.3V X5R 0805

C298 47UF 6.3V X5R 0805

C299 47UF 6.3V X5R 0805

C302 47UF 6.3V X5R 0805

GND

TI DERIVED BULK FILTERING TO MEET 10MV MAX RIPPLE

R200 0.005 2W 1%

I1 I1 I2 I2 V1 V1 V2 V2

C529 0.1UF 25V X5R 0402

C528 0.1UF 25V X5R 0402

C303 47UF 6.3V X5R 0805

C531 100UF 6.3 X5R

C556 100UF 6.3V TANT 0805

MGTAVTT 1.2V 3A MAX

MGTAVTT

D7 1N5335BRLG 3.9V 320MA

GND

MGTAVTT 0A-1.5A => CS = 0V - 2.013V
G=268.4, Rg=374

R49 374 1%

VCC5V0

C166 0.1UF 25V X5R

GND

XADC TAP

36 MGTAVTT_XADC_SENSE_N

36 MGTAVTT_XADC_SENSE_P

Z60 0201_SHORT

Z61 0201_SHORT

MGTAVTT_R_SENSE_N

MGTAVTT_R_SENSE_P

1	RG1	RG2	8
2	VIN_N	V_P	7
3	VIN_P	VOUT	6
4	V_N	REF	5

U47 INA333

GND GND

MGTAVTT_CS_P 45

MGTAVTT 1.2V

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
MGTAVTT REGULATOR

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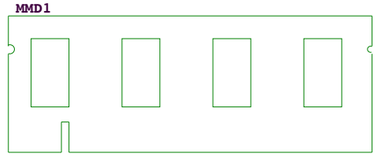
MMD1



DDR3_SODIMM

CBL1

4-Pin ATX Power

6-Pin Molex Mini-fit Jr.

PCIe Adapter Cable

PCIE_ADAPTER_CABLE

CBL2

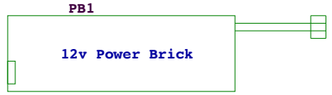
110V Prong

IEC320-C13

Power Cord

PC_POWER_CABLE

PB1



PWR_BRICK_12V

CBL3

USB A

USB Mini-B

USB Mini-B Cable

USB_MINIB_CABLE

CBL4

USB A

USB Mini-B

USB Micro-B Cable

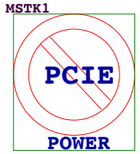
USB_MICRO_CABLE

PL1

AC701_PCIE_PLATE

MANF=PURCELL
MANF_P/N=P1155-0003

MSTK1



PCIE_POWER_STICKER

MJB1 JUMPER_BLOCK_2-PIN
MJB2 JUMPER_BLOCK_2-PIN
MJB3 JUMPER_BLOCK_2-PIN
MJB4 JUMPER_BLOCK_2-PIN
MJB5 JUMPER_BLOCK_2-PIN
MJB6 JUMPER_BLOCK_2-PIN
MJB7 JUMPER_BLOCK_2-PIN
MJB8 JUMPER_BLOCK_2-PIN
MJB9 JUMPER_BLOCK_2-PIN
MJB10 JUMPER_BLOCK_2-PIN
MJB11 JUMPER_BLOCK_2-PIN
MJB12 JUMPER_BLOCK_2-PIN
MJB13 JUMPER_BLOCK_2-PIN
MJB14 JUMPER_BLOCK_2-PIN
MJB15 JUMPER_BLOCK_2-PIN

MS1 MACHINE_SCREW_4-40
MSO1 STANDOFF_0P375
MRB1 RUBBER_BUMPER
MS13 MACHINE_SCREW_4-40
MH_125_250 MH1 GND

MS2 MACHINE_SCREW_4-40
MSO2 STANDOFF_0P375
MRB2 RUBBER_BUMPER
MS14 MACHINE_SCREW_4-40
MH_125_250 MH2 GND

MS3 MACHINE_SCREW_4-40
MSO3 STANDOFF_0P375
MRB3 RUBBER_BUMPER
MS15 MACHINE_SCREW_4-40
MH_125_250 MH3 GND

MS4 MACHINE_SCREW_4-40
MSO4 STANDOFF_0P375
MRB4 RUBBER_BUMPER
MS16 MACHINE_SCREW_4-40
MH_125_250 MH4 GND

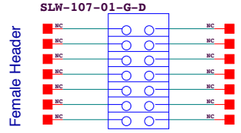
MS5 MACHINE_SCREW_4-40
MSO5 STANDOFF_0P375
MRB5 RUBBER_BUMPER
MS17 MACHINE_SCREW_4-40
MH_125_250 MH5 GND

MS6 MACHINE_SCREW_4-40
MSO6 STANDOFF_0P375
MRB6 RUBBER_BUMPER
MS18 MACHINE_SCREW_4-40
MH_125_250 MH6 GND

LCD Display Assembly

SLW-107-01-G-D

Female Header



LCD1_J11

LCD1

LCD Mounting HW

STANDOFF_10MM MSO9
MACHINE_SCREW_M2_5 MS12
MACHINE_SCREW_M2_5 MS9
MH_110_135 MH9 GND

STANDOFF_10MM MSO7
MACHINE_SCREW_M2_5 MS7
MACHINE_SCREW_M2_5 MS10
MH_110_135 MH7 GND

STANDOFF_10MM MSO8
MACHINE_SCREW_M2_5 MS8
MACHINE_SCREW_M2_5 MS11
MH_110_135 MH8 GND

Mechanical Components

XILINX

PCB P/N: 1280669
SCH P/N: 0381502

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