

Data Sheet

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Pin Assignments

Table 1. Pin Assignments

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{REFDQ}	53	DQ19	105	V _{DD}	157	DQ42	2	V _{SS}	54	V _{SS}	106	V _{DD}	158	DQ46
3	V _{SS}	55	V _{SS}	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V _{SS}	6	DQ5	58	DQ29	110	RAS#	162	V _{SS}
7	DQ1	59	DQ25	111	V _{DD}	163	DQ48	8	V _{SS}	60	V _{SS}	112	V _{DD}	164	DQ52
9	V _{SS}	61	V _{SS}	113	WE#	165	DQ49	10	DQS0#	62	DQ3#	114	S0#	166	DQ53

11	DM0	63	DM3	115	CAS#	167	V _{SS}	12	DQS0	64	DQ3	116	ODT0	168	V _{SS}
13	V _{SS}	65	V _{SS}	117	V _{DD}	169	DQS6#	14	V _{SS}	66	V _{SS}	118	V _{DD}	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	NC	172	V _{SS}
17	DQ3	69	DQ27	121	NC	173	V _{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V _{SS}	71	V _{SS}	123	V _{DD}	175	DQ50	20	V _{SS}	72	V _{SS}	124	V _{DD}	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	NC	126	V _{REFCA}	178	V _{SS}
23	DQ9	75	V _{DD}	127	V _{SS}	179	V _{SS}	24	DQ13	76	V _{DD}	128	V _{SS}	180	DQ60
25	V _{SS}	77	NC	129	DQ32	181	DQ56	26	V _{SS}	78	A15	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	V _{SS}
29	DQS1	81	V _{DD}	133	V _{SS}	185	V _{SS}	30	RESET#	82	V _{DD}	134	V _{SS}	186	DQS7#
31	V _{SS}	83	A12	135	DQS4#	187	DM7	32	V _{SS}	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V _{SS}	34	DQ14	86	A7	138	V _{SS}	190	V _{SS}
35	DQ11	87	V _{DD}	139	V _{SS}	191	DQ58	36	DQ15	88	V _{DD}	140	DQ38	192	DQ62
37	V _{SS}	89	A8	141	DQ34	193	DQ59	38	V _{SS}	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V _{SS}	40	DQ20	92	A4	144	V _{SS}	196	V _{SS}
41	DQ17	93	V _{DD}	145	V _{SS}	197	SA0	42	DQ21	94	V _{DD}	146	DQ44	198	NF
43	V _{SS}	95	A3	147	DQ40	199	V _{DDSPD}	44	V _{SS}	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V _{SS}	202	SCL
47	DQS2	99	V _{DD}	151	V _{SS}	203	V _{TT}	48	V _{SS}	100	V _{DD}	152	DQS5#	204	V _{TT}
49	V _{SS}	101	CK0	153	DM5	-	-	50	DQ22	102	CK1	154	DQS5	-	-
51	DQ18	103	CK0#	155	V _{SS}	-	-	52	DQ23	104	CK1#	156	V _{SS}	-	-

Products and specifications discussed herein are subject to change by Micron without notice. This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Pin Descriptions

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Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 1. Pin Descriptions

Symbol	Type	Description
Ax	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	Bank address inputs: Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	Clock: Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
		Clock enable: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks

CKEx	Input	on the DRAM.
DMx	Input	Data mask (x8 devices only): DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	On-die termination: Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	Parity input: Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	Reset: RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	Chip select: Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I ² C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I ² C bus.
CBx	I/O	Check bits: Used for system error detection and correction.
DQx	I/O	Data input/output: Bidirectional data bus.
DQSx, DQSx#	I/O	Data strobe: Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.
SDA	I/O	Serial data: Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I ² C bus.
TDQSx, TDQSx#	Output	Redundant data strobe (x8 devices only): TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	Parity error output: Parity error found on the command and address bus.
EVENT#	Output (open drain)	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V _{DD}	Supply	Power supply: 1.5V ±0.075V. The component V _{DD} and V _{DDQ} are connected to the module V _{DD} .
V _{DDSPD}	Supply	Temperature sensor/SPD EEPROM power supply: 3.0–3.6V.
V _{REFCA}	Supply	Reference voltage: Control, command, and address V _{DD} /2.
V _{REFDQ}	Supply	Reference voltage: DQ, DM V _{DD} /2.
V _{SS}	Supply	Ground.
V _{TT}	Supply	Termination voltage: Used for control, command, and address V _{DD} /2.
NC	–	No connect: These pins are not connected on the module.
NF	–	No function: These pins are connected within the module, but provide no functionality.

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