EmbHardw Exercises

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Contents

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1.1 Design Unit Hierarchy

This inheritance list is sorted roughly, but not completely, alphabetically:

Chapter 2

Design Unit Index

2.1 Design Unit List

Here is a list of all design unit members with links to the Entities they belong to:

Chapter 3

File Index

3.1 File List

Here is a list of all documented files with brief descriptions:

Chapter 4

Class Documentation

4.1 behavioural Architecture Reference

Processes

- edgeDetect(**Reset_NRI , Clk_CI**)
- nextState(**Clk_CI , Reset_NRI**)
- logic(**Clk_CI , Push_Edge_D , Pop_Edge_D , numEl_D**)

Types

- **state_T(stateReset,stateEmpty,stateFilling,stateFull)**
- **memory_T(SIZE- 1 downto 0)std_logic_vector(15 downto 0)**

Signals

- stateNext_D **state_T**
- statePres_D **state_T**
- data_D **memory_T**
- numEl_D **natural**
- head_D **natural**
- tail_D **natural**
- Push_Edge_D **std_logic**
- Push_Last_D **std_logic**
- Pop_Edge_D **std_logic**
- Pop_Last_D **std_logic**

The documentation for this class was generated from the following file:

- fifo.vhdl

4.2 behavioural Architecture Reference

Processes

- clk_process( )
- stim_proc( )

Components

- FIFO

Constants

- TimeMax_C **time:=** 1000 **ns**
- Clk_period_C **time:=** 20 **ns**

Signals

- Clk_S **std_logic**
- Reset_NR **std_logic**
- Push_S **std_logic**
- Pop_S **std_logic**
- DataPush_D **std_logic_vector(** 15 **downto** 0 **)**
- DataPop_D **std_logic_vector(** 15 **downto** 0 **)**
- Full_S **std_logic**
- Empty_S **std_logic**
- Time_S **time:=** 0 **ns**

Instantiations

- dut **FIFO**

The documentation for this class was generated from the following file:

- testbenchFifo.vhdl

4.3 behavioural Architecture Reference

Processes

- clk_process( )
- stim_proc( )

Components

- LcdDriver

Constants

- TimeMax_C **time:= 1000 ns**
- Clk_period_C **time:= 20 ns**

Signals

- Clk_S **std_logic**
- Reset_NR **std_logic**
- Address_D **std_logic_vector(1 downto 0)**
- Write_S **std_logic**
- WriteData_D **std_logic_vector(15 downto 0)**
- Read_S **std_logic**
- ByteEnable_D **std_logic**
- BeginBurstTransfer_D **std_logic**
- BurstCount_D **std_logic_vector(7 downto 0)**
- WaitReq_S **std_logic**
- ReadData_D **std_logic_vector(15 downto 0)**
- DB_D **std_logic_vector(15 downto 0)**
- Rd_NS **std_logic**
- Wr_NS **std_logic**
- Cs_NS **std_logic**
- DC_NS **std_logic**
- LcdReset_NR **std_logic**
- IM0_S **std_logic**
- Time_S **time:= 0 ns**

Instantiations

- lcd **LcdDriver**

The documentation for this class was generated from the following file:

- testbenchLcd.vhdl

4.4 behavioural Architecture Reference

The documentation for this class was generated from the following file:

- reader.vhdl

4.5 behavioural Architecture Reference

Processes

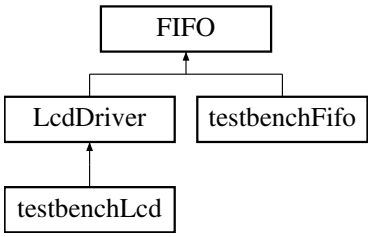
- pRegWrite**(Clk_Cl)**

The documentation for this class was generated from the following file:

- writer.vhdl

4.6 FIFO Entity Reference

Inheritance diagram for FIFO:



Entities

- behavioural architecture

Libraries

- ieee

Use Clauses

- std_logic_1164
- numeric_std
- std_logic_unsigned

Generics

- SIZE **natural:=** 256

Ports

- Clk_CI **in std_logic**
- Reset_NRI **in std_logic**
- Push_SI **in std_logic**
- Pop_SI **in std_logic**
- Data_DI **in std_logic_vector(** 15 **downto** 0 **)**
- Data_DO **out std_logic_vector(** 15 **downto** 0 **)**
- Full_SO **out std_logic**
- Empty_SO **out std_logic**

The documentation for this class was generated from the following file:

- fifo.vhdl

4.7 LCD Architecture Reference

Processes

- edgeDetect(**Reset_NRI , Clk_CI**)
- nextStateRx(**Clk_CI , Reset_NRI**)
- logicRx(**Clk_CI , RxStatePres_D , FifoFull_D , Write_Edge_D , RxData_D**)
- nextStateTx(**Clk_CI , Reset_NRI**)
- logicTx(**Clk_CI , TxStatePres_D , FifoEmpty_D**)

Components

- FIFO

Types

- **RxState_T(RxStateReset,RxStateIdle,RxStateRxPrePushCmd,RxStateRxPrePushDataIdentifier,Rx↩ StateRxPrePushData,RxStateRxPostPushDataIdentifier,RxStateRxPostPush)**
- **TxState_T(TxStateReset,TxStateDispReset,TxStateIdle,TxStatePreTx,TxStateTx,TxStatePostTx)**

Signals

- RxStateNext_D **RxState_T:=RxStateReset**
- TxStateNext_D **TxState_T:=TxSTateReset**
- RxStatePres_D **RxState_T:=RxStateReset**
- TxStatePres_D **TxState_T:=TxSTateReset**
- Pop_S **std_logic**
- Push_S **std_logic**
- RxData_D **std_logic_vector(15 downto 0)**
- TxData_D **std_logic_vector(15 downto 0)**
- FifoFull_D **std_logic**
- FifoEmpty_D **std_logic**
- IsData_D **std_logic**
- BitEnable_D **std_logic_vector(15 downto 0)**
- Write_Edge_D **std_logic**
- Write_Last_D **std_logic**
- Read_Edge_D **std_logic**
- Read_Last_D **std_logic**

Instantiations

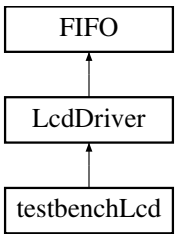
- databuffer **FIFO**

The documentation for this class was generated from the following file:

- lcdDriver.vhdl

4.8 LcdDriver Entity Reference

Inheritance diagram for LcdDriver:



Entities

- LCD architecture

Libraries

- ieee

Use Clauses

- std_logic_1164
- numeric_std

Ports

- Clk_CI **in std_logic**
- Reset_NRI **in std_logic**
- Address_DI **in std_logic_vector(1 downto 0)**
- Write_SI **in std_logic**
- WriteData_DI **in std_logic_vector(15 downto 0)**
- Read_SI **in std_logic**
- ByteEnable_DI **in std_logic_vector(1 downto 0)**
- BeginBurstTransfer_DI **in std_logic**
- BurstCount_DI **in std_logic_vector(7 downto 0)**
- WaitReq_SO **out std_logic**
- ReadData_DO **out std_logic_vector(15 downto 0)**
- ReadDataValid_SO **out std_logic**
- DB_DIO **inout std_logic_vector(15 downto 0)**
- Rd_NSO **out std_logic**
- Wr_NSO **out std_logic**
- Cs_NSO **out std_logic**
- DC_NSO **out std_logic**
- LcdReset_NRO **out std_logic**
- IM0_SO **out std_logic**

The documentation for this class was generated from the following file:

- lcdDriver.vhdl

4.9 reader Entity Reference

Entities

- behavioural architecture

Libraries

- ieee

Use Clauses

- std_logic_1164

Ports

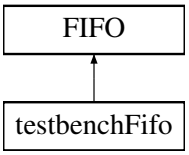
- Clk_CI **in std_logic**
- Address_DI **in std_logic_vector(2 downto 0)**
- Read_SI **in std_logic**
- RegDir_DI **in std_logic_vector(7 downto 0)**
- RegPort_DI **in std_logic_vector(7 downto 0)**
- RegPin_DI **in std_logic_vector(7 downto 0)**
- ReadData_DO **out std_logic_vector(7 downto 0)**

The documentation for this class was generated from the following file:

- reader.vhdl

4.10 testbenchFifo Entity Reference

Inheritance diagram for testbenchFifo:



Entities

- behavioural architecture

Libraries

- ieee

Use Clauses

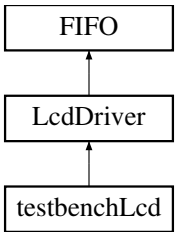
- std_logic_1164

The documentation for this class was generated from the following file:

- testbenchFifo.vhdl

4.11 testbenchLcd Entity Reference

Inheritance diagram for testbenchLcd:



Entities

- behavioural architecture

Libraries

- ieee

Use Clauses

- std_logic_1164

The documentation for this class was generated from the following file:

- testbenchLcd.vhdl

4.12 writer Entity Reference

Entities

- behavioural architecture

Libraries

- ieee

Use Clauses

- std_logic_1164

Ports

- Clk_CI **in std_logic**
- Address_DI **in std_logic_vector(2 downto 0)**
- Write_SI **in std_logic**
- WriteData_DI **in std_logic_vector(7 downto 0)**
- RegDir_DO **out std_logic_vector(7 downto 0)**
- RegPort_DIO **inout std_logic_vector(7 downto 0)**
- IRQCtrl_SO **out std_logic**
- IRQState_SO **out std_logic**

The documentation for this class was generated from the following file:

- writer.vhdl

Chapter 5

File Documentation

5.1 lcdDriver.vhdl File Reference

LCD driver. Translates avalon bus data and commands to the LCD interface.

Entities

- LcdDriver entity
- LCD architecture

5.1.1 Detailed Description

LCD driver. Translates avalon bus data and commands to the LCD interface.

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