

Legend

Connectors

Internal Features

External Components

Power

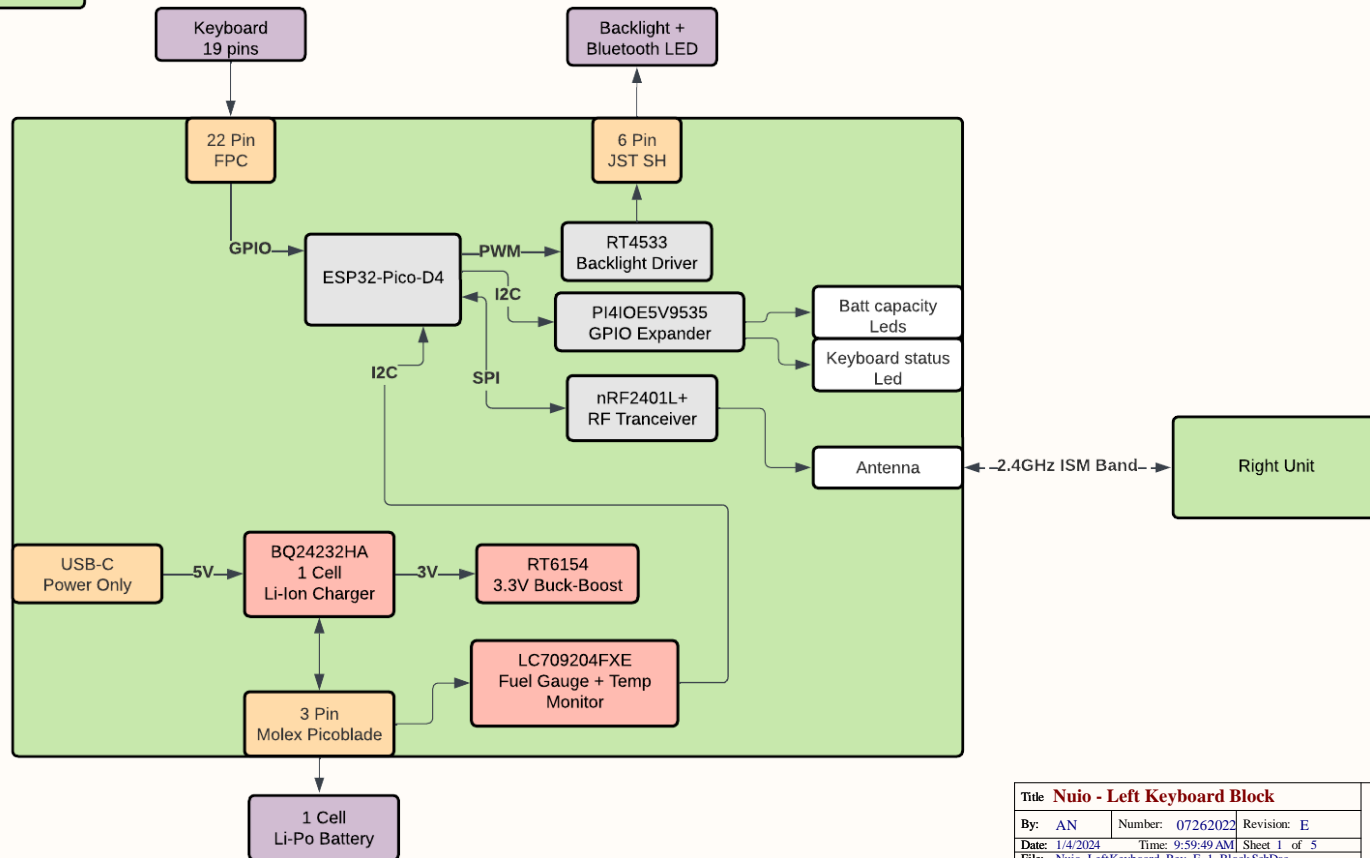
ICs

PCB

Nuio Block Diagram

11/20/2023

Left Unit Rev E



Title: **Nuio - Left Keyboard Block**

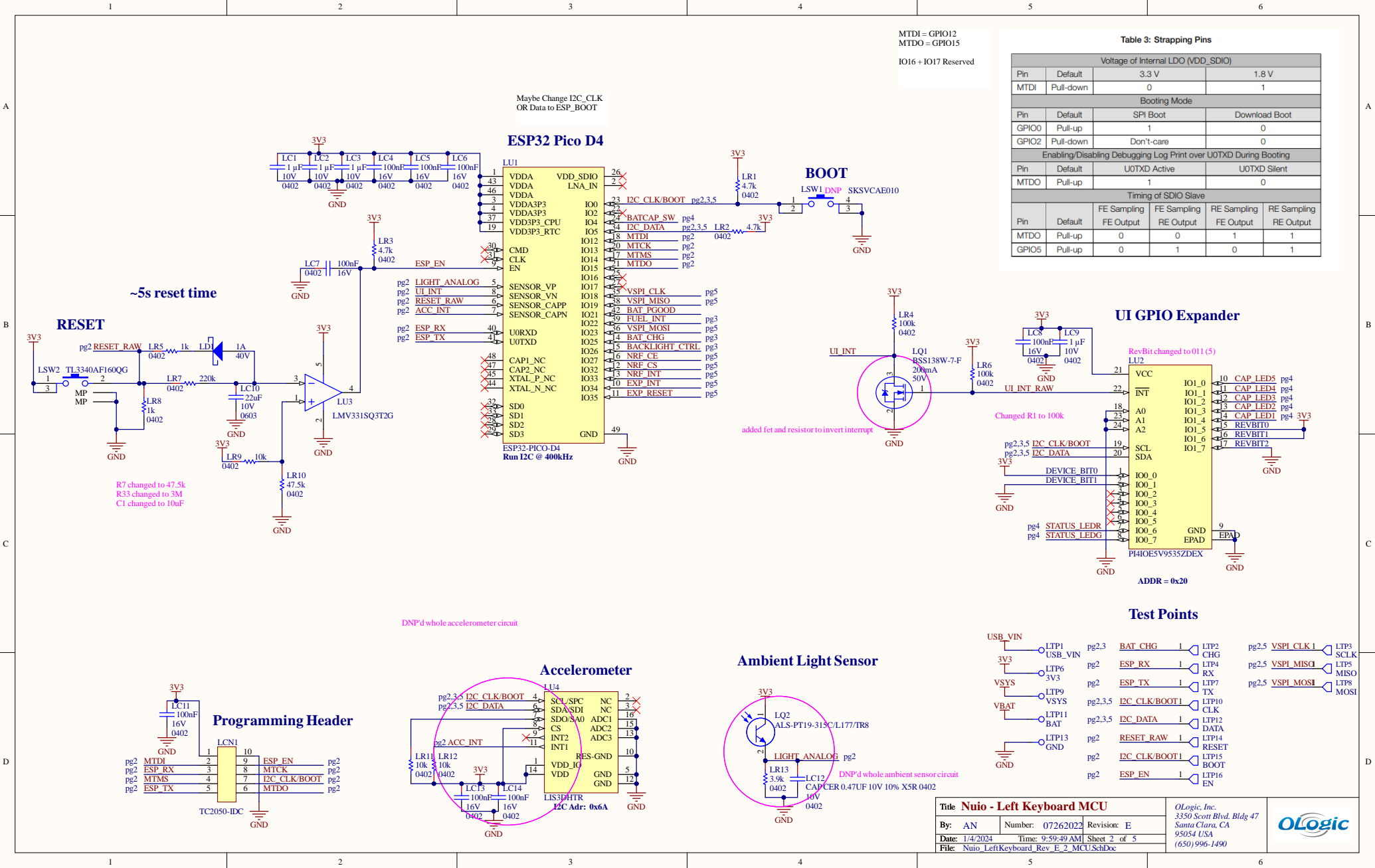
By: **AN** Number: **07262023** Revision: **E**

Date: **1/4/2024** Time: **9:59:49 AM** Sheet **1** of **5**

File: **Nuio_LeftKeyboard_Rev_E_1_Block.SchDoc**

OLogic, Inc.
3350 Scott Blvd. Bldg 47
Santa Clara, CA
95054 USA
(650) 996-1490





MTDI = GPIO12
MTDO = GPIO15
IO16 + IO17 Reserved

Table 3: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V	1.8 V		
MTDI	Pull-down	0	1		
Booting Mode					
Pin	Default	SPI Boot	Download Boot		
GPIO0	Pull-up	1	0		
GPIO2	Pull-down	Don't-care	0		
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active	U0TXD Silent		
MTDO	Pull-up	1	0		
Timing of SDIO Slave					
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

UI GPIO Expander

RevBit changed to 011 (5)

ADDR = 0x20

Test Points

TitleNuio - Left Keyboard MCU

By: AN

Date: 1/4/2024

File: Nuio_LeftKeyboard_Rev_E_2_MCU.SchDoc

Number: 07262023

Time: 9:59:49 AM

Sheet 2 of 5

Revision: E


OLogic, Inc.

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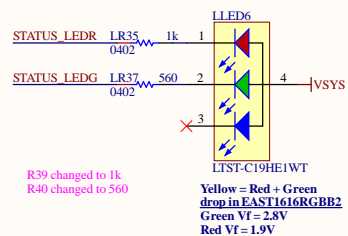
Santa Clara, CA

95054 USA

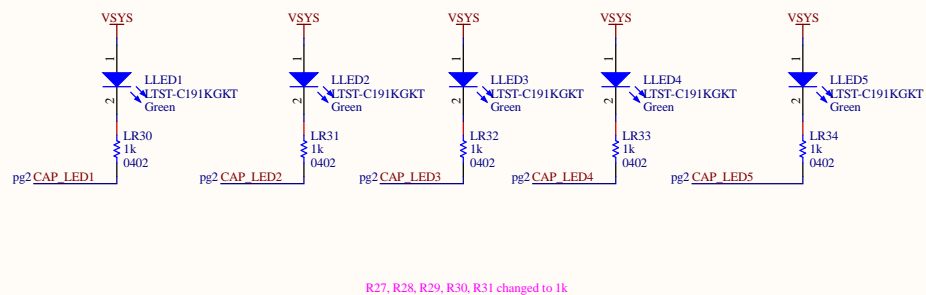
(650) 996-1490

Title Nuio - Left Keyboard Power			<i>OLogic, Inc.</i> 3350 Scott Blvd. Bldg 47 Santa Clara, CA 95054 USA (650) 996-1490		
By: AN	Number: 07262022	Revision: E			
Date: 1/4/2024	Time: 9:59:49 AM	Sheet 3 of 5			
File: Nuio_LeftKeyboard_Rev_E_3_PowerSchDoc					

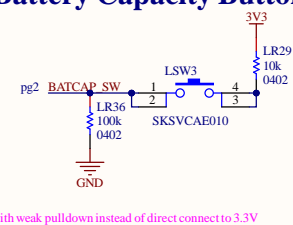
Status LEDs




Battery Capacity LEDS



Battery Capacity Button



Title Nuio - Left Keyboard UI			<i>OLogic, Inc.</i> 3350 Scott Blvd. Bldg 47 Santa Clara, CA 95054 USA (650) 996-1490	
By: AN	Number: 07262022	Revision: E		
Date: 1/4/2024	Time: 9:59:50 AM Sheet 4 of 5			
File: Nuio_LeftKeyboard_Rev E.4_UI_SchDoc				

ISM Band Transceiver/Receiver

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFOs. Will empty all levels in TX FIFOs ^a .
TX mode	1	0	Minimum 10µs high pulse	Data in TX FIFOs. Will empty one level in TX FIFOs ^b .
Standby-II	1	0	1	TX FIFO empty.
Standby-I	1	-	0	No ongoing packet transmission.
Power Down	0	-	-	-

- a. If **CE** is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the **CE** is still high, nRF24L01+ enters standby-II mode. In this mode the transmission of a packet is started as soon as the **CSN** is set high after an upload (UL) of a packet to TX FIFO.
- b. This operating mode pulses the **CE** high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitted, the nRF24L01+ enters standby-I mode.

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFOs. Will empty all levels in TX FIFOs ^a .
TX mode	1	0	Minimum 10µs high pulse	Data in TX FIFOs. Will empty one level in TX FIFOs ^b .
Standby-II	1	0	1	TX FIFO empty.
Standby-I	1	-	0	No ongoing packet transmission.
Power Down	0	-	-	-

- a. If **CE** is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the **CE** is still high, nRF24L01+ enters standby-II mode. In this mode the transmission of a packet is started as soon as the **CSN** is set high after an upload (UL) of a packet to TX FIFO.
- b. This operating mode pulses the **CE** high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitted, the nRF24L01+ enters standby-I mode.

Membrane Keyboards how they work

