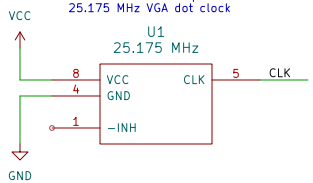
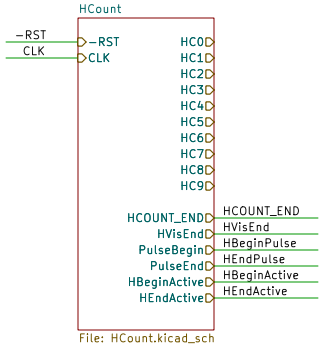
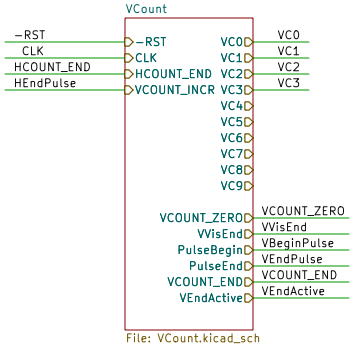
Oscillator module to produce
25.175 MHz VGA dot clock



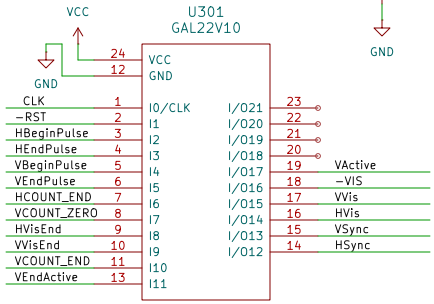
Horizontal count

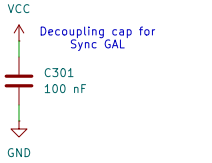


Vertical count

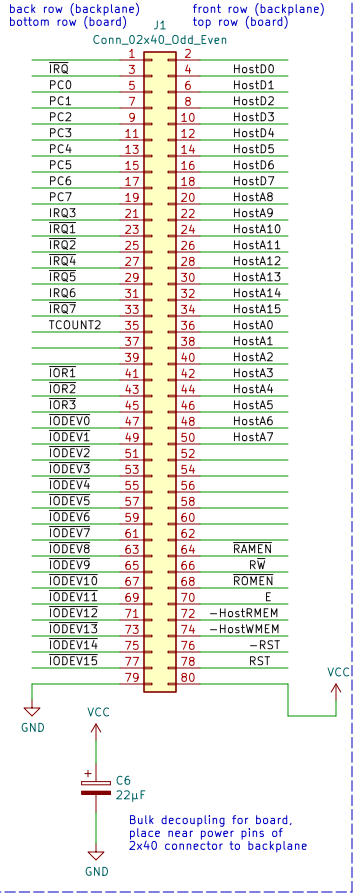


Sync gen and visibility signals:
Logic is in Sync.pld

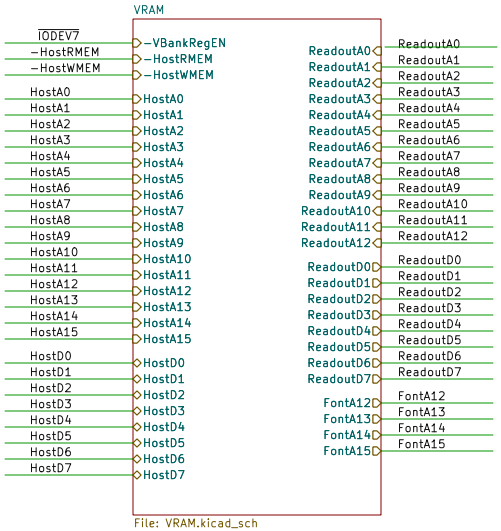




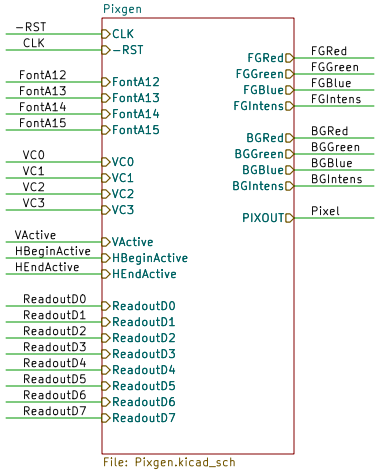
Backplane connector: one per board PCB
(appears here because all backplane signals
exist on this sheet)



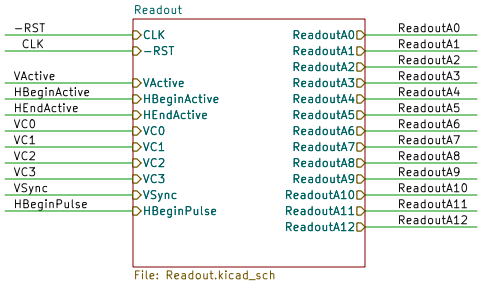
VRAM (video memory for
character and attribute data)



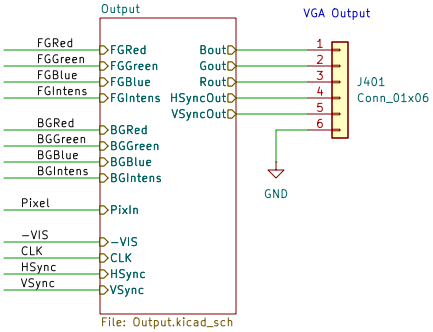
Pixel generation (using data from VRAM,
generate sequence of pixel fg/bg values
along with fg/bg color information
to send to Output module for display)



Readout module (generate addresses
for reading character and attribute
data from VRAM)



Video output
(to VGA monitor)

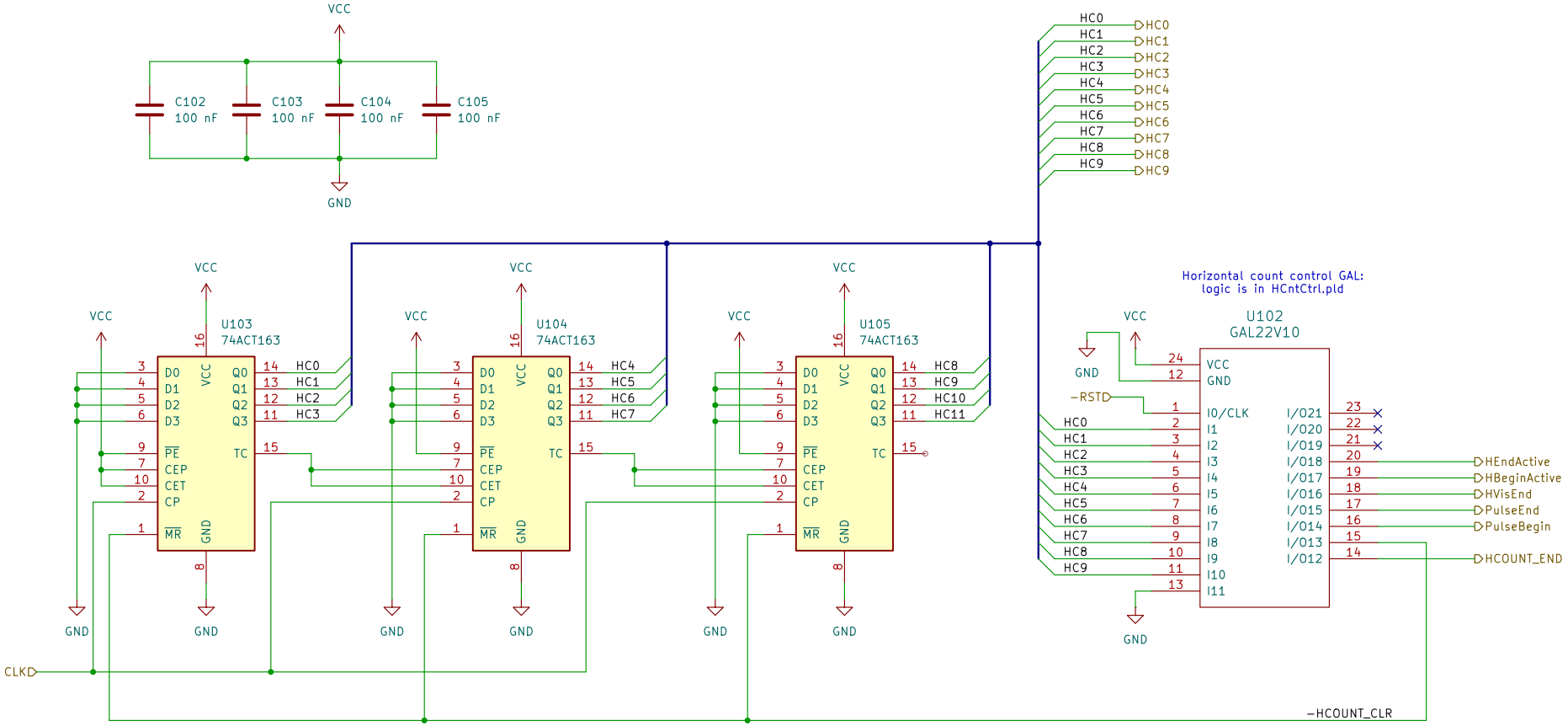


daveho hacks

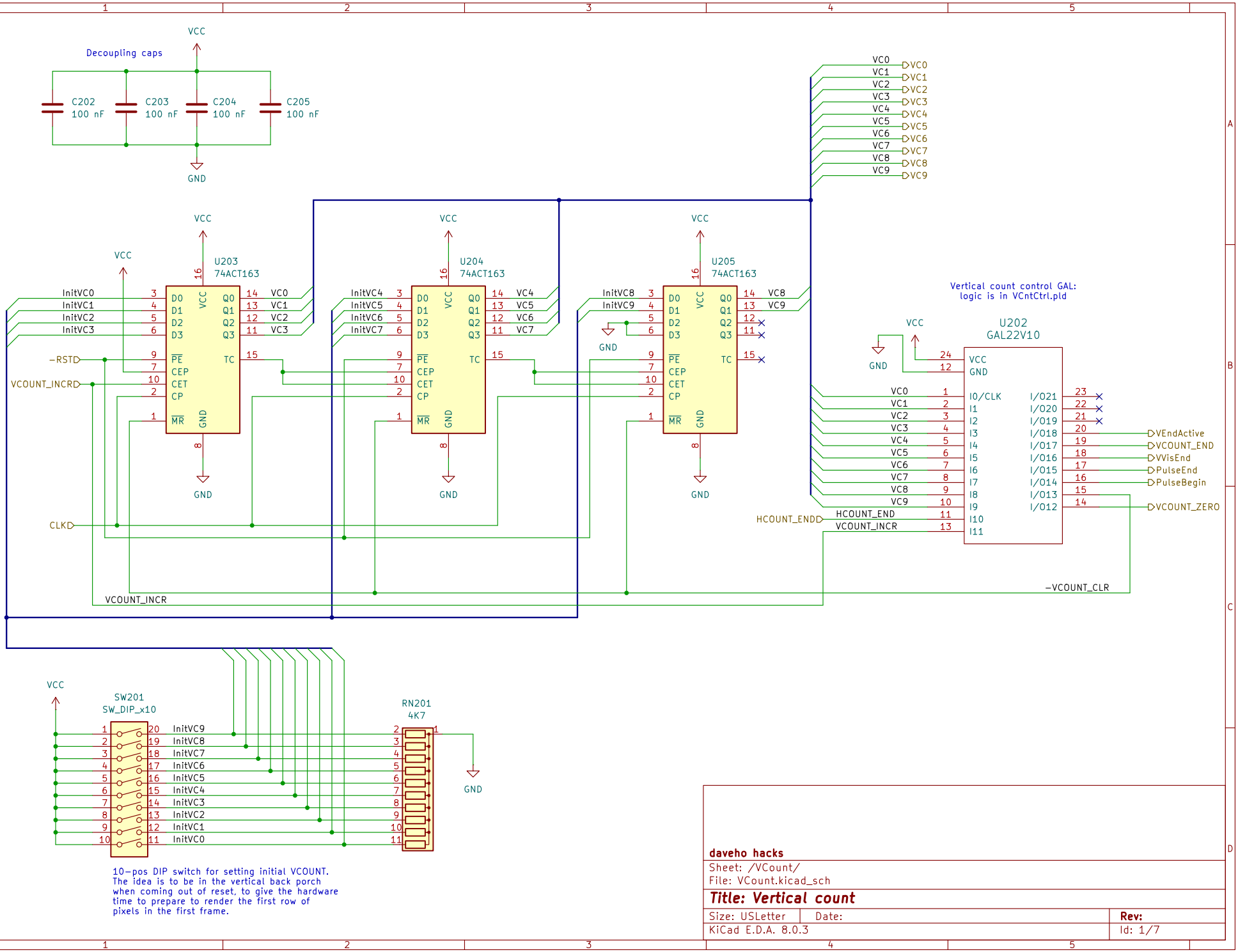
Sheet: /
File: HW_VGA.kicad_sch

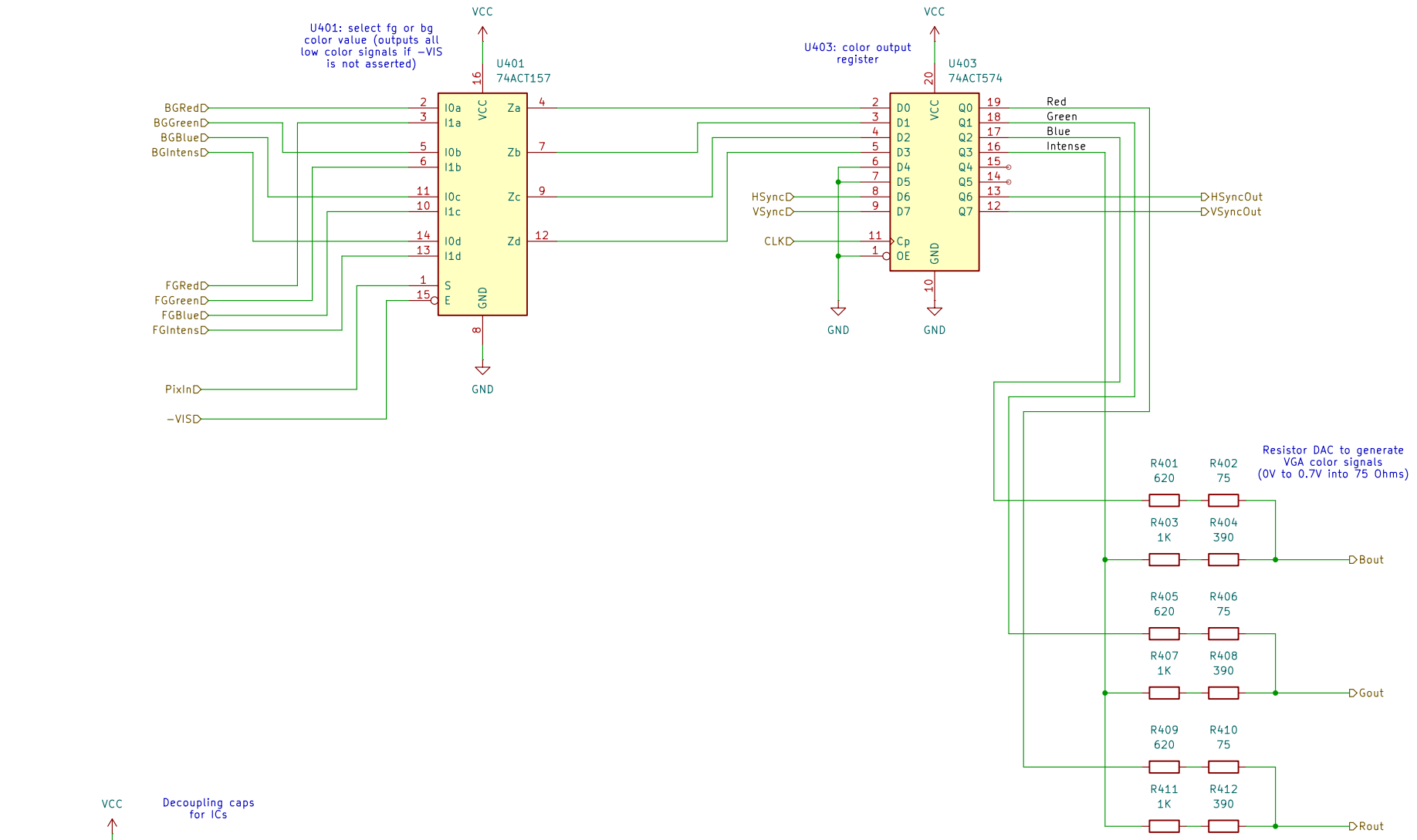
Title: Hardware VGA

Size: User	Date:	Rev:
KiCad E.D.A. 8.0.3		Id: 1/7

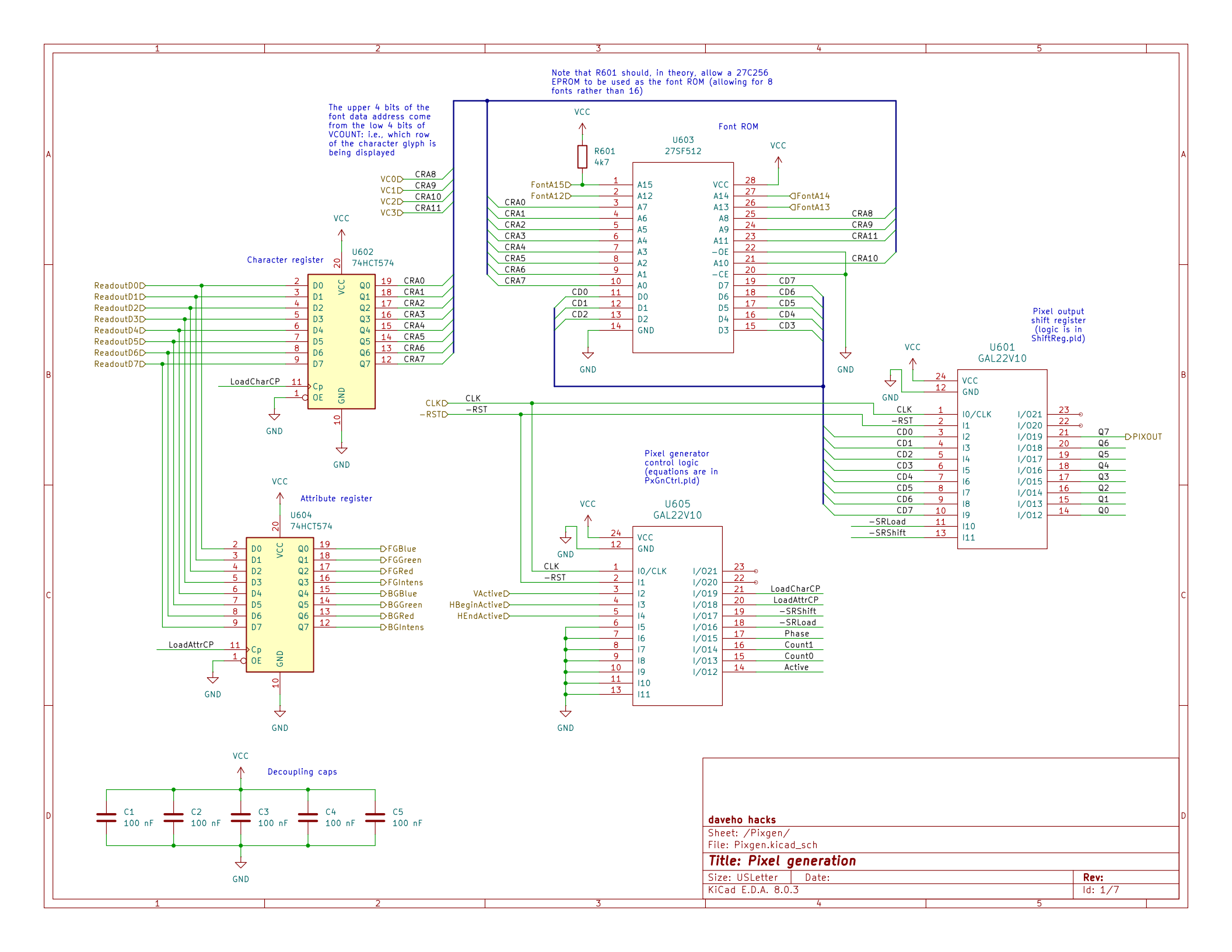


daveho hacks	
Sheet: /HCount/	
File: HCount.kicad_sch	
Title: Horizontal count	
Size: USLetter	Date:
KiCad E.D.A. 8.0.3	Rev: Id: 1/7

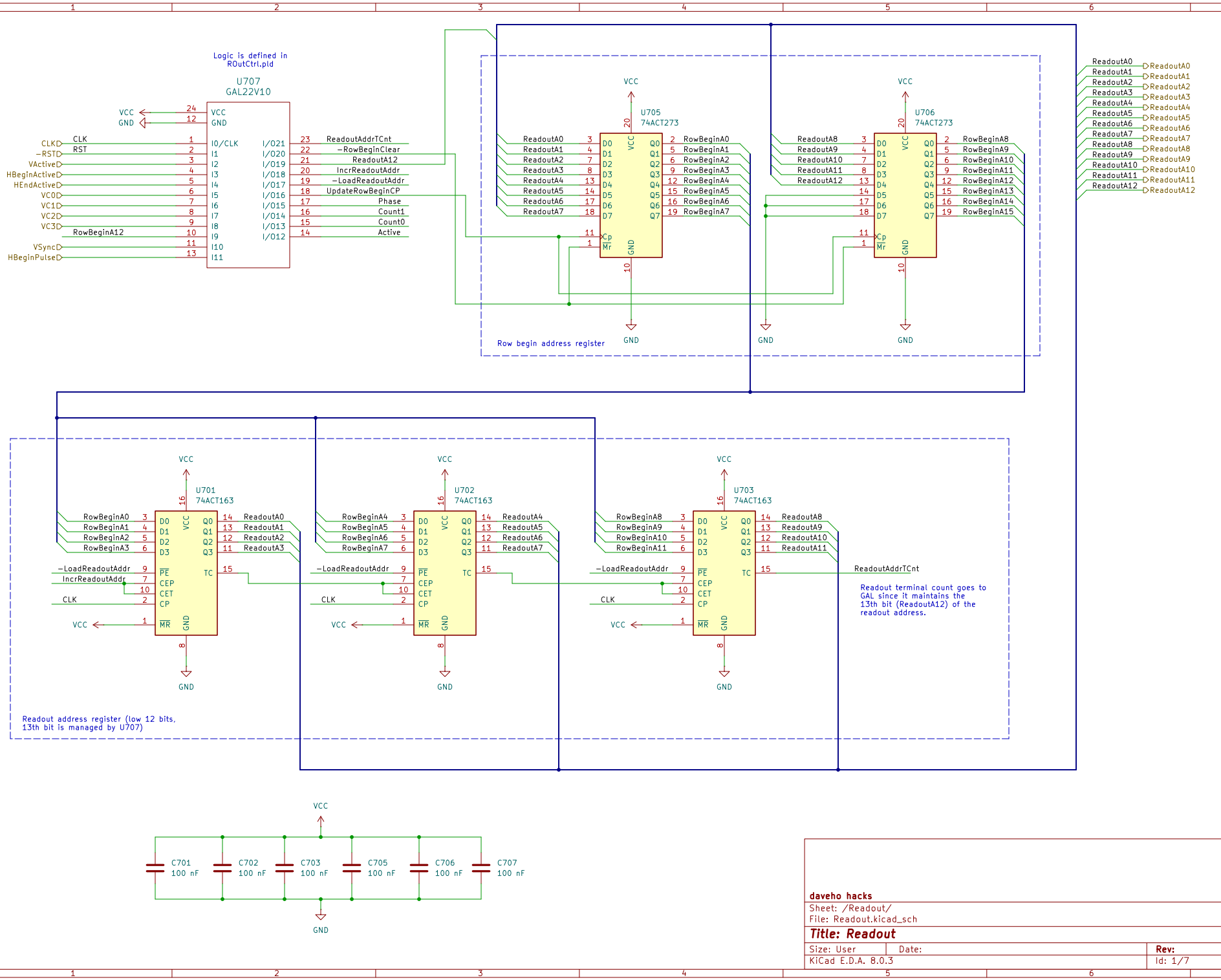
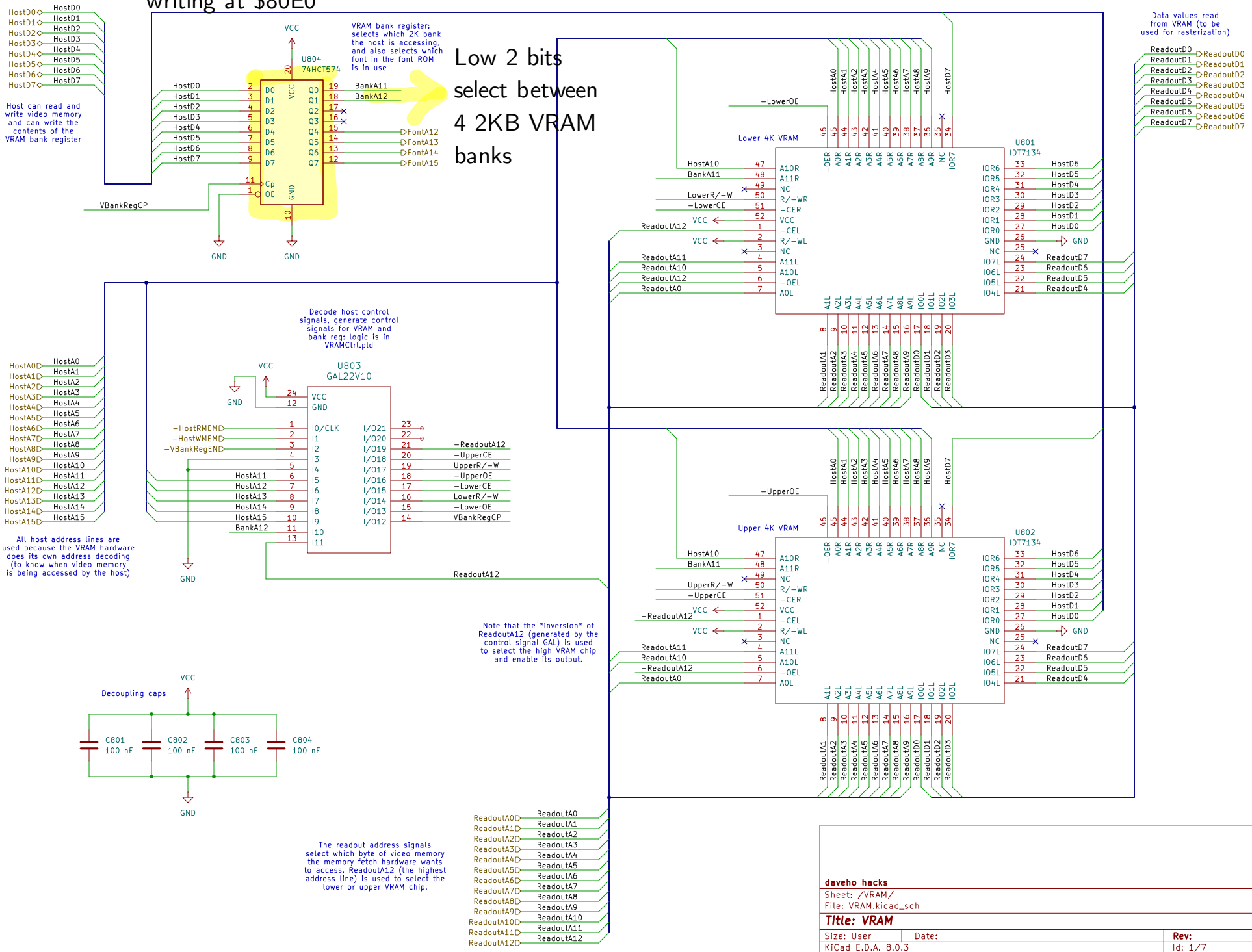

Decoupling caps
VCC
GND
C202
100 nF
C203
100 nF
C204
100 nF
C205
100 nF
U203
74ACT163
U204
74ACT163
U205
74ACT163
InitVC0
InitVC1
InitVC2
InitVC3
InitVC4
InitVC5
InitVC6
InitVC7
InitVC8
InitVC9
VC0
VC1
VC2
VC3
VC4
VC5
VC6
VC7
VC8
VC9
−RSTD
VCOUNT_INCRD
CLKD
VCOUNT_INCR
Vertical count control GAL:
logic is in VCntCtrl.pld
U202
GAL22V10
HCOUNT_END
VCOUNT_INCR
HCOUNT_ENDD
VEndActive
VCOUNT_END
VVisEnd
PulseEnd
PulseBegin
VCOUNT_ZERO
−VCOUNT_CLR
SW201
SW_DIP_x10
RN201
4K7
10−pos DIP switch for setting initial VCOUNT.
The idea is to be in the vertical back porch
when coming out of reset, to give the hardware
time to prepare to render the first row of
pixels in the first frame.
daveho hacks
Sheet: /VCount/
File: VCount.kicad_sch
Title: Vertical count
Size: USLetter
Date:
Rev:
KiCad E.D.A. 8.0.3
Id: 1/7



daveho hacks	
Sheet: /Output/	
File: Output.kicad_sch	
Title: Output	
Size: USLetter | Date:	**Rev:**
KiCad E.D.A. 8.0.3	Id: 4/7



daveho hacks	
Sheet: /Pixgen/	
File: Pixgen.kicad_sch	
Title: Pixel generation	
Size: USLetter | Date:	**Rev:**
KiCad E.D.A. 8.0.3	Id: 1/7


Logic is defined in
ROutCtrl.pld
U707
GAL22V10
VCC
GND
CLK
RST
−RST
VActive
HBeginActive
HEndActive
VC0
VC1
VC2
VC3
RowBeginA12
VSync
HBeginPulse
I/O/CLK
I/O21
I/O20
I/O19
I/O18
I/O17
I/O16
I/O15
I/O14
I/O13
I/O12
I10
I11
ReadoutAddrTCnt
−RowBeginClear
ReadoutA12
IncrReadoutAddr
−LoadReadoutAddr
UpdateRowBeginCP
Phase
Count1
Count0
Active
U705
74ACT273
U706
74ACT273
ReadoutA0
ReadoutA1
ReadoutA2
ReadoutA3
ReadoutA4
ReadoutA5
ReadoutA6
ReadoutA7
ReadoutA8
ReadoutA9
ReadoutA10
ReadoutA11
ReadoutA12
RowBeginA0
RowBeginA1
RowBeginA2
RowBeginA3
RowBeginA4
RowBeginA5
RowBeginA6
RowBeginA7
RowBeginA8
RowBeginA9
RowBeginA10
RowBeginA11
RowBeginA12
RowBeginA13
RowBeginA14
RowBeginA15
Row begin address register
U701
74ACT163
U702
74ACT163
U703
74ACT163
−LoadReadoutAddr
IncrReadoutAddr
CLK
ReadoutAddrTCnt
Readout terminal count goes to
GAL since it maintains the
13th bit (ReadoutA12) of the
readout address.
Readout address register (low 12 bits,
13th bit is managed by U707)
C701
100 nF
C702
100 nF
C703
100 nF
C705
100 nF
C706
100 nF
C707
100 nF
daveho hacks
Sheet: /Readout/
File: Readout.kicad_sch
Title: Readout
Size: User
Date:
Rev:
KiCad E.D.A. 8.0.3
Id: 1/7

Bank register mapped for writing at $80E0