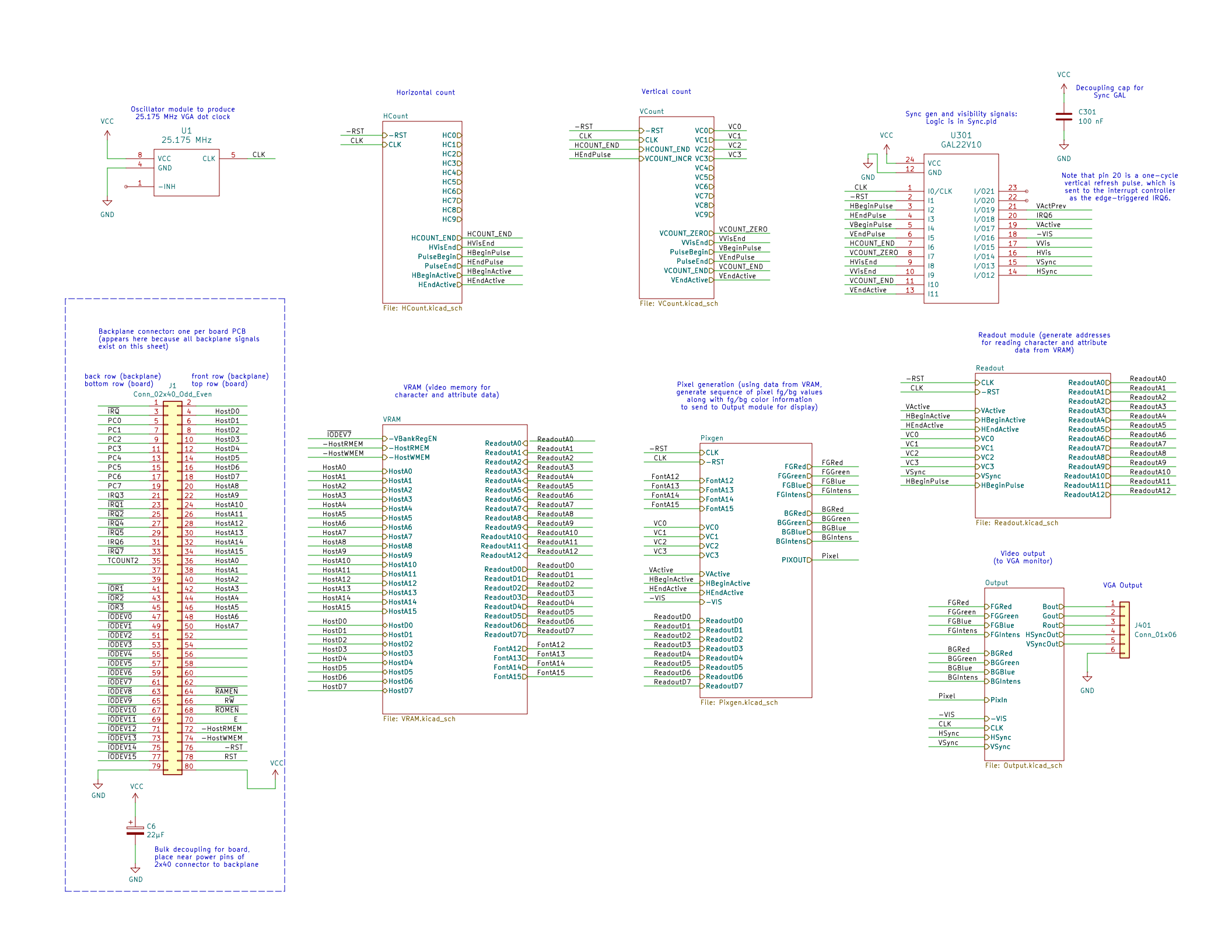
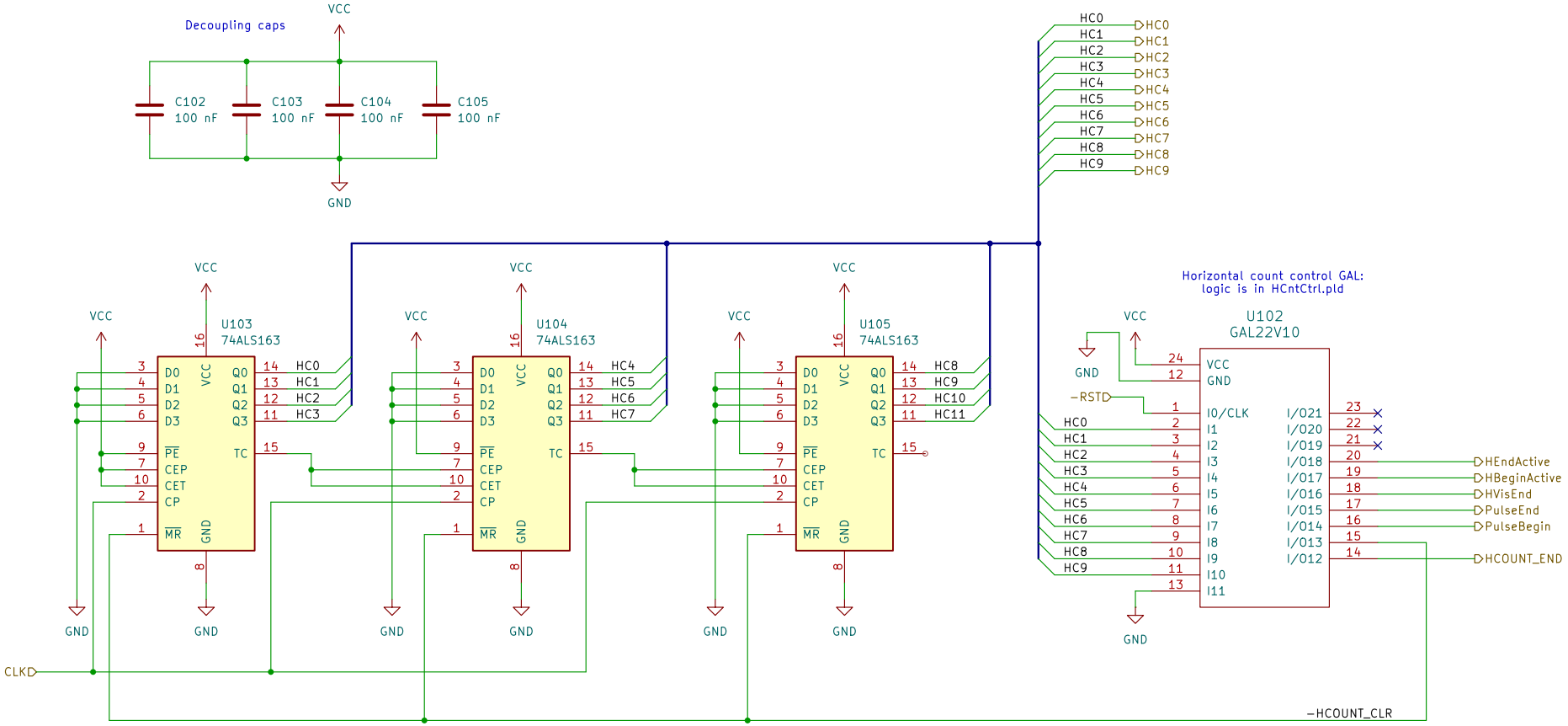
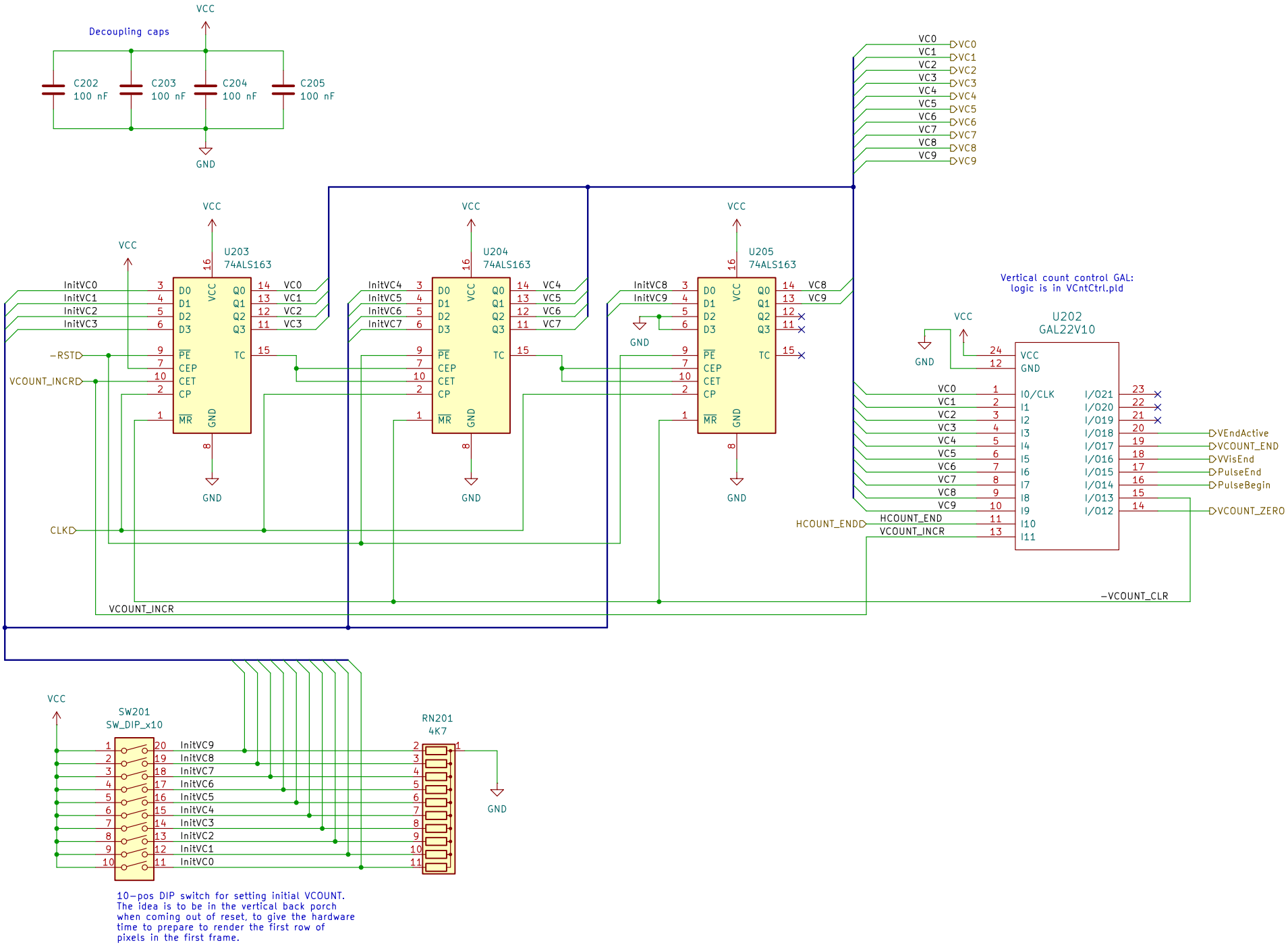
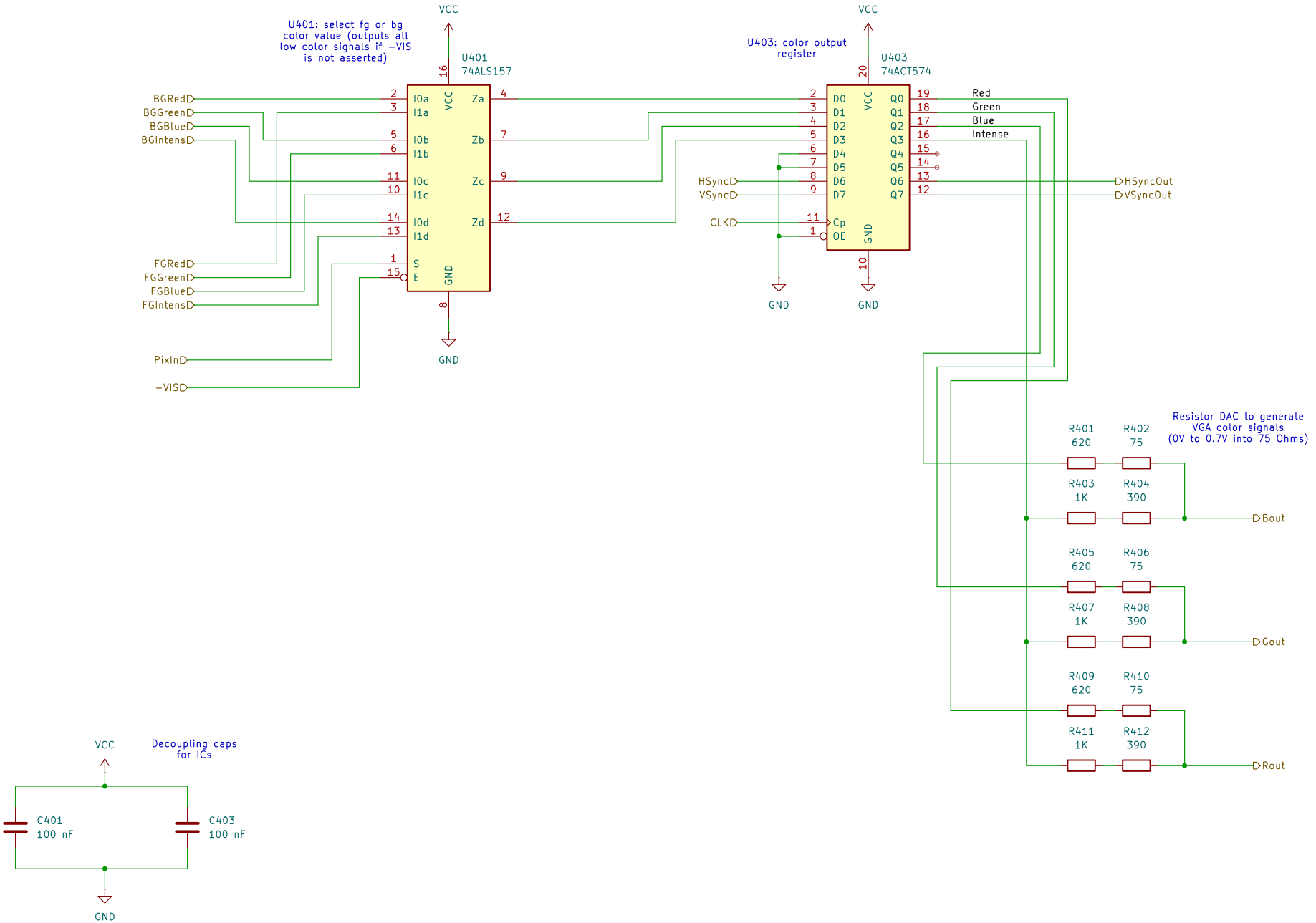
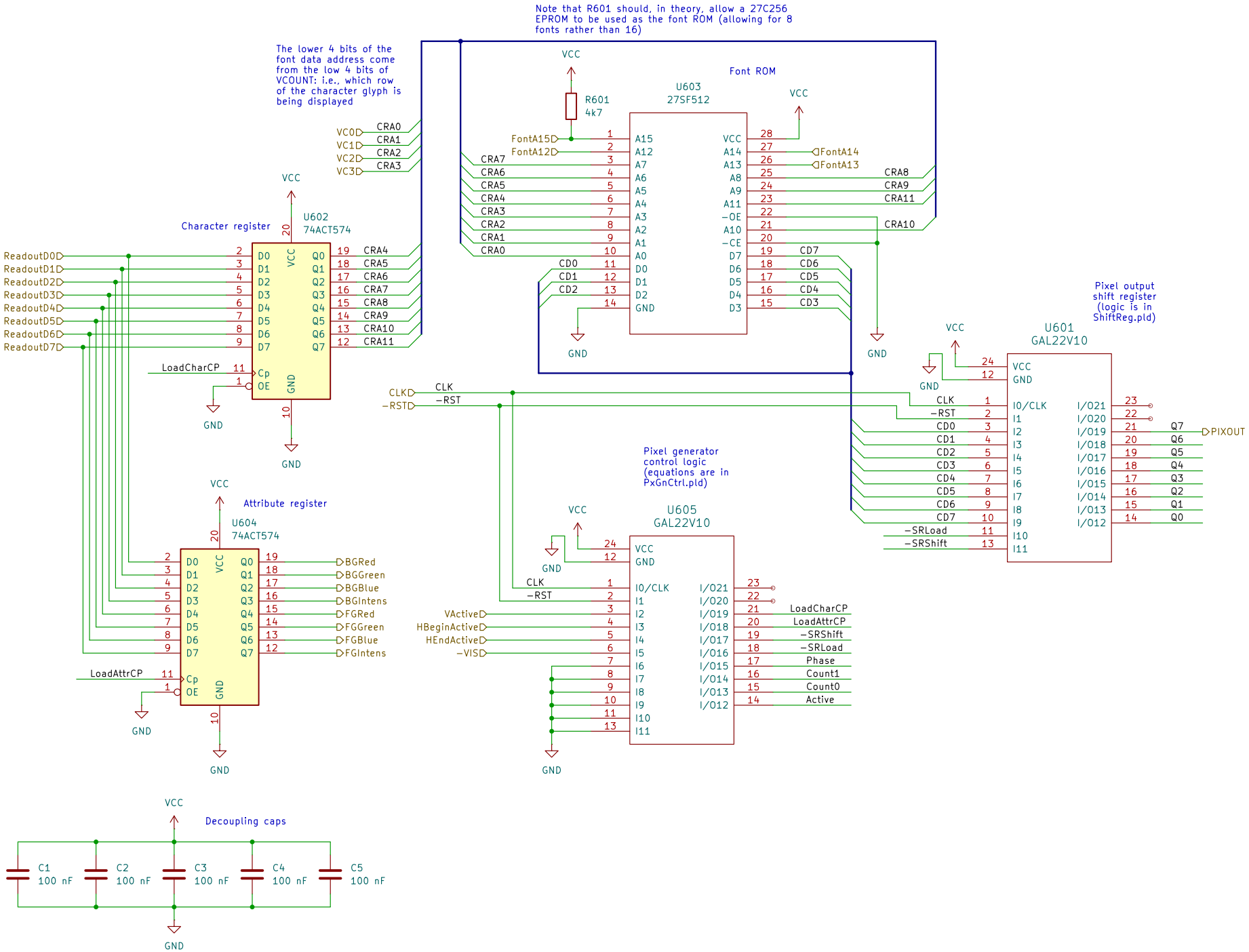
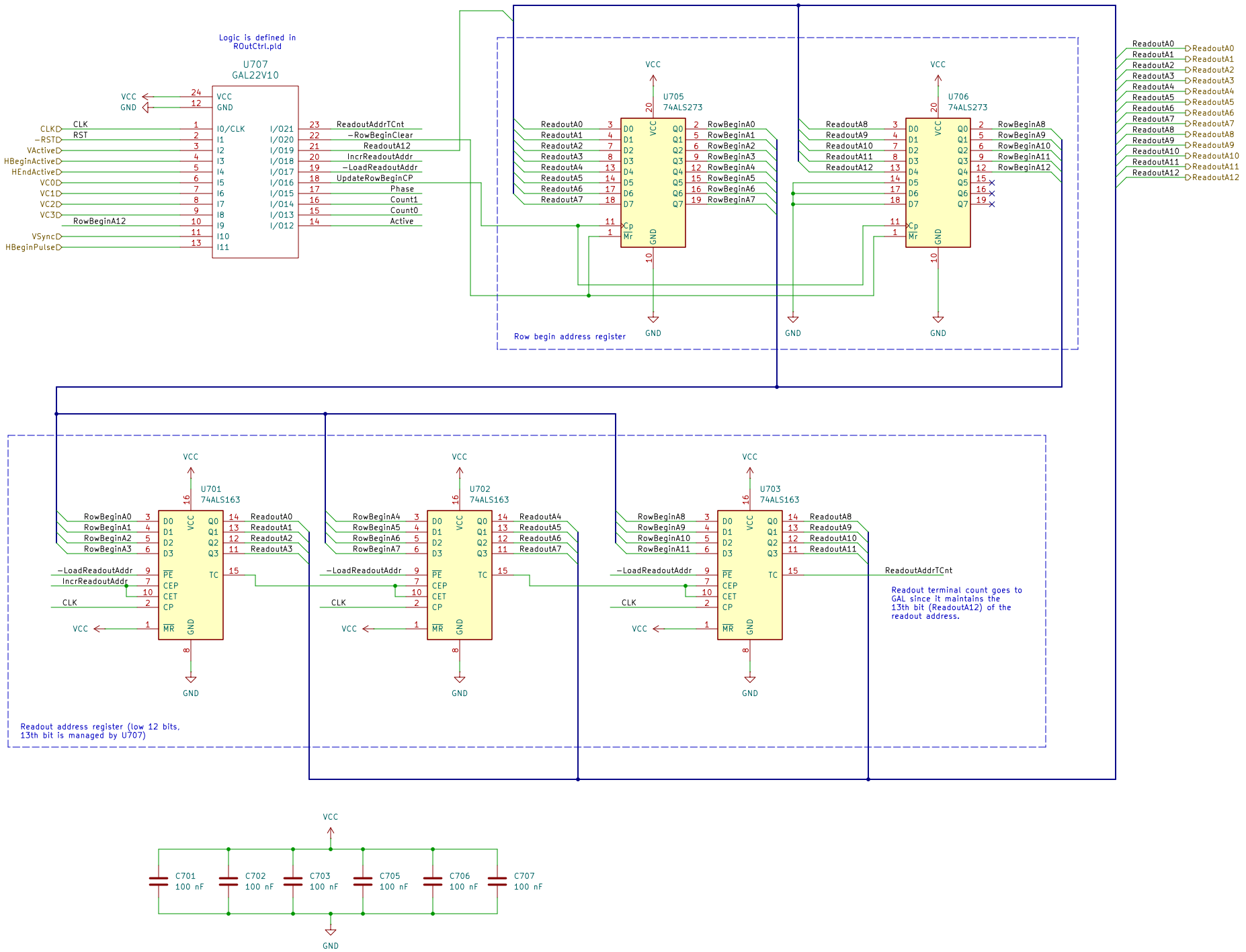

Oscillator module to produce
25.175 MHz VGA dot clock
U1
25.175 MHz
VCC
GND
CLK
−INH
Horizontal count
HCount
HC0
HC1
HC2
HC3
HC4
HC5
HC6
HC7
HC8
HC9
HCOUNT_END
HVisEnd
HBeginPulse
HEndPulse
HBeginActive
HEndActive
File: HCount.kicad_sch
Vertical count
VCount
VC0
VC1
VC2
VC3
VCOUNT_ZERO
VVisEnd
VBeginPulse
VEndPulse
VCOUNT_END
VEndActive
File: VCount.kicad_sch
Sync gen and visibility signals:
Logic is in Sync.pld
U301
GAL22V10
Decoupling cap for
Sync GAL
C301
100 nF
Note that pin 20 is a one−cycle
vertical refresh pulse, which is
sent to the interrupt controller
as the edge−triggered IRQ6.
VActPrev
IRQ6
VActive
−VIS
VVis
HVis
VSync
HSync
Backplane connector: one per board PCB
(appears here because all backplane signals
exist on this sheet)
back row (backplane)
bottom row (board)
front row (backplane)
top row (board)
J1
Conn_02x40_Odd_Even
HostD0
HostD1
HostD2
HostD3
HostD4
HostD5
HostD6
HostD7
HostA8
HostA9
HostA10
HostA11
HostA12
HostA13
HostA14
HostA15
HostA0
HostA1
HostA2
HostA3
HostA4
HostA5
HostA6
HostA7
RAMEN
RW
ROMEN
E
−HostRMEM
−HostWMEM
−RST
RST
VCC
C6
22µF
Bulk decoupling for board,
place near power pins of
2x40 connector to backplane
VRAM (video memory for
character and attribute data)
VRAM
−VBankRegEN
−HostRMEM
−HostWMEM
ReadoutA0
ReadoutA1
ReadoutA2
ReadoutA3
ReadoutA4
ReadoutA5
ReadoutA6
ReadoutA7
ReadoutA8
ReadoutA9
ReadoutA10
ReadoutA11
ReadoutA12
ReadoutD0
ReadoutD1
ReadoutD2
ReadoutD3
ReadoutD4
ReadoutD5
ReadoutD6
ReadoutD7
FontA12
FontA13
FontA14
FontA15
File: VRAM.kicad_sch
Pixel generation (using data from VRAM,
generate sequence of pixel fg/bg values
along with fg/bg color information
to send to Output module for display)
Pixgen
−RST
CLK
FontA12
FontA13
FontA14
FontA15
VC0
VC1
VC2
VC3
VActive
HBeginActive
HEndActive
−VIS
FGRed
FGGreen
FGBlue
FGIntens
BGRed
BGGreen
BGBlue
BGIntens
Pixel
PIXOUT
File: Pixgen.kicad_sch
Readout module (generate addresses
for reading character and attribute
data from VRAM)
Readout
File: Readout.kicad_sch
Video output
(to VGA monitor)
Output
VGA Output
Bout
Gout
Rout
HSyncOut
VSyncOut
J401
Conn_01x06
PixIn
File: Output.kicad_sch

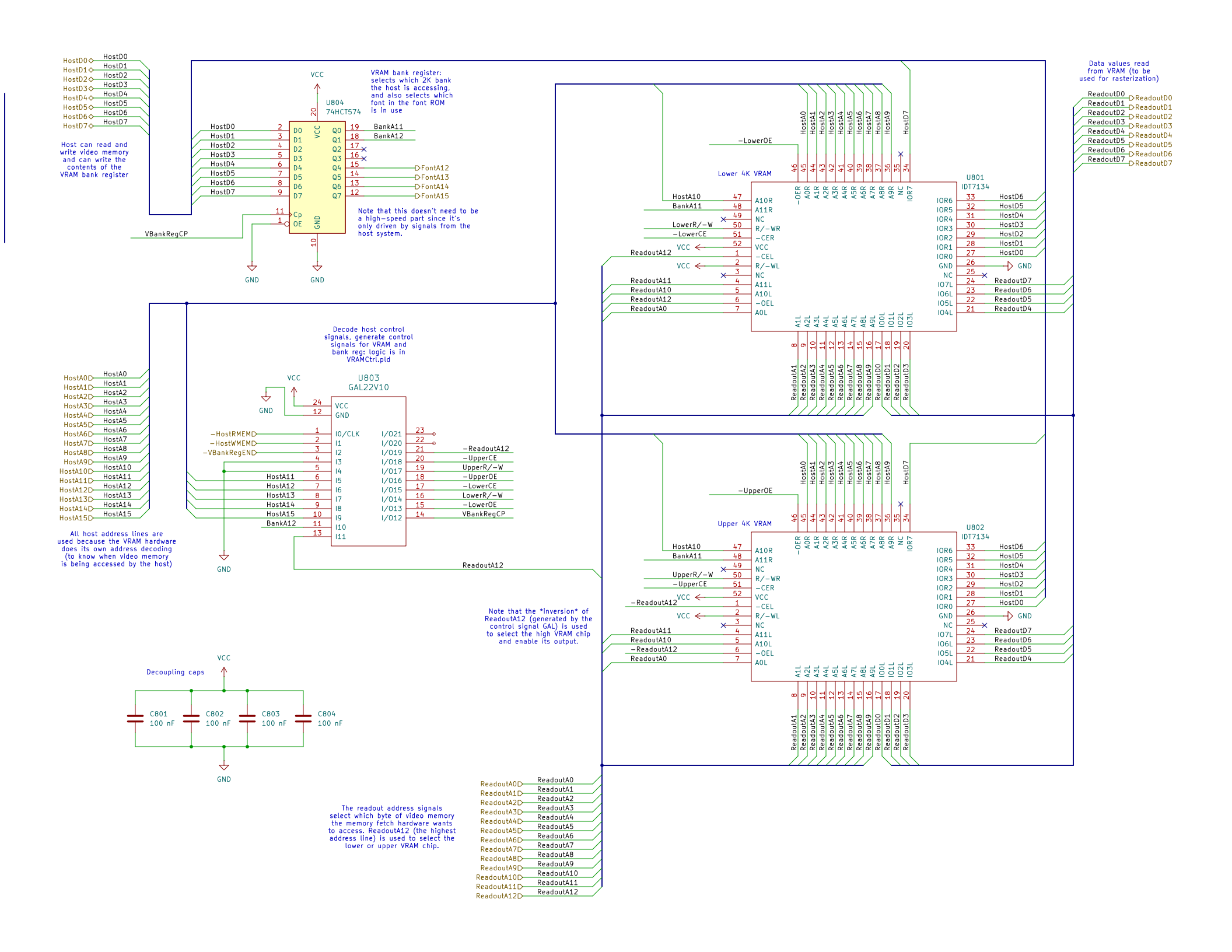

Decoupling caps
VCC
C102
100 nF
C103
100 nF
C104
100 nF
C105
100 nF
GND
HC0
HC1
HC2
HC3
HC4
HC5
HC6
HC7
HC8
HC9
U103
74ALS163
U104
74ALS163
U105
74ALS163
D0
D1
D2
D3
Q0
Q1
Q2
Q3
PE
CEP
CET
CP
MR
TC
Horizontal count control GAL:
logic is in HCntCtrl.pld
U102
GAL22V10
-RST
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I/O21
I/O20
I/O19
I/O18
I/O17
I/O16
I/O15
I/O14
I/O13
I/O12
HEndActive
HBeginActive
HVisEnd
PulseEnd
PulseBegin
HCOUNT_END
CLK
-HCOUNT_CLR


Decoupling caps
VCC
C202
100 nF
C203
100 nF
C204
100 nF
C205
100 nF
GND
U203
74ALS163
U204
74ALS163
U205
74ALS163
InitVC0
InitVC1
InitVC2
InitVC3
InitVC4
InitVC5
InitVC6
InitVC7
InitVC8
InitVC9
VC0
VC1
VC2
VC3
VC4
VC5
VC6
VC7
VC8
VC9
D0
D1
D2
D3
Q0
Q1
Q2
Q3
PE
CEP
CET
CP
MR
TC
−RST
VCOUNT_INCR
CLK
Vertical count control GAL:
logic is in VCntCtrl.pld
U202
GAL22V10
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I/O21
I/O20
I/O19
I/O18
I/O17
I/O16
I/O15
I/O14
I/O13
I/O12
HCOUNT_END
VCOUNT_INCR
HCOUNT_ENDD
VEndActive
VCOUNT_END
VVisEnd
PulseEnd
PulseBegin
VCOUNT_ZERO
−VCOUNT_CLR
SW201
SW_DIP_x10
RN201
4K7
10−pos DIP switch for setting initial VCOUNT.
The idea is to be in the vertical back porch
when coming out of reset, to give the hardware
time to prepare to render the first row of
pixels in the first frame.


U401: select fg or bg color value (outputs all low color signals if –VIS is not asserted)
U401
74ALS157
VCC
GND
BGRed
BGGreen
BGBlue
BGIntens
FGRed
FGGreen
FGBlue
FGIntens
PixIn
–VIS
U403: color output register
U403
74ACT574
HSync
VSync
CLK
Red
Green
Blue
Intense
HSyncOut
VSyncOut
Resistor DAC to generate VGA color signals (0V to 0.7V into 75 Ohms)
R401 620
R402 75
R403 1K
R404 390
R405 620
R406 75
R407 1K
R408 390
R409 620
R410 75
R411 1K
R412 390
Bout
Gout
Rout
Decoupling caps for ICs
C401 100 nF
C403 100 nF


Note that R601 should, in theory, allow a 27C256 EPROM to be used as the font ROM (allowing for 8 fonts rather than 16)
The lower 4 bits of the font data address come from the low 4 bits of VCOUNT: i.e., which row of the character glyph is being displayed
Font ROM
U603
27SF512
R601
4k7
VC0
VC1
VC2
VC3
CRA0
CRA1
CRA2
CRA3
FontA15
FontA12
FontA14
FontA13
CRA4
CRA5
CRA6
CRA7
CRA8
CRA9
CRA10
CRA11
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
Character register
U602
74ACT574
ReadoutD0
ReadoutD1
ReadoutD2
ReadoutD3
ReadoutD4
ReadoutD5
ReadoutD6
ReadoutD7
LoadCharCP
Pixel output shift register (logic is in ShiftReg.pld)
U601
GAL22V10
CLK
−RST
PIXOUT
Pixel generator control logic (equations are in PxGnCtrl.pld)
U605
GAL22V10
VActive
HBeginActive
HEndActive
−VIS
LoadCharCP
LoadAttrCP
−SRShift
−SRLoad
Phase
Count1
Count0
Active
Attribute register
U604
74ACT574
LoadAttrCP
BGRed
BGGreen
BGBlue
BGIntens
FGRed
FGGreen
FGBlue
FGIntens
Decoupling caps
C1
C2
C3
C4
C5
100 nF
VCC
GND


Logic is defined in
ROutCtrl.pld
U707
GAL22V10
VCC
GND
CLK
RST
−RST
VActive
HBeginActive
HEndActive
VC0
VC1
VC2
VC3
RowBeginA12
VSync
HBeginPulse
I/O/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I/O21
I/O20
I/O19
I/O18
I/O17
I/O16
I/O15
I/O14
I/O13
I/O12
ReadoutAddrTCnt
−RowBeginClear
ReadoutA12
IncrReadoutAddr
−LoadReadoutAddr
UpdateRowBeginCP
Phase
Count1
Count0
Active
U705
74ALS273
U706
74ALS273
ReadoutA0
ReadoutA1
ReadoutA2
ReadoutA3
ReadoutA4
ReadoutA5
ReadoutA6
ReadoutA7
ReadoutA8
ReadoutA9
ReadoutA10
ReadoutA11
ReadoutA12
RowBeginA0
RowBeginA1
RowBeginA2
RowBeginA3
RowBeginA4
RowBeginA5
RowBeginA6
RowBeginA7
RowBeginA8
RowBeginA9
RowBeginA10
RowBeginA11
RowBeginA12
Row begin address register
U701
74ALS163
U702
74ALS163
U703
74ALS163
−LoadReadoutAddr
IncrReadoutAddr
CLK
ReadoutAddrTCnt
Readout terminal count goes to GAL since it maintains the 13th bit (ReadoutA12) of the readout address.
Readout address register (low 12 bits, 13th bit is managed by U707)
C701
C702
C703
C705
C706
C707
100 nF


HostD0
HostD1
HostD2
HostD3
HostD4
HostD5
HostD6
HostD7
Host can read and write video memory and can write the contents of the VRAM bank register
VCC
U804
74HCT574
VRAM bank register: selects which 2K bank the host is accessing, and also selects which font in the font ROM is in use
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Cp
OE
GND
BankA11
BankA12
FontA12
FontA13
FontA14
FontA15
VBankRegCP
Note that this doesn't need to be a high-speed part since it's only driven by signals from the host system.
Data values read from VRAM (to be used for rasterization)
ReadoutD0
ReadoutD1
ReadoutD2
ReadoutD3
ReadoutD4
ReadoutD5
ReadoutD6
ReadoutD7
Lower 4K VRAM
U801
IDT7134
-LowerOE
HostA0
HostA1
HostA2
HostA3
HostA4
HostA5
HostA6
HostA7
HostA8
HostA9
HostD7
-OER
A0R
A1R
A2R
A3R
A4R
A5R
A6R
A7R
A8R
A9R
NC
IOR7
HostA10
BankA11
LowerR/-W
-LowerCE
ReadoutA12
ReadoutA11
ReadoutA10
ReadoutA0
A10R
A11R
NC
R/-WR
-CER
VCC
-CEL
R/-WL
NC
A11L
A10L
-OEL
A0L
IOR6
IOR5
IOR4
IOR3
IOR2
IOR1
IOR0
GND
NC
IO7L
IO6L
IO5L
IO4L
HostD6
HostD5
HostD4
HostD3
HostD2
HostD1
HostD0
ReadoutD7
ReadoutD6
ReadoutD5
ReadoutD4
A1L
A2L
A3L
A4L
A5L
A6L
A7L
A8L
A9L
IO0L
IO1L
IO2L
IO3L
ReadoutA1
ReadoutA2
ReadoutA3
ReadoutA4
ReadoutA5
ReadoutA6
ReadoutA7
ReadoutA8
ReadoutA9
ReadoutD0
ReadoutD1
ReadoutD2
ReadoutD3
Decode host control signals, generate control signals for VRAM and bank reg; logic is in VRAMCtrl.pld
U803
GAL22V10
-HostRMEM
-HostWMEM
-VBankRegEN
HostA11
HostA12
HostA13
HostA14
HostA15
BankA12
IO/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I/O21
I/O20
I/O19
I/O18
I/O17
I/O16
I/O15
I/O14
I/O13
I/O12
-ReadoutA12
-UpperCE
UpperR/-W
-UpperOE
-LowerCE
LowerR/-W
VBankRegCP
All host address lines are used because the VRAM hardware does its own address decoding (to know when video memory is being accessed by the host)
Upper 4K VRAM
U802
IDT7134
-UpperOE
UpperR/-W
-UpperCE
-ReadoutA12
Note that the *inversion* of ReadoutA12 (generated by the control signal GAL) is used to select the high VRAM chip and enable its output.
Decoupling caps
C801
100 nF
C802
100 nF
C803
100 nF
C804
100 nF
The readout address signals select which byte of video memory the memory fetch hardware wants to access. ReadoutA12 (the highest address line) is used to select the lower or upper VRAM chip.