Field testing for cosmic ray soft errors in semiconductor memories

by T. J. O'Gorman

J. M. Ross

A. H. Taber

J. F. Ziegler

H. P. Muhlfeld

C. J. Montrose

H. W. Curtis

J. L. Walsh

This paper presents a review of experiments performed by IBM to investigate the causes of soft errors in semiconductor memory chips under field test conditions. The effects of alphaparticles and cosmic rays are separated by comparing multiple measurements of the softerror rate (SER) of samples of memory chips deep underground and at various altitudes above the earth. The results of case studies on four different memory chips show that cosmic rays are an important source of the ionizing radiation that causes soft errors. The results of field testing are used to confirm the accuracy of the modeling and the accelerated testing of chips.

Introduction

The normal background radiation environment on the surface of the earth has an ionizing component that affects the reliability of semiconductor memory chips used in computers. A single subatomic particle can interact with a memory chip to cause individual bits of stored data to be lost, resulting in what are termed *soft errors*. A soft error in a semiconductor memory chip has two attributes: a) the data retrieved from an address on the chip differ from the data originally stored in that address, and b) the absence of

physical damage or defects on the chip, which continues to function normally thereafter. A soft error in a large memory system can transmit incorrect data or an improper instruction to the processor. Fortunately, such occurrences can be controlled with error-correction and error-recovery techniques at the system level that make the fault and its correction transparent to the user [1]. The phenomenon of single-bit soft errors induced by ionizing radiation is well known to chip designers and reliability engineers [2, 3]. The rate at which single-bit errors occur in a population of chips of a particular design is often referred to as its soft-error rate (SER), or single-event upset (SEU) rate.

Originally, electronic noise and alpha-particles emitted by the radioactive decay of on-chip impurities were thought to be the only significant cause of these occurrences in ground-based computers. In 1979, Ziegler proposed that cosmic rays were another significant source of ionizing radiation that contributed to the problem [4], although the effects were believed to be small for the state-of-the-art 64Kb DRAM chips of the time.

Over the past several years, researchers at IBM have performed a number of experiments to investigate the effects of cosmic rays on chip SER [5]. The results of these experiments have shown that energetic neutrons generated in the atmosphere by cosmic rays cause soft errors on memory chips at ground level. The neutrons collide with silicon nuclei in the chips and generate

•Copyright 1996 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the Journal reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to republish any other portion of this paper must be obtained from the Editor.

0018-8646/96/\$5.00 © 1996 IBM

42

Table 1 Locations where Nitetrain SER measurements were performed. The last column is the time from the start of the experiment in September 1983 to the midpoint of each SER measurement.

Location	Altitude (km)	Atmospheric depth (g/cm²)	Time (khr)
1st Essex Junction, VT	0.1	1033	1.46
Hutchinson, KS	0.2 underground	N/A	6.21
Boulder, CO	1.6	840	10.04
2nd Essex Junction, VT	0.1	1033	17.7
Leadville, CO	3.1	700	29.93

charged particles which can interact with the electronic circuits [6]. Detailed models of charge collection have been developed to simulate the effects of ionizing radiation on memory circuits [7–12].

This paper reviews various important "field testing" experiments on VLSI memory chips. Field testing is the measurement of the error rate of chips due to natural background radiation. During field testing, the natural radiation may be changed by making terrestrial measurements at sea level, above sea level, where the radiation may increase ten times, or under shielding, where the radiation is reduced.

The following sections provide descriptions of four experiments performed by IBM to examine the behavior of memory chip SER under field test conditions. The results of these experiments showed how the SER was affected by altitude, latitude, and shielding thickness. The altitude dependence of the SER data is in good agreement with projections based on accelerated testing [13].

Cosmic ray SER measurements

• Nitetrain cosmic ray experiment (1983–1988)

The Nitetrain cosmic ray experiment was the first IBM effort to measure the effects of cosmic rays on semiconductor memory chips. The primary motivation for doing this experiment was to determine the magnitude of the effect of cosmic rays on the SER of a real memory product chip.

The SER of a sample of dynamic random access memory (DRAM) chips was measured at 0.1 km and again 200 m underground to identify soft errors caused by cosmic rays. This was done by operating the chips under nominal voltage and temperature conditions in a custombuilt tester. The tester continuously searched for soft errors on the chips by sequentially reading each byte of

data stored in the memory arrays. A blanket logical pattern was written into the memory arrays that charged all of the silicon diffusion nodes in the storage capacitors to a high potential. The operating cycle time of the chips was a constant for all of the measurements. All above-ground tests were performed in normal office environments in singlestory buildings. The same tester, data-acquisition system, and chip operating conditions were used at each location.

Since complete descriptions of the chip and this experiment have been published elsewhere [14, 15], only a summary of the details is provided here. The memory chip used for this experiment, called Nitetrain within IBM, was a 288Kb DRAM. It was chosen because of its relatively high sensitivity to ionizing radiation. The bit lines on the chip are allowed to float, making them sensitive to charge collection about 90% of the time. This particular memorycell design is especially vulnerable to soft errors induced by ionizing radiation. The combination of a low-doped silicon substrate and 10 V across the storage node results in a wide depletion region and an enhanced charge collection by funneling [16], where the depletion region is distorted along the track of an ionizing particle which momentarily acts like a conducting wire. The SER of this chip in the field was not a reliability problem because it was used in an environment with robust error correction.

An initial measurement of the SER was made in Essex Junction, Vermont, about 0.1 km above sea level. The SER measurement was repeated 200 m underground in Hutchinson, Kansas. This was done to separate the components of the SER caused by cosmic rays from that caused by electronic noise in the tester and on-chip radioactive sources of alpha-particles. The flux of neutrons and protons from cosmic radiation was virtually eliminated by the 200 m of rock shielding [4] in this underground test site.

The altitude dependence of the effect of cosmic rays on memory-chip SER was investigated by moving the Nitetrain tester to Boulder, Colorado, for SER measurements at an altitude of 1.6 km. Afterward, the tester was returned to Essex Junction for an additional measurement at 0.1 km, and it was then moved to Leadville, Colorado, at an altitude of 3.1 km.

■ Nitetrain results

The location, altitude, atmospheric depth, and time of each of the SER measurements reported here are listed in Table 1. The times listed in the fourth column of the table correspond to the time from the start of the experiment to the midpoint in time of each SER measurement. The altitudes given in the table are the vertical distances above sea level for each of the locations at which data were collected. Atmospheric depth is defined as the mass of air in a column above the tester extending to space, which is a measure of the shielding provided by the atmosphere at each test location.

The SER data points are plotted versus real time in Figure 1. Here, real time refers to the time since the beginning of the experiment in September 1983 until the midpoint in time of each SER measurement. The SER data are reported in units of FITs (failures in time). One FIT is equal to one fail in one billion chip-hours. An event is defined as the detection of one or more soft errors by the tester.

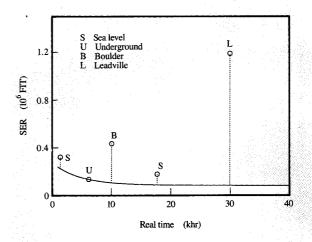
The SER was observed to have a strong time-dependent component during the early part of this experiment. The SER of the sample of chips changed by almost a factor of 2 during the two years between measurements under identical conditions at 0.1 km in Essex Junction. This was attributed to the presence of a nonequilibrium mixture of Po²¹⁰ and some of the long-lived daughters of thorium or uranium on the chips. The half-life of Po²¹⁰ is 138 days, which has important consequences in the analysis of the data [17]. Similar contamination of chips had been reported previously [5, 18]. Because of its very short radioactive half-life, every Po²¹⁰ atom on a chip would decay and emit an alpha-particle, which could result in a very high SER during testing.

In order to separate the effects of the various radiation sources and to determine the magnitude of the cosmic ray component of the SER, the total SER was expressed as a function of time,

$$SER = A \exp\left(-\frac{t}{t_{10}}\right) + B + C,\tag{1}$$

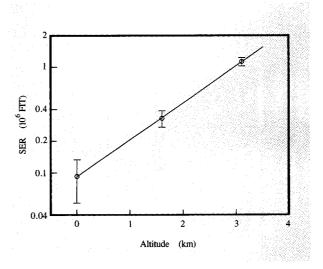
where A is the initial SER due to Po²¹⁰ contamination, $t_{1/2}$ is the half-life of Po²¹⁰, B is the SER contribution of alpha-particle emitters with long half-lives, and C is the SER contribution from cosmic rays. This equation can be used to separate the alpha-particle component of the SER from the total SER. Inserting the SER data from the two sea-level measurements and the underground measurement into the equation along with the time of each of the measurements listed in Table 1 provides a set of three equations that can be used to obtain the three unknowns, A, B, and C. The constants A and B are related to sources of alpha-particle radiation on the chip as well as electronic noise, while the constant C is the cosmic ray component of the SER at each test location. Deep underground, C is set equal to zero. Solving this set of simultaneous equations provides the coefficients for the alpha-particle component of the SER and the sea-level cosmic ray component, C. In Figure 1, the solid curve shows the alpha-particle component of the SER for the chips based on Equation (1).

The SER caused by cosmic rays is the total SER minus the portion due to alpha-particle radiation and electronic noise. The cosmic ray component of the SER as a function of altitude is plotted in **Figure 2**. The data show that even



Emilia

SER measurements of Nitetrain, a 288Kb DRAM, 200 m underground, at 1.6 km at Boulder, CO, and at 3.1 km at Leadville, CO. The data are plotted versus real time. The chips were initially contaminated with Po²¹⁰, which emits alpha-particles and has a half-life of 138 days. The solid curve is the alpha-particle component of the SER. The vertical distance above this curve (dotted lines) corresponds to the cosmic ray component of the SER. (FIT = failure in time.)



atome?

Cosmic ray component of SER for the Nitetrain chip as a function of altitude. The alpha-particle component has been subtracted from the measured values of the total SER. The solid line is a least-squares fit of an exponential function to the data.



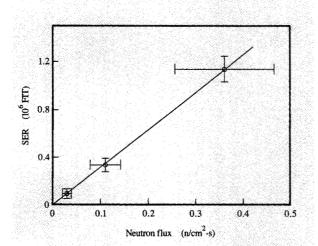


Figure 3

Cosmic ray SER versus atmospheric neutron flux in the energy range from 10 to 170 MeV. The straight line is a least-squares fit showing that there is a very strong linear correlation between the SER and the neutron flux.

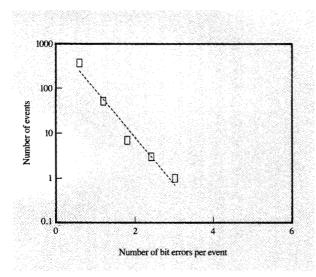


Figure 4

Frequency of occurrence of multiple bit errors. Some ionizing radiation events can result in several simultaneous bit errors.

at sea level, cosmic rays were responsible for a significant fraction of the observed error rate, and that the effect of cosmic rays increased greatly with altitude. At the high altitude in Leadville, the effect of cosmic rays on SERs was more than ten times greater than it was at sea level, because the flux of energetic neutrons generated in the atmosphere by cosmic rays increases with altitude. Figure 3 shows the cosmic ray component of the SER plotted against Saxena's measurement of the integrated flux of atmospheric neutrons in the energy range from 10 to 170 MeV at sea level, Boulder, and Leadville [19]. Since the cosmic ray SER should be directly proportional to the flux of neutrons, the linear least-squares fit to the data (the solid line in Figure 3) was required to pass through the origin. These data show that there is a very good correlation between the SER and the integrated neutron flux measurements.

A fraction of the soft-error events observed during the experiment resulted in multiple bit errors, where two or more bit errors were detected nearly simultaneously by the tester. Each error in a multiple-error event had the same time stamp in the data record (within the two or three minutes it took the tester to find each error), and the physical addresses on the chip always corresponded to adjacent bit lines. The distribution of the number of errors per event observed in Leadville is plotted in **Figure 4**. A single event included as many as five bit errors.

To determine the relative likelihood that cosmic ray events and alpha-particles cause multiple bit errors, the measurement data from all of the geographic locations were examined. In Figure 5, the fraction of events that resulted in more than one error is plotted versus the fraction of the total SER that can be attributed to cosmic rays on the basis of Equation (1). When the SER is dominated by cosmic rays, more than twice as many events have multiple errors as when the SER is dominated by alpha-particle radiation. This indicates that, on average, the charge made available for collection in the memory cells is much larger for a cosmic ray event than for an alpha-particle event (for details, see [14]).

• Blue Spruce experiment (1987–1990)

At the same time that the Nitetrain experiment was moved to Leadville, another experiment, nicknamed Blue Spruce, was planned to investigate cosmic ray effects on a 4Kb bipolar memory array chip.

Two testers were built to hold a total of 2304 chips. The testers were controlled by a PC equipped with a modem. From 1987 to 1990, SER measurements were conducted at sites in Boulder and Leadville, Colorado, and underground at a site in Kansas City, Kansas. Measurements were made at nominal chip voltages and then at a series of lower, or "pinched," voltages to increase the sensitivity of the chip and to determine how much, if any, of the observed SER was due to alpha-particle activity on the chips.

Leadville was selected for these experiments because it is the highest-altitude incorporated city in the United States. A site in an urban setting was necessary because of the 50 kW of power required for the experiments and also for security of the equipment.

The measurements in Kansas City were performed in an underground facility with an office-like environment. There was about 5000 g/cm² of overlying rock, composed mostly of limestone and shale. At the three locations—Leadville, Boulder, and Kansas City—the cosmic ray flux was measured and compared to published data [20].

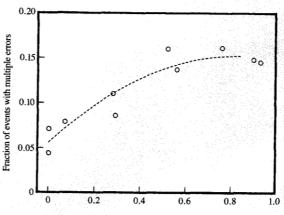
During the experiments at the three locations, power line noise and ambient electronic noise were constantly surveyed with Dranetz noise-monitoring systems. These instruments produced hard-copy plots of noise in real time, recording the date and time of events that exceeded a preset threshold. Although the temporal resolution of the noise monitors was at three-minute intervals, hundreds of soft errors were observed without any statistically significant correlation to noise spikes recorded by the monitors during the first year of operation.

The results of the SER measurements made with the Blue Spruce chips are shown in Figure 6. The pinch voltage is actually a voltage reduction from the nominal full operating voltage of the chip. The full-voltage SER measurement results at each location are shown in the figure as 0 V pinch. As the pinch voltage is increased (decreasing chip voltage), the chips become more sensitive to ionizing radiation. When the chips were operated at full voltage underground, there were no soft errors after nine months of testing. When the chips were pinched by 0.4 V, they became more sensitive to alpha-particles emitted by on-chip radioactive sources. This resulted in a dramatic increase in the SER as the chips were operated at deeper pinch voltages.

The two components of the SER under pinch voltage conditions are shown more clearly in Figure 7. At all locations, when the chips were operated near their nominal full-voltage conditions, the alpha-particle component of the SER dropped to zero. The error rates observed under full-voltage conditions in Boulder and Leadville were due entirely to cosmic rays. Recently, a contribution of cosmic rays to chip SER was also suggested by other workers [21].

A substantial amount of test time in Leadville was used to examine the effect of shielding materials on the SER induced by cosmic rays. It was important to find out how much of an effect the upper floors of a building might have on chip SER, and how much shielding would be needed to eliminate cosmic ray SER.

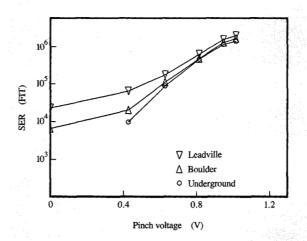
In two independent sets of measurements, the Nitetrain and Blue Spruce testers were shielded from the cosmic ray flux primarily with concrete blocks. Layers of wood and iron plates were used to support the weight of the concrete. In the first set of measurements, the Blue Spruce testers was placed under the equivalent of two feet of



Fraction of SER due to cosmic ray neutrons

Gure 5

Fraction of events where multiple simultaneous bit errors were detected versus the fraction of the total SER attributable to cosmic rays. Cosmic ray events (1.0 on the x-axis scale) cause a greater fraction of multiple errors than do alpha-particles (0 on the x-axis scale). The dashed line is a visual guide. The data shown are taken from measurements at all locations.



Figure

SER measurements of Blue Spruce, a 4Kb bipolar memory chip. The ''pinch voltage'' is the amount by which full voltage is reduced to make the chips more sensitive to ionizing radiation. The large increase in SER at higher pinch voltage is due to alphaparticles. No soft errors were observed underground when the chips were operated at full voltage (0 V pinch).

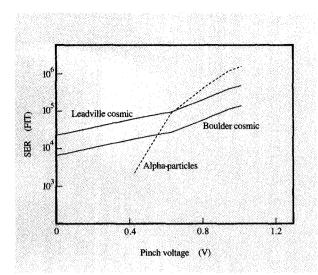
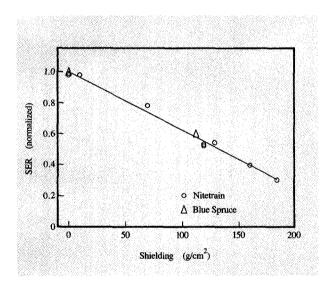


Figure 7 Separation of the cosmic ray and alpha-particle components of the SER for the Blue Spruce measurements.



Effect of shielding above the Nitetrain and Blue Spruce testers in Leadville, CO.

concrete shielding. There was no shielding around the sides of the tester. The measured Blue Spruce SER was reduced by 40% compared to the SER without concrete shielding.

In the second set of measurements, the Nitetrain tester was placed inside a concrete box shielded from above and

from all four sides. The sides of the concrete box were roughly two feet thick. The SER of the Nitetrain chips was measured under several different thicknesses of concrete shielding. Figure 8 shows the results of these shielding measurements, with the Blue Spruce data shown for comparison. The data point on the right end of the X-axis was obtained under a shield which included 18 cm of wood, 19 cm of iron plates, and more than 0.8 m of concrete. With this much shielding, the cosmic ray SER was reduced by a factor of 3. No discernible effect of side shielding was observed, which is consistent with the cosmic ray flux distribution varying by $\cos^3 \theta$, where θ is the trajectory angle from vertical [20].

• Cosmic ray SER of a vendor 4Mb DRAM (1992) The purpose of this experiment was to study the SER of a non-IBM, commercially available 4Mb DRAM. Two life tests were conducted to measure the actual SER of the 4Mb DRAM chips. The first field test experiment was conducted at approximately sea level in East Fishkill, New York. A total of 864 modules were operated for 4671 hours on the second floor of a two-story building. Soft errors could only be isolated to a single word address. It was assumed that each failed word address contained a single bit error in its data. This is a reasonable assumption, since the individual bits of each word are in physically separate locations on the chip.

During the 4.036-million-device-hour test, 24 single-address (assumed single-bit) fails were recorded, resulting in an SER of 5950 FIT per chip. The fails were randomly distributed in time.

Next, the tester system and DRAM samples were moved nearby to a vault shielded by about 20 m of rock, which eliminated cosmic ray neutrons as a source of ionizing radiation. This was done to measure the portion of the SER observed in the above-ground test that may be caused by alpha-particle emissions from the chip itself, or by tester noise. The original 864 modules were operated under the same conditions as the sea-level measurement for 5863 hours, giving a total of 5.066 million device hours. In this time, no fails were recorded. The SER measured underground is less than 450 FIT to a confidence level of 90%. Virtually all of the soft errors observed at sea level in this experiment can be attributed to cosmic rays.

• Cosmic ray SER in aircraft (1993)

Some military aircraft with computers that contain large amounts of semiconductor memory have experienced single-event upsets (SEUs) on almost every flight. Existing data suggested that these soft errors were caused by cosmic rays, in particular by atmospheric neutrons generated by cosmic rays [22]. This is a relatively new finding for the aerospace industry, and little work had been

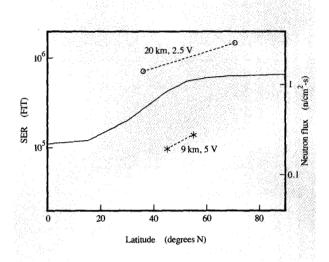
done to quantify and develop appropriate solutions to the problem.

As part of a study to investigate and characterize these effects, an experimental soft-error measurement package was developed to operate on board two types of aircraft to record memory bit upsets at high altitude [23]. An approach similar to experiments performed on the Space Shuttle was used for these measurements. A large quantity of CMOS SRAM memory chips were programmed on the ground, flown in the data-retention mode (2.5-V battery power), and read out on return.

At an altitude of approximately 9 km, 280 pieces of an IMS1601 64k×1 SRAM, manufactured by the Inmos Corporation, were tested on a total of 19 flights aboard a Boeing E-3/AWACS aircraft. The IMS1601 is a CMOS SRAM built on a 25.4-mm² n-type substrate using 1.3- μ m effective channel lengths and four-transistor cells. The chips were designed to run with a 5-V power supply, but these tests were performed with the chips in the 2.5-V battery backup mode.

The same set of IMS1601 SRAMs was also flown on board a NASA ER-2 aircraft at 20 km (20 flights over California and 14 flights over Norway). For the Norway flights, 28 EDI81256 256k×1 SRAMs, manufactured by Electronic Designs, Inc., were also included. The EDI81256 has the same type of four-transistor cells as the IMS1601, but is built using smaller $1.1-\mu m$ ground rules in a twin-well CMOS process.

The primary cosmic rays incident upon the atmosphere from space are deflected by the earth's magnetic field. The magnetic field acts as a momentum filter, preventing particles with less than a given momentum from penetrating to certain altitude-latitude combinations. Because the earth's magnetic field is approximately a dipole, the shield effect is maximum at the equator and minimum at the poles. The neutron flux is approximately six times more intense at the poles than it is at the equator. The neutron flux is shown as a function of geographic latitude in Figure 9 (solid line), and is based on neutron measurements by Merker et al. [24] and geomagnetic cutoff values from Adams [25]. A small scale factor was used to adjust the 1-10-MeV flux to a value of 0.85 n/cm²-s at 45° and 12 km altitude [26]. The SERs for the SRAMs appear to track the neutron flux as it increases with latitude (dotted lines connect the data points). The upset rates for the data shown at the two altitudes in Figure 9 differ by a factor of about 10, largely because of the change in chip operating voltages. Upset rates (or SERs) for CMOS devices operated at 2.5 V increased by about a factor of 2 as the altitude was increased from 9 km to 20 km (Figure 10). [Note that the SER sensitivity to pinch voltage differs for bipolar (Figure 6) and CMOS (Figure 9) circuits.] The sea-level data point in Figure 10 shows a higher SER than expected from atmospheric neutrons alone. The sea-level SER measured at 2.5 V probably had



al militare

Cosmic ray SER at aircraft altitudes of a 64Kb CMOS SRAM versus geomagnetic latitude. The solid curve is the 1-10-MeV neutron flux (right scale). The dotted lines connect the data points collected at altitudes of 9 km and 20 km. Data at 9 km were collected from chips operated at 5 V; data at 20 km were collected from chips operated at 2.5 V.

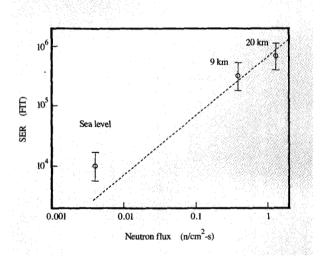


Figure 10

Cosmic ray SER at aircraft altitudes versus atmospheric neutron flux in the energy range from 1 to 10 MeV. The dashed line with a slope of 1 is a linear fit adjusted to pass through the origin for the two data points at high altitude. The chips were tested at 2.5 V. The sea-level measurement falls well above the line because it probably includes a significant SER contribution from alphaparticles.

Table 2 CMOS SRAM soft-error rates at aircraft altitudes. These measurements were performed at 2.5 V to increase their sensitivity so that a sufficiently large number of bit errors could be observed for each SER experiment.

SRAM type (kb)	Operating voltage (V)	Flight latitude (degrees)	Flight altitude (km)	Measured SER (FIT)	Projected SER (FIT)
64	5	54-60	9	1.48×10^{5}	1.18×10^{5}
64	5	44-50	9	1.03×10^{5}	8.52×10^4
64	2.5	39 - 48	9	3.28×10^{5}	2.88×10^{5}
64	2.5	32-40	20	7.20×10^{5}	6.34×10^{5}
64	2.5	59-82	20	1.48×10^{6}	1.51×10^{6}
256	2.5	59-82	20	1.21×10^{6}	2.15×10^{6}

Table 3 Comparison of projected and actual SER at ground level. Projections are based on accelerated testing of memory chips exposed to beams of protons and neutrons. Actual SERs are measured by counting the number of soft errors that occur after operating a large population of chips.

Chip name	Location	Projected SER	Actual SER	
Nitetrain	Essex Junction	7.7×10^4	9.4 × 10 ⁴	
Nitetrain	Boulder	2.81×10^{5}	3.32×10^{5}	
Nitetrain	Leadville	9.35×10^{5}	$1.11 \times 10 \times 10^{6}$	
Blue Spruce	Boulder	6.31×10^{3}	6.58×10^{3}	
Blue Spruce	Leadville	2.06×10^{4}	2.28×10^4	
Vendor 4Mb DRAM	E. Fishkill	7.33×10^{3}	5.95×10^{3}	

a large alpha-particle component, which overwhelmed the smaller cosmic ray component at low altitude.

In addition to this experiment, flight tests of military aircraft equipped with a CC-2E digital computer with semiconductor memory were carried out over two separate areas of Europe during the period of November 1990 through March 1992. The aircraft each contained 1560 of the 64Kb CMOS SRAM chips, which were run in the computer with a nominal 5-V power supply. These chips are identical in type to the 64Kb CMOS SRAM chips used in the measurements in the E-3/AWACS and the NASA ER-2 aircraft, mentioned in the previous paragraph. The status of five monolithic memory units (MMUs) was determined from the logs of these flights. Single bit errors detected by the EDAC circuitry were recorded by the onboard computer, and the computer log was read to determine the number of errors for each flight. Most flights were about five to six hours in duration and were conducted at an altitude of 9 km to optimize the performance of the onboard electronics. Occasionally, portions of a few flights were conducted at lower altitudes. These 5-V and 2.5-V measurements are shown in Table 2.

Correlation to accelerated testing

In each of the four case studies described above, samples of the memory chip used in the field SER tests were independently subjected to testing in proton and neutron beams. The purpose of the testing was to measure the sensitivity of each chip to neutrons and protons as a function of the energy of the particles in the beam. These particles are identical to those generated in the atmosphere by cosmic rays, and they produce the same interactions with memory chips. The details of accelerated testing with particle beams are described by Ziegler et al. [13].

A curve describing the bit-fail cross section determined by this method can then be used to calculate the expected SER due to energetic neutrons and protons in each environment where field tests were performed. The rate at which soft errors occur (i.e., the SER) in a given environment is determined by

$$SER = \int_{0}^{\infty} \sigma(E) f(E) dE, \qquad (2)$$

where $\sigma(E)$ is the bit-fail cross section obtained from the beam testing and f(E) is the flux of neutrons in the environment. Using this calculation, the projected SER at sea level for a vendor's 4Mb DRAM is 7330 FIT. This compares reasonably well to the measured sea-level SER of 5950 FIT.

Nitetrain and Blue Spruce chips were also tested in proton beams to obtain their bit-fail cross sections. The expected SER of each memory chip at each geographic location was calculated on the basis of these measurements [13]. Table 3 shows the projected SER for each chip and location and the actual measured SER at each location. In all cases, the correlation between the projection based on accelerated testing and the actual SER is good to within 30%.

Chips used in the SER measurements at aircraft altitudes were similarly tested [13]. Bit-fail cross-section data were obtained at low energies (<65 MeV) with a neutron beam at Crocker Nuclear Laboratory at the University of California–Davis, in addition to proton beam measurements at higher energies. The differential energy spectrum of neutrons in the upper atmosphere is based on measurements by NASA at 12 km [14]. The SERs of the SRAMs were projected for the average latitude and altitude of each of the series of flight tests. The results of these calculations appear in Table 2 along with the measured values. Again, the correlation of the projected error rates from beam testing to the measured rates is reasonably good.

Conclusions

The IBM experiments relating to cosmic ray SER as of this date have been briefly summarized. The ground-level and underground field SER tests show that, at the chip level, cosmic rays can be the dominant cause of soft errors observed in a variety of memory circuit types manufactured in n-MOS, CMOS, and bipolar technologies. The particle-beam experiments show that neutrons and protons can induce soft errors under controlled laboratory conditions, and projections based on this accelerated testing are very close to the measured SER in numerous cases. The multiple-error data show that cosmic ray events can be more severe than alpha-particle events. A memory chip that is completely immune to alpha-particle radiation may still be sensitive to cosmic rays. Shielding chips under several feet of concrete or its equivalent can significantly reduce the SER due to cosmic rays.

References

- D. C. Bossen and M. Y. Hsiao, "A System Solution to the Memory Soft Error Problem," *IBM J. Res. Develop.* 24, No. 3, 390-397 (May 1980).
- T. C. May and M. H. Woods, "Alpha-Particle-Induced Soft Errors in Dynamic Memories," *IEEE Trans. Electron Devices* ED-26, 2 (1979).
- 3. D. S. Yaney, J. T. Nelson, and L. L. Vanskike, "Alpha Particle Tracks in Silicon and Their Effect on Dynamic MOS RAM Reliability," *IEEE Trans. Electron Devices* ED-26, No. 1, 10-16 (January 1979).
- J. F. Ziegler and W. A. Lanford, "Effect of Cosmic Rays on Computer Memories," Science 206, 776-788 (November 16, 1979).
- J. F. Ziegler, H. W. Curtis, H. P. Muhlfeld, C. J. Montrose, B. Chin, M. Nicewicz, C. A. Russell, W. Y. Wang, L. B. Freeman, P. Hosier, L. E. LaFave, J. L. Walsh, J. M. Orro, G. J. Unger, J. M. Ross, T. J. O'Gorman, B. Messina, T. D. Sullivan, A. J. Sykes, H. Yourke, T. A. Enger, V. Tolat, T. S. Scott, A. H. Taber, R. J. Sussman, W. A. Klein, and C. W. Wahaus, "IBM Experiments in Soft Fails in Computer Electronics (1978–1994)," IBM J. Res. Develop. 40, No. 1, 3–18 (1996, this issue).
- H. H. K. Tang, "Nuclear Physics of Cosmic Ray Interaction with Semiconductor Materials: Particle-Induced Soft Errors from a Physicist's Perspective," *IBM J. Res. Develop.* 40, No. 1, 91–108 (1996, this issue).
- G. A. Sai-Halasz, "Monte Carlo Modeling of the Transport of Ionizing Radiation Created Carriers in Integrated Circuits," *IEEE Electron Device Lett.* EDL-1, No. 10, 2111–2113 (October 1980).
- 8. G. A. Sai-Halasz and D. D. Tang, "Soft Error Rate in Static Bipolar RAMs," *IEEE IEDM Tech. Digest* 83, 344-346 (1983).
- G. R. Srinivasan, H. K. Tang, and P. C. Murley, "Parameter-Free, Predictive Modeling of Single Event Upsets Due to Protons, Neutrons, and Pions in Terrestrial Cosmic Rays," *IEEE Trans. Nucl. Sci.* 41, 2063–2070 (1994).
- G. R. Srinivasan, P. C. Murley, and H. H. K. Tang, "Accurate, Predictive Modeling of Soft Error Rate Due to Cosmic Rays and Chip Alpha Radiation," Proceedings of the 32nd Annual IEEE International Reliability Physics Symposium, April 1994, pp. 12–16.
- G. R. Srinivasan, "Modeling the Cosmic-Ray-Induced Soft-Error Rate in Integrated Circuits: An Overview," IBM J. Res. Develop. 40, No. 1, 77-89 (1996, this issue).

- 12. P. C. Murley and G. R. Srinivasan, "Soft-Error Monte Carlo Modeling Program, SEMM," *IBM J. Res. Develop.* **40**, No. 1, 109–118 (1996, this issue).
- J. F. Ziegler, H. P. Muhlfeld, C. J. Montrose, H. W. Curtis, T. J. O'Gorman, and J. M. Ross, "Accelerated Testing for Cosmic Soft-Error Rate," *IBM J. Res. Develop.* 40, No. 1, 51–72 (1996, this issue).
- T. J. O'Gorman, "The Effect of Cosmic Rays on the Soft Error Rate of a DRAM at Ground Level," *IEEE Trans.* Electron Devices 41, No. 4, 553-557 (April 1994).
- B. F. Fitzgerald and E. P. Thoma, "A 288K-bit Dynamic Random Access Memory," ISSCC Digest, p. 64 (February 1982)
- C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "Collection of Charge from Alpha-Particle Tracks in Silicon Devices," *IEEE Trans. Electron Devices* ED-30, No. 6, 686-693 (June 1983).
- Radiological Health Handbook, U.S. Dept. of Health, Education, and Welfare, Washington, DC, January 1970, pp. 110-113.
- Ž. Hasnain and A. Ditali, "Building-In Reliability: Soft Errors—A Case Study," Proceedings of the 30th Annual IEEE International Reliability Physics Symposium, 1992, pp. 276–280.
- R. Saxena, "Ground Level Atmospheric Neutron Flux Measurements in the 10-170 MeV Range," Ph.D. thesis, University of New Hampshire, May 1990.
- J. F. Ziegler, "Terrestrial Cosmic Rays," IBM J. Res. Develop. 40, No. 1, 19-39 (1996, this issue).
- C. Lage, D. Burnett, T. McNelly, K. Baker, A. Bormann, D. Dreier, and V. Soorholtz, "Soft Error Rate and Stored Charge Requirements in Advanced High-Density SRAMs," *IEDM Tech. Digest*, pp. 821–824 (1993).
- 22. A. Taber and E. Normand, "Investigation and Characterization of SEU Effects and Hardening Strategies in Avionics," *Report No. 92-L75-020*, Loral Federal Systems Co., Owego, NY, August 26, 1992.
- 23. A. Taber and E. Normand, "Single Event Upsets in Avionics," *IEEE Trans. Nucl. Sci.* 40, 120-126 (April 1993)
- M. Merker, E. S. Light, H. J. Verschell, R. B. Mendell, and S. A. Korff, "Time Dependent Worldwide Distribution of Atmospheric Neutrons and Their Products" I. Geophys. Res. 78, 2727 (1973)
- Products," J. Geophys. Res. 78, 2727 (1973).

 25. J. Adams, "Cosmic Ray Effects on Microelectronics," Report No. 5901, Naval Research Laboratory, Washington, DC, 1986.
- J. Hewitt, L. Hughes, J. W. Baum, A. V. Kuehner, J. B. McCaslin, A. Rindi, A. R. Smith, L. D. Stephens, R. H. Thomas, R. V. Griffith, and C. G. Welles, "Ames Collaborative Study of Cosmic Ray Neutrons and Mid-Latitude Flights," Health Phys. 34, 375 (1978).

Received November 10, 1994; accepted for publication February 28, 1995

Timothy J. O'Gorman IBM Microelectronics Division, Burlington facility, Essex Junction, Vermont 05452 (OGORMAN at BTVLABVM, ogorman@vnet.ibm.com).

Mr. O'Gorman received the B.S. degree in physics from Manhattan College, Bronx, New York, in 1976, and the M.S. degree in physics from Pennsylvania State University, State College, Pennsylvania, in 1978. He joined the IBM General Technology Division in Burlington, Vermont, in 1981. Since then he has worked in semiconductor reliability engineering.

Mr. O'Gorman's main interests have been in radiation-induced soft errors in memory chips. He is currently working on reliability modeling of CMOS circuits.

John M. Ross IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (JMROSS at FSHVMFK1, jmross@vnet.ibm.com). Mr. Ross is an electrical engineer in the Storage Subsystems and Interface Products Department of the IBM Microelectronics Division. He received a B.S. degree in electrical engineering from Virginia Polytechnic Institute and State University in 1989, and an M.S. degree in electrical engineering from Columbia University in 1993. Mr. Ross joined IBM in 1989 at the East Fishkill facility, where he became involved in the study of soft errors in computer memories. He is currently working on the design of high-performance multibyte interface circuits.

Allen H. Taber Loral Federal Systems Company, Route 17C, Owego, New York 13827 (ATABER at OWGVM3, ataber@owgvm3.vnet.ibm.com). Since 1992, Mr. Taber has managed the Electromagnetic Effects group at Loral Federal Systems in Owego, New York. Prior to the sale of IBM Federal Systems to Loral, he was an advisory engineer/scientist in this same group. He was responsible for nuclear survivability and single-event upset research and evaluation on many types of semiconductor devices and systems, including the E3/AWACS, Space Shuttle, and Space Station programs. From 1984 to 1986, Mr. Taber was a member of the IBM Owego Memory System Development group, where he designed a set of nonvolatile data storage cards for the North Warning System. Until 1984, he was a member of Monolithic Memory Devices at IBM in Manassas, Virginia. In that group, he obtained experience in radiation effects and device physics by performing transient upset, total dose, single-particle upset, SCR latchup, data retention, and performance testing on monolithic memory devices. Mr. Taber received his B.S. in physics in 1977 from the College of William and Mary, Williamsburg, Virginia.

James F. Ziegler IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ZIEGLER at YKTVMV, ziegler@watson.ibm.com). After receiving B.S., M.S., and Ph.D. degrees from Yale, Dr. Ziegler joined IBM in 1967 at the Thomas J. Watson Research Center, where he now manages the Material Analysis and Radiation Effects group. Most of his research concerns the interaction of radiation with matter. Dr. Ziegler is the author of over 130 publications and 14 books; he holds 11 U.S. patents. He received IBM Corporate Awards in 1981 and 1990. Dr. Ziegler is a Fellow of the American Physical Society and of the IEEE. He has been awarded the von Humboldt Senior Scientist Prize by the German government.

Hans P. Muhlfeld IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (MUHLFELD at FSHVMFKI). Mr. Muhlfeld is an advisory engineer in Reliability Services at the IBM East Fishkill facility. He joined the Military Products Division of IBM in 1957 at Kingston, New York. After two years at a SAGE installation at McCord AFB, Tacoma, Washington, he joined the memory development area of SMD in Poughkeepsie, New York, where he was involved in memory testing and memory tester design. In 1986 he joined Reliability Services in East Fishkill, designing test equipment and testing for soft fails in memory chips.

Charles J. Montrose IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (MONTROSE at FSHVMFK1). Mr. Montrose is an advisory engineer in the Reliability Services Department at the East Fishkill facility. His responsibilities include test system design, system control software, and data acquisition. He joined IBM in 1982, after receiving a B.S. degree in electrical engineering from the New Jersey Institute of Technology. He was initially involved in the design of a custom high-speed driver/receiver chip for a high-performance test system.

Huntington W. Curtis IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (CURTIS at YKTVMV, curtis@watson. ibm.com). Dr. Curtis received a B.S. in chemistry and physics from the College of William and Mary in 1942, an M.S. in physics and electrical engineering from the University of New Hampshire in 1948, and a Ph.D. in electrical engineering from the State University of Iowa in 1950. Prior to joining IBM, he was a professor of electrical engineering at Dartmouth College. Dr. Curtis joined IBM in 1959, becoming a senior engineer in 1960. After serving as manager of technical requirements at FSD headquarters, he was promoted to technical advisor to the IBM Vice President for Research and Engineering, followed by assignments on the IBM Corporate engineering staff as director of government technical liaison and as director of scientific and technical information. He held subsequent positions as engineering consultant for IBM Biomedical Systems and engineering consultant for Manufacturing Research. Dr. Curtis retired from IBM in 1993 and is now an emeritus scientist at the IBM Thomas J. Watson Research Laboratory. He is a member of Phi Beta Kappa, Tau Beta Pi, and Sigma Xi, a senior member of the Institute of Electrical and Electronics Engineers, and a trustee of the Mount Washington Observatory.

James L. Walsh IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533. Mr. Walsh, who joined IBM in 1952, has had various assignments in advanced technology and product areas. He managed the cosmic ray soft-error program at the East Fishkill site and was involved with experimental testing and modeling of chips, as well as coordinating efforts on soft errors between IBM divisions. Mr. Walsh received a B.S. in electrical engineering from the University of Rhode Island in 1949, and an M.A. in physics from Hofstra University in 1952. In 1990, Mr. Walsh retired from IBM; he is an IBM Fellow.