# **HEF4081B**

## **Quad 2-input AND gate**

Rev. 7 — 16 November 2011

Product data sheet

## 1. General description

The HEF4081B is a quad 2-input AND gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

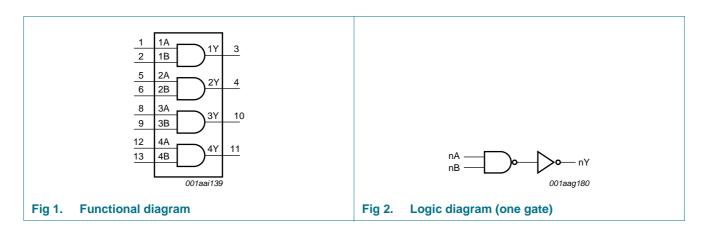
## 3. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +125 °C.

Type number	Package								
	Name	Description	Version						
HEF4081BP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1						
HEF4081BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1						

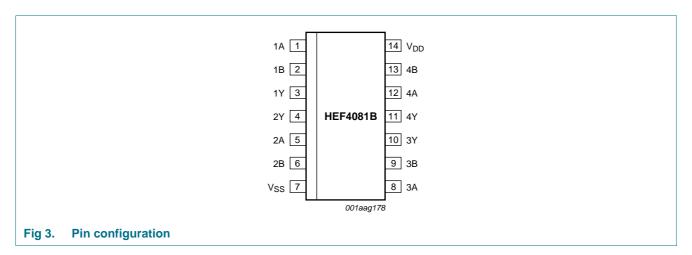
## 4. Functional diagram





## 5. Pinning information

### 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 5, 8, 12	input
1B to 4B	2, 6, 9, 13	input
1Y to 4Y	3, 4, 10, 11	output
V <sub>SS</sub>	7	ground (0 V)
$V_{DD}$	14	supply voltage

## 6. Functional description

Table 3. Function table[1]

Input		Output				
nA	nB	nY				
L	L	L				
L	Н	L				
Н	L	L				
Н	Н	Н				

[1] H = HIGH voltage level; L = LOW voltage level.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V<sub>SS</sub> = 0 V (ground).

					-
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	$V_{DD} + 0.5$	V
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+125	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to + } 125  ^{\circ}\text{C}$			
		DIP14	<u>[1]</u> -	750	mW
		SO14	[2] _	500	mW
Р	power dissipation	per output	-	100	mW

<sup>[1]</sup> For DIP14 packages: above  $T_{amb}$  = 70 °C,  $P_{tot}$  derates linearly with 12 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
VI	input voltage		0	$V_{DD}$	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{DD} = 5 V$	-	3.75	μs/V
		V <sub>DD</sub> = 10 V	-	0.5	μs/V
		V <sub>DD</sub> = 15 V	-	0.08	μs/V

### 9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$  V;  $V_{I} = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V

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<sup>[2]</sup> For SO14 packages: above  $T_{amb} = 70$  °C,  $P_{tot}$  derates linearly with 8 mW/K.

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 Table 6.
 Static characteristics ...continued

 $V_{SS} = 0 \ V$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	T <sub>amb</sub> =	–40 °C	T <sub>amb</sub> =	+25 °C	T <sub>amb</sub> =	+85 °C	T <sub>amb</sub> =	+125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	HIGH-level	$ I_O  < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
OL -	LOW-level	$ I_{O}  < 1 \mu A$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	$V_0 = 2.5 \text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mΑ
		$V_0 = 4.6 \text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mΑ
		$V_0 = 9.5 V$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mΑ
		$V_{O} = 13.5 \text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level	$V_0 = 0.4 \ V$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mΑ
	output current	$V_{O} = 0.5 \ V$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mΑ
		$V_0 = 1.5 \text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mΑ
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μΑ
$I_{DD}$	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μΑ
		combinations; $I_O = 0 A$	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μΑ
		10 – 0 Å	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μΑ
C <sub>I</sub>	input capacitance			-	-	-	7.5	-	-	-	-	pF

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

 $T_{amb}$  = 25 °C; for waveforms see Figure 4; for test circuit see Figure 5; unless otherwise specified. [1]

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Тур	Max	Unit
$t_{PHL}$	HIGH to LOW	nA or nB to nY	5 V	28 ns + $(0.55 \text{ ns/pF})C_L$	-	55	110	ns
	propagation delay		10 V	14 ns + (0.23 ns/pF)C <sub>L</sub>	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C <sub>L</sub>	-	20	40	ns
t <sub>PLH</sub>	LOW to HIGH	nA or nB to nY	5 V	18 ns + $(0.55 \text{ ns/pF})C_L$	-	45	90	ns
propagati	propagation delay		10 V	9 ns + (0.23 ns/pF)C <sub>L</sub>	-	20	40	ns
			15 V	7 ns + $(0.16 \text{ ns/pF})C_L$	-	15	30	ns
$t_{THL}$	HIGH to LOW output		5 V	10 ns + $(1.0 \text{ ns/pF})C_L$	-	60	120	ns
	transition time		10 V	9 ns + $(0.42 \text{ ns/pF})C_L$	-	30	60	ns
			15 V	6 ns + $(0.28 \text{ ns/pF})C_L$	-	20	40	ns
t <sub>TLH</sub>	LOW to HIGH output		5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns

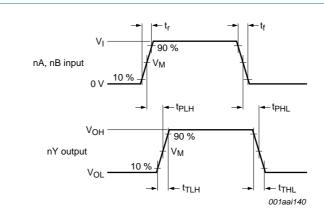
<sup>[1]</sup> The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C<sub>L</sub> in pF).

Table 8. Dynamic power dissipation

 $V_{SS} = 0 \ V; \ t_f = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$ 

Symbol	Parameter	$V_{DD}$	Typical formula	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 450 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	f <sub>i</sub> = input frequency in MHz;
		10 V	$P_D = 2900 \times f_i + \Sigma (f_0 \times C_L) \times V_{DD}^2 (\mu W)$	f <sub>o</sub> = output frequency in MHz;
		15 V	$P_D = 11700 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	$C_L$ = output load capacitance in pF;
				$\Sigma(f_0 \times C_L)$ = sum of the outputs;
				$V_{DD}$ = supply voltage in V.

### 11. Waveforms



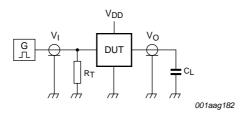
Measurement points are given in Table 9.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 4. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	V <sub>M</sub>	V <sub>M</sub>
5 V to 15 V	0.5V <sub>DD</sub>	0.5V <sub>DD</sub>



Test data is given in <u>Table 10</u>.

Definitions for test circuit:

DUT = Device Under Test.

C<sub>L</sub> = load capacitance including jig and probe capacitance.

 $R_T$  = termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

Fig 5. Test circuit

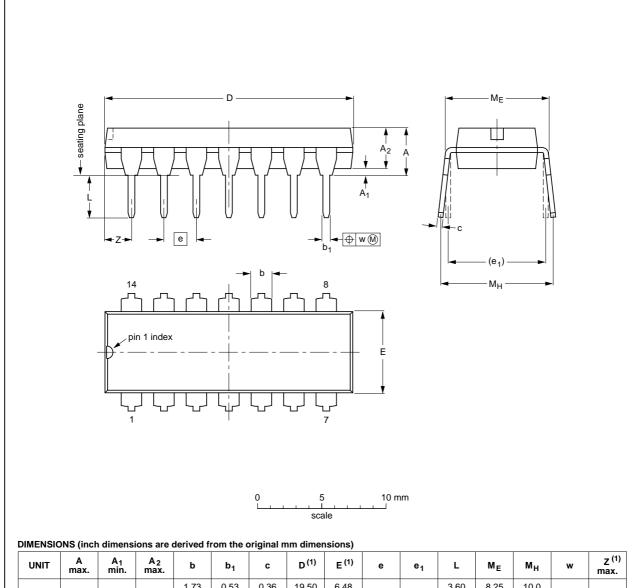
Table 10. Test data

Supply voltage	Input		Load
$V_{DD}$	VI	t <sub>r</sub> , t <sub>f</sub>	CL
5 V to 15 V	$V_{SS}$ or $V_{DD}$	≤ 20 ns	50 pF

## 12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	Мн	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

#### Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

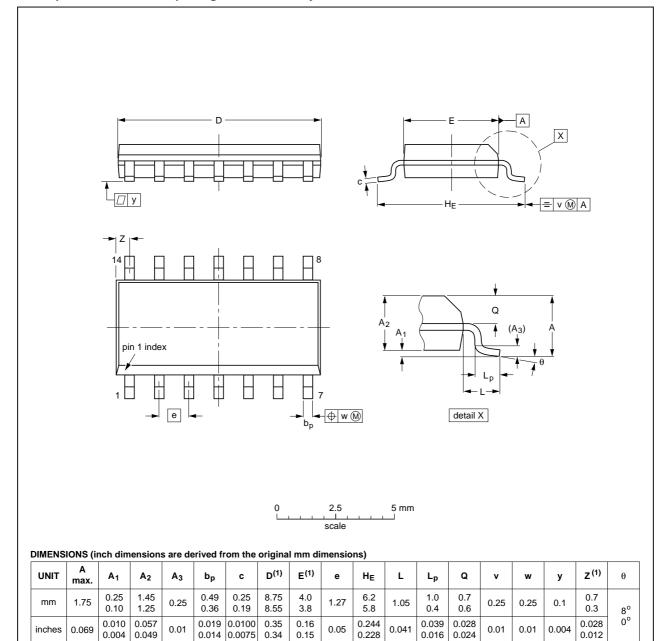
OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT27-1	050G04	MO-001	SC-501-14			<del>99-12-27</del> 03-02-13

Fig 6. Package outline SOT27-1 (DIP14)

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig 7. Package outline SOT108-1 (SO14)

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## 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4081B v.7	20111116	Product data sheet	-	HEF4081B v.6
Modifications:	• Table 6: I <sub>OH</sub>	minimum values changed to m	aximum	
HEF4081B v.6	20091202	Product data sheet	-	HEF4081B v.5
HEF4081B v.5	20090629	Product data sheet	-	HEF4081B v.4
HEF4081B v.4	20080526	Product data sheet	-	HEF4081B_CNV v.3
HEF4081B_CNV v.3	19950101	Product specification	-	HEF4081B_CNV v.2
HEF4081B_CNV v.2	19950101	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
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