Thermal Issues of 3D ICs

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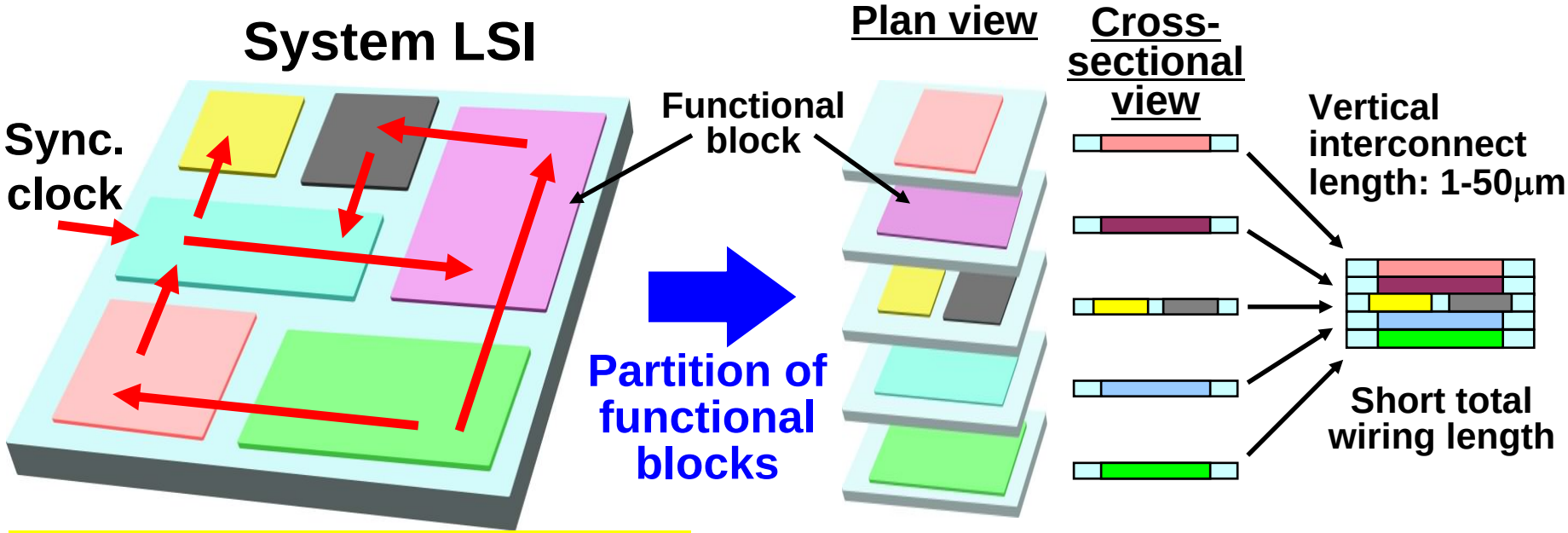
Outline

1. Background
2. 3D Integration Technology in Tohoku University
3. Thermal Characteristics Evaluation of 3D LSI by Simulation and Experiments
4. Summary

Advantages of 3D Integration Technology

1. Short interconnect length
2. High packing density
3. High-speed operation
4. Low power consumption
5. Parallel processing
6. New functionality
7. New applications



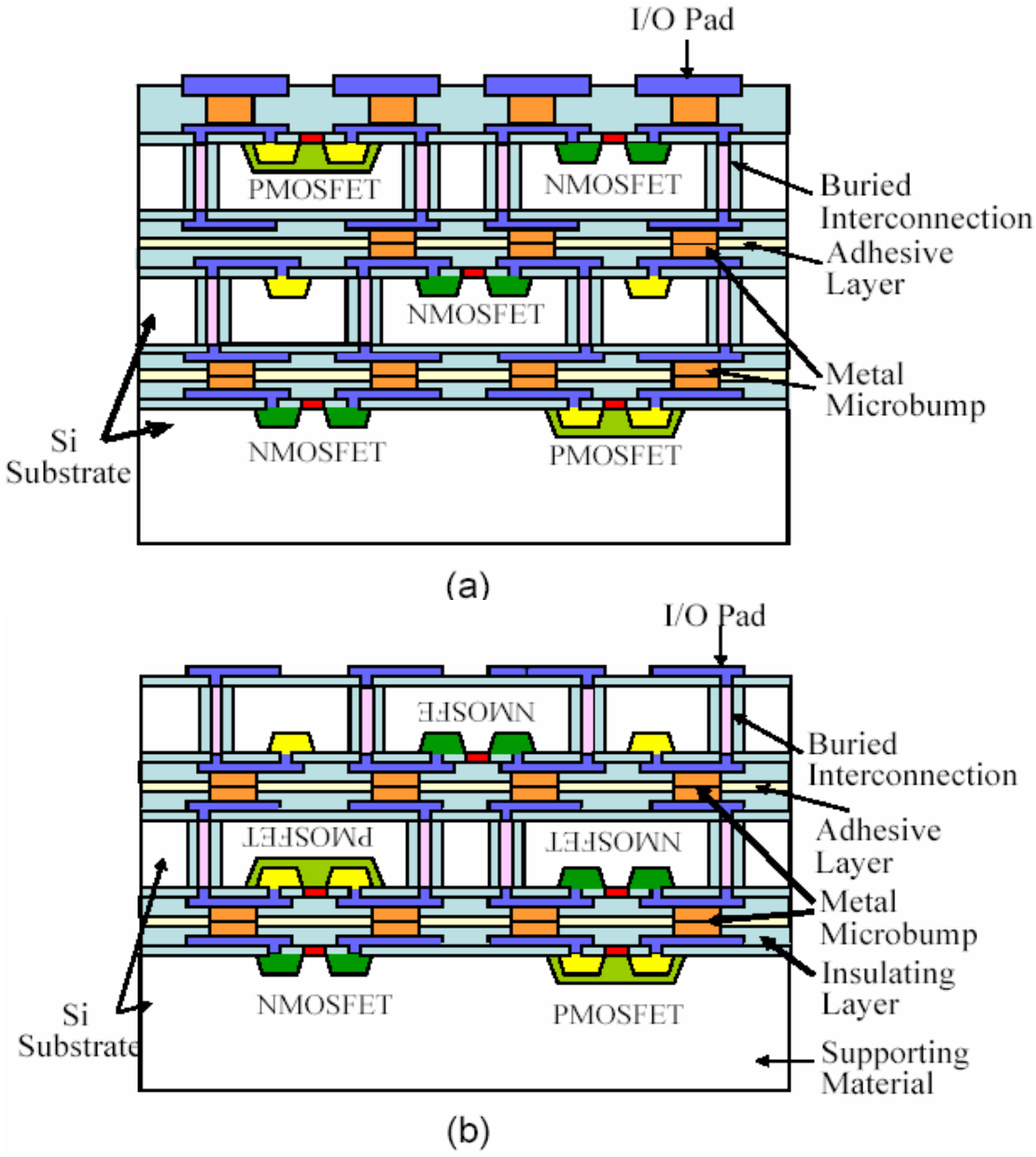
Big concerns: Long wiring
Global wiring

Conventional 2D LSI

Replaced by vertical interconnections

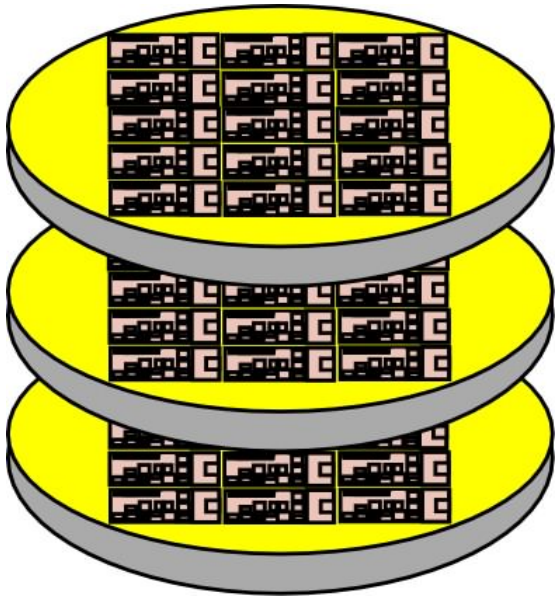
3D stacked LSI

Cross-Sectional Structure of 3D LSI



3D Technology Based on Wafer-to-Wafer Bonding in Tohoku University

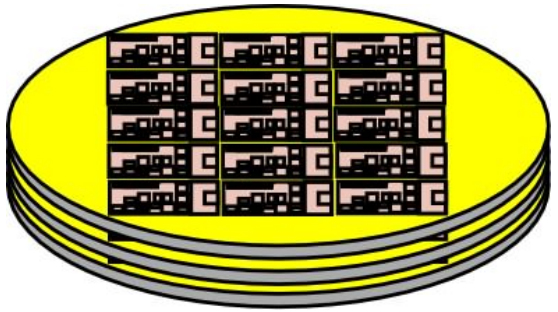
Completed LSI wafers with TSVs



Wafer-to-wafer bonding

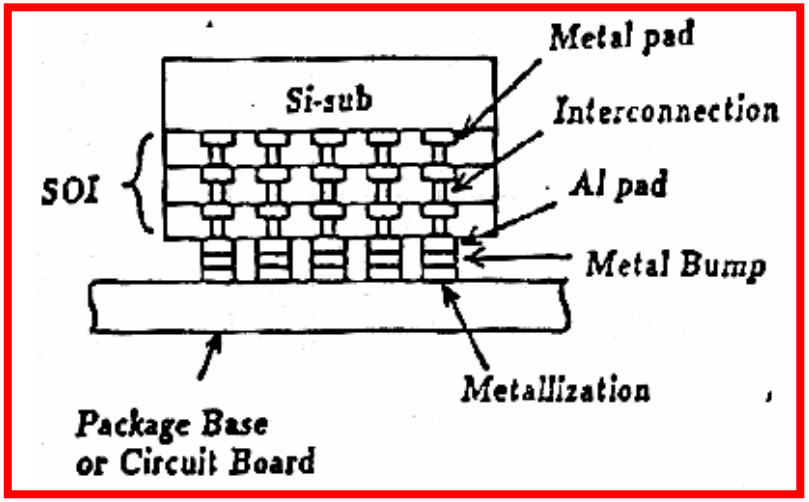
Wafer thinning

3D LSI



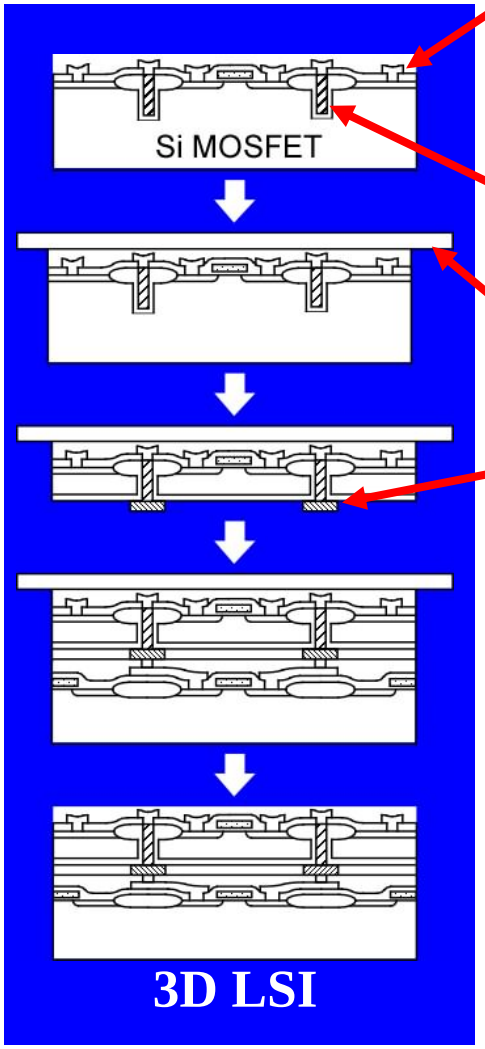
First Proposal of Wafer-to-Wafer Bonding Technique (1989)

3D Projects in Tohoku Univ. (Koyanagi Group)



M. Koyanagi,
Proc. 8th Symposium on Future Electron Devices, pp.50-60 (Oct. 1989)

H. Takata, M. Koyanagi et. al., Proc. Intern. Semiconductor Device Research Symposium, pp.327-330 (Dec. 1991)



A completed LSI wafer

TSV

Supporting substrate

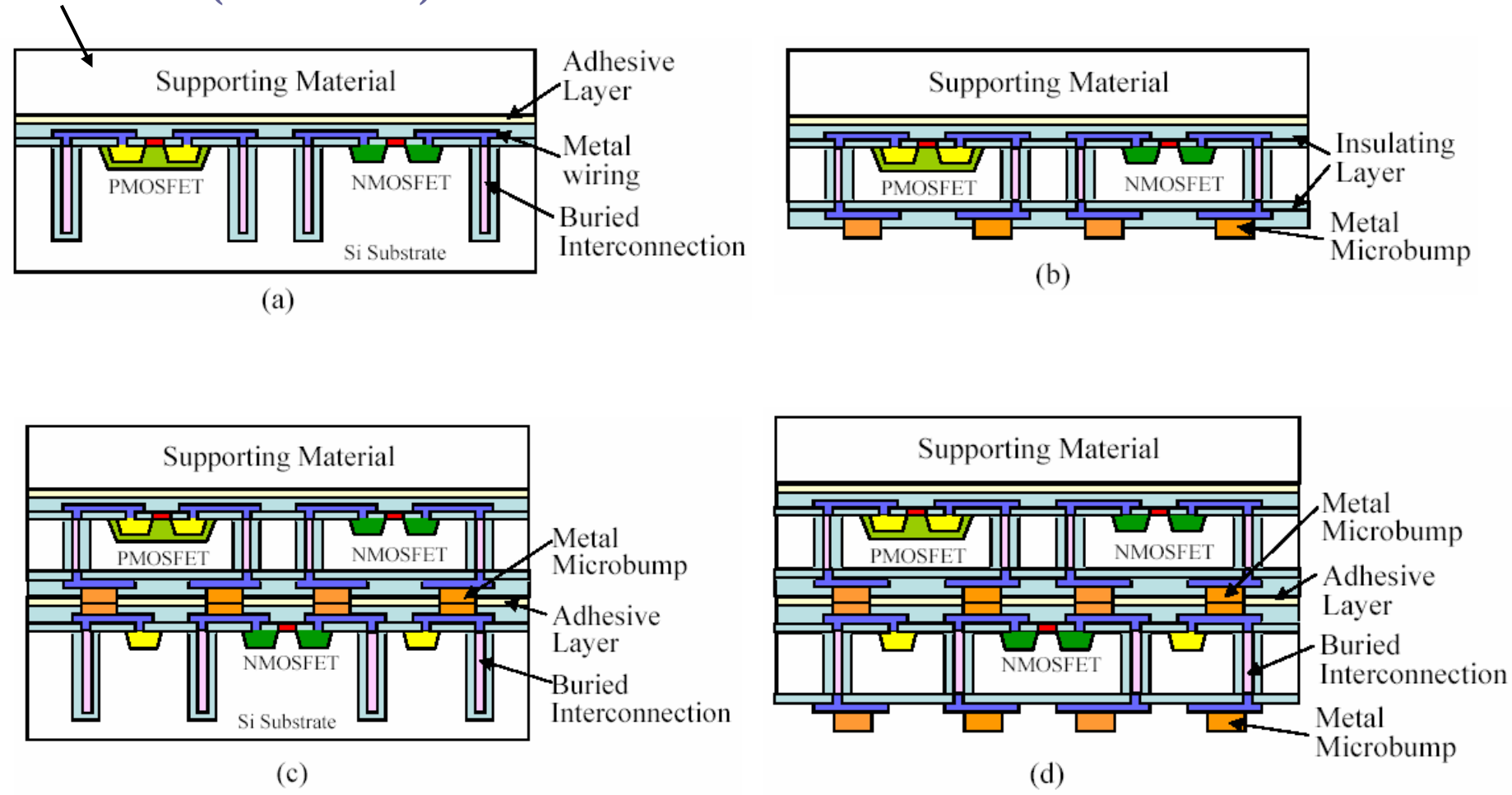
Metal microbump

Additional wafer stacking

Removal of supporting substrate

Fabrication Sequence of 3D LSI

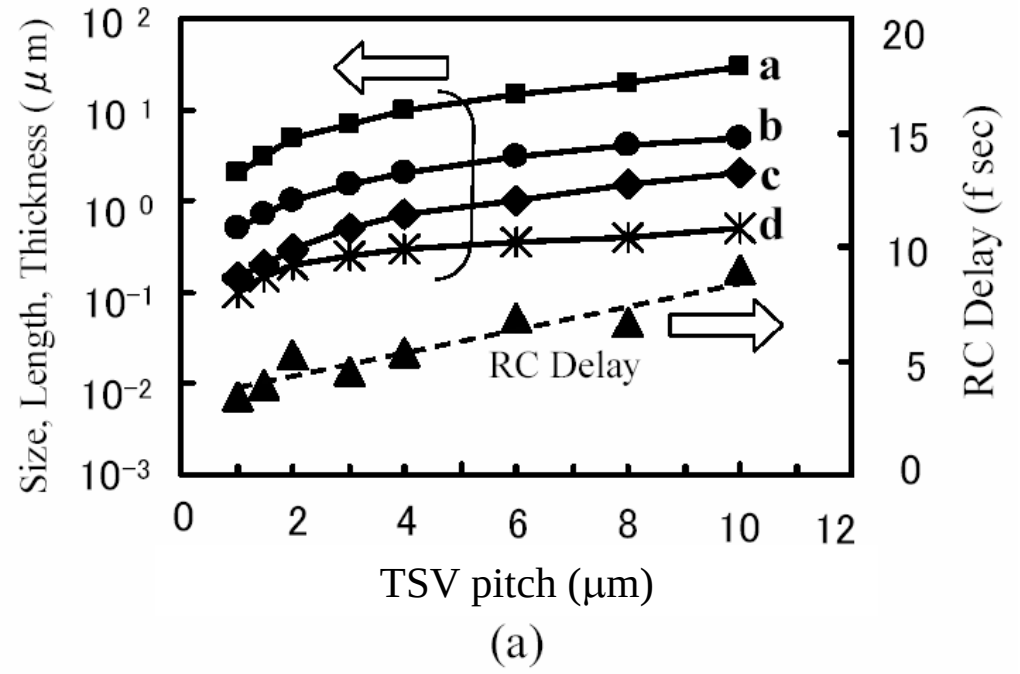
LSI wafer (face-to-face)



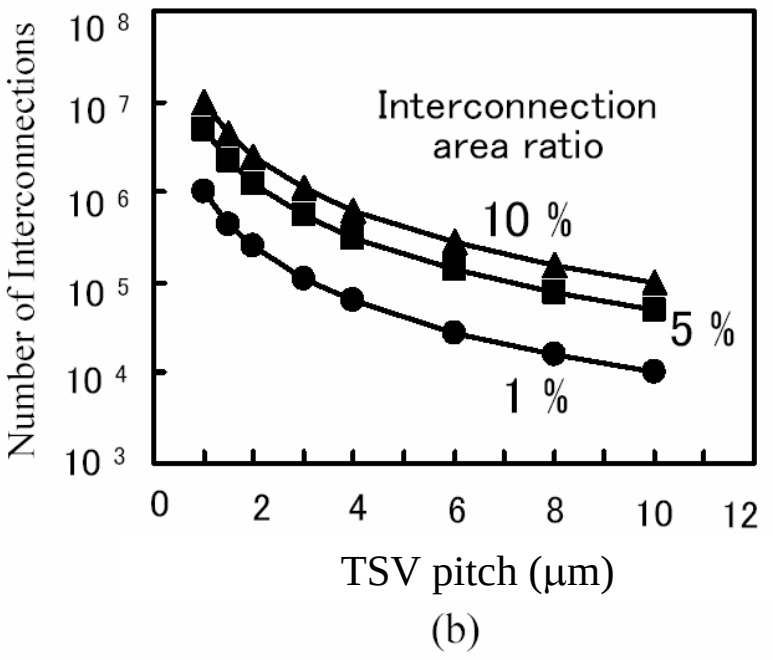
Scaling Capability of TSVs

a: TSV (W) length, b: microbump width

c: TSV diameter, d: insulator (SiO_2) thickness

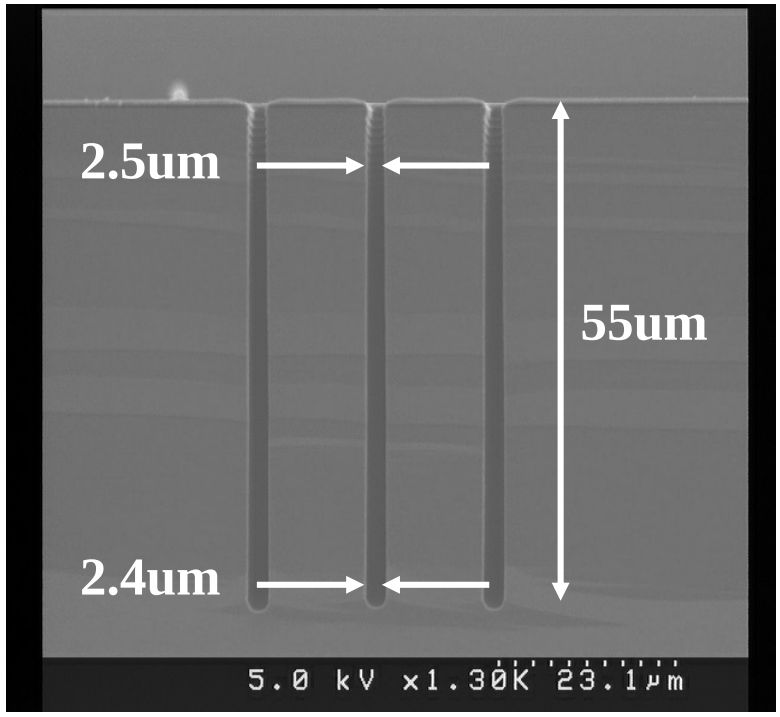


(a)

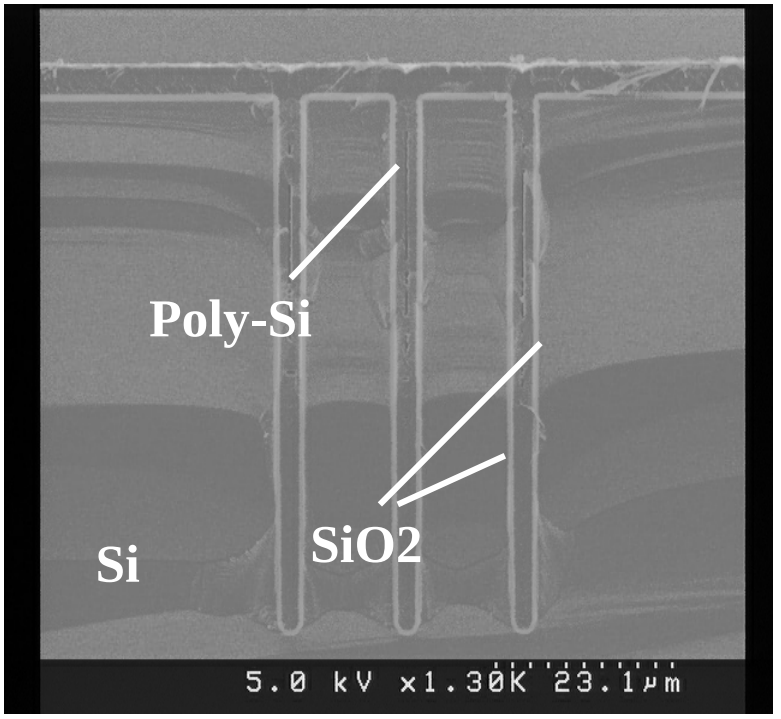


(b)

SEM Cross Section of Poly-Si TSV

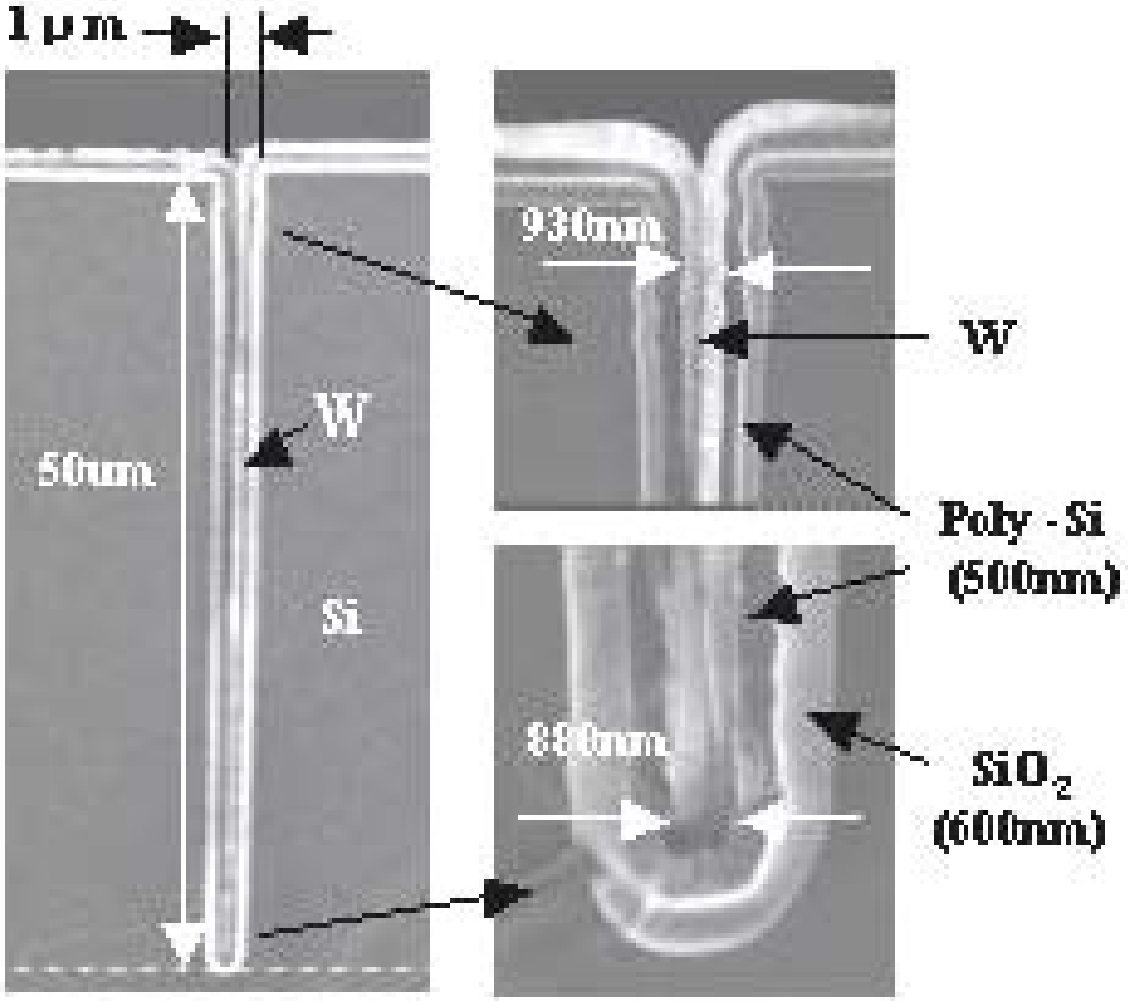


(a) Si deep trench etching

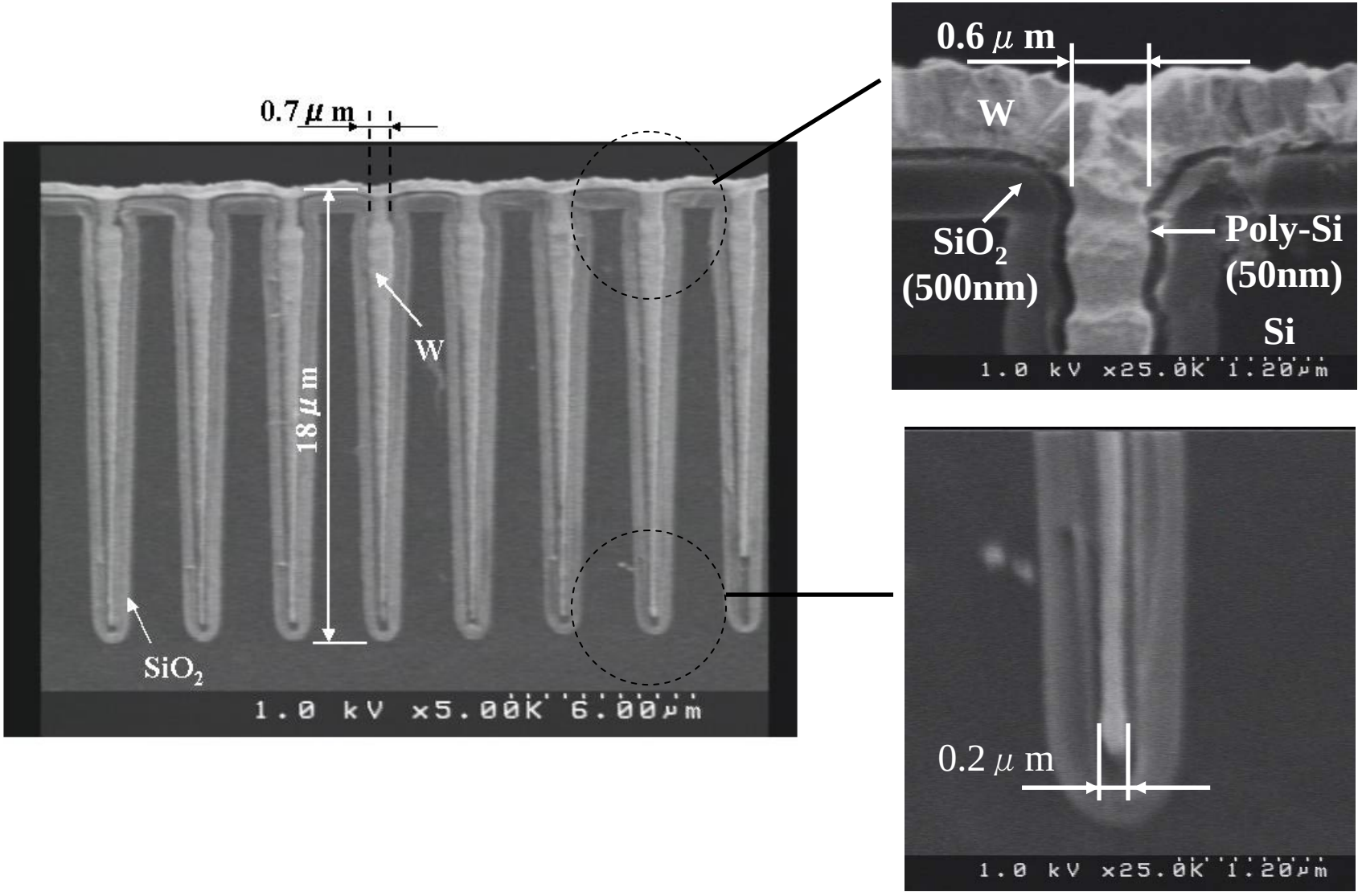


(b) Filling with Poly-Si

SEM Cross Section of Tungsten TSV



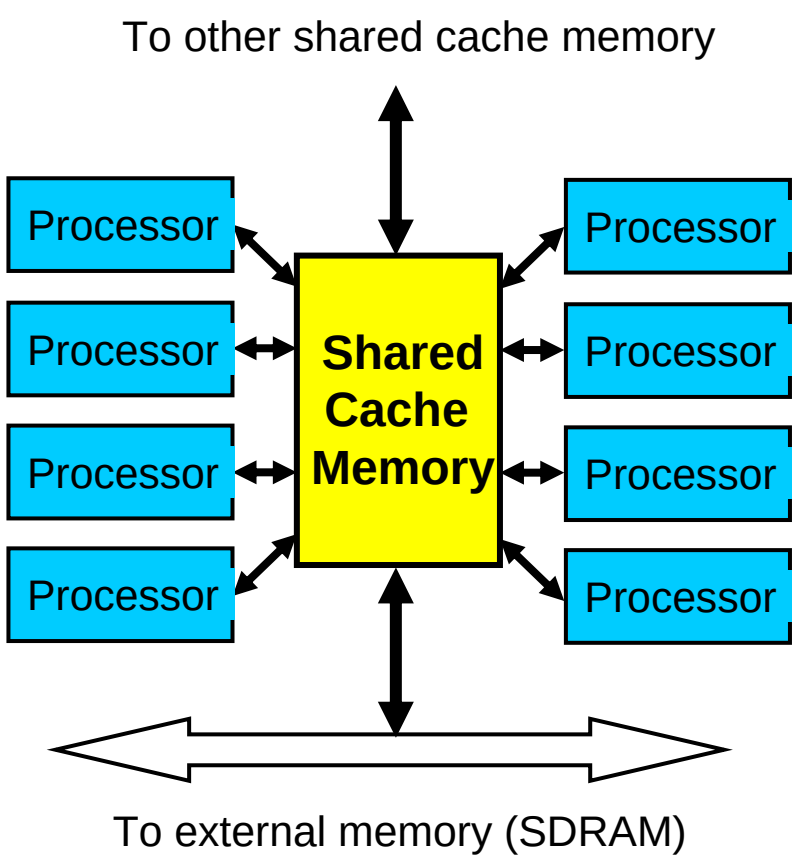
SEM Cross Section of Tungsten TSV with Smaller Diameter

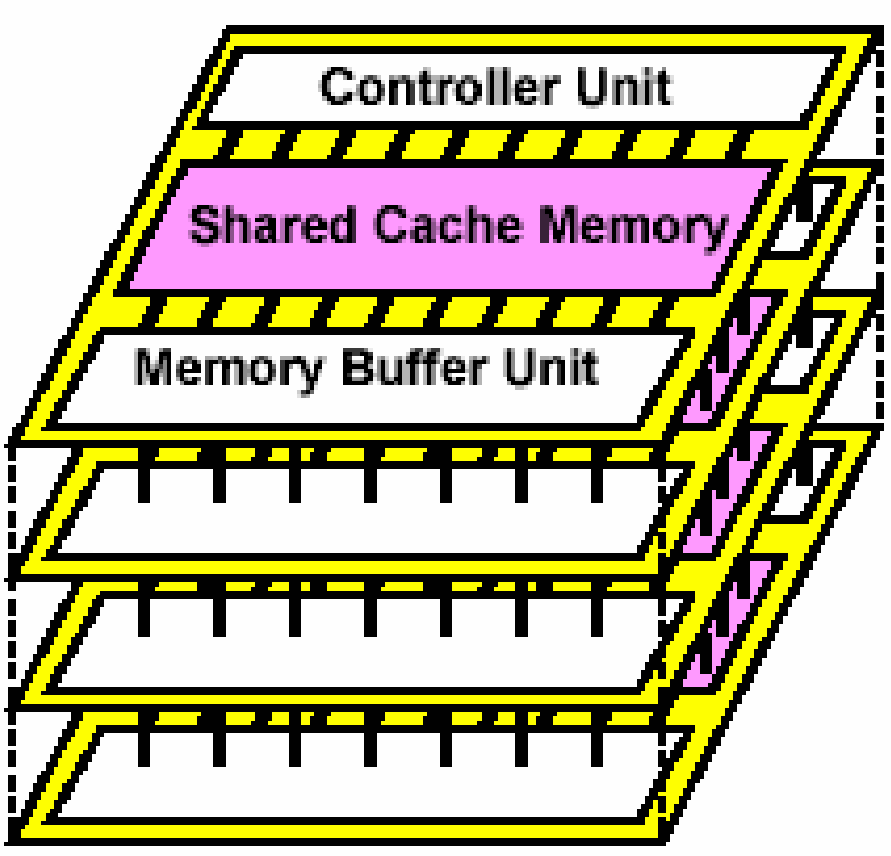


3D LSI Test Chips Fabricated in Tohoku University

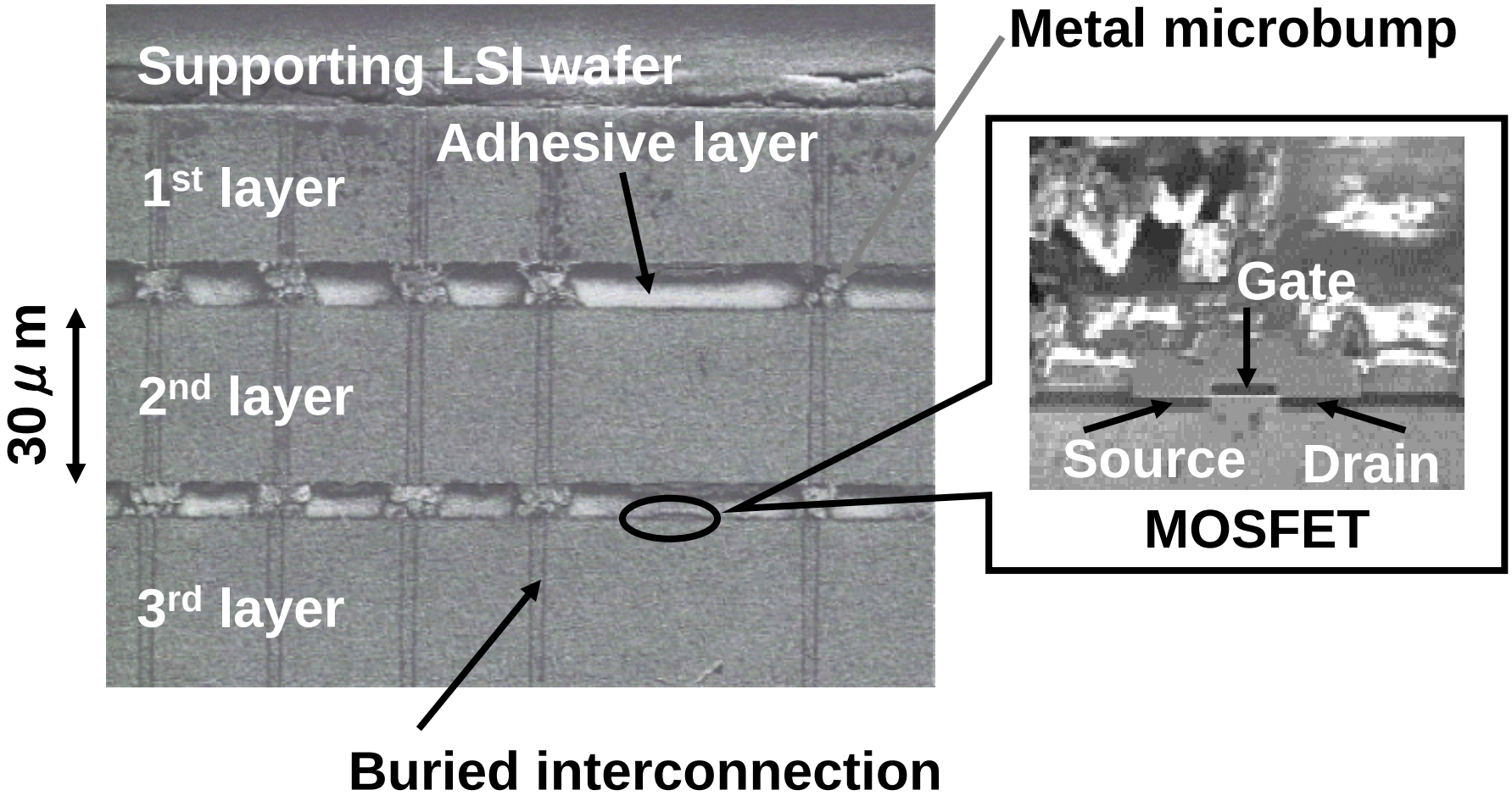
- 3-layer stacked image sensor chip (IEDM, 1999)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked memory chip (IEDM, 2000)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked artificial retina chip (ISSCC, 2001)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked microprocessor chip (**Cool Chips**, 2002)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 10-layer stacked memory chip (IEDM, 2005)
  Chip-to-wafer bonding (Self assembly, Buried interconnection)

Shared Cache Memory with 3D Structure

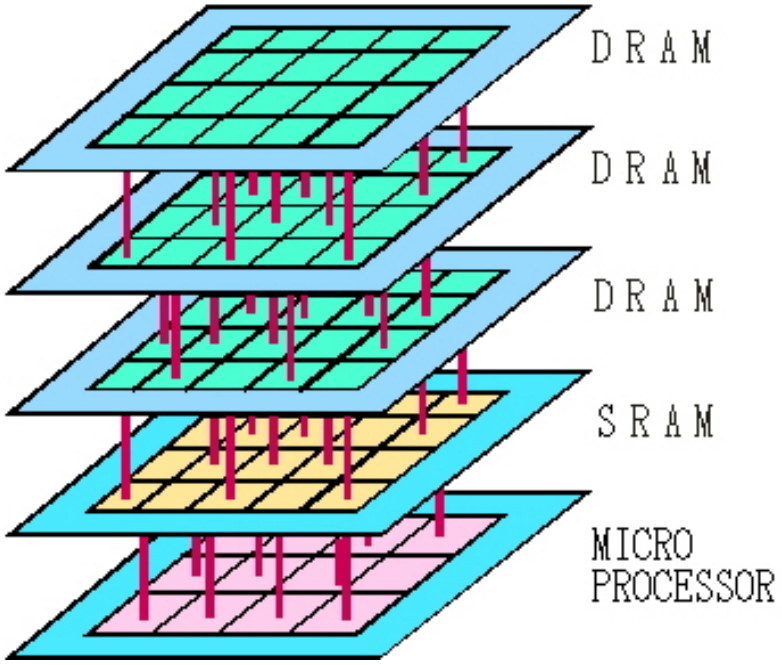


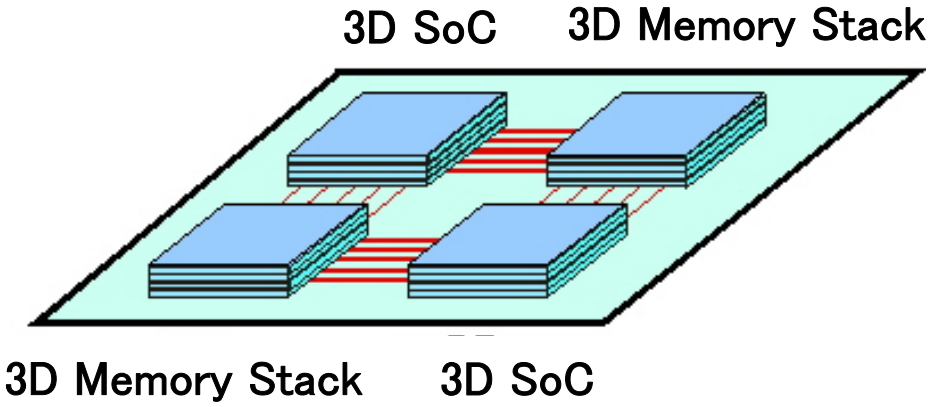


SEM Cross-Sectional View of 3D Microprocessor Chip Fabricated by Wafer-to-Wafer Bonding

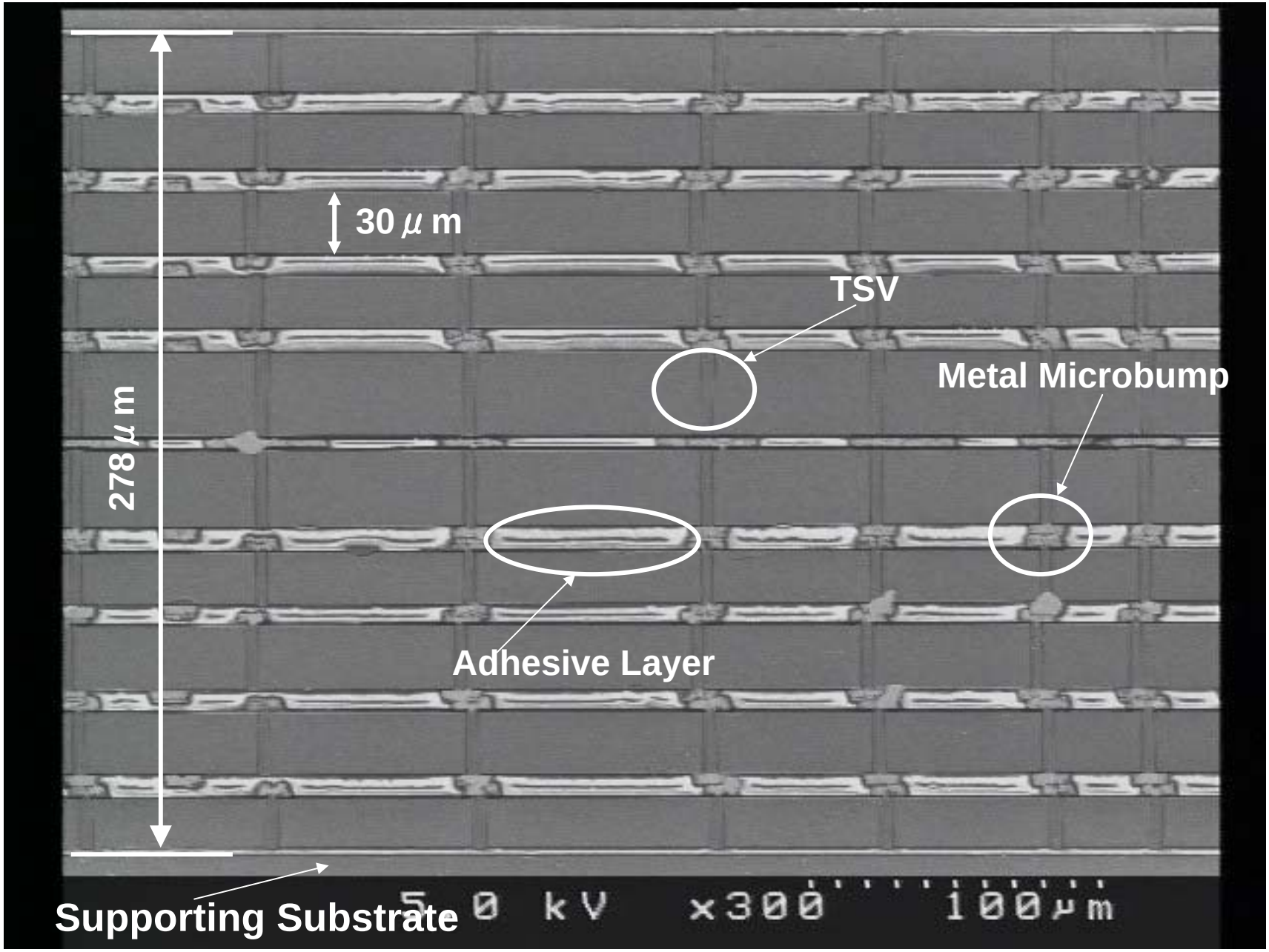


3D Microprocessor and 3D Multi-chip Module





SEM Cross Section of 3D Memory with 10 Layers



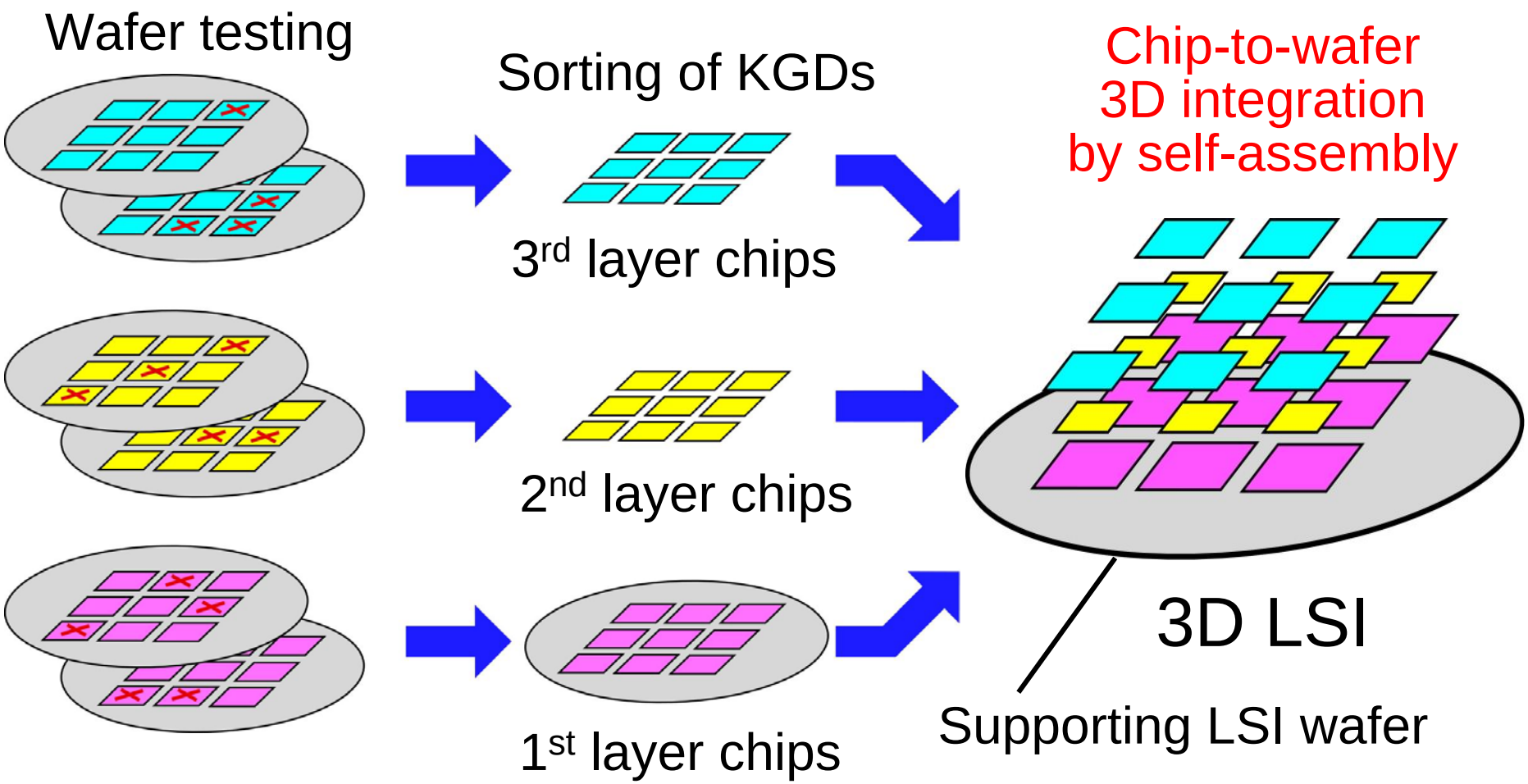
Comparing 3D Integration Technologies

Stacking methods	Wafer-to-wafer	Chip-to-wafer	Chip-to-chip
Production yield	Low	High (use of KGDs)	High
Production throughput	High	High or Low (limited by alignment/bonding)	Low
Applications	DRAM (High-yield memory)	Heterogeneous system (processor/memories, LSI and MEMS)	Packaging

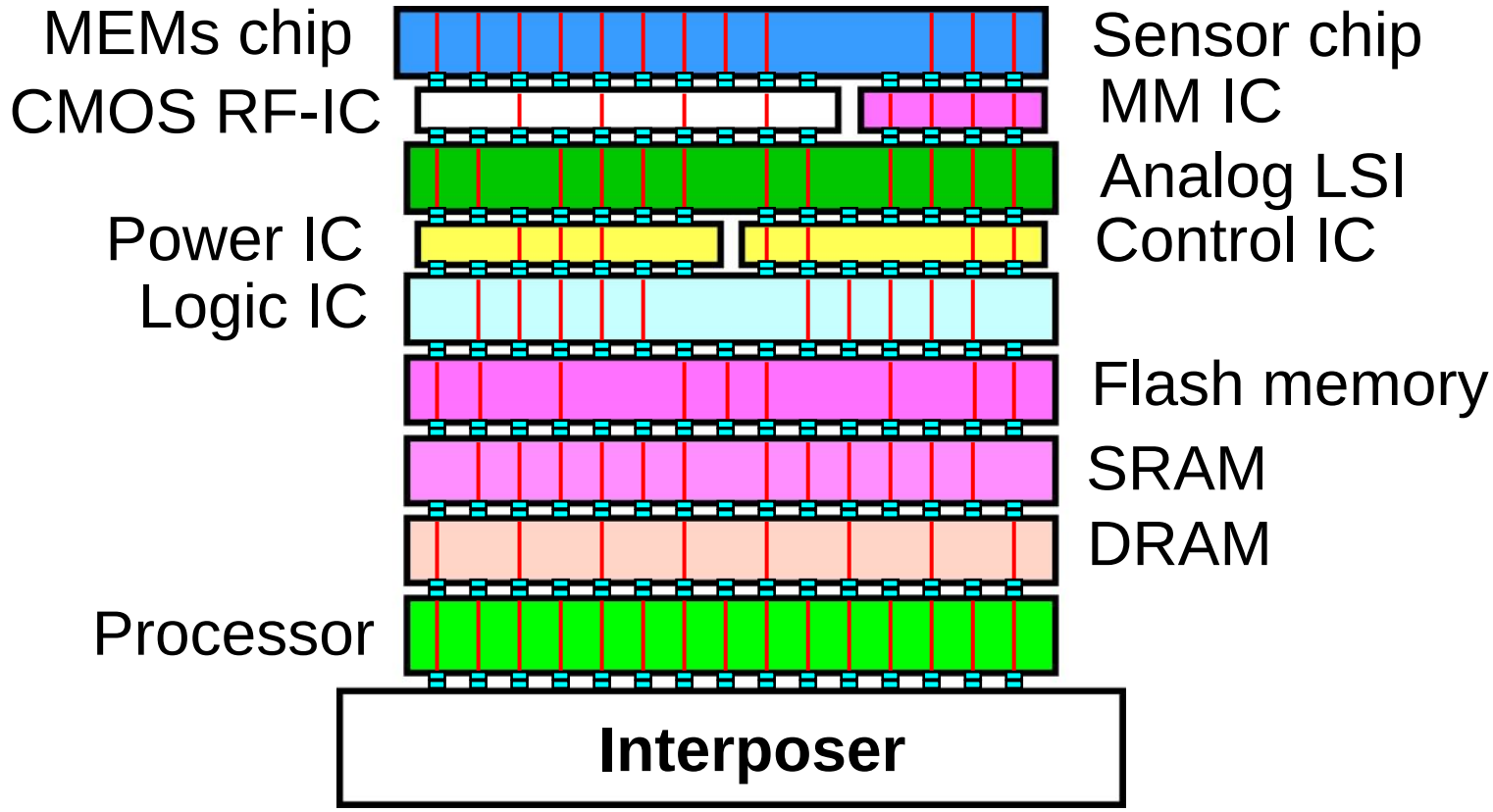
3D Technology Based on Chip-to-Wafer Bonding in Tohoku University : Super-Chip Integration

Batch alignment

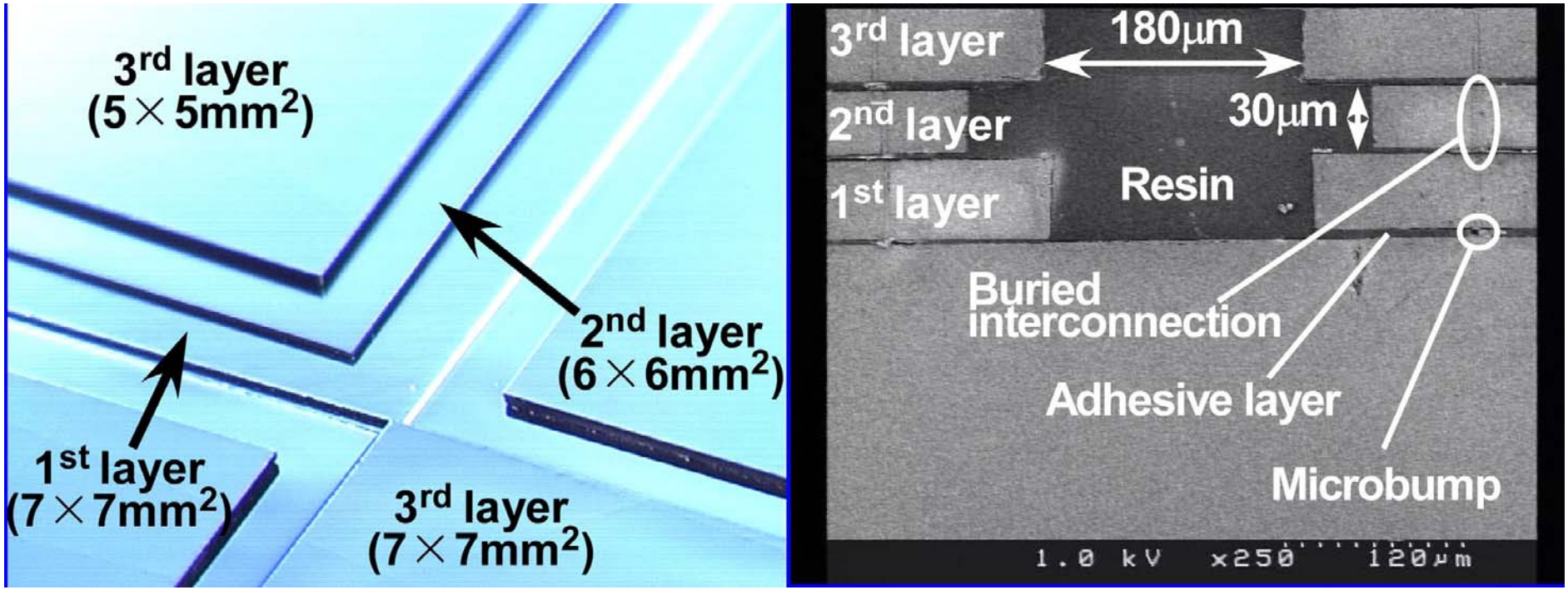
Chip Self-Assembly



Configuration of Super-Chip



Photomicrograph and SEM of 3-Layer Stacked Chips with Different Chip Size Fabricated Using Self-Assembly Method



Outline

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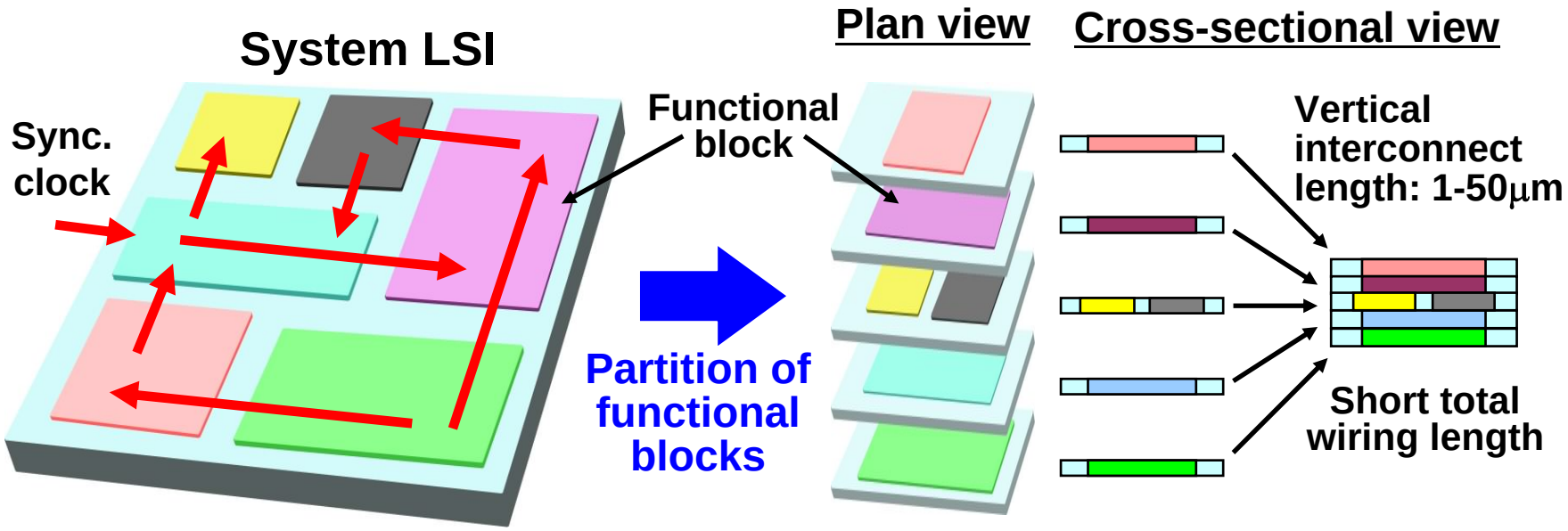
3. **Thermal Characteristics Evaluation of 3D LSI by Simulation and Experiments**
4. Summary

Big Concerns in 3D LSI



Conventional 2D LSI

Large footprint

↓

Large heat sink area

↓

Effective heat removal

3D LSI

Small footprint

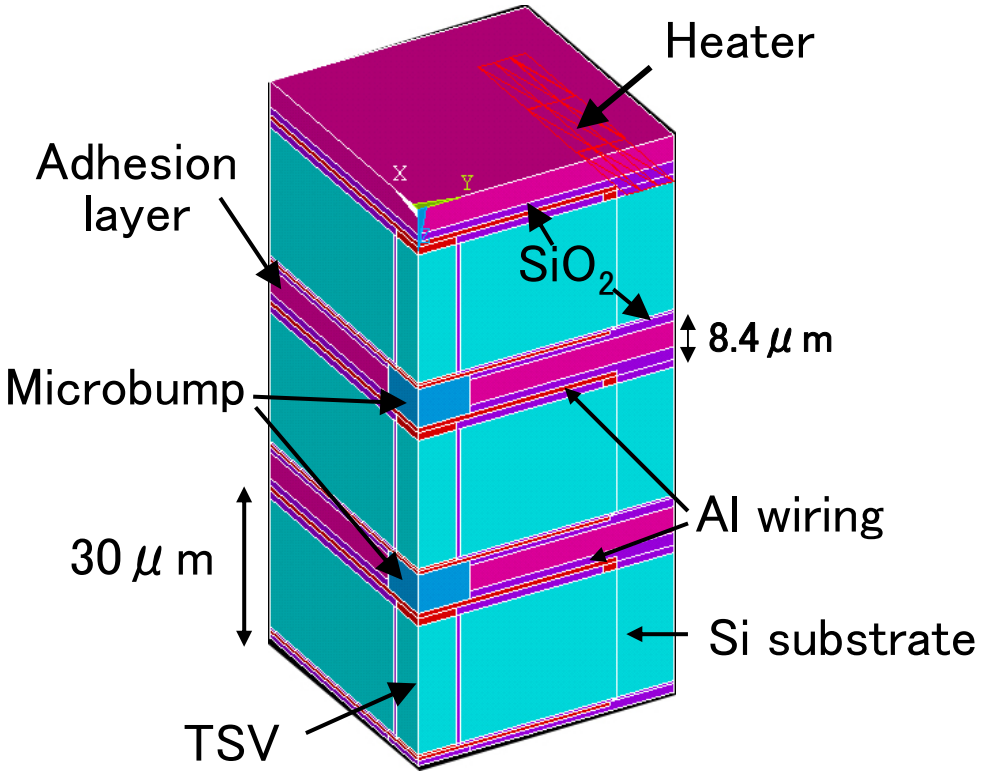
↓

Small heat sink area

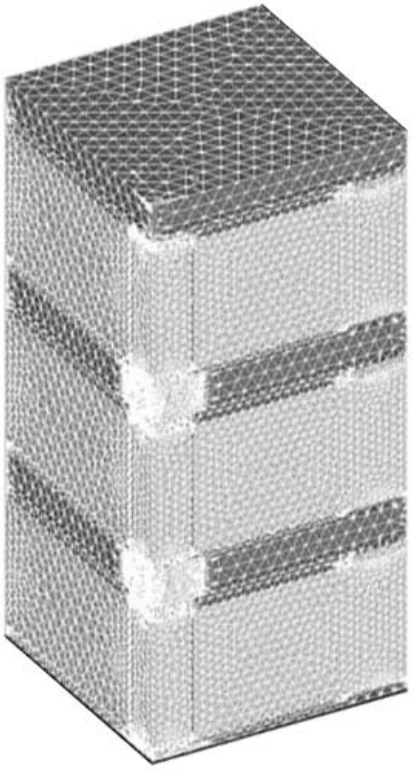
↓

Heat accumulation

3D Mesh Structure for Thermal Simulation Based on FEM Method

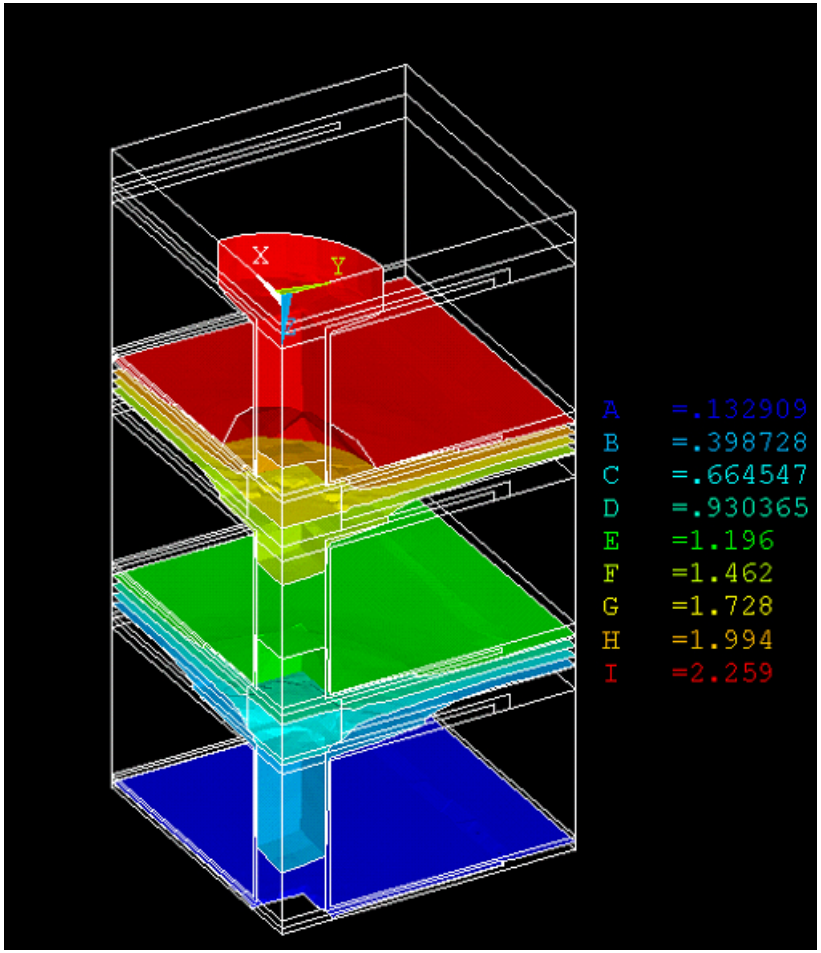


(a) Physical 3D structure

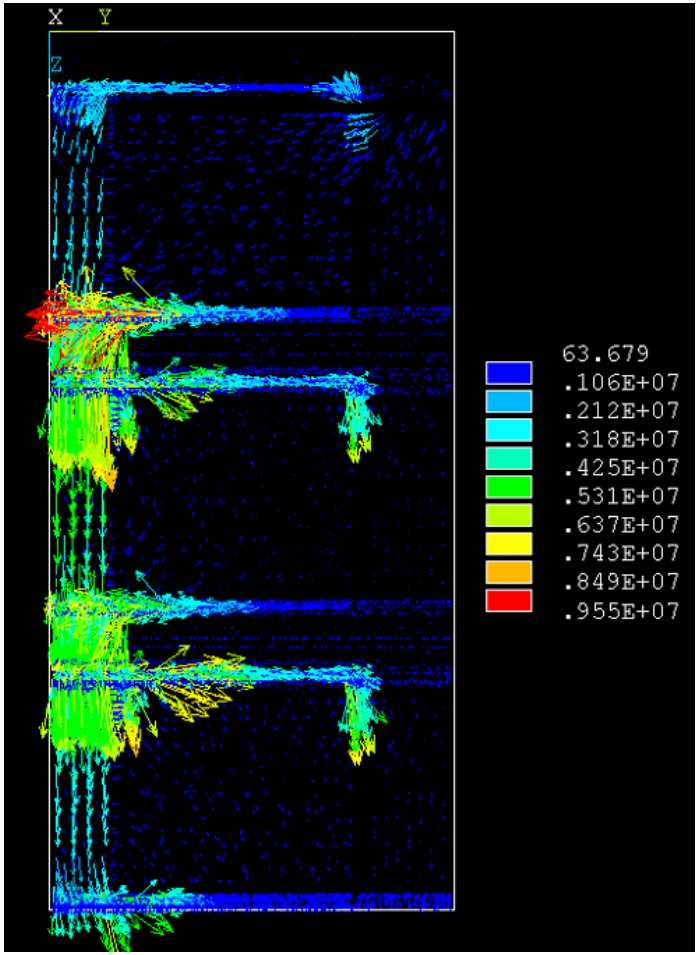


(b) Mesh structure

Simulation Results I of Isothermal Plane and Heat Flux

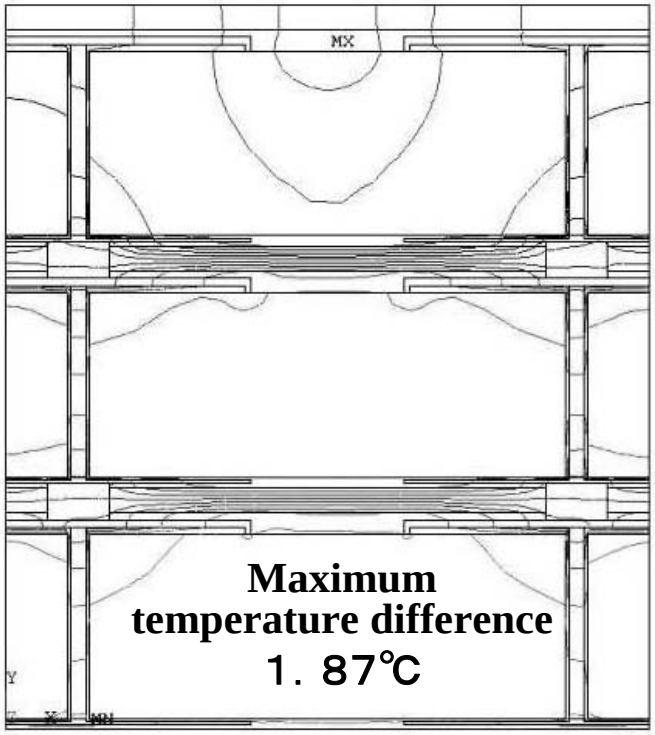


Isothermal plane (℃)

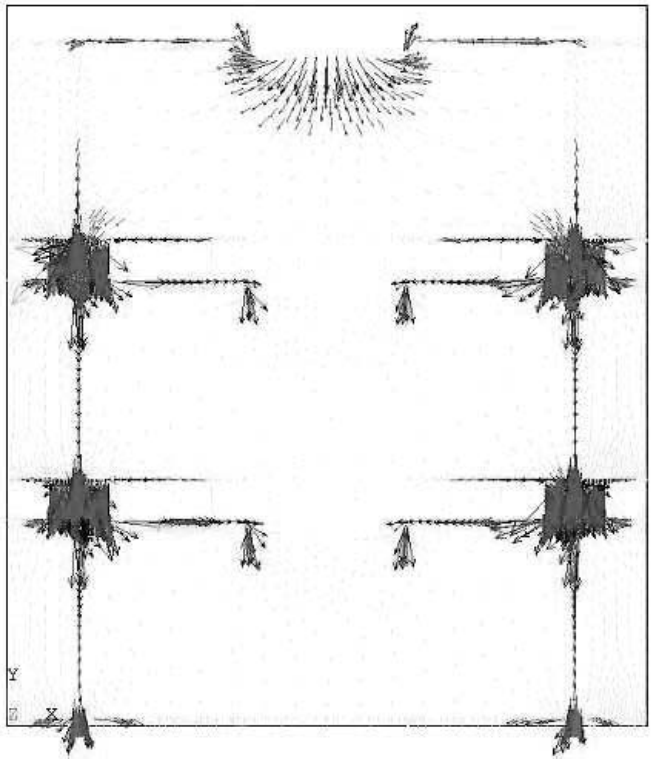


Heat flux (W/m²)

Simulation Results II of Isothermal Line and Heat Flux



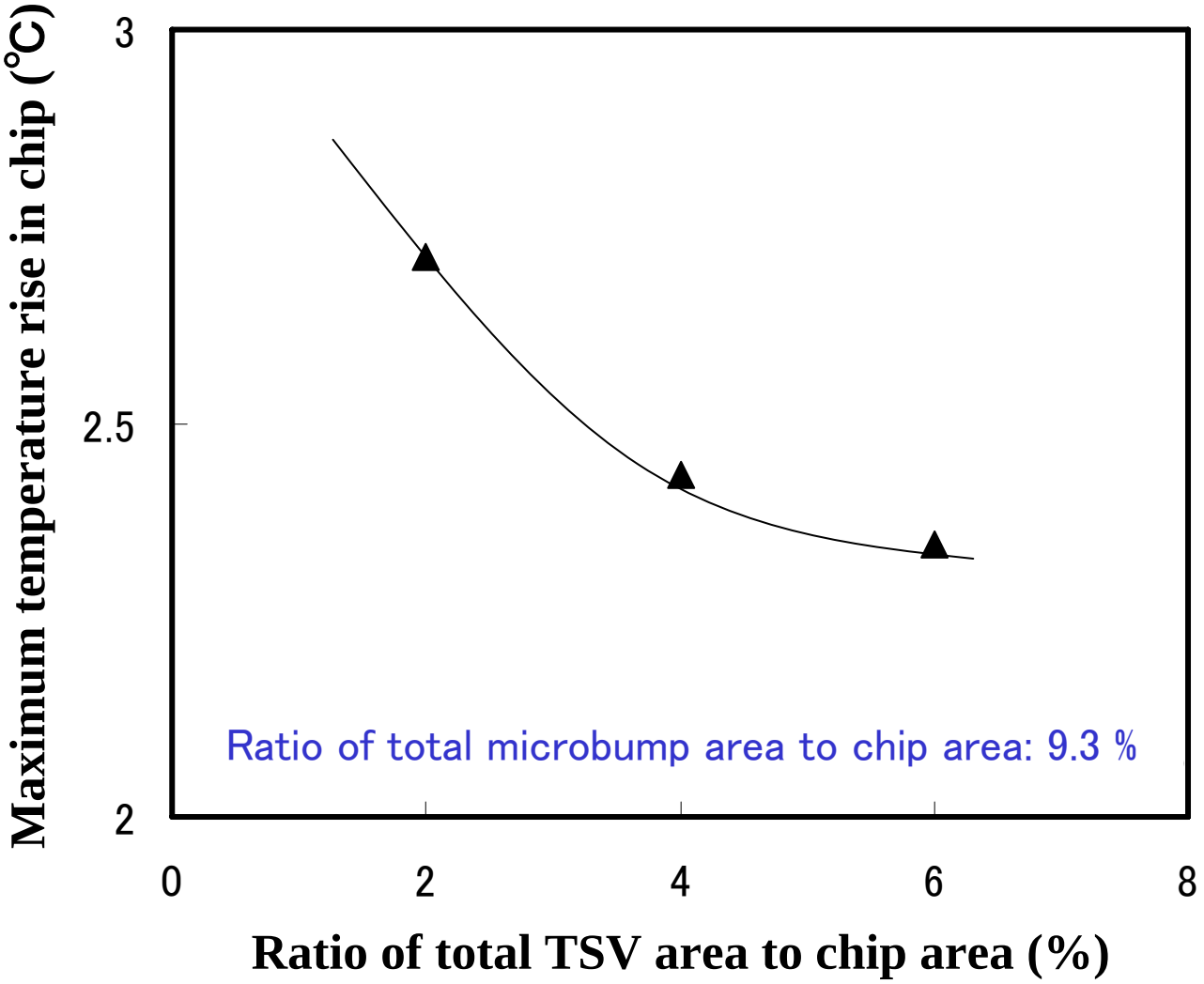
(a) Contour map of isothermal lines



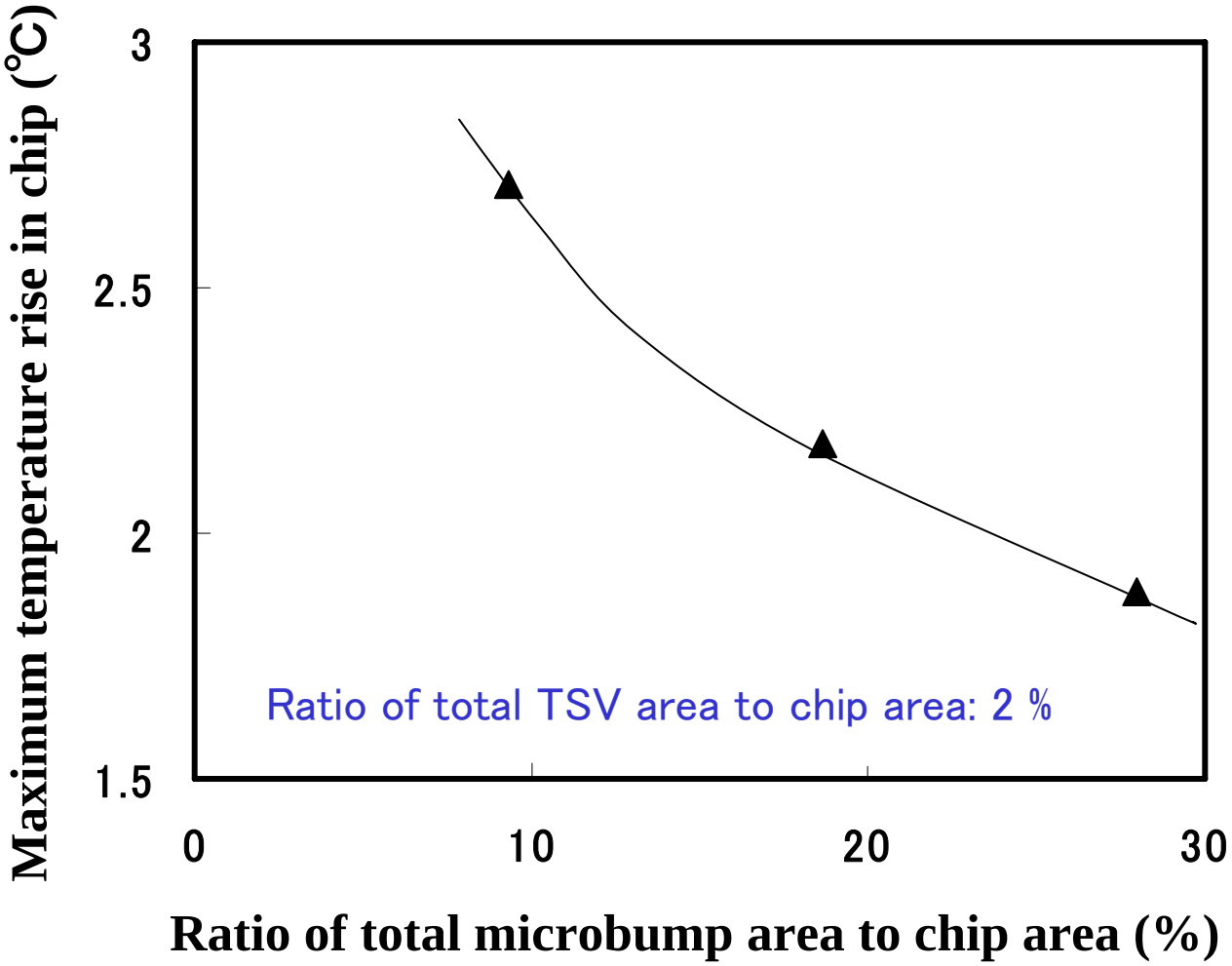
(b) Heat flow distribution

Distance between heat source and buried interconnection: 31.9 μm
Micro-bump size : 10 μm × 10 μm
Diameter of buried interconnection: 2.5 μm
Si thickness : 30 μm

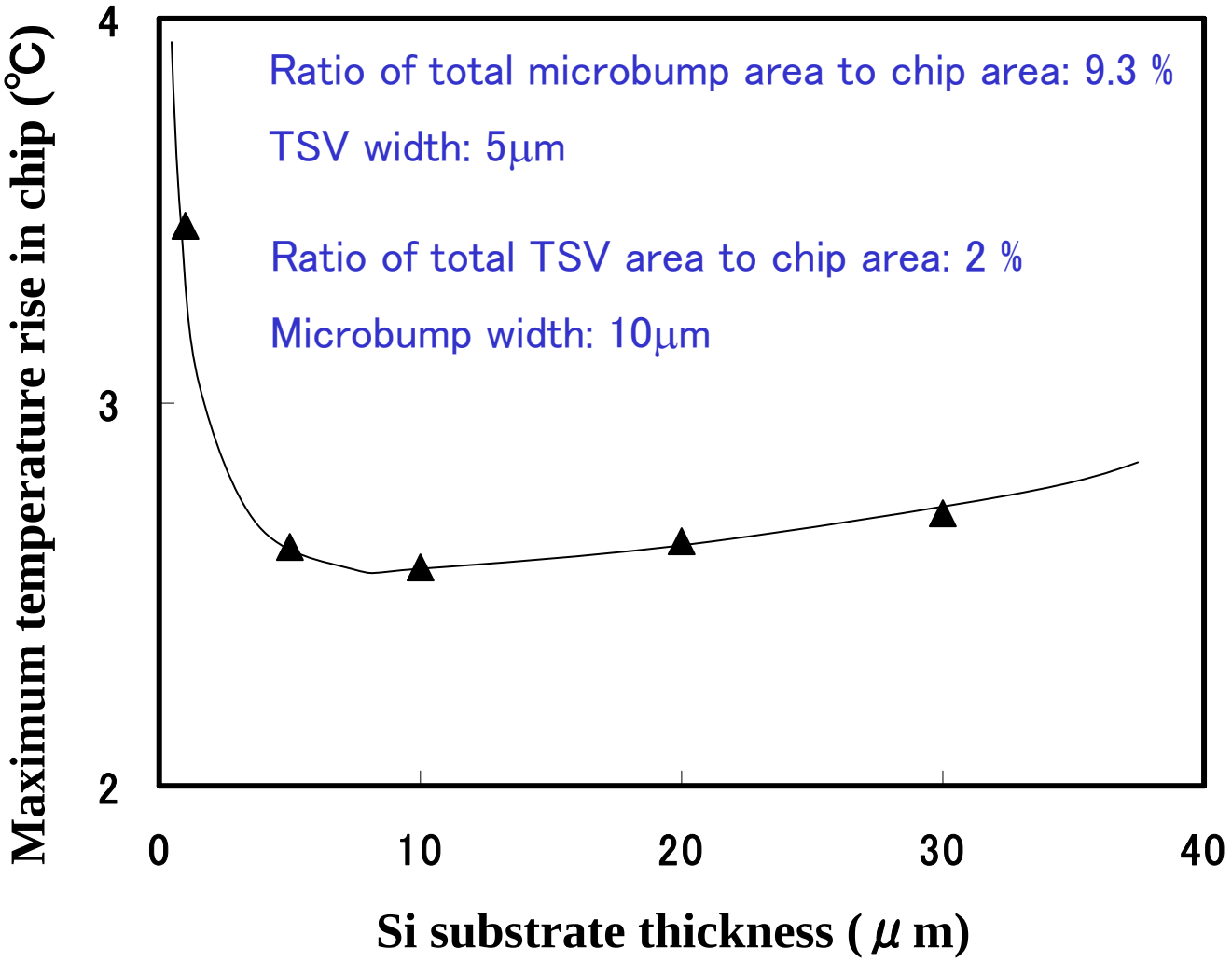
Maximum Temperature Rise in Chip as a Function of Ratio of Total TSV Area to Chip Area



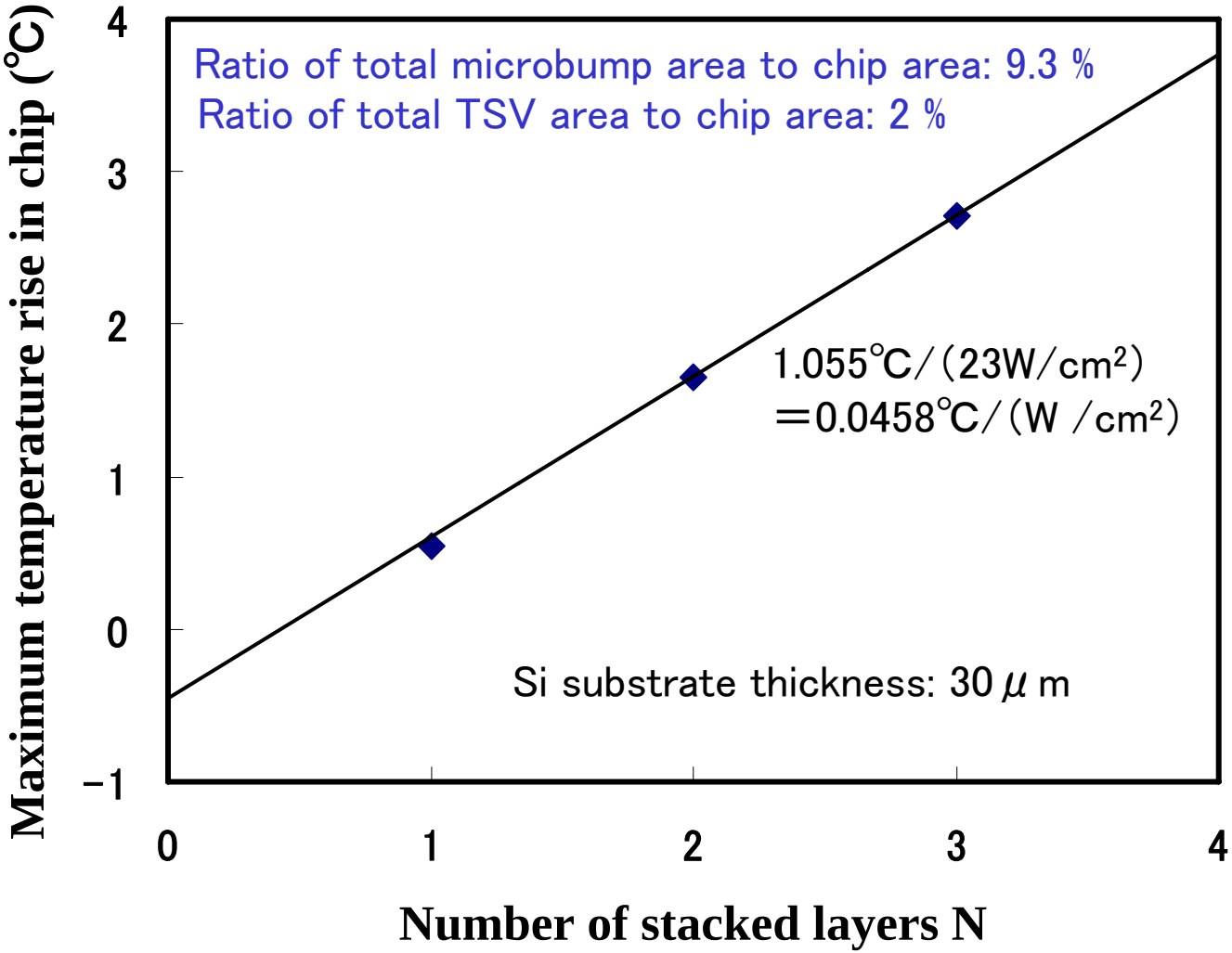
Maximum Temperature Rise in Chip as a Function of Ratio of Total Microbump Area to Chip Area



Maximum Temperature Rise in Chip as a Function of Si Substrate Thickness

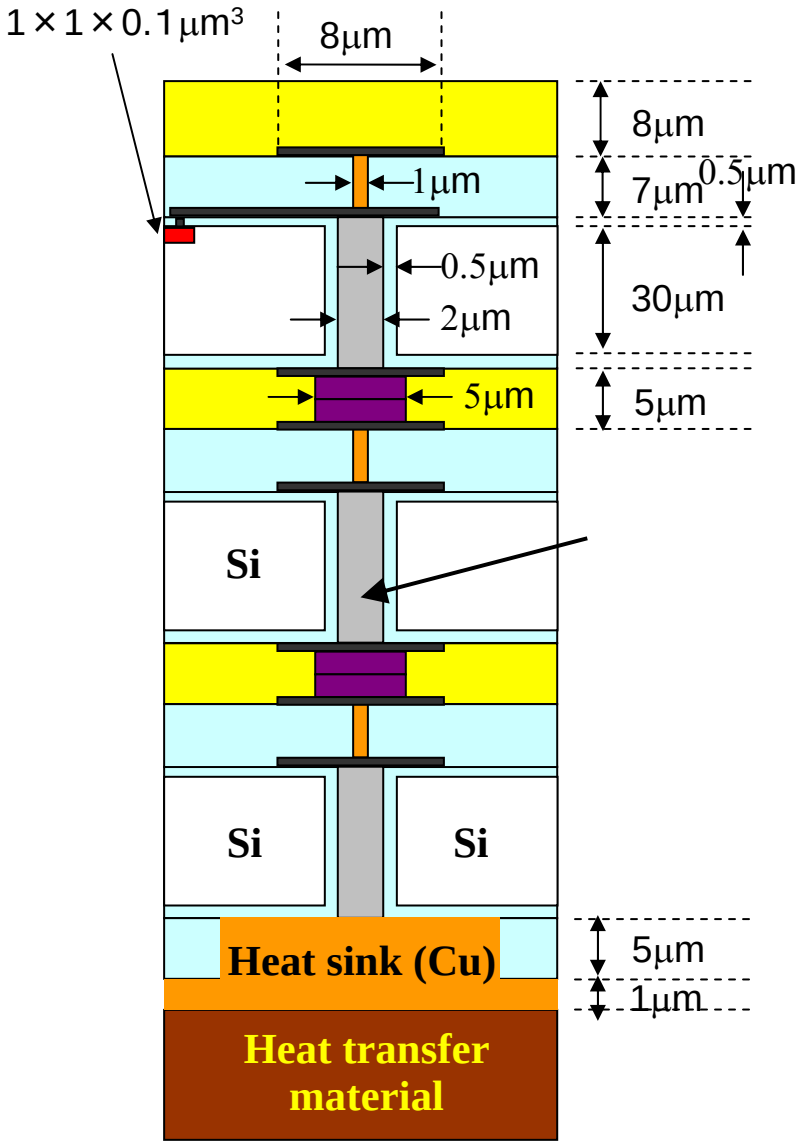


Maximum Temperature Rise in Chip as a Function of Number of Stacked Layers



Simulation Results III: Sizes of 3D Structure Used in Thermal Simulation

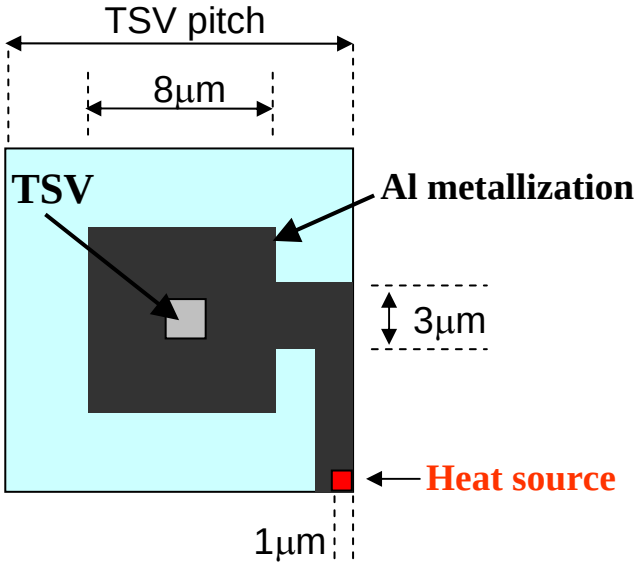
Heat source size:



Cross-sectional view

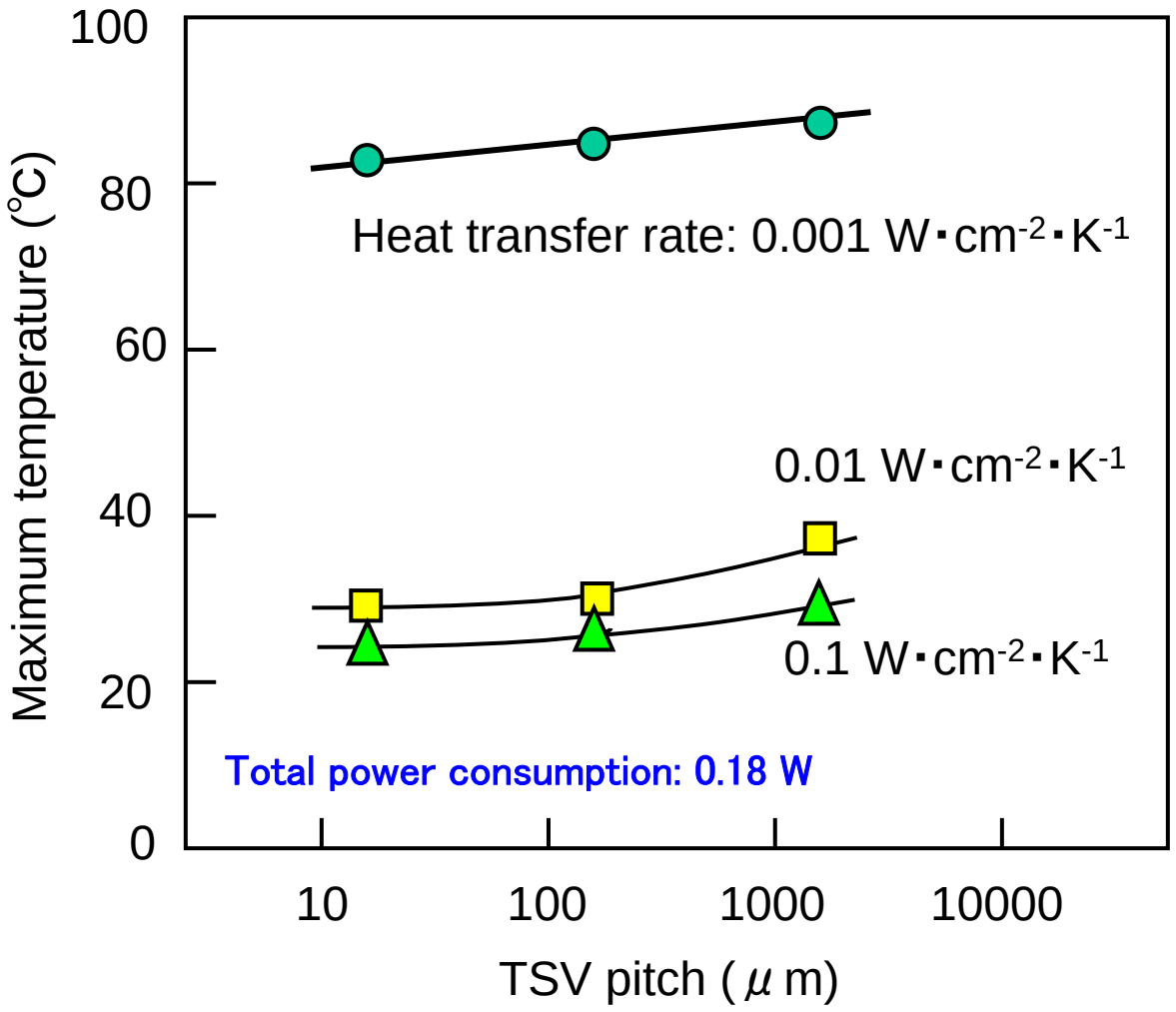
Simulation Parameters

- TSV pitch: 15 μm, 150 μm, 1500 μm
- TSV diameter: 1 μm, 2 μm, 10 μm,, 50 μm
- Si thickness: 10 μm, 30 μm
- Insulator thickness: 0.5 μm., 1 μm
- Bonding materials: adhesive, Cu, SiO_2
- Heat transfer rate: 0.001、0.01、0.1 $W \cdot cm^{-2} \cdot K^{-1}$
- Number of Si layers: 3, 5, 10
- Total chip power: 0.18W, 1.8W, 18W
- Chip size: 9mm × 9mm
- Ambient temperature: 23℃

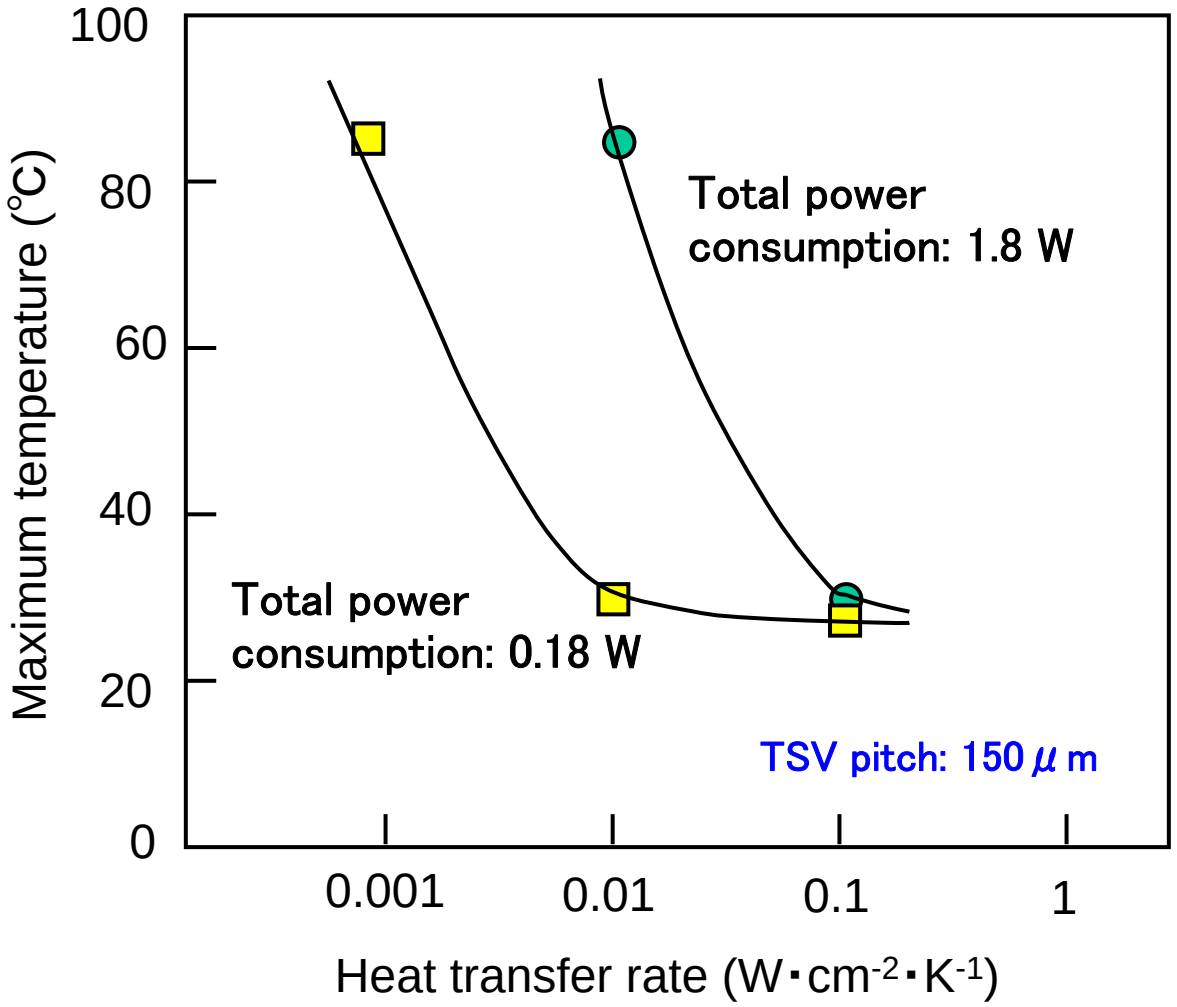


Planar view

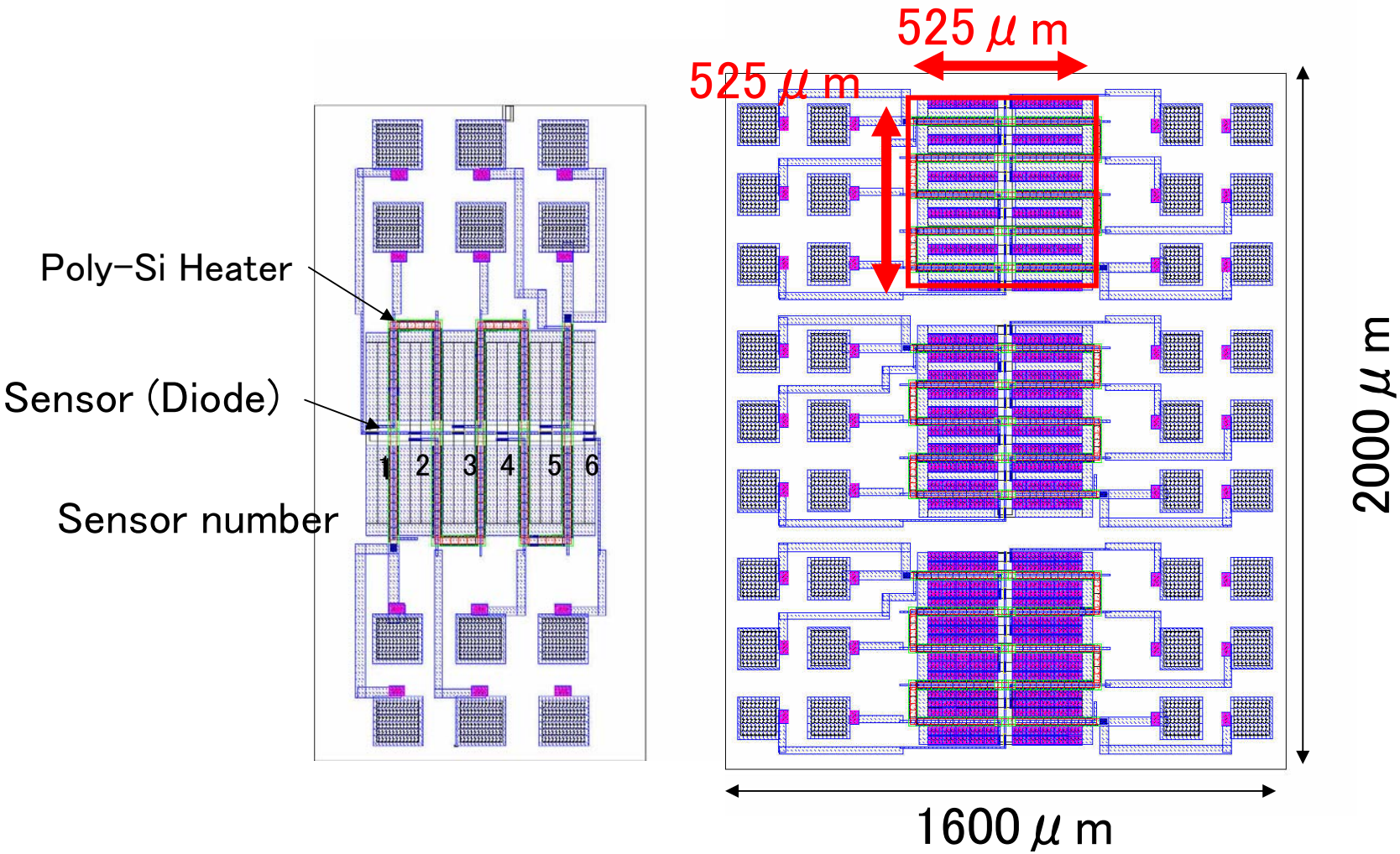
Maximum Temperature of 3D Stacked Chip as a Function of TSV Pitch



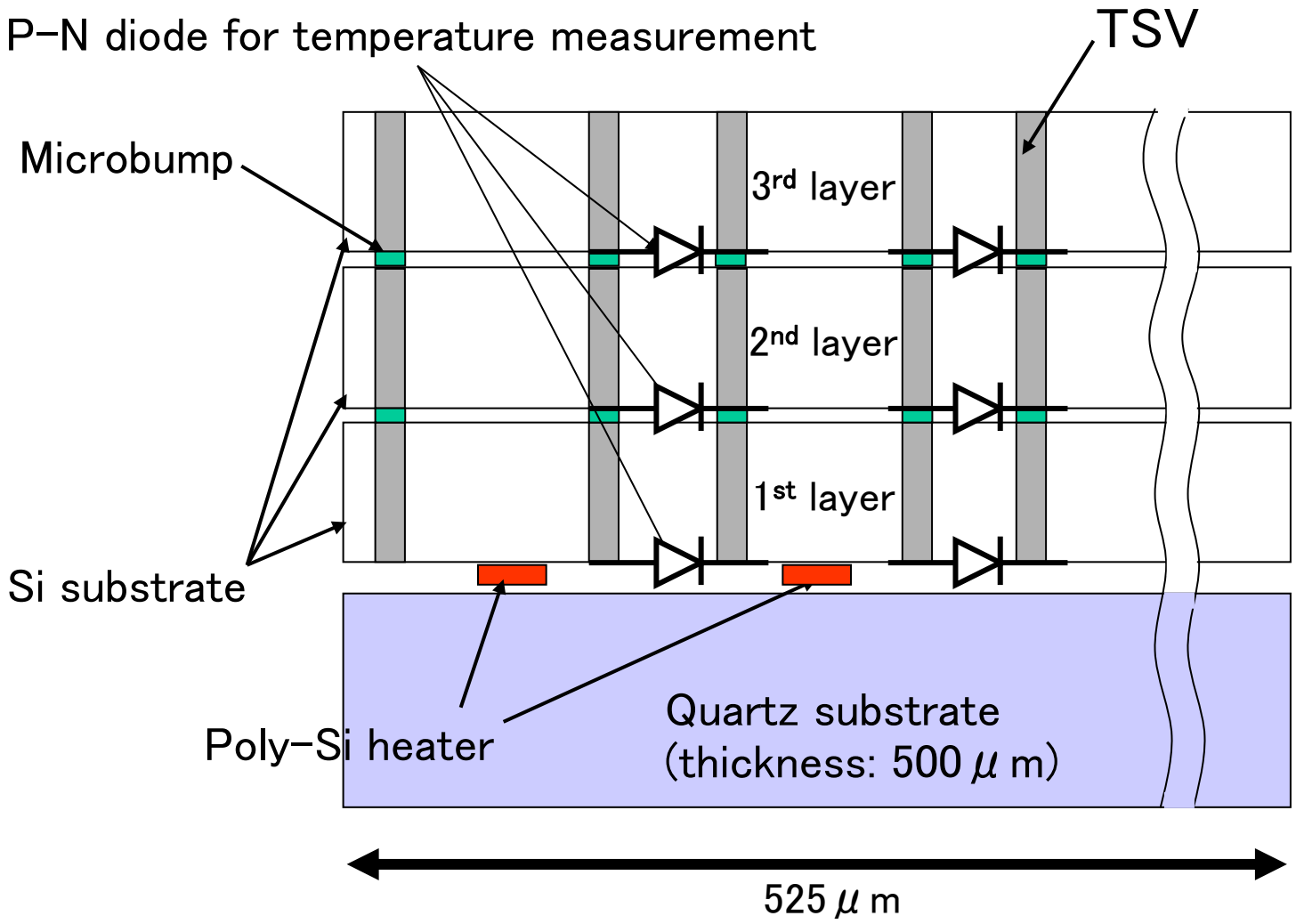
Maximum Temperature of 3D Stacked Chip as a Function of Heat Transfer Rate



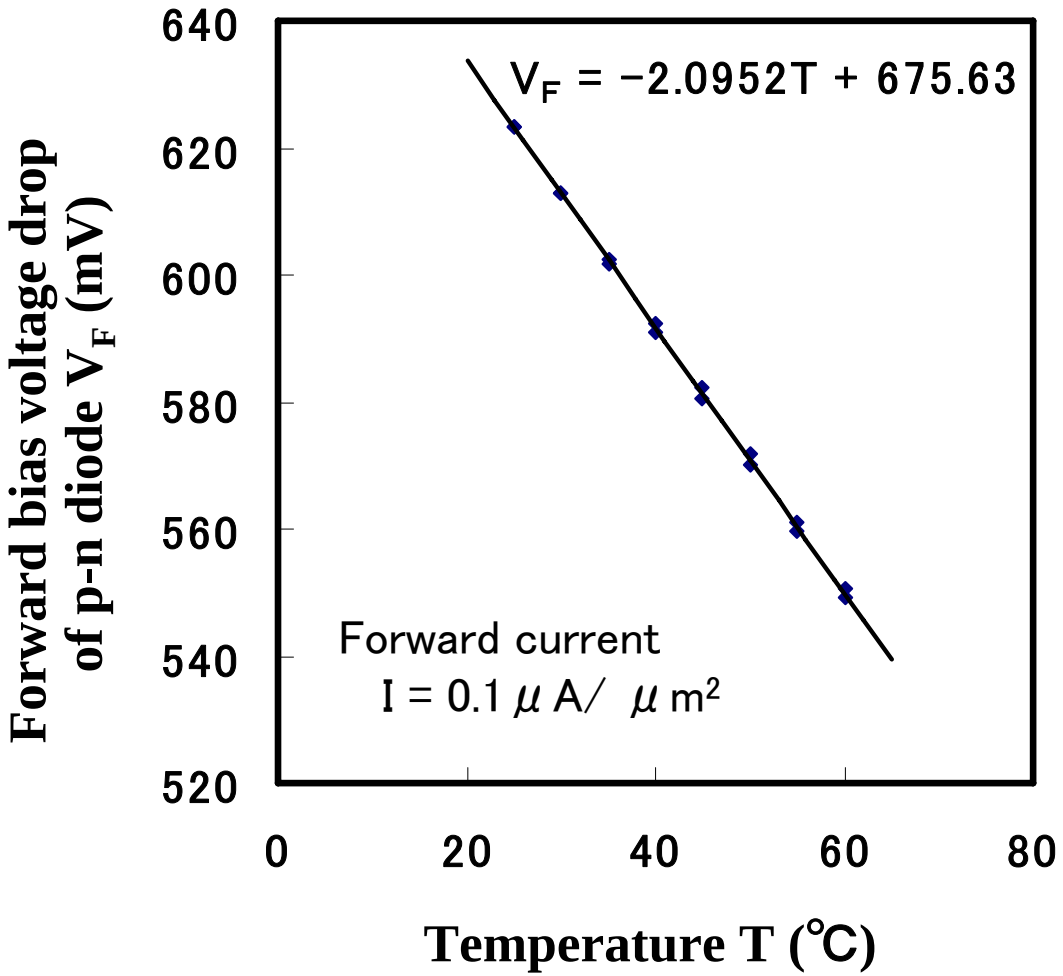
Layout Pattern of Test Devices for Heat Generation Measurement



Cross-Sectional View of Test Devices for Heat Generation Measurement



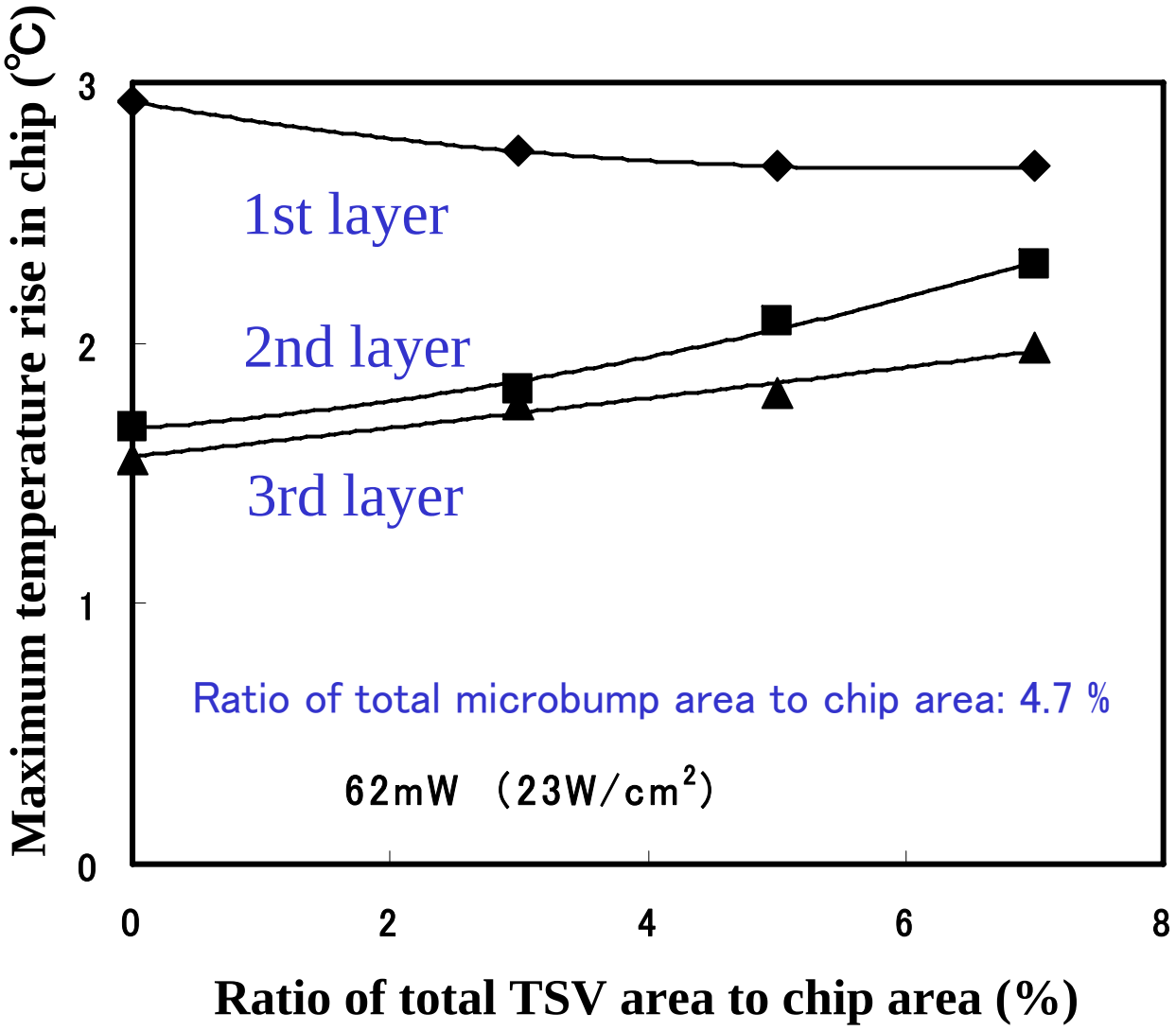
Temperature Dependence of Forward Bias Voltage Drop of P-N Diode for Heat Generation Measurement



$$I = I_0 (e^{qV_F / kT} - 1)$$

$$T = V_F \frac{q}{k} / \ln \frac{I + I_0}{I_0}$$

Temperature Rise in Each Layer as a Function of Ratio of Total TSV Area to Chip Area



Summary

1. We explained about 3D integration technology in Tohoku University
2. We evaluated thermal characteristics of 3D LSI by simulation and experiments.
   We confirmed,
   1) The maximum temperature rise in chip can be suppressed by increasing the ratio of total TSV area and microbump area to a chip area.
   2) Too thin Si substrate results in the increase of the maximum temperature rise.
   3) The maximum temperature of 3D chip can be lowered by reducing TSV pitch.
   4) Heat transfer rate should be increased to decrease the maximum temperature of 3D chip.