SDRAM portmap

signal	bit	mapped to
dq[16]	0..15	P16B:0..15
a[13]	0	P1G
	1..12	P32A:31..20*
ba[2]	0	P1C
	1	P1D
clk		P1A
cke		P1B
dqm[2]	0	P1E
	1	P1F
cs		4D:0
we		4D:1
ras		4D:2
cas		4D:3

* Address bits are bitreversed
  This way we replace shift-left by 20 (needs a register) by a bit-reverse