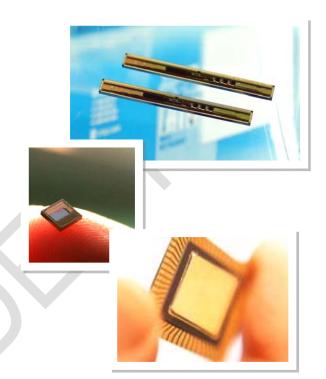
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RM67160 Data Sheet

Single Chip Driver with 16.7M color for 480RGBx480 OLED driver

Revision : 0.2

Date : Jan 30, 2015



Revision History

Version No.	Date	Description	Page	Modified By	Checked By
0.0	2014/12/15	First Release		CL Hou	
0.1	2014/12/26	Modify Pad Diagram: BUMP dimension & coordinate	136	CL Hou	
0.2	2015/01/23	Update CMD list & description Update alignment mark coordinate	39 133	CL Hou	
	2015/01/30	Update Deep standby mode notice. Update power on sequence to add Tini>1ms.	94 131	CL Hou	



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1. General Description

The RM67160 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 480RGBx480, 400RGBx400, 360RGBx480, 320RGBx320, 320RGBx480, 272RGBx480, 240RGBx240, 240RGBx320, 180RGBx360, 180RGBx540, 128RGBx432with internal GRAM. It includes a 5,529,600 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The RM67160 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The RM67160 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 480-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for wearable device applications, including I-watch and smart band.

2. Features

- Single chip AMOLED controller/driver with display RAM
- Display resolution option
 - 480RGB x 480 with 480x24-bits x 480 GRAM
 - 400RGB x 400 with 400x24-bits x 400 GRAM
 - > 360RGB x 480 with 360x24-bits x 480 GRAM
 - 320RGB x 320 with 320x24-bits x 320 GRAM
 - 320RGB x 480 with 320x24-bits x 480 GRAM
 - > 272RGB x 480 with 272x24-bits x 480 GRAM
 - 240RGB x 240 with 240x24-bits x 240 GRAM
 - > 240RGB x 320 with 240x24-bits x 320 GRAM
 - > 180RGB x 360 with 180x24-bits x 360 GRAM
 - > 180RGB x 540 with 180x24-bits x 540 GRAM
 - > 128RGB x 432 with 128x24-bits x 432 GRAM
- Display data RAM (frame memory): 480 x480 x 24-bits = 5,529,600 bits
- Display mode (Color mode)
 - > Full color mode: 16.7M-colors
 - ldle mode: 16.7M-colors, 4096-colors, 8-colors

■ Interface

- 8-bits 80-series MPU interface
- Serial peripheral interface (SPI)
- Dual serial peripheral interface (Dual-SPI)
- MIPI Display Serial Interface (1 clock and 2 data lane pairs)
 - ◆ Support 1lane/2lane (1lane: 500Mbps)
 - Maximum total bit rate is 500Mbps of 2 data lanes 24-bit data format/ 360Mbps of 2 data lanes 18-bit data format/ 320Mbps of 2 data lanes 16-bit data format

Abundant color display and drawing functions

- Programmable y-correction function for 16.7 million color display
- Individual gamma correction setting for RGB dots
- Partial display function
- Sunlight readable
- Control power IC by one-wire interface
- On chip
 - VREFP5/VREFN5 voltage generator for panel voltage
 - VGHR/VGLR voltage for gate control signal
 - Internal oscillator for display clock
 - Source output MUX 1-6 with 240ch source output pins
 - Supports gate control signals to gate driver in the panel
- Built-in OTP function to adjust panel setting
- Logic / interface power supply voltage VDDI = 1.65V ~ 1.8V
- Analog power supply voltage VDD = 2.7V ~ 3.6V



Output voltage levels

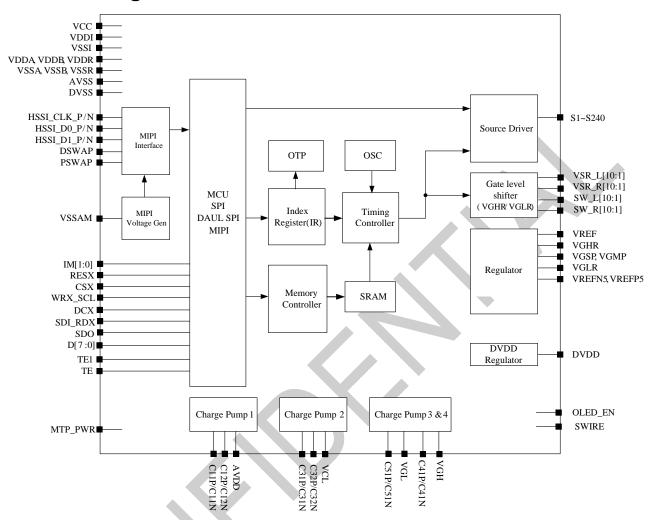
- Positive gate driver voltage range for VGHR: 3 ~ 10V
- ➤ Negative gate driver voltage range for VGLR: -2V ~ -9V
- VREFP5 panel voltage range : 0~5V
- ➤ VREFN5 panel voltage range : -0.5~-5V
- ➤ Step-up 1,2 output voltage range for AVDD: 4.5 ~ 6.5V, VCL: -3.5 ~ -5.0V
- Gamma high/low voltage range for VGMP: 2.0V ~ 6.0V (Max<=AVDD-0.5v) , VGSP: 0V, 0.3V ~ 4.5V</p>
- Package: COF/COG
- Chip size evaluation: 8300um x 2360um(including scribe line)



■ Power Supply Specifications

No.	Item		Description
1	Source Driver		240 pins (480 x RGB)
2	gate control timing Le	vel shift	VGHR-VGLR
5	Input Voltage	VDDI	1.65 ~ 1.8V
		VCC	Connect to VDDI or VDD(VCI)
		VDD (VDDA/VDDB/VDDR)	2.70 ~ 3.60V
6	OLED drive voltages	AVDD	4.5V ~ 6.5V
		VGHR	3V ~ 10V
		VGLR	-2V ~ -9V
		VREFP5	0V ~ 5V
		VREFN5	-0.5V ~ -5V
7	Internal step-up circuits	AVDD	VCI x2.0(dual), x3.0(single)
	- Sil Gallo	VCL	VCI x -1.0(dual), x-2.0(single)
		VGH	VCI x2, x3, x4
		VGL	VCI x-2, x-3, x-4

3. Block Diagram



Interface

The RM67160 supports MIPI DSI interface. MIPI DSI can access both internal command and display data.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the y correction register. The RM67160 displays 16.7M colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to OLED panel, VGH, VGL.

Timing Generating

The timing controller generates timing signals for internal circuits such as the display timing.

Oscillator

The RM67160 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The OLED display driver circuit consists of 240 source drivers (S1~S240). The gate signal consists of VSR_R/L[1:10], SW_R/L[1:10] and outputs either VGHR or VGLR level.



4. Pin Description

4.1 Power Supply Pins

4.1 Power Supp	лу Еш	
Signal	I/O	Function
		Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	Р	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	Р	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDDI	Р	Power supply for interface system except MIPI interface
VCC	Р	Power supply for DVDD regulator
VSSB	Р	System ground for DC/DC converter
VSSA	Р	System ground for analog system
VSSR	Р	System ground for regulator system
VSSAM	Р	System ground for internal MIPI analog system
VSSI	Р	System ground for interface system except MIPI interface
DVSS	Р	System ground for internal digital system
AVSS	Р	System ground for source OP system.
MTP_PWR	Р	MTP programming power supply pin (7.5V typical) Must be left open or connected to DVSS in normal condition.



4.2 Interface Pins

Signal	I/O	Function
CSX	ı	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. If not used, please connect to VSSI.
WRX_SCL	I	WRX : Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. If not used, please connect to VSSI.
D/CX	I	Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter If not used, please connect to VSSI.
SDI: Serial input signal in SPI I/F. The data is input on the rising edge		SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. RDX: Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface.
SDO	0	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. If not used, please open this pin.
D[7:0]	I/O	8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F. These pins are not used for SPI, MIPI, please leave it Open.



4.3 MIPI Interface Pins

Signal	I/O	Function											
HSSI_CLK_P HSSI_CLK_N	I		-These pins are DSI-CLK+/- differential clock signals if MIPI interface is usedIf not used, please connect these pins to VSSAM.										
HSSI_D0_P HSSI_D0_N	I/O		-These pins are DSI-D0+/- differential data signals if MIPI interface is usedIf not used, please connect these pins to VSSAM.										
HSSI_D1_P HSSI_D1_N	I/O		-These pins are DSI-D1+/- differential data signals if MIPI interface is usedIf not used, please connect these pins to VSSAM.										
	1	Pin Name	ect HSSI_D(D/D1 data lan	e sequence HSSI_CLK_ P	and polarity i	n high speed	HSSI_D1_N					
		I	DSWAP=0 PSWAP=0	DSI D0+	DSI D0-	DSI CLK+	DSI CLK-	DSI D1+	DSI D1-				
DSWAP PSWAP			I	I	I	I	DSWAP=0 PSWAP=1	DSI D0-	DSI D0+	DSI CLK-	DSI CLK+	DSI D1-	DSI D1+
					DSWAP=1 PSWAP=0	DSI D1+	DSI D1-	DSI CLK+	DSI CLK-	DSI D0+	DSI D0-		
		DSWAP=1 PSWAP=1	DSI D1-	DSI D1+	DSI CLK+	DSI CLK-	DSI D0-	DSI D0+					

NOTE: "1" = VDDI level, "0" = VSSI level.



4.4 Interface Logic Pins

Signal	1/0	Function				
RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.				
IM[1:0]	I	Interface type selection. The connections of IM[1:0] which not shown in table are invalid. IM[1:0]				
BSTM	ı	Boost mode selection pin. BSTM Mode 2 PWR(VDDI, VCI) 0 AVDD> internal CP VCL> internal CP				
		1 Reserved				
TE	0	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.				
TE1	0	If not used, please open this pin.				
SWIRE	0	Swire protocol setting pin of Power IC, If not used, please open this pin.				
OLED_EN	0	Power IC enable control pin, If not used, please open this pin.				

NOTE: "1" = VDDI level, "0" = VSSI level.



4.5 Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S1 ~ S240	0	Pixel electrode driving output.
SDMY	0	Dummy Source, leave it Open.
VSR_L[10:1] VSR_R[10:1]	0	VSR control signals, Level shift output, (VGHR-VGLR)
SW_L[10:1] SW_R[10:1]	0	VSR control signals, Level shift output, (VGHR-VGLR)



4.6 DC/DC Convert Pins

Signal	I/O	Function
AVDD	0	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
VCL	0	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	0	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGL	0	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C11P, C11N C12P, C12N	0	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	Ю	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	0	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	0	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitor as requirement.
VGHR	0	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	0	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	0	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	0	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VREF	0	Regulator output for internal reference voltage. Connect capacitor for stabilization.
DVDD	0	Regulator output for logic system power. Connect a capacitor for stabilization.
VREFP5	0	Regulator output for VREFP(0~5V)
VREFN5	0	Regulator output for VREFP(-0.5~-5V)



4.7 Test Pins

Signal	I/O	Function	
ANALOG_TEST 1~2	0	Test pin, not accessible to user. Must be left open.	
TEST1~3	Ю	Test pin, not accessible to user. Must be left open.	
TESTEN	I	Test pin, not accessible to user. Must be left open., Internal pull low	
EXTCLK		Test pin, not accessible to user. Must be left open.	
DUMMY	I	Dummy PAD, leave it open	

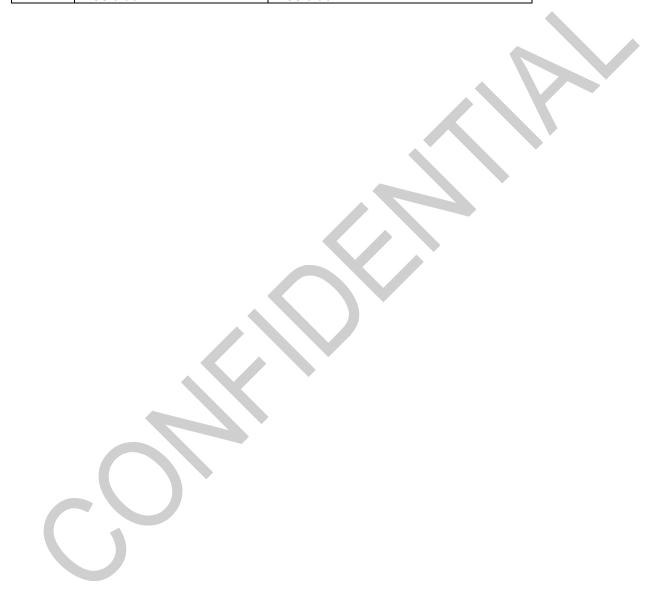


5. Function Description

5.1 Interface Type Selection

Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / 16-SPI	MIPI / 16-SPI
11	MCU 8-bit	MCU 8-bit





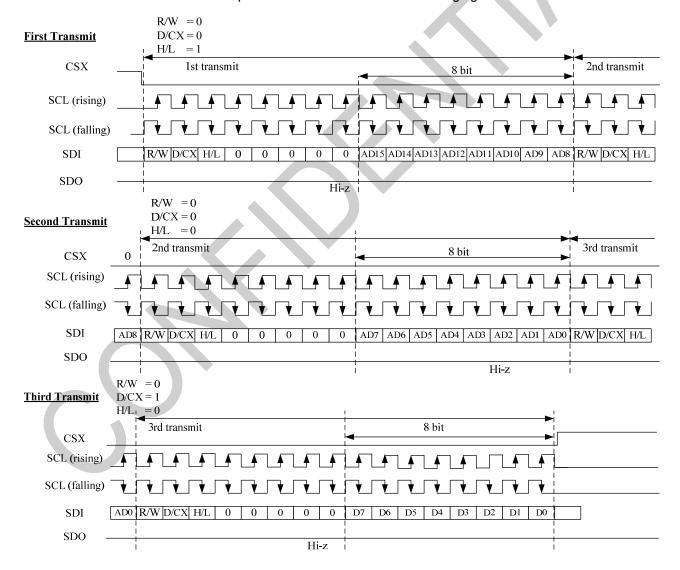
5.2 Serial Interface

5.2.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The SPI interface utilizes CSX, SCL and SDI and SDO signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight write cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface write command sequences are described in the following figure.



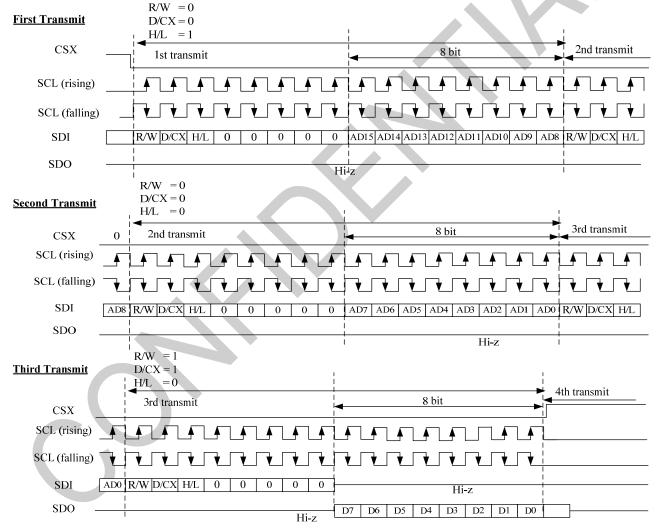


5.2.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The SPI interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight read cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface read command sequences are described in the following figure.

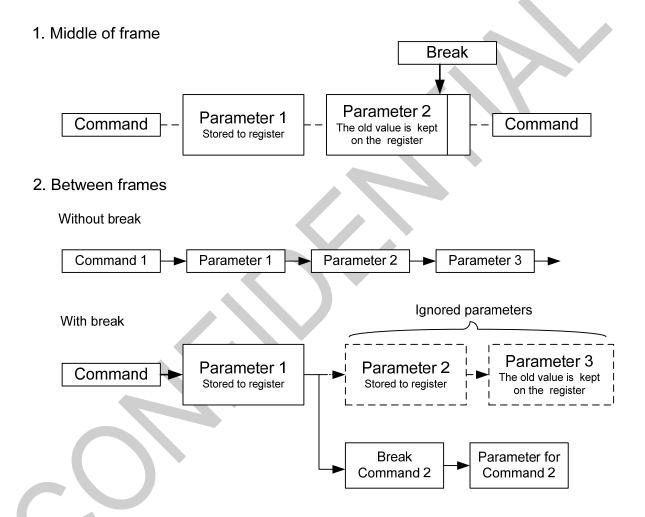




5.2.3 Break and Pause Sequence

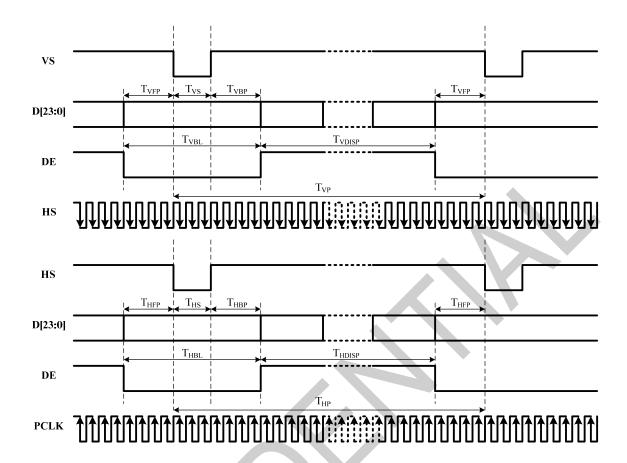
The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.



Break can be e.g. another command or noise pulse.







5.3 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

RM67160 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller.

The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

RM67160 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

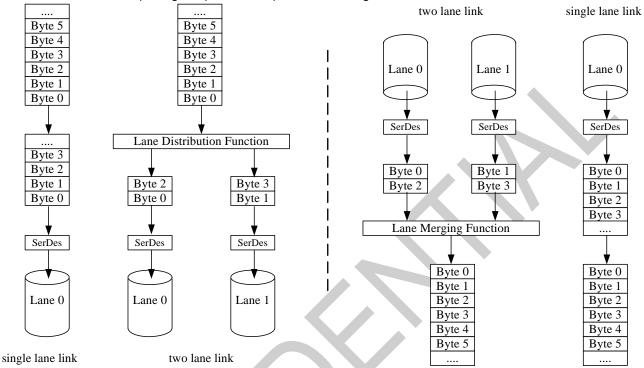
RM67160 Configuration:

A.O						
Lane Pair	MCU(Master) RM67160(Slave)					
Clock Lane	Unidirectional Lane					
	Clock only					
Data Lane 0	Bi-directional Lane					
	Forward High-speed					
	Bi-directional Escape Mode					
	Bi-directional LPDT					
Data Lane 1	Unidirectional Lane					
	Forward High-Speed					
	Escape Mode					
	No LPDT					



5.3.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.



There are two kinds of packets, short packet and long packet.

Short packet structure:

LP-11: low power mode SoT: start of transmission DI: data identification Data 0, Data1: packet data ECC: error correction code

EoT: End of Transmission

Packet Header

Packet Data

Packet Data

Data 0 Data 1 ECC EoT LP-11

Time



DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

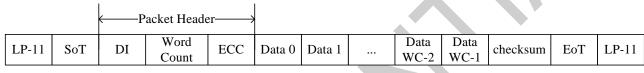
Long packet structure: LP-11: low power mode SoT: start of transmission DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission



Time-



5.3.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type		Description	Packet
,,	binary	•	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6	Long
		Format	
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long



Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall syntem reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM67160 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

DCS commands

DCS short write command

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

DCS read commands

The commands are used to request data from s display module.

DCS Long Write / write_LUT command

The commands are used to send larger blocks of data to a display module.

Maximum return packet size

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Null Packet

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

Blanking Packet

A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

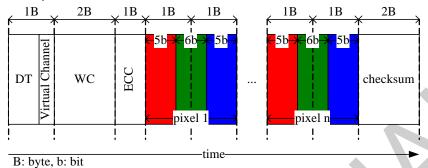
Generic Long Write

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.



Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

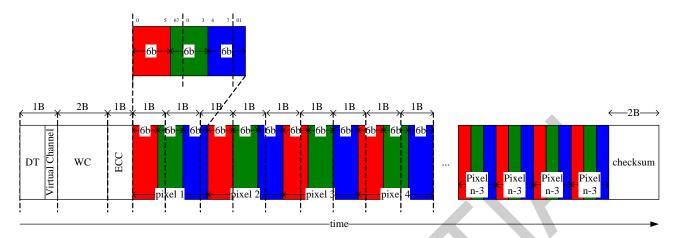
The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.





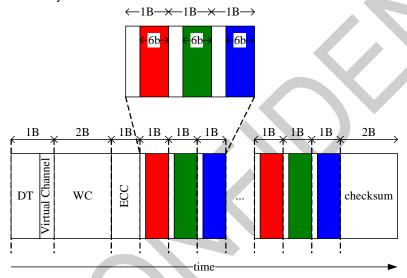
Packet pixel stream, 18-bit format, Data Type: 01 1110

The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.



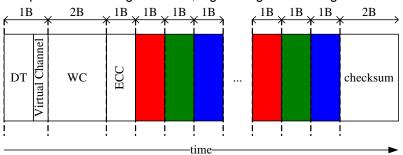
Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.





Packet pixel stream, 24-bit format, Data Type: 11 1110
The pixel format is eight bits red, eight bits green and eight bits blue.





5.3.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission.

Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor. Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.

Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.

Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.

Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.

Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.

Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.

Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.

Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.

Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.

Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.



5.3.4 Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved



5.3.5 Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read reponse, 1byte returned	short
12h	01 0010	GEN short read reponse, 2bytes returned	short
1Ah	01 1010	Generic long read reponse	long
1Ch	01 1100	DCS long read reponse	long
21h	10 0001	DCS short read reponse, 1byte returned	short
22h	10 0010	DCS short read reponse, 2bytes returned	short

Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

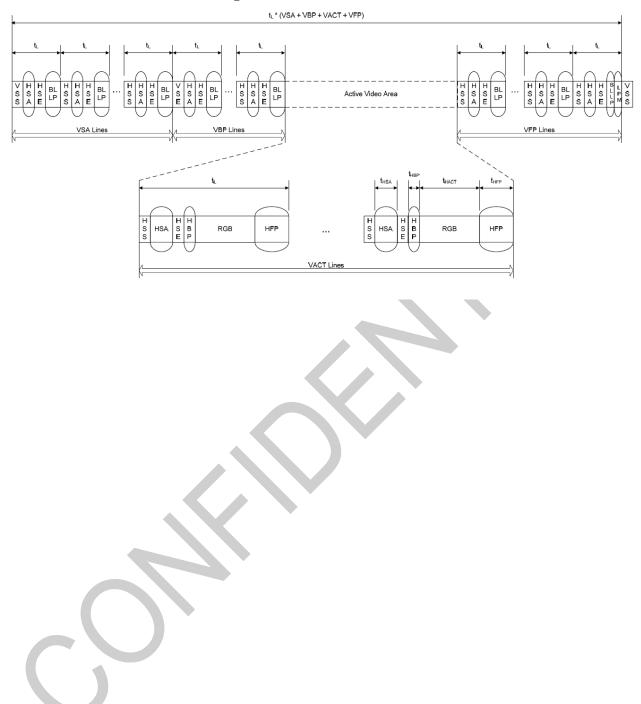
Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.



5.3.6 DSI Video Mode Interface Timing





5.3.7 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

The parity bits of ECC are defined as below:

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

ECC Parity Generation Rules:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B



5.3.8 Notice

- 1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
- 2. We recommend users to adopt EoTp to enhance overall robustness of the system during HSDT.



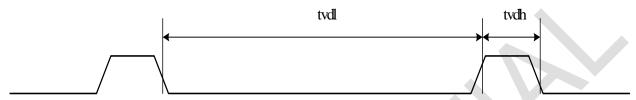


5.4 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

5.4.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:



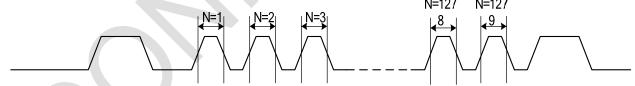
tvdh = The LCD display is not updated from the frame memory. tvdl = The LCD display is updated from the frame memory.

Mode 2, the tearing effect output signal consist of V-sync and H-sync information:



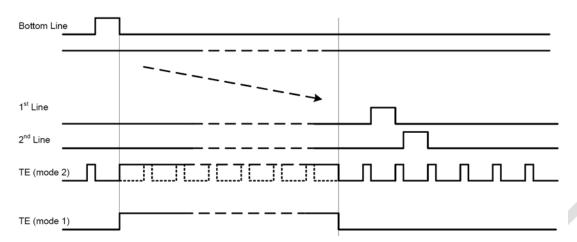
thdh = The LCD display is not updated from the frame memory. thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.



N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



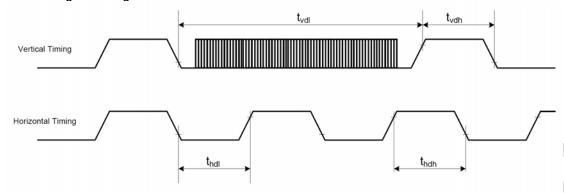


Note. During Sleep In mode, the tearing effect output signal is active low.



5.4.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

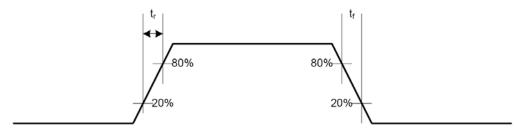


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical timing low duration	TBD		ms	
tvdh	Vertical timing high duration	TBD		us	
thdl	Horizontal timing low duration	TBD		us	
thdh	Horizontal timing high duration	TBD		us	

Notes:

- 1. The timings apply when MADCTL B4=0 and B4=1
- 2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

TEON (35h)	TELOM (35h, 1 st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)



6. Command

6.1 Command List

0.1	C	///////	Iaii	LIST	1	1	1	1	1	1						
Co Page	mmar		W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	МТР		
CMD1	00h	- ara.	w	NOP				No Arc	jument				-	-		
CMD1	01h		w	Software reset					jument				-	-		
CMD1	04h	1st											00h	-		
CMD1	04h	2nd	R	Read display identification					[7:0]				80h	-		
CMD1	04h	3rd		information					[7:0]				00h	-		
CMD1	05h		R	Read number of the errors					7:0]				00h	Α.		
CMD1	0Ah	1st	R	on DSI Read display power mode	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON			08h			
CMD1	0Bh	1st	R		MY	MX	MV	ML	RGB	DISPON	RSMX	RSMY	00h			
CMD1	0Ch	1st	R	Read display MADCTR	-	1	1	1	RGB	IFPF2	IFPF1	IFPF0	77h			
CMD1	0Dh	1st		Read display pixel format	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h			
CMD1	0Eh	1st	R R	Read display image mode	TEON	M	0	0	0	0	0	ERR	00h	-		
				Read display signal mode Read display self-diagnostic								checksum	00h	-		
CMD1	0Fh	1st	R	result	0	0 0 0 0 0 0 comp										
CMD1	10h	•	W	Sleep-in		No Argument										
CMD1	11h	-	w	Sleep-out		No Argument										
CMD1	12h	-	w	Partial display mode on		No Argument										
CMD1	13h	•	W	Normal display mode on		No Argument										
CMD1	20h	•	w	Display inversion off		No Argument										
CMD1	21h	•	w	Display inversion on		No Argument										
CMD1	22h	-	w	All pixel off		No Argument										
CMD1	23h	-	w	All pixel on	No Argument											
CMD1	28h	-	w	Display off				No Arg	jument				-	-		
CMD1	29h	-	w	Display on	,			No Arg	jument				-	-		
CMD1		1st	w					sc	9:8]				00h	-		
CMD1	2Ah	2nd	w	Set column start address					7:0]				00h	-		
CMD1		3rd	w				<u> </u>	EC	9:8]				01h	-		
CMD1		4th	w					EC	7:0]				8Fh	-		
CMD1		1st	w					SP[9:8]				00h	-		
CMD1	2Bh	2nd	w	Set row start address				SP[7:0]				00h	-		
CMD1		3rd	W					EP[9:8]				01h	-		
CMD1		4th	w					EP[7:0]				8Fh	-		
CMD1	2Ch	•	W	Memory write				No Arg	jument				-	-		
CMD1	2Eh	•	W	Memory read				No Arg	jument				-	-		
CMD1		1st	W					SR	9:8]				00h	-		
CMD1	30h	2nd	W	Partial area				SR	7:0]				00h	-		
CMD1		3rd	W						9:8]				01h	-		
CMD1		4th	W						7:0]				8Fh	-		
CMD1		1st	W						[9:8]				00h	-		
CMD1	31h	2nd	W	Vertical partial area					[7:0]				00h	-		
CMD1		3rd	W						[9:8]				01h	-		
CMD1		4th	W						[7:0]				8Fh	-		
CMD1		-	W	Tearing effect line off	No Argument											
CMD1	35h	•	W	Tearing effect line on	0	0	0	0	0	0	0	TELOM	00h	-		
CMD1	36h	٠	W	Scan direction control					TR[7:0]				00h	-		
CMD1	38h	٠	W	Idle mode off					jument				-	-		
CMD1	39h	٠	w	Enter idle mode			1		jument	1	1	1	-	-		
CMD1	3Ah	-	W	Interface Pixel Format	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77h	-		
CMD1	3Ch	-	W	Memory Continuous Write	· ·											
CMD1	3Eh	-	W	Memory Continuous Read					jument				-	-		
CMD1	44h	1st	W	Set tear scan-line				STS	15:8]				00h	-		



ı	1 1	i	i	Ī	Г							1			
CMD1		2nd	W					STS	[7:0]				00h		
CMD1	45h	1st	R	Get scan line				GTS	15:8]				00h	-	
CMD1		2nd	R	001 00411 11110				GTS	[7:0]				00h	-	
CMD1	4Fh	-	w	Deep standby	0	0	0	0	0	0	0	DSTB	00h	-	
CMD1	51h	-	W	Write display brightness				DBV	[7:0]				FFh	-	
CMD1	52h	•	R	Read display brightness				DBV	[7:0]				FFh	-	
CMD1	53h	•	W	Write CTRL display	0	0	BCTRL	0	DD	0	0	0	28h	-	
CMD1	54h	١	R	Read CTRL display	0	0	BCTRL	0	DD	0	0	0	28h	-	
CMD1	58h		W	Set color enhancement	0	0	0	0	0	SLR_EN		SLR_LEVE L0	00h	-	
CMD1	59h	•	R	Read color enhancement	0	0	0	0	0	SLR_EN	SLR_LEVE L1	L0	00h	-	
CMD1	5Ah		w	Set color enhancement1	SLR_AMBI _IN7	SLR_AMBI _IN6	SLR_AMBI _IN5	SLR_AMBI _IN4-	SLR_AMBI _IN3	SLR_AMBI _IN2	SLR_AMBI _IN1	SLR_AMBI _IN0	00h		
CMD1	5Bh		R	Read color enhancement1	SLR_AMBI _IN7	SLR_AMBI _IN6	SLR_AMBI _IN5	SLR_AMBI _IN4-	SLR_AMBI _IN3	SLR_AMBI _IN2	SLR_AMBI _IN1	SLR_AMBI _IN0	00h	<u>.</u>	
CMD1		1st	R			SID[7:0]									
CMD1		2nd	R			SID[15:8]									
CMD1	A1h	3rd	R	Read DDB				MID	[7:0]				80h	-	
CMD1		4th	R					MID[15:8]				90h	-	
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-	
CMD1		1st	R				•	SID	7:0]				D0h	-	
CMD1		2nd	R					SID[15:8]				01h	-	
CMD1	A8h	3rd	R	Read DDB Continuous				MID	[7:0]				80h	-	
CMD1		4th	R					MID[15:8]				90h	-	
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-	
CMD1	AAh	-	R	Read first checksum				FCS	[7:0]				00h	-	
CMD1	AFh	-	R	Read continuous checksum				ccs	[7:0]				00h	-	
	C2h			Set_DSI Mode	0 0 0 0 0 0 DM1 DM0								00h	-	
	C4h			Set_DSPI Mode	0	0	DSPI_CFG 1	DSPI_CFG 0	0	0	0	DSPI_EN	00h	-	
CMD1	DAh	-	R	Read display identification				ID1	7:0]				00h	-	
CMD1	DBh		R	information	ID2[7:0]									-	
CMD1	DCh		R	(the same as 04h)	ID3[7:0]										
CMD1	FEh	-	W	Write CMD mode page	0	0	0	0		CMD_P	age[3:0]		00h	-	
CMD1	FFh	-	R	Read CMD page Status	0	0	0	0	_	CMD_St	atus[3:0]		00h	-	



6.2 Command Description NOP (0000h)

0000Н	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Status Power On Sequence N/A SW Reset N/A															
Inst/Para	R/W			D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
NOP							•	•								
Description	Th	is comm	and is an	empty comr				e any	effect o	on the	display	modul	e.			
Restriction	None															
Register Availability		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes														
Default		Power On Sequence N/A														
Flow Chart	None															



SWRESET(0100h): Software Reset

0100H				SW	VRESE	T(Soft	ware R	eset)					
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	W	01h	0100h		1	1	No Ar	gumen	t	l	l	l	
Description	paramete	ers to thei	ir S/W Re	ommand is v set default v	alues.	(See d	efault ta	ables ii	n each				
Poetriotion		comman	d cannot	cannot be se be sent for 1						enters	Sleep	-In mod	de. Do
			atus	de O 1-11- 1	Ma-1- 5) (f C)	an 6	V0 000	ilabilit	:y			
				de On, Idle I				-					
Register Availability				de On, Idle I		-	-		-				
Availability				e On, Idle M				Yes					
			ep In	e On, Idle M	lode O	n, Sie	ep Out	Yes					
		SIE	ep in					res	<u> </u>				
					7								
			St	atus			Default	Value					
			Po	wer On Sec	quence) I	N/A						
Default			SV	V Reset		ı	N/A						
			HV	V Reset		ı	N/A						
Flow Chart		<	Display Set 0 to S	ep In Mode						Pa Se	Legend ommand aramete Display Action Mode equentia ransfer		



RDDID(0400h~0402h): Read Display ID

0400H							RDDI	D						
		Add	ress											
Inst/Para	R/W	MIPI	Other	D15	-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			0400h	х		ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
RDDID	R	04h	0401h	Х		ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80
			0402h	Х		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	The 3 rd pa Note: Co	arameter mmands	(ID1): the (ID2): the (ID3): the RDID1/2/spectively	: Modul 3 (DAh/	e/driv	er ID			espon	d to the	e paran	neter 1	, 2, 3 0	f
Restriction														
		Statu	IS						Availa	ability				
			nal Mode					- 100	Yes					
Register			nal Mode				1000		Yes					
Availability			al Mode (al Mode (•					Yes					
		Sleep		Jii, iuie	, IVIOC	ie OII,	Sieeb	Out	Yes					
		3133												
					D (
		Status				ult Val	ue	Befo	re MT	P				
Default			On Sequ			value		+			h / ID3			
		SW Res				value value					h / ID3 h / ID3			
		nw ke	SEI		IVIII	value		=וטו	0011 / 1	DZ=60	נטו / ווו	=0011		
Flow Chart		ID1[Send 2nd ID2[paramel 7:0] d parame 7:0]	eter							Com Para Dis Ac Mo	gend nmand nmand splay stion ode uentia	>	



RDNUMED(0500h): Read Number of Errors on DSI

0500H						RDNU	MED						
		Add	Iress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	after tl	HEX
RDNUMED	R	05h	0500h	х	D7	D6	D5	D4	D3	D2	D1	D0	00
Description	the bits D[60] D[7] is s D[70] sent the	is below bits are to set to "1" bits are s e first par	elling a nu if there is et to "0"s ameter in	umber of the overflow wit (as well as f formation (=	parity of th D[6 RDDSN The re	errors. 0] bits. //(0Eh) ad fun	's D0 aı ction is	re set '	"0" at th	ne sam	e time) after t	
Restriction	_									V			
		S	status					Δ.	vailabi	lity			
				ode On, Idle	Mode	Off, S	leep O	7000	es	y			
Register		N	Iormal Mo	ode On, Idle	Mode	On, S	leep O	ut Y	es		D2 D1 D0 (ore detailed description essame time) after there ace operation.		
Availability		-		de On, Idle			_		es				
			artial Mo Sleep In	de On, Idle	Mode	On, Si	eep Ou		es es			D0 descript	
			лоор										
			S	tatus	_		Defaul	t Valu	е				
Default			P	ower On Se	quenc	е	00h						
Delault			S	W Reset			00h						
			Н	W Reset			00h						
Flow Chart	RDE	P[7:0]=	paramete					Lege Comn Paran Disp Acti Mod	neter lay on de ential				



RDDPM (0A00h): Read Display Power Mode

RDDPM (0A)	JUh) : R	ead L	JISPI	_									
0A00H					RDD	PM (R	ead D	isplay	Powe	r Mod	e)			
Inst/Para	D/	w	Add	Iress	D15-8	D7	D6	D5	D4	D3	D2	D1	DO	HEV
IIISVF ala	IV	V V	MIPI	Othe		וט	50		D4	D3	D2	וט	D0 08 e table below:	ΠLΛ
RDDPM	F	٦	0Ah	0A00)h x	D7	D6	D5	D4	D3	D2	D1	D0	08
	This	s con	nmand	indica	tes the cur	rent st	atus of	the d	isplay a	as des	cribed	in the	table b	elow:
		Bit			•									
	-	D7	BSTC	ON	Booster Vo	Itage S	tatus	'0' :	=Booste	er off				
	_	D6	IDMO	N	Idle Mode C	n/Off		'0'	= Idle N	lode Of	í 🦚			
Description		D5	PTLC	N	Partial Mod	e On/O	ff	'0'	= Partia	I Mode				
'		D4	SLPC	ON				'0'	= Sleep	In				
		D3	NOR	NC	Display Nor On/Off	mal Mo	ode	'0'	= Partia	l Displa				
		D2			Display On/	Off		'0'						
		D1 D0						0						
														
				Status	S						Availa	bility		
				Norm	al Mode O	n, Idle	e Mode	Off,	Sleep	Out \	Yes			
Register				Norm	al Mode O	n, Idl	e Mode	On, S	Sleep	Out	Yes			
MIPI Other														
			<u> </u>			n, Idle	Mode	On, S	leep C	out '	Yes			
				Sleep	In	V					Yes			
				S	tatus			Def	fault V	alue				
Default				P	ower On S	Seque	nce	180	1					
Sciadit				S	W Reset			08ł	1					
				Н	W Reset			08ł	1					
			Serial I	/F Mo	de	Para	allel I/F	Mode	:		r			,
		ı	RDDP	M (0Ah	1)	RI	ODPM (0Ah)			i 1 1			-
		I			<u> </u>						! ! !	_		
		/	Send	↓ D[7:01		D	↓ ummv F	Read	_	Driver	į			
Flow Chart		_		1								`>=		$\rightarrow \Box$
						/-5	• Send D[7:0]	7		1	\leq	Action	$\geq \cdot $
					4				•		! ! !		Mode	
											1			al ¦
											! ! !		ransfer	
											·-			



RDDMADCTR (0B00h): Read Display MADCTR

0В00Н			ı	RDDMAD	CTR	(Read	Displa	y MAI	DCTR)				
		Addr	ess	Ī.,									
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTR	R	0Bh	0B00h	ı x	D7	D6	D5	D4	D3	D2	D1	D0	00
	This con	nmand in	dicates	the curre	nt sta	tus of t	he dis	play as	descr	ibed ir	the ta	ble be	elow:
	Bit	Symbo	ı	Description	on		Com	ment					
	D7	MY		Row Add Incremen	ress			creasin ecreasi					
	D6	MX		Column A	Address	3	0: In	creasin	g in ho	rizontal			
		MV		Incremen		~ (NA) ()		creasin ow/colun				\/	
Description	D5			Row/Colu			1: No	ormal CD Refre			m	<u> </u>	
	D4	ML		Vertical Re			1: LC	D Refre	sh Botto	om to To			
	D3 D2	RGB Reserv	ed .	RGB/BG	R Orde	r	0	BGR, "()"=RGE	3	·		
	D1	RSMX		Horizonta	al Flip			Norma			D1='0') D1='1')		
	D0	RSMY		Vertical F	lip		,0, =	Norma	l displa	y(36H-l	D0='0')		
							1 =	Flipped	a dispia	y(36H-	DU= 1)		
		St	atus						Av	ailabi	lity		
		No	ormal N	lode On	, Idle I	Mode C	Off, Sle	ер О	ıt Ye	s			
Register		No	ormal N	Mode On	, Idle I	Mode C	On, Sle	ер Оі	ıt Ye	:S			
Availability		Pa	artial M	ode On,	Idle M	ode O	ff, Sle	ep Ou	t Ye	s			
		Pa	artial M	ode On,	Idle M	ode O	n, Sle	ep Ou	t Ye	s			
		SI	eep In						Ye	es .			
		Statu	IS				Def	ault Va	alue			1	
				Sequence			00h		4.40			1	
Default		SW F	Reset				00h	1				1	
			Reset				00h	<u> </u>					
Flow Chart		DMADCTR Send D[7:	(0Bh)		DDMAD Dumn	I/F Mo	_	Ho: Driv		P2	Display Action Mode equentiaransfer		



RDDCOLMOD (0C00h): Read Display Pixel Format

0C00H		,		DDCOLMO			splay	Pixel	Forma	at)			
		Addı								Ī			
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	R	0Ch	0C00h	Х	0	1	1	1	0	IFPF[2]	IFPF[1]	[1] IFPF[0]	77
	This co	ommand	indicates	the curren	t statu	s of th	e disp	lay as	descri	bed in	the ta	ble be	low:
	Bi	t Syml	bol	Description	on		Comr	nent					
	D:			_ DBI Pixe _ Format(C				= 16-bi = 18-bi					
	D			Interface			'111'	= 24-bi	ts / pix	el,			
Description		0 1111	[0]	Format)			others	s are no	o defin	Э		Y	
		;	Status						Av	ailabil	ity		
			Normal N	/lode On, I	dle M	ode O	ff, Sle	ep Ou	t Ye	s			
Register			Normal N	/lode On, I	dle M	ode O	n, Sle	ep Ou	t Ye	s			
Availability				ode On, Id	7000		•	•		s			
				ode On, Id	lle Mo	de On	, Slee	p Out					
		_;	Sleep In						Ye	S			
		St	atus				Defa	ault Va	alue				
Default			_	Sequence			77h					_	
			V Reset	·			77h						
		HV	V Reset				77h						
	Se	erial I/F M	lode	Paral	lel I/F	Mode				[Le	egend	
		COLMOD					1				Со	mmand	
	RDL	COLMOD	(UCII)	RDDCC	OLMOD	(UCII)]	Host		_	Par	ameter	
Flow Chart		Send D[7:	01	D	ımmy Re	and and	-	Driver		<		isplay	
		JCHU D[7.	<u></u>		anniny Kt		-			 	\geq		$\geq \parallel$
				So	end D[7:	0]	7			 		/lode	$egin{array}{c} \parallel \end{array}$
										 		quential	\
										i 	tra	ansfer	<u> </u>



RDDIM (0D00h): Read Display Image Mode

RDDIM (0D0	UII). K	au Di	spiay iii										
0D00H				RDDIM	(Read	Disp	iay Ima	age Mo	ode)				
Inst/Para	R/W	Ad MIPI	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	_				_								
RDDIM	R	0Dh	0D00h	X	D7	D6	D5	D4	D3	D2	D1	D0	00
	The dis	piay mo	dule returr	is the disp	Jiay III	iage ii	ioue si	alus.					
	Bit	Sym		Descri	otion		Comr	nent					
	D7 D6		erved erved				'0'						
December	D5	INVO	N	Inversi	on On	Off	"0" =	nversi nversi	on is C	Off	\rightarrow	V	
Description	D4	ALLO	NC	All Pixe	el On		'1' = V	Normal Vhite c	lisplay				
	D3	ALLO	OFF	All Pixe	el Off			Normal Black d		у			
	D2~ D0	Rese	erved				'000'						
		·											
			Status						Ave	: - -: :4			
			Normal M	ode On. I	dle Mo	ode Of	ff. Slee	p Out	Yes	ilabilit	y		
Register			Normal M					•	Yes				
Availability		ı	Partial Mo	de On, Id	lle Mo	de Off	, Slee	Out	Yes				
		ı	Partial Mo	de On, Ic	lle Mo	de On	, Sleep	Out	Yes				
			Sleep In		\checkmark				Yes				
		St	tatus				Def	ault Va	alue]	
Default		P	ower On S	Sequence)		00h						
Belauit		S	W Reset				00h						
		H	W Reset				00h						
)								ļ	Leg	gend	
	Sei	rial I/F M	lode	Para	llel I/F	Mode	1			Г	Com	mand	7 []
	R	DDIM (0D	h)	RE	DIM (0I	Oh)		II4			Para	meter	
	<u> </u>							Host Driver		<	Dis	splay	$\supset $
Flow Chart		Send D[7:	0]	D	ummy Ro	ead				<	Ac	tion	>
						0.7	7			(Mo	ode	
					end D[7:	0]					Seal	uential	
										(nsfer	



RDDSM (0E00h): Read Display Signal Mode

0E00H		touu I	<u> </u>	/ Signal RDDS		ead Dis	splay S	Signal	Mode)				
		Add	dress	Т									
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	R	0Eh	0E00h	х	D7	D6	D5	D4	D3	D2	D1	D0	00
				rns the D		Signal			•				
	Bit	Sym	bol	Descript Tearing E			Com	ment					
	D7	TEON	N	On/Off				On, "0"					
	D6	TELC	DM	Tearing e mode	πect iin	е		mode1 mode2	,				
Description	D5	Rese				'0'							
Boochplion	D4 D3	Rese Rese					'0'		_				
	D2	Rese					,0,						
	D1	Rese	rved				ʻ0'						
	D0	Error	on DSI	Error on I	DSI		'0' = 1	No Erro Error	r				
										>			
		9	Status						Ava	ailabili	tv		
				Mode On,	Idle N	lode C	ff, Sle	ep Ou			-9		
Register		-		Mode On,				7		<u> </u>			
Availability		F	Partial M	lode On,	Idle M	ode O	f, Slee	p Out	Yes	;			
		F	Partial M	lode On,	Idle M	ode O	n, Slee	p Out	Yes	3			
		5	Sleep In						Yes	3			
					$\overline{}$								
		S	status				Do	efault '	Value				
Default		Р	ower O	n Sequen	се		00)h					
Boladit	4	S	W Rese	t			00)h					
		Н	IW Rese	et			00)h					
										[-	Le	egend	
	Se	rial I/F I	Mode	Pa	arallel I	/F Mod	le				Co	mmand	$\neg \sqcup$
	R	DDSM (0	DEh)		RDDSM	1 (0Eh)					=	rameter	
								Host					\prec \mid \mid
Flow Chart		◆ Send D[7	7:01		Dumm	v Read	_	Drive	ſ		=	Display	$\mathcal{A} \cap \mathcal{A}$
	_											Action	$\geq \mid \mid$
					Send I) D[7:01	_					Mode	
					Sena I	-[/.0]				į	Sec	quential	
									:		ansfer	<u> </u>	



RDDSDR (0F00h): Read Display Self-Diagnostic Result

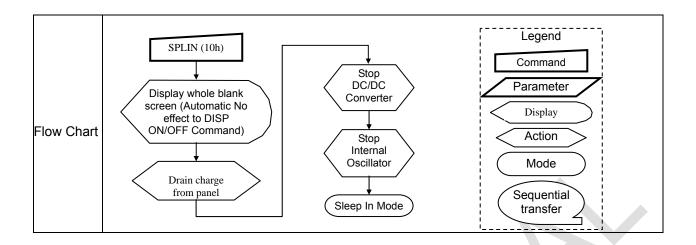
0F00H							ad Dis			agnos	tic Res	sult)		
Inst/Para	R/W	1	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	DO)	HEX
RDDSDR	R	0Fh	0F00h	х	0	0	0	0	0	0	0	checksum	_comp	00
	The	displ	ay mod	lule ret	urns th	ne self	-diagno	ostic re	esults f	ollowir	ig a Sl	eep Out co	ommand	l.
		Bit D0	Symb		Descrip	tion um_con	np			Comme O'	nt			
Description														
Register Availability			N F F	Status Iormal Iormal Partial Partial	Mode Mode Mode	On, Id	dle Mo	de On le Off,	, Slee Sleep	p Out Out	Yes Yes Yes Yes Yes Yes	lability		
			St	atus					Defa	ault Va	alue			
D ("		4	10000	wer O	n Seq	uence	<u> </u>		00h					
Default			SV	V Rese	et				00h					
			H	N Rese	et				00h					
Flow Chart		RE	DDSDR (0Fh)]	R	DDSTR Dummy I	(0Fh)] 7	<u>Hos</u> t Driver			Command Parameter Display Action Mode Sequentia transfer	



SLPIN (1000h): Sleep In

1000H	SLPIN (Sleep In)												
		Ad	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	W	10h	1000h				No A	rgume	nt				
Description	In this n scannin values. After Sle display Out-mod	This command causes the display module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. The control Interface such as registers is still working and keeps its values. After Sleep in command, user can send PCLK, HS and VS information on RGB I/F for blank display and this information is valid during 2 frames if there is used Normal Mode On in Sleep Dut-mode. There is used an internal oscillator for blank display. This command has no effect when the display module is already in Sleep mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).											
Restriction	Sleep Ir It must v stabilize It must v	n Mode wait 5m e. wait 12	can only nsec befo	be exit by re sending ter sendin	the S g next	leep O comma	ut Com and for	mand the su	(11h). pply vo	oltages	and c	ock cir	
			Ctatus							-:1-1-:1:	4		
		-	Status	Mode On	Idle N	Mode C	off Sla	en Ou		ailabili	ty		
Register				Mode On	-		•	-					
Availability		_		lode On,				•					
				lode On,				-					
			Sleep In				<u> </u>		Yes	3			
Default			SW	ver On Se Reset Reset	quenc	e S	Default Gleep Ir Gleep Ir Gleep Ir	n Mode n Mode)				

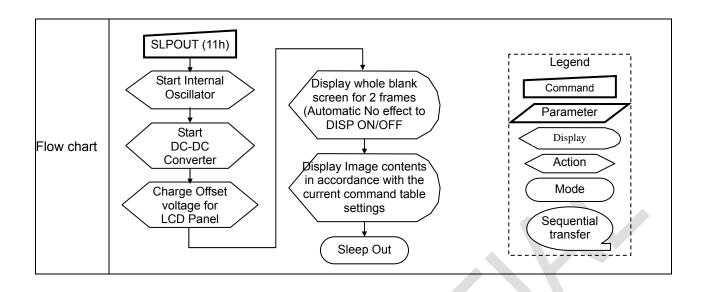






SLPOUT (1100h): Sleep Out

1100H					SLPC	OUT (S	leep O	ut)					
		Add	lress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	W	11h	1100h		•	•	No A	Argum	ent		•		
Description	This comi module a modules f	re enable	d. The ho	st proce	essor s	ends F	CLK, I	HS and	d VS in	format	ion to	display	,
Restriction	is not in S command circuits to The host sending a the registe display de or when t	his command shall not cause any visible effect on the display device when the display module not in Sleep mode. The host processor must wait five milliseconds after sending this ommand before sending another command. This delay allows the supply voltages and clock recuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command before ending a Sleep-In command. The display module loads the display module's default values to be registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same of when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.											
		Sta	tus					\	Avail	ability			
			rmal Mod	le On, lo	dle Mo	de Off	Sleep	Out	Yes				
Register		No	rmal Mod	le On, le	dle Mo	de On	, Sleep	Out	Yes				
Availability		Par	tial Mode	On, Id	le Mod	le Off,	Sleep	Out	Yes				
		Par	tial Mode	On, Id	le Mod	le On,	Sleep	Out	Yes				
		Sle	ep In						Yes				
Default	Status Power On Sequence Sleep In Mode SW Reset Sleep In Mode HW Reset Sleep In Mode												





PTLON (1200h): Partial Display Mode On

1200H		PTLON (Partial Display Mode On)												
Inst/Para	R/W		ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
		MIPI	Other											
PTLON	W	12h	1200h				No	Argum	ent					
Description	Display To leave written.	Mode we Partial The hoses for two	causes the display module to enter the Partial Display Mode. The Partial vindow is described by the Partial Area (30h) command. I Display Mode, the Normal Display Mode On (13h) command should be st processor continues to send PCLK, HS and VS information to display of frames after this command is sent when the display module is in Normal											
Restriction	This cor	his command has no effect when Partial Display Mode is already active.												
			Status Normal	Mode O	n. Idle	Mode (Off. Sle	ep Ou	7000	ilabilit	у			
Register		_		Mode O				-		<u> </u>				
Availability		F	Partial N	lode On	, Idle N	/lode O	ff, Sle	ep Out	Yes					
		F	Partial M	lode On	, Idle N	/lode C	n, Sle	ep Out	Yes	i				
		\$	Sleep In						Yes	i				
						\ 								
Default	Status Default Value Power On Sequence Normal display mode On SW Reset Normal display mode On HW Reset Normal display mode On													
Flow Chart	Refer to Partial Area (30h)													



NORON (1300h): Normal Display Mode On

1300H				NORON (No	rmal	Displ	ay Mo	de O	n)						
		Add	dress												
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
NORON	W	13h	1300h			No A	Argun	nent							
Description	as Parti The hos	This command causes the display module to enter the Normal mode. Normal Mode is define as Partial Display mode. The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode. This command has no effect when Normal Display mode is already active.													
Restriction	This cor	nmand	has no e	ffect when Norma	al Dis	play r	node	is alre	eady a	active					
										V					
			Status						Avail	abilit	y				
		I	Normal I	Mode On, Idle M	ode (Off, S	leep (Out	Yes	A,					
Register		Ī	Normal I	Mode On, Idle M	ode (On, S	leep (Out	Yes						
Availability		I	Partial M	lode On, Idle Mo	de O	ff, Sl	еер О	ut	Yes						
		I	Partial M	lode On, Idle Mo	de O	n, Sle	еер О	ut	Yes						
		:	Sleep In						Yes						
			Sta	tus	D	efault	Value	9							
Default			Pov	ver On Sequence	N	ormal	Displ	ay Mo	ode O	n					
Delaan				Reset			Displ								
			HW	Reset	N	ormal	Displ	ay Mo	ode Ö	n					
Flow Chart	Refer to	the des	scription	of Partial Area (3	000h)									

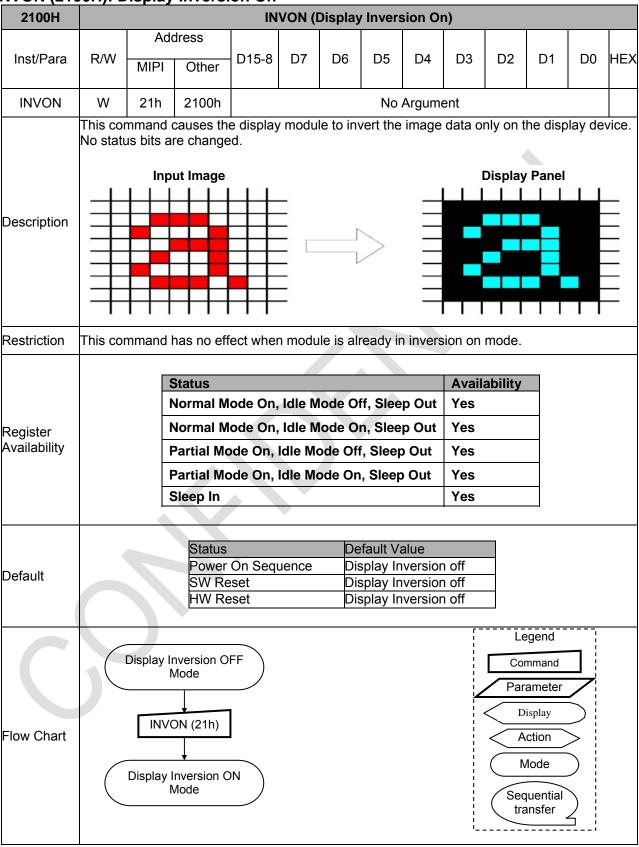


INVOFF (2000H): Display Inversion Off

2000H		,	<u>,</u>		OFF (D	isplay	Inver	sion O	ff)				
		Addres	SS										
Inst/Para	R/W	MIPI (Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	W	20h	2000h				No Arç	gumen	t				
				the display are changed		to sto	p inver	ting th	e imag				У
			Input Ima	age					1 1	Dis	splay I	Panel	1
Description													
Restriction	This c	comman	nd has no	effect when	the dis	play m	odule i	is not i	nverting	g the d	isplay	image	
Register Availability			Norma Partial	I Mode On, I I Mode On, I Mode On, Id Mode On, Id	ldle Mo	ode Or	, Sleep	p Out Out	Avail Yes Yes Yes Yes	ability			
Default			P S	tatus ower On Sec W Reset W Reset	quence	Di: Di:	efault V splay li splay li splay li	nversio nversio	n off				
Flow Chart			INVC	OFF (20h) nversion OFF Mode							Pa I Se	egend ommand rameter Display Action Mode quentia ansfer	



INVON (2100H): Display Inversion On

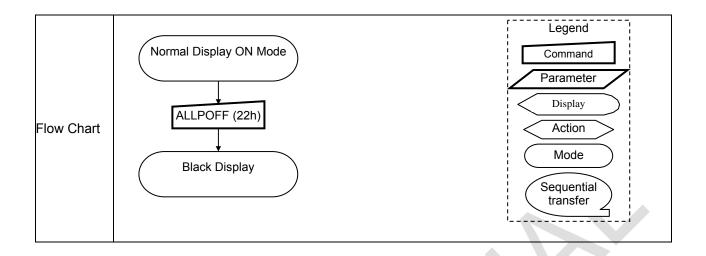




ALLPOFF (2200H): All Pixel Off

ALLPOFF (2200	1). 🔼	I I IXEI O	11		A115							
2200H						ALLPO)FF						
		Ad	ddress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ALLPOFF	W	22h	2200h				No A	raumor	\				
ALLPOFF				display pa	nol bla	ck in S		rgumer		ctatus	of the	Dienla	<u> </u>
	On/Of	f regist	er can be o				·	ut mou	e and a	siaius	o or trie	Dispia	ıy
		li	nput Ima	ge					Disp	olay P	anel		
Description	this m	ode. Tr	ne display p	Display Mo	wing th								
Restriction	-												
			Status						Availa	bility			
			Normal I	Mode On, I	dle Mo	de Off	, Sleep	Out	Yes				
Register			Normal I	Mode On, I	dle Mo	de On	, Sleep	Out	Yes				
Availability			Partial N	lode On, Id	lle Mo	de Off,	Sleep	Out	Yes				
			Partial M	lode On, Id	lle Mo	de On,	Sleep	Out	Yes				
			Sleep In						Yes				
Default			SW F	r On Seque	ence	Disp Disp	ault Va blay Inv blay Inv blay Inv	ersion/ersion	off				



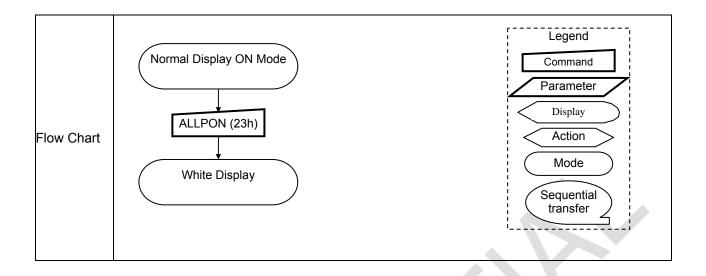




ALLPON (2300H): All Pixel On

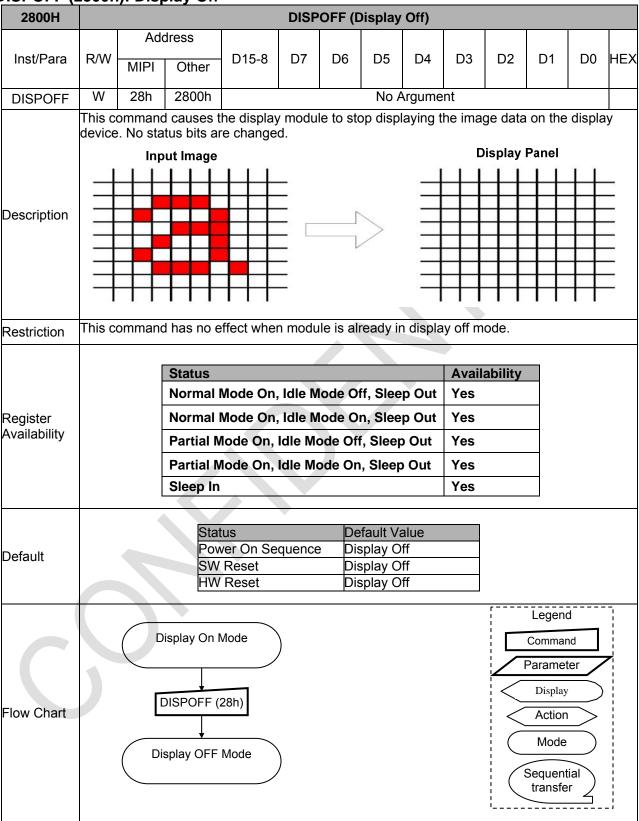
2300H						ALLP	ON						
Inst/Para	R/W	Ad MIPI	ldress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ALLPON	W	23h	2300h				No A	Argum	ent				
Description	On/Off r This cor	els Off", 6	furns the discan be on codoes not character Image "Normal Disdisplay pan Mode On" of	or off. lange an splay Moel is sho	ode On	r status	· ·	ode Or	Displation of the community of the commu	ay Pa	nel	ed to le	eave
Restriction	-												
Register Availability		1 1 F	Status Normal Mod Partial Mod Partial Mod Sleep In	de On, I le On, Id	dle Mo	de On de Off,	, Sleep Sleep	Out Out	Availa Yes Yes Yes Yes	ability			
Default			Status Power C SW Res HW Res	et .	ence	Disp Disp	ault Val blay Inv blay Inv	ersion ersion	off				





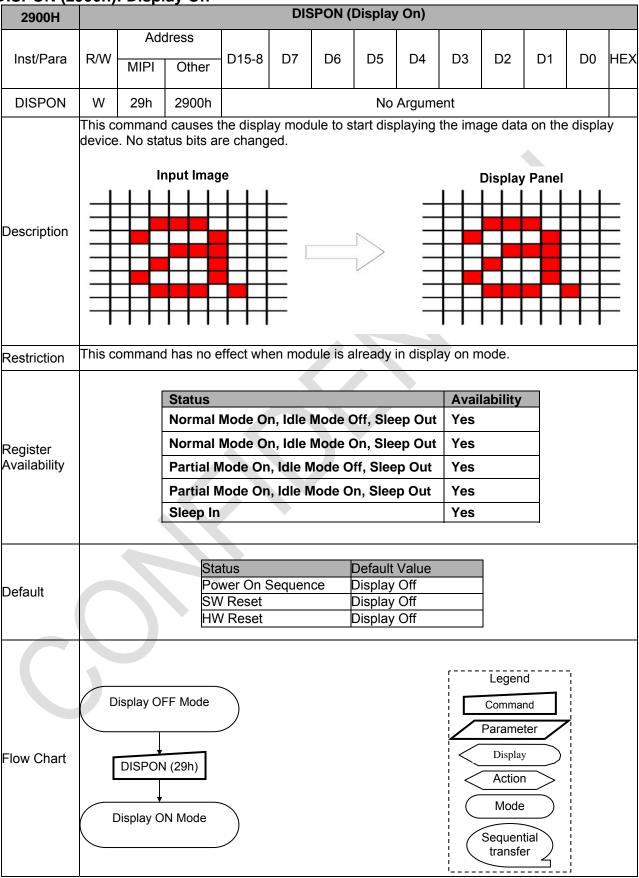


DISPOFF (2800h): Display Off





DISPON (2900h): Display On



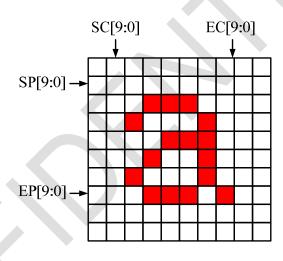


CASET(2A00h~2A03h) : Set Column Start Address

	CASET												
In at/Dana	DAM	Add	lress	D45.0	D.7	DC	Dr	D4	Da	DO	D4	DO	ш
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			2A00h	х	_	-	-	_	-	-	SC9	SC8	00
CASET	W/R	2Ah	2A01h	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
CASET	VV/IX	2/(11	2A02h	х	-	-	-	-	-	-	EC9	EC8	01
			2A03h	Х	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.

This command makes no change on the other driver status. The values of SC[9:0] and EC[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Description

(1) SC[9:0] always must be equal to or less than EC[9:0].

(2) The SC[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.

Register Availability

Restriction

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes



	Status	D	efault Value	
	Status	SC[9:0]	EC[9:0]	
Default	Power On Sequence	0000h	018Fh	
	SW Reset	0000h	018Fh	
	HW Reset	0000h	018Fh	
Flow Chart	CASET 1st & 2nd Param 3rd & 4th Param RASET 1st & 2nd Param 3rd & 4th Param RAMWR RAMWR D1[B:0],D2[B:0	eter: SC[9:0] eter: EC[9:0] (2Bh) eter: SP[9:0] eter: EP[9:0] (2Ch) Data]Dn[B:0]	Legend Command Parameter Display Action Mode Sequential transfer	

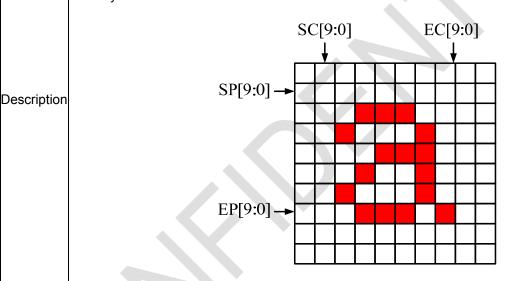


RASET(2B00h~2B03h): Set Row Start Address

2B00H	RASET												
La at/Dana	DAA	Add		D45.0	45.0		ר	D.4	D0	D0	D.4	DO	
Inst/Para	ara R/W M	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		W/R 2Bh	2B00h	х	1	-	1	-	ı	1	SP9	SP8	00
RASET	DACET W/D		2B01h	х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
NASET W/	VV/IX		2B02h	х	ı	-	-	-	ı	-	EP9	EP8	01
			2B03h	Х	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	8F

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.

This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



(1) SP[9:0] always must be equal to or less than EP[9:0]

Restriction (2) The SP[9:0] and EP[9:0]-SP[9:0]+1 must can be divisible by 2.

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Pogiator	Normal Mode On, Idle Mode On, Sleep Out	Yes
Register vailability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes



	Otatua	Defa	ault Value
	Status	SP[9:0]	EP[9:0]
Default	Power On Sequence	0000h	018Fh
	SW Reset	0000h	018Fh
	HW Reset	0000h	018Fh
Flow Chart	CASET (2Ah 1st & 2nd Parameter: 3rd & 4th Parameter: RASET (2Bh 1st & 2nd Parameter: 3rd & 4th Parameter: RAMWR (2Cl Image Data D1[B:0],D2[B:0]	SC[9:0] EC[9:0] SP[9:0] EP[9:0] h)	Legend Command Parameter Display Action Mode Sequential transfer



RAMWR (2C00h): Memory Write

2C00H						RAN	/WR						
la at/Dana	DAM	Ad	ddress	D45.0	D.7	Do	D.5	D.4	D0	D0	D4	Do	
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR			2C00h	Х	0	0	1	0	1	1	0	0	2C
	DAM	2Ch	1 st Pixel	Х	D ₁ 7	D₁6	D₁5	D ₁ 4	D ₁ 3	D ₁ 2	D ₁ 1	D ₁ 0	
	R/W	2Ch	:	X	:	:	:	:	:		1		
			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0	
Description	memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command.												
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												
					Statu	S			A۱	/ailabili	ty		
	Normal Mode On, Idle Mode Off, Sleep Out												
			Normai i		,	/lode O	off, Slee	ep Out		Yes			
Register			Normal I					<u> </u>		Yes Yes			

Partial Mode On, Idle Mode On, Sleep Out

Sleep In

Yes

Yes



		Status Power On Sequence	Default Value Contents of memory is set randomly	
Default		SW Reset	Contents of memory is not cleared	
		HW Reset	Contents of memory is not cleared	
Flow chart		RAMWR (2Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer	



RAMRD (2E00h): Memory Read

2E00H	RAMRD												
Inst/Para	R/W	Ac MIPI	Idress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			2E00h	Х	0	0	1	0	1	1	1	0	2E
RAMRD	D.044	0=1	1 st Pixel	Х	D ₁ 7	D ₁ 6	D ₁ 5	D ₁ 4	D ₁ 3	D ₁ 2	D ₁ 1	D ₁ 0	
	R/W	2Eh	:	Х	:	:	:	:	:	:	:	:	
			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0	
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	There is	no res	triction or	length o	of parai	neters	1						
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												



Default	Status Power On Sequence SW Reset HW Reset	Default Value Contents of memory is set randomly Contents of memory is not cleared Contents of memory is not cleared	
Flow chart	Dummy Read Dummy Read Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer	



3000H					Р	TLAR (Partial	Area)					
		۸۵۵	****										
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
moor ara		MIPI	Other	2.00	.								,
			3000h	х	-	-	-	-	-	-	SR9	SR8	00
			3001h	Х	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
PTLAR	R/W	30h	3002h	х	-	-	-	-	-	-	ER9	ER8	01
			3003h	х	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	8F
-			d defines										
			illustrate										
	If End	d Row >	Start Ro	ow									
	Star	t Row								-			
	SR[\rightarrow							_			
	J. (1)	0.01											
			-		-	+-	++		+	-			
			_						11	- >	Partia Area		
			_							-	Alea	8	
	End	Row											
	ER[9:0] -	→ ±										
			-							-			
Description				//	_					-			
	If End	d Row <	Start Ro	ow									
			_										
			_		-	-	-	-		+	3	Partial	
	ER	[9:0]	→_							二	5	Area	
			_			-				++-			
			=							世			
										\blacksquare			
			-	Н					-	+			
										\equiv			
	SR	[9:0]		-		_	_	_	-	++-	7	Partial	
		.[3.0]	_							二	>	Area	
			_							\perp	ノ		
	IE E		a										
			Start Ro R[9:0] se						ow deep				



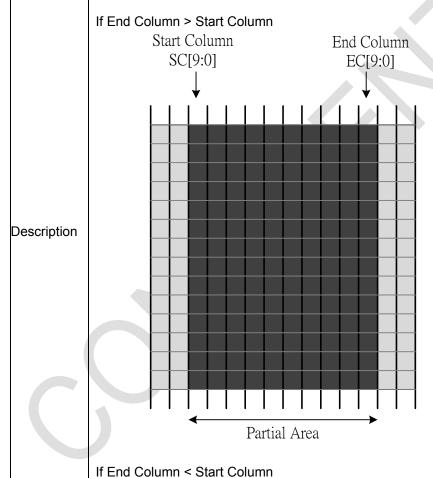
	Status		Availability	
	Normal Mode (On, Idle Mode Off, Sleep Ou	t Yes	
Register	Normal Mode (On, Idle Mode On, Sleep Ou	t Yes	
Availability	Partial Mode C	on, Idle Mode Off, Sleep Out	Yes	
	Partial Mode C	on, Idle Mode On, Sleep Out	Yes	
	Sleep In		Yes	
	Ctatua	Default Value		
	Status	SR[9:0]	ER[9:0]	
Default	Power On Sequence	0000h	018Fh	
	SW Reset	0000h)18Fh	1
	HW Reset	0000h	018Fh	
				_
	1. To Enter Partial Mod		Mode	
	PTLAR (30h)	Partial Mode	Optional to	
	1 st & 2 nd Parameter:	DISPOFF (28h)	nrevent tearing	
	SR[9:0]		display	
	3 rd & 4 th Parameter: ER[9:0]	NORON (13h)	Legend	
		Partial Mode OF	F	
Flow chart	PTLON (12h)		Parameter	
	Partial Mode	, 1	Display	\supset
	Fartial Wode	Image Data	Action	\geq
		(D1[B:0],D2[B:0].	Mode	
		Dn[B:0]	Sequential	
		DISON (29h)	transfer	<u> </u>
			'	'
	Note : B=23			



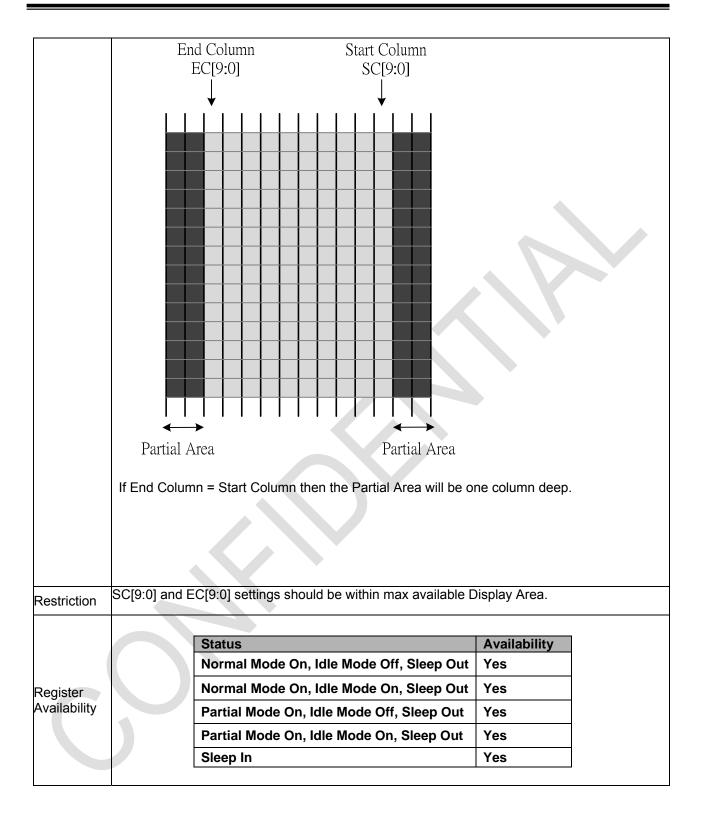
PTLAR (3100h): Vertical Partial Area

3000H		PTLAR (Partial Area)												
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
IIISVFala	moor ard TVVV	MIPI	Other	D 13-0	D1	Do	DS	D4	50	DZ	וט		ПЕЛ	
		:/W 30h	3100h	х	ı	-	-	-	-	ı	-	SC8	00	
DTLAD	DAA		3101h	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00	
PTLAR	K/VV		3102h	х	ı	-	-	-	-	ı	-	EC8	01	
			3103h	х	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F	

This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure.









	Status	Default Value	
		SC[9:0]	EC[9:0]
Default	Power On Sequence	0000h	018Fh
	SW Reset	0000h	018Fh
	HW Reset	0000h	018Fh
Flow chart	1. To Enter Partial Mod PTLAR (30h) 1st & 2nd Parameter: SR[9:0] 3rd & 4th Parameter: ER[9:0] PTLON (12h) Partial Mode Note: B=23	Partial Mode DISPOFF (28) NORON (13h Partial Mode O Image Data D1[B:0],D2[B:0Dn[B:0] DISON (29h)	Optional to prevent tearing effect image display Legend Command Parameter Display Action Mode Sequential transfer



TEOFF (3400h): Tearing Effect Line OFF

3400H		<u> </u>		TEC	OFF (T	earing	Effec	t Line	OFF)				
		Addr	ess										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	W	34h	3400h				No A	rgume	nt				
Description	This line.	command	d turns o	ff the disp	olay mo	odule's	Tearir	ng Effe	ct outp	out sigi	nal on	the TE	signal
Restriction	This	command	d has no	effect wh	en the	Tearir	ng Effe	ct outp	out is a	Iready	off.		
			Status	l Mada O	n Idla	Mada	04. 0	·loon (A. 1	Availab	oility		
				l Mode O l Mode O	-					es es		-	
Register Availability				Mode Or						es es			
				Mode Or	-				- 100	es		_	
			Sleep I		•					'es			
		•											
Default				Status Power (SW Res HW Res	set	quence	:	Defau OFF OFF OFF	lt Valu	e			
Flow Chart	(TE	ne Output	h)							Para Dis	gend mand meter splay etion ode uential nsfer	



TEON (3500h): Tearing Effect Line ON

	TEON (Tearing Effect Line ON)												
D/M/	Address		D15.9	D7	De	DE	D4	D3	D2	D1	DO	HEX	
FX/VV	MIPI	Other	ס-פום	יט	סם	D3	D4	БЗ	DZ	ים	D0	ПЕХ	
R/W	35h	3500h	Х	0	0	0	0	0	0	0	TELOM	00	
	R/W	R/W MIPI	R/W Address MIPI Other	Address	Address	TEON (Tearing R/W Address D15-8 D7 D6	TEON (Tearing Effect R/W Address D15-8 D7 D6 D5	TEON (Tearing Effect Line R/W Address D15-8 D7 D6 D5 D4	TEON (Tearing Effect Line ON) R/W Address D15-8 D7 D6 D5 D4 D3	TEON (Tearing Effect Line ON)	Name	Name	

Bit	Symbol	Description	Comment
D0	TELOM	Output mode of TE signal	0:only V-blanking 1:V-blanking +H-blanking

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.



If TELOM = 1:

Description

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.

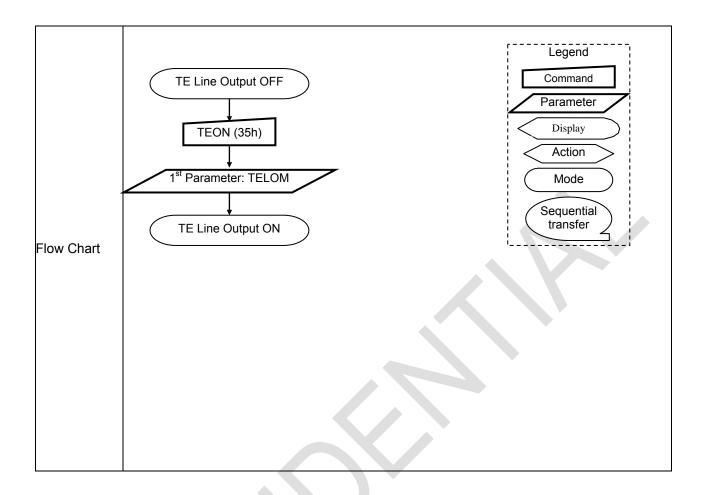


The Tearing Effect Output line shall be active low when the display module is in Sleep mode.



Restriction	This command has no effect when Tearing Effect output is alr	eady ON.
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
Register	Partial Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
		D
Default	Status Power On Sequence OFF SW Reset HW Reset OFF	





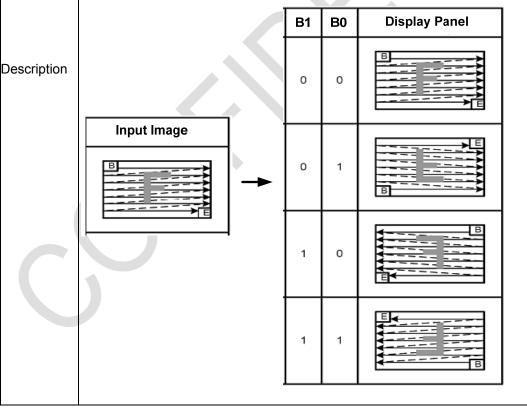


MADCTR (3600h): Scan Direction Control

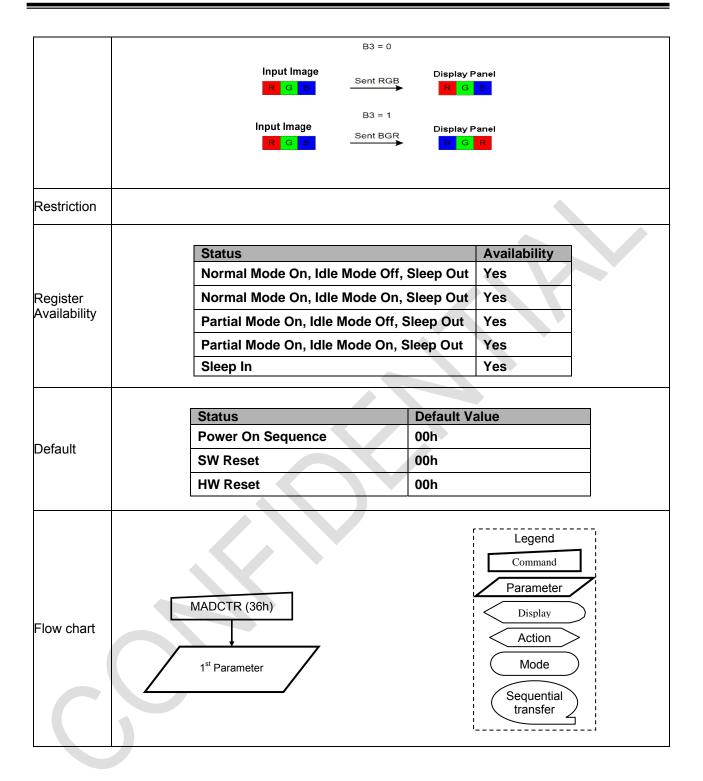
3600H		MADCTR (Scan Direction Control)												
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
	I TO VV	MIPI	Other	ס-פוע			D3	D4						
MADCTR	W	36h	3600h	х	D7	D6	D5	D4	D3	D2	D1	D0	00	

This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.

Bit	Symbol	Description	Comment
D7	MY	Row Address Increment	0: Increasing in vertical
D1	IVI I	Now Address increment	1: Decreasing in vertical
D6	MX	Column Address Increment	Increasing in horizontal
DO	IVIA	Column Address increment	1: Increasing in horizontal
D5	MV	Row/Column Order (MV)	0: Row/column exchange
DS	IVIV	Row/Column Order (MV)	1: Normal
D4	ML	Vertical Refresh Order	0: LCD Refresh Top to Bottom
D4	IVIL	Vertical Refresh Order	1: LCD Refresh Bottom to Top
D3	RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
D2	Reserved		0
D1	RSMX	Horizontal Flip	'0' = Normal display
וטו	KOWA	Horizontal Filp	'1' = Flipped display
D0	RSMY	Vertical Flip	'0' = Normal display
טט	KOIVII	Vertical Flip	'1' = Flipped display









IDMOFF (3800h): Idle Mode Off

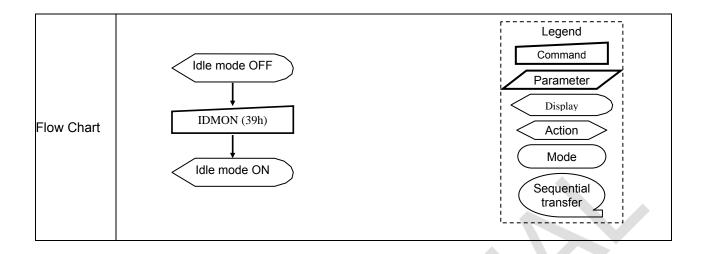
3800H		10110 111	<u> </u>	II	DMOF	F (Idle	Mode	Off)					
Inst/Para	R/W	MIPI	Idress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	W	38h	3800h		l		No A	rgume	nt	l			
Description	This c	ommano	d causes th	e display	module	e to ex	it Idle r	node.					
Restriction	This c	ommano	d has no eff	ect when	the dis	splay n	nodule	is not	in Idle	mode.			
Register Availability			Status Normal M Normal M Partial M Partial M Sleep In	ode On, I	dle Mo	ode Off	n, Slee	p Out	Yes		у		
Default				Status Power Or SW Rese HW Rese	t	ience	ldle ldle	fault V e Mode e Mode e Mode	e Off e Off				
Flow Chart	\ [\	IDMC	node ON DFF (38h) ode OFF							Pal D A A Sec	egend mmand rametel Display Action Mode quentia ansfer		



IDMON (3900h): Enter_idle_mode

3900H					Ent	er_idle	e_mod	de					
		Add	Iress										
Inst/Para	R/W			D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
moor ara	1000	MIPI	Other										''_/
IDMON	W	39h	3900h				No <i>i</i>	Argum	ent				
			auses the								Δ.		
			or express he R, G a								device	e using	the
	IVISBUI				OI COIII	ponen	ເຣ ແາ ແາ	e iripu	ı ımaye		nel Di	oplov	
		ır	put Imag	ge								Spiay	Î
	-							-					
								\					
İ								/ .	-				
i													
i	_												
Description					_								
	la.								9				
	Color		6 R5 R4 R3	R2 R1 R0	700	37 G6 G			B5 B4 B	3 B2 B1	В0		
	Black		XXXX)XXXXX				0XXXX			
	Blue		XXXX		- 4	XXXXX							
	Red		XXXX		VIII.	XXXXX				0XXXX			
	Mager Green		XXXXX			XXXXX				1XXXX			
	Cyan		XXXX			1XXXXX				1XXXX			
	Yellow		XXXX			1XXXXX				0XXXX			
	White		XXXX			1XXXXX				1XXXX			
					l								
Restriction	This cor	nmand h	as no effe	ct when	modul	e is alr	eady ir	n idle o	n mod	e.			
		S	tatus						Avai	lability	/		
		N	ormal Mo	de On,	Idle M	ode Of	f, Slee	p Out	Yes				
Register		N	ormal Mo	de On,	Idle M	ode Or	n, Slee	p Out	Yes				
Availability		P	artial Mod	de On, le	dle Mo	de Off	, Sleep	Out	Yes				
		P	artial Mod	de On, Id	dle Mo	de On	, Sleep	Out	Yes				
		S	leep In						Yes				
				atus				ult Valu					
Default				wer On	Seque	nce		Mode C					
Default			<u> </u>	V Reset				Mode C			_		
			HV	V Reset			idle N	Mode C)TT				







COLMOD (3A00h): Interface Pixel Format

3A00H		. IIItei	iace i) (Inter	face Pi	ixel Foi	mat)				
OAGGII		Δ.1.							maty				
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
COLMOD	W	3Ah	3A00h	Х	0	1	1	1	0		IFPF[1]		77
	This cor	mmand	sets the	pixel for	mat fo	r the R	GB ima	ge data	used	by the i	nterfac	e.	
	IFPF[2:	0] : MCI	J Pixel F	ormat D	efinitio	n.							
			interface				_					d.	
Description			ace Col		nat	<u> </u>	FPF[2]	IFP		IFPF[0	0]		
			,536 col 2,144 co				<u>1</u> 1	(,	0			
			.7M cold				1	_		1			
	ΣΤΟΙΟΡ	10 10	.7 101 0010	<i>,,,</i> ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		I	<u> </u>						
Restriction	_										<u> </u>		
			Status						Ava	ailabilit	у		
			Normal	Mode O	n, Idle	Mode	Off, Sle	eep Ou	t Yes	3			
Register			Normal	Mode O	n, Idle	Mode	On, Sle	eep Ou	t Yes	3			
Availability			Partial N	/lode Or	n, Idle	Mode (Off, Sle	ep Out	Yes	5			
		_	Partial N	_	n, Idle	Mode (On, Sle	ep Out	_				
			Sleep In						Yes	S			
		5	Status				D	efault '	Value				
Default		F	Power O	n Seque	ence		7	7h				-	
Delauit	4		SW Rese	et			7	7h					
		F	W Rese	et			7	7h					
	Exampl	e :							r -				
		16-bits	s/Pixel Mo	ode					! ! !		egend	- , i	
									1	_	mmand		
		COL	MOD (3Ah	1)					į	Par	rameter		
			COLMOD (SAII)							<	Display	\supset \vdash	
Flow chart	_	1 st 1	↓ Parameter		_				!	$\langle $	ction	>	
		•	(06h)	/					į		Mode	$) \mid$	
		_							!	Ser	quential		
		18-bits	s/Pixel Mo	ode					1 1 1		ansfer	$\exists \perp$	
				-					'-				



RAMWRC (3C00h): Memory Continuous Write

3C00H							MWRC								
300011			Address												
Inst/Para	R/W	Ac	ldress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
moor ara	1000	MIPI	Other	D 10 0					20		J.	20	III ZX		
			3C00h	Х	0	0	1	1	1	1	0	0	3C		
RAMWR	R/W	3Ch	1 st Pixel	Х	D ₁ 7	D₁6	D₁5	D ₁ 4	D ₁ 3	D ₁ 2	D ₁ 1	D ₁ 0			
KAWWK	IK/VV	3011	:	Х	:	:	:	:	:	:		:			
1			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0			
Description	memory write_r If MV(3 Data is RAMW written The co written host pr (EP - 3 If MV(3 Data is RAMW written registe frame proces + 1) th Frame When ignore A Mem	ry continuency con	n continuin or RAM frame me register is frame me or sends a to the extra of the ext	m the pix mmand. Ing from WRC(30 emory un another of a pixels a pixels a mory un another of a pixels a mory un a SP and e column er comme ignored a follow a different differen	the pix Ch). The till the pix commander ignored the pix Ch). The till the pix the concept	el locate e column C and to bage rend. If the pred. el locate e page page relumn reer equal the nuisetting eeds (E	ion after register end register	er the wester is the requals to the quals to the quals to the quals to the quals to the record for the wester is the quals to the quals	rite ranhen inc s the E ter is in the End prite ran n incre he End mented umn (E exceed DE=0	orite_m ange of the rement of Page of the rement of the remember of the r	ne preved and umn (Ented. Picker of the prevented and picker of the prevented and picker of the prevented are with	ious pixels C) va xels an alue or SC + 1 ious xels ar lue. Th ritten to e host 1) * (E)	are lue. e the) * e e page the P – SF will be		
Restriction	write lo	cation	. Otherwis written to	se, data	written	with R									



	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Ou	t Yes
	Normal Mode On, Idle Mode On, Sleep Ou	t Yes
Register Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Status Defa	ault Value
Default		mory is set randomly
Delault		emory is not cleared
		emory is not cleared
Flow chart	RAMWRC (3Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer



RAMRDC (3E00h): Memory Continuous Read

RAMRDC (3		. IVICI	nory CC	munuc	Jus K								
3E00H				T		RA	MRDC						
Inst/Para	R/W	Ad	ldress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Description	1000	MIPI	Other	D 10 0		D	D		20	<i>52</i>	<i>D</i> ,	20	I ILX
			3E00h	Х	0	0	1	1	1	1	1	0	3E
DAMBDO	R/W	3Eh	1 st Pixel	Х	D ₁ 7	D₁6	D₁5	D₁4	D₁3	D ₁ 2	D ₁ 1	D ₁ 0	
RAWRDC	FK/VV	SEII	:	Х	:	:	:	:	:	:			
			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0	
Description	memory write_r If MV(3) Data is RAMW written host process or the	sy continemore and the transfer of the state	n continuin or RAM frame me egister is frame me or sends a) the extra or RAM frame me en reset to ry until the nds anoth or pixels are ory Accessorsfer num	m the pix mmand. Ing from WRC(30 mory un another of a pixels a mory un of SP and e column er commer ignored and into ber of da follow a f	the pix Ch). The till the pix Ch). The comma are ignorable the pix Ch). The till the pix the coregister and. If d. erface at a exc	el locate column C and to page rend. If the page render e page render e ender e eds (EET(2Ah	ion after register en en umle register en en umle register en en umle register en	er the wester is the requals to ber of pure the were the were the were the were the were the were the wester the were the wester the were the wester the were the wester the wes	rite rannen incremente Endone	rrite_minge of the rement of Color crement of Page (see the remented Page (see the remember of the remember	me preved and umn (Ented. Pix (EP) value and pix EP) value are wise or the SC +	ious pixels C) va xels are ilue or SC + 1 ious xels are ue. The ritten to e host 1) * (El	are lue. e the) * e e page o the P – SP will be
Restriction			. Otherwis written to				AMWR	(2Ch) a	ınd any	followi	ng RAN	//WRC	(3Ch)



	Status	Availability
	Normal Mode On, Idle Mode Off, Sle	ep Out Yes
Register	Normal Mode On, Idle Mode On, Sle	ep Out Yes
Availability	Partial Mode On, Idle Mode Off, Slee	ep Out Yes
	Partial Mode On, Idle Mode On, Slee	ep Out Yes
	Sleep In	Yes
	Status	Default Value
Default		of memory is set randomly
Delault		s of memory is not cleared
		s of memory is not cleared
Flow chart	RAMWRC (3Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer



STESL(4400h): Set_Tear_Scanline

STESL(4400	11) . 3	et_rea	ar_Sca										
4400H					STESI	_(Set_	Tear_S	canlin	e)				
Inst/Para	R/W		ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other								gend nmand planeter Display		
STESL	W	44h	4400h 4401h	X				STS[12]					00
			440111	Х	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	515[1]	515[0]	00
Description	the dis B4. Th Line m	splay rea ne Tearin	aches lin ng Effect	e N. The	TÉ sigr	nal is n	ot affec	ted by	changi cribes	ing set_	_addres	ss_moo	de bit utput
	The To	earing E	ffect Ou	tput line s	hall be	active	low wh	en the	display	y modu	le is in	Sleep	mode.
Restriction													
		ĺ	Status						Av	ailabili	41/		
				Mode O	n, Idle	Mode	Off, SI	eep Oı			Ly		
Register				Mode O		- 1000			_	s			
Availability			Partial	Mode On	, Idle I	Mode (Off, Sle	ep Ou	t Ye	s			
			Partial	Mode On	, Idle I	Mode (On, Sle	ep Out	Ye	s			
			Sleep I	n					Ye	S			
Default				Status Power Or SW Rese HW Rese	t	ence	STS STS	ault Val [15:0]= [15:0]= [15:0]=	:16'h00 :16'h00	000			
Flow Chart			Send 1st p	tear_scanlin tear_scanlin tear_scanlin tear_scanlin tear_scanlin tear_scanlin tear_scanlin tear_scanlin	e [8]	7			< < <	Paran Dis Acti	nand neter splay		



GSL (4500h): Get_Scanline

93L (4500H)	. 001	_ocan	iiiie										
4500H					GSI	_(Get_	Scanli	ne)					
Inst/Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISUFAIA	FX/VV	MIPI	Other	ס-כו ט	וט	БО	טט	D 4	כם	DZ	וט	DU	
CCI	J	45h	4500h	Х	GTS[15]	GTS[14]	GTS[13]	GTS[12]	GTS[11]	GTS[10]	GTS[9]	GTS[8]	0x
GSL	R	45h	4501h	х	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx
Description	numbe first sc	er of sca an line i	turns the on lines on s defined Mode, th	a display as the firs	device I line o	e is def of V-Sy	ined as nc and	S VSYN	NC + V oted a	BP + V s Line	ACT +		
Restriction	_							A					
		[Status						Ava	ilabili	ty		
			Normal	Mode On	, Idle N	lode O	ff, Sle	ep Ou	Yes	•			
Register			Normal	Mode On	, Idle N	lode C	n, Sle	ep Ou	Yes	i			
Availability		-	Partial N	lode On,	Idle M	ode Of	ff, Slee	p Out	Yes	i			
		-		lode On,	Idle M	ode Oı	n, Slee	p Out	Yes				
		_	Sleep In						Yes	i			
Flow Chart		Send 1s	get_scanline Wait 3us Dummy Read t parameter GTS			2	Com Para A	gend nmand Display Ction Mode equential transfer					



DSTBON (4F00h): Deep Standby Mode On

DSTBON (4F	-uun):	реер	Stand										
4F00H				D	STBON	I(Deep	Stand	by Mod	de On)				
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DSTBON	W	4Fh	4F00h	Х	0	0	0	0	0	0	0	DSTB	00
Description	DSTB: Notes: 1. To 2. Fo	="1", en exit De or MIPI I	d is used ter deep eep Stan F, if dee ~D1_P/N	standby dby Mod standb	mode de, inpu y mode	it low p	ulse mo	ore than	HSSI_	CLK_P		(.	
Restriction	-												
Register Availability			Norma Partial	I Mode (I Mode (Mode ()	On, Idl	e Mode	On, S	leep O	ut Ye	es es	ity		
Default		;	Status Power C SW Res HW Res	et	ence		(Default OOh OOh	Value				
Flow chart		Parai	TBON (4F	B=1						P	Legend Command aramete Display Action Mode equentiatransfer		



WRDISBV (5100h): Write Display Brightness

5100H		,					RDISB	٧					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	W	51h	5100h	х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF
		ciple rela	is used to					st bright	ness ar	nd FFh v	alue me	eans the	highest
Description													
Restriction	The d	isplay s	upplier o	annot u	se this	comm	and for	tuning					
			Status						Α,	vailabil	li4v/		
				l Mode	On, Idl	e Mod	e Off, S	Sleep O		valiabii es	пгу		
Register				I Mode		_		-		es			
Availability			Partial	Mode (On, Idle	Mode	Off, S	leep O	ut Ye	es			
			Partial	Mode (On, Idle	Mode	On, S	leep Ou	ıt Ye	es			
			Sleep	ln					Ye	es			
			Status					Defaul	t Value)			
Default				On Seq	uence			FFh					
			SW Re					FFh					
			nw ke	set				FFh					
Flow chart		Para	RDISBV (5	/[7:0]						P	Legend Command aramete Display Action Mode equenti- transfer	d er	



RDDISBV (5200h): Read Display Brightness

5200H		11000	. <u>- 10 p</u> .	<u>.,</u>	111100		DISBV						
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	R	52h	5200h	Х		DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF
Description		le relat		rightness v s that 00h v		eans the	e lowest	brightn	ess and	l FFh va	alue mea	ans the	highest
Restriction	-									1			
		ſ	Ctatus						L Ave	ailabili	4		
			Status Norma	I Mode O	n, Idle	Mode	Off, SI	eep Ou		<u>ailabili</u> s	ty		
Register			Norma	l Mode O	n, Idle	Mode	On, Sl	еер Оі	ıt Ye	s			
Availability				Mode Or	•			-					
		-		Mode Or	, Idle I	Mode (On, Sle	ep Ou					
			Sleep I	<u>n</u>					Ye	<u>S</u>			
		9	Status			\checkmark	D	efault	Value				
				n Seque	nce			Fh	raido				
Default		;	SW Res	et			FI	Fh					
Delault		I	HW Res	et	\mathbf{V}		FI	Fh					
Flow Chart		nd param DBV[7:0	neter	<u>Ho</u> st Driver	(Lege Comn Paran Disp Acti Moo	neter lay on de						



WRCTRLD (5300h): Write Display Control

5300H		711). .	TIC DIC	piay c	Jones		RDISB	V					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	W	53h	5300h	х	0	0	BCTRL	0	DD	0	0	0	28
Description			ness cont										
Restriction	The d	isplay s	upplier o	cannot u	se this	comm	and for	tuning					
Register Availability Default			Norma Partial Partial Sleep Status Power	Il Mode Il Mode Mode (Mode (In On Seq	On, Idle On, Idle On, Idle	e Mod	e On, S e Off, Si e On, Si	Sleep Oleep Ou	out Yeut Yeut Ye	es es es	lity		
			SW Res					28h 28h					
Flow chart		Para	RDISBV (5	/[7:0]						P	Legend Command Paramete Display Action Mode equentiatransfer	d er	



RDCTRLD (5400h): Read Display Control

		<u>р</u>			RDI	DISBV						
	Add	dress										
R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	54h	5400h	х	0	0	BCTRL	0	DD	0	0	0	28
_									1			
		Status						Av	oilobili	410		
	_		l Mode O	n, Idle	Mode	Off, SI	еер Оі		A 10000	Ly		
	-	Norma	l Mode O	n, Idle	Mode	On, Sl	еер Оі	ıt Ye	s			
	-			-			-					
	-			, Idle I	Mode (On, Sle	ep Ou					
		опсер і						10	<u> </u>			
	9	Status	_		$\underline{}$	D	efault '	Value			1	
			n Seque	nce							1	
	3	SW Res	et			28	3h					
	I	HW Res	et			28	3h					
RDD	DISBV (52hH)	>	,			-					
			Host Driver									
Se	nd param	neter /		<		=						
	DBV[7:0				Acti	on						
		_		(Mo	de						
				i			_ ;					
	R/W R BCTRL: DD: Disp	R/W MIPI R 54h BCTRL: Brightn DD: Display dim	Address R/W MIPI Other R 54h 5400h BCTRL: Brightness contr DD: Display dimming cor Status Norma Partial Partial Sleep I Status Power C SW Rese	R/W Address MIPI Other R 54h 5400h x BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable DD: DD: DD: DD: DD: DD: DD: DD: DD: DD	R/W MIPI Other R 54h 5400h x 0 BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable Status Normal Mode On, Idle Normal Mode On, Idle I Partial Mode On, Idle I Sleep In Status Power On Sequence SW Reset HW Reset RDDDISBV (52hH) Host Driver	RDI R/W Address MIPI Other D15-8 D7 D6 R 54h 5400h x 0 0 BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable Status Normal Mode On, Idle Mode Partial Mode On, Idle Mode Partial Mode On, Idle Mode On Sleep In Status Power On Sequence SW Reset HW Reset RDDDISBV (52hH) Host Driver Paran Disp Acti Mo Sequence	RDDISBV Address MIPI Other D15-8 D7 D6 D5 R 54h 5400h x 0 0 BCTRL BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable Status Normal Mode On, Idle Mode Off, Sle Partial Mode On, Idle Mode Off, Sle Partial Mode On, Idle Mode On, Sle Sleep In Status Power On Sequence SW Reset HW Reset Address D7 D6 D5 BCTRL BCTRL: Brightness control ,1=enable Status Partial Mode On, Idle Mode Off, Sle Partial Mode On, Idle Mode On, Sle Sleep In Legend Command Parameter Display	RW Address MIPI Other D15-8 D7 D6 D5 D4 R 54h 5400h x 0 0 BCTRL 0 BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable DD: Display dimming control ,1=enable Normal Mode On, Idle Mode Off, Sleep Ou Partial Mode On, Idle Mode Off, Sleep Ou Partial Mode On, Idle Mode On, Sleep Ou Sleep In Status Power On Sequence 28h SW Reset 28h HW Reset 28h RDDDISBV (52hH) Host Command Parameter Display Action Mode Sequential	RDDISBV	RDDISBV	RDDISBV	RDDISBV



IMGEHCCTR (5800h) : Set_color_enhance

MGEHCCTR	(580	10h) :	Set_co	lor_	<u>enhan</u>	ice							
5800H					WF	RCE (se	et_colo	r_enha	nce)				
Inst/Para	R/W	Add MIPI	dress Other)15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCE	W	58h	5800h	х	0	0	0	0	0	SLR_EN	SLR_LEV EL1	SLR_LEV EL0	00
Description		R_EN	EL[1:0]	Sun Enh Sun	light Rea	adable nt Enal			'1': e	e disable; nable 2, low to h	nigh		
Restriction	-												
Register Availability		Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Flow Chart		Con Part	gend Inmand Inma										



IMGEHCCTR (5900h): Read_color_enhance

WIGETICCT	(390	UII) . F	reau_u	JOIOI_E	HIIIaII	CE									
5900H					RDCI	E (set_	color_e	enhan	ce)						
Inot/Doro	DAM	Add	ress	D15 0	D7	De	DE	D4	Da	Da	D1	DO	HEX		
IIISVPara	R/W	MIPI	Other	ס-פוע	וט	Do	סט	D4	D3			LEV SLR_LE 1 VEL0			
RDCE	R	59h	5900h	Х	0	0	0	0	0	SLR_EN	SLR_LEV EL1	SLR_LE VEL0	00		
	Dit	_	_	Dog	ccrintio	n	_		Value	_					
				Sur	Sunlight Readable '0'						: disable;				
Inst/Para R/W Address D15-8 D7 D6 D5 D4 D3 D2 D1 D0															
Description				1											
Restriction	_														
			Norma Norma Partial Partial	Mode C	On, Idle	e Mode Mode	On, S	leep O	out out out out	Yes Yes Yes Yes	oility				
Flow Chart	2	Param Param Dis Action Mo Seq	neter play on ode uuential												



CESLRCTR (5A00h): Set color enhance1

CESLRCTR (5AU)n) : 8	et_co	ior_e	ennanc	:e 1							
5A00H					CESL	RCTR (set_co	lor_enh	nance1)				
la a MD a na	D.0.4/	Add	dress	D45.0		Do	DE	D4	D0	D0	D4	D0	LIEV
Inst/Para	R/W	MIPI	Other	D15-8		D6	D5	D4	D3	D2	D1	D0	HEX
CESLRCTR	W/R	5Ah	5A00h	Х	SLR_AM BI_IN7	SLR_AM BI_IN6	SLR_AM BI_IN5	SLR_AM BI_IN4-	SLR_AM BI_IN3	SLR_AM BI_IN2	SLR_AM BI_IN1	SLR_AM BI_IN0	00
	D:				Danasia	41			Valen	_			
	Bit				Descrip				Value	9			
	SLI	R_AMB	SI_IN[7:0]	l	Low byt	e of amb	ient ligh	t value	00h	-			
Description													
Restriction	-												
			01-1	-						A 'I -	1. *1*4	-	
											DIIITY		
Status Availabilit Normal Mode On, Idle Mode Off, Sleep Out Yes Register Normal Mode On, Idle Mode On, Sleep Out Yes													
Availability				_	de On, I	-				Yes			
			Partia	al Mod	de On, le	dle Mod	de On,	Sleep C	Out	Yes			
			Sleep	ln						Yes			
				,									
			jend										
		Con	nmand	_									
	2	Para	ameter										
		\subset	Display										
Flow Chart		< Ac	ction	.									
			Mode										
		S	equential										
			transfer										
				'									



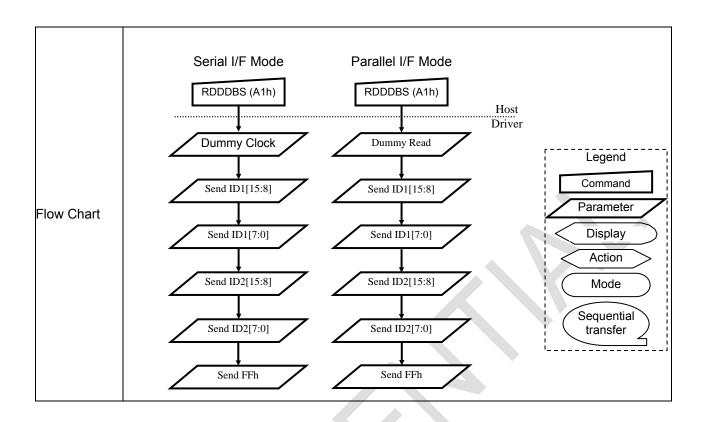
CESLRCTR (5B00h): set_color_enhance1

CESLRCIR	(3000	11) . Se	t_corc	л_ С П	IIIaIICE	_							
5B00H					CESLR	CTR (se	t_colo	r_enha	ince1)				
Inot/Doro	R/W	Add	ress	D15	8 D7	De	D5	D4	D3	D2	D1	DO	ЦГV
Inst/Para	FK/VV	MIPI	Other	D15-	יט ס	D6	טט	D4	D3	D2	וטו	D0	ПЕЛ
CESLRCTR	W/R	5Bh	5B00h	Х	SLR_AN BI_IN15	SLR_AM BI_IN14	SLR_AM BI_IN13	SLR_AM BI_IN12-	SLR_AM BI_IN11	SLR_AM BI_IN10	SLR_AM BI_IN8	00	
	Bit				Description	on			Value				
	SLF	R_AMBI_	_IN[15:8]	F	ligh byte	of ambie	nt light	value	00h			DI_IIA BI_IIAO	
Description													
Restriction	_								<u> </u>				
Register Availability			Norma Partial	l Mode Mode Mode	e On, Id e On, Idle e On, Idle	le Mode	On, S Off, SI	leep O	ut ut ut it	Availal Yes Yes Yes Yes	oility		
Flow Chart		Action Mc Seq	neter play										



RDDDBS(A100h): Read_DDB_Start

A100H						DDBS(RDDDBS(Read_DDB_Start)														
Inst/Para	R/W	Add	Iress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
			A100h	х	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0								
			A101h	х	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01								
RDDDBS	R	A1h	A102h	х	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80								
			A103h	х	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90								
			A104h	х	1	1	1	1	1	1	1	1	FF								
	1 st 2 nd 3 rd 4 th 5 th	param param param	neter: S neter: M	upplier II upplier I lodule IE odule IE h).	D code)																
Restriction																					
Register Availability		4	Nor Part	mal Mod mal Mod tial Mod tial Mod	de On, I	dle Mo	de On, le Off,	Sleep C	Out Y Out Y Out Y Out Y Out Y	es es es es es	lity										
						Defai	ult Value	e.													
		Status	S			After			Before M	ITP											
Default		Powe	r On Se	equence		MTP	Value	0	1h, D0h	n, 90h, 6	60h, FF	h									
		SW R	Reset			MTP	Value	0	1h, D0h	n, 90h, 6	60h, FF	h									
		HW F	Reset			MTP	Value	0	1h, D0h	SW Reset MTP Value 01h, D0h, 90h, 60h, FFh HW Reset MTP Value 01h, D0h, 90h, 60h, FFh											

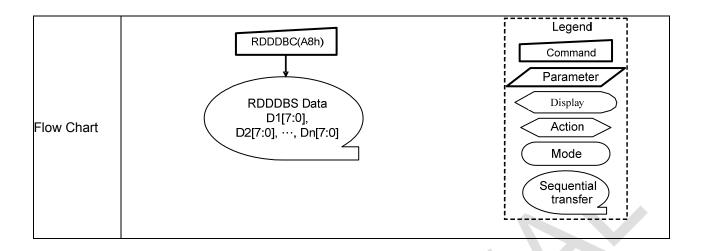




RDDDBC(A800h): Read DDB Continous

A800H		. 116	ad DD	D 0011	mous		RDDDB	C					
		Ado	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			A800h	х	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0
			A801h	Х	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01
RDDDBC	R	A8h	A802h	х	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80
			A803h	х	MID[15]	MID[14]	MID[13]	MID[12]	SID [3] SID [2] SID [1] SID [0] SID [3] SID [2] SID [1] SID [0] MID[3] MID[2] MID[1] MID[0] MID[11] MID[10] MID[9] MID[8] 1 1 1 1 play module mode/revision other command. If there is no more data in the DE cuted at least once before a Real vise, data read with a Read DDE Availability Out Yes 90				
			A804h	x	1	1	1	1				SID [0] SID [0] SID[8] MID[0] MID[8] 1 vision ta in the D	FF
Description	point Note: block Note: 1. Se 2. Re	where Paran For us maxii ad 0x	meter 0x se exan mum re A1, retui	BS comr	n "Exit C ket size es SID[7	Code", tl =3 7:0], SIE	his mea 0[15:8],	ns that MID[7:0	there is	: no moi	re data	in the E	DDB
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue c ommnd is undefined.												
			Stat	us		Α				vailabi	litv		
		•	Nor	Normal Mode On, Idle Mode Off, Sleep Out									
Register			Nor	mal Mod	de On, l	ldle Mo	de On,	Sleep	Out Y	es			
Availability			Part	ial Mod	e On, Id	dle Mod	le Off,	Sleep C	Out Y	es			
			Part	ial Mod	e On, Id	dle Mod	le On, S	Sleep C	Out Y	es			
			Slee	ep In					Υ	es			
		04-4				Default	Value						
		Stat	ius			After M	TP E	Before N	ЛТР				
Default		Pow	ver On S	Sequenc	e l	MTP Va	alue C)1h, D0	h, 90h,	60h, FF	h		
		sw	Reset			MTP Va	alue 0)1h, D0	h, 90h,	60h, FF	h		
		HW	Reset		l	MTP Va	alue C)1h, D0	h, 90h,	60h, FF	h		







RDFCS(AA00h): Read First Checksum

AA00H							RDFCS	3					
Inst/Para	R/W		dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDFCS	R	AAh	AA00h	х	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00
Description	Set" regis	area ters (no ss to th	ot includ	rns the f de "Manu me mem	ıfacture	Comm	and Se						
Restriction	area	vill be necessary to wait 150ms after there is the last write access on "User Command Set ea pisters before there can read this checksum value.											
	_							. 47			<u> </u>	_	
		Status		On, Idl			Availability Yes						
	-					Yes							
Register Availability	-	Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out											
	_			On, Idle		Yes							
		Sleep		On, idie	Widde	On, Sie	ep Oui	•	Yes				
	L	Sieep	111						163				
Default		Status Powe S/W F H/W F	r On Se Reset	quence		C	Default \ 00h 00h 00h	Value _					
Flow Chart				RDFCS Send Pa FCS	rameter					P	Legend Command aramete Display Action Mode equentia transfer		



RDCCS(AF00h): Read Continue Checksum

AF00H							RDCC	S								
Inst/Para	R/W	Add	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
RDCCS	R	AFh	AF00h	х	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00			
Description	the fir	rst ksum h	nas calc	ulated fr	om "Us	er Com	RDCCS D6 D5 D4 D3 D2 D1 D0 HI CCS6 CCS5 CCS4 CCS3 CCS2 CCS1 CCS0 CC checksum what has been calculated continuously after r Command Set" area registers and the frame memoraters and/or frame memory has been done. It there is the last write access on "User Command Set" area registers and the frame memory has been done. It this checksum value in the first time. Availability Fe Off, Sleep Out Yes Fe On, Sleep Out Yes Default Value Ooh									
Restriction												ommar	nd Set"			
		Stati							Avoile	hility.						
				de On Jo	dle Mod	le Off	Sleen (Out	40000	ability						
Register																
Availability		Parti	ial Mod	e On, Id	le Mod	Yes										
		Parti	ial Mod	e On, Id	le Mod	Yes										
		Slee	p In						Yes			ommand				
Default		Powe S/W F H/W F	r On Se Reset	quence				00h 00h	ault Valu	Je						
Flow Chart		5		Send Pa CCS	rameter					P	aramete Display Action					



SetDSIMode (C200h): set_DSI Mode

<u>SetDSIMode</u>	(C20	0h) :	set_DS	<u> </u>	de								
C200H		SetDSIMode											
		Add	dress										HEX
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	4 D3	D2	D1	D0	
SetDSIMode	W/R	C2h	C200h	х	0	0	0	0	0	0	DM1	DM0	00
	В	Bit		Des	cription				Value		_		
	D)M[1:0]			-		selection	n	2'b00: inte 2'b01: auto exte 2'b10: rese 2'b11: exte	o detecti ernal tim erved	on interr ing	nal or	
Description													
Restriction	Note: (1) If	video	mode, ne	eed to	set DN	/I[1:0] =	2'b01 o	or 2'b	o11.				
			Status					_		Availa	hility		
					de On.	Idle Mo	de Off,	Sle	ep Out	Yes	Dility	1	
Register				_		-	de On,		-	Yes			
Availability							de Off,		-	Yes			
							de On, S		-	Yes			
			Sleep	In			· · · · · · · · · · · · · · · · · · ·		-	Yes			
Flow Chart		Con Para	gend nmand Display Ction Mode equential transfer										

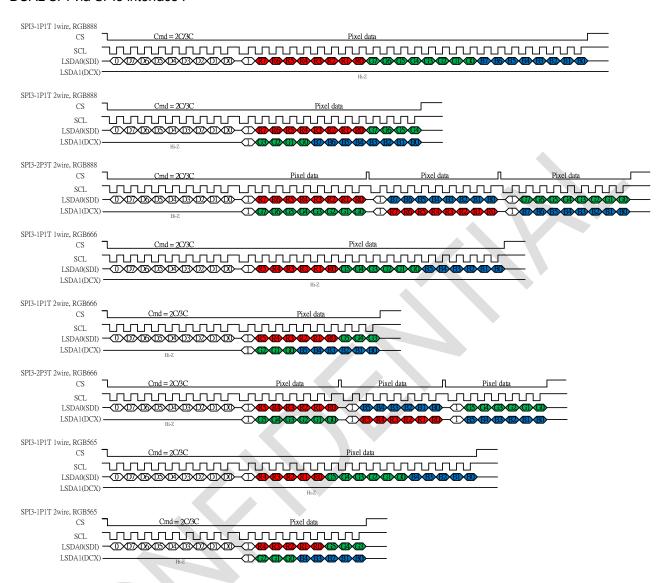


SetDSPIMode (C400h): set_DSPI Mode

<u>е (С4</u>	iuun)	: set_L	<u> </u>	<u>woae</u>								
					Set	DSPI r	node					
R/W	Add		D15 <u>-</u> 8	D7	D6	D5	Π4	D3	D2	D1	DO	HEX
17///	MIPI	Other	D 10-0	<i>D1</i>	Do				DZ	וט		
W/R	C2h	C200h	Х	-	-	DSPI_C FG1	DSPI_0 FG0	-	-	-	DSPI_E N	00
E	Bit		Des	cription	1		V	/alue				
С	SPI_EN	l	DAU	JL SPI N	ODE E	nable						
С	SPI_CF	G[1:0]	DAU	JL SPI M	IODE S	election	1	0: 1P1T f 1: 2P3T f	or 2 wire or 2 wire			
Note	: detail	ed DAUL	. SPI f	ormats	are des	scribed	at next	t page.				
		Status	•						Δvaila	hility		
				de On,	Idle Mo	ode Off,	Sleep	Out	Yes	Dility		
		-		\ \					Yes			
		Partia	l Mod	e On, I	dle Mo	de Off,	Sleep	Out	Yes			
		Partia	l Mod	e On, I	dle Mo	de On,	Sleep	Out	Yes			
•		Sleep	In						Yes			
	Com Para L An Si	ameter Display Etion Mode)									
	R/W W/R	R/W Add MIPI W/R C2h Bit DSPI_EN DSPI_CF Note: detail	R/W Address MIPI Other W/R C2h C200h Bit DSPI_EN DSPI_CFG[1:0] Note: detailed DAUL Status Norma Norma Partia Partia	R/W Address MIPI Other W/R C2h C200h x Bit Destar DAL DSPI_EN DAL DSPI_CFG[1:0] DAL DSPI_CFG[1:0] DAL SPI 1 Note: detailed DAUL SPI 1 Status Normal Mode Normal Mode Sleep In Legend Command Parameter Display Action Mode Sequential	R/W Address MIPI Other W/R C2h C200h x - Bit Description DSPI_EN DAUL SPI M DSPI_CFG[1:0] DAUL SPI M Note: detailed DAUL SPI formats Status Normal Mode On, Normal Mode On, Partial Mode On, le Partial Mode On, le Sleep In Legend Command Parameter Display Action Mode Sequential	R/W Address MIPI Other W/R C2h C200h x Bit Description DSPI_EN DAUL SPI MODE E DSPI_CFG[1:0] DAUL SPI MODE So Note: detailed DAUL SPI formats are description Normal Mode On, Idle Mode On,	R/W Address D15-8 D7 D6 D5 W/R C2h C200h x - DSPI_C FG1 Bit Description DSPI_EN DAUL SPI MODE Enable DSPI_CFG[1:0] DAUL SPI MODE Selection Note: detailed DAUL SPI formats are described Status Normal Mode On, Idle Mode Off, Normal Mode On, Idle Mode Off, Partial Mode On, Idle Mode Off, Partial Mode On, Idle Mode On, Sleep In	R/W Address MIPI Other D15-8 D7 D6 D5 D4	R/W Address D15-8 D7 D6 D5 D4 D3	R/W Address D15-8 D7 D6 D5 D4 D3 D2 W/R C2h C200h x DSPI_C DSPI_C FG0 Bit DAUL SPI MODE Enable D3 D3 D4 D3 D3 D4 D3 D5 D3 D4 D3 D5 D3 D4 D3 D5 D3 D5 D4 D4 D3 D5 D5 D4 D4 D3 D5	Set DSPI mode	Set DSPI mode R/W Address MIPI Other D15-8 D7 D6 D5 D4 D3 D2 D1 D0 W/R C2h C200h x - DSPLC DSPLC - DSPLC D1 D1 D0 Bit Description Value D3 D2 D1 D1 D0 D3 D2 D1 D3 D3 D2 D1 D3 D3 D3 D2 D1 D3

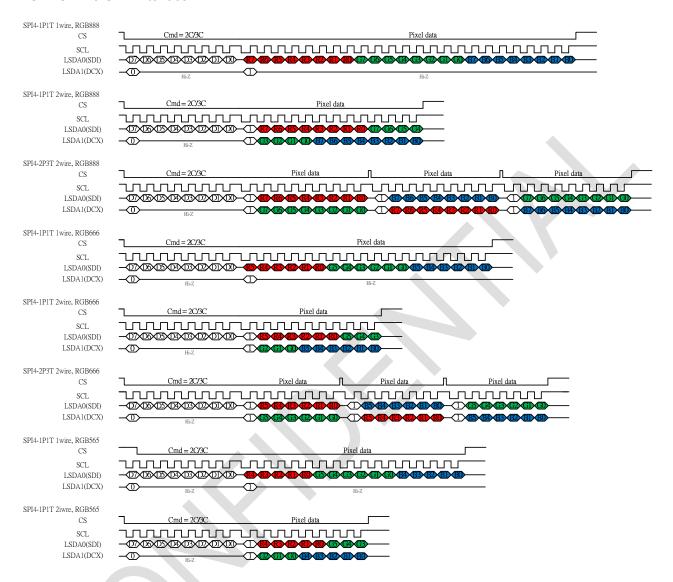


DUAL SPI via SPI3 interface:





DUAL SPI via SPI4 interface:

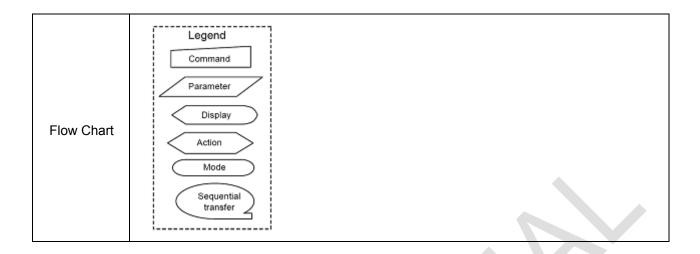




(FE00h): CMD Mode Switch

-	IVIOU	MAUGCER (Manufacture Command Set Control)											
FE00H		MAUCCTR (Manufacture Command Set Control)											
Instruction	R/W		dress					Param		1	I		
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HE
CMD Mode Switch	W/R	FEh	FE00h	00h	0	0	0	0	C	CMD_P	age[3:	0]	00
	This	comm	and is u	sed to sw	itch the	Manu	ıfacture	Comn	nand P	ages a	nd Use	er	
	Com	mands	s sets.										
	CI	MD_Pa	ge[3:0]	Hex '	Value			Description					
		0000		00h (d	lefault)	Us	er Com	nmand Set (UCS = CMD1)					
D		000)1	0.	1h	Ма	anufactu	ire Com	mand S	Set Page	e0 (CN	ID2 P0)	
Description		001	0	02	2h	Ма	anufactu	ire Com	mand S	Set Page	e1 (CN	ID2 P1)	
		001	1	03	3h	Ma	anufactu	re Com	mand S	Set Page	e2 (CN	ID2 P2)	
		010	00	04	4h	Ma	anufactu	re Com	re Command Set Page3 (CMD2 P3) re Command Set Page4 (CMD2 P4)				
		010)1	0	5h	Ma	anufactu	re Com					
Restriction	-												
				Sta	tus					Availal	oility		
		Nori	mal Mod	e On, Idle	Mode	Off, SI	leep O	ut		Yes	3		
Register		Nori	mal Mod	e On, Idle	Mode	On, SI	leep O	ut		Yes	6		
Availability		Par	tial Mod	e On, Idle	Mode	Off, SI	еер Ои	ıt		Yes	3		
		Par	tial Mod	e On, Idle	Mode	On, Sl	еер Ои	ıt		Yes	6		
				Slee	p In					Yes	3		
1													
		S	tatus					Defa	ult Valu	ne			
								FEh	/ FE00)h			
Default	Po	wer O	n Seque	ence					00h				
		S/W	/ Reset						00h				
		H/W	/ Reset						00h				



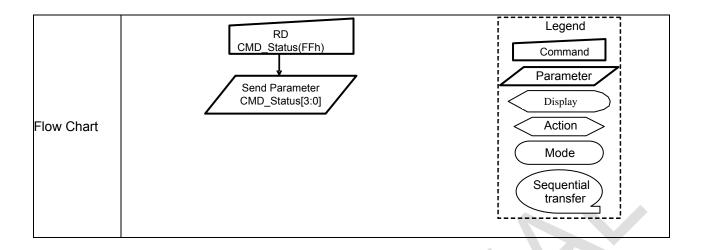




(FF00h): Read CMD Status

FF00H Instruction R/W Addr		MAUCCT	R (Man	ufactu	ire Cor	nmand	Set C	ontrol	\		
Addr		MAUCCTR (Manufacture Command Set Control)									
Instruction R/W	ress					Param	eter			1	
MIPI C	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RD CMD Status R FFh F	FF00h	00h	0	0	0	0	С	MD_St	atus[3:	0]	00
This comman		sed to sw	itch the	Manu	ıfacture	Comn	nand P	ages a	nd Use	er	
Commands	sets.										
CMD_Status	s[3:0]	Hex	Value				Desc	ription			
0000)	00h ((default) U	Iser Con	nmand	Set (UC	S = CM	ID1)		
Description 0001	1	(01h	N	1anufact	ure Cor	mmand	Set Pag	ge0 (CN	MD2 P0)
0010)		02h	M	1anufact	ure Cor	nmand	Set Pag	ge1(CN	MD2 P1)
0011	1		03h	N	1anufact	ure Cor	nmand	Set Pag	ge2(Cl	MD2 P2)
0100	0100 04h Manufacture Command Set Page3 (CMD2 P3))	
0101	0101 05h Manufacture Command Set Page4 (CMD2 P4)										
Restriction -			_ <			<u> </u>					
		Sta	itus					Availat	oility		
Norma	al Mod	e On, Idle	Mode	Off, S	leep Ou	ıt		Yes	8		
Register	al Mod	e On, Idle	Mode	On, S	leep Ou	ıt		Yes	5		
Availability Partia	al Mode	On, Idle	Mode	Off, SI	eep Ou	t		Yes	3		
Partia	al Mode	On, Idle	Mode	On, SI	eep Ou	t		Yes	3		
		Slee	p In					Yes	6		
		ı									
Sta	Status Default Value										
Sta	atus					FFh	/ FF00	h			
Default Power On	Seque	nce					00h				
S/W F	Reset						00h				
H/W F	Reset						00h				







7. Electrical Characteristics

7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM67160 is used out of the absolute maximum ratings, the RM67160 may be permanently damaged. To use the RM67160 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM67160 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ + 5.5	V
Power supply voltage	VDD (VDDA, VDDB, VDDR)	-0.3 ~ + 5.5	V
Owner have the rea (MA) ()	AVDD-AVSS	-0.3 ~ + 6.6	V
Supply voltage (MV)	VCL-AVSS	-0.3 ~ + 6.6	V
Supply voltage (HV)	VGH - VGLX	-0.3 ~ + 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Operating temperature	Topr	-40 ~ + 85	°C
Storage temperature	Tstg	-55 ~ + 125	°C
N	<u> </u>		·

Notes:

If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	Pass 3KV
Machine Mode	R = 0 ohm / C = 200 pF	Pass 300V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.



7.4 DC Characteristics

.1 Basic Characteristics	Symbol	Condition	Min.	Тур.	Max.	Unit	Related Pins
ameter							1113
alog Power Supply Voltage	VDD	Operation Voltage	2.7	2.8	3.6	V	Note 1
pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1,2
——————————————————————————————————————							
ic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 3
ic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 3
ic High level Output voltage	VOH	lout = -1 mA	0.8* VDDI	-	VDDI	V	Note 3
ic Low level Output voltage	VOL	lout = +1 mA	0.0	-	0.2* VDDI	V	Note 3
ic High level input current cept MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
ic Low level input current cept MIPI)	IILD	Vin=0~VDDI	-1	_ <		uA	Note 3
ic High level input current PI)	IIHD	Vin=0~VDDI			1	uA	Note 3
ic Low level input current PI)	IILD	Vin=0~VDDI	-1			uA	Note 3
DD booster voltage	AVDD		4.5		6.5	V	Note 3
booster voltage	VCL		-3.5		-5	V	Note 3
H booster voltage	VGH		AVDD		2AVDD	V	Note 3
L booster voltage	VGL		VCL		VCL -AVDD	V	Note 3
tage difference between VGH and L	VGHL	VGH-VGL			30	٧	Note 3
nma reference voltage	VGMP		2.0		6.0	V	Note 3,4
mma reference voltage	VGSP		0.0		4.5	V	Note 3
<u> </u>	Eosc		20.24	22	23.76	N/IU-	
	1 050	Court > AVDD 1 OV 577	20.24	~~	23.70	IVIFIZ	TBD
annel deviation voltage	V_{DEV}	0V < Sout ≤ 1.0V				mV	
annel deviation voltage	V_{DEV}	1.0V < Sout < AVDD-1.0V				mV	TBD
		1.0V < Sout <	20.24	22	23.	.76	mV

Notes:

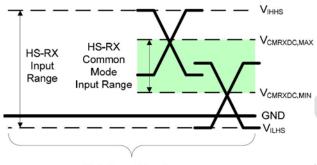
- 1. VDD means VDDA, VDDR, VDDB. And VSS means VSSA, VSSR, VSSB, AVSS, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
- 2. Recommend VDDI=1.8V for power saving.
- 3. Ta(ambient temperature) ranges from -30 $^{\circ}$ C to 85 $^{\circ}$ C.
- 4. VGMP <= AVDD 0.2V



7.5 MIPI Characteristics

7.5.1 High-Speed Receiver Specification

DC Specifications



High Speed Receiver

Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

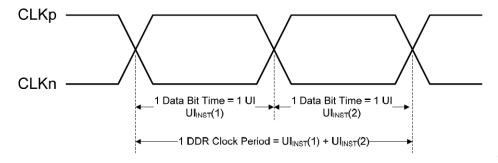
Notes:

- 1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
- 2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz



7.5.2 Forward high speed transmissions

DDR Clock Definition



Clock Parameter	Symbol	Min	Тур	Max	Units	Notes
UI instantaneous	UI _{INST}	2		12.5	ns	1,2

Notes:

- 1. This value corresponds to a minimum 80 Mbps data rate.
- 2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

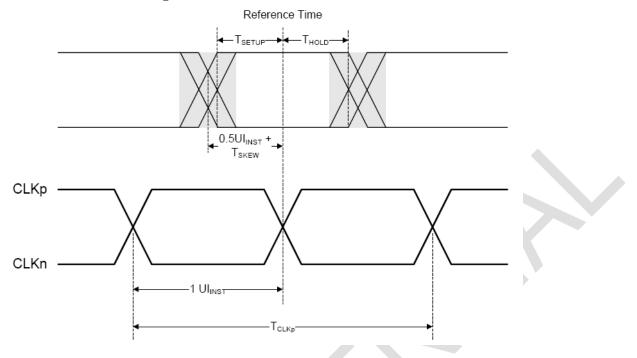
Parameter	Symbol	Min	Тур	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	7000	-0.15		0.15	UI _{INST}	1
Data to Clock Setup Time [receiver]	T _{SETUP[RX]}	0.15			UI _{INST}	2
Clock to Data Hold Time [receiver]	T _{HOLD[RX]}	0.15			UI _{INST}	2

Notes:

- 1. Total silicon and package delay budget of 0.3*UI_{INST}
- 2. Total setup and hold window for receiver of 0.3*UIINST



7.5.3 Data to Clock Timing Definitions





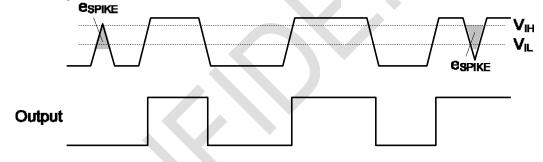
7.5.4 Low power transceiver specifications

Parameters	Symbol	Condition	Min	Тур	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE ^(1.2.3)	Fig. 2	Input pulse rejection			300	V.ps

Notes:

Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State. An impulse less than this will not change the receiver state.

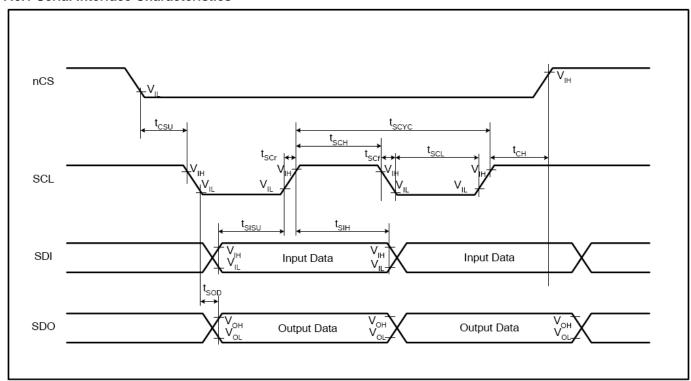
In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers. Input Glitch Rejection of Low Power Receivers as follow.





7.6 AC Characteristics

7.6.1 Serial Interface Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
	T _{SCYC}	Clock cycle (Write)	100		ns	
	T _{SCYC}	Clock cycle (Read)	300		ns	
	T _{SCH}	Clock "H" pulse width (Write)	40		ns	
SCL	T _{SCH}	Clock "H" pulse width (Read)	140		ns	
SCL	T _{SCL}	Clock "L" pulse width (Write)	40		ns	-
	T _{SCL}	Clock "L" pulse width (Read)	140		ns	
	T _{SCr}	Clock rise time		5	ns	
	T_{SCf}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	20		ns	
1103	T _{CH}	Chip select hold time	50		ns	-
SDI	T_{SISU}	Data input setup time	20		ns	
וטט	T _{SIH}	Data input hold time	20		ns	-
SDO	T_{SOD}	Data output setup time		120	ns	
300	T _{SOH}	Data output hold time	5		ns	-

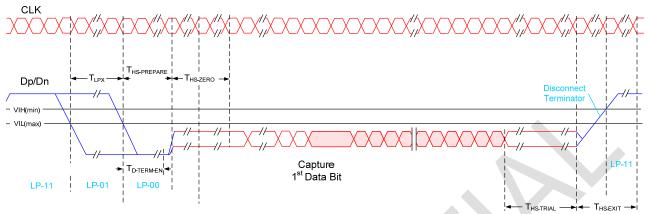
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, GND=0V

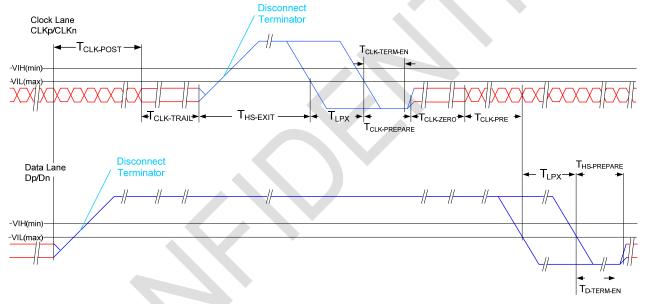


7.6.2 DSI Timing Characteristics

HS Data Transmission Burst



HS clock transmission



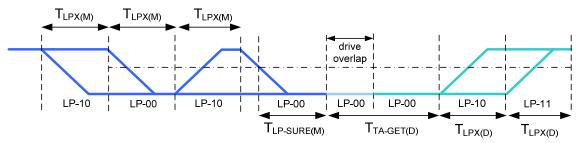


Timing Parameters:

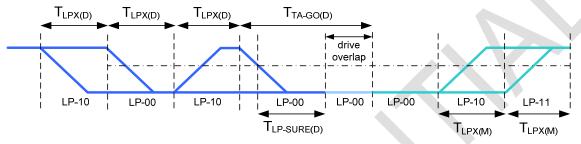
Parameter	Description	Min	Тур	Max	Unit
T _{CLK-POST}	Time that the transmitter continues to send HS clock after the last associated Data	60ns + 52*UI	- 712		ns
	Lane has transitioned to LP Mode. Interval				
	is defined as the period from the end of				
	$T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.				
T _{CLK-TRAIL}	Time that the transmitter drives the HS-0	60			ns
CLK-TRAIL	state after the last payload clock bit of a HS				110
	transmission burst.				
T _{HS-EXIT}	Time that the transmitter drives LP-11	300		_	ns
· H2-EXII	following a HS burst.				110
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable	Time for Dn to		38	ns
· CLK-TERIVI-EIN	the HS line termination, starting from the	reach V _{TERM-EN}		00	
	time point when Dn crosses V _{IL,MAX} .	TERIVI-EN			
T _{CLK-PREPARE}	Time that the transmitter drives the Clock	38		95	ns
- CEN-I NEI ANE	Lane LP-00 Line state immediately before				
	the HS-0 Line state starting the HS				
	transmission.				
T _{CLK-PRE}	Time that the HS clock shall be driven by	8			UI
OLICTIC	the transmitter prior to any associated Data				
	Lane beginning the transition from LP to				
	HS mode.				
T _{CLK-PREPARE}	T _{CLK-PREPARE} + time that the transmitter	300			ns
+ T _{CLK-ZERO}	drives the HS-0 state prior to starting the				
	Clock.				
T _{D-TERM-EN}	Time for the Data Lane receiver to enable	Time for Dn to		35 ns +4*UI	
	the HS line termination, starting from the	reach V _{TERM-EN}			
	time point when Dn crosses V _{IL,MAX} .				
T _{HS-PREPARE}	Time that the transmitter drives the Data	40ns + 4*UI		85 ns + 6*UI	ns
	Lane LP-00 Line state immediately before				
	the HS-0 Line state starting the HS				
	transmission				
T _{HS-PREPARE}	T _{HS-PREPARE} + time that the transmitter	145ns + 10*UI			ns
+ T _{HS-ZERO}	drives the HS-0 state prior to				
	transmitting the Sync sequence.				
T _{HS-TRAIL}	Time that the transmitter drives the flipped	60ns + 4*UI			ns
	differential state after last payload data bit				
	of a HS transmission burst				



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode:

Parameter	Description	Min	Тур	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA\text{-SURE}(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{LPX(M)}		2*T _{LPX(M)}	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA\text{-}GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*T _{LPX(D)}		ns	2
$T_{TA\text{-}GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*T _{LPX(D)}		ns	2
T _{TA-SURE(D)}	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{LPX(D)}		2*T _{LPX(D)}	ns	2

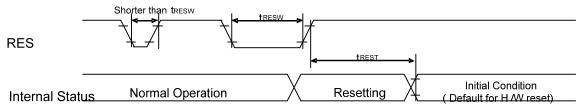
NOTE:

2. Transmitter-specific parameter

^{1.} T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.



7.6.3 Reset Timing



Reset input timing:

VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

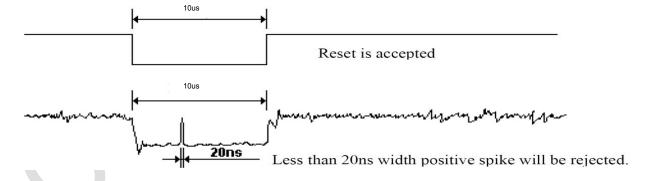
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t _{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μS
t _{REST} *2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms	
	-		-	120	When reset applied during Sleep out mode	ms	

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX. Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

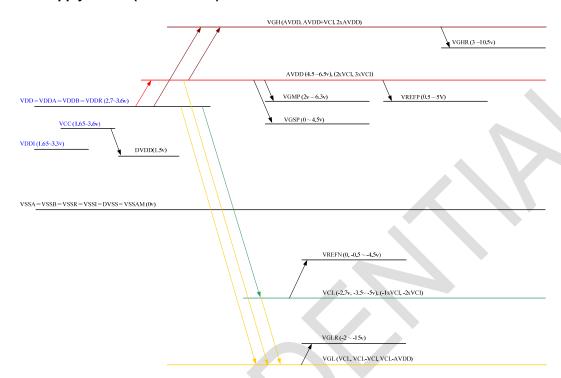


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



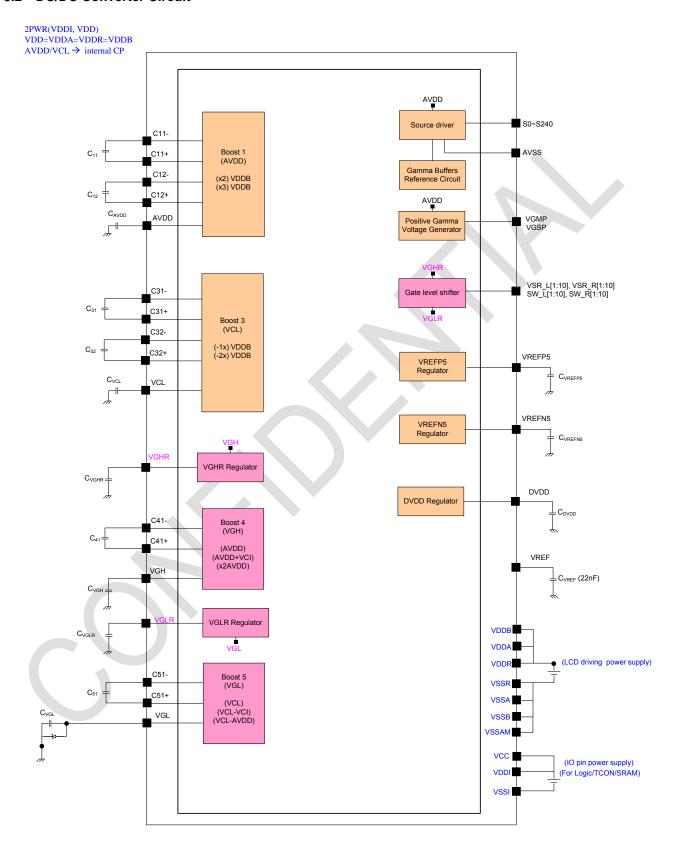
8. Power Generation

8.1 2 Supply Power (VDDI/VDD)





8.2 DC/DC Converter Circuit





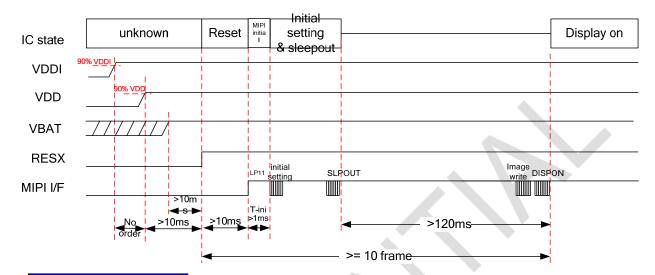
8.3 External Components

No.	Signal name	Values	Max ability
1	VDDA, VDDR, VDDB	Cap , 2.2uF	6.3V
2	VDDI, VCC	Cap , 2.2uF	6.3V
3	VREF	Cap , 22nF	6.3V
4	DVDD	Cap , 1.0uF	6.3V
5	VREFN5/VREFP5	Cap , 1.0uF	6.3V
6	VGHR	Cap , 1.0uF	16V
7	VGLR	Cap , 1.0uF	16V
8	BVP3D	Cap , 2.2uF	10V
9	BVN3D	Cap , 2.2uF	10V
10	C11P/C11N	Cap , 1.0uF	6.3V
11	C12P/C12N	Cap , 1.0uF	6.3V
12	AVDD	Cap , 2.2uF	10V
13	C31P/C31N	Cap , 1.0uF	6.3V
14	C32P/C32N	Cap , 1.0uF	6.3V
15	VCL	Cap , 2.2uF	6.3V
16	C41P/C41N	Cap , 1.0uF	16V
17	VGH	Cap , 2.2uF	25V
18	C51P/C51N	Cap , 1.0uF	16V
19	VGL	Cap , 2.2uF	25V
20	VGL (VGL-GND)	Schottky Diode	

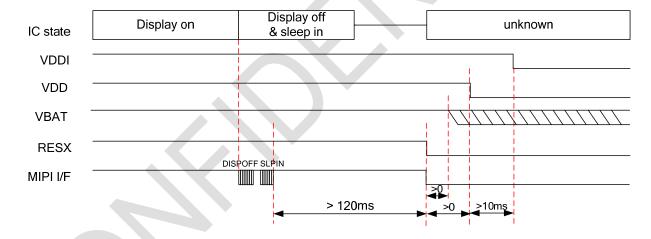


8.4 Power on/off sequence and timing

Power On sequence



Power Off sequence





8.5 Power Level Modes

Normal display mode on = NORON Partial mode on = PTLON Idle mode off = IDMOFF Idle mode on = IDMON Sleep out = SLPOUT Sleep in = SLPIN Deep standby mode = DSTBON

Definition example:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.

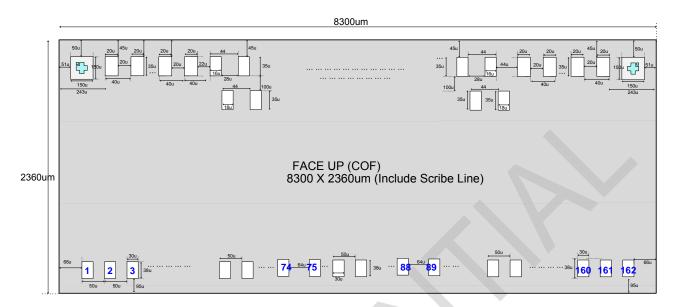
7. Power Off Mode

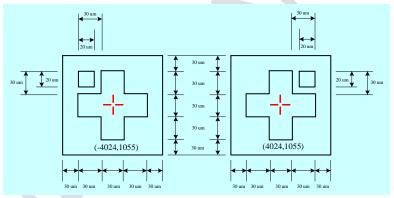
In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.



9. Pad Diagram and Coordination





■ Chip size: 8300 um x 2360um (Include sealing and scribe line)

Chip thickness: 200/300 um
 PAD coordinates: PAD center
 PAD coordinates origin: Chip center

Au bump size

17um x 35um: Source:S0~S240
 20um x 35um: gate control signal

3. 30um x 38um: Input Pads

Au bump pitch: See PAD coordinates table

■ Au bump height: 12±2 um (typ.)

No. in the figure corresponds to No. in the PAD coordinates table

Alignment mark

Alignment mark shape	Х	Υ
left	4024	1055
right	-4024	1055



■ Pad Coordinate (Unit: um)

_	Fau Coordii
NO.	PAD NAME
1	ANALOG_TEST1
2	VGLR
3	VGLR
4	VGHR
5	VGHR
6	VREFP5
7	VREFP5
8	VREFP5
9	VREFN5
10	VREFN5
11	VREFN5
12	BVP3D
13	BVP3D
14	BVN3D
15	BVN3D
16	VCL
17	VCL
18	AVDD
19	AVDD
20	VREF
21	VGSP
22	VGMP
23	DUMMY
24	ANALOG_TEST2
25	VDDR
26	VDDR
27	VDDA
28	VDDA
29	AVSS
30	AVSS
31	AVSS
32	VSSR
33	VSSR
34	VSSR
35	TE1
36	SWIRE
37	OLED_EN
38	TE
39	RESX
40	SDO
41	VSSI
42	SDI_RDX
43	DCX
44	WRX_SCL
45	CSX
46	D[0]
47	VSSI
48	D[1]
49	D[2]
50	D[3]
50	רוסו

_,	5	
51	D[4]	
52	D[5]	
53	VSSI	
54	D[6]	
55	D[7]	
56	TEST1	
57	EXTCLK	
58	TEST2	
59	VSSI	
60	TEST3	
61	IM1	
62	IM0	
63	DSWAP	
64	TESTEN	
65	PSWAP	
66	BSTM	
67	VDDI	
68	VDDI	
69	VCC	
70	VCC	
71	DVDD	
72	DVDD	
73	DVSS	
74	DVSS	
75	HSSI_D1_P	
76	HSSI_D1_P	
77	HSSI_D1_N	
78	HSSI_D1_N	
79	VSSAM	
80	HSSI_CLK_P	
81	HSSI_CLK_P	
82	HSSI_CLK_N	
83	HSSI_CLK_N	
84	VSSAM	
85	HSSI_D0_P	
86	HSSI_D0_P	
87	HSSI_D0_N	
88	HSSI_D0_N	
89	VSSR	
90	VSSR	
91	VSSA	
92	VSSA	
93	AVSS	
94	AVSS	
95	VSSB	
96	VSSB	
97	VSSB	
98	C11P	
99	C11P	
100	C11P	
. 30	.	

101 C11N 102 C11N 103 C11N 104 C12P 105 C12P 106 C12P 107 C12N 108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P <	
103 C11N 104 C12P 105 C12P 106 C12P 107 C12N 108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
104 C12P 105 C12P 106 C12P 107 C12N 108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
105 C12P 106 C12P 107 C12N 108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
106 C12P 107 C12N 108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
107 C12N 108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
108 C12N 109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
109 C12N 110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
110 VDDB 111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
111 VDDB 112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
112 VDDB 113 VDDR 114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
113 VDDR 114 VDDR 115 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	4
114 VDDR 115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	4
115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
115 VDDR 116 AVDD 117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
117 AVDD 118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
118 AVDD 119 C31P 120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
119 C31P 120 C31P 121 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	7
120 C31P 121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
121 C31P 122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
122 C31N 123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
123 C31N 124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	7
124 C31N 125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
125 VCL 126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
126 VCL 127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
127 VCL 128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
128 C32P 129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
129 C32P 130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
130 C32P 131 C32N 132 C32N 133 C32N 134 C41P	
131 C32N 132 C32N 133 C32N 134 C41P	
132 C32N 133 C32N 134 C41P	
133 C32N 134 C41P	
134 C41P	
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137 C41N	
138 C51N	
139 C51N	
140 C51P	
141 C51P	
142 VGH	
143 VGH	
144 VGHR	
145 VGHR	
146 VGHR	
146 VGHR 147 VGHR	
147 VGHR 148 VGHR	
146 VGHR 149 VGLR	
150 VGLR	
150 VGLR	

151	VGL
152	VGL
153	AVSS
154	AVSS
155	AVSS
156	MTP_PWR
157	MTP_PWR
158	MTP_PWR
159	MTP_PWR
160	MTP_PWR
161	MTP_PWR
162	DUMMY
163	VGLR
164	VGHR
165	VREFP5
166	VREFN5
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168	VSR_L[9]
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172	VSR_L[5]
173	VSR_L[4]
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175	VSR_L[2]
176	VSR_L[1]
177	SW_L[1]
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179	SW_L[3]
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277	Allegania
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449	S5
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454	SDMY
455	SW_R[10]
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458	SW_R[7]
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463	SW_R[2]
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472	VSR_R[8]
473	VSR_R[9]
474	VSR_R[10]
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476	VREFP5
477	VGHR
478	VGLR