OSD DISPLAYS

135 W. Central Blvd., Suite 330
Orlando, FL 32801
Phone: 407-629-0500
Fax: 407-645-5376
sales@osddisplays.com
www.osddisplays.com

Customer:	
Model Number:	OSD015A2637-21TS
Specification Number:	
Date:	9/13/2016
Version:	A.2

For Customer's Acceptance

Approved by	Comments

Approved by	Reviewed by	Prepared by

Table of Contents

Record of Revision

Rev	Issue Date	Description	Editor
A0	2015-11-2	Draft	Huang Saibo
A1	2016-06-26	Update Current Consumption ,Initial Code and Mechanical Drawing	Huang Saibo
A2	2016-09-13	Update Mechanical Drawing	Huang Saibo

1 General Specifications

Feature		Spec	Remark
Display Spec	Screen Size (inch)	1.45	
	Display Mode	AMOLED	
	Resolution(dot)	272 (W) x RGB x 340(H)	
	Active Area(mm)	23.01 (W)×28.77 (H)	
	Pixel Pitch (um)	84.60 (W) x 84.60 (H)	
	Pixel Configuration	V-Style3	
	Technology Type	LTPS	
	Color Depth	16.7M	
	Interface	MIPI 1LANE	
	Surface Treatment	Hard Coating	
Mechanical Characteristics	With TP/Without TP	With TP(on Cell)	
	Module Outline Dimension(W x H x D) (mm)	26.01(W)x33.77(H)x0.833 (D)	Without metal frame
	Weight (g)	TBD	
Electronic	Driver IC(Type)	RM67160	
	TP IC(Type)	FT3207	

Note 1: Requirements on Environmental Protection: RoHS.

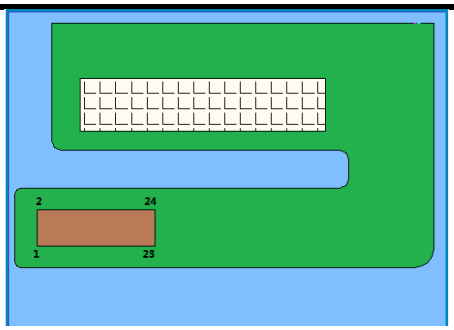
2 Input/output Terminals

2.1 Main FPC Pin Assignment-AMOLED Panel Input / Output Signal Interface

FPC connector: 504248-2410 (Molex)

Main board recommended connector: 504208-2410 (Molex)

No	Symbol	I/O	Description
1	GND	GND	Ground
2	XRES	I	Device reset signal(0:Enable;1:Disable)
3	DSI_D0N	I/O	MIPI negative data signal
4	SWIRE	O	SWIRE signal for PWR IC control
5	DSI_D0P	I/O	MIPI positive data signal
6	OTP	power	7.5 V, OTP function Pin. Leave this pin OPEN if it is not used.
7	GND	GND	Ground
8	TE	O	Vsync(vertical sync)signal output from panel to avoid tearing effect
9	DSI_CLKN	I	MIPI negative clock signal
10	GND	GND	Ground
11	DSI_CLKP	I	MIPI positive clock signal
12	GND	GND	Ground
13	GND	GND	Ground
14	GND	GND	Ground
15	VDDIO	Power	Power supply for Interface system except MIPI interface
16	VCI	Power	Driver analog power supply
17	GND	GND	Ground
18	GND	GND	Ground
19	ELVSS	Power	AMOLED negative power supply
20	ELVDD	Power	AMOLED positive power supply
21	ELVSS	Power	AMOLED negative power supply
22	ELVDD	Power	AMOLED positive power supply
23	ELVSS	Power	AMOLED negative power supply
24	ELVDD	Power	AMOLED positive power supply

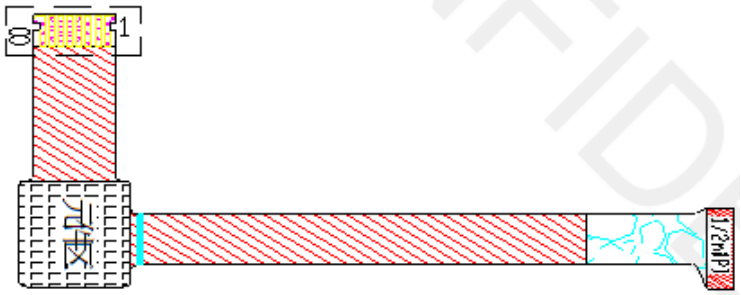


Pin layout of B-to-B contact pads

Note: I=Input; O=Output; P=Power; I/O=Input / Output

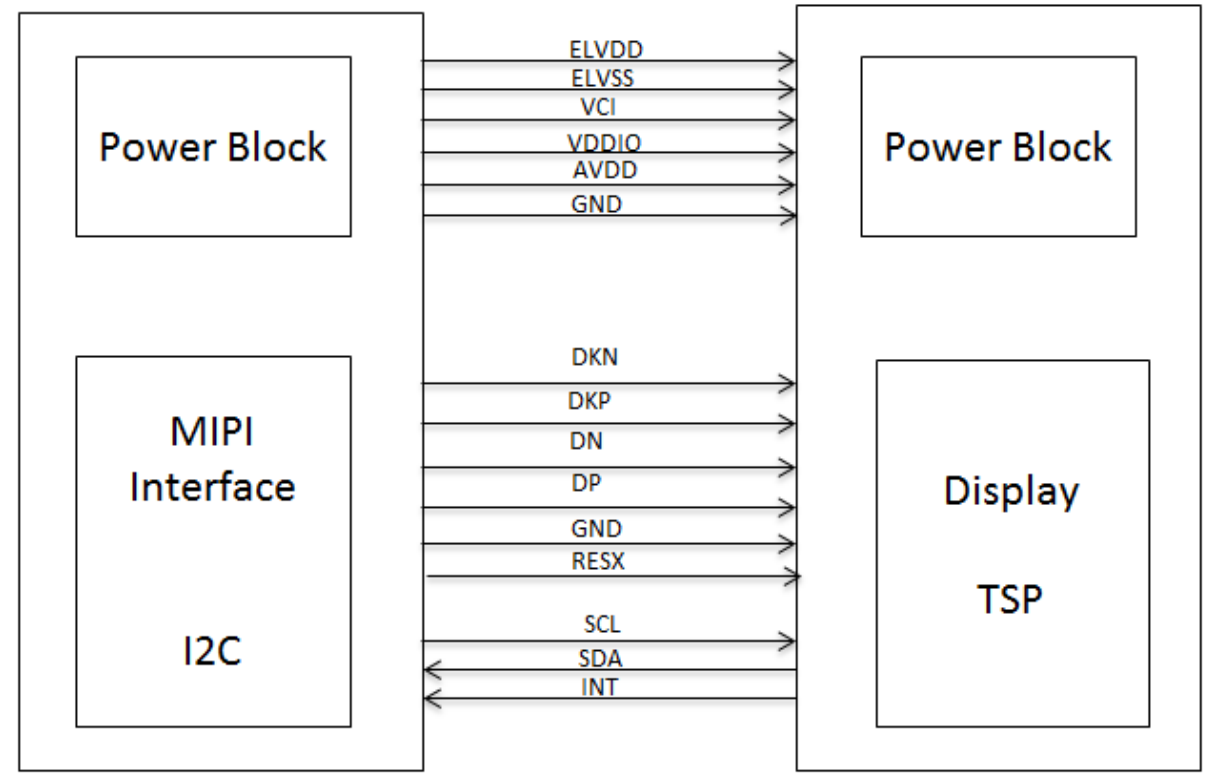
2.2 TP FPC Pin Assignment-On-cell TP Input / Output Signal Interface

No	Symbol	I/O	Description
1	GND	GND	Ground
2	INT	I/O	External interrupt to the host
3	RSTN	I	External Reset, Low is active
4	SCL	I/O	I2C clock input
5	SDA	I/O	I2C data input and output
6	GND	GND	Ground
7	NC	-	Not Connected
8	AVDD	Power	TP power supply input.



TP main board recommended connector: 04 6298 008 100 883+

2.3 System BD and Display Module Interface Conflagration



3 Absolute Maximum Ratings

3.1 Driving AMOLED Panel

Maximum Ratings (Voltage Referenced to VSS) Vss=0V, Ta=25°C

Item	Symbol	MIN	MAX	Unit	Remark
Input Voltage	VCI	-0.3	+5.5	V	
Digital Power supply	VDDIO	-0.3	+5.5	V	
Positive Power Input	ELVDD	-	+5.0	V	
Negative Power Input	ELVSS	-5.0	-	V	
TP power supply Input	AVDD	-0.3	+3.6	V	

Note: Functional operation should satisfy the limits in the Electrical Characteristics tables or Pin Description section. If the module exceeds the absolute maximum ratings, permanent damage may occur. Besides, if the module is operated with the absolute maximum ratings for a long time, the reliability may also drop.

4 Electrical Characteristics

4.1 Driving AMOLED Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Input Digital Supply Voltage		VDDIO	1.65	1.80	3.30	V	Note1、Note2
Analog Supply Voltage		VCI	2.70	2.80	3.60	V	
ELVDD Supply Voltage		ELVDD	4.55	4.60	4.65	V	
ELVSS Supply Voltage		ELVSS	-2.46	-2.4	-2.34	V	
TP power supply Input		AVDD	2.8	2.8	3.6	V	
Input Signal Voltage	High Level	VIH	0.80*VDDIO	-	VDDIO	V	
	Low Level	VIL	0.00	-	0.20*VDDIO	V	
Output Signal Voltage	High Level	VOH	0.80*VDDIO	-	VDDIO	V	
	Low Level	VOL	0.00	-	0.20*VDDIO	V	

Note1: The input digital voltage is the I/O reference voltage.

Note2: VDDIO usually ranges from 1.65V to 1.95 V. If VDDIO is changed, the remaining voltage needs to be changed to the same voltage as VDDIO.

4.2 Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD=4.6V	-	129	143	mW	Note1
		I_{NL}	ELVSS=-2.4V	-	15	17	mA	Note1
IC	**Normal**	I_{VCI}	VCI=2.8V	-	6	-	mA	-
		I_{IOVCC}	VDDIO=1.8V	-	4	-	mA	-
	Stand-by	I_{VCI}	VCI=2.8V	-	4.5	-	uA	-
		I_{IOVCC}	VDDIO=1.8V	-	7	-	uA	-

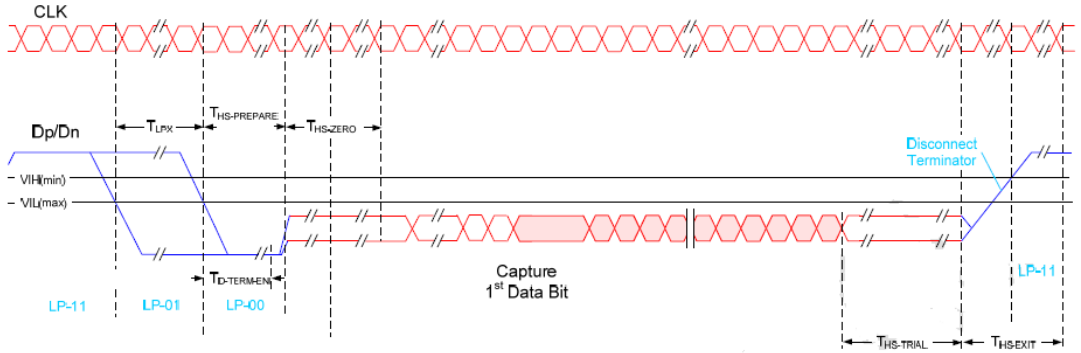
Note1: Based on L255 (350nits) full white pattern.

Note2: Based on white pattern. MIPI-DSI frame 60Hz.

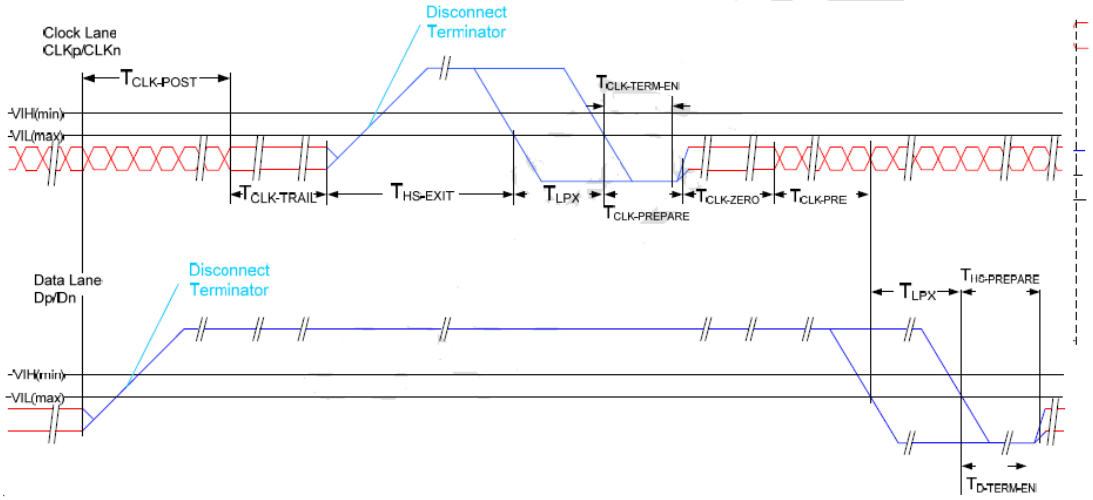
5 AC Characteristics

5.1 MIPI Interface Characteristics

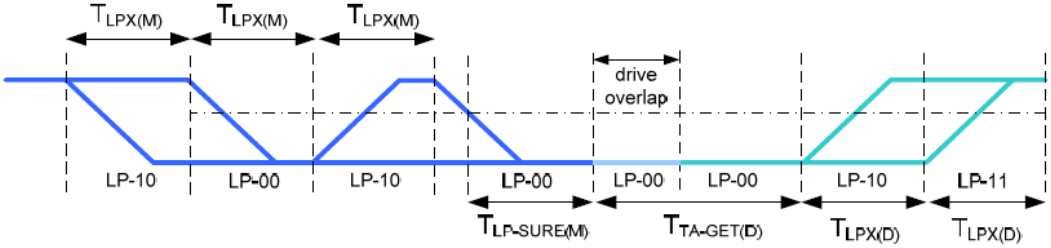
HS Data Transmission Burst



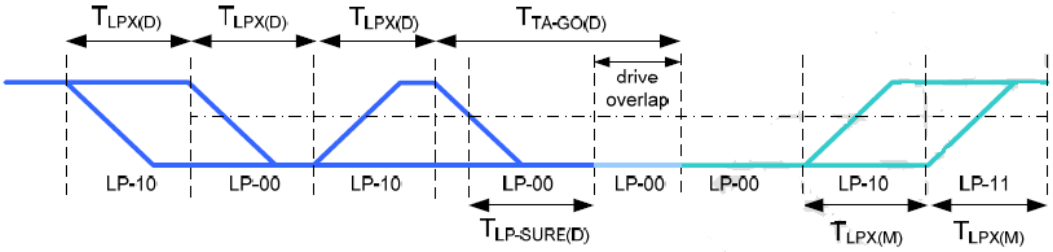
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



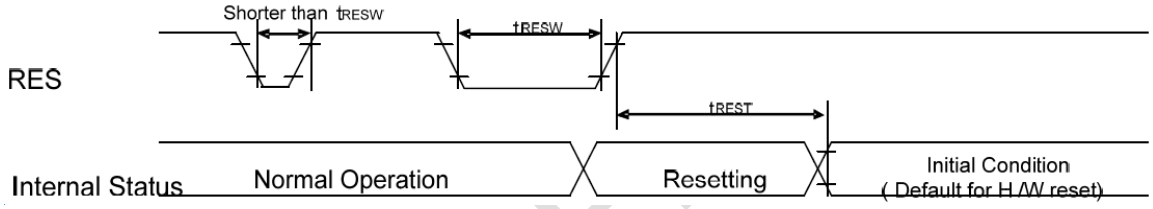
Timing Parameters：

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

5.2 Display RESET Timing Characteristics

Reset input timing:



VDDIO=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Timing Parameters:

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1. Spike caused by an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

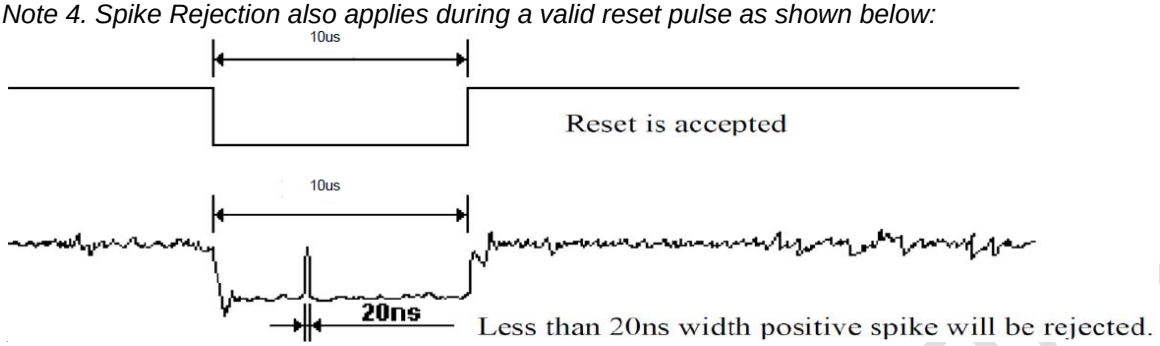
RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blank (The display is entering blanking sequence, whose maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains blank in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge

of RESX.

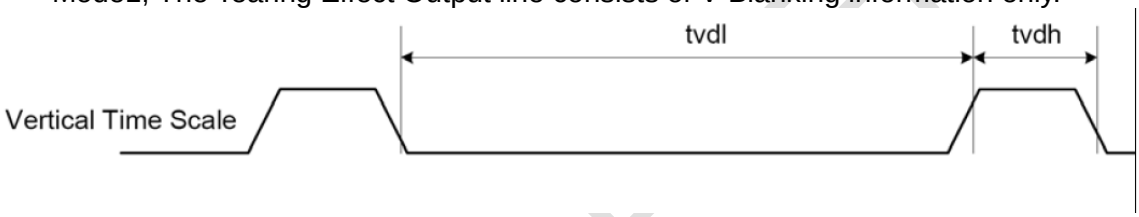
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.3 TE Timing Characteristics

Mode1, The Tearing Effect Output line consists of V-Blanking information only.

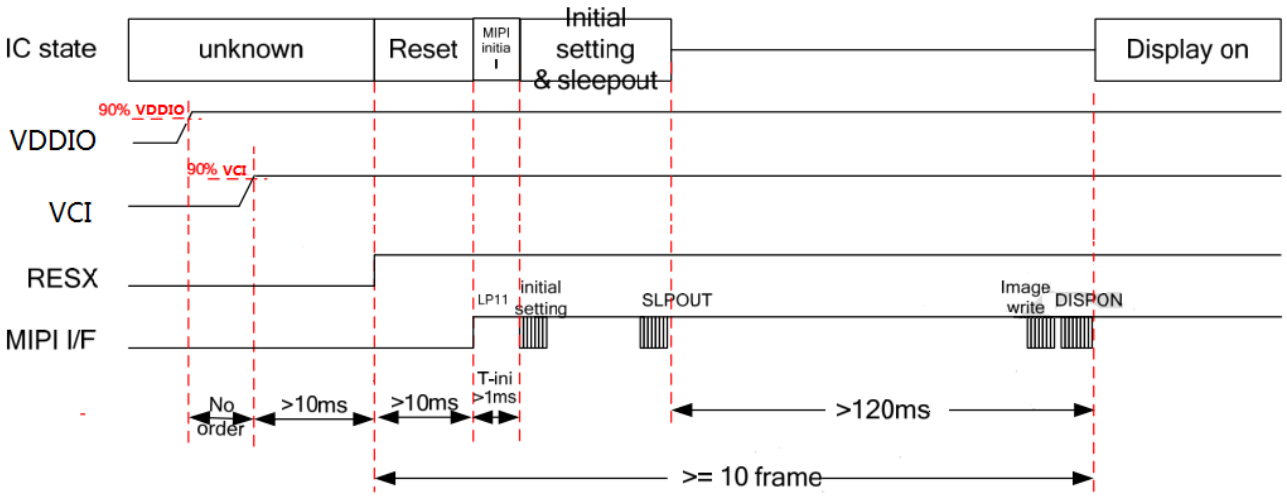


Tvdh = The LCD display is not updated from the frame memory.
Tvdl = The LCD display is updated from the frame memory.

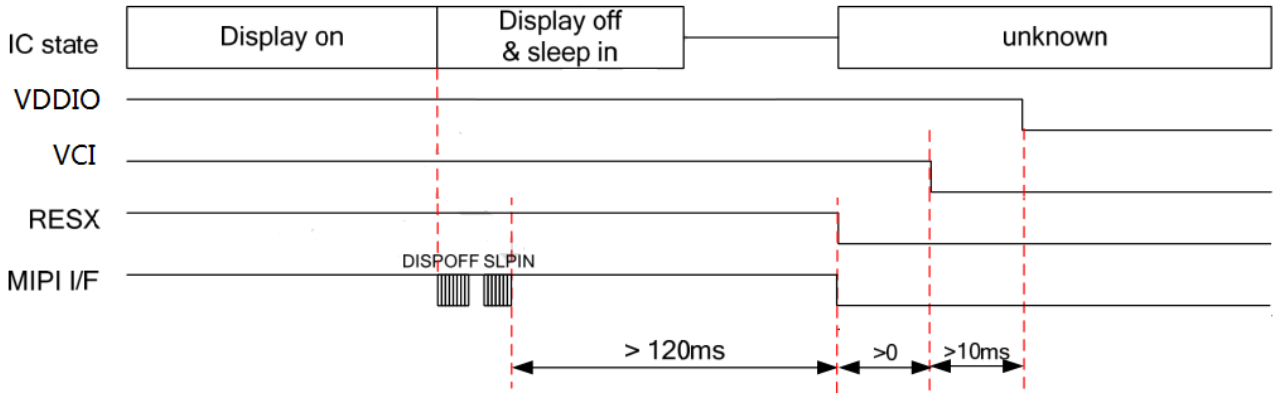
6 Recommended Operating Sequence

6.1 Display Power on / off Sequence

6.1.1 Power On Sequence



6.1.2 Power Off Sequence



6.2 Display Initial code

step	Instruction/ Parameter	Delay times	R/W	mipi data type	address		data
					mipi	others	
1	IC frame rate control		w	0x39	0xFE	0xFE40	0x01
					0x05	0x0540	0x40
					0x06	0x0640	0x55
					0x10	0x1040	0x71
					0x0E	0x0E40	0x80
					0x0F	0x0F40	0x80
					0x19	0x1940	0x55

					0x18	0x1840	0x88
					0x1A	0x1A40	0x10
					0x1C	0x1C40	0x77
					0x1D	0x1D40	0x03
					0x23	0x2340	0x21
					0x21	0x2140	0x40
					0x22	0x2240	0xb7
					0x25	0x2540	0x05
					0x26	0x2640	0xFC
					0x2A	0x2A40	0x25
					0x2B	0x2B40	0xFC
					0x70	0x7040	0xFF
2	VSR Command		w	0x39	0xFE	0xFE70	0x04
					0x5D	0x5D70	0x10
					0x5A	0x5A70	0xFF
3	VSR1 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x00	0x0070	0xCC
					0x01	0x0170	0x00
					0x02	0x0270	0x02
					0x03	0x0370	0x00
					0x04	0x0470	0xA8
					0x05	0x0570	0x01
					0x06	0x0670	0x8E
					0x07	0x0770	0xFC
					0x08	0x0870	0x05
4	VSR2 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x09	0x0970	0xCC
					0x0A	0x0A70	0x00
					0x0B	0x0B70	0x04
					0x0C	0x0C70	0x00
					0x0D	0x0D70	0x80
					0x0E	0x0E70	0x02
					0x0F	0x0F70	0x01
					0x10	0x1070	0x00
					0x11	0x1170	0x05
5	VSR3 Timing Set		w	0x39	0xFE	0xFE70	0x04

					0x12	0x1270	0x8C
					0x13	0x1370	0x00
					0x14	0x1470	0x02
					0x15	0x1570	0x01
					0x16	0x1670	0x08
					0x17	0x1770	0x00
					0x18	0x1870	0x8E
					0x19	0x1970	0x36
					0x1A	0x1A70	0x05
6	VSR4 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x1B	0x1B70	0xCC
					0x1C	0x1C70	0x00
					0x1D	0x1D70	0x02
					0x1E	0x1E70	0x00
					0x1F	0x1F70	0x08
					0x20	0x2070	0x00
					0x21	0x2170	0x8E
					0x22	0x2270	0x00
					0x23	0x2370	0x05
7	VSR5 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x24	0x2470	0xCC
					0x25	0x2570	0x00
					0x26	0x2670	0x02
					0x27	0x2770	0x00
					0x28	0x2870	0x08
					0x29	0x2970	0x01
					0x2A	0x2A70	0x8E
					0x2B	0x2B70	0x42
					0x2D	0x2D70	0x05
8	VSR6 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x2F	0x2F70	0x8C
					0x30	0x3070	0x00
					0x31	0x3170	0x01
					0x32	0x3270	0x03
					0x33	0x3370	0x00
					0x34	0x3470	0x00

					0x35	0x3570	0x01
					0x36	0x3670	0x43
					0x37	0x3770	0x05
9	VSR7 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x38	0x3870	0xCC
					0x39	0x3970	0x00
					0x3A	0x3A70	0x02
					0x3B	0x3B70	0x00
					0x3D	0x3D70	0x20
					0x3F	0x3F70	0x01
					0x40	0x4070	0xA4
					0x41	0x4170	0x57
					0x42	0x4270	0x05
10	VSR8 Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x43	0x4370	0xCC
					0x44	0x4470	0x00
					0x45	0x4570	0x04
					0x46	0x4670	0x00
					0x47	0x4770	0x00
					0x48	0x4870	0x00
					0x49	0x4970	0x01
					0x4A	0x4A70	0x00
					0x4B	0x4B70	0x05
11	VSR Timing Set		w	0x39	0xFE	0xFE70	0x04
					0x4C	0x4C70	0x88
					0x4D	0x4D70	0x00
					0x4E	0x4E70	0x01
					0x4F	0x4F70	0x08
					0x50	0x5070	0x01
					0x51	0x5170	0x8E
					0x52	0x5270	0x36
12	Mux SWitch Timing command		w	0x39	0xFE	0xFE40	0x01
					0x3A	0x3A40	0x00
					0x3B	0x3B40	0x00
					0x3D	0x3D40	0x10
					0x3F	0x3F40	0x2F

					0x40	0x4040	0x10
					0x41	0x4140	0x0A
					0x37	0x4240	0x10
13	VSR Marping command		w	0x39	0xFE	0xFE70	0x04
					0x5E	0x5E70	0x30
					0x5F	0x5F70	0x32
					0x60	0x6070	0x84
					0x61	0x6170	0x76
					0x62	0x6270	0x51
14	ELVSS VOLTAGE SET		w	0x39	0xFE	0xFE80	0x05
					0x05	0x5E80	0x17
					0x2A	0x5F80	0x00
					0x91	0x6080	0x00
15	SW Mapping		w	0x39	0xFE	0xFE40	0x01
					0x42	0x4240	0x33
					0x43	0x4340	0x22
					0x44	0x4440	0x11
					0x45	0x4540	0x66
					0x46	0x4640	0x55
					0x47	0x4740	0x44
					0x4C	0x4C40	0x33
					0x4D	0x4D40	0x22
					0x4E	0x4E40	0x11
					0x4F	0x4F40	0x66
					0x50	0x5040	0x55
					0x51	0x5140	0x44
					0x56	0x5640	0x11
					0x58	0x5840	0x22
					0x59	0x5940	0x33
					0x5A	0x5A40	0x44
					0x5B	0x5B40	0x55
					0x5C	0x5C40	0x66
					0x61	0x6140	0x11
					0x62	0x6240	0x22
					0x63	0x6340	0x33
					0x64	0x6440	0x44

					0x65	0x6540	0x55
					0x66	0x6640	0x66
16			w	0x39	0xFE	0xFE00	0x00
					0x35	0x3500	0x00
17	sleep out		w	0x39	0x11	0x1100	
18	delay(ms)	120					
19	display on		w	0x39	0x29	0x2900	

Send format: send cmd , data.
Example:
send 0xFE,0x04
0x4C,0x88

address		data
mipi	other	
0xFE	0xFE70	0x04
0x4C	0x4C70	0x88

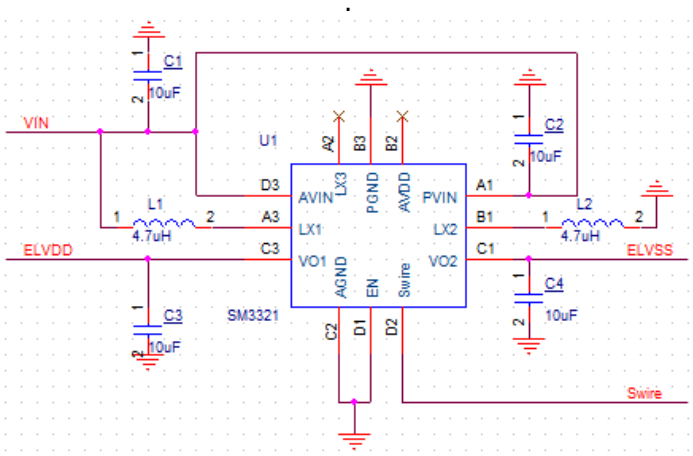
6.3 Brightness control

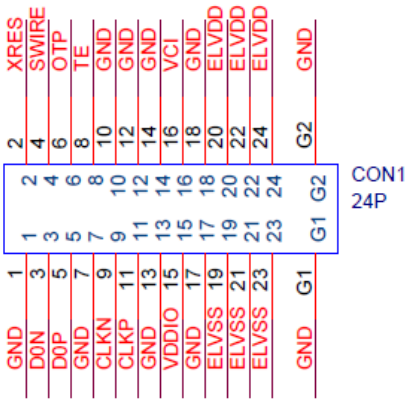
Inst/Para	R/W	Address		Date Type	Description
		MIPI	Other		
BRTCTRL	W	51h	5100h	Hex	Value form 0~255(FF)

Note: 00h value means the lowest brightness and FFh value means the highest brightness

7 Application Circuit

ELVDD & ELVSS power supply schematic, The Triple DC/DC converter SM3321 is recommended. The application schematics and external components are as below.





Component	Part Number	Specification	Quantity	Manufacturer
Capacitance	LMK105CBJ106MVLF	10uF/10V X5R 0402 ±20%	4	TAIYO YUDEN
	CL05A106MP5NUNC			Samsung
Inductance	KMNR201610-4R7M-S-Z	4.7uH±20% 444mΩ 0.76A	2	Ke ming
	ACPI201610PF-4R7MT			Amode

Note：Main board recommended connector, 504208-2410 (Molex).

8 Optical Characteristics Optical Specification

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angle		θT	CR≥10	80			Degree	Note 2 Test Equipment：CS2000A
		θB		80				
		θL		80				
		θR		80				
Contrast Ratio		CR	θ=0°	10000				Note1 Note3 Test Equipment：CS2000A
Response Time		T_{ON}	25℃			4	ms	Note1 Note4 Test Equipment：Admesy MSE
		T_{OFF}						
Chromaticity	White	x		(0.292)	(0.312)	(0.332)		Test Equipment：CS2000A Note: Chromaticity can be modified according to customer demand
		y		(0.309)	(0.329)	(0.349)		
	Red	x		(0.624)	(0.664)	(0.704)		
		y		(0.305)	(0.335)	(0.365)		
	Green	x		(0.200)	(0.250)	(0.300)		
		y		(0.656)	(0.706)	(0.756)		
	Blue	x		(0.097)	(0.137)	(0.177)		
		y		(0.015)	(0.055)	(0.095)		
Uniformity		U		75			%	Note1 Note6 luminance of center point is 350±35nits Test Equipment：CS2000A
NTSC				85	100		%	Note5
Luminance		L		315	350	385	Cd/m^2	Note1 Note7 Test Equipment：CS2000A
Cross-talk						3	%	Note8 L≤350nits Test Equipment：

							CS2000A
Gamma			1.9	2.2	2.5		Gamma=2.2±0.3（L≤350nits）； Gamma Self-adjustment (L＞350nits) Test Equipment：CS2000A

Test Conditions:

1. the ambient temperature is 25℃.
2. The test systems refer to Note1 and Note2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the AMOLED screen. All input terminals AMOLED panel must be ground when measuring the center area of the panel.

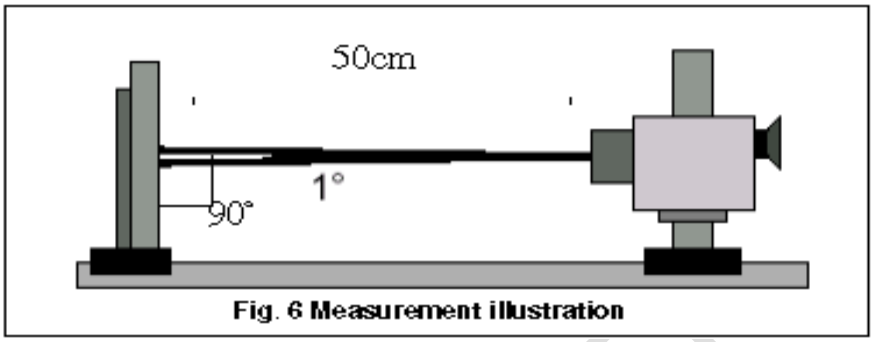


Fig. 6 Measurement illustration

Note 2: Definition of viewing angle range and measurement system.

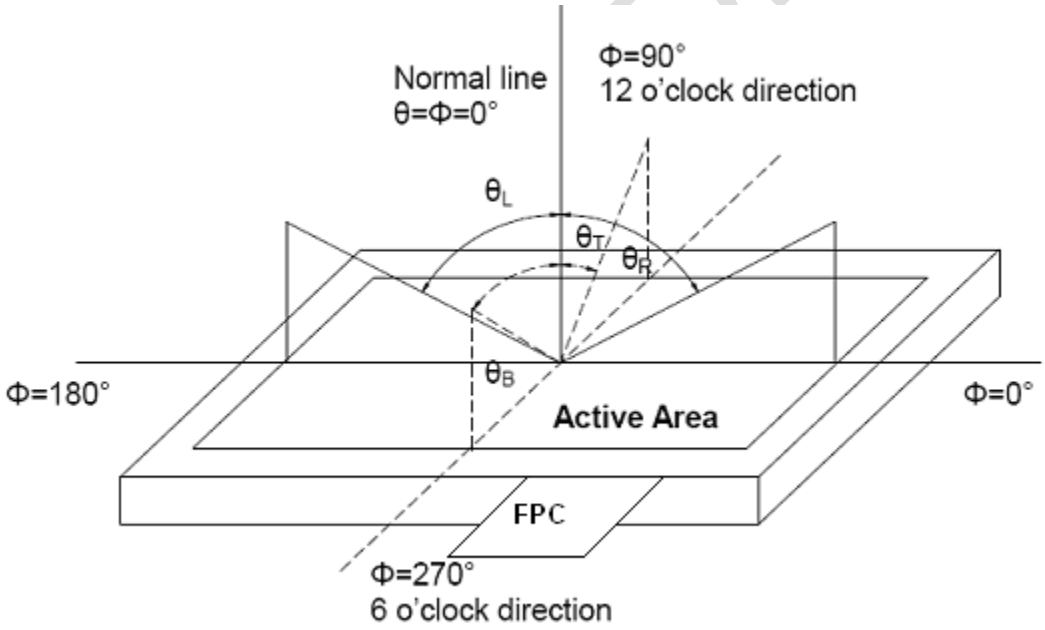


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

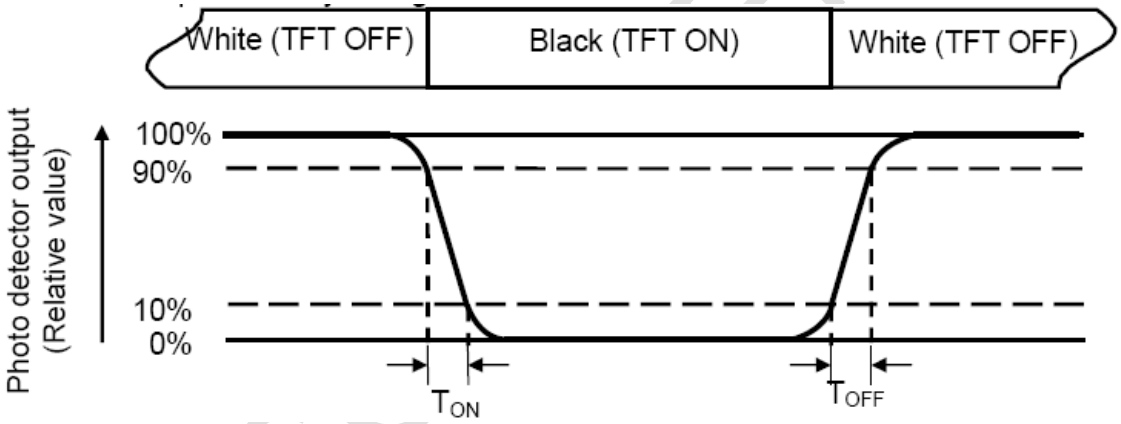
$$\text{Contrast ratio(CR)} \quad \frac{\text{Luminance measured when LCD is on the "white" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “: A state where the AMOLED should be driven by Vwhite.

“Black state”: A state where the AMOLED should be driven by Vblack.

Note 4: Definition of response time

The response time is defined as the AMOLED optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of AMOLED.

Note 6: Definition of luminance uniformity

Active area is divided into 5 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

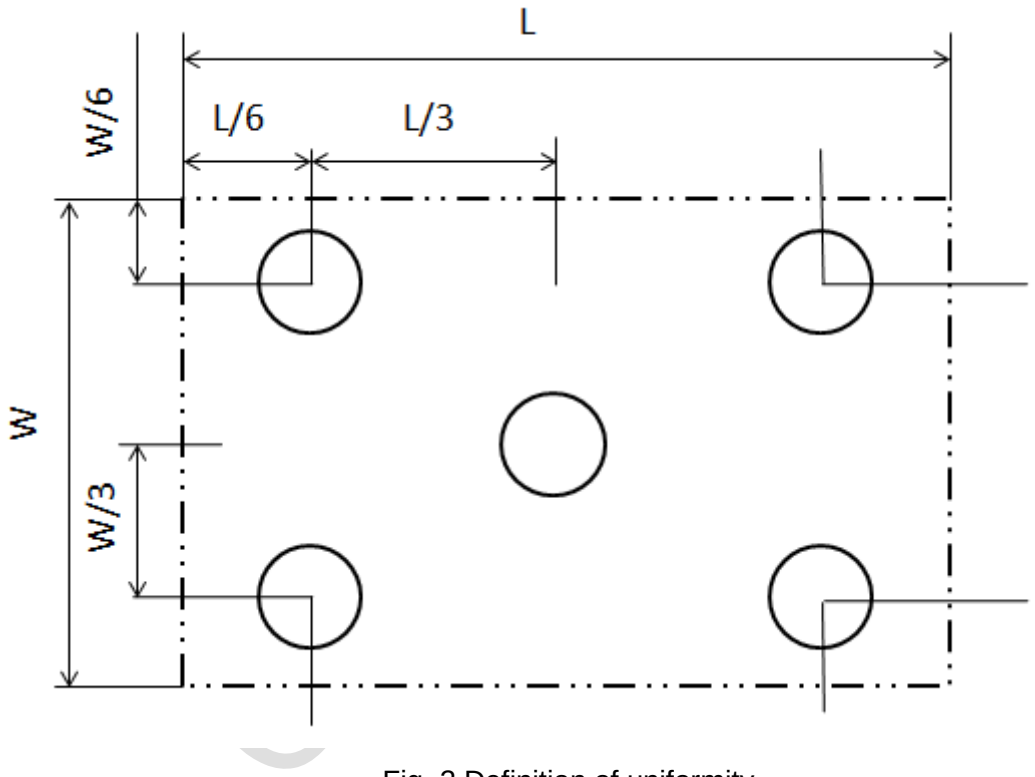


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of luminance:

Measure the luminance of white state at center point.

Note 8: Cross Talk

A. Measure luminance at the position, P0.

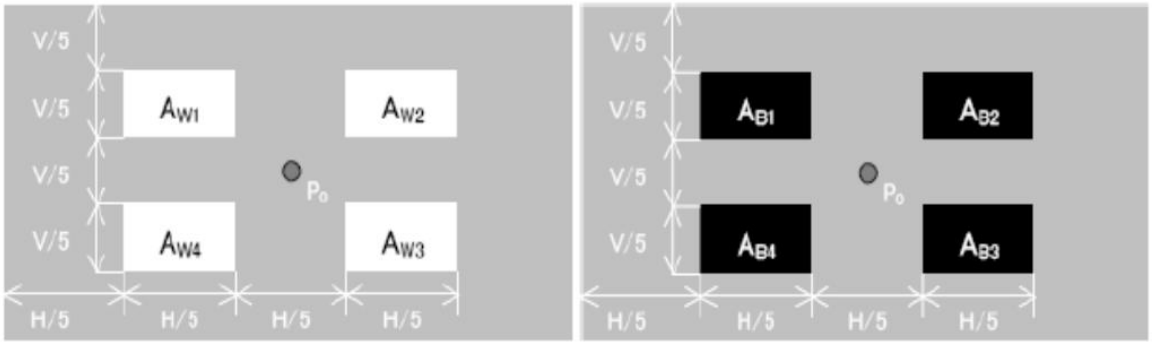
B. Calculate cross talk as below equation.

$$L_{W\_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

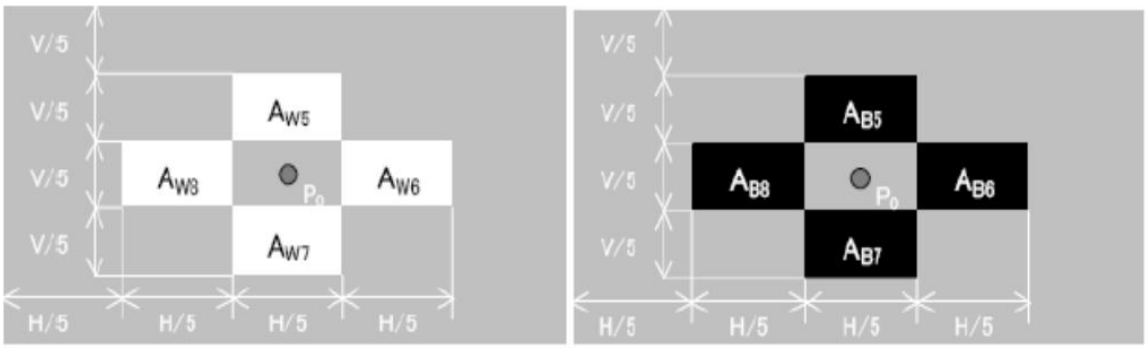
$$L_{B\_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$\text{crosstalk} = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \qquad (i = 5 \text{ to } 8)$$

$$\text{crosstalk} = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \qquad (i = 5 \text{ to } 8)$$

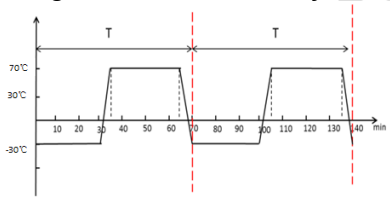
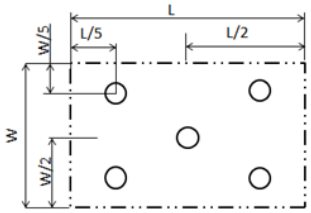


(a) L_{W_OFF}, L_{B_OFF} measuring pattern



(b) L_{W_ON}, L_{B_ON} measuring pattern

9 Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	+60℃, 240hrs	IEC60068-2-2,GB2423.2
2	Low Temperature Operation	-20℃, 240hrs	IEC60068-2-1 GB2423.1
3	High Temperature Storage	+70℃, 240hrs	IEC60068-2-2 GB2423.2
4	Low Temperature Storage	-30℃, 240hrs	IEC60068-2-1 GB2423.1
5	High Temperature & High Humidity Operation	60℃, 90% RH,240hrs	IEC60068-2-78 GB/T2423.3
6	Thermal Shock (Non-operation)	-30℃(30 min)~+70℃(30 min), Change time:5min, 100 Cycles 	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22
7	Electro Static Discharge (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; (Environment: 15℃~35℃, 30%~60%, 86Kpa~106Kpa). 	IEC61000-4-2 GB/T17626.2
8	Package Drop Test	1 corner, 3 edges, 6 surfaces Drop height:760mm	IEC60068-2-32 GB/T2423.8
9	Package Vibration Test	Random Vibration: 1.15Grms, 1~200Hz, Random, 30mins/ (X，Y，Z) axis	IEC60068-2-34 GB/T2423.11

10 Quality Level

10.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

(1) Ambient temperature: 22± 3℃

(2) Humidity: 65 ± 20%RH

(3) Ambient light intensity: 800 ~ 1200 lux

(4) Viewing Distance: 35 ± 5cm

(5) Viewing angle (tolerance): the front side 90° (Z) ±30°

(6) Inspection time: 10 ±2 sec

10.2 Sampling Procedures for each item acceptance table

Defect type	Sampling Procedures	AQL
Major defect	GB/T2828.1-2003 Inspection level Ⅱ normal inspection single sample inspection	0.65
Minor defect	GB/T2828.1-2003 Inspection level Ⅱ normal inspection single sample inspection	1.50

Major defect

Any defect may result in functional failure, or reduce the usability of product for its purpose, such as electrical failure, deformation and etc.

Minor defect

A defect does not reduce the usability of product for its intended purpose and un-uniformity, such as dot defect and etc.

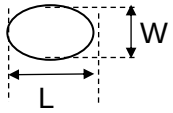
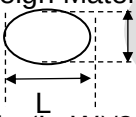
The criteria on major and/or minor judgment will be according with the classification of defects. AQL means that the quality level of product is acceptable for shipment, and the AQL shall satisfy with customer's quality request.

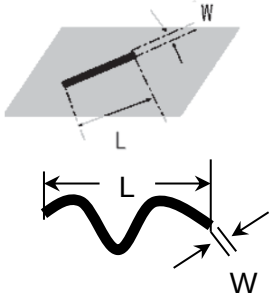
10.3 Inspection Item

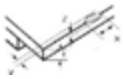
10.3.1 Function tests

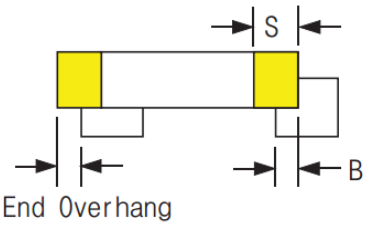
<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>1</td><td>Dot Defect</td><td>
<table>
<tr><th colspan="2">Defect</th><th>Acceptable number</th></tr>
<tr><td colspan="2">Bright Dot</td><td>0</td></tr>
<tr><td rowspan="3">Dark Dot</td><td>Red</td><td>2</td></tr>
<tr><td>Green</td><td>2</td></tr>
<tr><td>Blue</td><td>2</td></tr>
</table>
Dark Dot Distance≧5mm(Acceptable)
</td><td>Minor</td></tr>
<tr><td>2</td><td>No Display</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>3</td><td>Abnormal Display</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>4</td><td>Normally white</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>5</td><td>Flicker</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>6</td><td>Missed Line</td><td>Not allowed</td><td>Major</td></tr>
</table>

10.3.2 Visual inspection

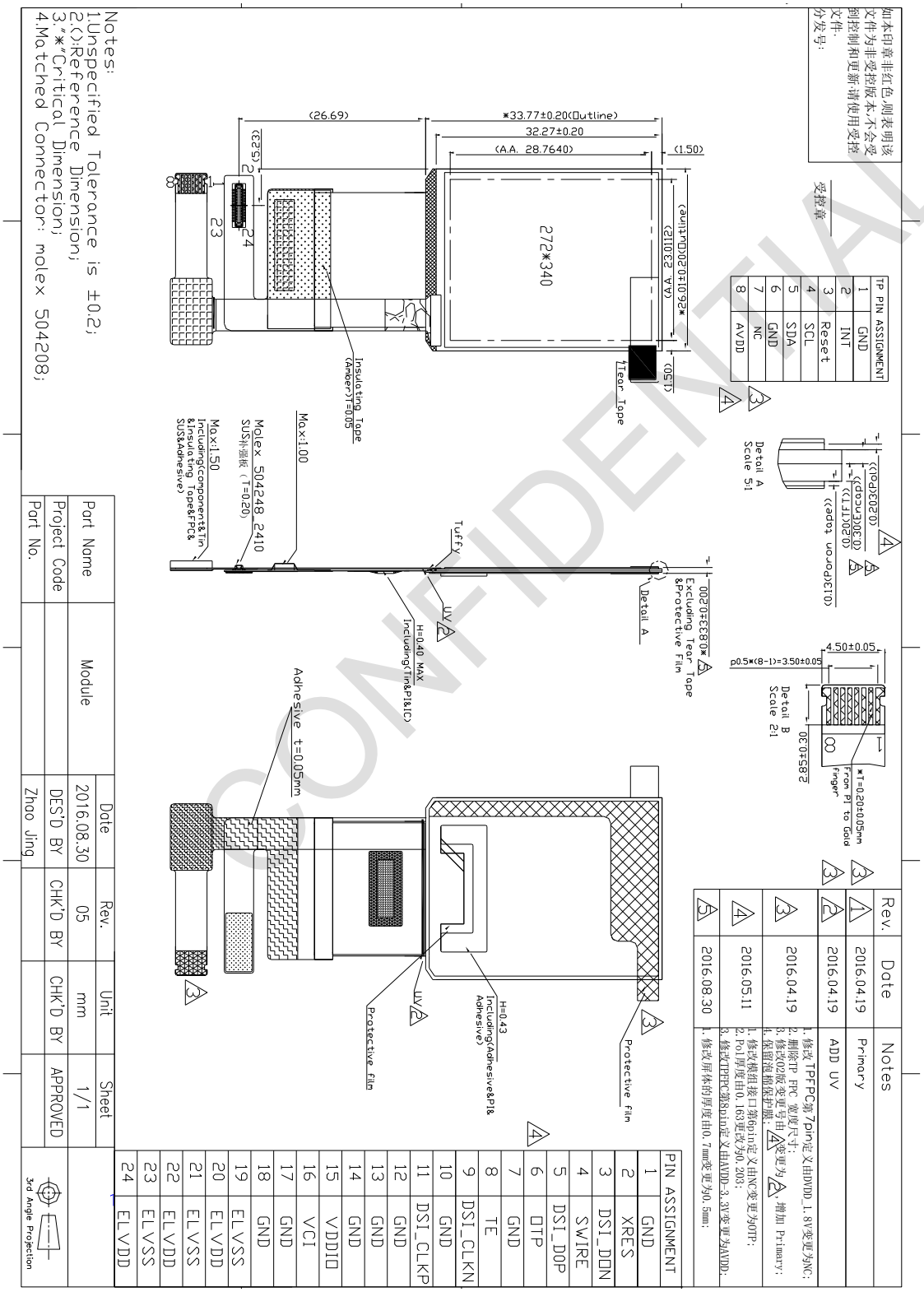
<table>
<tr><td rowspan="2">1</td><td>Polarizer Dent/Bubble
 
</td><td>
<table>
<tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr>
<tr><td>Φ≦0.15</td><td>Ignore</td></tr>
<tr><td>0.15<Φ≦0.30</td><td>1</td></tr>
<tr><td>0.30<Φ</td><td>0</td></tr>
</table>
</td><td>Major</td></tr>
<tr><td>Polarizer Dark/Bright Spots (Foreign Material)
 

Φ=(L+W)/2</td><td>
<table>
<tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr>
<tr><td>Φ≦0.10</td><td>Ignore</td></tr>
<tr><td>0.10<Φ≦0.20</td><td>1</td></tr>
<tr><td>0.20<Φ</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>Polarizer Scratch/ Fiber(Linear)
 
</td><td>
<table>
<tr><th>Width(mm)</th><th>Length(mm)</th><th>Acceptable number</th></tr>
<tr><td>W≦0.02</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.02<W≦0.03</td><td>L≦1.00</td><td>1</td></tr>
<tr><td>0.03<W</td><td>-</td><td>0</td></tr>
<tr><td></td><td>L>1.00</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
</table>

<table>
<tr><td>3</td><td>Discoloration</td><td>If its limit sample is needed, it can be fixed mutually with a customer</td><td>Minor</td></tr>
<tr><td rowspan="3">4</td><td>Encap glass chipping \ chipping
  </td><td>The following standards apply to any side of the panel. (unit: mm)<table><tr><td>Z</td><td>X</td><td>Y</td></tr><tr><td><t</td><td>⩽1.0</td><td>⩽0.5</td></tr></table></td><td>Minor</td></tr>
<tr><td>Substrate glass chipping \ chipping
 
Front
 
Rear</td><td>The following standards just apply to the side of the pad.(unit: mm)<table><tr><td colspan="2"></td><td>Z</td><td>X</td><td>Y</td></tr><tr><td rowspan="2">Front of the pad</td><td>Near the screen</td><td><t</td><td>⩽1.0</td><td>⩽0.3</td></tr><tr><td>Away from the pattern</td><td><t</td><td>⩽1.2</td><td>⩽0.4</td></tr><tr><td colspan="2">Rear of the pad</td><td><t</td><td>⩽1.2</td><td>⩽0.4</td></tr></table></td><td>Minor</td></tr>
<tr><td>The following standards apply to any side of the panel (except pad side). (unit: mm)<table><tr><td>Z</td><td>X</td><td>Y</td></tr><tr><td><t</td><td>⩽1.0</td><td>⩽0.5</td></tr></table></td><td>Minor</td></tr>
<tr><td>5</td><td>Glass crack</td><td>Not allowance</td><td>Major</td></tr>
<tr><td>6</td><td>Panel Scratch</td><td><table><tr><td>Width(mm)</td><td>Length(mm)</td><td>Acceptable number</td></tr><tr><td>W⩽0.03</td><td>Ignore</td><td>Ignore</td></tr><tr><td rowspan="2">0.03＜W⩽0.05</td><td>L⩽2.0</td><td>Ignore</td></tr><tr><td>2.0＜L⩽5.0</td><td>2</td></tr><tr><td>0.05＜W</td><td>-</td><td>0</td></tr><tr><td></td><td>L>5.0</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Encapsulation</td><td>Frit width can’t be less than the design width of 9/10.</td><td>Minor</td></tr>
<tr><td>8</td><td>Over Coating</td><td>The coating of non-IC side must not exceed glass section.
The coating of IC side is not allowed higher than POL.</td><td>Minor</td></tr>
<tr><td rowspan="4">9</td><td rowspan="4">FPCA</td><td>(1) The component should not be polarity opposition</td><td>Major</td></tr>
<tr><td>(2) No wrong insertion</td><td>Major</td></tr>
<tr><td>(3)FPC should not have serious crease which causes the line, prick and spots damage. Scratch is not allowed if Cu layer is exposed.</td><td>Minor</td></tr>
<tr><td>(4) The gold fingers should not be oxidized, scraped, folded, impressed, broken, spotted or</td><td>Major</td></tr>
</table>

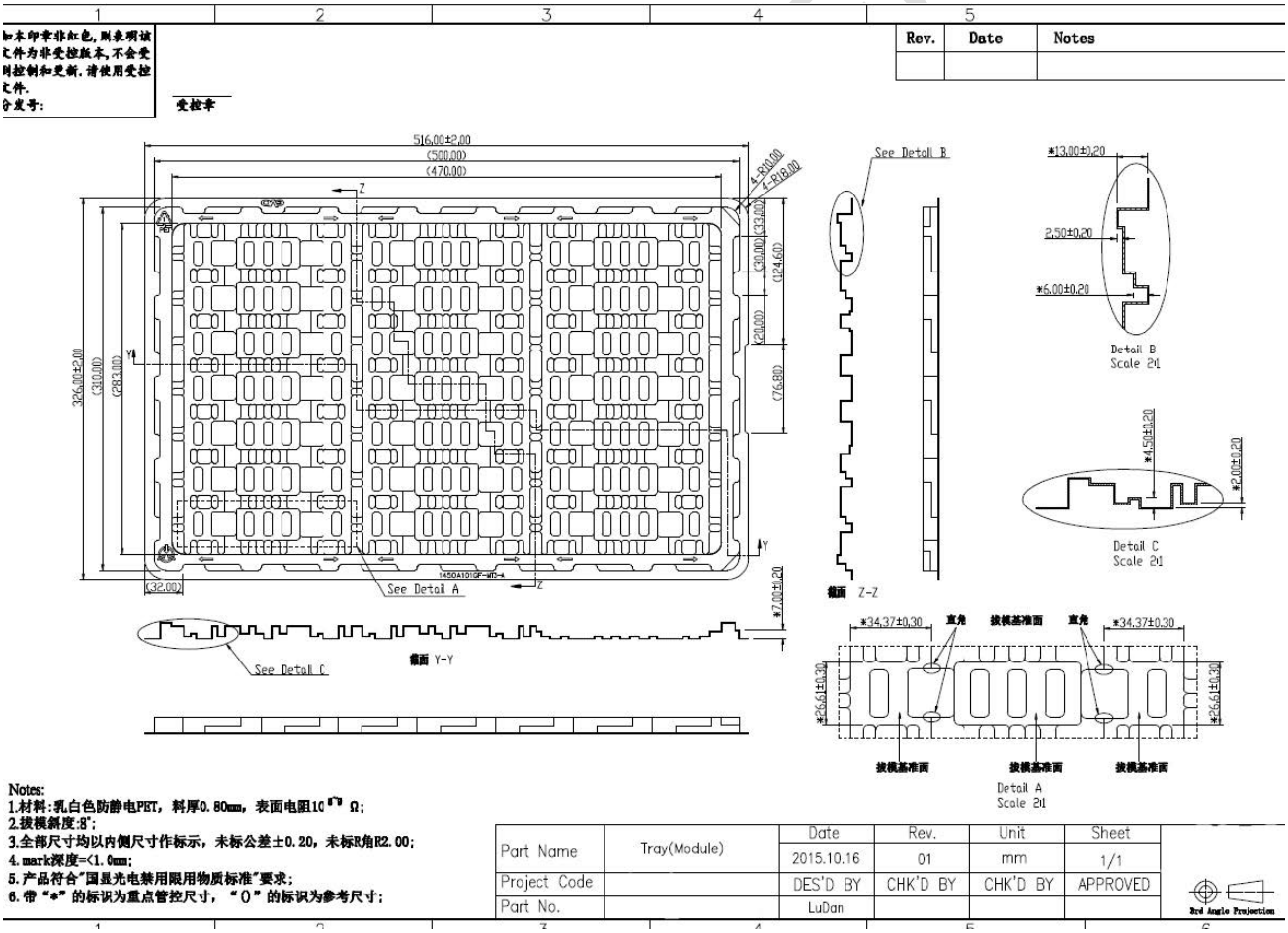
		dissymmetry.	
		(5) Make sure FPC is not scalded, with its location holes not having deficiency or obviously shift.	Major
		(6)The component of FPC should be the same as BOM list.	Major
		(7)No remaining soldering Sn.	Major
		(8)No visual particle on the pad line.	Minor
10	FPCA End Overhang	The size above 1/2 of soldering electrode of the parts overhang to the LAND is prohibited. (but contacting near other components is prohibited)  End Overhang	Major
11	FPC Tilt Defect	Not allowed	Major
12	Package	(1) Products should put into the anti-static trays, with non-overlapping, and the trays should be staggered placed. (2) Different products cannot be mixed into the same inner package. (3) The package should not have obvious deformation or breakage .The printing labels type and quantity are correct. (4) The package should have QC signature. ROHS label is needed if the product is under ROHS control.	Minor

11 Mechanical Drawing



Packing Drawing

Packing Condition	Contents
Packing Type	TRAY + Carton packing type
TRAY material model	tray (10^5~$10^9\Omega$)
Tray packing type	See the picture 1
Number of panels per tray	42 pieces
Number of Tray per carton	19units ((18 units + 1 empty)PET tray)
Number of panels per carton	756 pieces



12 Precautions for Use of AMOLED Modules

12.1 Handling Precautions:

12.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height.

12.1.2 Do not press down the screen or the adjoining areas too hard because the color tone may be shifted.

12.1.3 The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.

12.1.4 If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.

12.1.5 Solvents may damage the polarizer. Do not use water、ketone or aromatic solvents except ethyl alcohol.
Do not attempt to disassemble the AMOLED Module.

12.1.6 If the logic circuit power is off, do not apply the input signals.

12.1.7 To prevent destruction from static electricity, be careful to maintain an optimum working environment.

12.1.8 Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.

12.1.9 Tools required for assembly, such as soldering irons, must be properly ground.

12.1.10 To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.

12.1.11 To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

12.2 Storage Precautions:

12.2.1 When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.

12.2.2 The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is:
Temperature: 0℃~40℃ Relatively humidity: ≤80%

12.2.3 The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

12.3 Transportation Precautions:

12.3.1 The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.