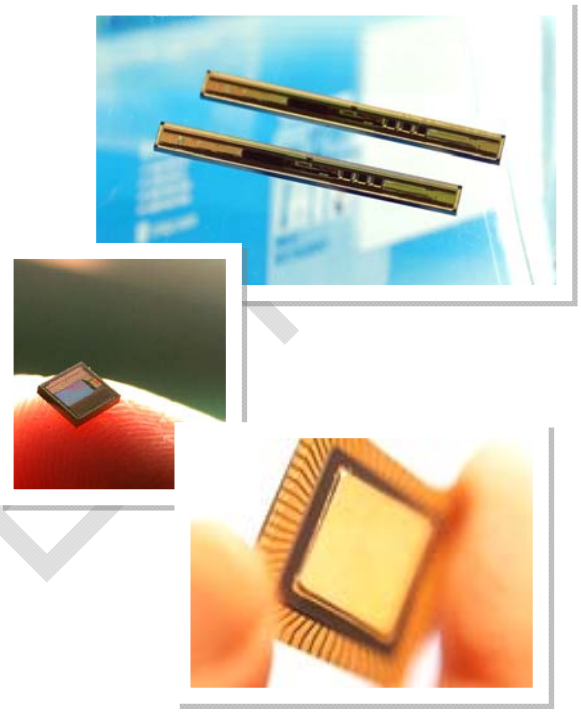
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM67160 Data Sheet

Single Chip Driver with 16.7M color

for 480RGBx480 OLED driver

Revision：0.2

Date：Jan 30, 2015

Revision History

Version No.	Date	Description	Page	Modified By	Checked By
0.0	2014/12/15	First Release		CL Hou	
0.1	2014/12/26	Modify Pad Diagram: BUMP dimension & coordinate	136	CL Hou	
0.2	2015/01/23	Update CMD list & description Update alignment mark coordinate	39 133	CL Hou	
	2015/01/30	Update Deep standby mode notice. Update power on sequence to add Tini>1ms.	94 131	CL Hou	

Table of Contents

1. General Description

The RM67160 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 480RGBx480, 400RGBx400, 360RGBx480, 320RGBx320, 320RGBx480, 272RGBx480, 240RGBx240, 240RGBx320, 180RGBx360, 180RGBx540, 128RGBx432with internal GRAM. It includes a 5,529,600 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The RM67160 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The RM67160 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 480-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for wearable device applications, including I-watch and smart band.

2. Features

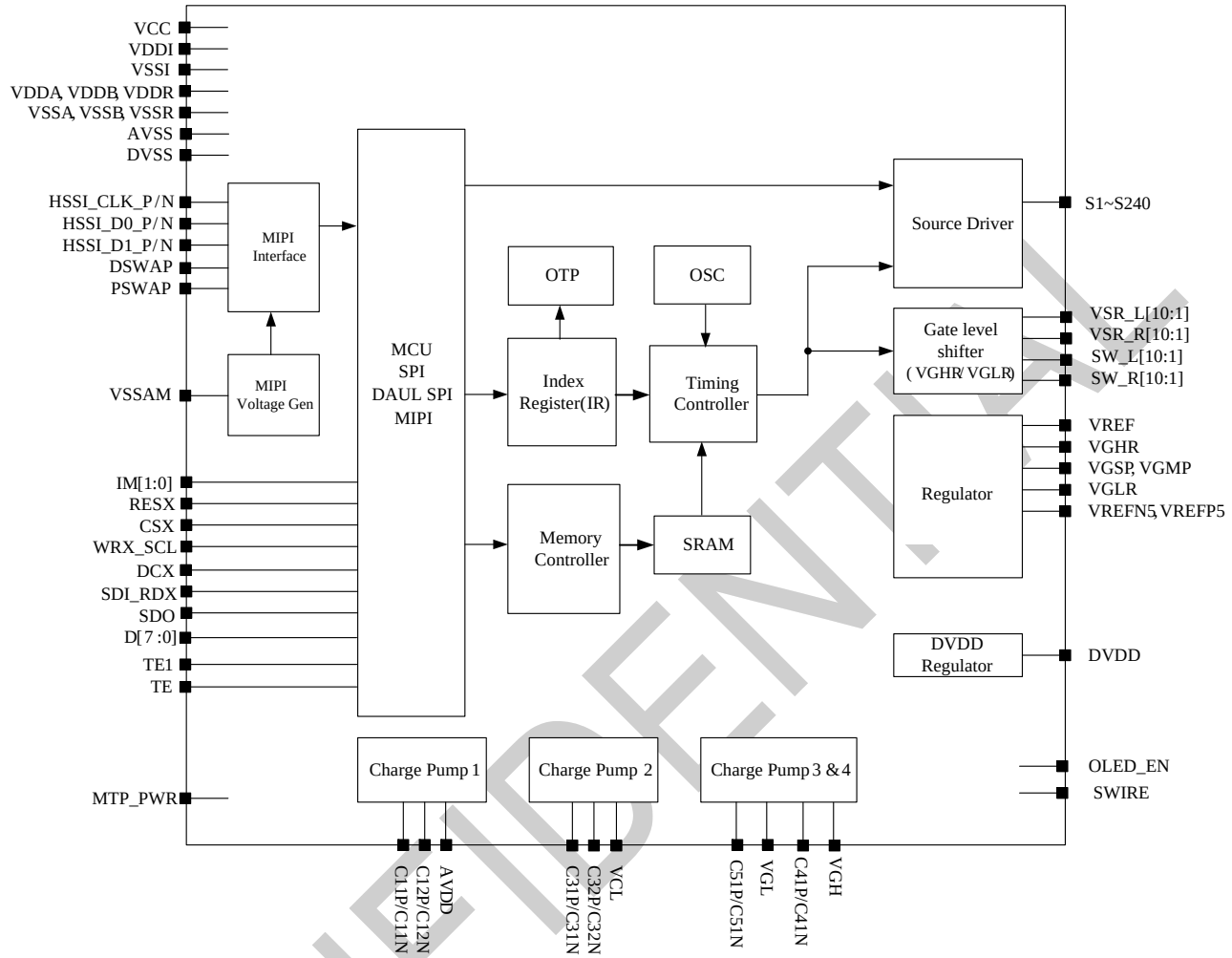
- **Single chip AMOLED controller/driver with display RAM**
- **Display resolution option**
  - 480RGB x 480 with 480x24-bits x 480 GRAM
  - 400RGB x 400 with 400x24-bits x 400 GRAM
  - 360RGB x 480 with 360x24-bits x 480 GRAM
  - 320RGB x 320 with 320x24-bits x 320 GRAM
  - 320RGB x 480 with 320x24-bits x 480 GRAM
  - 272RGB x 480 with 272x24-bits x 480 GRAM
  - 240RGB x 240 with 240x24-bits x 240 GRAM
  - 240RGB x 320 with 240x24-bits x 320 GRAM
  - 180RGB x 360 with 180x24-bits x 360 GRAM
  - 180RGB x 540 with 180x24-bits x 540 GRAM
  - 128RGB x 432 with 128x24-bits x 432 GRAM
- **Display data RAM (frame memory): 480 x480 x 24-bits = 5,529,600 bits**
- **Display mode (Color mode)**
  - Full color mode: 16.7M-colors
  - Idle mode: 16.7M-colors, 4096-colors, 8-colors
- **Interface**
  - 8-bits 80-series MPU interface
  - Serial peripheral interface (SPI)
  - Dual serial peripheral interface (Dual-SPI)
  - MIPI Display Serial Interface (1 clock and 2 data lane pairs)
    - Support 1lane/2lane (1lane: 500Mbps)
    - Maximum total bit rate is 500Mbps of 2 data lanes 24-bit data format/ 360Mbps of 2 data lanes 18-bit data format/ 320Mbps of 2 data lanes 16-bit data format
- **Abundant color display and drawing functions**
  - Programmable γ-correction function for 16.7 million color display
  - Individual gamma correction setting for RGB dots
  - Partial display function
- **Sunlight readable**
- **Control power IC by one-wire interface**
- **On chip**
  - VREFP5/VREFN5 voltage generator for panel voltage
  - VGHR/VGLR voltage for gate control signal
  - Internal oscillator for display clock
  - Source output MUX 1-6 with 240ch source output pins
  - Supports gate control signals to gate driver in the panel
- **Built-in OTP function to adjust panel setting**
- **Logic / interface power supply voltage VDDI = 1.65V ~ 1.8V**
- **Analog power supply voltage VDD = 2.7V ~ 3.6V**

- **Output voltage levels**
  - Positive gate driver voltage range for VGHR: 3 ~ 10V
  - Negative gate driver voltage range for VGLR: -2V ~ -9V
  - VREFP5 panel voltage range : 0~5V
  - VREFN5 panel voltage range : -0.5~-5V
  - Step-up 1,2 output voltage range for AVDD: 4.5 ~ 6.5V, VCL: -3.5 ~ -5.0V
  - Gamma high/low voltage range for VGMP: 2.0V ~ 6.0V (Max<=AVDD-0.5v) , VGSP: 0V, 0.3V ~ 4.5V
- **Package: COF/COG**
- **Chip size evaluation : 8300um x 2360um(including scribe line)**

■ **Power Supply Specifications**

No.	Item		Description
1	Source Driver		240 pins (480 x RGB)
2	gate control timing Level shift		VGHR-VGLR
5	Input Voltage	VDDI	1.65 ~ 1.8V
		VCC	Connect to VDDI or VDD(VCI)
		VDD (VDDA/VDDB/VDDR)	2.70 ~ 3.60V
6	OLED drive voltages	AVDD	4.5V ~ 6.5V
		VGHR	3V ~ 10V
		VGLR	-2V ~ -9V
		VREFP5	0V ~ 5V
		VREFN5	-0.5V ~ -5V
7	Internal step-up circuits	AVDD	VCI x2.0(dual), x3.0(single)
		VCL	VCI x -1.0(dual), x-2.0(single)
		VGH	VCI x2, x3, x4
		VGL	VCI x-2, x-3, x-4

3. Block Diagram



Interface

The RM67160 supports MIPI DSI interface. MIPI DSI can access both internal command and display data.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the γ correction register. The RM67160 displays 16.7M colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to OLED panel, VGH, VGL.

Timing Generating

The timing controller generates timing signals for internal circuits such as the display timing.

Oscillator

The RM67160 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The OLED display driver circuit consists of 240 source drivers (S1~S240). The gate signal consists of VSR_R/L[1:10], SW_R/L[1:10] and outputs either VGHR or VGLR level.

4. Pin Description

4.1 Power Supply Pins

Signal	I/O	Function
VDDB	P	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	P	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	P	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDDI	P	Power supply for interface system except MIPI interface
VCC	P	Power supply for DVDD regulator
VSSB	P	System ground for DC/DC converter
VSSA	P	System ground for analog system
VSSR	P	System ground for regulator system
VSSAM	P	System ground for internal MIPI analog system
VSSI	P	System ground for interface system except MIPI interface
DVSS	P	System ground for internal digital system
AVSS	P	System ground for source OP system.
MTP_PWR	P	MTP programming power supply pin (7.5V typical) Must be left open or connected to DVSS in normal condition.

4.2 Interface Pins

Signal	I/O	Function
CSX	I	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. If not used, please connect to VSSI.
WRX_SCL	I	WRX : Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. If not used, please connect to VSSI.
D/CX	I	Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F. D/CX = ”0” : Command D/CX = ”1” : Display data or Parameter If not used, please connect to VSSI.
SDI_RDX	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. RDX : Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface. If not used, please leave it Open.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. If not used, please open this pin.
D[7:0]	I/O	8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F. These pins are not used for SPI, MIPI, please leave it Open.

4.3 MIPI Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>HSSI_CLK_P
HSSI_CLK_N</td><td>I</td><td>-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D0_P
HSSI_D0_N</td><td>I/O</td><td>-These pins are DSI-D0+/- differential data signals if MIPI interface is used.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D1_P
HSSI_D1_N</td><td>I/O</td><td>-These pins are DSI-D1+/- differential data signals if MIPI interface is used.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only.
<table>
<tr><th>Pin Name</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th></tr>
<tr><td>DSWAP=0
PSWAP=0</td><td>DSI
D0+</td><td>DSI
D0-</td><td>DSI
CLK+</td><td>DSI
CLK-</td><td>DSI
D1+</td><td>DSI
D1-</td></tr>
<tr><td>DSWAP=0
PSWAP=1</td><td>DSI
D0-</td><td>DSI
D0+</td><td>DSI
CLK-</td><td>DSI
CLK+</td><td>DSI
D1-</td><td>DSI
D1+</td></tr>
<tr><td>DSWAP=1
PSWAP=0</td><td>DSI
D1+</td><td>DSI
D1-</td><td>DSI
CLK+</td><td>DSI
CLK-</td><td>DSI
D0+</td><td>DSI
D0-</td></tr>
<tr><td>DSWAP=1
PSWAP=1</td><td>DSI
D1-</td><td>DSI
D1+</td><td>DSI
CLK+</td><td>DSI
CLK-</td><td>DSI
D0-</td><td>DSI
D0+</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
</table>

NOTE: “1” = VDDI level, “0” = VSSI level.

4.4 Interface Logic Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>RESX</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>Interface type selection. The connections of IM[1:0] which not shown in table are invalid.
<table>
<tr><th>IM[1:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>00</td><td>MIPI / 3-wire SPI</td><td>MIPI / 3-wire SPI</td></tr>
<tr><td>01</td><td>MIPI / 4-wire SPI</td><td>MIPI / 4-wire SPI</td></tr>
<tr><td>10</td><td>MIPI / 16-SPI</td><td>MIPI / 16-SPI</td></tr>
<tr><td>11</td><td>MCU 8-bit</td><td>MCU 8-bit</td></tr>
</table></td></tr>
<tr><td>BSTM</td><td>I</td><td>Boost mode selection pin.
<table>
<tr><th>BSTM</th><th>Mode</th></tr>
<tr><td>0</td><td>2 PWR(VDDI, VCI)
AVDD --> internal CP
VCL --> internal CP</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td rowspan="2">Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
When this pin is not activated, this pin is output low.
If not used, please open this pin.</td></tr>
<tr><td>TE1</td><td>O</td></tr>
<tr><td>SWIRE</td><td>O</td><td>Swire protocol setting pin of Power IC, If not used, please open this pin.</td></tr>
<tr><td>OLED_EN</td><td>O</td><td>Power IC enable control pin, If not used, please open this pin.</td></tr>
</table>

NOTE: “1” = VDDI level, “0” = VSSI level.

4.5 Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S1 ~ S240	O	Pixel electrode driving output.
SDMY	O	Dummy Source, leave it Open.
VSR_L[10:1] VSR_R[10:1]	O	VSR control signals, Level shift output, (VGHR-VGLR)
SW_L[10:1] SW_R[10:1]	O	VSR control signals, Level shift output, (VGHR-VGLR)

4.6 DC/DC Convert Pins

Signal	I/O	Function
AVDD	O	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGL	O	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C11P, C11N C12P, C12N	IO	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	IO	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	IO	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	IO	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitor as requirement.
VGHR	O	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	O	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	O	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	O	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VREF	O	Regulator output for internal reference voltage. Connect capacitor for stabilization.
DVDD	O	Regulator output for logic system power. Connect a capacitor for stabilization.
VREFP5	O	Regulator output for VREFP(0~5V)
VREFN5	O	Regulator output for VREFP(-0.5~-5V)

4.7 Test Pins

Signal	I/O	Function
ANALOG_TEST 1~2	O	Test pin, not accessible to user. Must be left open.
TEST1~3	IO	Test pin, not accessible to user. Must be left open.
TESTEN	I	Test pin, not accessible to user. Must be left open., Internal pull low
EXTCLK	I	Test pin, not accessible to user. Must be left open.
DUMMY	I	Dummy PAD, leave it open

5. Function Description

5.1 Interface Type Selection

Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / 16-SPI	MIPI / 16-SPI
11	MCU 8-bit	MCU 8-bit

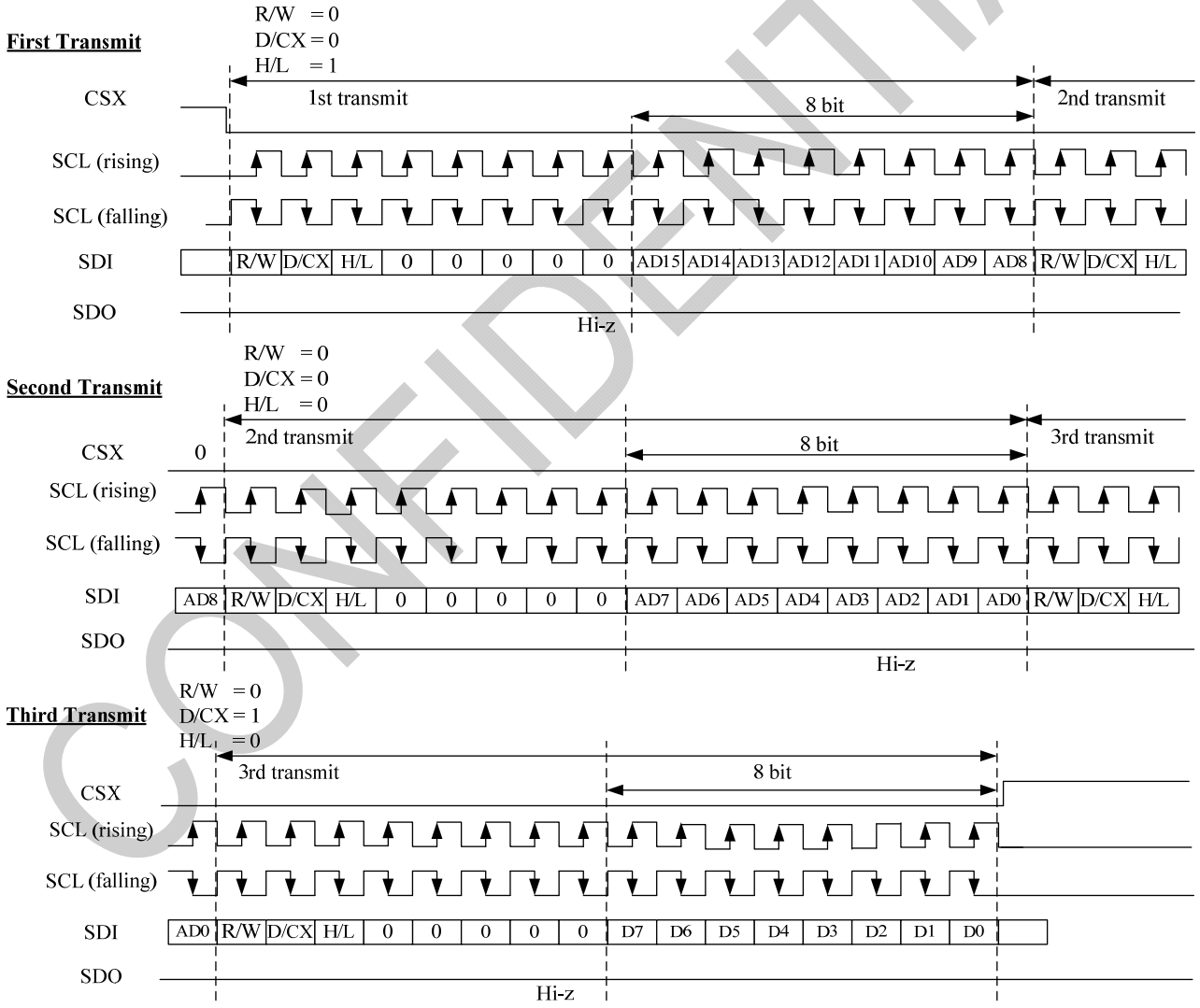
5.2 Serial Interface

5.2.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The SPI interface utilizes CSX, SCL and SDI and SDO signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight write cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface write command sequences are described in the following figure.

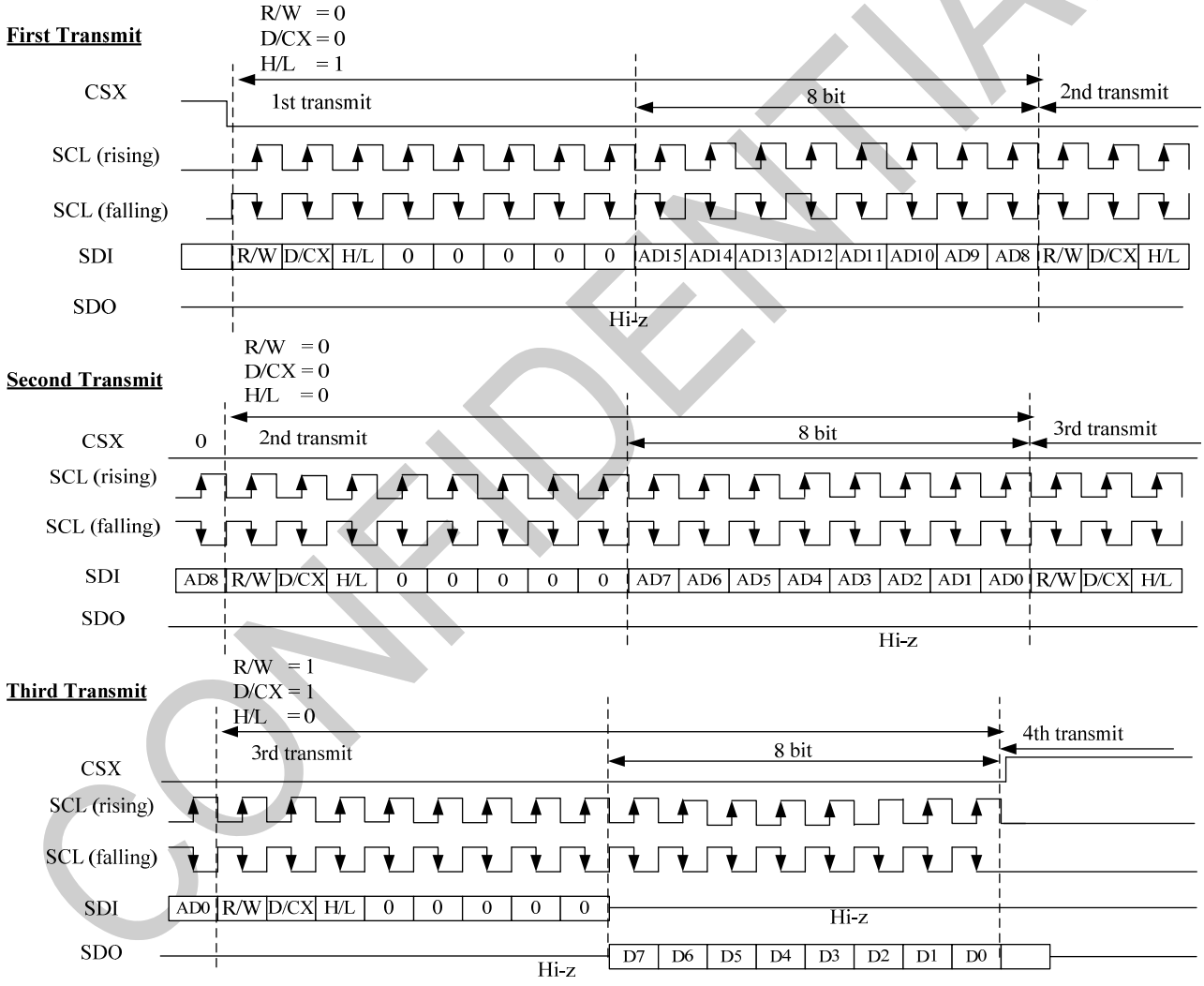


5.2.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The SPI interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight read cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

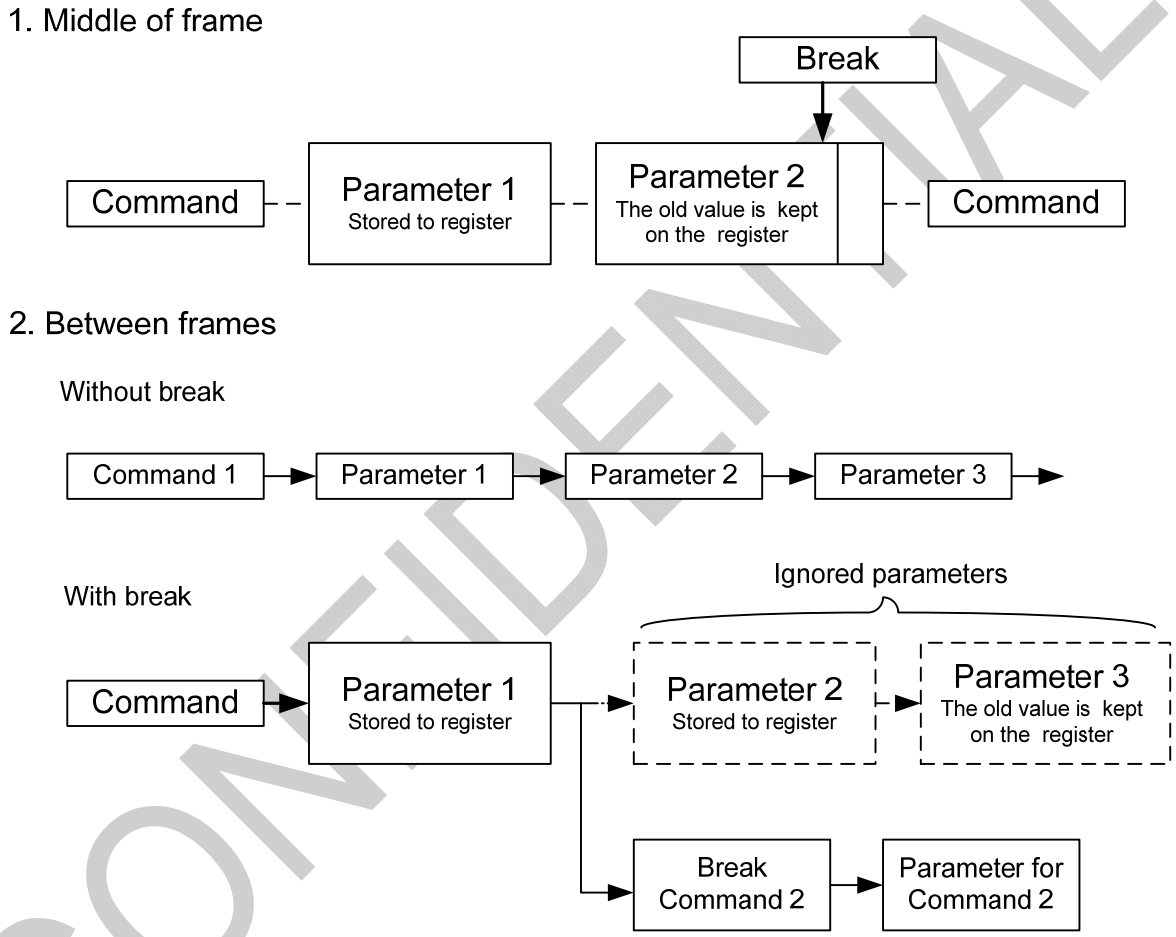
The SPI interface read command sequences are described in the following figure.



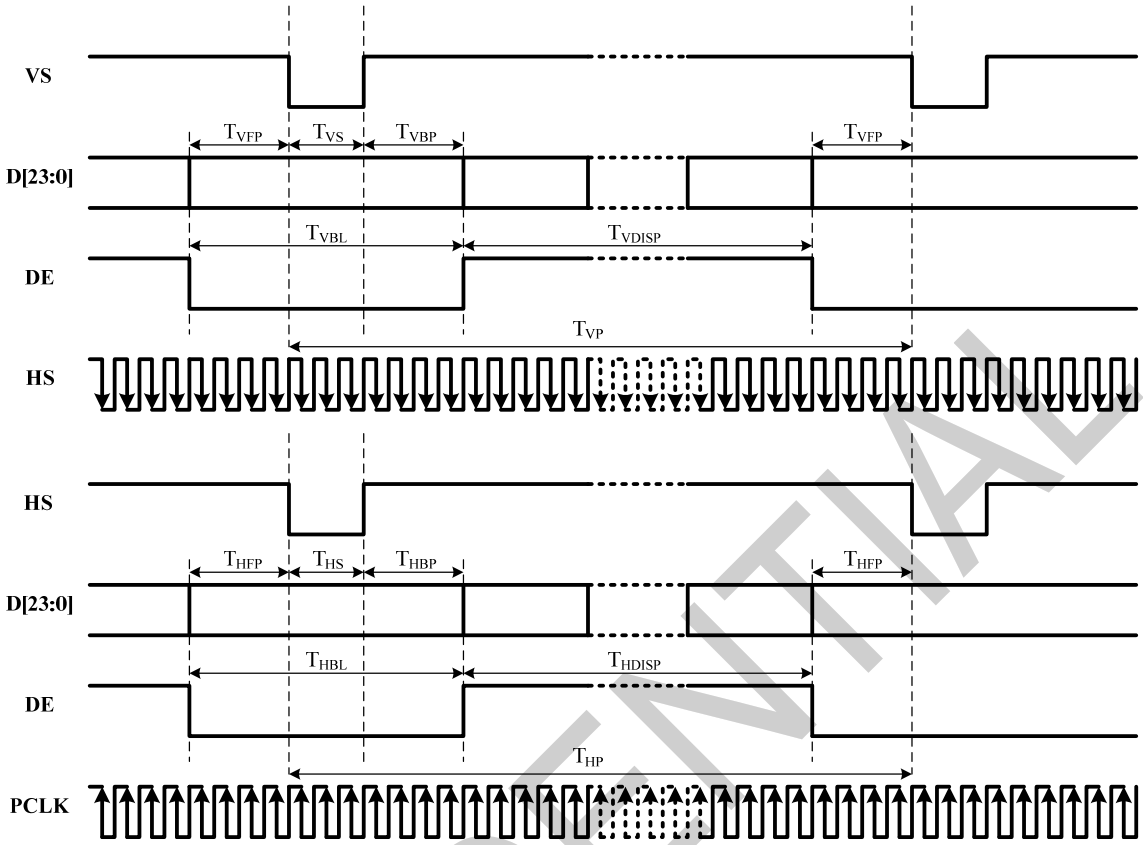
5.2.3 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.



Break can be e.g. another command or noise pulse.



5.3 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

RM67160 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller.

The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

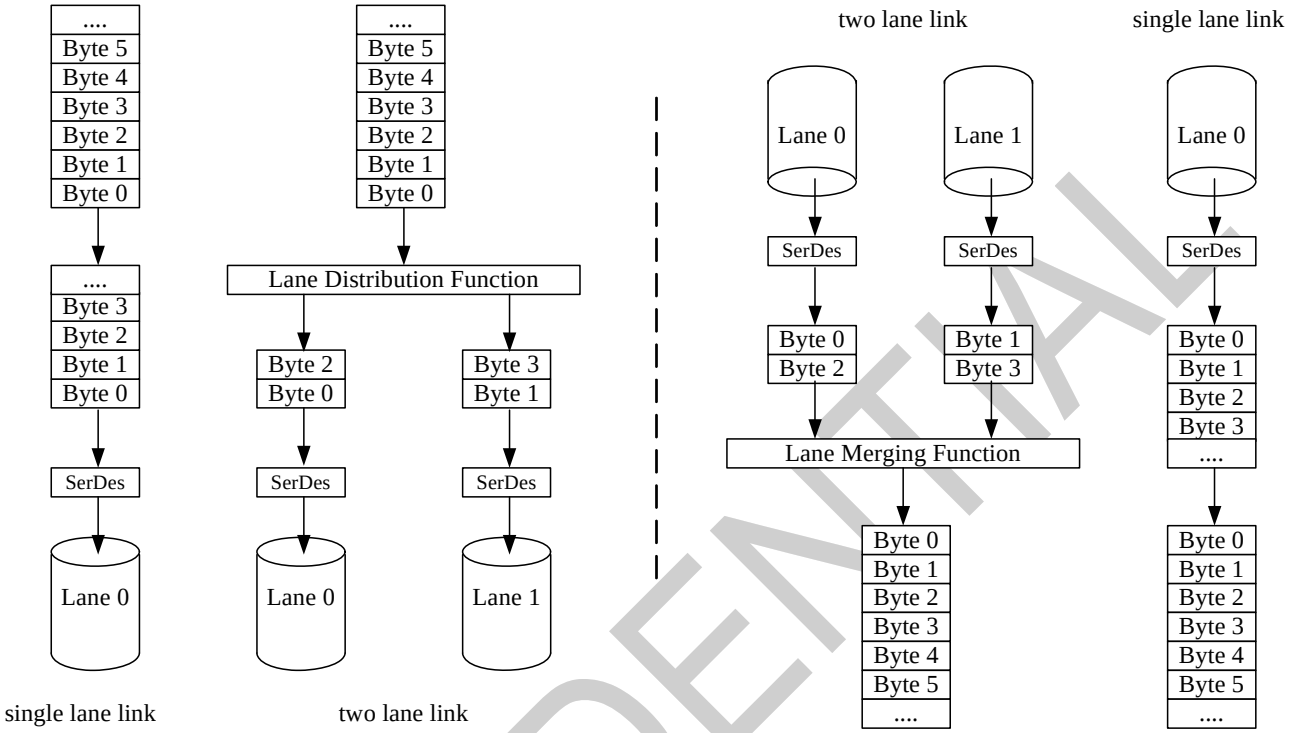
RM67160 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

RM67160 Configuration:

Lane Pair	MCU(Master)　RM67160(Slave)
Clock Lane	Unidirectional Lane Clock only
Data Lane 0	Bi-directional Lane Forward High-speed Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane Forward High-Speed Escape Mode No LPDT

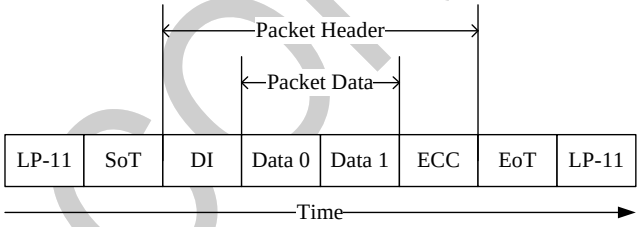
5.3.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.



There are two kinds of packets, **short packet and long packet**.

Short packet structure:
LP-11: low power mode
SoT: start of transmission
DI: data identification
Data 0, Data1: packet data
ECC: error correction code
EoT: End of Transmission



DI structure:
Virtual Channel: these two bits identify the data as directed to one of four virtual channels
Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Long packet structure:
LP-11: low power mode
SoT: start of transmission
DI: data identification
Word Count: the number of data bytes of packet data
ECC: error correction code
Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission

5.3.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type	Data Type binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

Sync Event, Data Type = xx 0001
Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

EoT packet
This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall syntem reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM67160 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

Color Mode Off / On Command
They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

Generic short write / read packet
Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

DCS commands
DCS short write command
DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

DCS read commands
The commands are used to request data from s display module.

DCS Long Write / write_LUT command
The commands are used to send larger blocks of data to a display module.

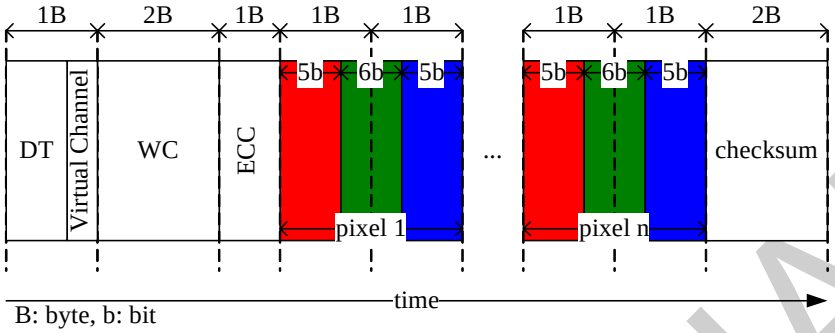
Maximum return packet size
This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Null Packet
This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

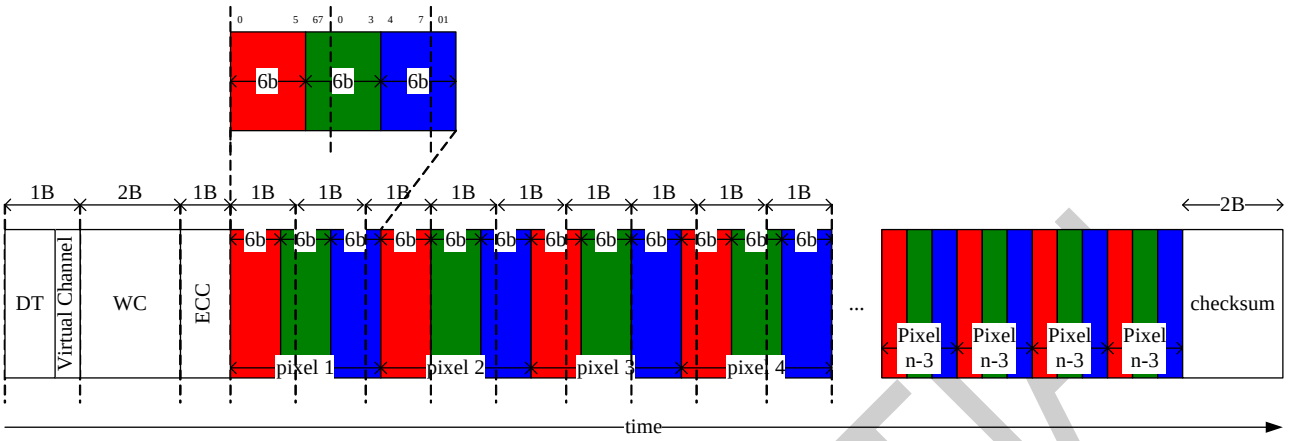
Blanking Packet
A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

Generic Long Write
This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

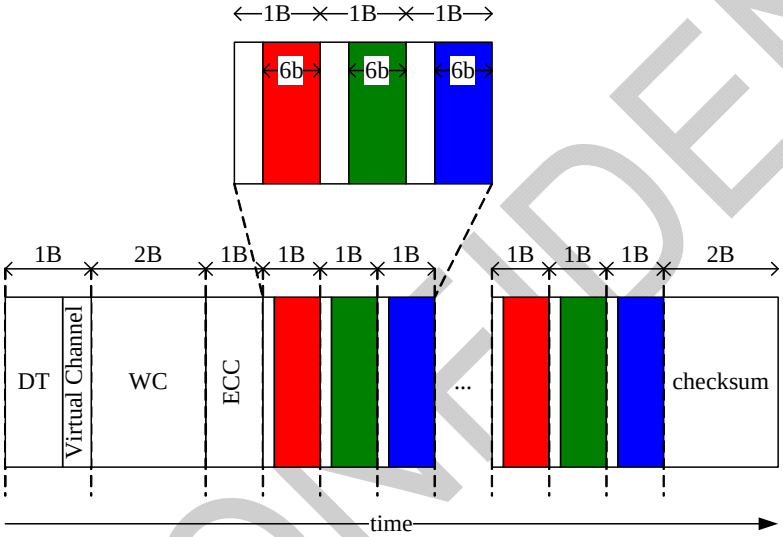
Packed Pixel Stream, 16-bit Format, Data Type: 00 1110
The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



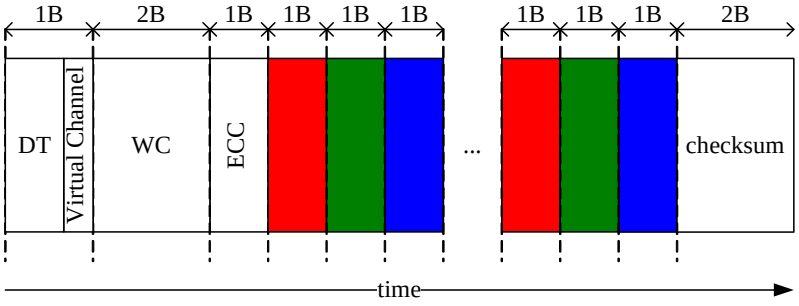
Packet pixel stream, 18-bit format, Data Type: 01 1110
The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.



Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110
This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.



Packet pixel stream, 24-bit format, Data Type: 11 1110
The pixel format is eight bits red, eight bits green and eight bits blue.



5.3.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission.

Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor.
Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.

Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.
Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:
Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.

Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.

Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.

Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.

Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.

Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.

Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.

Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.

5.3.4 Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

5.3.5 Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read reponse, 1byte returned	short
12h	01 0010	GEN short read reponse, 2bytes returned	short
1Ah	01 1010	Generic long read reponse	long
1Ch	01 1100	DCS long read reponse	long
21h	10 0001	DCS short read reponse, 1byte returned	short
22h	10 0010	DCS short read reponse, 2bytes returned	short

Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

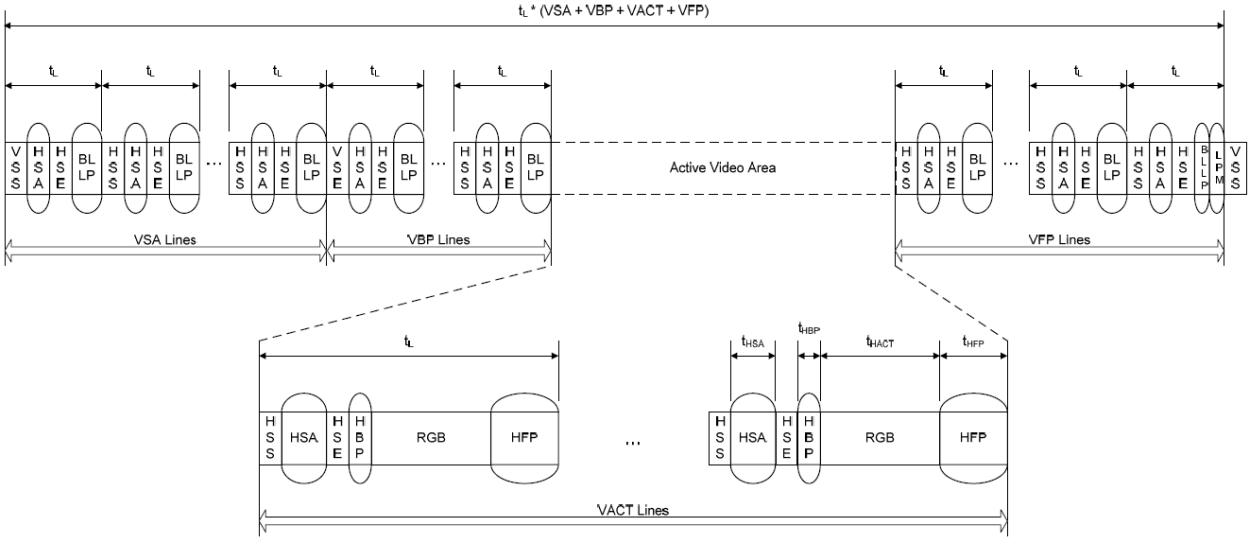
Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

5.3.6 DSI Video Mode Interface Timing



5.3.7 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

The parity bits of ECC are defined as below:
P7 = 0
P6 = 0
P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

ECC Parity Generation Rules:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B

5.3.8 Notice

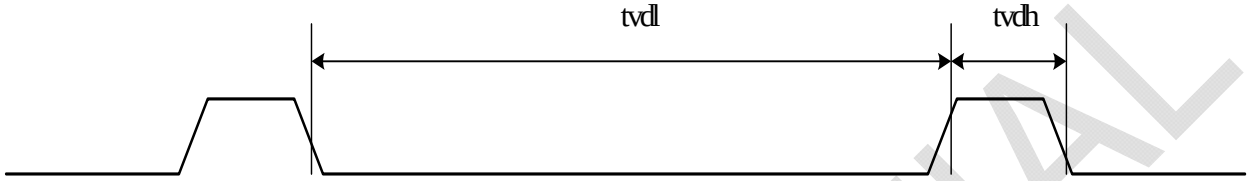
1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
2. We recommend users to adopt EoTp to enhance overall robustness of the system during HSDT.

5.4 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

5.4.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:

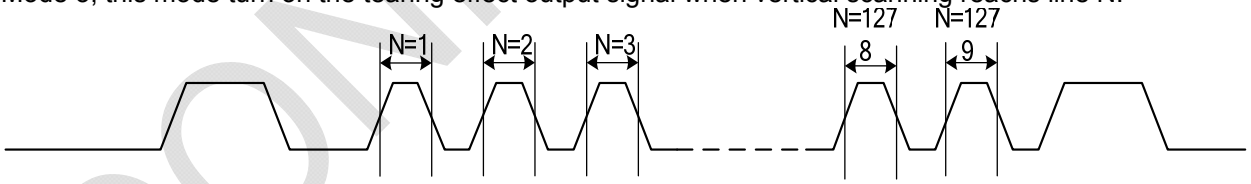


tvdh = The LCD display is not updated from the frame memory.
tvdl = The LCD display is updated from the frame memory.

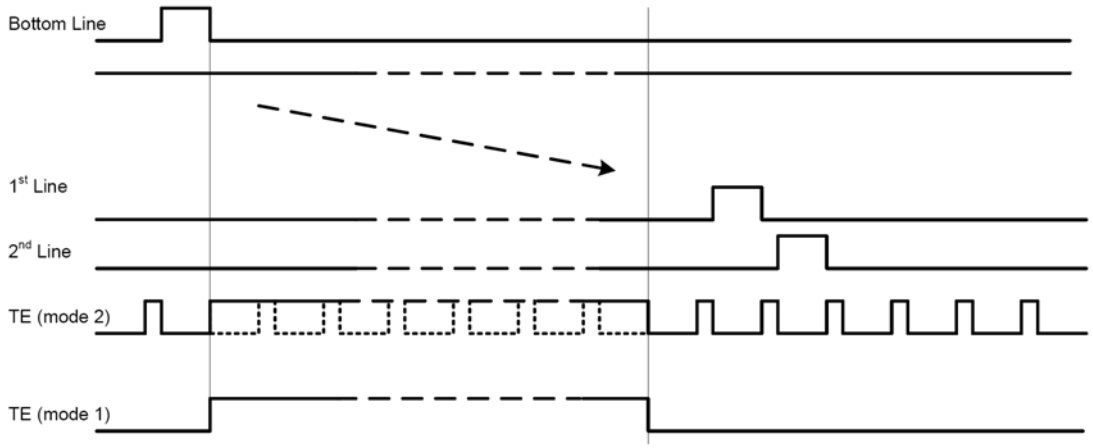
Mode 2, the tearing effect output signal consist of V-sync and H-sync information:

thdh = The LCD display is not updated from the frame memory.
thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.



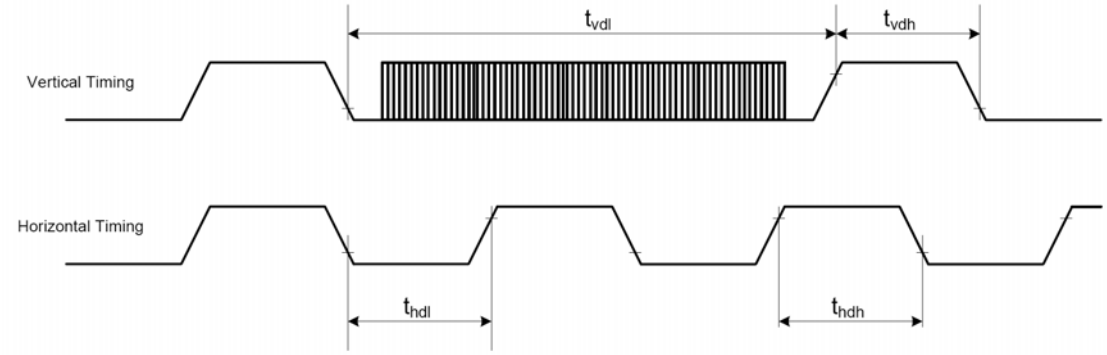
N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



Note. During Sleep In mode, the tearing effect output signal is active low.

5.4.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

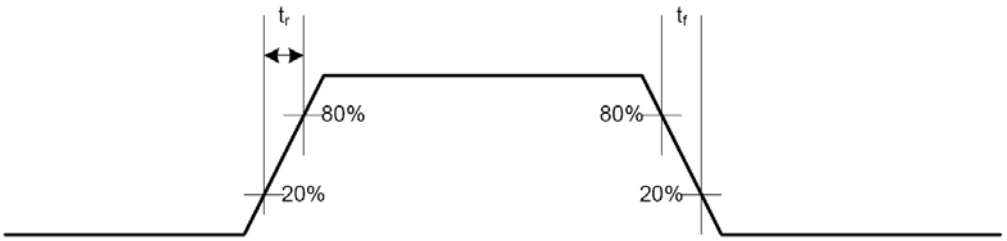


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical timing low duration	TBD		ms	
tvdh	Vertical timing high duration	TBD		us	
thdl	Horizontal timing low duration	TBD		us	
thdh	Horizontal timing high duration	TBD		us	

Notes:

1. The timings apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

TEON (35h)	TELOM (35h, 1st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

6. Command

6.1 Command List

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP
Page	Add.	Para.												
CMD1	00h	-	W	NOP	No Argument								-	-
CMD1	01h	-	W	Software reset	No Argument								-	-
CMD1	04h	1st	R	Read display identification information	ID1[7:0]								00h	-
CMD1	04h	2nd			ID2[7:0]								80h	-
CMD1	04h	3rd			ID3[7:0]								00h	-
CMD1	05h	-	R	Read number of the errors on DSI	P[7:0]								00h	-
CMD1	0Ah	1st	R	Read display power mode	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON	-	-	08h	-
CMD1	0Bh	1st	R	Read display MADCTR	MY	MX	MV	ML	RGB	-	RSMX	RSMY	00h	-
CMD1	0Ch	1st	R	Read display pixel format	-	1	1	1	-	IFPF2	IFPF1	IFPF0	77h	-
CMD1	0Dh	1st	R	Read display image mode	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h	-
CMD1	0Eh	1st	R	Read display signal mode	TEON	M	0	0	0	0	0	ERR	00h	-
CMD1	0Fh	1st	R	Read display self-diagnostic result	0	0	0	0	0	0	0	checksum_comp	00h	-
CMD1	10h	-	W	Sleep-in	No Argument								-	-
CMD1	11h	-	W	Sleep-out	No Argument								-	-
CMD1	12h	-	W	Partial display mode on	No Argument								-	-
CMD1	13h	-	W	Normal display mode on	No Argument								-	-
CMD1	20h	-	W	Display inversion off	No Argument								-	-
CMD1	21h	-	W	Display inversion on	No Argument								-	-
CMD1	22h	-	W	All pixel off	No Argument								-	-
CMD1	23h	-	W	All pixel on	No Argument								-	-
CMD1	28h	-	W	Display off	No Argument								-	-
CMD1	29h	-	W	Display on	No Argument								-	-
CMD1	2Ah	1st	W	Set column start address	SC[9:8]								00h	-
CMD1		2nd	W		SC[7:0]								00h	-
CMD1		3rd	W		EC[9:8]								01h	-
CMD1		4th	W		EC[7:0]								8Fh	-
CMD1	2Bh	1st	W	Set row start address	SP[9:8]								00h	-
CMD1		2nd	W		SP[7:0]								00h	-
CMD1		3rd	W		EP[9:8]								01h	-
CMD1		4th	W		EP[7:0]								8Fh	-
CMD1	2Ch	-	W	Memory write	No Argument								-	-
CMD1	2Eh	-	W	Memory read	No Argument								-	-
CMD1	30h	1st	W	Partial area	SR[9:8]								00h	-
CMD1		2nd	W		SR[7:0]								00h	-
CMD1		3rd	W		ER[9:8]								01h	-
CMD1		4th	W		ER[7:0]								8Fh	-
CMD1	31h	1st	W	Vertical partial area	PSC[9:8]								00h	-
CMD1		2nd	W		PSC[7:0]								00h	-
CMD1		3rd	W		PEC[9:8]								01h	-
CMD1		4th	W		PEC[7:0]								8Fh	-
CMD1	34h	-	W	Tearing effect line off	No Argument								-	-
CMD1	35h	-	W	Tearing effect line on	0	0	0	0	0	0	0	TELOM	00h	-
CMD1	36h	-	W	Scan direction control	MADCTR[7:0]								00h	-
CMD1	38h	-	W	Idle mode off	No Argument								-	-
CMD1	39h	-	W	Enter idle mode	No Argument								-	-
CMD1	3Ah	-	W	Interface Pixel Format	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77h	-
CMD1	3Ch	-	W	Memory Continuous Write	No Argument								-	-
CMD1	3Eh	-	W	Memory Continuous Read	No Argument								-	-
CMD1	44h	1st	W	Set tear scan-line	STS[15:8]								00h	-

CMD1		2nd	W		STS[7:0]								00h	-
CMD1	45h	1st	R	Get scan line	GTS[15:8]								00h	-
CMD1		2nd	R		GTS[7:0]								00h	-
CMD1	4Fh	-	W	Deep standby	0	0	0	0	0	0	0	DSTB	00h	-
CMD1	51h	-	W	Write display brightness	DBV[7:0]								FFh	-
CMD1	52h	-	R	Read display brightness	DBV[7:0]								FFh	-
CMD1	53h	-	W	Write CTRL display	0	0	BCTRL	0	DD	0	0	0	28h	-
CMD1	54h	-	R	Read CTRL display	0	0	BCTRL	0	DD	0	0	0	28h	-
CMD1	58h	-	W	Set color enhancement	0	0	0	0	0	SLR_EN	SLR_LEVEL1	SLR_LEVEL0	00h	-
CMD1	59h	-	R	Read color enhancement	0	0	0	0	0	SLR_EN	SLR_LEVEL1	SLR_LEVEL0	00h	-
CMD1	5Ah	-	W	Set color enhancement1	SLR_AMBI_IN7	SLR_AMBI_IN6	SLR_AMBI_IN5	SLR_AMBI_IN4-	SLR_AMBI_IN3	SLR_AMBI_IN2	SLR_AMBI_IN1	SLR_AMBI_IN0	00h	-
CMD1	5Bh	-	R	Read color enhancement1	SLR_AMBI_IN7	SLR_AMBI_IN6	SLR_AMBI_IN5	SLR_AMBI_IN4-	SLR_AMBI_IN3	SLR_AMBI_IN2	SLR_AMBI_IN1	SLR_AMBI_IN0	00h	-
CMD1	A1h	1st	R	Read DDB	SID[7:0]								D0h	-
CMD1		2nd	R		SID[15:8]								01h	-
CMD1		3rd	R		MID[7:0]								80h	-
CMD1		4th	R		MID[15:8]								90h	-
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-
CMD1	A8h	1st	R	Read DDB Continuous	SID[7:0]								D0h	-
CMD1		2nd	R		SID[15:8]								01h	-
CMD1		3rd	R		MID[7:0]								80h	-
CMD1		4th	R		MID[15:8]								90h	-
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-
CMD1	AAh	-	R	Read first checksum	FCS[7:0]								00h	-
CMD1	AFh	-	R	Read continuous checksum	CCS[7:0]								00h	-
	C2h			Set_DSI Mode	0	0	0	0	0	0	DM1	DM0	00h	-
	C4h			Set_DSPI Mode	0	0	DSPI_CFG1	DSPI_CFG0	0	0	0	DSPI_EN	00h	-
CMD1	DAh	-	R	Read display identification information (the same as 04h)	ID1[7:0]								00h	-
CMD1	DBh	-	R		ID2[7:0]								80h	-
CMD1	DCh	-	R		ID3[7:0]								00h	-
CMD1	FEh	-	W	Write CMD mode page	0	0	0	0	CMD_Page[3:0]				00h	-
CMD1	FFh	-	R	Read CMD page Status	0	0	0	0	CMD_Status[3:0]				00h	-

6.2 Command Description

NOP (0000h)

0000H	NOP (No Operation)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
NOP	W	00h	0000h	No Argument									
Description	This command is an empty command; it does not have any effect on the display module. X = Don't care.												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**N/A**
SW Reset	**N/A**
HW Reset	**N/A**

Flow Chart: None

SWRESET(0100h) : Software Reset

0100H	SWRESET(Software Reset)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SWRESET	W	01h	0100h	No Argument									
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)												
Restriction	Software Reset Command cannot be sent during Sleep Out sequence. Any new command cannot be sent for 10-frame period until the RM67160 enters Sleep-In mode. Do not send any command.												

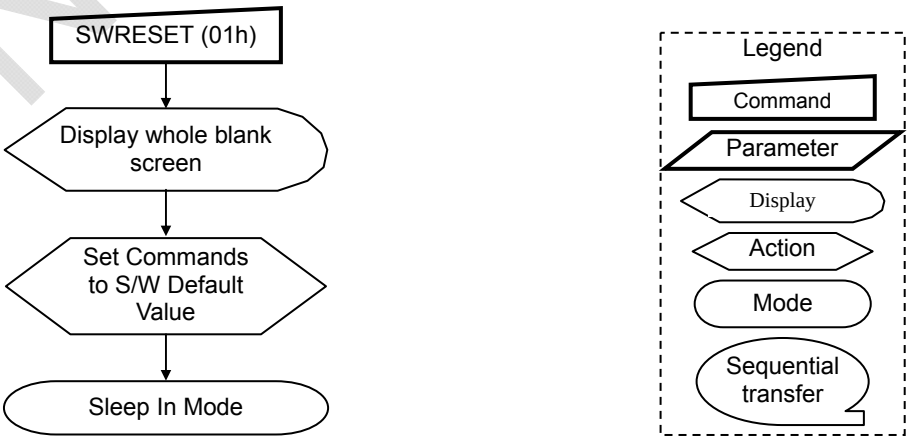
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**N/A**
SW Reset	**N/A**
HW Reset	**N/A**

Flow Chart



RDDID(0400h~0402h) : Read Display ID

0400H	RDDID												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDID	R	04h	0400h	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
			0401h	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80
			0402h	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	The 1st parameter (ID1): the Module's manufacture ID The 2nd parameter (ID2): the Module/driver version ID The 3rd parameter (ID3): the Module/driver ID Note: Commands RDID1/2/3 (DAh/DBh/DCh) read data correspond to the parameter 1, 2, 3 of command 04h, respectively.												
Restriction	-												

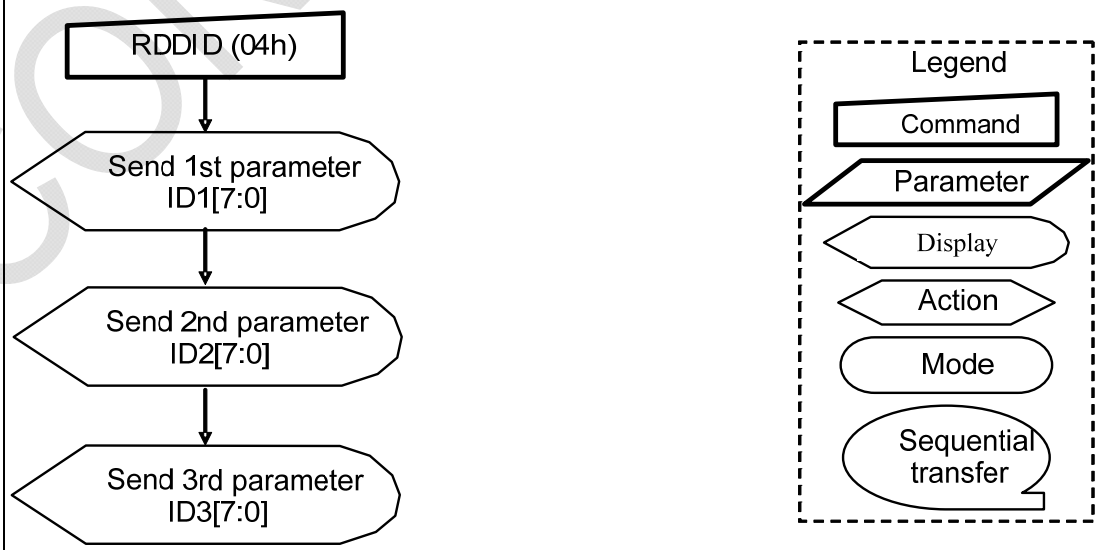
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	**MTP value**	**ID1=00h / ID2=80h / ID3=00h**
SW Reset	**MTP value**	**ID1=00h / ID2=80h / ID3=00h**
HW Reset	**MTP value**	**ID1=00h / ID2=80h / ID3=00h**

Flow Chart



RDNUMED(0500h) : Read Number of Errors on DSI

0500H	RDNUMED											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDNUMED	R	05h	0500h	x	D7	D6	D5	D4	D3	D2	D1	D0	00
Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. D[6..0] bits are telling a number of the parity errors. D[7] is set to “1” if there is overflow with D[6..0] bits. D[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed). This command is used for MIPI DSI only. It is no function for others interface operation.											
Restriction	-											

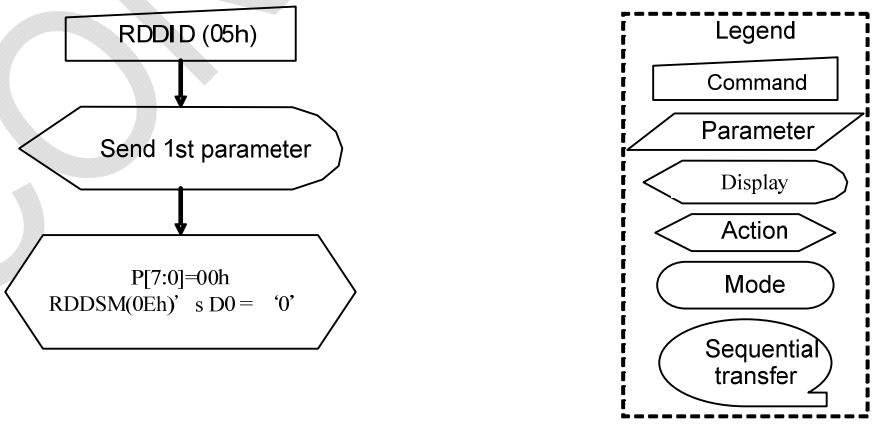
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow Chart



RDDPM (0A00h) : Read Display Power Mode

0A00H	RDDPM (Read Display Power Mode)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDPM	R	0Ah	0A00h	x	D7	D6	D5	D4	D3	D2	D1	D0	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D7	BSTON	Booster Voltage Status	'1'=Booster on, '0'=Booster off
D6	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
D5	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
D4	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
D3	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
D2	DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Reserved		0
D0	Reserved		0

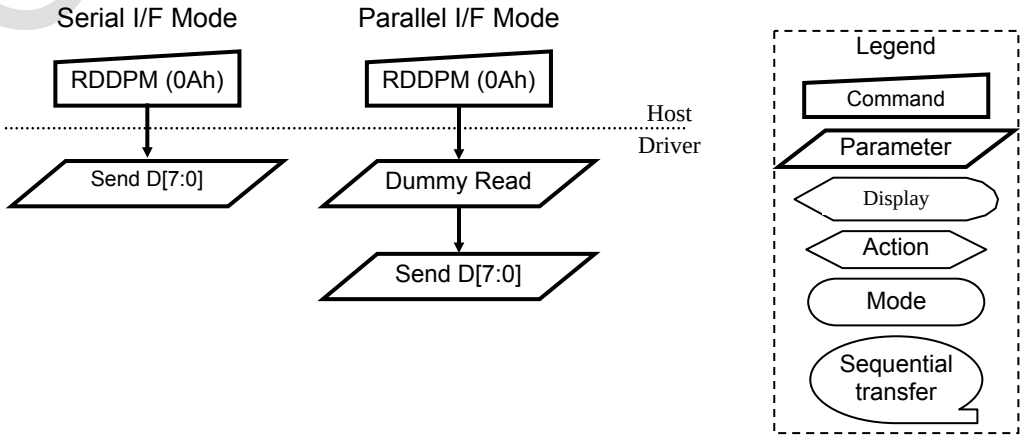
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



RDDMADCTR (0B00h): Read Display MADCTR

0B00H	RDDMADCTR (Read Display MADCTR)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDMADCTR	R	0Bh	0B00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D7	MY	Row Address Increment	0: Increasing in vertical 1: Decreasing in vertical
D6	MX	Column Address Increment	0: Increasing in horizontal 1: Increasing in horizontal
D5	MV	Row/Column Order (MV)	0: Row/column exchange 1: Normal
D4	ML	Vertical Refresh Order	0: LCD Refresh Top to Bottom 1: LCD Refresh Bottom to Top
D3	RGB	RGB/BGR Order	‘1’ =BGR, “0”=RGB
D2	Reserved		0
D1	RSMX	Horizontal Flip	‘0’ = Normal display(36H-D1=’0’) ‘1’ = Flipped display(36H-D1=’1’)
D0	RSMY	Vertical Flip	‘0’ = Normal display(36H-D0=’0’) ‘1’ = Flipped display(36H-D0=’1’)

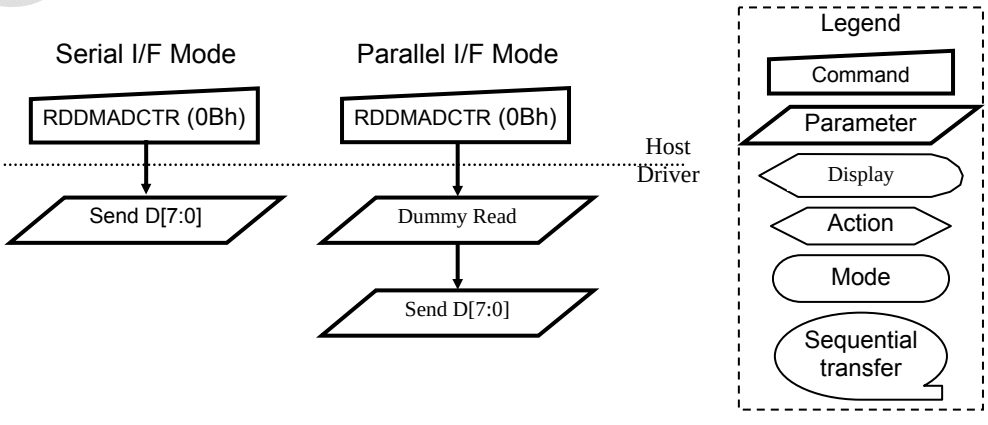
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow Chart



RDDCOLMOD (0C00h): Read Display Pixel Format

0C00H	RDDCOLMOD (Read Display Pixel Format)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDCOLMOD	R	0Ch	0C00h	x	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D2	IFPF[2]	DBI Pixel Format(Control Interface Color Format)	'101' = 16-bits / pixel, '110' = 18-bits / pixel, '111' = 24-bits / pixel, others are no define
D1	IFPF[1]		
D0	IFPF[0]		

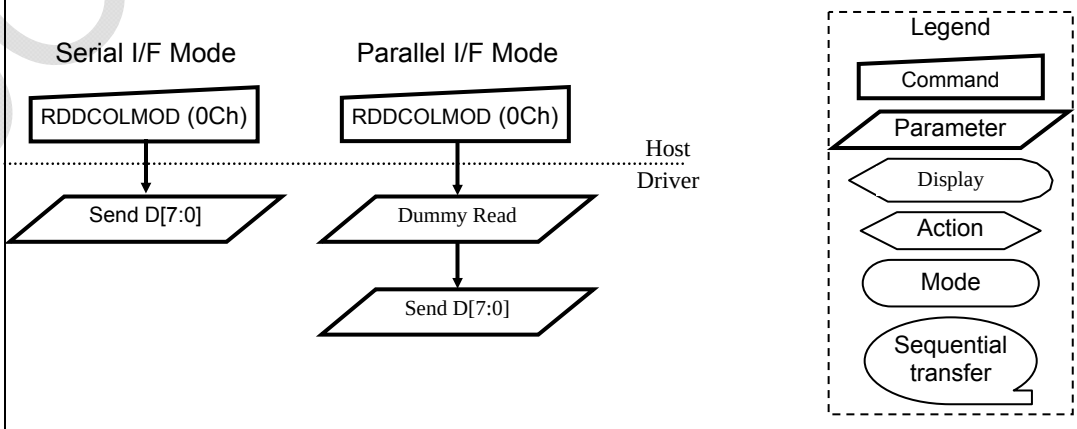
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**77h**
SW Reset	**77h**
HW Reset	**77h**

Flow Chart



RDDIM (0D00h): Read Display Image Mode

0D00H	RDDIM (Read Display Image Mode)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDIM	R	0Dh	0D00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the display image mode status.

Bit	Symbol	Description	Comment
D7	Reserved		'0'
D6	Reserved		'0'
D5	INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	ALLON	All Pixel On	'0' = Normal display '1' = White display
D3	ALLOFF	All Pixel Off	'0' = Normal display '1' = Black display
D2~ D0	Reserved		'000'

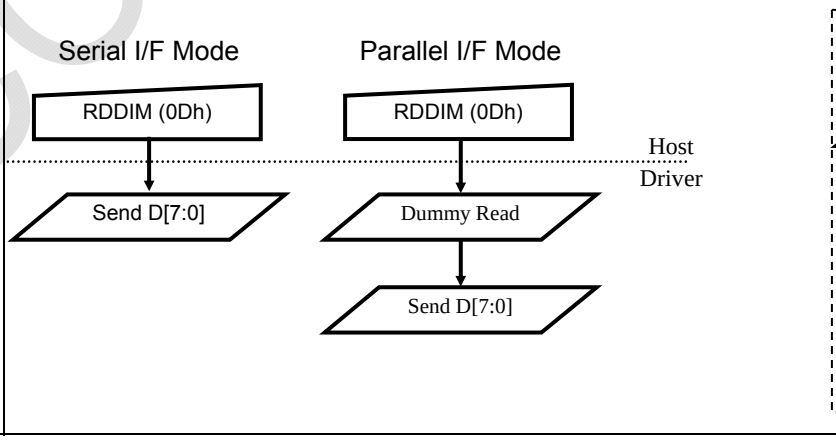
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow Chart



RDDSM (0E00h): Read Display Signal Mode

0E00H	RDDSM (Read Display Signal Mode)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDSM	R	0Eh	0E00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the Display Signal Mode.

Bit	Symbol	Description	Comment
D7	TEON	Tearing Effect Line On/Off	“1” = On, “0” = Off
D6	TELOM	Tearing effect line mode	“0” = mode1, “1” = mode2
D5	Reserved		‘0’
D4	Reserved		‘0’
D3	Reserved		‘0’
D2	Reserved		‘0’
D1	Reserved		‘0’
D0	Error on DSI	Error on DSI	‘0’ = No Error ‘1’ = Error

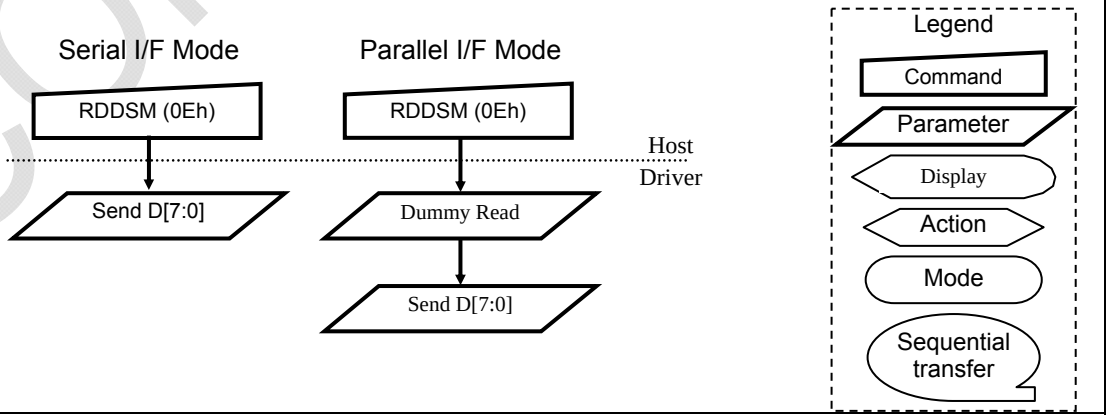
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow Chart



RDDSDR (0F00h): Read Display Self-Diagnostic Result

0F00H	RDDSDR (Read Display Self-Diagnostic Result)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDSDR	R	0Fh	0F00h	x	0	0	0	0	0	0	0	checksum_comp	00

Description

The display module returns the self-diagnostic results following a Sleep Out command.

Bit	Symbol	Description	Comment
D0	Reserved	checksum_comp	'0'

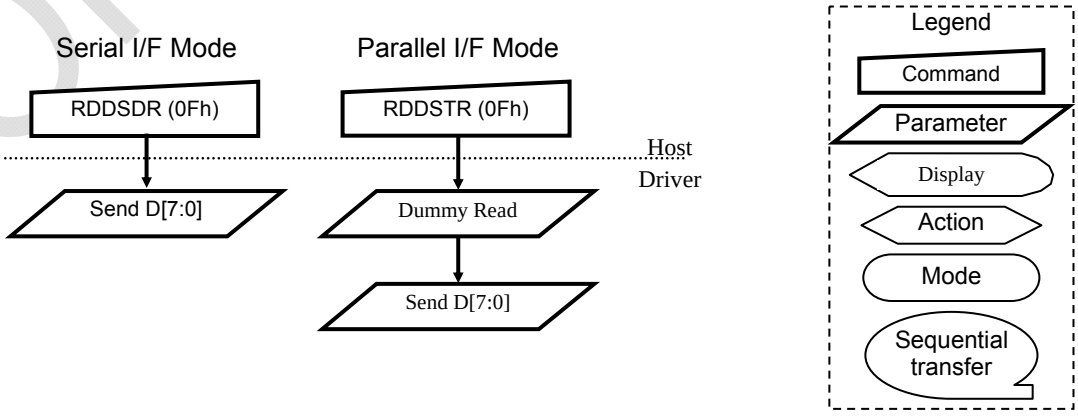
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow Chart



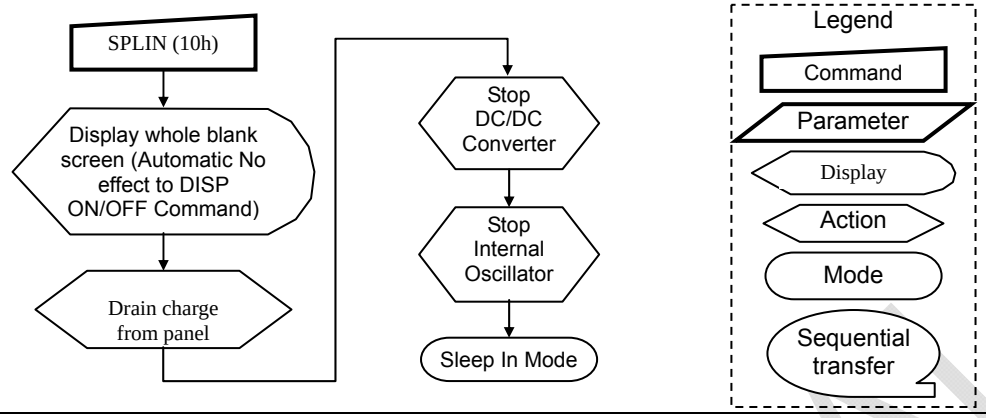
SLPIN (1000h): Sleep In

1000H	SLPIN (Sleep In)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SLPIN	W	10h	1000h	No Argument									
Description	This command causes the display module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. The control Interface such as registers is still working and keeps its values. After Sleep in command, user can send PCLK, HS and VS information on RGB I/F for blank display and this information is valid during 2 frames if there is used Normal Mode On in Sleep Out-mode. There is used an internal oscillator for blank display.											
Restriction	This command has no effect when the display module is already in Sleep mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It must wait 5msec before sending next command for the supply voltages and clock circuits to stabilize. It must wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.											
Register Availability												
Default												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart



SLPOUT (1100h): Sleep Out

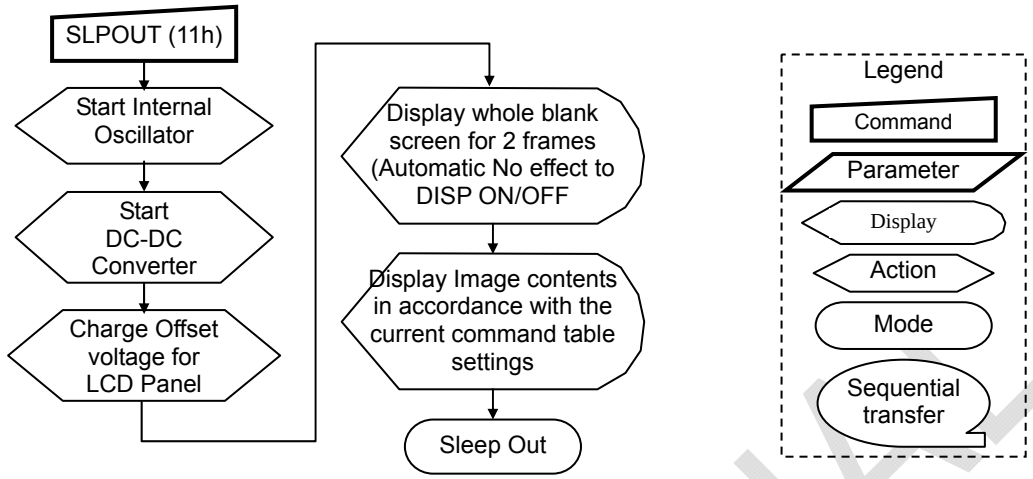
1100H	SLPOUT (Sleep Out)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SLPOUT	W	11h	1100h	No Argument									
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode.												
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow chart



PTLON (1200h): Partial Display Mode On

1200H	PTLON (Partial Display Mode On)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PTLON	W	12h	1200h	No Argument									
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command. To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.												
Restriction	This command has no effect when Partial Display Mode is already active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Normal display mode On
SW Reset	Normal display mode On
HW Reset	Normal display mode On

Flow Chart	Refer to Partial Area (30h)

NORON (1300h): Normal Display Mode On

1300H	NORON (Normal Display Mode On)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
NORON	W	13h	1300h	No Argument									
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode. The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.												
Restriction	This command has no effect when Normal Display mode is already active.												

Register Availability

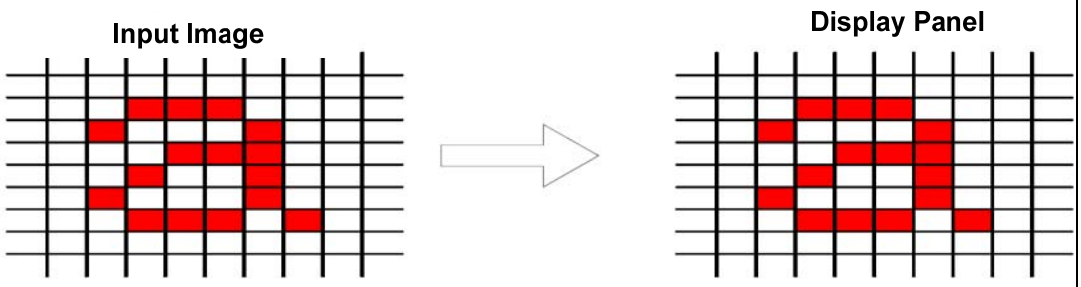
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

Flow Chart: Refer to the description of Partial Area (3000h)

INVOFF (2000H): Display Inversion Off

2000H	INVOFF (Display Inversion Off)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
INVOFF	W	20h	2000h	No Argument									
Description	This command causes the display module to stop inverting the image data on the display device. No status bits are changed. 												
Restriction	This command has no effect when the display module is not inverting the display image.												
Register Availability													

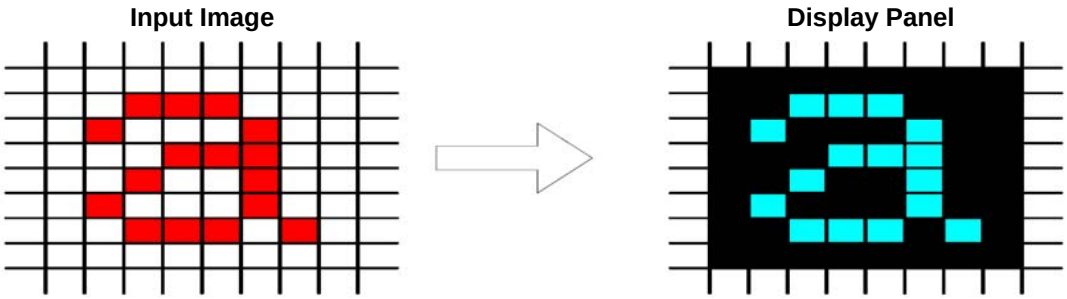
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart

INVON (2100H): Display Inversion On

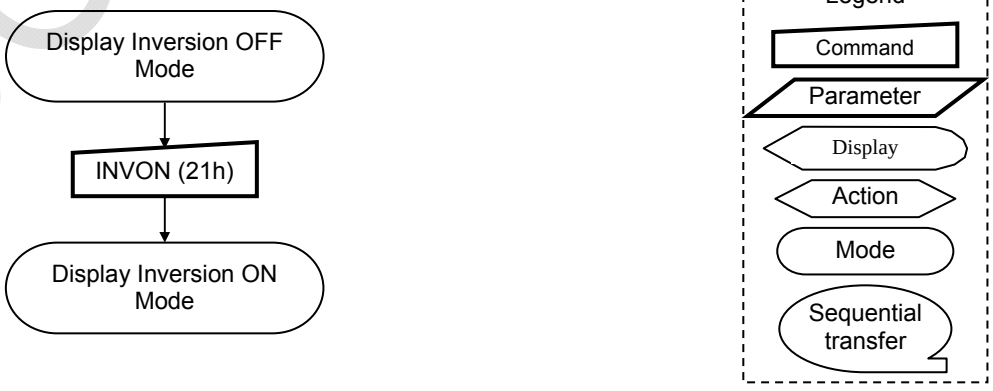
2100H	INVON (Display Inversion On)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
INVON	W	21h	2100h	No Argument									
Description	This command causes the display module to invert the image data only on the display device. No status bits are changed. 												
Restriction	This command has no effect when module is already in inversion on mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

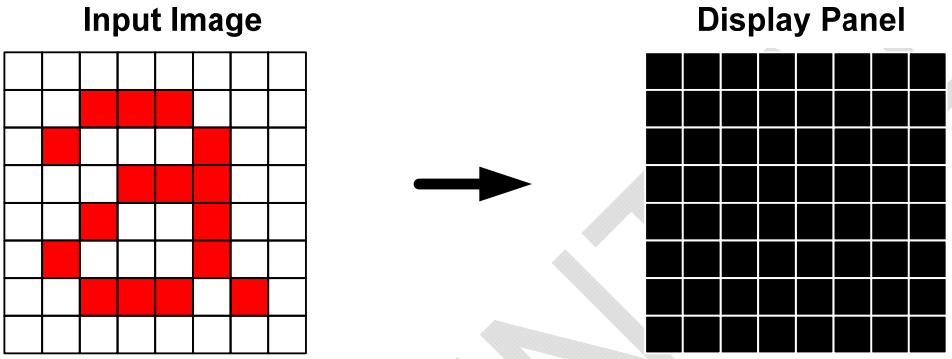
Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart



ALLPOFF (2200H): All Pixel Off

2200H	ALLPOFF											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
ALLPOFF	W	22h	2200h	No Argument									
Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.  "All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the Input Image after "Normal Display On" and "Partial Mode On" commands.											
Restriction	-											
Register Availability												

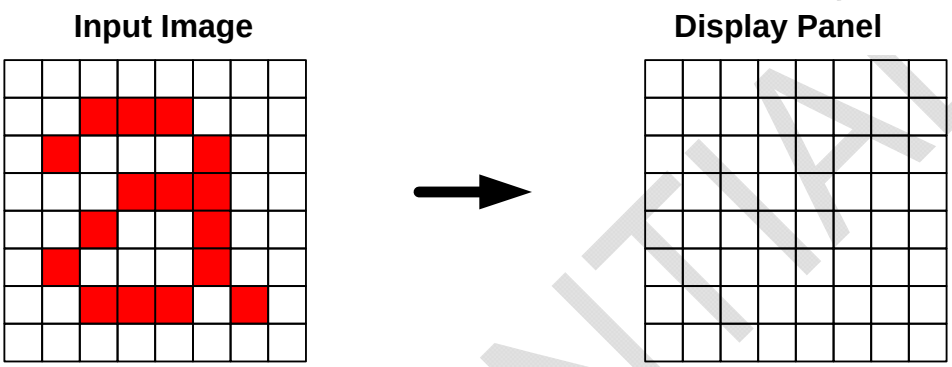
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart	

ALLPON (2300H): All Pixel On

2300H	ALLPON											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
ALLPON	W	23h	2300h	No Argument									
Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.  "All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the Input Image after "Normal Display On" and "Partial Mode On" commands.											
Restriction	-											
Register Availability												

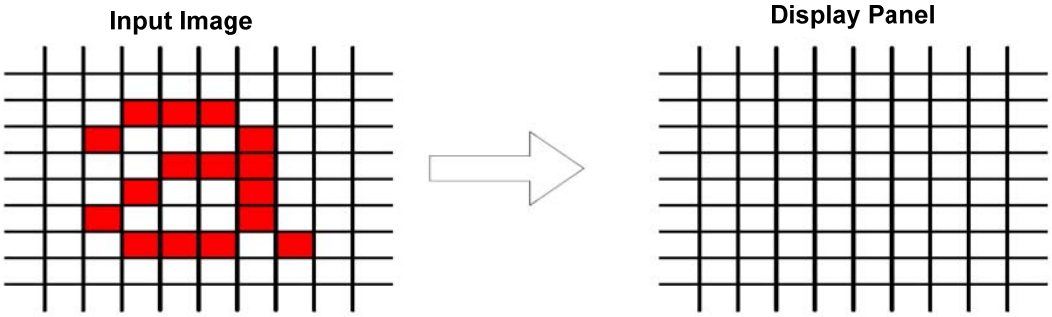
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart	

DISPOFF (2800h): Display Off

2800H	DISPOFF (Display Off)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DISPOFF	W	28h	2800h	No Argument									
Description	This command causes the display module to stop displaying the image data on the display device. No status bits are changed. 												
Restriction	This command has no effect when module is already in display off mode.												

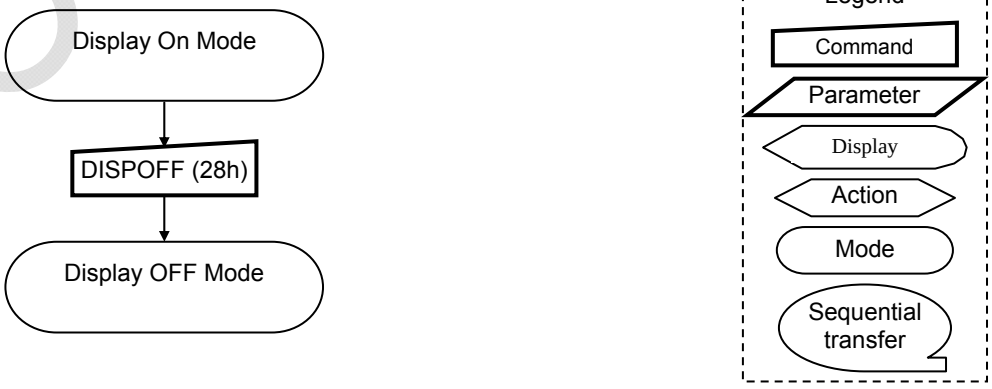
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

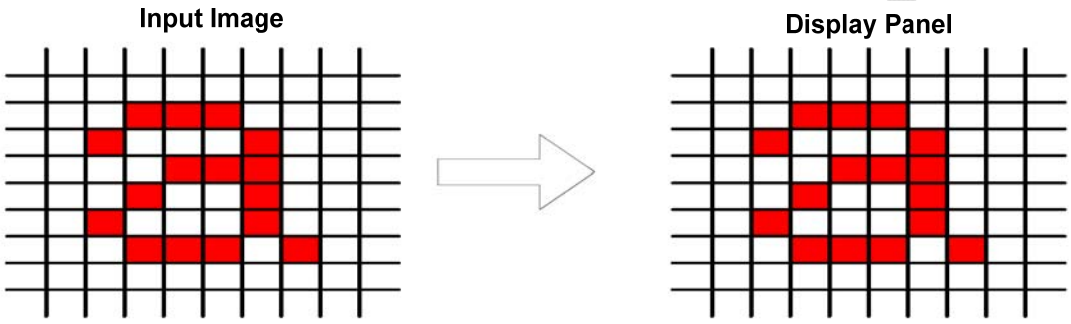
Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart



DISPON (2900h): Display On

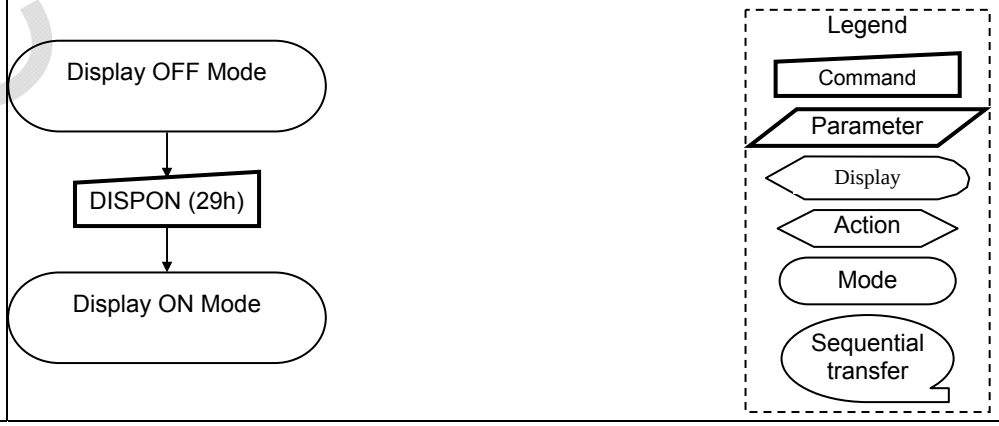
2900H	DISPON (Display On)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DISPON	W	29h	2900h	No Argument									
Description	This command causes the display module to start displaying the image data on the display device. No status bits are changed. 												
Restriction	This command has no effect when module is already in display on mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart

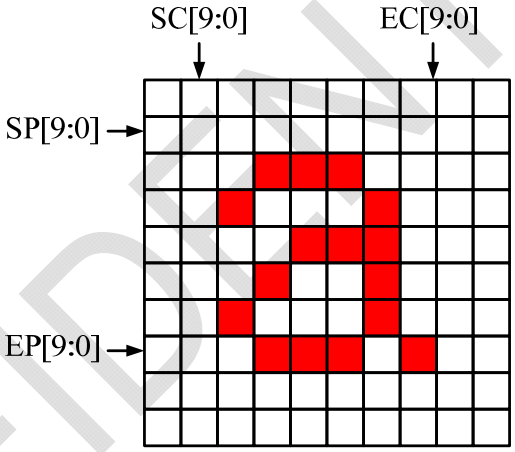


CASET(2A00h~2A03h) : Set Column Start Address

	CASET											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
CASET	W/R	2Ah	2A00h	x	-	-	-	-	-	-	SC9	SC8	00
			2A01h	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
			2A02h	x	-	-	-	-	-	-	EC9	EC8	01
			2A03h	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F

Description

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.
This command makes no change on the other driver status. The values of SC[9:0] and EC[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

(1) SC[9:0] always must be equal to or less than EC[9:0].

(2) The SC[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.

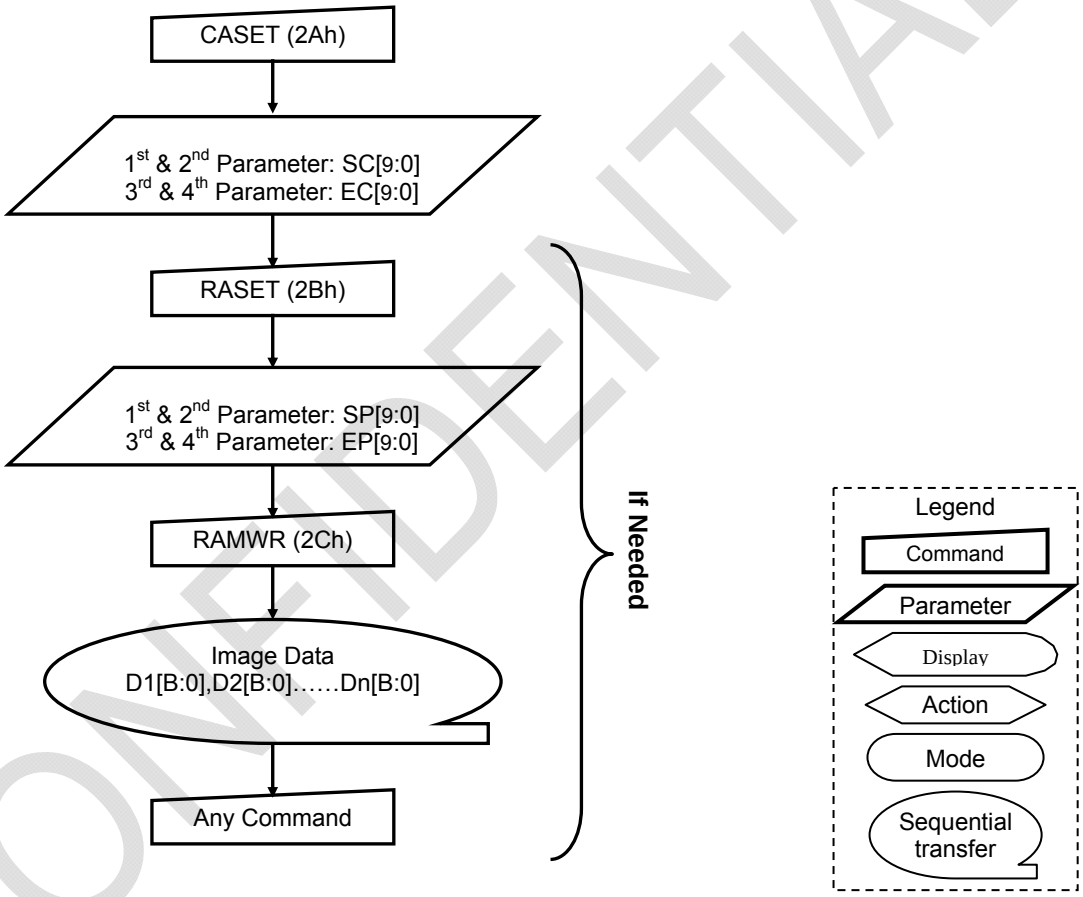
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value	
	SC[9:0]	EC[9:0]
Power On Sequence	0000h	018Fh
SW Reset	0000h	018Fh
HW Reset	0000h	018Fh

Flow Chart

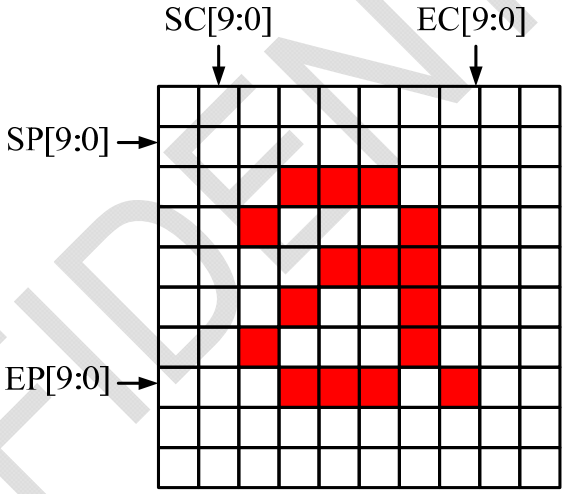


RASET(2B00h~2B03h) : Set Row Start Address

2B00H	RASET											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RASET	W/R	2Bh	2B00h	x	-	-	-	-	-	-	SP9	SP8	00
			2B01h	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
			2B02h	x	-	-	-	-	-	-	EP9	EP8	01
			2B03h	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	8F

Description

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.
This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



Restriction

(1) SP[9:0] always must be equal to or less than EP[9:0]

(2) The SP[9:0] and EP[9:0]-SP[9:0]+1 must can be divisible by 2.

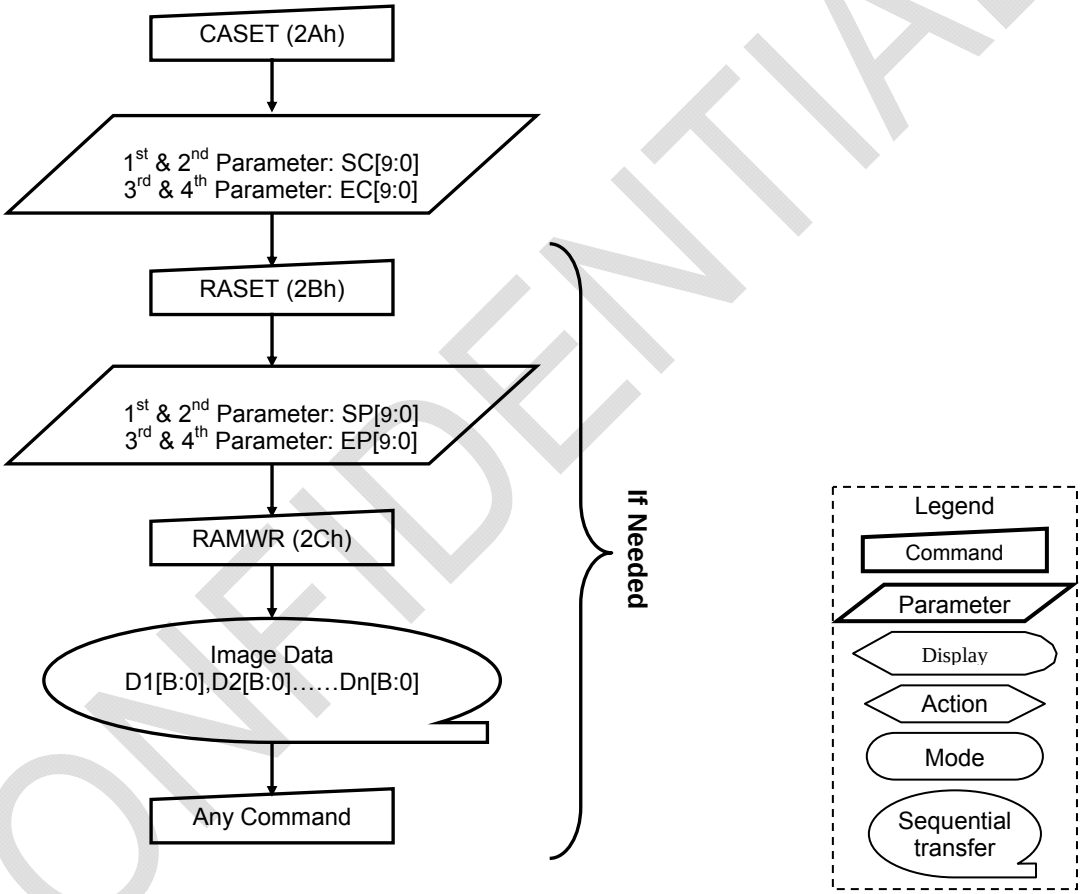
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value	
	SP[9:0]	EP[9:0]
Power On Sequence	0000h	018Fh
SW Reset	0000h	018Fh
HW Reset	0000h	018Fh

Flow Chart



RAMWR (2C00h): Memory Write

2C00H	RAMWR												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RAMWR	R/W	2Ch	2C00h	X	0	0	1	0	1	1	0	0	2C
			1st Pixel	X	$D_1$7	$D_1$6	$D_1$5	$D_1$4	$D_1$3	$D_1$2	$D_1$1	$D_1$0	
			:	X	:	:	:	:	:	:	:	:	
			Nth Pixel	X	D_N7	D_N6	D_N5	D_N4	D_N3	D_N2	D_N1	D_N0	

Description

This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.

If MV(36h-B5) = 0:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If MV(36h-B5) = 1:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command.

Restriction

A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.

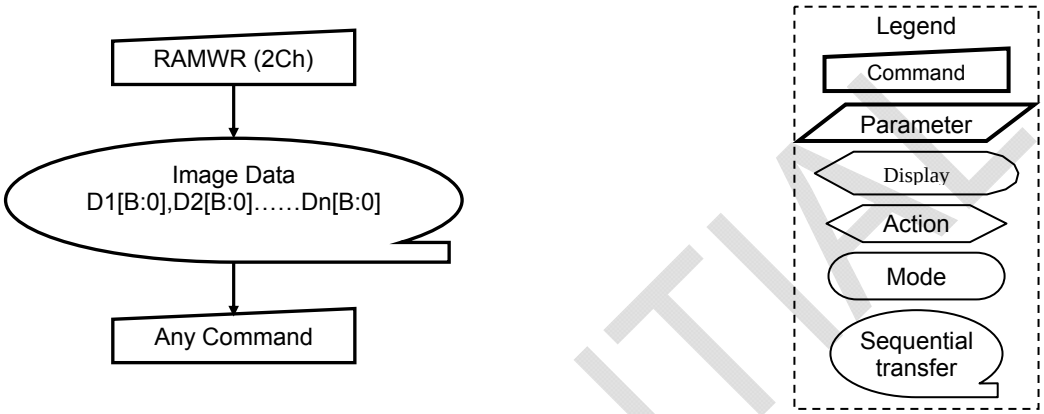
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



RAMRD (2E00h): Memory Read

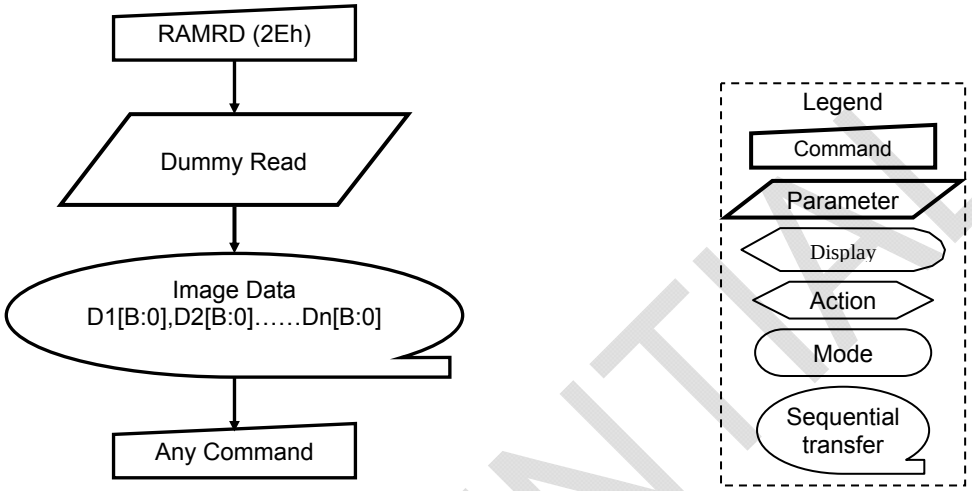
2E00H	RAMRD												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RAMRD	R/W	2Eh	2E00h	X	0	0	1	0	1	1	1	0	2E
			1st Pixel	X	$D_1$7	$D_1$6	$D_1$5	$D_1$4	$D_1$3	$D_1$2	$D_1$1	$D_1$0	
			:	X	:	:	:	:	:	:	:	:	
			Nth Pixel	X	D_N7	D_N6	D_N5	D_N4	D_N3	D_N2	D_N1	D_N0	
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	There is no restriction on length of parameters.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

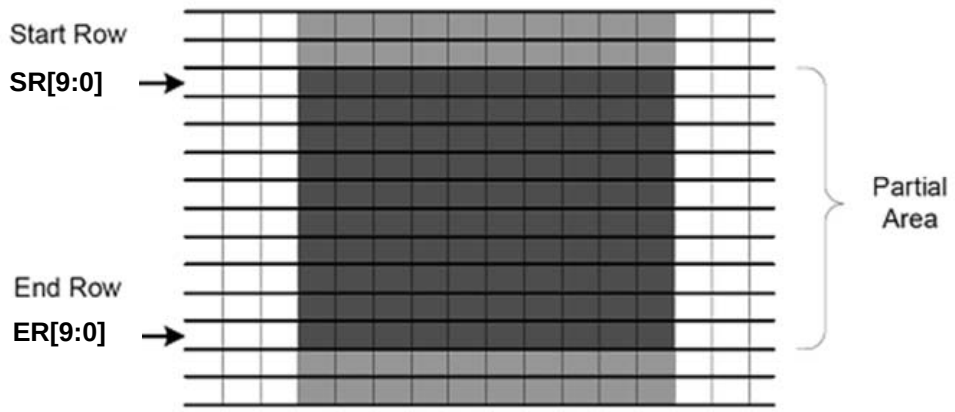
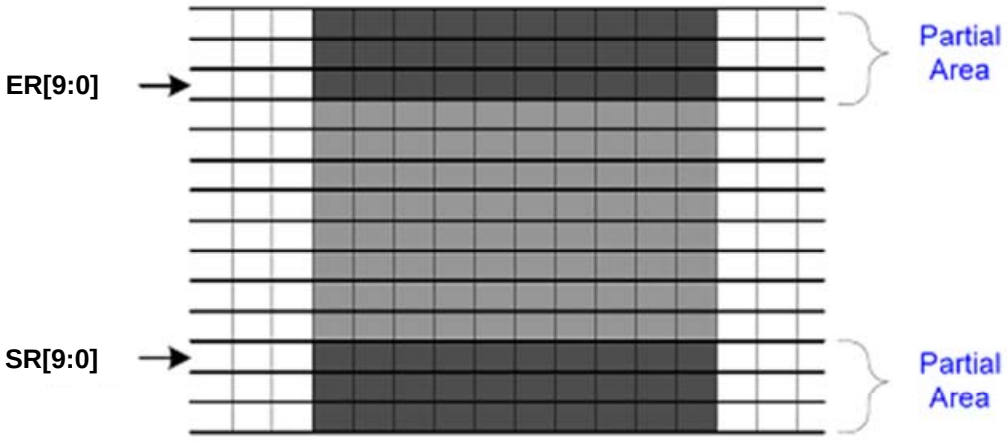
Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



PTLAR (3000h): Partial Area

3000H	PTLAR (Partial Area)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PTLAR	R/W	30h	3000h	x	-	-	-	-	-	-	SR9	SR8	00
			3001h	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
			3002h	x	-	-	-	-	-	-	ER9	ER8	01
			3003h	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	8F
Description	This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. If End Row > Start Row  If End Row < Start Row  If End Row = Start Row then the Partial Area will be one row deep.												
Restriction	SR[9:0] and ER[9:0] settings should be within max available Display Area.												

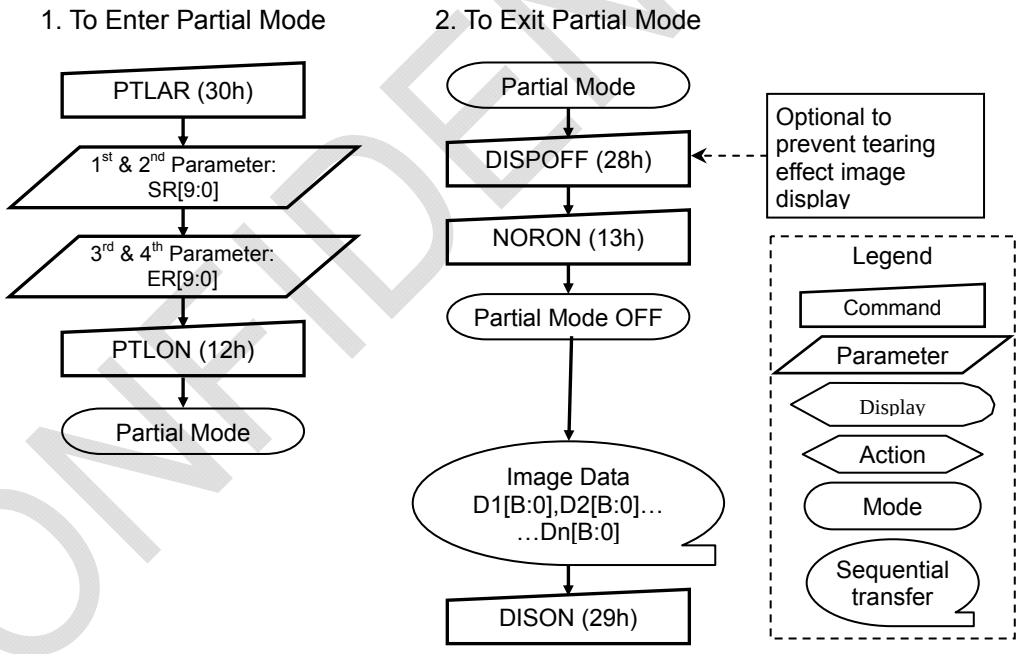
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

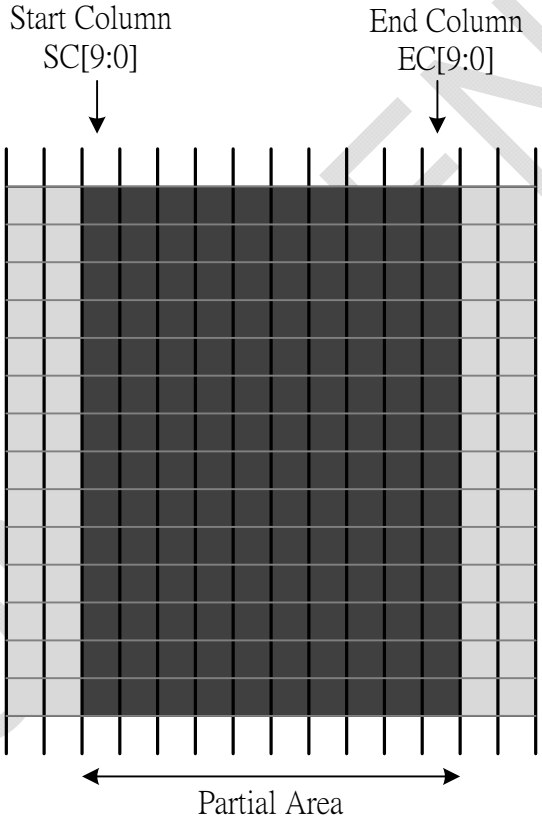
Status	Default Value	
	SR[9:0]	ER[9:0]
Power On Sequence	0000h	018Fh
SW Reset	0000h	018Fh
HW Reset	0000h	018Fh

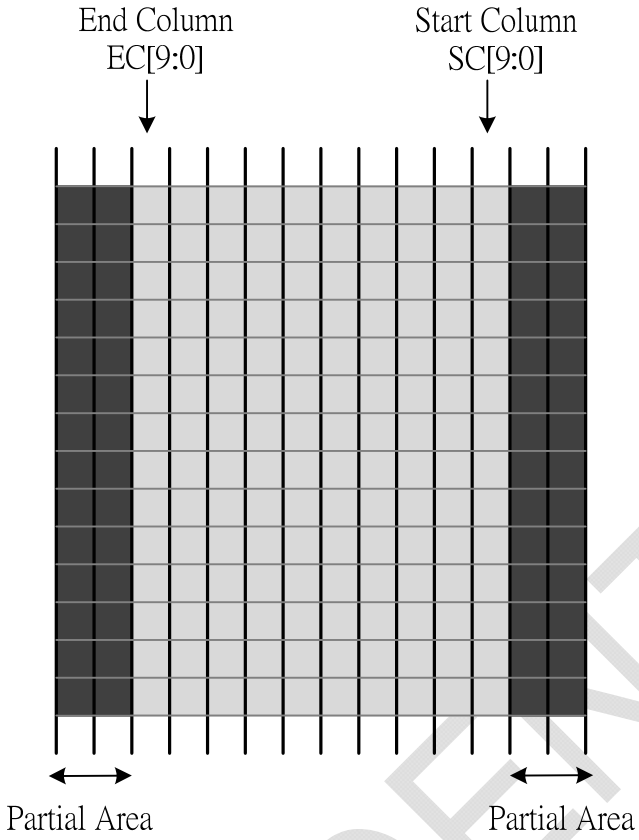
Flow chart



Note : B=23

PTLAR (3100h): Vertical Partial Area

3000H	PTLAR (Partial Area)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PTLAR	R/W	30h	3100h	x	-	-	-	-	-	-	-	SC8	00
			3101h	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
			3102h	x	-	-	-	-	-	-	-	EC8	01
			3103h	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F
Description	This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure. If End Column > Start Column  If End Column < Start Column												



If End Column = Start Column then the Partial Area will be one column deep.

Restriction	SC[9:0] and EC[9:0] settings should be within max available Display Area.

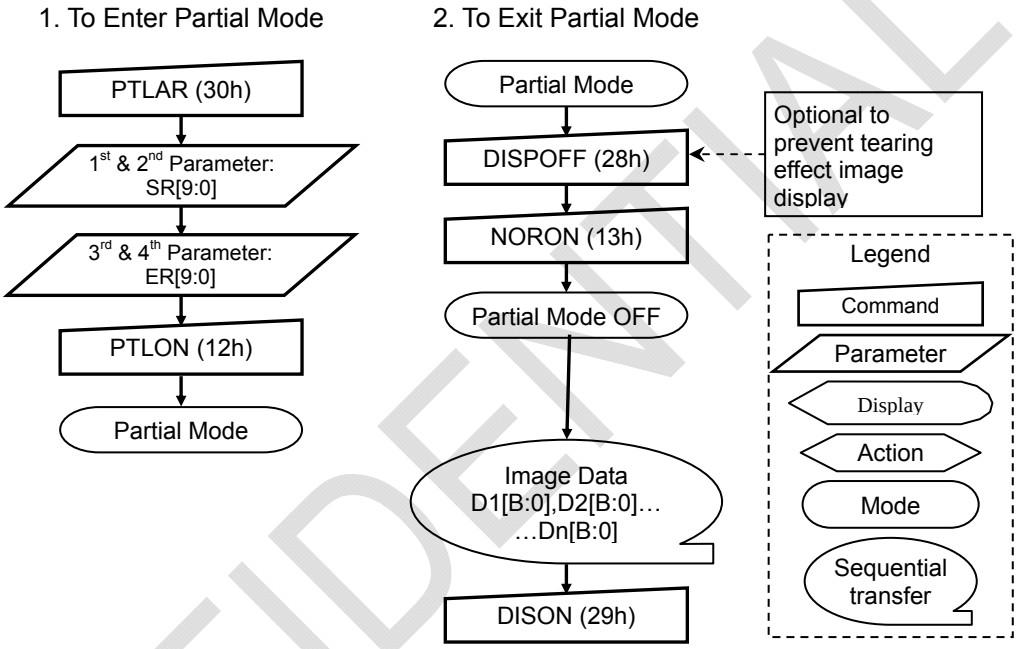
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value	
	SC[9:0]	EC[9:0]
Power On Sequence	0000h	018Fh
SW Reset	0000h	018Fh
HW Reset	0000h	018Fh

Flow chart



Note : B=23

TEOFF (3400h): Tearing Effect Line OFF

3400H	TEOFF (Tearing Effect Line OFF)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
TEOFF	W	34h	3400h	No Argument									
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.												
Restriction	This command has no effect when the Tearing Effect output is already off.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart

TEON (3500h): Tearing Effect Line ON

3500H	TEON (Tearing Effect Line ON)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
TEON	R/W	35h	3500h	x	0	0	0	0	0	0	0	TELOM	00

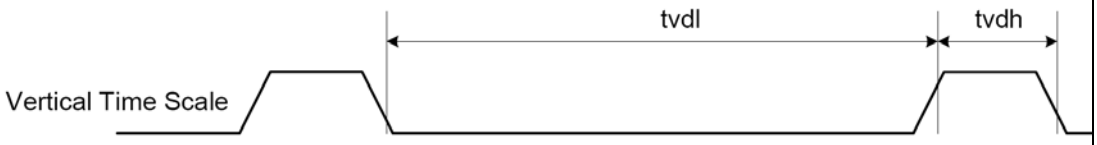
Bit	Symbol	Description	Comment
D0	TELOM	Output mode of TE signal	0:only V-blanking 1:V-blanking +H-blanking

Description

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).
The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.

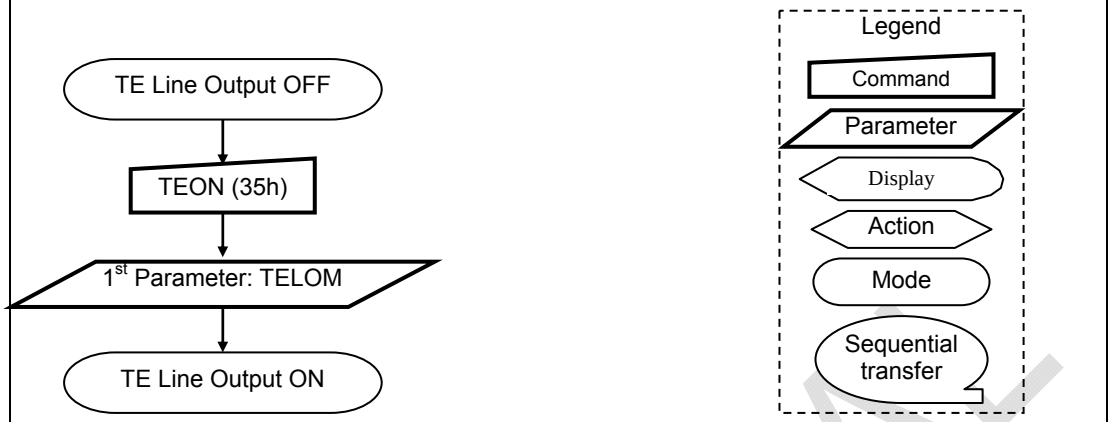


If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

<table>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>OFF</td></tr>
<tr><td>SW Reset</td><td>OFF</td></tr>
<tr><td>HW Reset</td><td>OFF</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

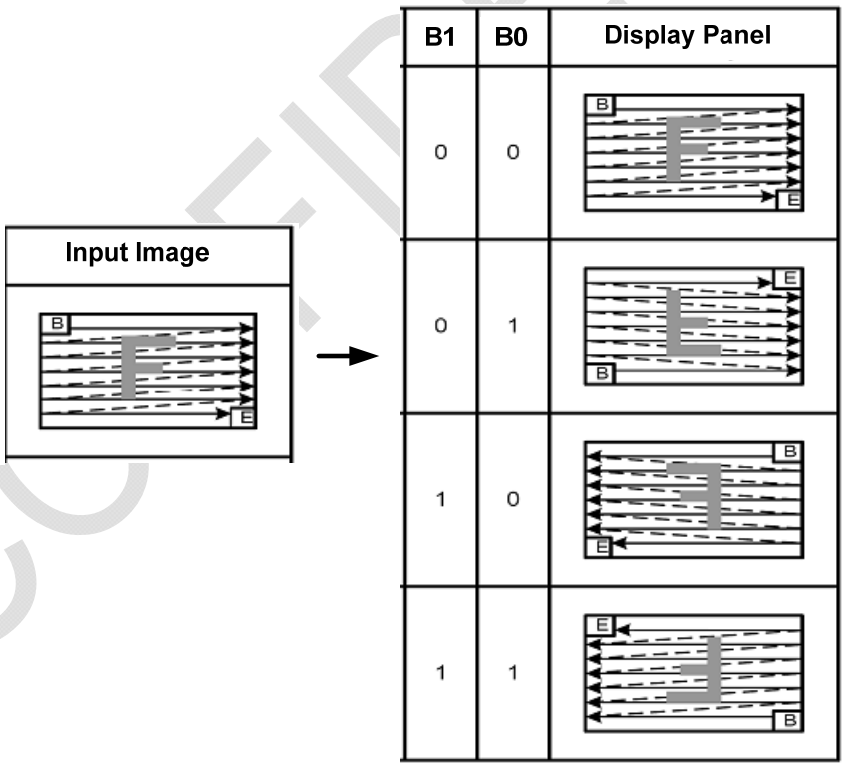
MADCTR (3600h): Scan Direction Control

3600H	MADCTR (Scan Direction Control)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
MADCTR	W	36h	3600h	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.

Bit	Symbol	Description	Comment
D7	MY	Row Address Increment	0: Increasing in vertical 1: Decreasing in vertical
D6	MX	Column Address Increment	0: Increasing in horizontal 1: Increasing in horizontal
D5	MV	Row/Column Order (MV)	0: Row/column exchange 1: Normal
D4	ML	Vertical Refresh Order	0: LCD Refresh Top to Bottom 1: LCD Refresh Bottom to Top
D3	RGB	RGB/BGR Order	‘1’ =BGR, “0”=RGB
D2	Reserved		0
D1	RSMX	Horizontal Flip	‘0’ = Normal display ‘1’ = Flipped display
D0	RSMY	Vertical Flip	‘0’ = Normal display ‘1’ = Flipped display



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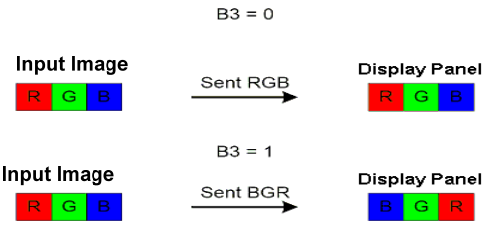
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
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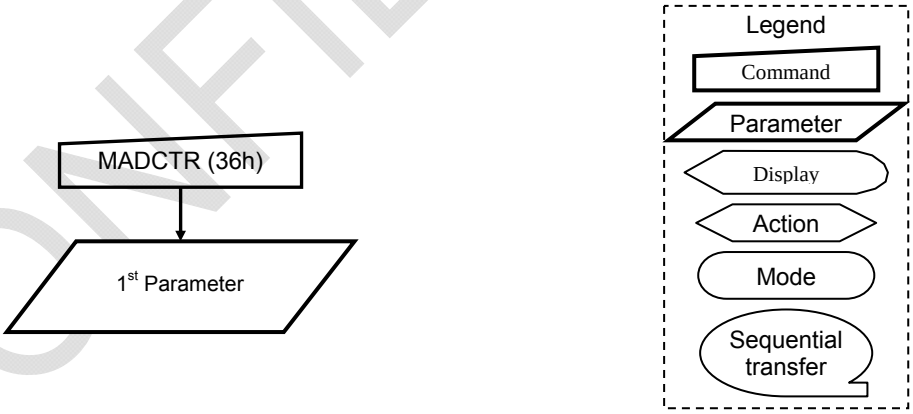
</td></tr>
<tr><td>Flow chart</td><td> 
</td></tr>
</table>

IDMOFF (3800h): Idle Mode Off

3800H	IDMOFF (Idle Mode Off)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
IDMOFF	W	38h	3800h	No Argument									
Description	This command causes the display module to exit Idle mode.												
Restriction	This command has no effect when the display module is not in Idle mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

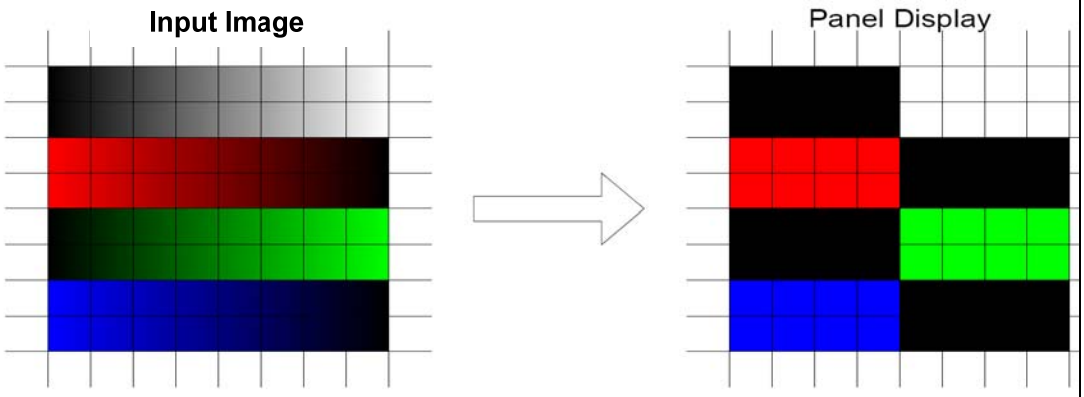
Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart

IDMON (3900h): Enter_idle_mode

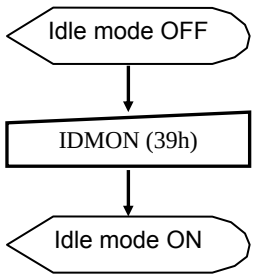
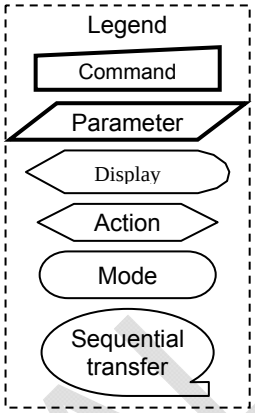
3900H	Enter_idle_mode												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
IDMON	W	39h	3900h	No Argument									
Description	This command causes the display module to enter Idle Mode. In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the Input Image.												
Restriction	This command has no effect when module is already in idle on mode.												
Register Availability													
Default													



Color	R7 R6 R5 R4 R3 R2 R1 R0	G7 G6 G5 G4 G3 G2 G1 G0	B7 B6 B5 B4 B3 B2 B1 B0
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart	 

COLMOD (3A00h): Interface Pixel Format

3A00H	COLMOD (Interface Pixel Format)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
COLMOD	W	3Ah	3A00h	x	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77

Description

This command sets the pixel format for the RGB image data used by the interface.

IFPF[2:0] : MCU Pixel Format Definition.

If not used DPI interface, then the corresponding bits in the parameter are ignored.

Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
24bit/pixel (16.7M colors)	1	1	1

Restriction

-

Register Availability

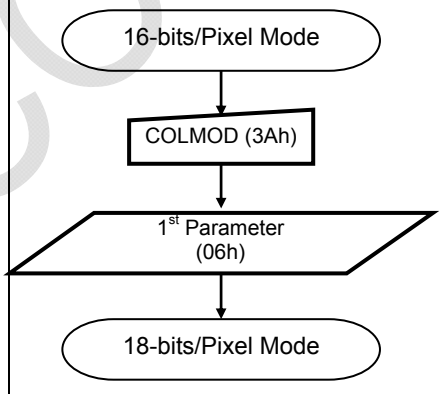
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

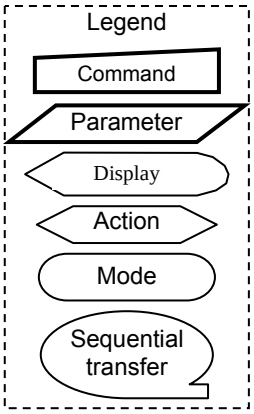
Default

Status	Default Value
Power On Sequence	**77h**
SW Reset	**77h**
HW Reset	**77h**

Flow chart

Example :





RAMWRC (3C00h): Memory Continuous Write

3C00H	RAMWRC												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RAMWR	R/W	3Ch	3C00h	X	0	0	1	1	1	1	0	0	3C
			1st Pixel	X	$D_1$7	$D_1$6	$D_1$5	$D_1$4	$D_1$3	$D_1$2	$D_1$1	$D_1$0	
			:	X	:	:	:	:	:	:	:	:	
			Nth Pixel	X	D_N7	D_N6	D_N5	D_N4	D_N3	D_N2	D_N1	D_N0	
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. If MV(36h-B5) = 0: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.												
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												

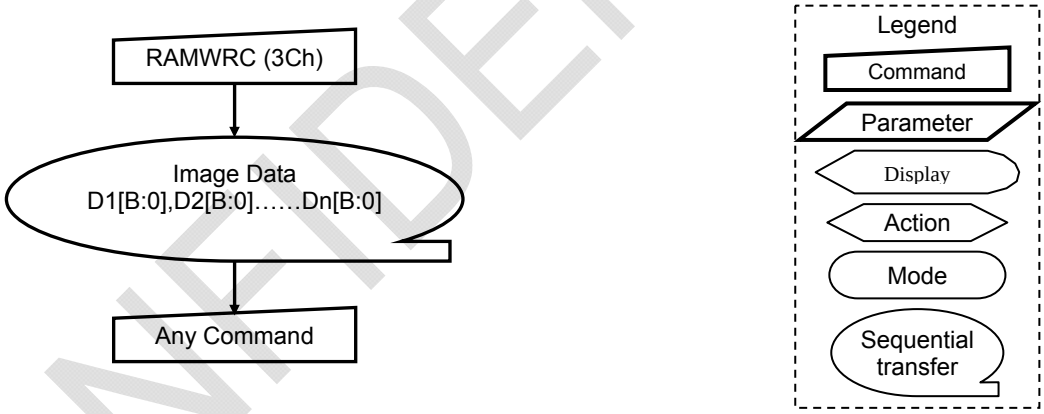
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



RAMRDC (3E00h): Memory Continuous Read

3E00H	RAMRDC												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RAMRDC	R/W	3Eh	3E00h	X	0	0	1	1	1	1	1	0	3E
			1st Pixel	X	$D_1$7	$D_1$6	$D_1$5	$D_1$4	$D_1$3	$D_1$2	$D_1$1	$D_1$0	
			:	X	:	:	:	:	:	:	:	:	
			Nth Pixel	X	D_N7	D_N6	D_N5	D_N4	D_N3	D_N2	D_N1	D_N0	
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. If MV(36h-B5) = 0: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.												
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												

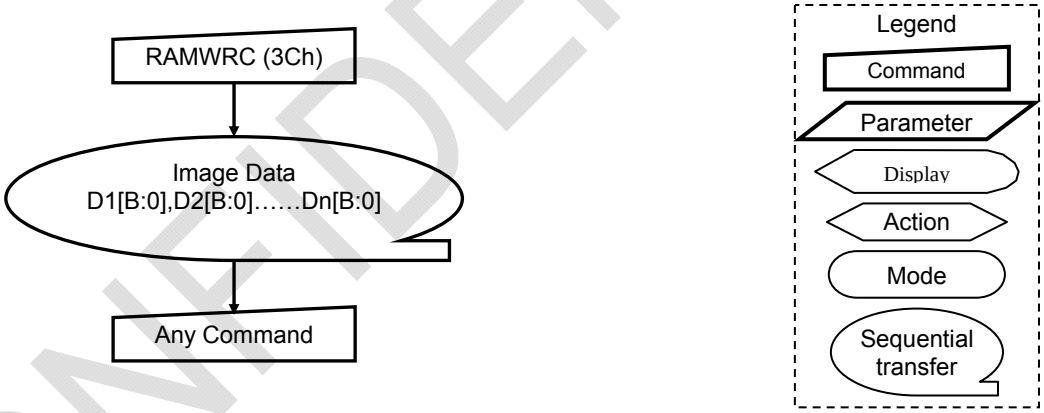
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart

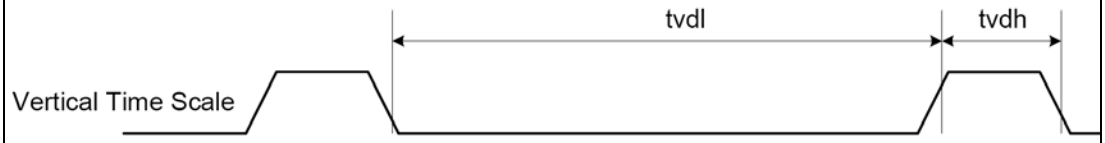


STESL(4400h) : Set_Tear_Scanline

4400H	STESL(Set_Tear_Scanline)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
STESL	W	44h	4400h	x	STS[15]	STS[14]	STS[13]	STS[12]	STS[11]	STS[10]	STS[9]	STS[8]	00
			4401h	x	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

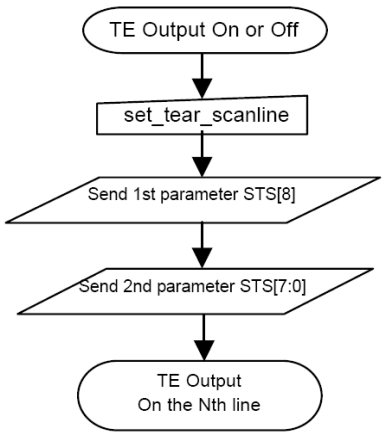
Register Availability

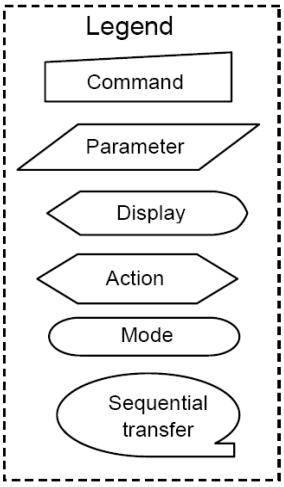
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	STS[15:0]=16'h0000
SW Reset	STS[15:0]=16'h0000
HW Reset	STS[15:0]=16'h0000

Flow Chart



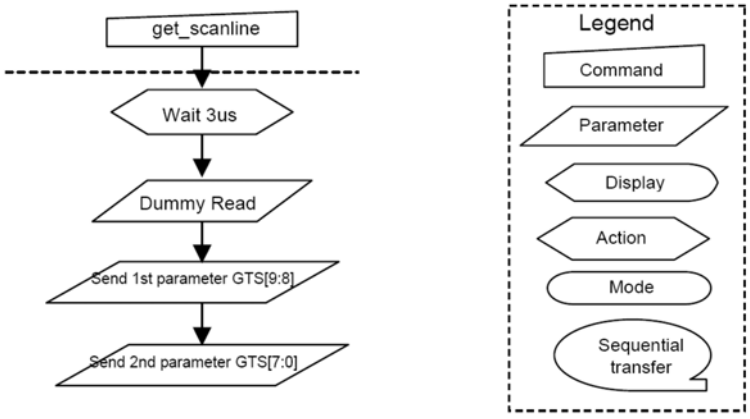


GSL (4500h) : Get_Scanline

4500H	GSL(Get_Scanline)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
GSL	R	45h	4500h	x	GTS[15]	GTS[14]	GTS[13]	GTS[12]	GTS[11]	GTS[10]	GTS[9]	GTS[8]	0x
			4501h	x	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined.												
Restriction	-												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart



DSTBON (4F00h): Deep Standby Mode On

4F00H	DSTBON(Deep Standby Mode On)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DSTBON	W	4Fh	4F00h	x	0	0	0	0	0	0	0	DSTB	00

Description

This command is used to enter deep standby mode.
DSTB="1", enter deep standby mode.
Notes:
1. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX.
2. For MIPI IF, if deep standby mode is used, please pull HSSI_CLK_P/N & HSSI_D0~D1_P/N to GND after executing deep standby command.

Restriction

-

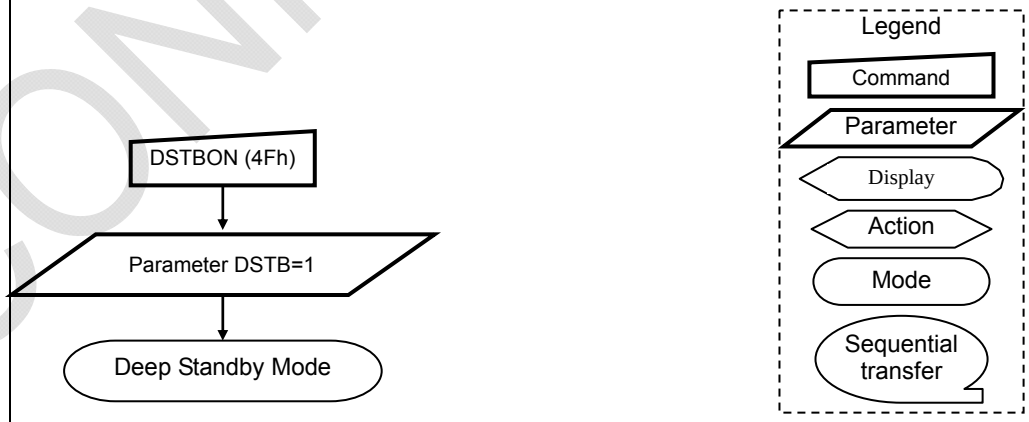
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow chart



WRDISBV (5100h): Write Display Brightness

5100H	WRDISBV											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRDISBV	W	51h	5100h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF

Description

This command is used to adjust brightness value.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

The display supplier cannot use this command for tuning

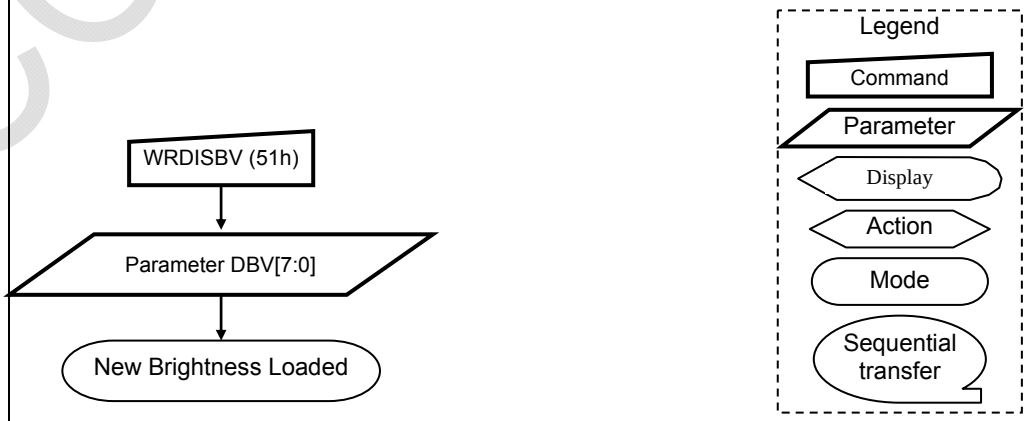
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**FFh**
SW Reset	**FFh**
HW Reset	**FFh**

Flow chart



RDDISBV (5200h): Read Display Brightness

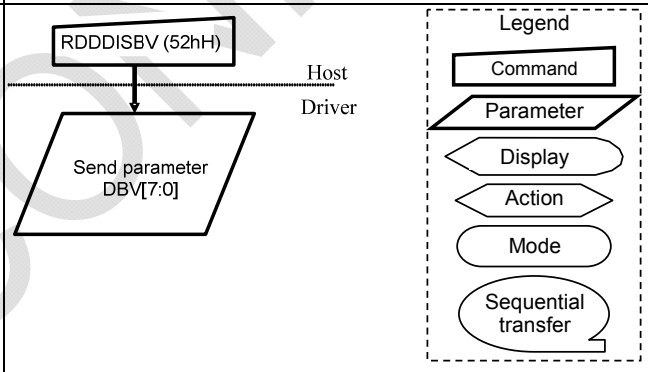
5200H	RDDISBV											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDISBV	R	52h	5200h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF
Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	-												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**FFh**
SW Reset	**FFh**
HW Reset	**FFh**

Flow Chart



WRCTRLD (5300h): Write Display Control

5300H	WRDISBV											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRCTRLD	W	53h	5300h	x	0	0	BCTRL	0	DD	0	0	0	28

Description

BCTRL: Brightness control ,1=enable
DD: Display dimming control ,1=enable

Restriction

The display supplier cannot use this command for tuning

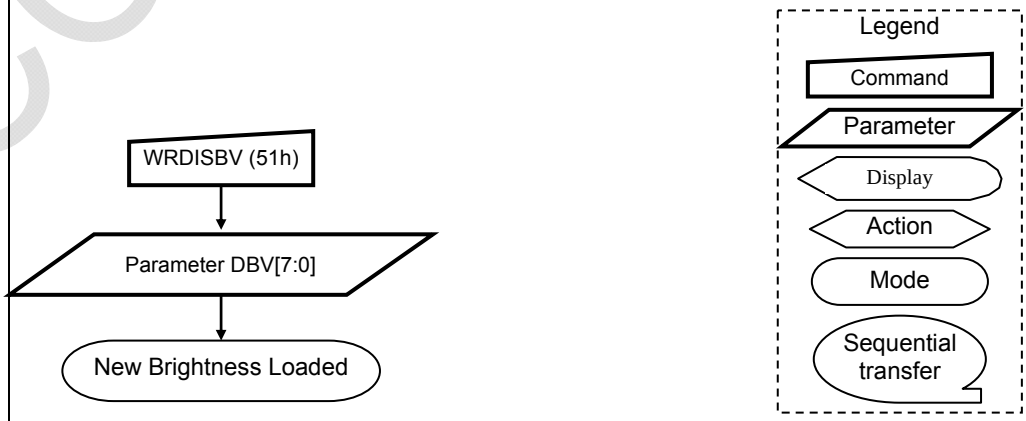
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**28h**
SW Reset	**28h**
HW Reset	**28h**

Flow chart



RDCTRLD (5400h): Read Display Control

5400H	RDDISBV											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDCTRLD	R	54h	5400h	x	0	0	BCTRL	0	DD	0	0	0	28
Description	BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable												
Restriction	-												

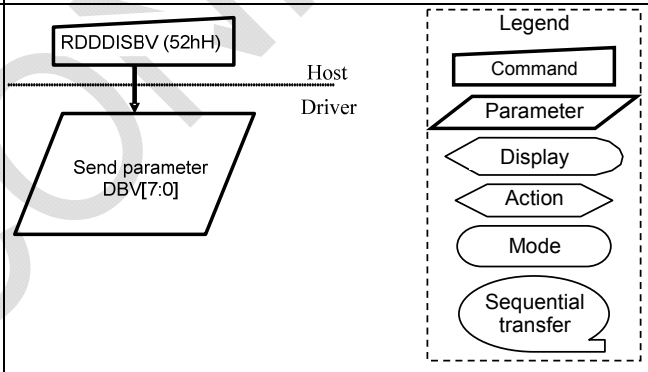
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	**28h**
SW Reset	**28h**
HW Reset	**28h**

Flow Chart



IMGEHCCTR (5800h) : Set_color_enhance

5800H	WRCE (set_color_enhance)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRCE	W	58h	5800h	x	0	0	0	0	0	SLR_EN	SLR_LEVEL1	SLR_LEVEL0	00

Description

Bit	Description	Value
SLR_EN	Sunlight Readable Enhancement Enable	'0' : disable; '1': enable
SLR_LEVEL[1:0]	Sunlight Readable Enhancement Level	0~2, low to high

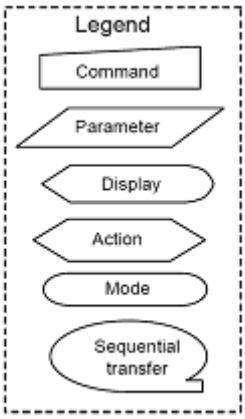
Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart



IMGEHCCTR (5900h) : Read_color_enhance

5900H	RDCE (set_color_enhance)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDCE	R	59h	5900h	x	0	0	0	0	0	SLR_EN	SLR_LEVEL1	SLR_LEVEL0	00

Description

Bit	Description	Value
SLR_EN	Sunlight Readable Enhancement Enable	'0' : disable; '1': enable
SLR_LEVEL[1:0]	Sunlight Readable Enhancement Level	0~2, low to high

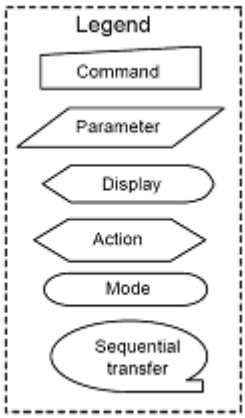
Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart



CESLRCTR (5A00h) : Set_color_enhance1

5A00H	CESLRCTR (set_color_enhance1)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
CESLRCTR	W/R	5Ah	5A00h	x	SLR_AMBI_IN7	SLR_AMBI_IN6	SLR_AMBI_IN5	SLR_AMBI_IN4-	SLR_AMBI_IN3	SLR_AMBI_IN2	SLR_AMBI_IN1	SLR_AMBI_IN0	00

Description

Bit	Description	Value
SLR_AMBI_IN[7:0]	Low byte of ambient light value	00h

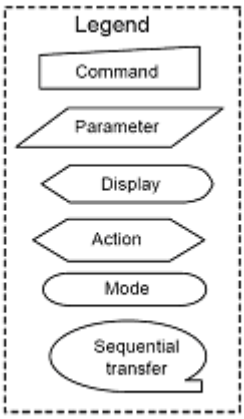
Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart



CESLRCTR (5B00h) : set_color_enhance1

5B00H	CESLRCTR (set_color_enhance1)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
CESLRCTR	W/R	5Bh	5B00h	x	SLR_AMBI_IN15	SLR_AMBI_IN14	SLR_AMBI_IN13	SLR_AMBI_IN12-	SLR_AMBI_IN11	SLR_AMBI_IN10	SLR_AMBI_IN9	SLR_AMBI_IN8	00

Description

Bit	Description	Value
SLR_AMBI_IN[15:8]	High byte of ambient light value	00h

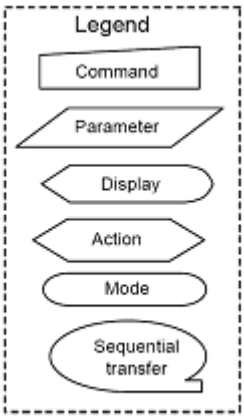
Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart



RDDDBS(A100h) : Read_DDB_Start

A100H	RDDDBS(Read_DDB_Start)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDDBS	R	A1h	A100h	x	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0
			A101h	x	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01
			A102h	x	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80
			A103h	x	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90
			A104h	x	1	1	1	1	1	1	1	1	FF
Description	1st parameter: Supplier ID code 2nd parameter: Supplier ID code 3rd parameter: Module ID 4th parameter: Module ID 5th Exit code (FFh).												
Restriction													

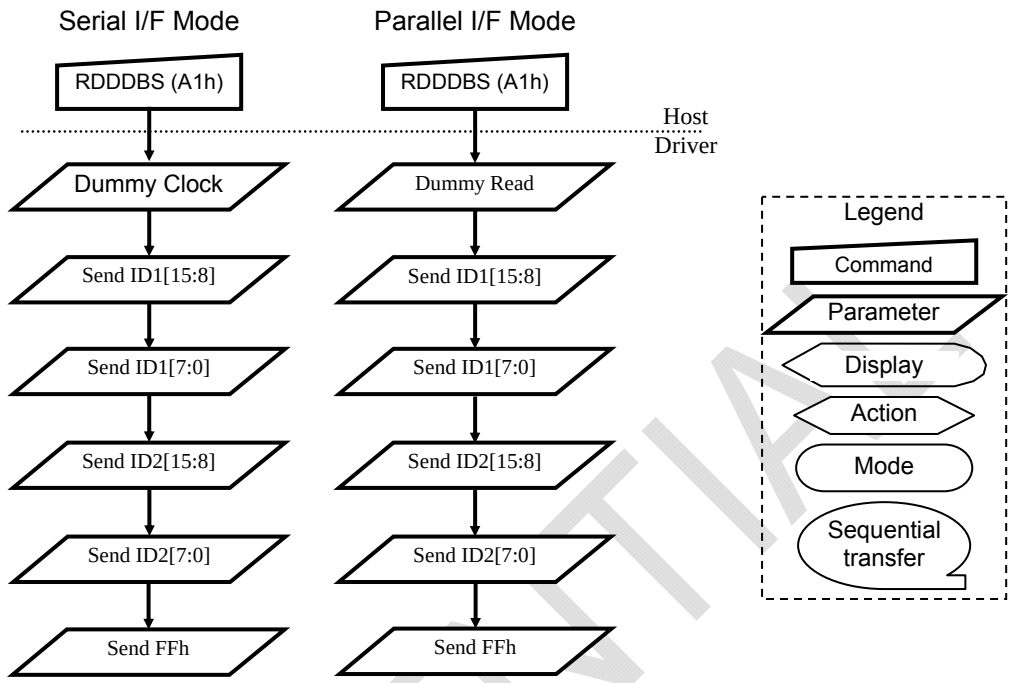
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	01h, D0h, 90h, 60h, FFh
SW Reset	MTP Value	01h, D0h, 90h, 60h, FFh
HW Reset	MTP Value	01h, D0h, 90h, 60h, FFh

Flow Chart



RDDDBC(A800h) : Read DDB Continous

A800H	RDDDBC												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDDBC	R	A8h	A800h	x	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0
			A801h	x	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01
			A802h	x	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80
			A803h	x	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90
			A804h	x	1	1	1	1	1	1	1	1	FF

Description

This command returns the supplier identification and display module mode/revision information from the
point where RDDDBS command was interrupted by an other command.
Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.
Note: For use example,
1. Set maximum return packet size=3
2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]
3. Read 0xA8*, return 2 bytes MID[15:8],RID[7:0], RID[15:8] and 0xFF*

Restriction

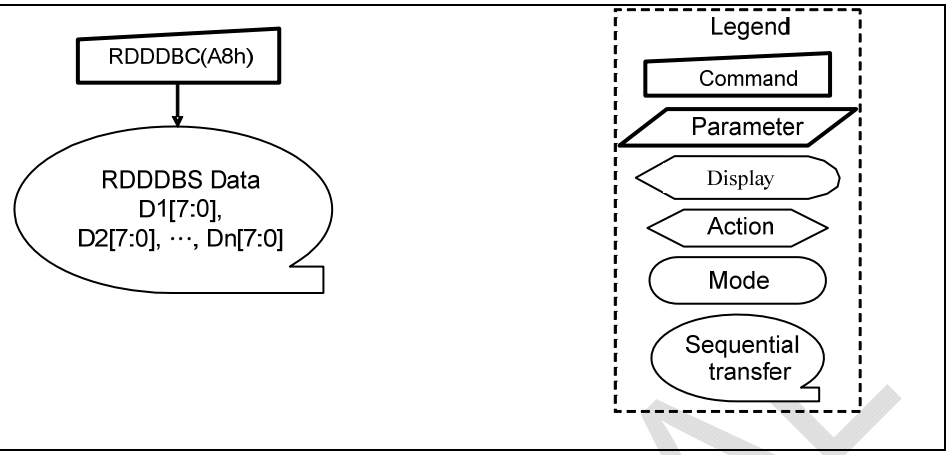
A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue
command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue c ommnd is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	01h, D0h, 90h, 60h, FFh
SW Reset	MTP Value	01h, D0h, 90h, 60h, FFh
HW Reset	MTP Value	01h, D0h, 90h, 60h, FFh

Flow Chart	

RDFCS(AA00h) : Read First Checksum

AA00H	RDFCS												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDFCS	R	AAh	AA00h	x	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00
Description	This command returns the first checksum what has been calculated from “User Command Set” area registers (not include “Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.												

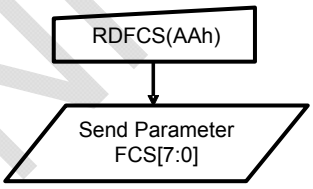
Register Availability

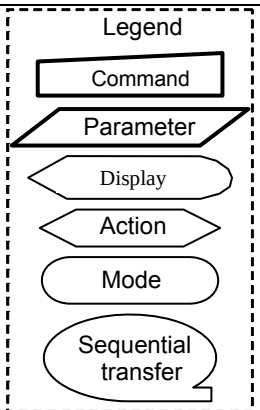
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart





RDCCS(AF00h) : Read Continue Checksum

AF00H	RDCCS												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDCCS	R	AFh	AF00h	x	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time.												

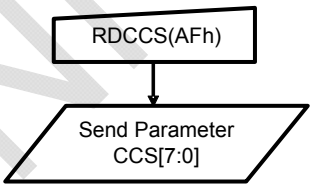
Register Availability

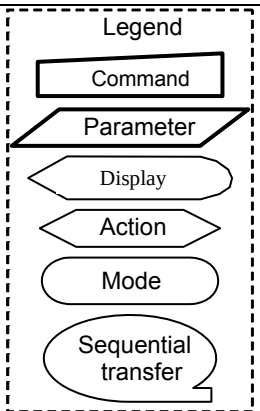
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart





SetDSIMode (C200h) : set_DSI Mode

C200H	SetDSIMode											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SetDSIMode	W/R	C2h	C200h	x	0	0	0	0	0	0	DM1	DM0	00

Description

Bit	Description	Value
DM[1:0]	Display timing mode selection	2'b00: internal timing 2'b01: auto detection internal or external timing 2'b10: reserved 2'b11: external timing

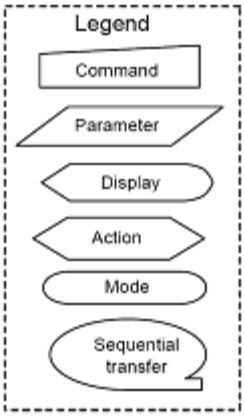
Restriction

Note:
(1) If video mode, need to set DM[1:0] = 2'b01 or 2'b11.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart



SetDSPIMode (C400h) : set_DSPI Mode

C400H	Set DSPI mode											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SetDSPIMode	W/R	C2h	C200h	x	-	-	DSPI_CFG1	DSPI_CFG0	-	-	-	DSPI_EN	00

Description

Bit	Description	Value
DSPI_EN	**DAUL SPI MODE Enable**	0: disable 1: enable
DSPI_CFG[1:0]	DAUL SPI MODE Selection	00: 1P1T for 1 wire 10: 1P1T for 2 wire 11: 2P3T for 2 wire 01: reserved

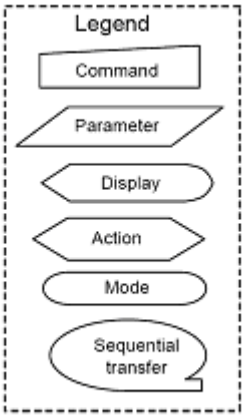
Note: detailed DAUL SPI formats are described at next page.

Restriction

Register Availability

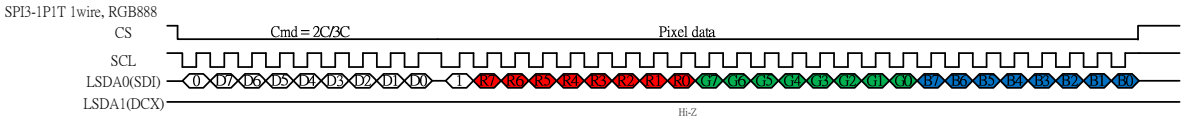
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	**Yes**
Normal Mode On, Idle Mode On, Sleep Out	**Yes**
Partial Mode On, Idle Mode Off, Sleep Out	**Yes**
Partial Mode On, Idle Mode On, Sleep Out	**Yes**
Sleep In	**Yes**

Flow Chart

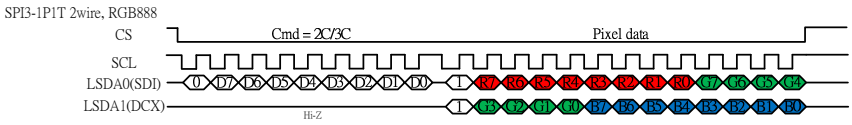


DUAL SPI via SPI3 interface :

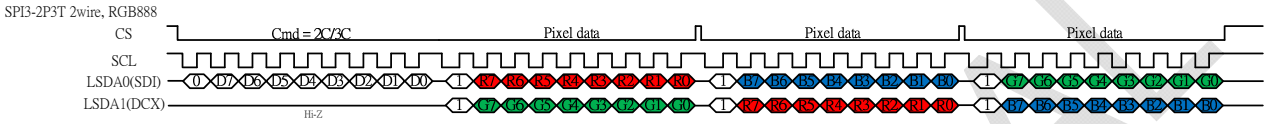
SPI3-1P1T 1wire, RGB888



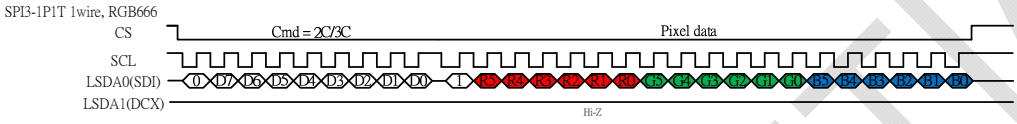
SPI3-1P1T 2wire, RGB888



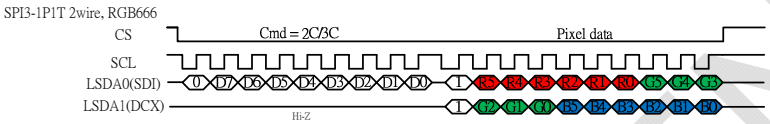
SPI3-2P3T 2wire, RGB888



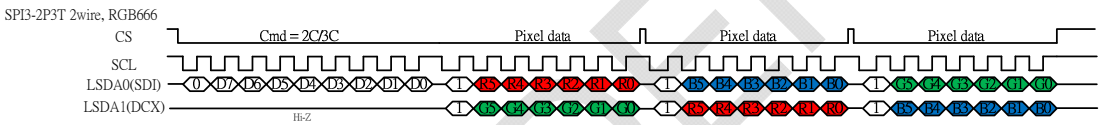
SPI3-1P1T 1wire, RGB666



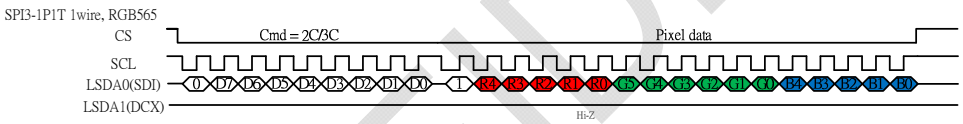
SPI3-1P1T 2wire, RGB666



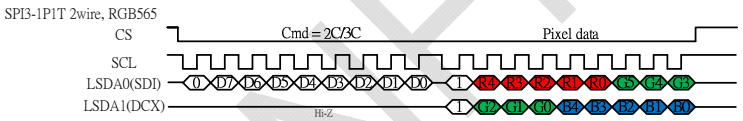
SPI3-2P3T 2wire, RGB666



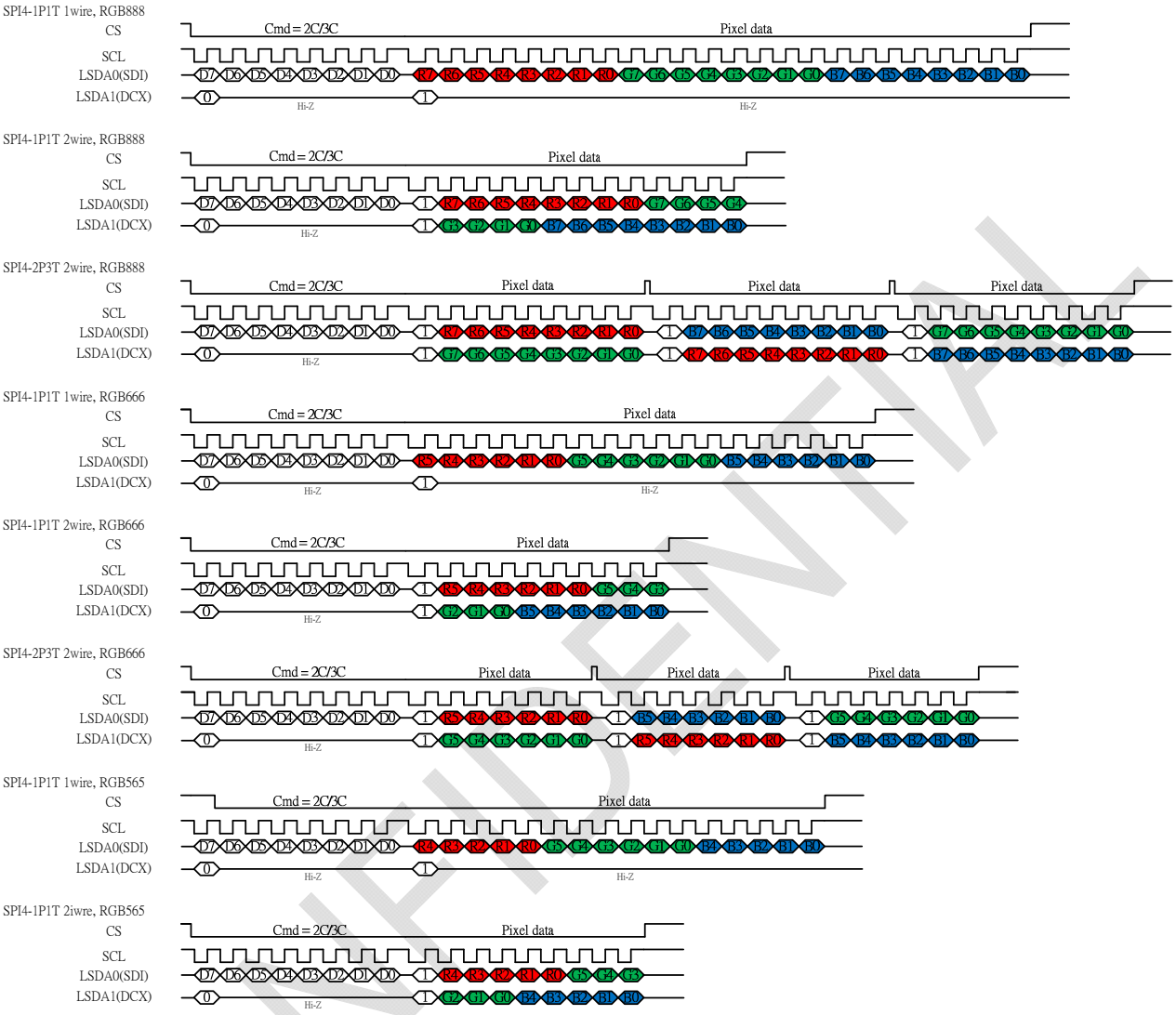
SPI3-1P1T 1wire, RGB565



SPI3-1P1T 2wire, RGB565



DUAL SPI via SPI4 interface :



(FE00h): CMD Mode Switch

FE00H	MAUCCTR (Manufacture Command Set Control)											
Instruction	R/W	Address		Parameter								
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CMD Mode Switch	W/R	FEh	FE00h	00h	0	0	0	0	CMD_Page[3:0]				00

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[3:0]	Hex Value	Description
0000	00h (default)	User Command Set (UCS = CMD1)
0001	01h	Manufacture Command Set Page0 (CMD2 P0)
0010	02h	Manufacture Command Set Page1 (CMD2 P1)
0011	03h	Manufacture Command Set Page2 (CMD2 P2)
0100	04h	Manufacture Command Set Page3 (CMD2 P3)
0101	05h	Manufacture Command Set Page4 (CMD2 P4)

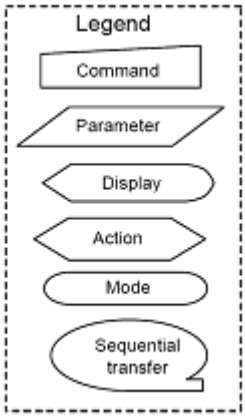
Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	FEh / FE00h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

(FF00h): Read CMD Status

FF00H	MAUCCTR (Manufacture Command Set Control)											
Instruction	R/W	Address		Parameter								
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RD CMD Status	R	FFh	FF00h	00h	0	0	0	0	CMD_Status[3:0]				00

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Status[3:0]	Hex Value	Description
0000	00h (default)	User Command Set (UCS = CMD1)
0001	01h	Manufacture Command Set Page0 (CMD2 P0)
0010	02h	Manufacture Command Set Page1 (CMD2 P1)
0011	03h	Manufacture Command Set Page2 (CMD2 P2)
0100	04h	Manufacture Command Set Page3 (CMD2 P3)
0101	05h	Manufacture Command Set Page4 (CMD2 P4)

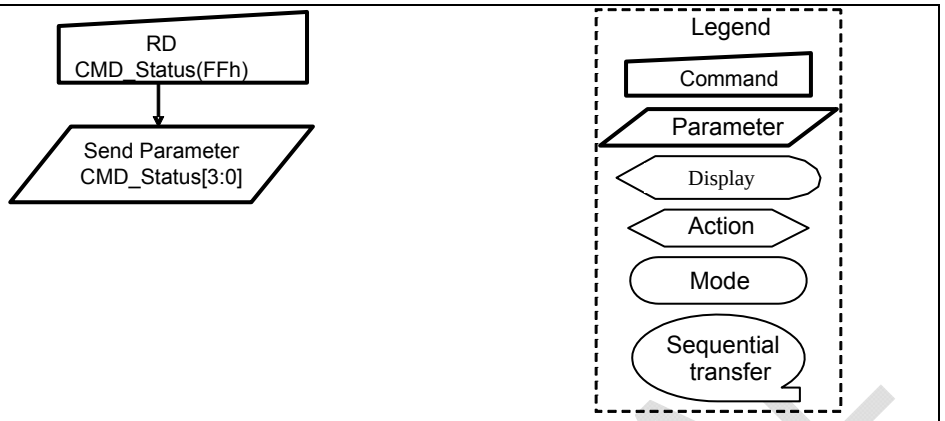
Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	FFh / FF00h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM67160 is used out of the absolute maximum ratings, the RM67160 may be permanently damaged. To use the RM67160 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM67160 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ + 5.5	V
Power supply voltage	VDD (VDDA, VDDB, VDDR)	-0.3 ~ + 5.5	V
Supply voltage (MV)	AVDD-AVSS	-0.3 ~ + 6.6	V
	VCL-AVSS	-0.3 ~ + 6.6	V
Supply voltage (HV)	VGH - VGLX	-0.3 ~ + 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Operating temperature	Topr	-40 ~ + 85	°C
Storage temperature	Tstg	-55 ~ + 125	°C

Notes:
If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	Pass 3KV
Machine Mode	R = 0 ohm / C = 200 pF	Pass 300V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

7.4 DC Characteristics

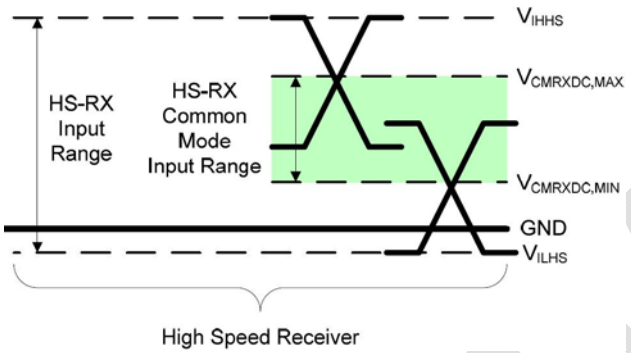
7.4.1 Basic Characteristics Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VDD	Operation Voltage	2.7	2.8	3.6	V	Note 1
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1,2
Logic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 3
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 3
Logic High level Output voltage	VOH	Iout = -1 mA	0.8* VDDI	-	VDDI	V	Note 3
Logic Low level Output voltage	VOL	Iout = +1 mA	0.0	-	0.2* VDDI	V	Note 3
Logic High level input current (Except MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (Except MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
Logic High level input current (MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
AVDD booster voltage	AVDD		4.5		6.5	V	Note 3
VCL booster voltage	VCL		-3.5		-5	V	Note 3
VGH booster voltage	VGH		AVDD		2AVDD	V	Note 3
VGL booster voltage	VGL		VCL		VCL -AVDD	V	Note 3
Voltage difference between VGH and VGL	VGHL	|VGH-VGL|			30	V	Note 3
Gamma reference voltage	VGMP		2.0		6.0	V	Note 3,4
Gamma reference voltage	VGSP		0.0		4.5	V	Note 3
OSC	Fosc		20.24	22	23.76	MHz	
Channel deviation voltage	V_{DEV}	Sout ≥ AVDD-1.0V, and 0V < Sout ≤ 1.0V				mV	TBD
Channel deviation voltage	V_{DEV}	1.0V < Sout < AVDD-1.0V				mV	TBD

Notes:
1. VDD means VDDA, VDDR, VDDB. And VSS means VSSA, VSSR, VSSB, AVSS, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
2. Recommend VDDI=1.8V for power saving.
3. Ta(ambient temperature) ranges from -30℃ to 85 ℃.
4. VGMP <= AVDD – 0.2V

7.5 MIPI Characteristics

7.5.1 High-Speed Receiver Specification

DC Specifications

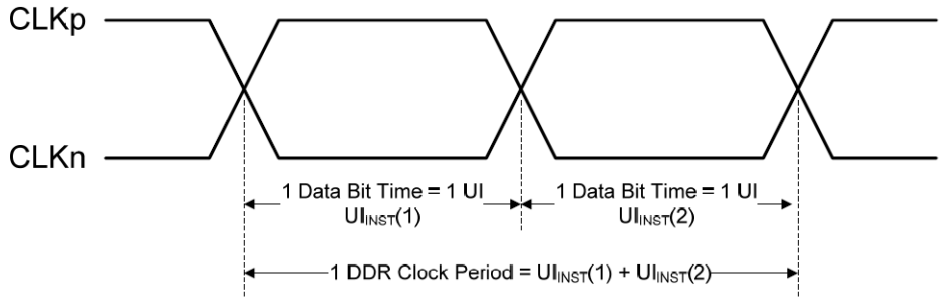


Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

Notes:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

7.5.2 Forward high speed transmissions

DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	2		12.5	ns	1,2

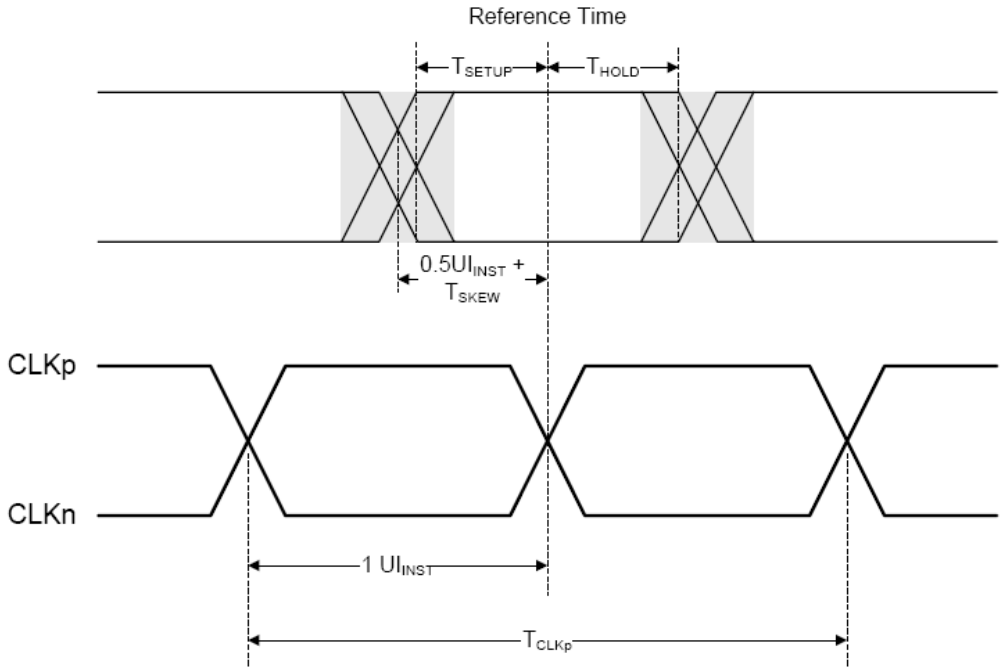
Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	$T_{SKEW[TX]}$	-0.15		0.15	UI_{INST}	1
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			UI_{INST}	2
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			UI_{INST}	2

Notes:
1. Total silicon and package delay budget of 0.3*UI_{INST}
2. Total setup and hold window for receiver of 0.3*UIINST

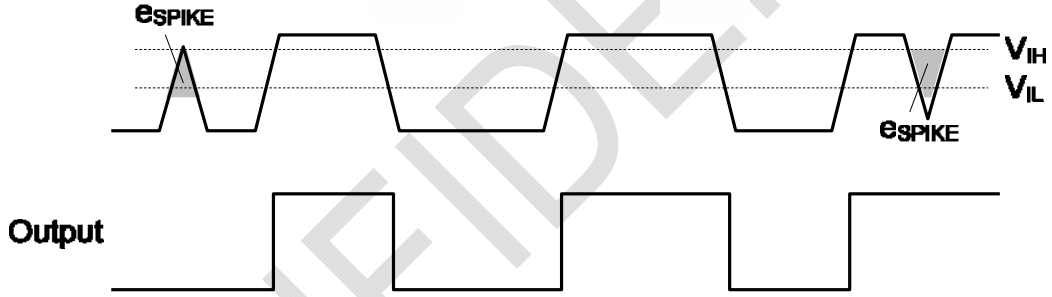
7.5.3 Data to Clock Timing Definitions



7.5.4 Low power transceiver specifications

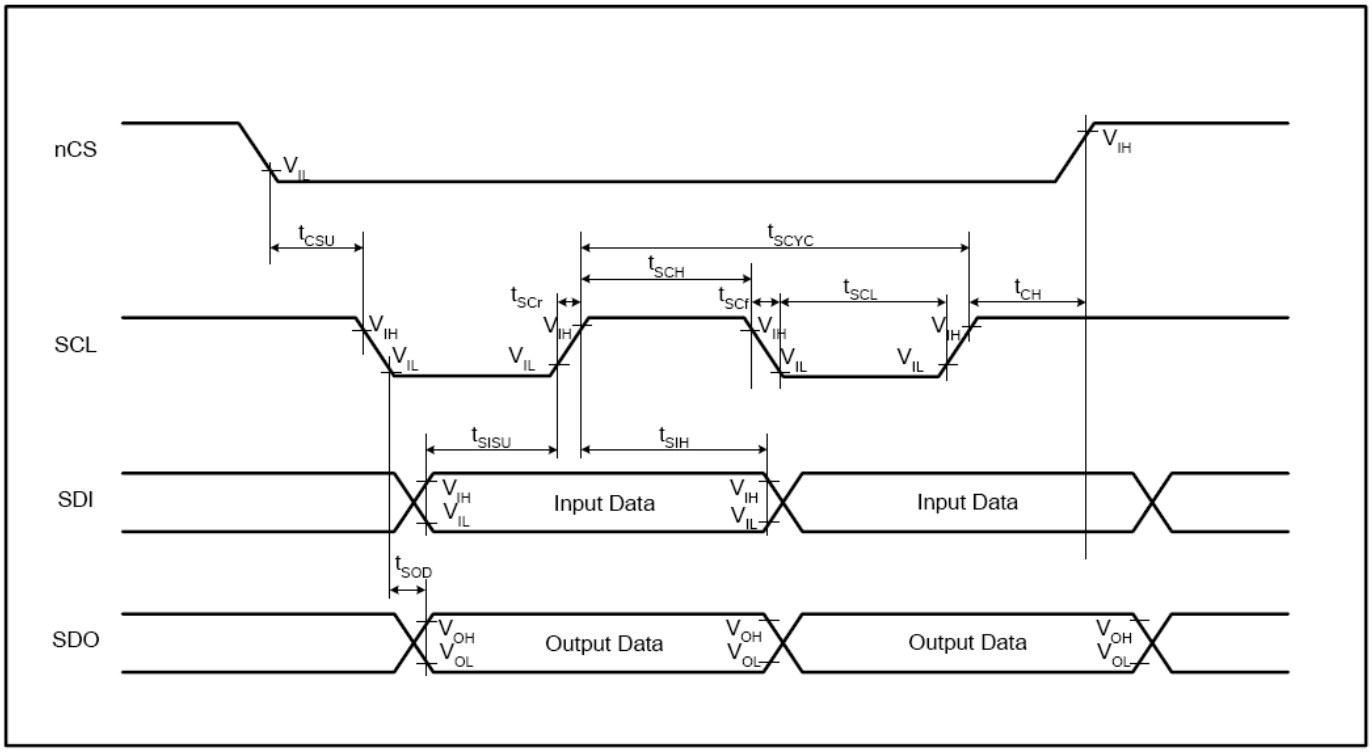
Parameters	Symbol	Condition	Min	Typ	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE[1.2.3]	Fig. 2	Input pulse rejection			300	V.ps

Notes:
Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State.
An impulse less than this will not change the receiver state.
In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
Input Glitch Rejection of Low Power Receivers as follow.



7.6 AC Characteristics

7.6.1 Serial Interface Characteristics

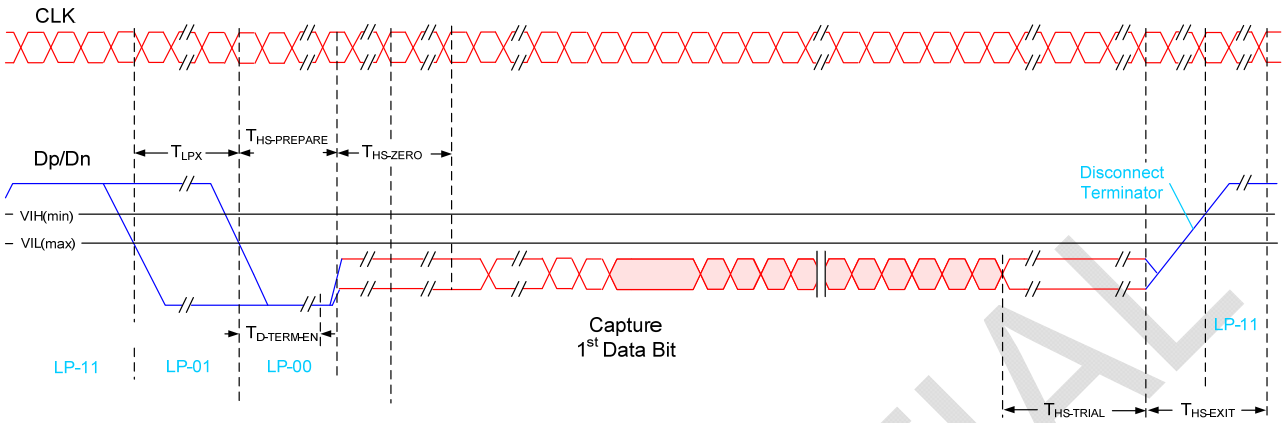


Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		ns	-
	T_{SCYC}	Clock cycle (Read)	300		ns	
	T_{SCH}	Clock “H” pulse width (Write)	40		ns	
	T_{SCH}	Clock “H” pulse width (Read)	140		ns	
	T_{SCL}	Clock “L” pulse width (Write)	40		ns	
	T_{SCL}	Clock “L” pulse width (Read)	140		ns	
	T_{SCr}	Clock rise time		5	ns	
	T_{SCf}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	20		ns	-
	T_{CH}	Chip select hold time	50		ns	
SDI	T_{SISU}	Data input setup time	20		ns	-
	T_{SIH}	Data input hold time	20		ns	
SDO	T_{SOD}	Data output setup time		120	ns	-
	T_{SOH}	Data output hold time	5		ns	

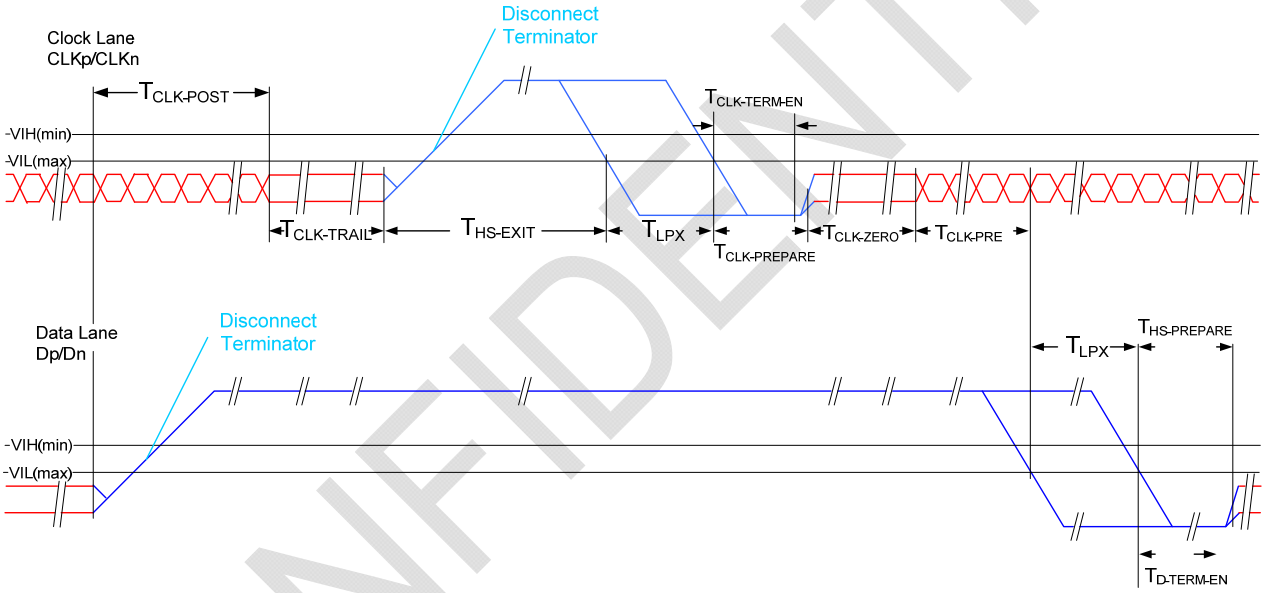
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, GND=0V

7.6.2 DSI Timing Characteristics

HS Data Transmission Burst



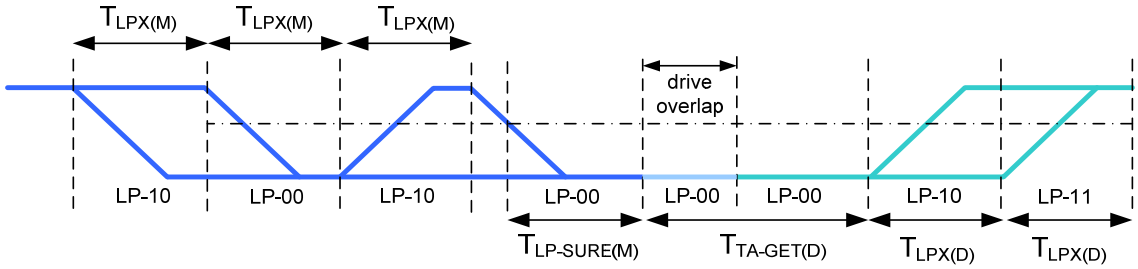
HS clock transmission



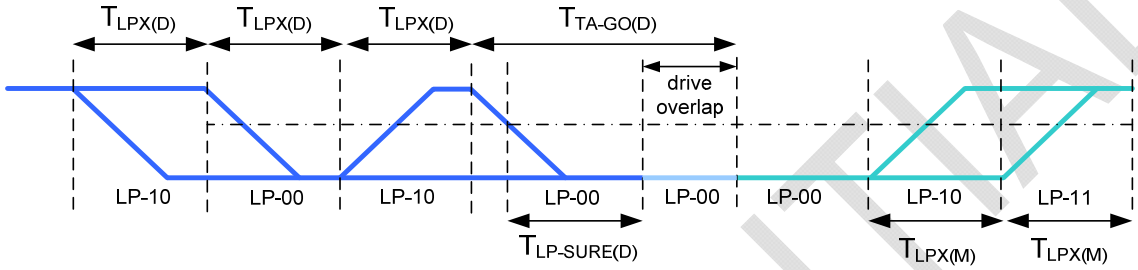
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



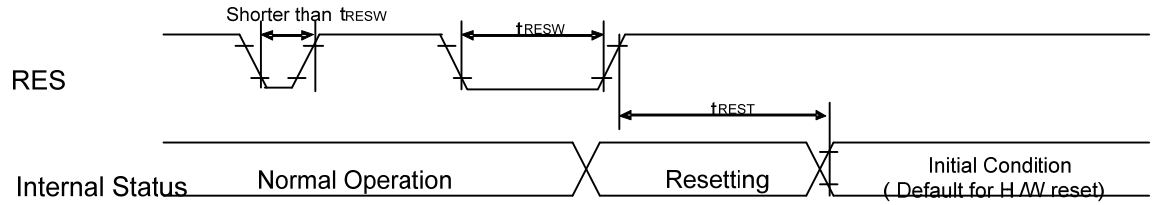
Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

7.6.3 Reset Timing



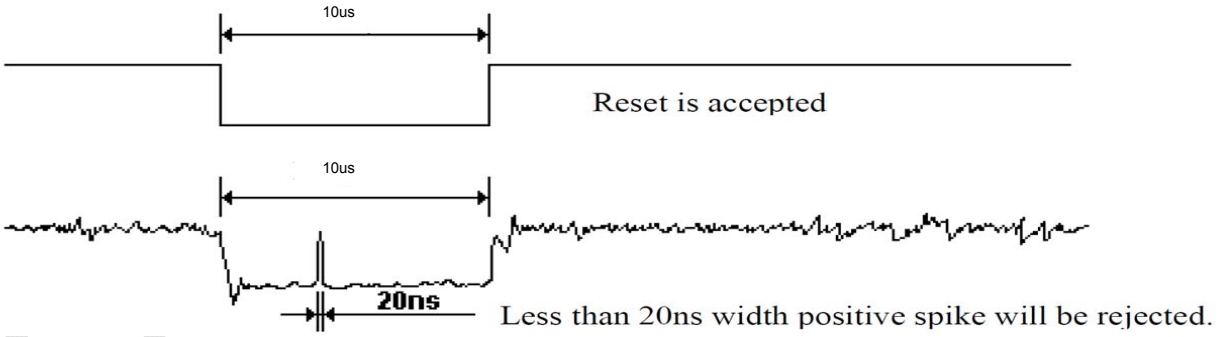
Reset input timing:
VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

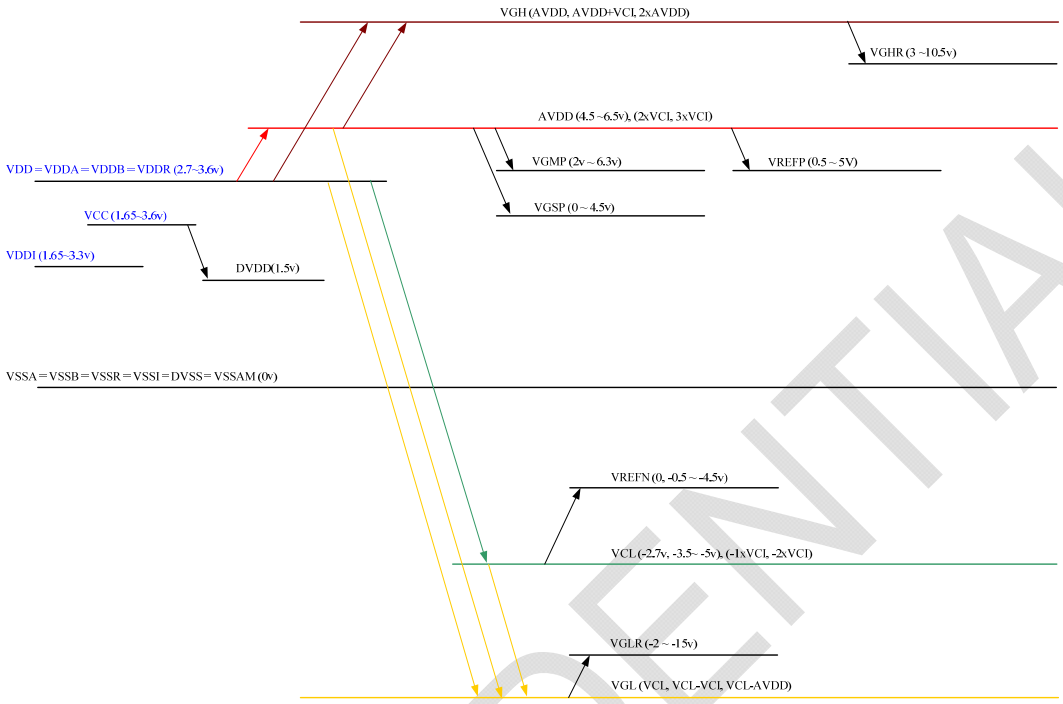
Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

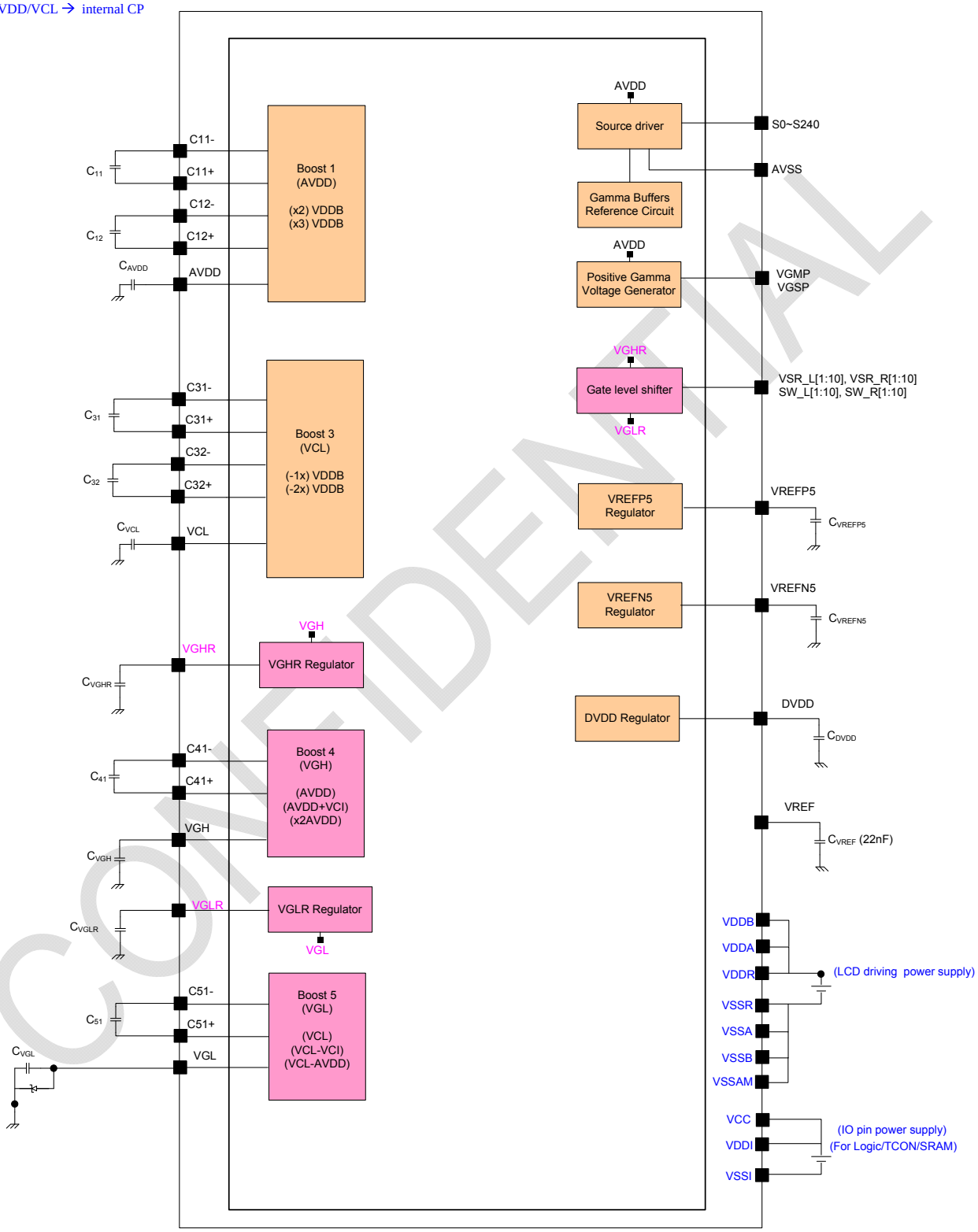
8. Power Generation

8.1 2 Supply Power (VDDI / VDD)



8.2 DC/DC Converter Circuit

2PWR(VDDI, VDD)
VDD=VDDA=VDDR=VDDB
AVDD/VCL → internal CP

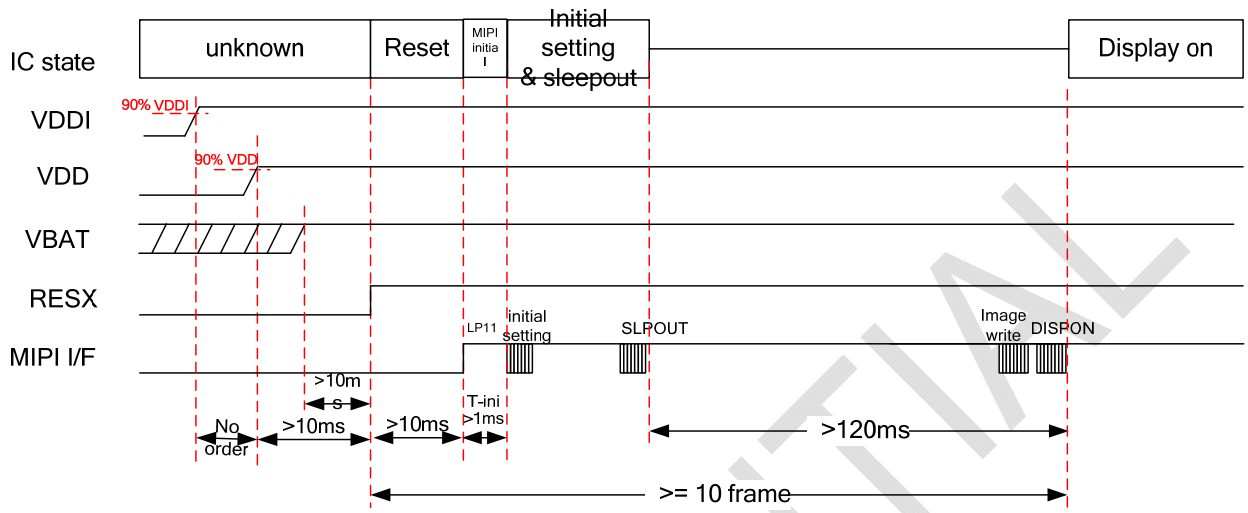


8.3 External Components

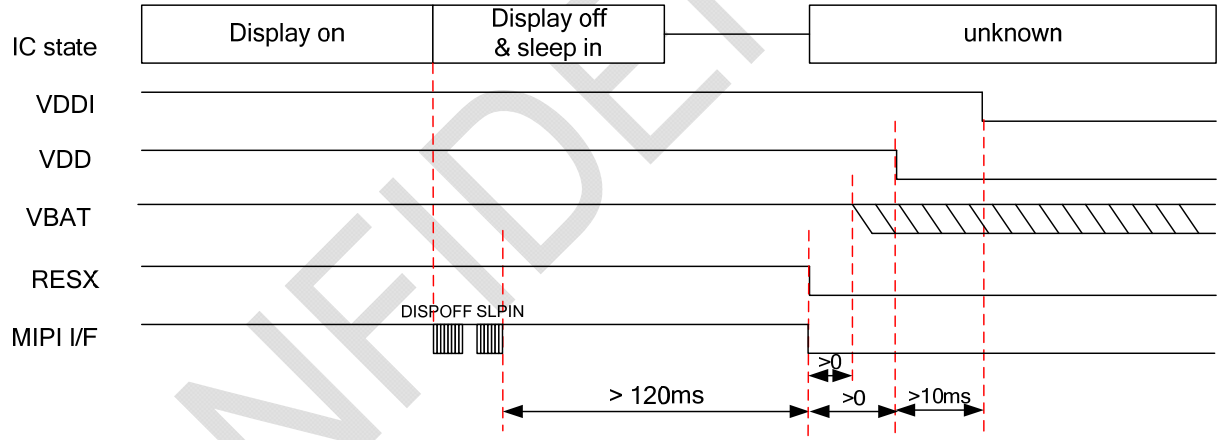
No.	Signal name	Values	Max ability
1	VDDA, VDDR, VDDB	Cap , 2.2uF	6.3V
2	VDDI, VCC	Cap , 2.2uF	6.3V
3	VREF	Cap , 22nF	6.3V
4	DVDD	Cap , 1.0uF	6.3V
5	VREFN5/VREFP5	Cap , 1.0uF	6.3V
6	VGHR	Cap , 1.0uF	16V
7	VGLR	Cap , 1.0uF	16V
8	BVP3D	Cap , 2.2uF	10V
9	BVN3D	Cap , 2.2uF	10V
10	C11P/C11N	Cap , 1.0uF	6.3V
11	C12P/C12N	Cap , 1.0uF	6.3V
12	AVDD	Cap , 2.2uF	10V
13	C31P/C31N	Cap , 1.0uF	6.3V
14	C32P/C32N	Cap , 1.0uF	6.3V
15	VCL	Cap , 2.2uF	6.3V
16	C41P/C41N	Cap , 1.0uF	16V
17	VGH	Cap , 2.2uF	25V
18	C51P/C51N	Cap , 1.0uF	16V
19	VGL	Cap , 2.2uF	25V
20	VGL (VGL-GND)	Schottky Diode	

8.4 Power on/off sequence and timing

Power On sequence



Power Off sequence



8.5 Power Level Modes

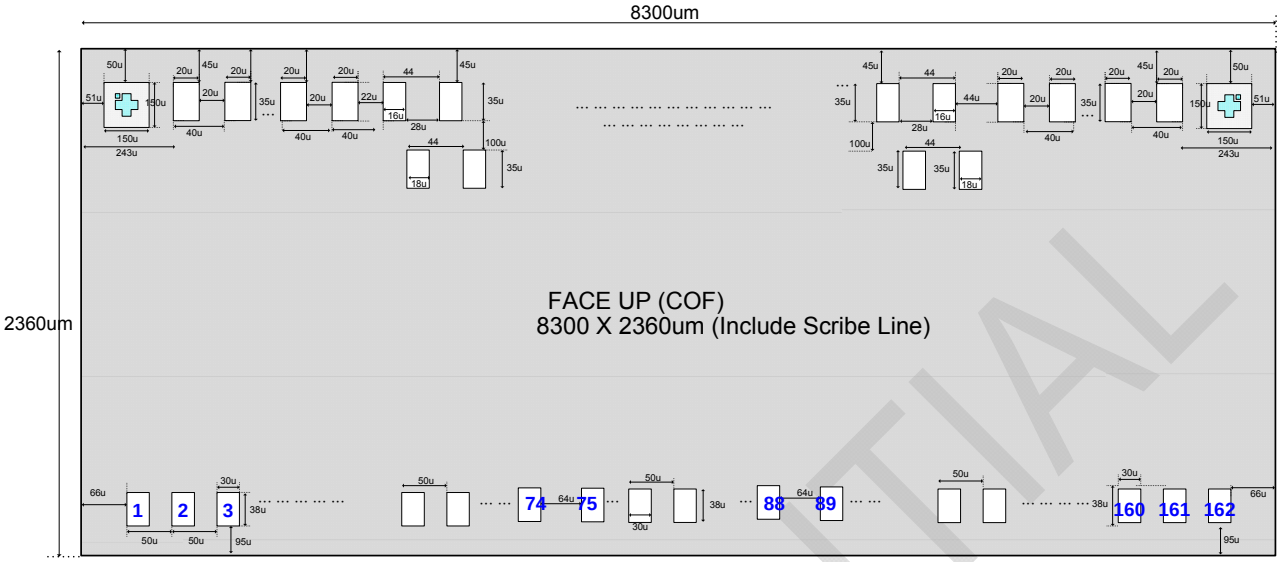
Normal display mode on = NORON
Partial mode on = PTLON
Idle mode off = IDMOFF
Idle mode on = IDMON
Sleep out = SLPOUT
Sleep in = SLPIN
Deep standby mode = DSTBON

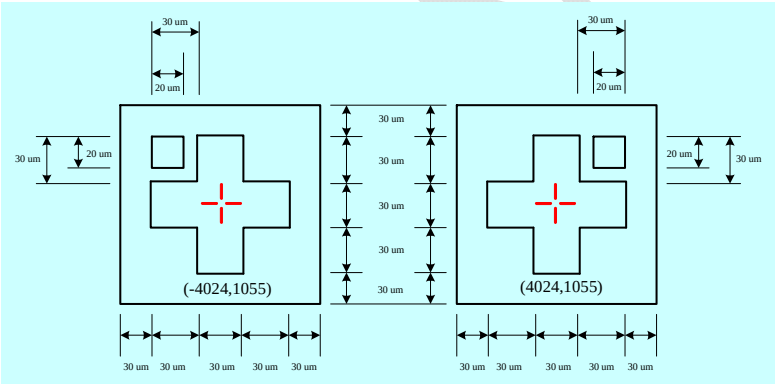
Definition example:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 16.7M colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
In this mode, part of the display is used with maximum 16.7M colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.
6. Deep Standby Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.
7. Power Off Mode
In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

9. Pad Diagram and Coordination





- Chip size: 8300 um x 2360um (Include sealing and scribe line)
- Chip thickness: 200/300 um
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size
  1. 17um x 35um: Source:S0~S240
  2. 20um x 35um: gate control signal
  3. 30um x 38um: Input Pads
- Au bump pitch: See PAD coordinates table
- Au bump height: 12±2 um (typ.)
- No. in the figure corresponds to No. in the PAD coordinates table
- Alignment mark

Alignment mark shape	X	Y
left	4024	1055
right	-4024	1055

-

■ Pad Coordinate (Unit: um)

NO.	PAD NAME	NO.	PAD NAME	NO.	PAD NAME	NO.	PAD NAME
1	ANALOG_TEST1	51	D[4]	101	C11N	151	VGL
2	VGLR	52	D[5]	102	C11N	152	VGL
3	VGLR	53	VSSI	103	C11N	153	AVSS
4	VGHR	54	D[6]	104	C12P	154	AVSS
5	VGHR	55	D[7]	105	C12P	155	AVSS
6	VREFP5	56	TEST1	106	C12P	156	MTP_PWR
7	VREFP5	57	EXTCLK	107	C12N	157	MTP_PWR
8	VREFP5	58	TEST2	108	C12N	158	MTP_PWR
9	VREFN5	59	VSSI	109	C12N	159	MTP_PWR
10	VREFN5	60	TEST3	110	VDDB	160	MTP_PWR
11	VREFN5	61	IM1	111	VDDB	161	MTP_PWR
12	BVP3D	62	IM0	112	VDDB	162	DUMMY
13	BVP3D	63	DSWAP	113	VDDR	163	VGLR
14	BVN3D	64	TESTEN	114	VDDR	164	VGHR
15	BVN3D	65	PSWAP	115	VDDR	165	VREFP5
16	VCL	66	BSTM	116	AVDD	166	VREFN5
17	VCL	67	VDDI	117	AVDD	167	VSR_L[10]
18	AVDD	68	VDDI	118	AVDD	168	VSR_L[9]
19	AVDD	69	VCC	119	C31P	169	VSR_L[8]
20	VREF	70	VCC	120	C31P	170	VSR_L[7]
21	VGSP	71	DVDD	121	C31P	171	VSR_L[6]
22	VGMP	72	DVDD	122	C31N	172	VSR_L[5]
23	DUMMY	73	DVSS	123	C31N	173	VSR_L[4]
24	ANALOG_TEST2	74	DVSS	124	C31N	174	VSR_L[3]
25	VDDR	75	HSSI_D1_P	125	VCL	175	VSR_L[2]
26	VDDR	76	HSSI_D1_P	126	VCL	176	VSR_L[1]
27	VDDA	77	HSSI_D1_N	127	VCL	177	SW_L[1]
28	VDDA	78	HSSI_D1_N	128	C32P	178	SW_L[2]
29	AVSS	79	VSSAM	129	C32P	179	SW_L[3]
30	AVSS	80	HSSI_CLK_P	130	C32P	180	SW_L[4]
31	AVSS	81	HSSI_CLK_P	131	C32N	181	SW_L[5]
32	VSSR	82	HSSI_CLK_N	132	C32N	182	SW_L[6]
33	VSSR	83	HSSI_CLK_N	133	C32N	183	SW_L[7]
34	VSSR	84	VSSAM	134	C41P	184	SW_L[8]
35	TE1	85	HSSI_D0_P	135	C41P	185	SW_L[9]
36	SWIRE	86	HSSI_D0_P	136	C41N	186	SW_L[10]
37	OLED_EN	87	HSSI_D0_N	137	C41N	187	SDMY
38	TE	88	HSSI_D0_N	138	C51N	188	S240
39	RESX	89	VSSR	139	C51N	189	S239
40	SDO	90	VSSR	140	C51P	190	S238
41	VSSI	91	VSSA	141	C51P	191	S237
42	SDI_RDX	92	VSSA	142	VGH	192	S236
43	DCX	93	AVSS	143	VGH	193	S235
44	WRX_SCL	94	AVSS	144	VGHR	194	S234
45	CSX	95	VSSB	145	VGHR	195	S233
46	D[0]	96	VSSB	146	VGHR	196	S232
47	VSSI	97	VSSB	147	VGHR	197	S231
48	D[1]	98	C11P	148	VGHR	198	S230
49	D[2]	99	C11P	149	VGLR	199	S229
50	D[3]	100	C11P	150	VGLR	200	S228

201	S227	251	S177	301	S127	351	S103
202	S226	252	S176	302	S126	352	S102
203	S225	253	S175	303	S125	353	S101
204	S224	254	S174	304	S124	354	S100
205	S223	255	S173	305	S123	355	S99
206	S222	256	S172	306	S122	356	S98
207	S221	257	S171	307	S121	357	S97
208	S220	258	S170	308	SDMY	358	S96
209	S219	259	S169	309	SDMY	359	S95
210	S218	260	S168	310	VGHR	360	S94
211	S217	261	S167	311	VGLR	361	S93
212	S216	262	S166	312	SDMY	362	S92
213	S215	263	S165	313	SDMY	363	S91
214	S214	264	S164	314	SDMY	364	S90
215	S213	265	S163	315	SDMY	365	S89
216	S212	266	S162	316	SDMY	366	S88
217	S211	267	S161	317	VREFN5	367	S87
218	S210	268	S160	318	SDMY	368	S86
219	S209	269	S159	319	SDMY	369	S85
220	S208	270	S158	320	SDMY	370	S84
221	S207	271	S157	321	SDMY	371	S83
222	S206	272	S156	322	SDMY	372	S82
223	S205	273	S155	323	SDMY	373	S81
224	S204	274	S154	324	VREFP5	374	S80
225	S203	275	S153	325	SDMY	375	S79
226	S202	276	S152	326	SDMY	376	S78
227	S201	277	S151	327	SDMY	377	S77
228	S200	278	S150	328	SDMY	378	S76
229	S199	279	S149	329	SDMY	379	S75
230	S198	280	S148	330	VGLR	380	S74
231	S197	281	S147	331	VGHR	381	S73
232	S196	282	S146	332	SDMY	382	S72
233	S195	283	S145	333	SDMY	383	S71
234	S194	284	S144	334	S120	384	S70
235	S193	285	S143	335	S119	385	S69
236	S192	286	S142	336	S118	386	S68
237	S191	287	S141	337	S117	387	S67
238	S190	288	S140	338	S116	388	S66
239	S189	289	S139	339	S115	389	S65
240	S188	290	S138	340	S114	390	S64
241	S187	291	S137	341	S113	391	S63
242	S186	292	S136	342	S112	392	S62
243	S185	293	S135	343	S111	393	S61
244	S184	294	S134	344	S110	394	S60
245	S183	295	S133	345	S109	395	S59
246	S182	296	S132	346	S108	396	S58
247	S181	297	S131	347	S107	397	S57
248	S180	298	S130	348	S106	398	S56
249	S179	299	S129	349	S105	399	S55
250	S178	300	S128	350	S104	400	S54

401	S53
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441	S13
442	S12
443	S11
444	S10
445	S9
446	S8
447	S7
448	S6
449	S5
450	S4

451	S3
452	S2
453	S1
454	SDMY
455	SW_R[10]
456	SW_R[9]
457	SW_R[8]
458	SW_R[7]
459	SW_R[6]
460	SW_R[5]
461	SW_R[4]
462	SW_R[3]
463	SW_R[2]
464	SW_R[1]
465	VSR_R[1]
466	VSR_R[2]
467	VSR_R[3]
468	VSR_R[4]
469	VSR_R[5]
470	VSR_R[6]
471	VSR_R[7]
472	VSR_R[8]
473	VSR_R[9]
474	VSR_R[10]
475	VREFN5
476	VREFP5
477	VGHR
478	VGLR