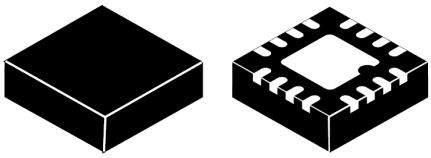
STAM1330

300mA TRIPLE DC/DC CONVERTER FOR POWERING AMOLED DISPLAY

Preliminary data

General Features

- Operating input voltage range from 2.5V to 4.5V
- 300mA output current for VO1 Step-up and VO2 Inverting converters (Vin>2.9V)
- 55mA output current for VO3 Auxiliary step-up converter (Vin>2.9V)
- High accuracy VO1 positive voltage 4.6V
- VO2 Programmable negative voltage from -1.4V to -5.4V default -2.0V
- VO3 Auxiliary step-up converter positive voltage programmable from 5.8V to 7.6V default 6.1V
- Soft-start with inrush current protection
- Over temperature protection
- True shutdown mode
- Short circuit protection
- Package QFN 3.0x3.0 16 Leads, 0.5mm pitch, 0.6mm height



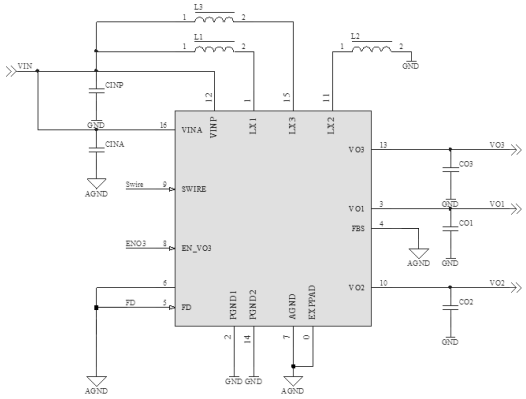
QFN16(3.0x3.0 mm)

Applications

- Active Matrix OLED power supply in portable devices
- Cellular phones, multimedia players, camcorders and digital still cameras

Description

The STAM1330 integrates 300mA step-up and inverting DC-DC converters plus auxiliary step-up converter. The device is particularly suitable for battery operated products, in which the major concern is the overall system efficiency.
VO2 and VO3 voltages can be programmed by S-wire protocol. Soft start with controlled inrush current limit, thermal shutdown and short circuit protection are integrated functions of the device.



Order codes

Order Code	Negative Voltage	Aux. Pos. Voltage	Package	Packaging
STAM1330TPQR	-1.4V to -5.4V	5.8V to 7.9V	QFN16 3x3mm	3000 samples per reel

1 Pin Configuration

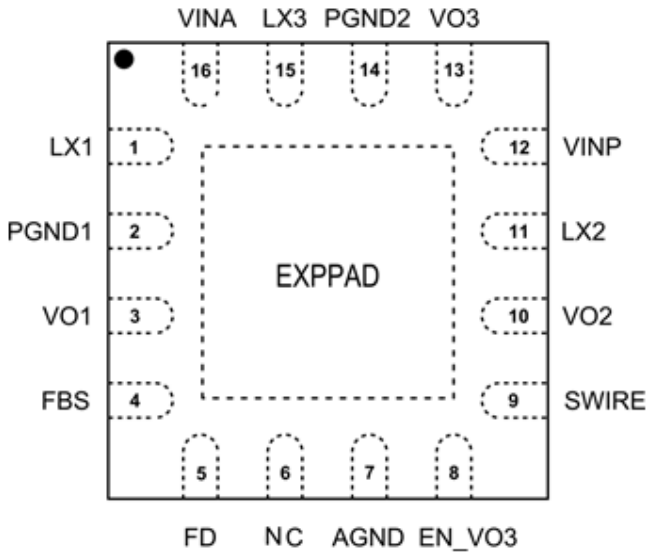


Figure 1 Pin Configuration (Top View)

Table 1 Pin Description

Pin	Pin Name	Description
1	LX1	Step-up switching pin
2	PGND1	Power ground
3	VO1	Step-up output voltage pin
4	FBS	Feedback sense
5	FD	Fast Discharge pin
6	NC	Not Connected or Ground
7	AGND	Analog Ground
8	EN_VO3	Aux. step-up enable pin
9	SWIRE	SWIRE pin
10	VO2	Inverter output voltage pin
11	LX2	Inverter switching pin
12	VINP	Power input voltage pin
13	VO3	Aux. step-up output voltage pin
14	PGND2	Power ground
15	LX3	Aux. step-up switching pin
16	VINA	Analog input voltage pin
EXP PAD		To guarantee proper operation of the device exposed pad must be connected to ground layers on the PCB

2 Block Schematics

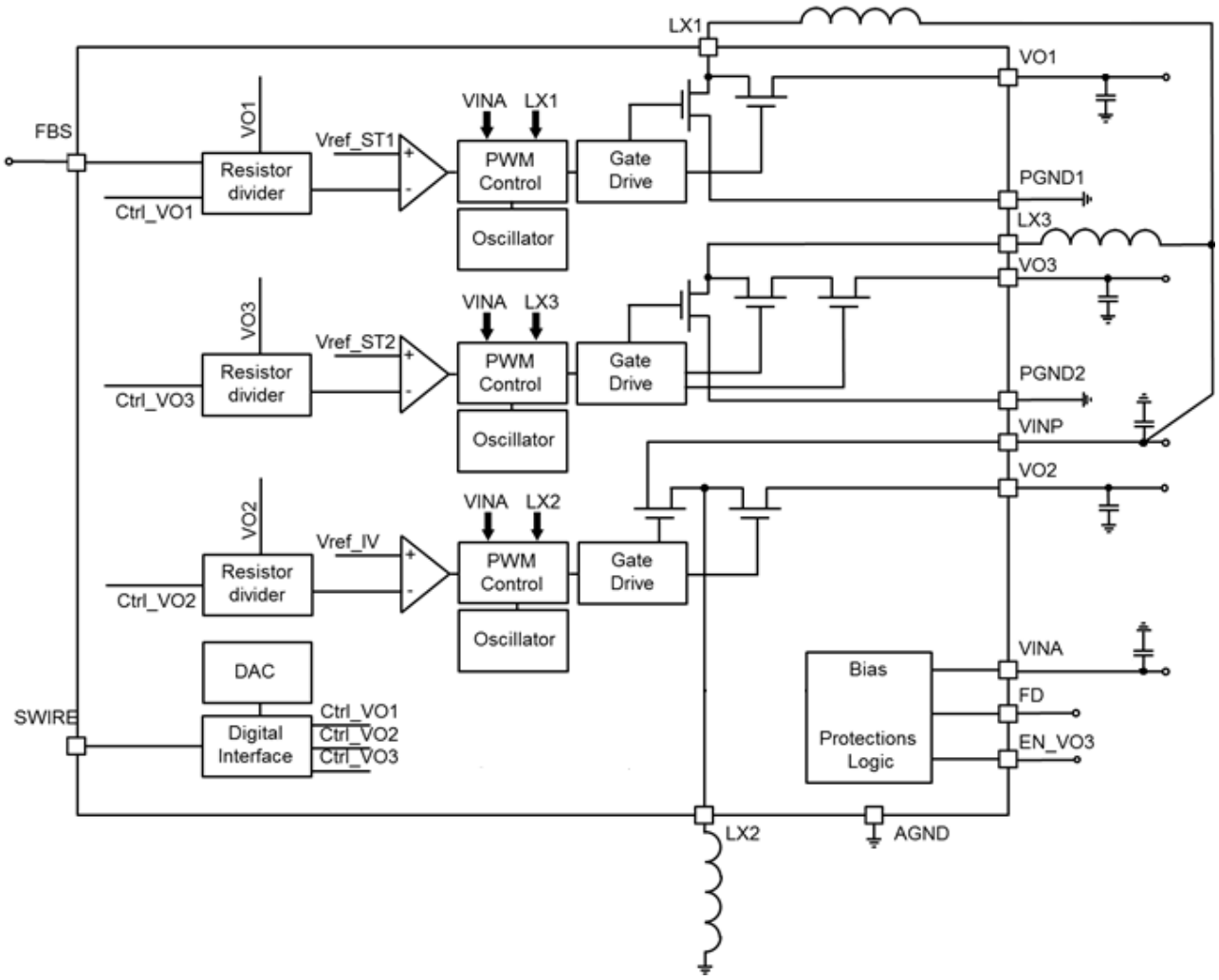


Figure 2 Block Schematics

3 Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VINA, VINP, VO1, FBS	DC Supply Voltage, Step up output voltage and output voltage sense input	-0.3 to 6.0	V
SWIRE, EN_VO3	Logic input pins	-0.3 to VINA+0.3	V
FD	Fast Discharge configuration pin	-0.3 to VINA+0.3	V
Lx2	Inverting converter switching node voltage	-6.0 to VINP	V
VINP – VOUT2	Differential Inverting converter voltage	11	V
VO2	Inverting converter output voltage	-6.0 to GND+0.3	V
Lx1	Step-up converter switching node voltage	GND-0.3 to VO1+0.3	V
Lx3	Aux. step-up converter switching node voltage	GND-0.3 to VO3+0.3	V
VO3	Aux. step-up converter output voltage	-0.3 to 8.0	V
TST	Storage Temperature Range	-65 to 150	°C
TJ	Maximum Junction Temperature	+150	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3 Thermal Data

Symbol	**Parameter**	**Value**	**Unit**
R_{THJA}	Junction to ambient thermal resistance (1)	55	°C/W
R_{THJC}	Junction to case thermal resistance	2.3	
OTP	Over Temperature Protection	140	°C

(1) The package is mounted on a 4-layers (2S2P) JEDEC board as per JESD51-7 and JESD51-5

4 Electrical Characteristics

Table 4 Electrical Characteristics

T_A = 25°C, V_{INA} = V_{INP} = 3.7V, I_{O1-O2} = 10mA, I_{O3} no load, C_{IN} = 22µF, C_{INA} = 10µF, C_{O1} = 22µF, **C_{O2} =** 22µF, C_{O3} = 22µF, L1 = L2 = 4.7µH, L3 = 10µH, V_{O1} = 4.6V, V_{O2} = -2.0V, V_{O3} = 6.1, V_{FD} = High

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
General Section						
$V_{INA,}$ V_{INP}	Supply Input Voltage		2.5	3.7	4.5	V
UVLO_H	Under voltage lockout HIGH	V_{INA} rising		2.2	2.3	V
UVLO_L	Under voltage lockout LOW	V_{INA} Falling	2.0	2.1		V
Logic Signals (EN, FD, Swire)						
V_H	High threshold	V_{INA}=2.9V to 4.5V	1.2			V
V_L	Low threshold				0.4	
Rdown	Pull down resistor at S-Wire and EN		200	300	400	KΩ
Step-up converter Section V_{O1}						
VO1 / FBS	Default Positive Output Voltage			4.6		
	Positive Output voltage total variation	V_{INA}=V_{INP}=2.9V to 4.5V;	-0.8		+0.8	%
		V_{INA}=V_{INP}=2.9V to 4.5V; T_A = -40°C to +85°C	-1.3		+1.3	%
R_{DSON}	P-channel Static Drain-source On Resistance	V_{INA}=V_{INP}=3.7V, I_{SW-P1}=100mA		0.3	0.5	Ω
	N-channel Static Drain-source On Resistance	V_{INA}=V_{INP}=3.7V, I_{SW-N1}=100mA		0.3	0.5	Ω
V_{O1} SCP	Short circuit threshold in operation	Percentage at nominal V_{Vo1}	75	85	90	%
f_{LX1}	LX1 Switching frequency	V_{INA}=V_{INP}=3.7V;	1.3	1.55	1.8	MHz
I_{LEAK_VO1}	VO1, no discharge	FD=GND, SWIRE=GND			1	uA
R_{VO1}	Discharge Resistance	SWIRE=GND, IVO1= 1mA	150	220	350	Ω
Inverting Converter Section V_{O2}						
V_{O2}	Negative Output voltage range	41 different values set by S_{WIRE} pin (see SWIRE table 6)	-5.4		-1.4	V
	Default Negative Output voltage			-2.0		V
	Negative output voltage total variation	V_{INA}=V_{INP}=2.9V to 4.5V; V_{O2} = -5.4V to -2.4V	-1.3		+1.3	%
		V_{INA}=V_{INP}=2.9V to 4.5V; V_{O2} = -2.3V to -1.4V	-1.5		+1.5	
R_{DSON}	P-channel Static Drain-source On Resistance	V_{INA}=V_{INP}=3.7V, I_{SW-P1}=100mA		0.2	0.5	Ω
	N-channel Static Drain-source On Resistance	V_{INA}=V_{INP}=3.7V, I_{SW-N1}=100mA		0.3	0.5	Ω
V_{O2} SCP	Short circuit threshold in operation	Percentage at nominal V_{Vo2}	70	80	90	%
I_{LEAK_VO2}	VO2 leakage, no discharge	FD=GND, SWIRE=GND			1	uA
f_{LX2}	LX2 Switching frequency	V_{INA}=V_{INP}=3.7V;	1.3	1.55	1.8	MHz
R_{VO2}	Discharge Resistance	SWIRE=GND, IVO1= 1mA	200	300	400	Ω
Auxiliary Step-up Converter Section V_{O3}						
V_{O3}	Positive Output voltage range	8 different values set by S_{WIRE} pin (see SWIRE table 7)	5.8		7.6	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
	Default positive Output voltage			6.1		V
	Total output voltage variation	V_{INA}=V_{INP}=2.9V to 4.5V; T_A = -40°C to +85°C	-1.5		1.5	%
R_{DSON}	P-channel Static Drain-source On Resistance	V_{INA}=V_{INP}=3.7V, I_{SW-P3}=100mA	0.9	1.7	2.3	Ω
	N-channel Static Drain-source On Resistance	V_{INA}=V_{INP}=3.7V, I_{SW-N3}=100mA	0.5	0.8	1.3	Ω
V_{O3} SCP	Short circuit threshold in operation	Percentage at nominal V_{VO3}	70	80	90	%
I_{LEAK_VO3}	VO3 leakage, no discharge	FD=GND, EN_VO3=GND			1	uA
R_{VO3}	Discharge Resistance	EN_VO3=GND, I_{VO3}= 1mA	200	300	400	Ω

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5 Detailed Description

5.1 General Description

The STAM1330 is a high efficiency DCDC converter which integrates two step-up and one inverting power stages suitable to supply AMOLED panels. Thanks to the high level of integration it needs only eight external components to operate and it achieves very high efficiency using synchronous rectification technique for all DC-DC converters.

The controller uses an average current mode technique to obtain good stability and precise voltage regulation in all possible conditions of input voltage, output voltage and output current. In addition, the peak inductor current is monitored in order to avoid saturation of the coils.

The STAM1330 implements a power saving technique in order to maintain high efficiency at very light load and it switches to PWM operation as the load increases in order to guarantee the best dynamic performances and low noise operation.

The STAM1330 avoids battery leakage thanks to the true-shutdown feature and it is self-protected by over-temperature. Under voltage lockout and soft start guarantee proper operation during start-up.

5.2 Enable Functionality

In typical application the device generally operates as two channel power supply. The main channel consists of positive voltage output VO1 and negative voltage output VO2. The auxiliary channel is step-up converter with configurable output voltages.

Thus device provides two separated enable functionalities. SWIRE pin can be used to operate main channel to its output voltage default values. And EN_VO3 pin enables the auxiliary channel.

During expected start-up procedure auxiliary channel is enabled first by EN_VO3 and then the main power channel is enabled or configured by SWIRE pin. Equally during disable sequence the main channel is disabled prior to auxiliary one.

When the device is disabled it stops switching and all the internal blocks are turned off. In this condition the current drawn from V_{INP}/V_{INA} is very low in the whole temperature range. In addition, the internal switches are in off state so the load is electrically disconnected from the input, this avoids unwanted current leakage from the input to the load.

5.3 FBS Pin

Two kinds of feedback control loop are implemented in this device to control positive output voltage VO1. When FBS pin is connected to AMOLED panel VO1 node, external feedback is used. Thus the control loop regulates positive output voltage VO1 according to FBS. When pin is connected to AGND or floating, internal feedback is used to instead.

Proper PCB layout of FBS track is mandatory, the principle of Kelvin sensing should be applied in a routing technique. It's suggested to follow Recommended PCB Layout chapter.

Table 5 FBS Operation Table

FBS	Action
AGND or Floating	Internal feedback enabled
VO1 at Panel	External feedback enabled (*) *(*) It is recommended to do not use ferrite bead in order to do not alter FBS sensing. VO2, VO3 can optionally make use of beads whatever FBS condition.*

5.4 Soft Start and Inrush Current Limiting

In order to limit inrush current soft start feature is implemented. The feature ensures correct start-up procedure and optimizes power supply battery operation lifetime.

5.5 Under voltage Lockout

The under voltage lockout function avoids improper operation of the device when the input voltage is not high enough. When the input voltage is below the UVLO threshold the device is in shutdown mode. The hysteresis of 50mV avoids unstable operation when the input voltage is close to the UVLO threshold.

5.6 Over-temperature Protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds OTP threshold the device stops operating. As soon the temperature falls below typically normal operation is restored.

5.7 Short Circuit Protection

Output current is internally limited. An overload condition on any output switches the device to power-off state. To reset the normal functionality (assuming that the short condition was removed), it is necessary to restart the converter.

5.8 Output Fast Discharge

When fast discharge feature is enabled (FD=High) and the device goes into shutdown mode converters stop switching. A fast discharge pull-down resistor is connected between V_{O1} and GND to discharge quickly C_{O1} capacitor. The same circuitry is implemented on V_{O2}. Fast discharge feature is also implemented on V_{O3} output.

5.9 S_{WIRE} Protocol Description

Protocol to digitally communicate over a single cable with single wire components

Swire protocol is based on pulse counting. Pulse is defined as a transition to low state followed by a transition to high state those follow Tl, Th, Tr and Tf requirements.

Each pulse is counted when received. Pulse counting is terminated by reception of a stop bit which is defined as high state longer than Tstop.

VO2 Negative output voltage and VO3 can be set through S_{WIRE} interface by providing number of pulses according to following table.

Table 6 VO2 SWIRE Operation Table

Pulse	V_{O2}	Pulse	V_{O2}	Pulse	V_{O2}	Pulse	V_{O2}	Pulse	V_{O2}
1	-5.4	**11**	-4.4	**21**	-3.4	**31**	-2.4	**41**	-1.4
2	-5.3	**12**	-4.3	**22**	-3.3	**32**	-2.3		
3	-5.2	**13**	-4.2	**23**	-3.2	**33**	-2.2		
4	-5.1	**14**	-4.1	**24**	-3.1	**34**	-2.1		
5	-5.0	**15**	-4.0	**25**	-3.0	**35**	**-2.0** (*)		
6	-4.9	**16**	-3.9	**26**	-2.9	**36**	-1.9		
7	-4.8	**17**	-3.8	**27**	-2.8	**37**	-1.8		
8	-4.7	**18**	-3.7	**28**	-2.7	**38**	-1.7		
9	-4.6	**19**	-3.6	**29**	-2.6	**39**	-1.6		
10	-4.5	**20**	-3.5	**30**	-2.5	**40**	-1.5		

Table 7 VO3 SWIRE Operation Table

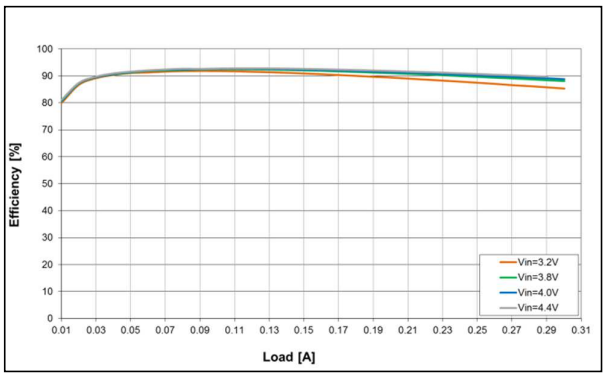
Pulse	V_{O3}
43	7.6
44	7.3
45	7.0
46	6.7
47	6.4
48	**6.1** (*)
49	5.8

(*) Default value

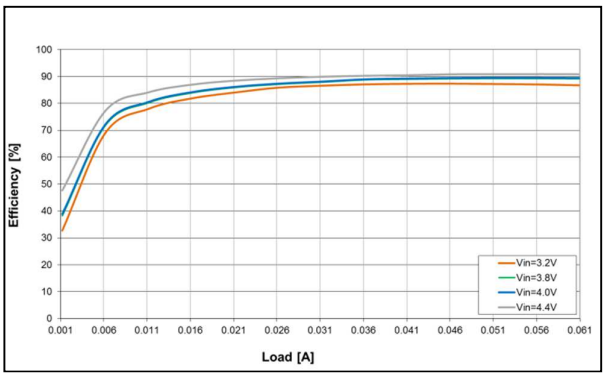
6 Typical Application Performance

V_{INA}=V_{INP}=3.7V, V_{O2} = -4.0V, V_{O3} = 7.6V T_A = 25°C; See Table for external components used in the below tests.

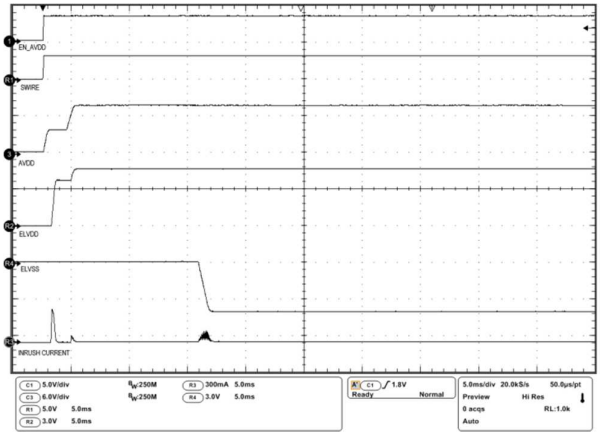
Efficiency vs Output Current
V_{INA}=V_{INP}=3.2V to 4.4V, $I_{O1,O2}$=10 to 300mA,
I_{O3}= no load



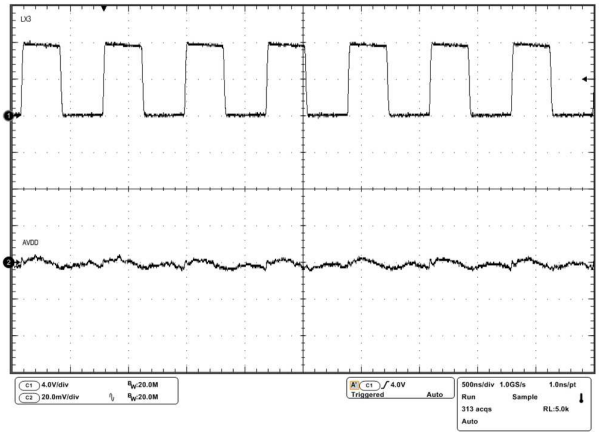
Efficiency vs Output Current
V_{INA}=V_{INP}=3.2V to 4.4V, I_{O3}= 1 to 55mA,
$I_{O1,O2}$=no load



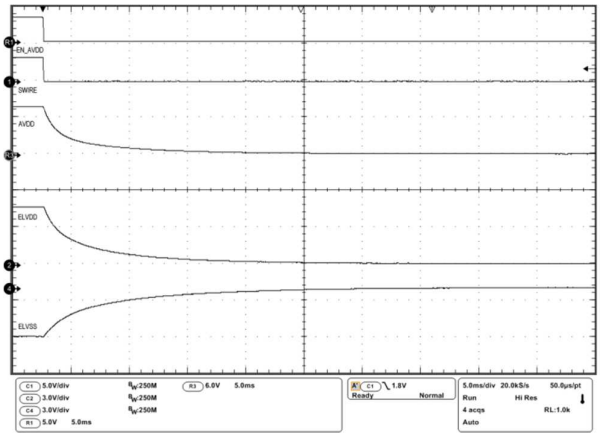
Soft-start and Inrush Current
No Load



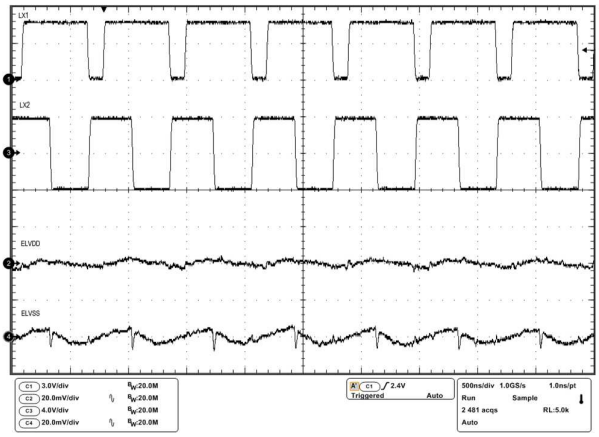
Switching and Output Waveforms
V_{INA}=V_{INP}=2.9V, $I_{O1,\ O2}$ no load, I_{O3}=30mA



Fast Discharge
No load, SW=Low, FD=High



Switching and Output Waveforms
V_{INA}=V_{INP}=2.9V, $I_{O1,\ O2}$=300mA, I_{O3} no load



7 Application Schematics

Figure 3 Application Schematics

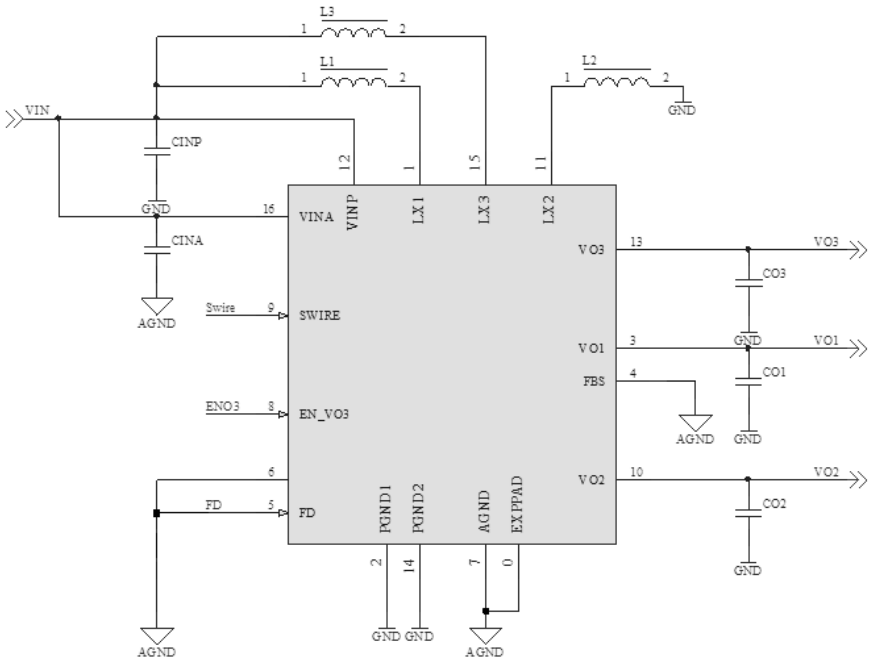


Table 8 Typical External Components

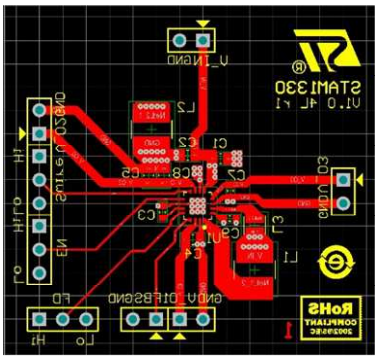
Component	Manufacturer	Part Number	Value	Size	Ratings
L_1, L_2	TOKO	1239AS-H-4R7N=P2	4.7μH	2.5 x 2.0 x 1.2	±30% 1.60A 240mΩ
	ALPS	GLCLM4R7		2.5 x 2.0 x 1.2	±20% 1.50A 180mΩ
	COILCRAFT	LPS4012-472ML		4.0 x 4.0 x 1.2	±20% 1.70A 175mΩ
L_3	TOKO	1239AS-H-100N=P2	10μH	2.5 x 2.0 x 1.2	±30% 1.00A 460mΩ
	TAIYO YUDEN	MDKK2020T100MM		2.0 x 1.6 x 1.2	±20% 0.75A 690mΩ
	CYNTEC	PIT20161T-100MDR		2.0 x 1.6 x 1.0	±20% 0.72A 750mΩ
C_{INA}	MURATA	GRM219R61A226MEA0	22μF	0805 (2012)	±20%, X5R, 10V
	SEMCO	CL05A106MP5NUNC	10μF	0402 (1005)	
	SEMCO	CL10A226MP8NUNE	22μF	0603 (1608)	
C_{INP}	MURATA	GRM219R61A226MEA0	22μF	0805 (2012)	±20%, X5R, 10V
	SEMCO	CL10A226MP8NUNE	22μF	0603 (1608)	
C_{O1}	MURATA	GRM219R61A226MEA0	22μF	0805 (2012)	±20%, X5R, 10V
	SEMCO	CL10A226MP8NUNE	22μF	0603 (1608)	
	SEMCO	CL21A226MPCLRNC	22μF	0805 (2012)	
C_{O2}	MURATA	GRM219R61A226MEA0	22μF	0805 (2012)	±20%, X5R, 10V
	SEMCO	CL10A226MP8NUNE	22μF	0603 (1608)	
	SEMCO	CL21A226MPCLRNC	22μF	0805 (2012)	
C_{O3}	MURATA	GRM219R61A226MEA0	22μF	0805 (2012)	±20%, X5R, 10V
	SEMCO	CL10A226MP8NUNE	22μF	0603 (1608)	
	SEMCO	CL21A226MPCLRNC	22μF	0805 (2012)	

All the above components refer to the typical application performance characteristics. Operation of the device is not limited to the choice of these external components.

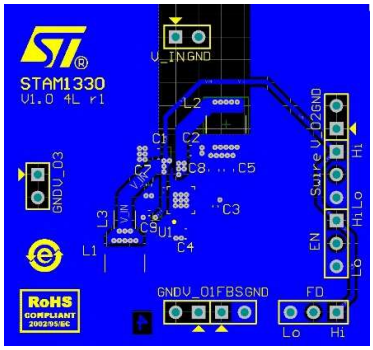
7.1 Recommended PCB Layout

The STAM1330 is high frequency power switching device so it requires a proper PCB layout in order to obtain the necessary stability and optimize line/load regulation and output voltage ripple.

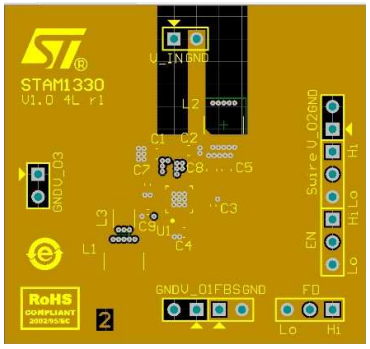
Top layer

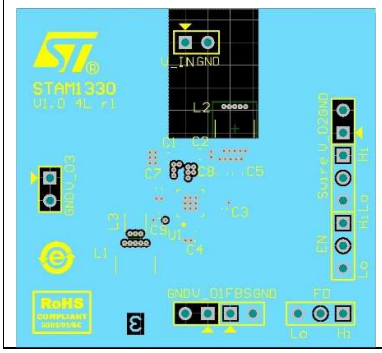


Bottom layer



Mid Layer 1&2



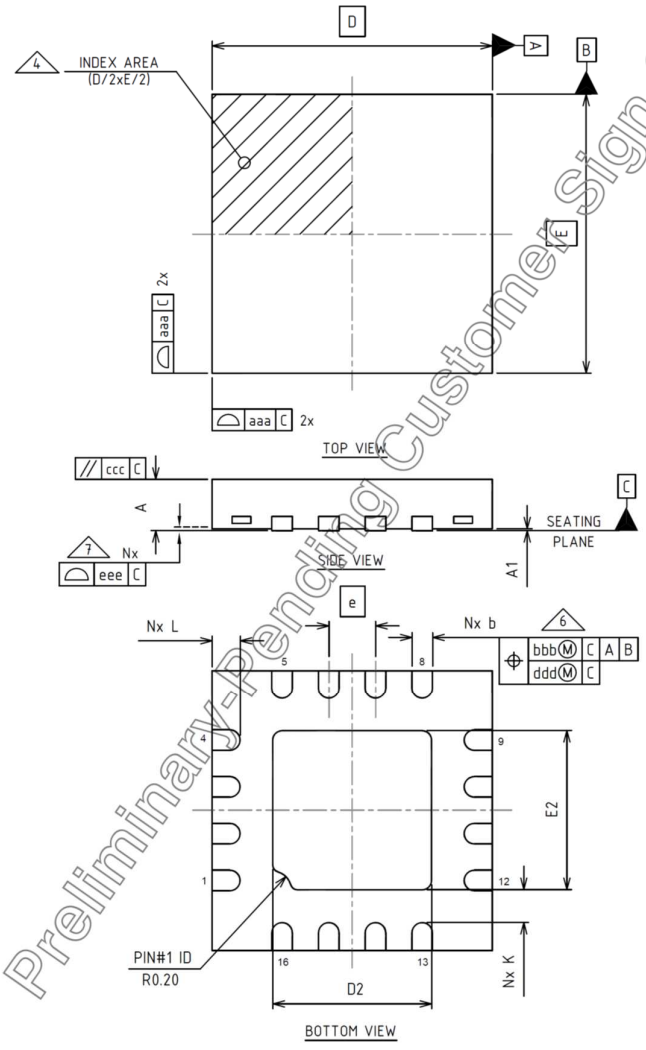


1. Place and connect the output capacitor of VO1 as close as possible to pin 3.
2. Place the power input capacitors as close as possible to pin 12 so the trace connecting one end of the capacitors to VINP pin and the trace connecting the other end of the capacitors to the PGND plane is as short as possible.
3. Place and connect the output capacitors of VO2 and VO3 as close as possible to their respective pins (10,13).
4. Create a power ground plane (PGND) so the other end of these capacitors and the PGND pins (2, 14) can connect to this plane directly.
5. Place the boost converters L1, L3 inductors so the traces connecting the inductor to the LX1 pin (1) and to LX3 pin (15) and the input capacitors are as short as possible.
6. Create an analog ground plane (AGND) so the other end of these capacitors and the AGND pin can connect to this plane directly. FBS (4), FD (5) and CT (6) pins are normally connected to AGND. Place the inverting converter L2 inductor so the trace connecting the inductor to the LX2 pin (11) and the distance the inductor current has to travel through the PGND plane to the PGND pin are as short as possible.
7. Make a single connection between the AGND and PGND planes together at a point closest to the PGND pin only. Connect the entire backside pad to inner PGND with a larger plane for good thermal performance. Make no other connections between these two ground planes. If vias are needed to make this connection, use multiple vias instead of a single via to help reduce the resistance and the inductance attributed by the vias and place the vias close to the PGND pins so the AGND plane can connect to the PGND plane at a point closest to the PGND pins.
8. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias instead of single vias to help reduce the resistance and the inductance attributed by the vias. Avoid using vias in connection with switched current. Use vias, if necessary, in connections with continuous currents. For the step-up regulators, the continuous-current connections are between the input capacitors and the inductors and between the inductors and LX1, LX3. For the inverting regulator, the continuous current paths are between the inductor and PGND and between the inductor and LX2. Avoid vias in all other high-current connections including ground connections.
9. In case of FBS connected to VO1, it is recommended to do not use ferrite beads order to do not alter FBS sensing. VO2, VO3 can optionally make use of beads whatever FBS condition.
10. Minimize the length (<5mm) and maximize the width (>0.5mm) of traces between the output capacitor and the load to do not impact on transient responses.
11. Care should be taken to avoid running traces that carry any noise-sensitive signals near LX1, LX2, LX3 or high-current traces.

8 Package Description

Dim.	mm		
	Nom.	Min.	Max.
A	0.55	0.50	0.60
A1	0.02	0.00	0.05
b	0.25	0.20	0.30
D	3.00	2.9	3.1
D2	1.70	1.55	1.80
E	3.00	2.9	3.1
E2	1.70	1.55	1.80
e	0.50		
L	0.30	0.20	0.40

Recommended PCB Footprint



Tape & Reel QFN 16 Mechanical Data

DIM.	mm			Inch		
	MIN	TYP	MAX	MIN	TYP	MAX
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99			3.898		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		0.8			0.031	
Po		4			0.157	
P		8			0.315