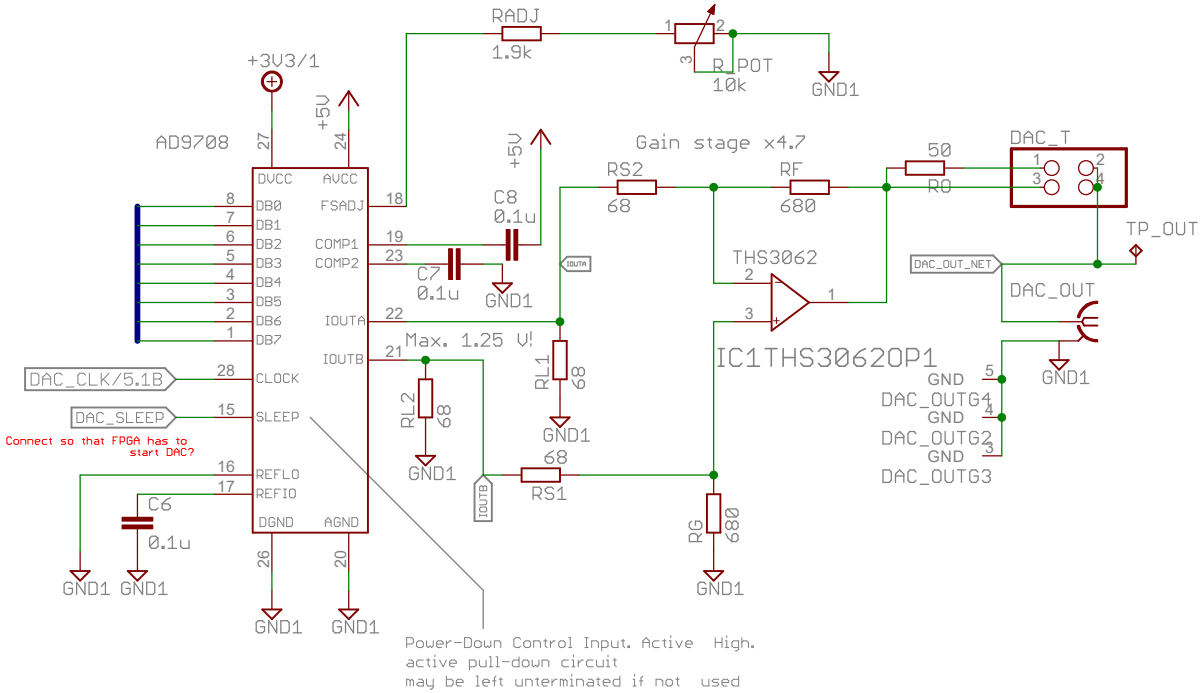

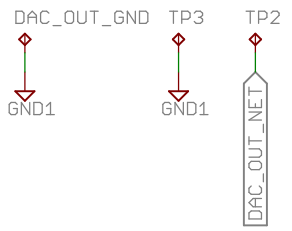

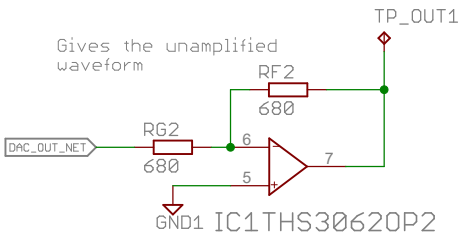

DAC
David Oswald

board
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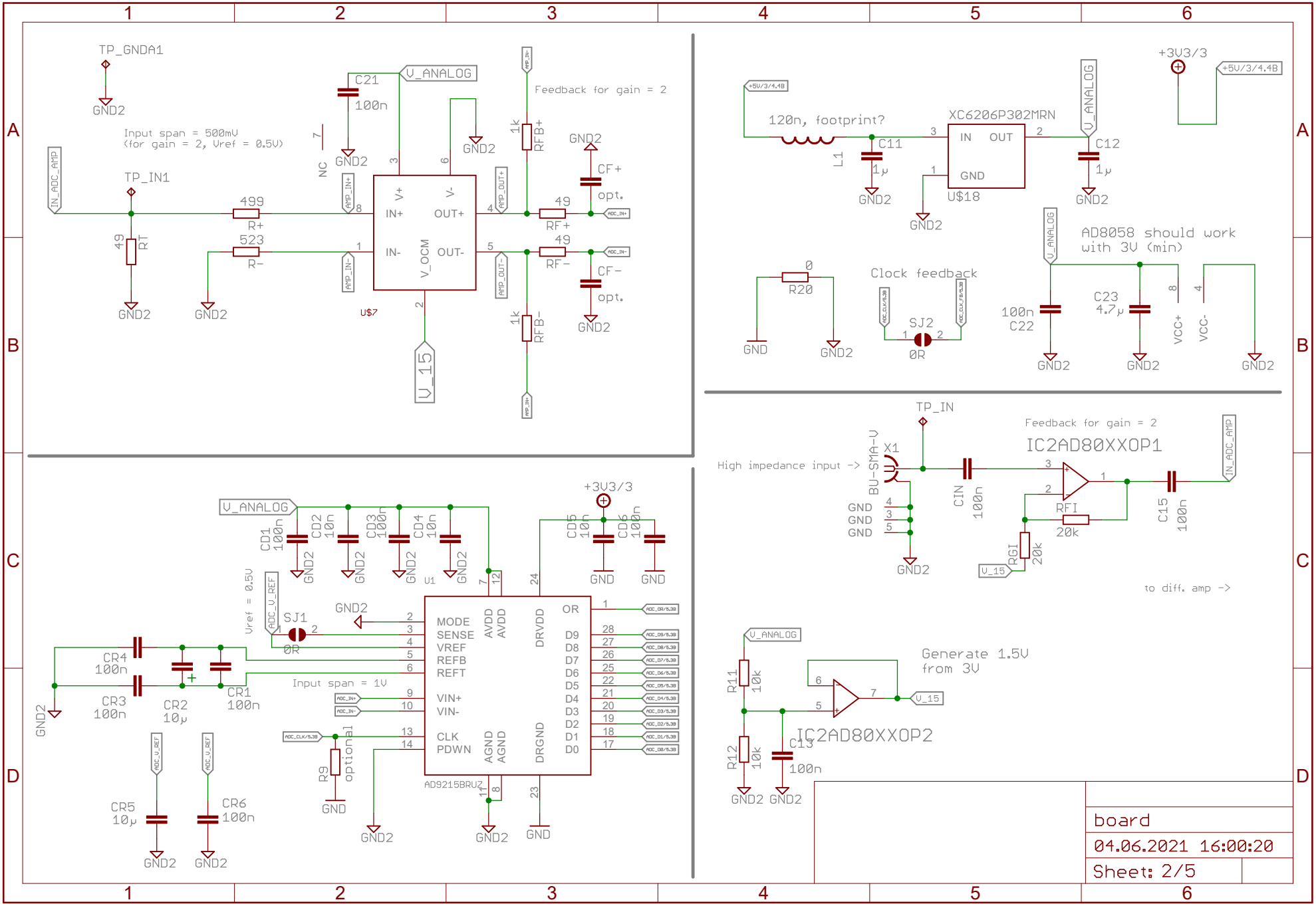
TP_GNDA1
GND2
Input span = 500mV
(for gain = 2, Vref = 0.5V)
IN_ADC_AMP
TP_IN1
499
R+
523
R-
49
RT
NC
C21
100n
V_ANALOG
AMP_IN+
AMP_IN-
IN+
IN-
V+
V-
OUT+
OUT-
V_OCM
U$7
V_15
AMP_OUT+
AMP_OUT-
Feedback for gain = 2
1k
RFB+
RFB-
49
RF+
RF-
CF+
CF-
opt.
ADC_IN+
ADC_IN-
+3V3/3
+5V/3/4.4B
120n, footprint?
L1
C11
1µ
XC6206P302MRN
IN
OUT
GND
U$18
C12
1µ
AD8058 should work
with 3V (min)
0
R20
GND
Clock feedback
SJ2
0R
100n
C22
C23
4.7µ
VCC+
VCC-
TP_IN
High impedance input ->
X1
BU-SMA-V
CIN
100n
Feedback for gain = 2
IC2AD80XXOP1
RFI
20k
RGI
20k
C15
100n
IN_ADC_AMP
to diff. amp ->
Generate 1.5V
from 3V
R11
10k
R12
10k
C13
100n
IC2AD80XXOP2
CD1
100n
CD2
10n
CD3
100n
CD4
10n
CD5
10n
CD6
100n
U1
Vref = 0.5V
ADC_V_REF
SJ1
0R
CR4
100n
CR3
100n
CR2
10µ
CR1
100n
Input span = 1V
MODE
SENSE
VREF
REFB
REFT
VIN+
VIN-
CLK
PDWN
AVDD
AGND
DRVDD
DRGND
OR
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
ADC_CLK/5.3B
R9
optional
AD9215BRUZ
CR5
10µ
CR6
100n
board
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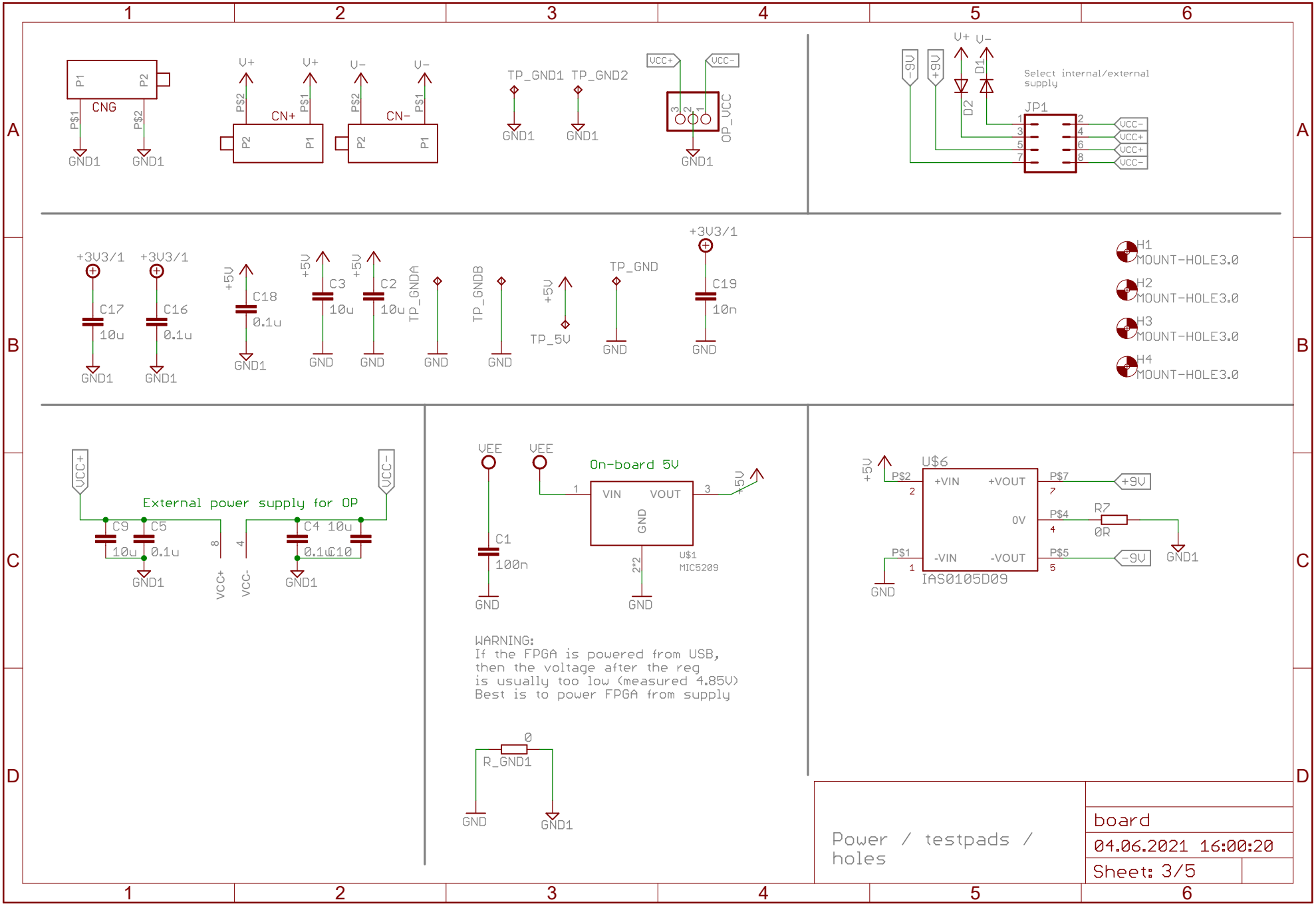

Power / testpads / holes

board

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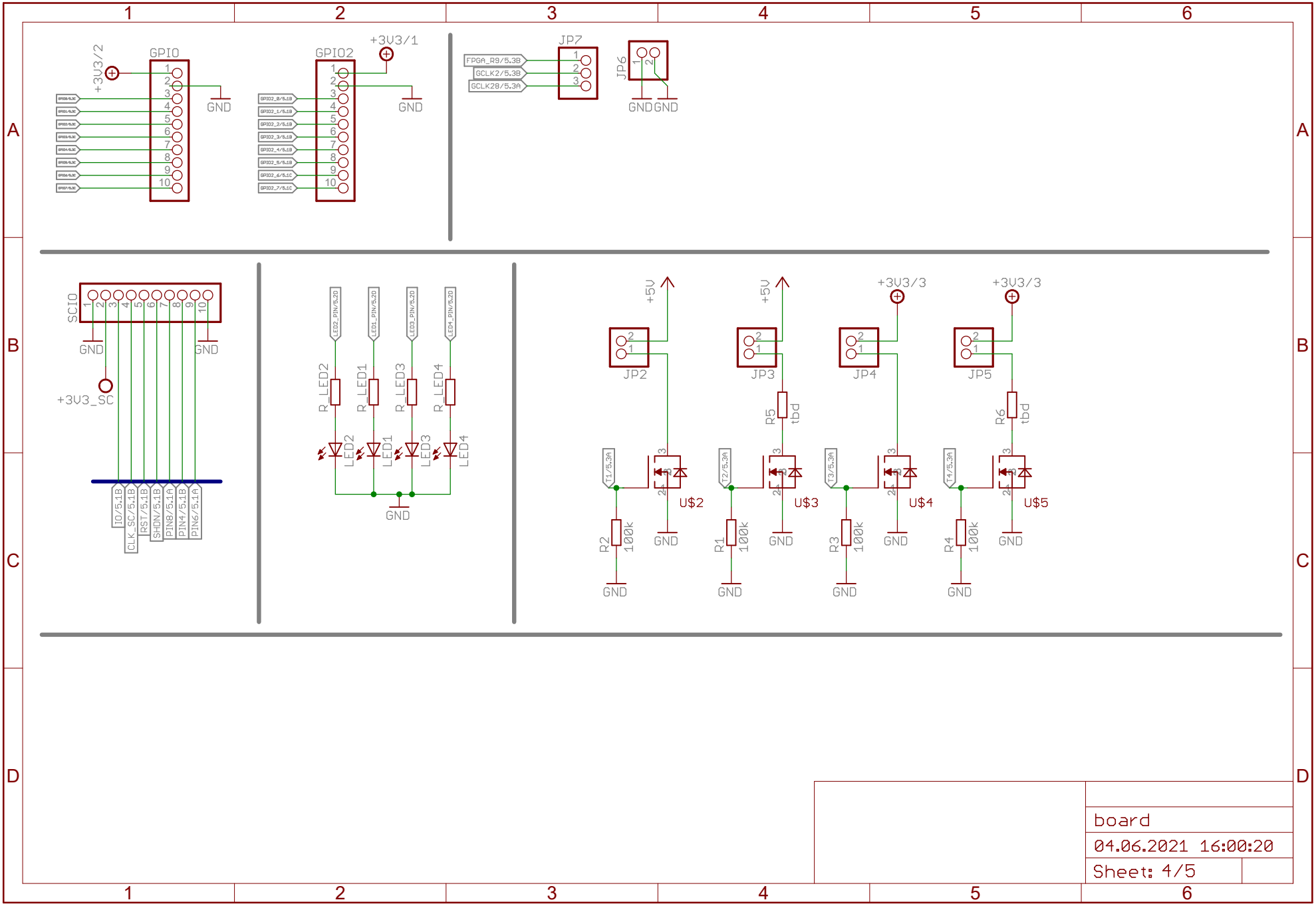

board

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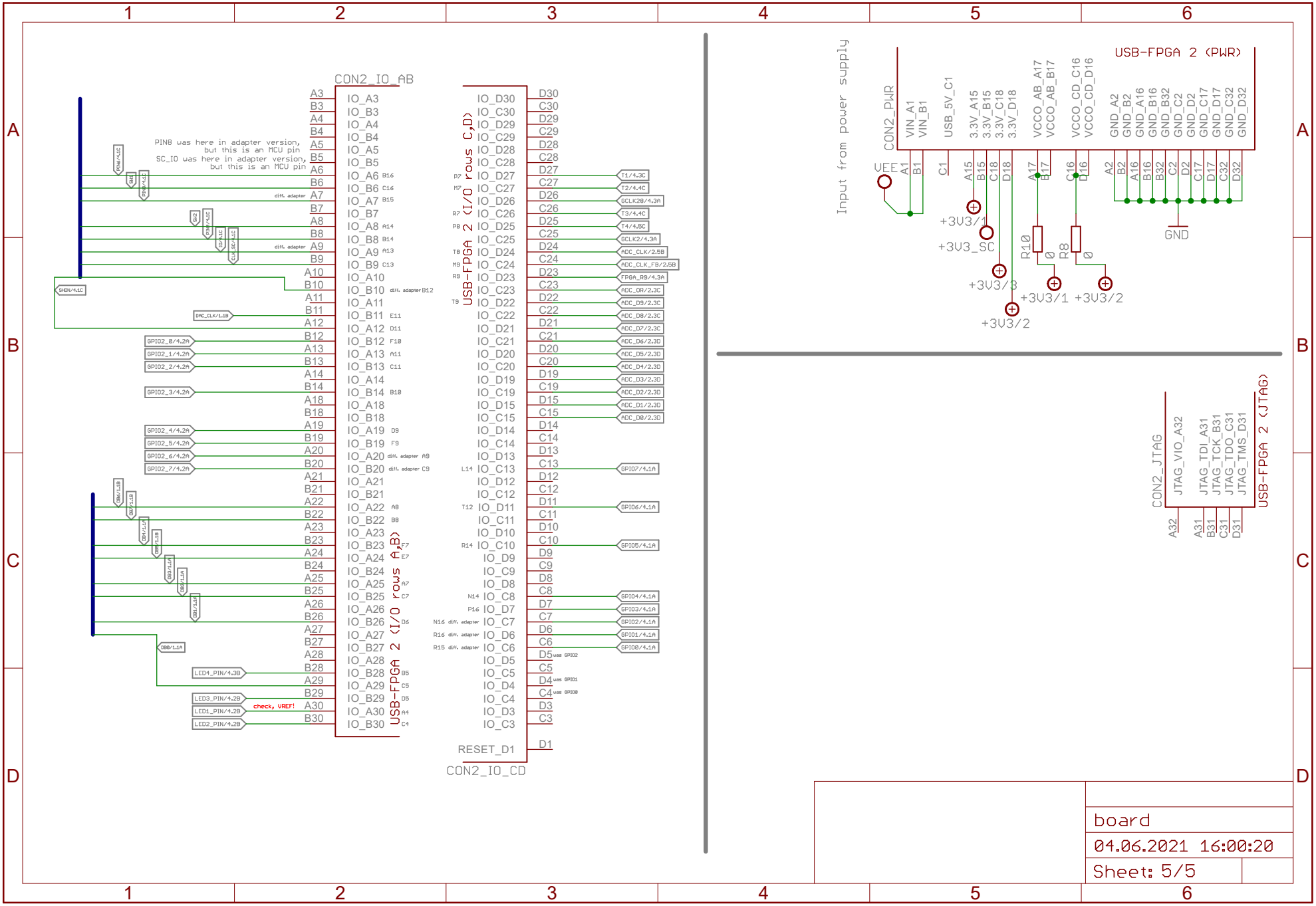
CON2_IO_AB
USB-FPGA 2 (I/O rows A,B)
USB-FPGA 2 (I/O rows C,D)
CON2_IO_CD
PIN8 was here in adapter version, but this is an MCU pin
SC_IO was here in adapter version, but this is an MCU pin
diff. adapter
check, VREF!
RESET_D1
CON2_PWR
USB-FPGA 2 (PWR)
Input from power supply
VIN_A1
VIN_B1
USB_5V_C1
3.3V_A15
3.3V_B15
3.3V_C18
3.3V_D18
VCCO_AB_A17
VCCO_AB_B17
VCCO_CD_C16
VCCO_CD_D16
GND_A2
GND_B2
GND_A16
GND_B16
GND_B32
GND_C2
GND_D2
GND_C17
GND_D17
GND_C32
GND_D32
GND
+3V3/1
+3V3_SC
+3V3/3
+3V3/2
R10
R8
CON2_JTAG
USB-FPGA 2 (JTAG)
JTAG_VIO_A32
JTAG_TDI_A31
JTAG_TCK_B31
JTAG_TDO_C31
JTAG_TMS_D31
board
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