CSE 560
Computer Systems Architecture

Final Exam Review

Logistics and Style

- Date and Time
  - Monday, Dec 18, 3:30 to 5:30pm, starting right at 3:30!
  - Not here! In McMillan G052
- Questions
  - Exam is comprehensive
  - Question 1 will be a collection of short answer things (e.g., true/false, fill in the blank, quick definition)
  - Questions 2 through N will be longer (going more in depth on a particular subject)
- One-page "crib sheet" is allowed
  - 8.5 x 11 sheet, front and back, whatever you want to include (content-wise)
- Calculator is allowed (but not required)

Instruction Set Architecture

- Definition
- Components
  - Machine instructions
  - Programmer-level memory model
  - Operating Modes
- What isn't included in the ISA, e.g.,
  - Pipelined execution
  - Branch predictors
  - Caches

Performance

- Metrics
- Fundamental Equation

$$\frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

- Benchmarks
- Architectural Simulation
- Memory

$$t_{AVG} = t_{HIT} + \%miss \times t_{MISS}$$

Technology

- Moore's Law
- Transistor Properties
  - Implications of scaling
    - Cost
    - Speed
    - Power and Energy
    - Reliability

Pipelining

- 5-stage example pipeline
  - Data dependencies
  - Hazards
  - Bypassing (forwarding)
- Pipeline diagrams (in-order and out-of-order)
- Multi-cycle operations
  - Pipelined functional units (e.g., multiplier)

Branch Prediction

- Why?
- How?
  - Classic types
- Where?
  - Esp. in context of 5-stage pipeline
- Performance implications?

Parallel Pipelines

- Superscalar
  - In-order execution
  - Out-of-order execution
- Scheduling
  - In-order and out-of-order
  - Single issue and multiple issue
  - ISA extensions – predication
- More pipeline diagrams!

Caches

- Locality
- How they work
  - Direct mapped
  - Fully associative
  - Set associative
- Cache coherence
  - VI, MSI, and MESI protocols
  - Snooping, Directory-based

Virtual Memory

- Uses
  - Isolation
  - Protection
  - "Caching" of main memory
- Mechanisms
  - Address translation
  - Page faults
  - TLBs
- Full memory hierarchy

Multcores

- Shared memory model
  - Multiplexed uniprocessor
  - Hardware multithreading
  - Multiprocessing
- Synchronization
  - Locks
- Memory consistency models

Multiprocessors

- Flynn's taxonomy
- Physically distributed memory
- Cluster interconnects
  - Virtualization
- Custom interconnects
- Programming paradigms
  - MPI
- Graphics engines and systolic arrays

Time for Q&A

- We'll start right at 3:30pm on Dec 18
- Comprehensive, slight emphasis on material since the midterm exam
- One page "crib sheet" allowed (both sides)
- Calculator OK but not required