



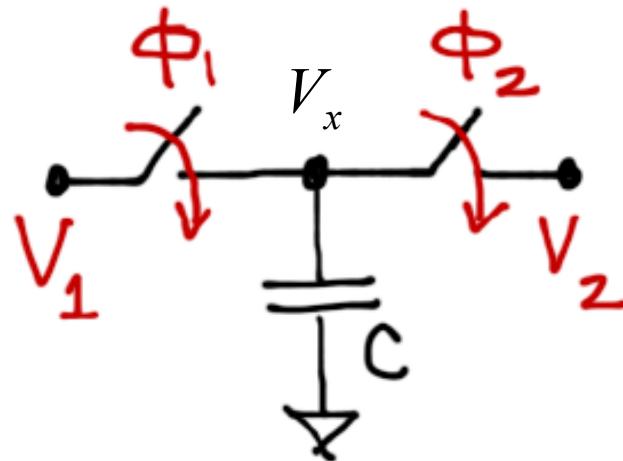
# Fundamental Switched Capacitor Circuits



CSE562: Analog Integrated Circuits  
**Shantanu Chakrabartty**



# Basic Switched Capacitor Element



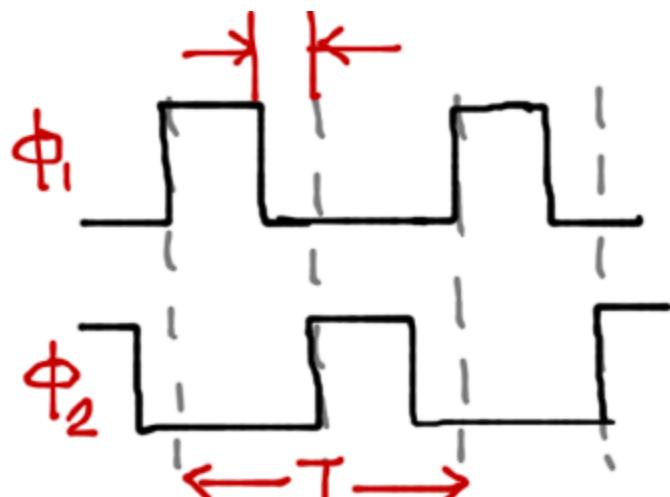
Phase 1

$$\Phi_1 = 1, \Phi_2 = 0$$

Charge on the capacitor  $Q_1 = CV_1$

$$\Phi_1 = 0, \Phi_2 = 0$$

Charge on the capacitor still remains  $CV_1$



Phase 2

$$\Phi_1 = 0, \Phi_2 = 1$$

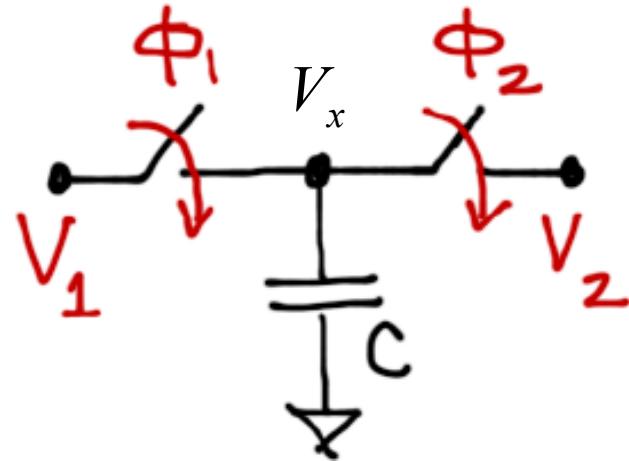
Charge on the capacitor  $Q_2 = CV_2$

$$\Delta Q = Q_1 - Q_2 = C(V_1 - V_2)$$

Current  $I = \frac{\Delta Q}{T} = \frac{C}{T}(V_1 - V_2)$



# Basic Switched Capacitor Element



Current  $I = \frac{\Delta Q}{T} = \frac{C}{T}(V_1 - V_2)$

Current  $I = \frac{1}{R}(V_1 - V_2)$

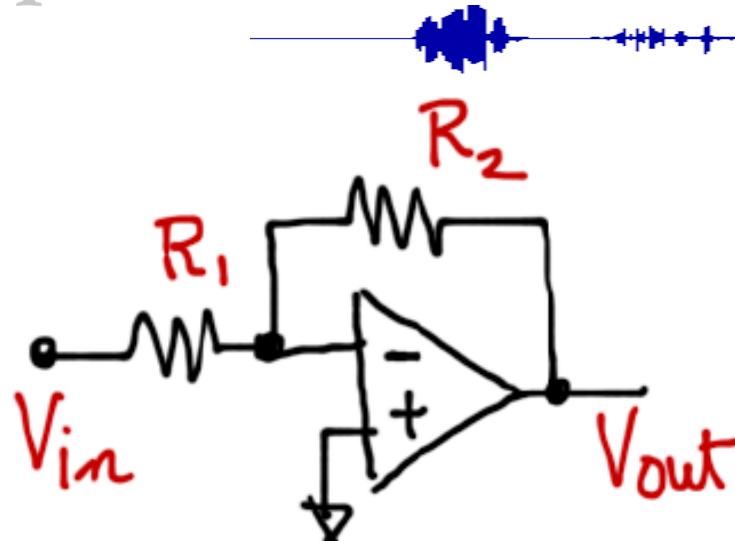
Switched capacitor equivalent resistance

$$R = \frac{T}{C} = \frac{1}{Cf}$$

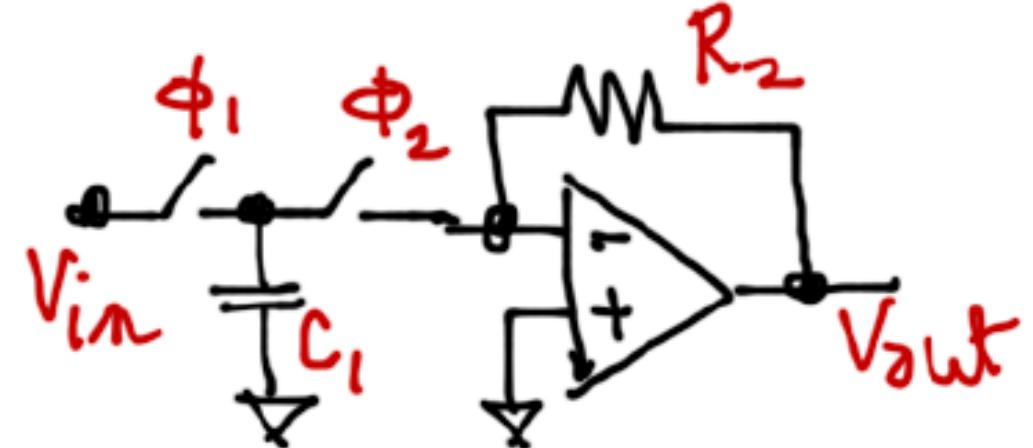
## Disadvantages

- Small resistance – High clock frequency and large capacitance.
- Large resistance – Low clock frequency and small capacitance.

# Replace all resistors

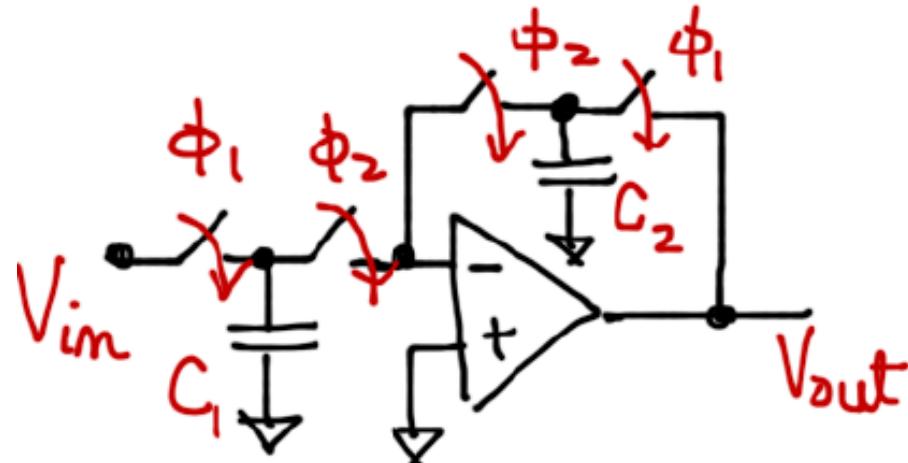


$$\text{Output } V_{out} = -\frac{R_2}{R_1} V_{in}$$

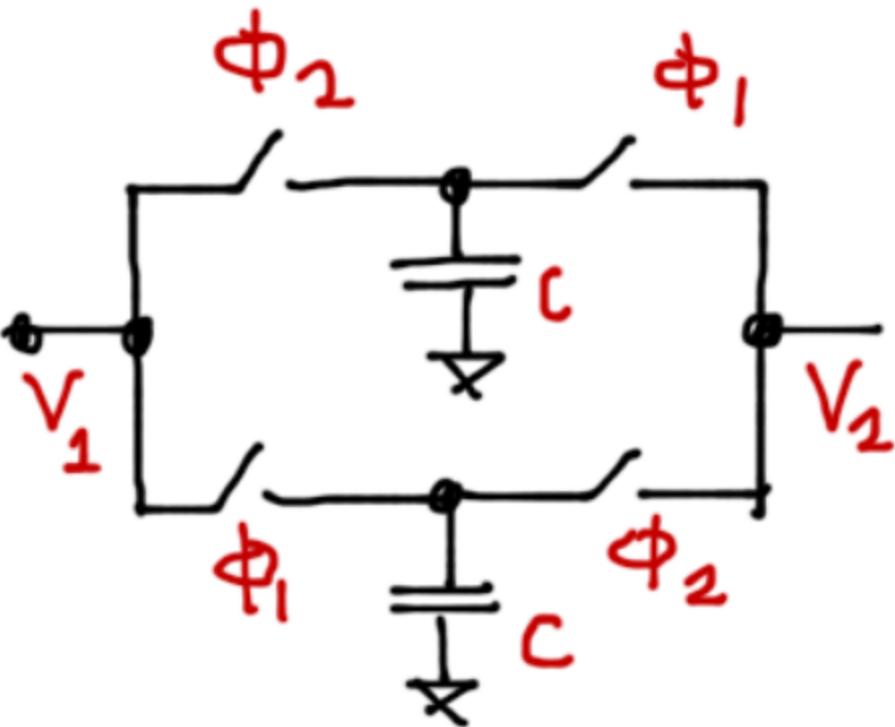


$$\text{Output } V_{out} = -R_2 f C_1 V_{in}$$

What about this circuit ?



# Calculate the equivalent resistance



$$\Delta Q = 2C(V_1 - V_2)$$

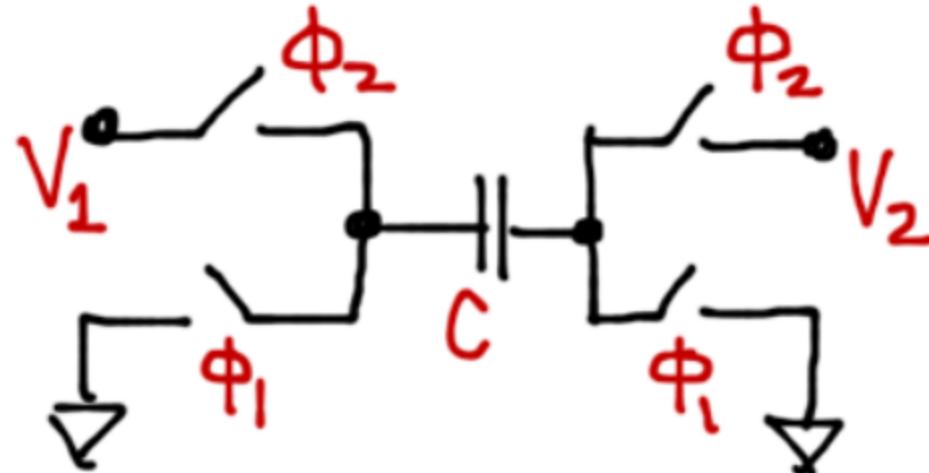
Current

$$I = \frac{\Delta Q}{T} = \frac{2C}{T}(V_1 - V_2)$$

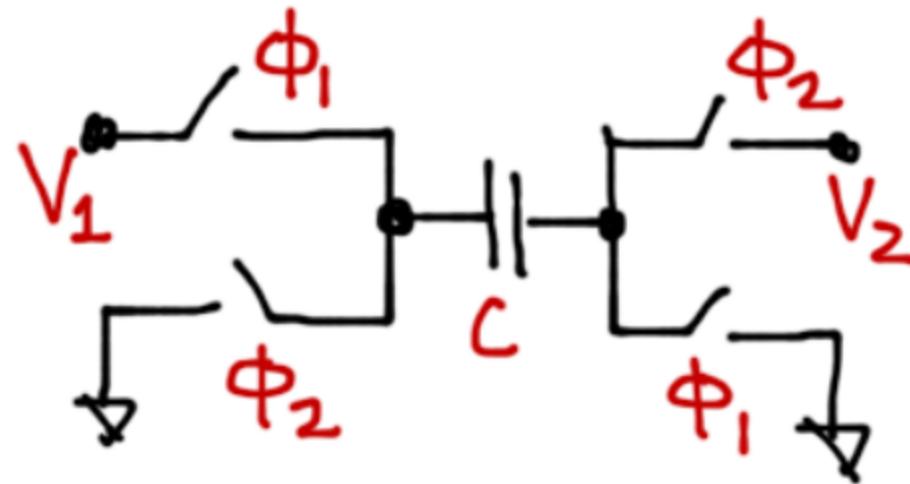
$$R = \frac{T}{2C} = \frac{1}{2Cf}$$



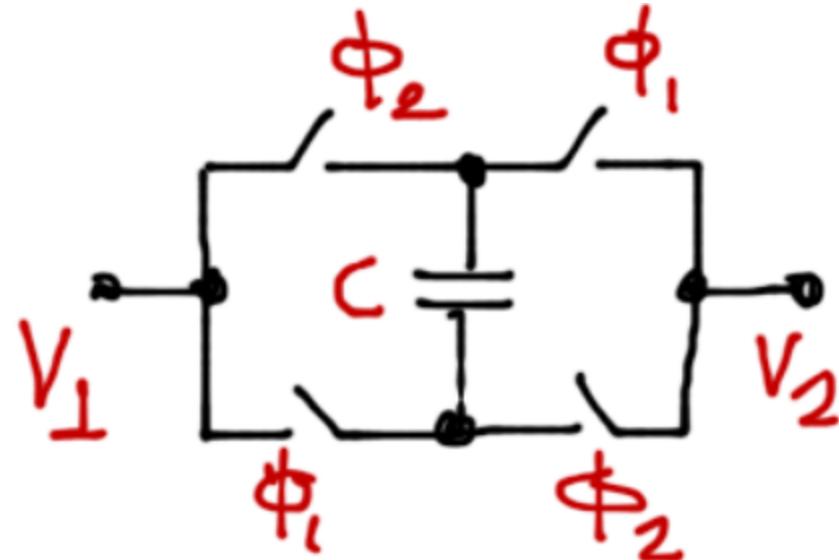
# Worksheet: Find equivalent resistance.



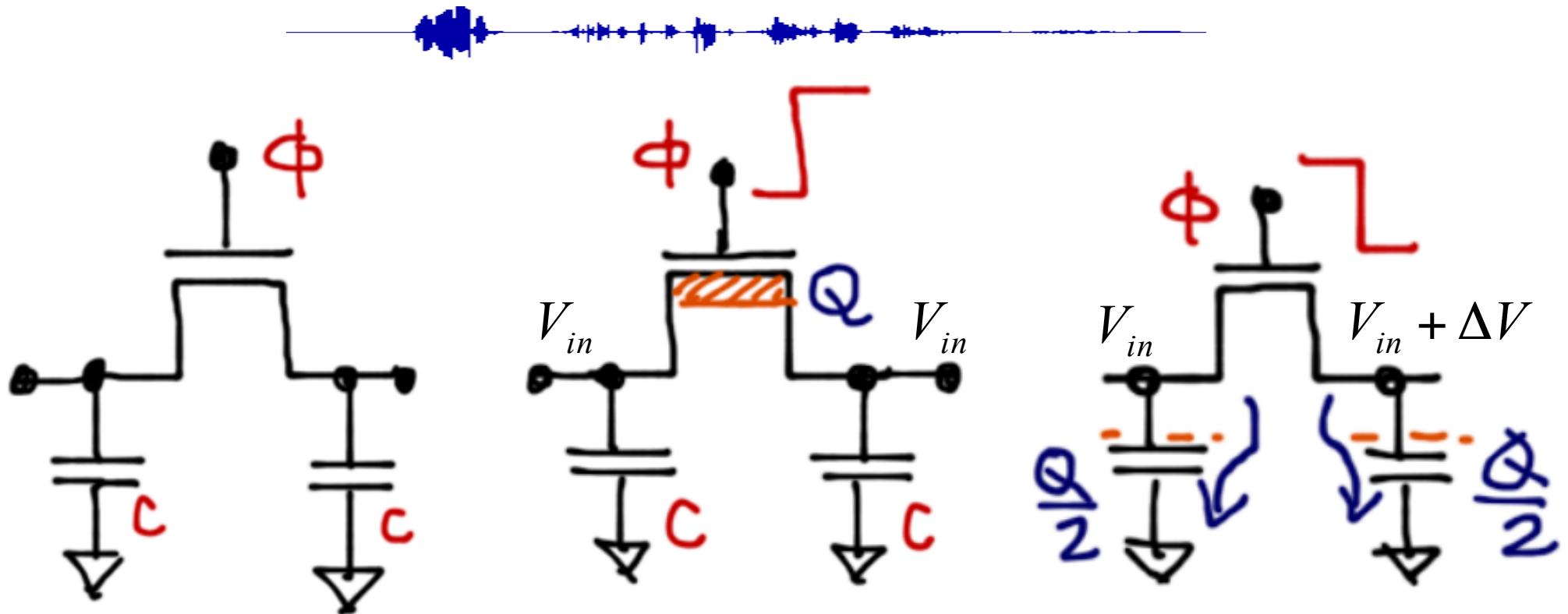
# Worksheet: Find equivalent resistance.



# Worksheet: Find equivalent resistance.



# Effect of non-ideal switches

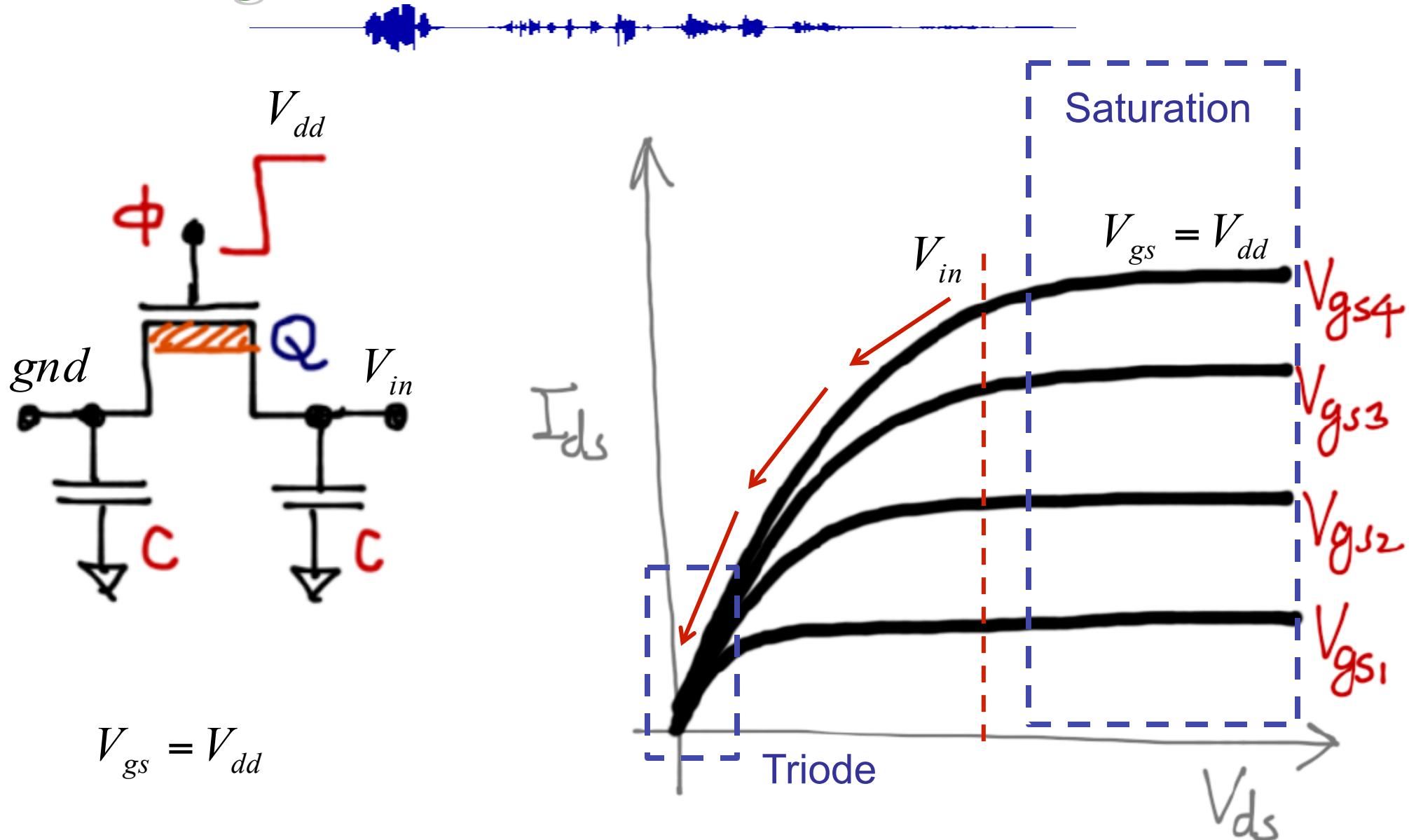


- When the transistor Q3 turns off, half the charge flows into the input capacitor (Charge injection).

$$\Delta V = \frac{(Q/2)}{C} = \frac{V_{eff} C_{ox} WL}{2C} = \frac{(V_{DD} - V_{in} - V_{th}) C_{ox} WL}{2C}$$

- Error is a dependent on the source/drain voltage (problem !)

# Discharge Characteristics of an nMOS



- A MOSFET switch most of the time operates in the triode region.

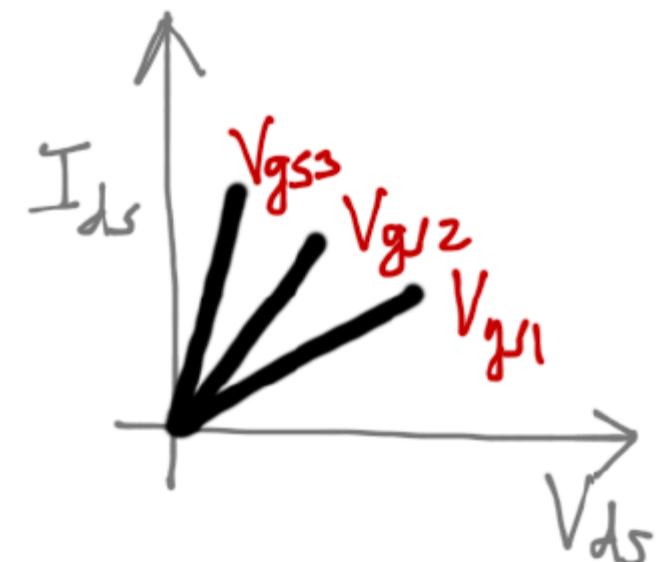
# Finite resistance of MOSFET switch

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2]$$

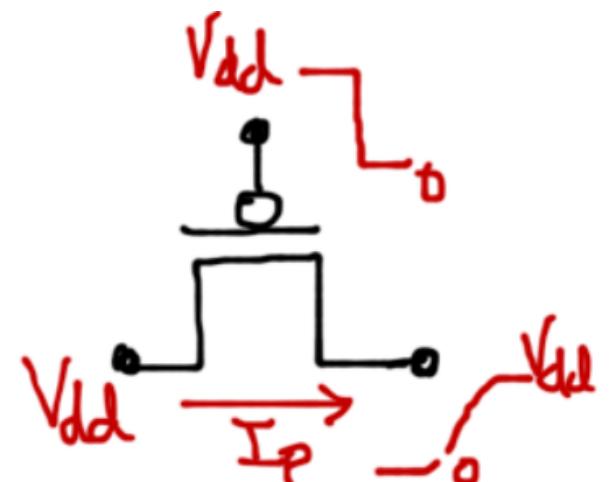
$$V_{DS} \ll 2(V_{GS} - V_{TH})$$

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

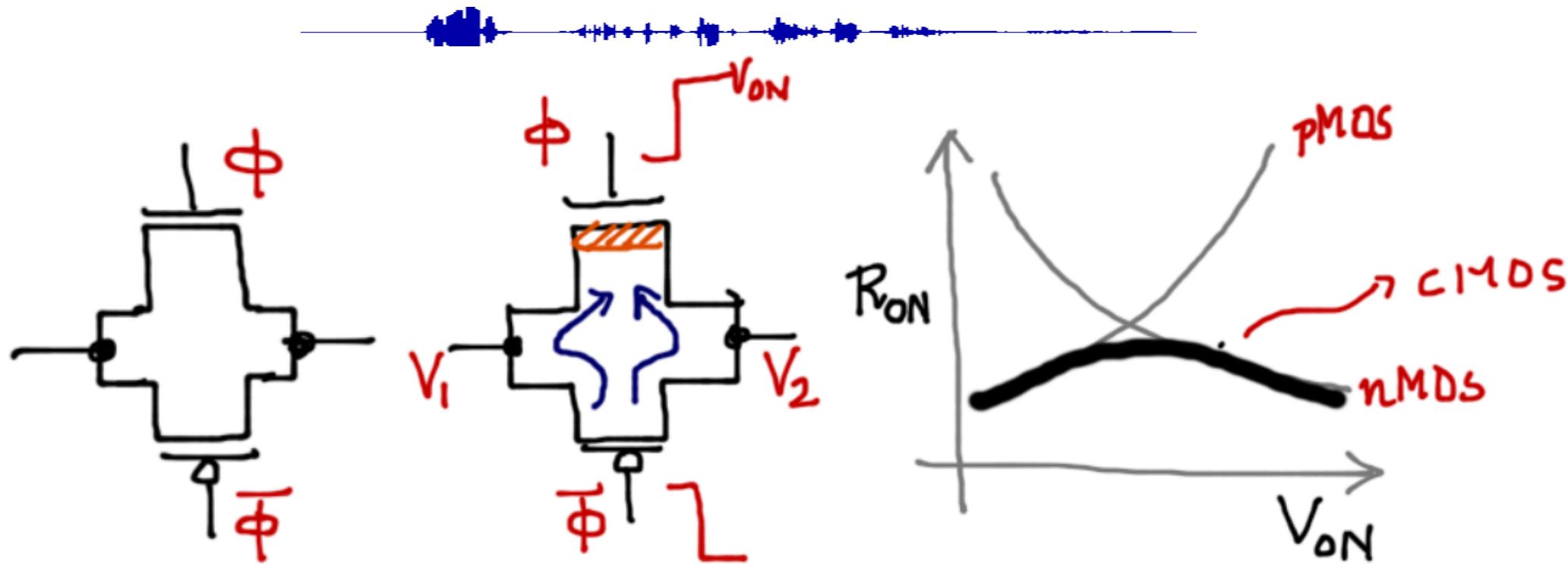
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$



- An nMOS switch is good for transmitting low voltages (close to gnd).
- A pMOS switch is good for transmitting high voltages (close to vdd).

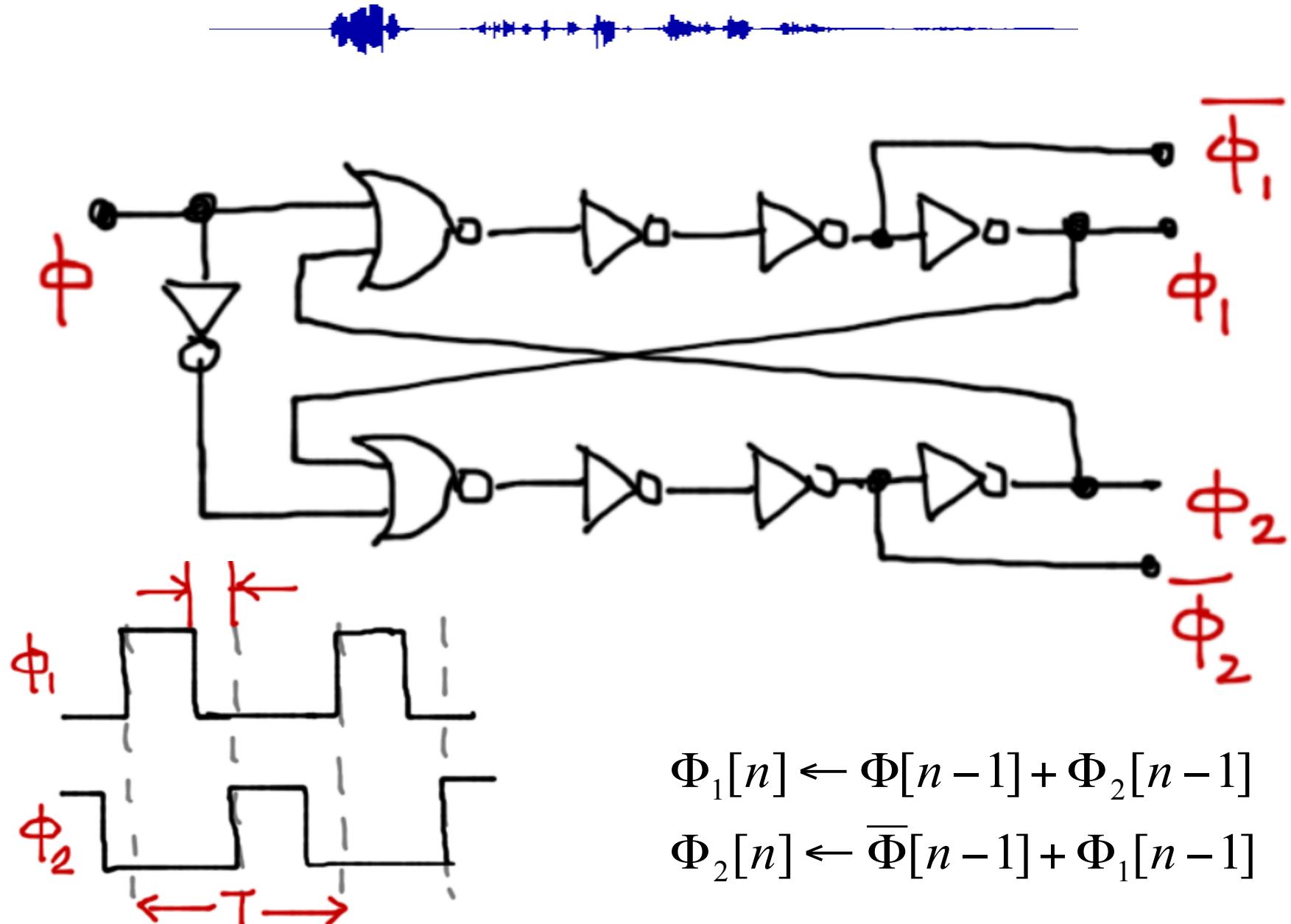


# CMOS Switch



- CMOS switch consists of a complementary pMOS and nMOS transistor.
- If transistor sizes are carefully chosen – reduced charge injection.
- Reduced ON resistance.

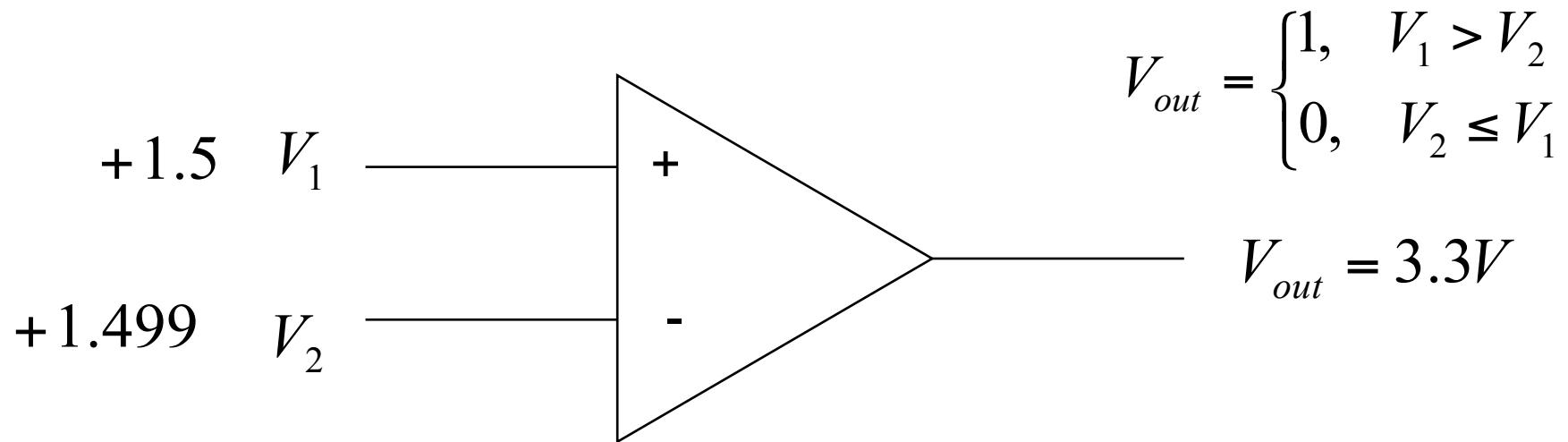
# Clock Generator Circuit



# Comparator



A comparator compares two ANALOG signals and produces a boolean (binary) output.

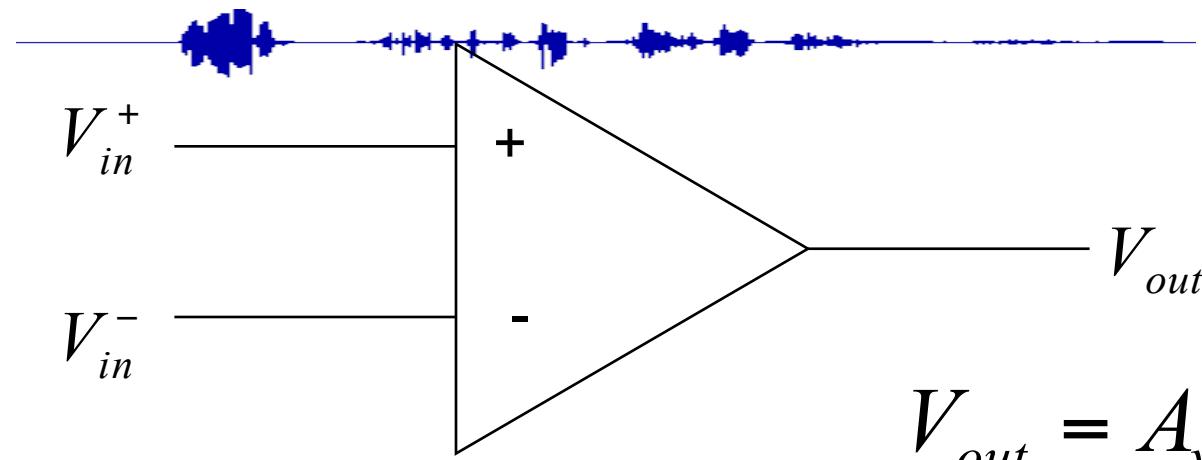


Op-amps in an open loop configuration are typically used for comparing analog signals. Requires very high gain (precise value of the gain is not important) !!!! Large signal behavior.

Accuracy of a comparator is determined by its OFFSET VOLTAGE.

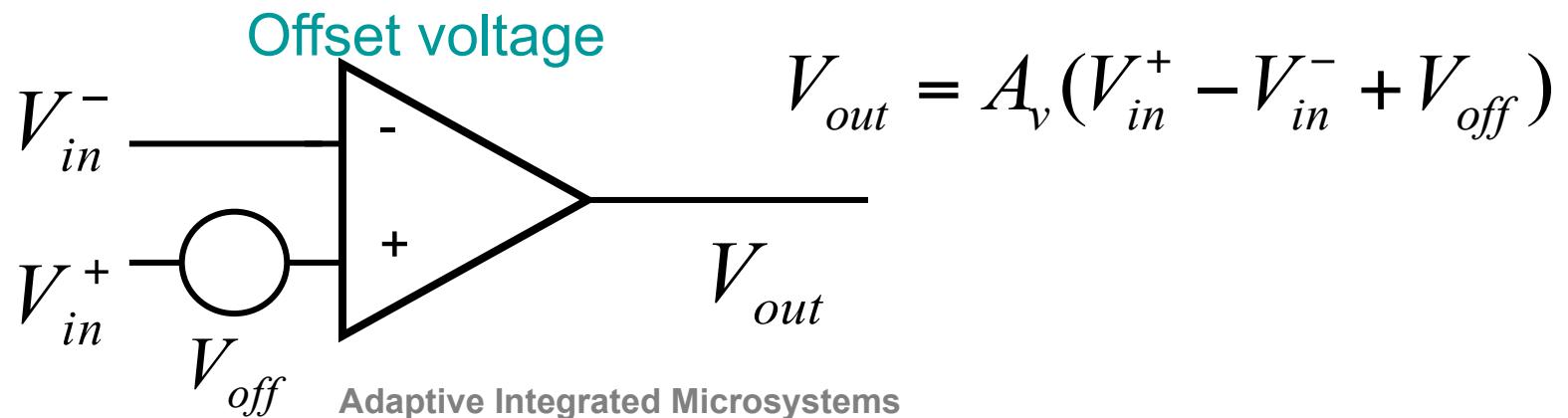


# Offset



Ideal :  $V_{in}^+ = V_{in}^-$  then  $V_{out} = 0$  Assumes symmetry

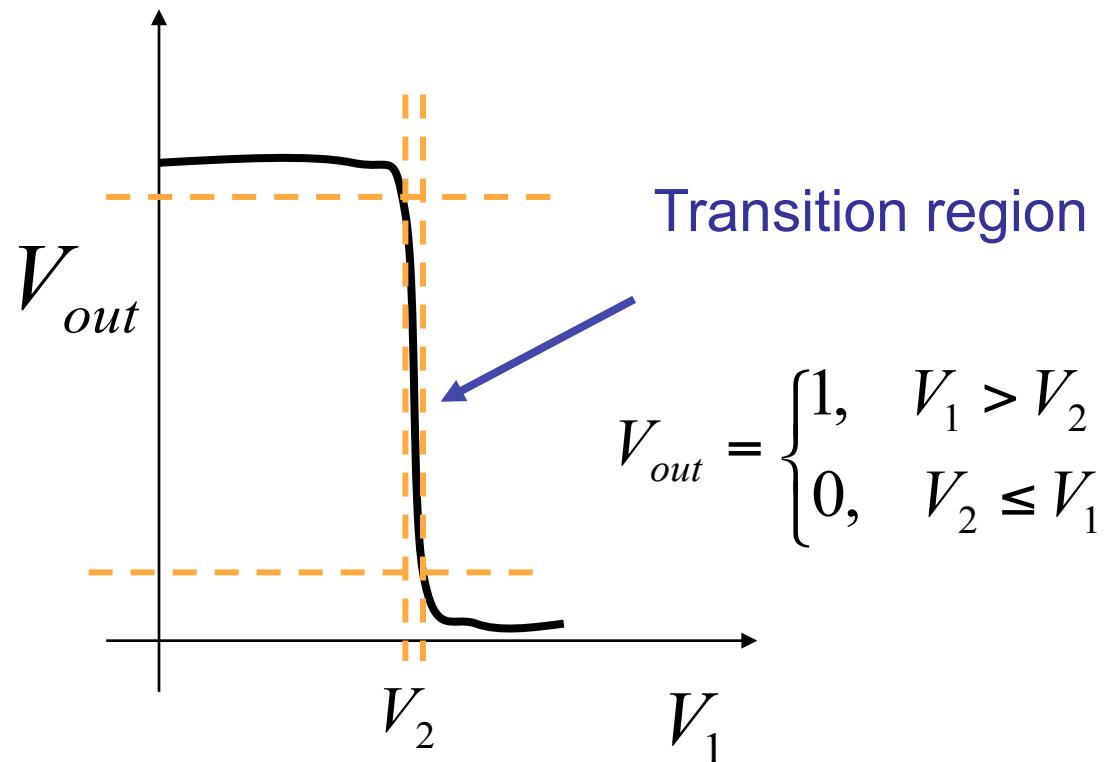
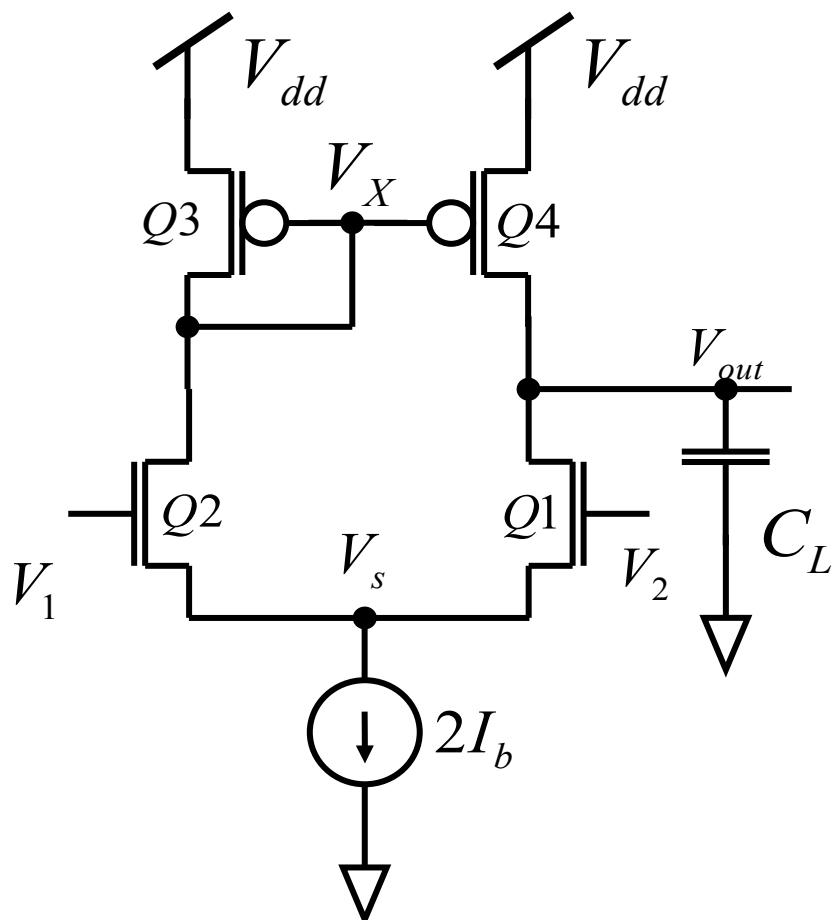
Non-ideal case:  $V_{in}^+ = V_{in}^- + V_{off}$  then  $V_{out} = 0$



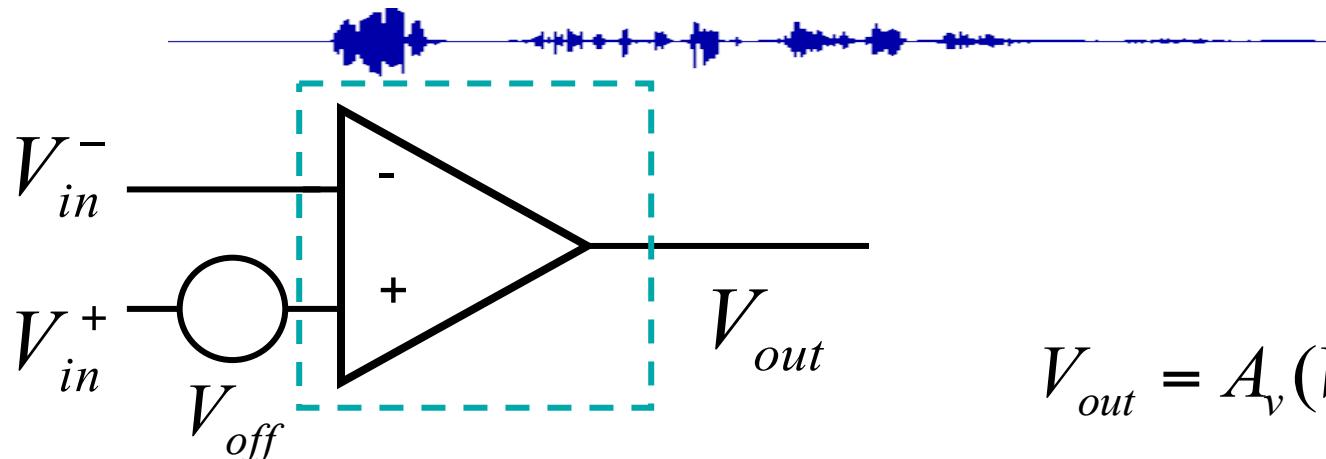
# Origins of Offset



Fully differential amplifier offset between two branches occur due to mismatch (mirrors, transistor sizes).



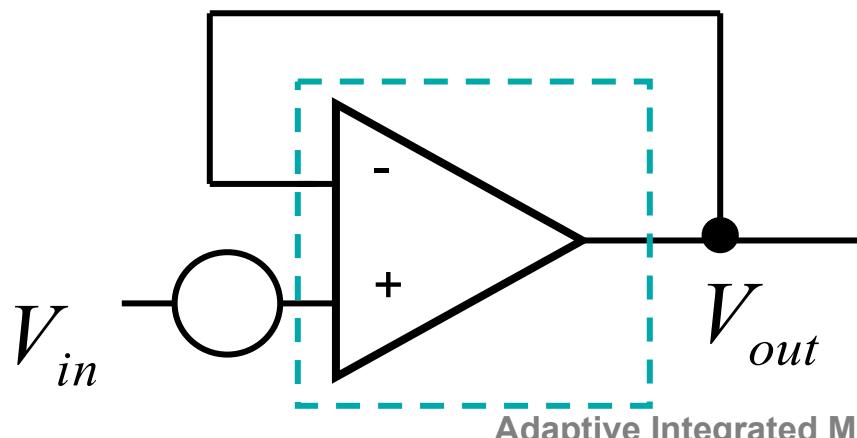
# How to calculate offset ?



$$V_{out} = A_v(V_{in}^+ - V_{in}^- + V_{off})$$

-Offset voltage slowly varies with time, depending on temperature and other environmental condition.

-Offset voltage is dependent on the gain of the amplifier. Higher the gain, smaller is the offset. Even though offset voltage has been assumed to be constant, it slowly varies with time.

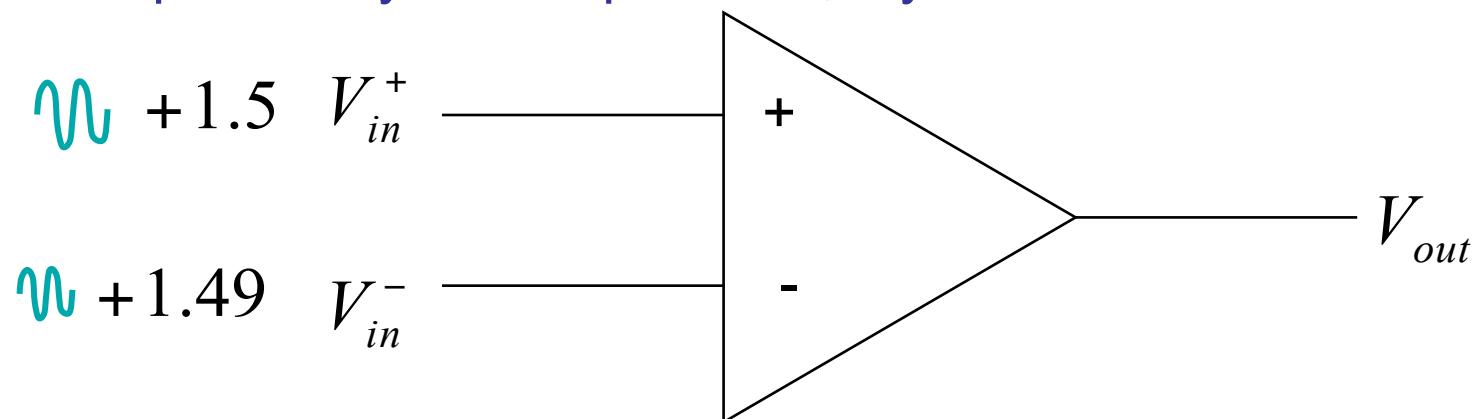


$$V_{out} \approx V_{in} + V_{off}$$

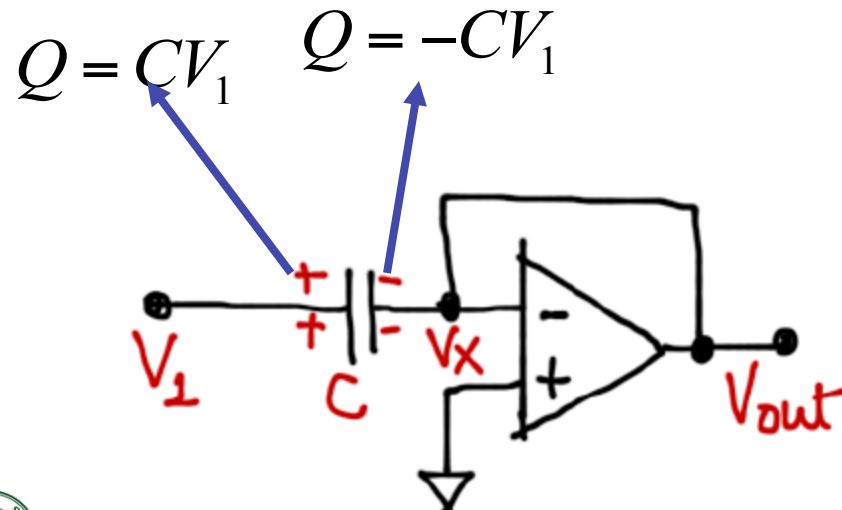
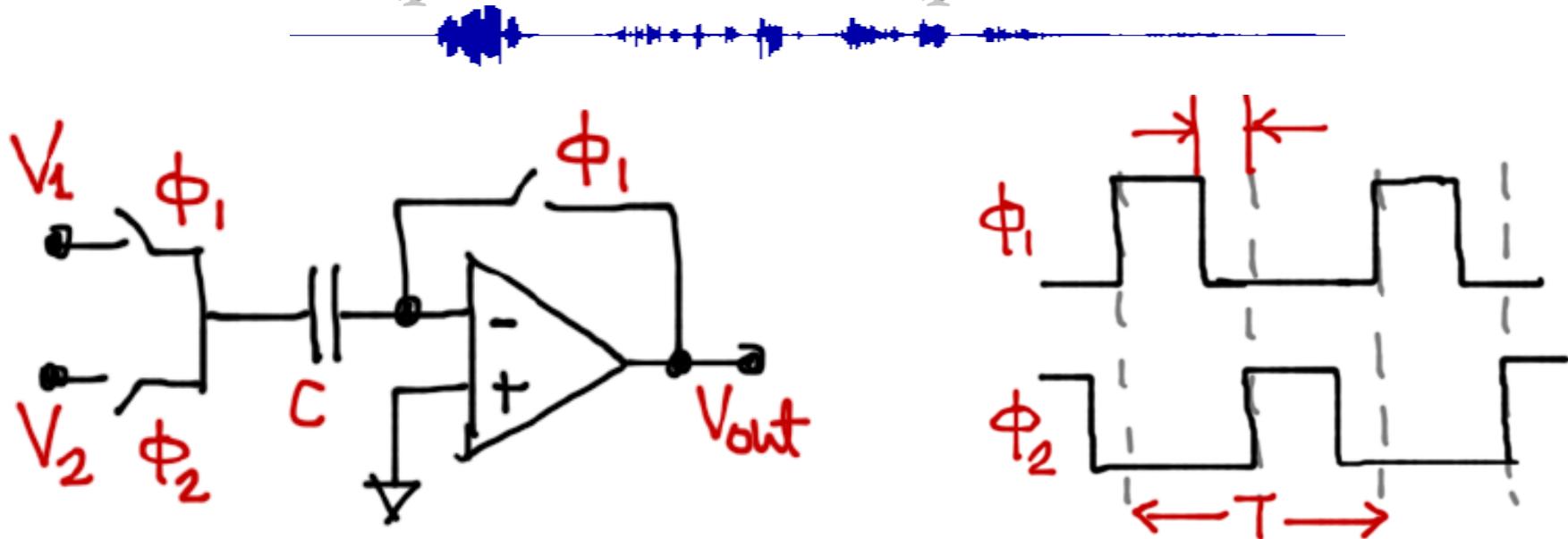
# Problems with Offsets



- Typical offset voltage is in the range of 5-10mV. Commercial comparators achieve offsets in the range of micro-volts.
- Comparator produces an error when comparing analog signals less than the offset voltage.
- Comparison will be dependent on offset voltage which will introduce dependency on temperature, layout of the devices.



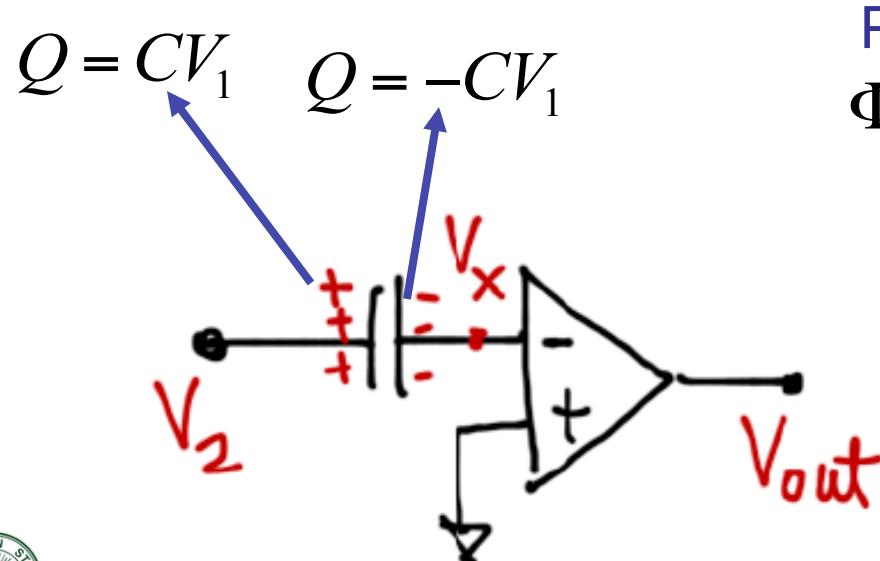
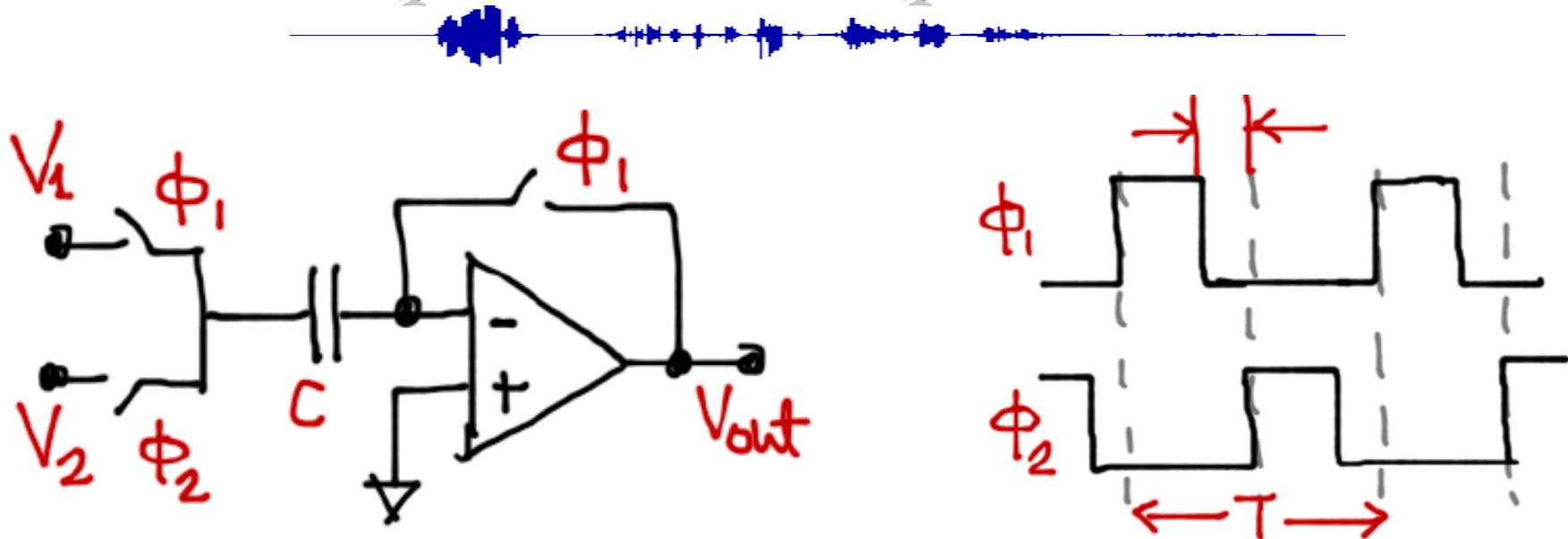
# Offset Compensated Comparator



Phase 1  
 $\Phi_1 = 1, \Phi_2 = 0$

$$V_x = 0$$

# Offset Compensated comparator



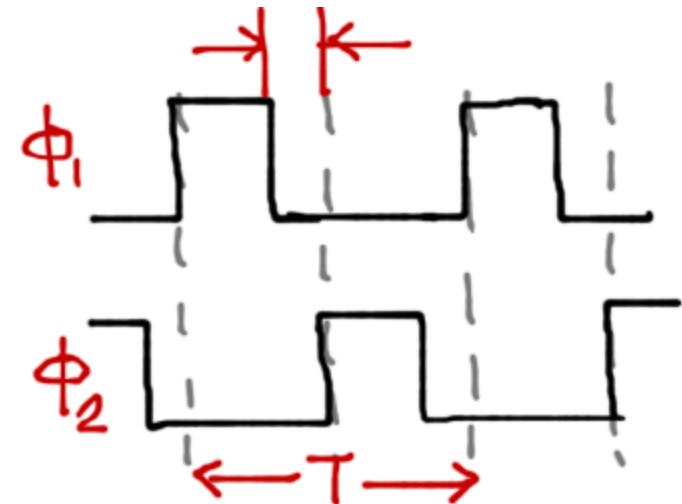
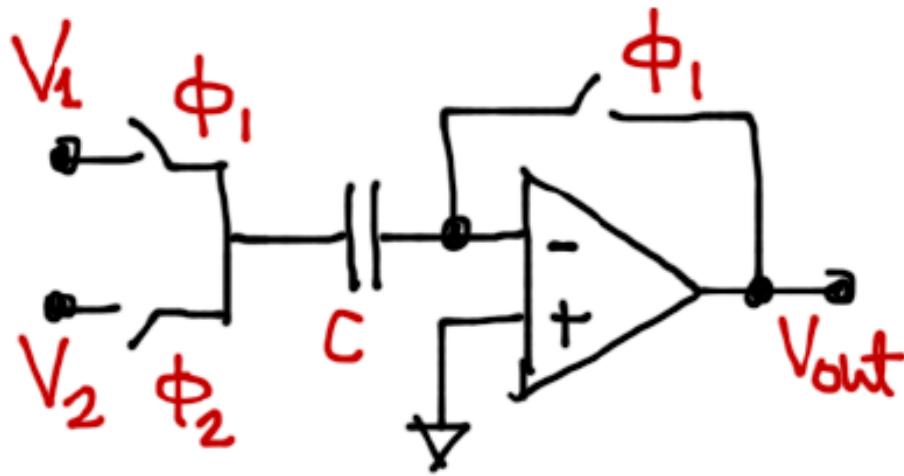
Phase 2  
 $\Phi_1 = 0, \Phi_2 = 1$

$$C(V_2 - V_x) = CV_1$$

$$V_x = V_2 - V_1$$

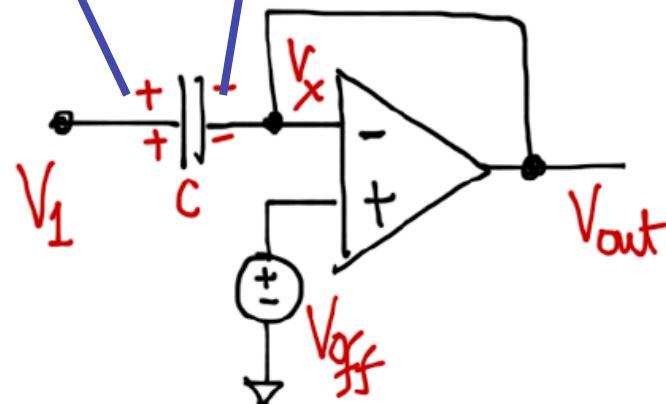
$$V_{out} = \begin{cases} 1, & V_1 > V_2 \\ 0, & V_2 \leq V_1 \end{cases}$$

# Offset Compensated Comparator



$$Q = C(V_1 - V_{off})$$

$$Q = -C(V_1 - V_{off})$$

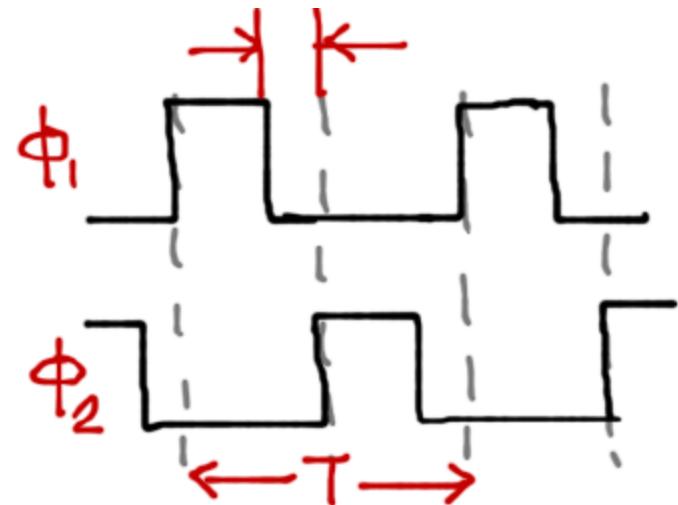
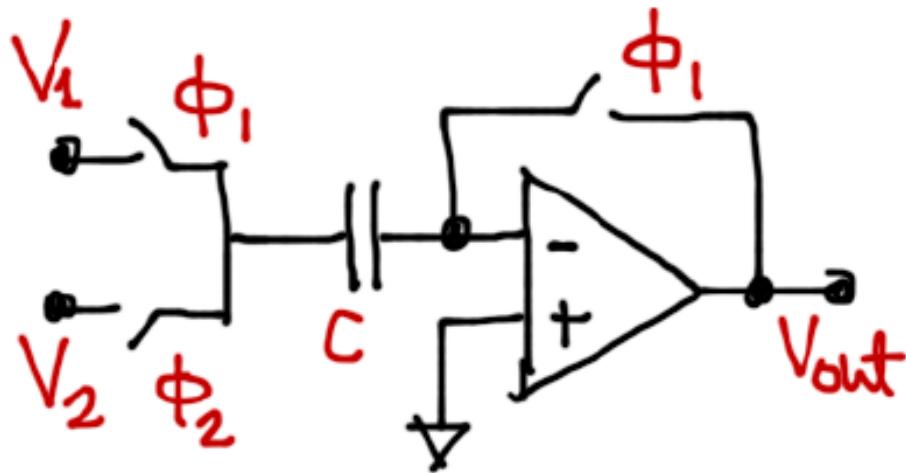


Phase 1  
 $\Phi_1 = 1, \Phi_2 = 0$

$$V_x = V_{off}$$

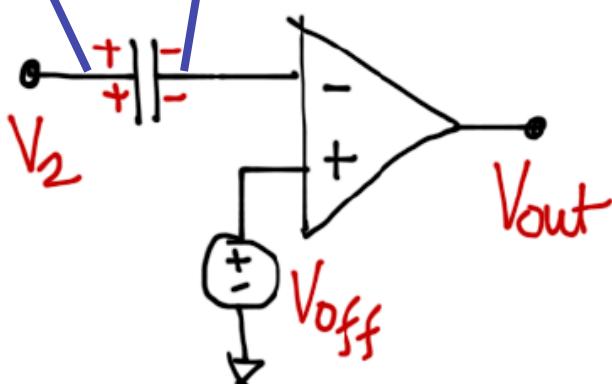


# Offset Compensated Comparator



$$Q = C(V_1 - V_{off})$$

$$Q = -C(V_1 - V_{off})$$



Phase 1

$$\Phi_1 = 0, \Phi_2 = 1$$

$$C(V_2 - V_x - V_{off}) = C(V_1 - V_{off})$$

$$V_x = V_2 - V_1$$

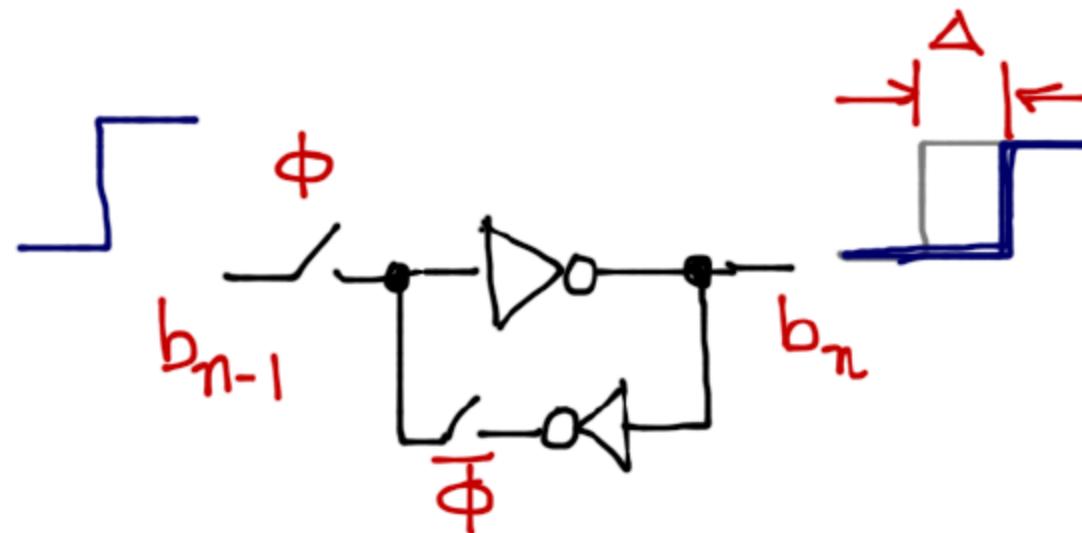
$$V_{out} = \begin{cases} 1, & V_1 > V_2 \\ 0, & V_2 \leq V_1 \end{cases}$$



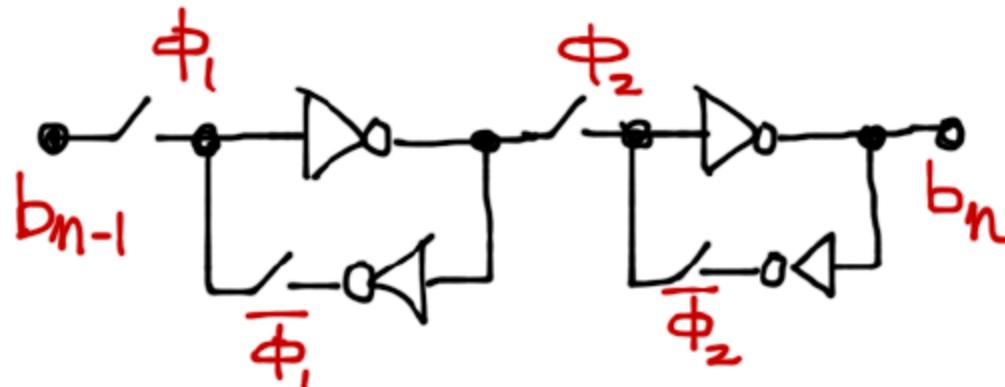
# Delays and Shift-registers



Simple Latch – can delay the input digital signal by one clock cycle.



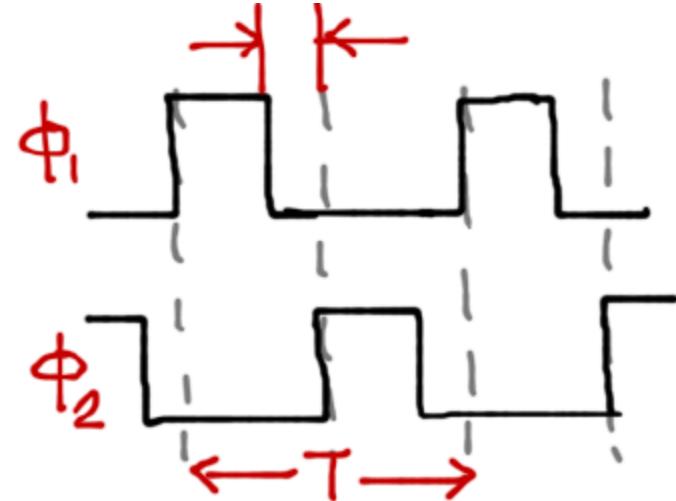
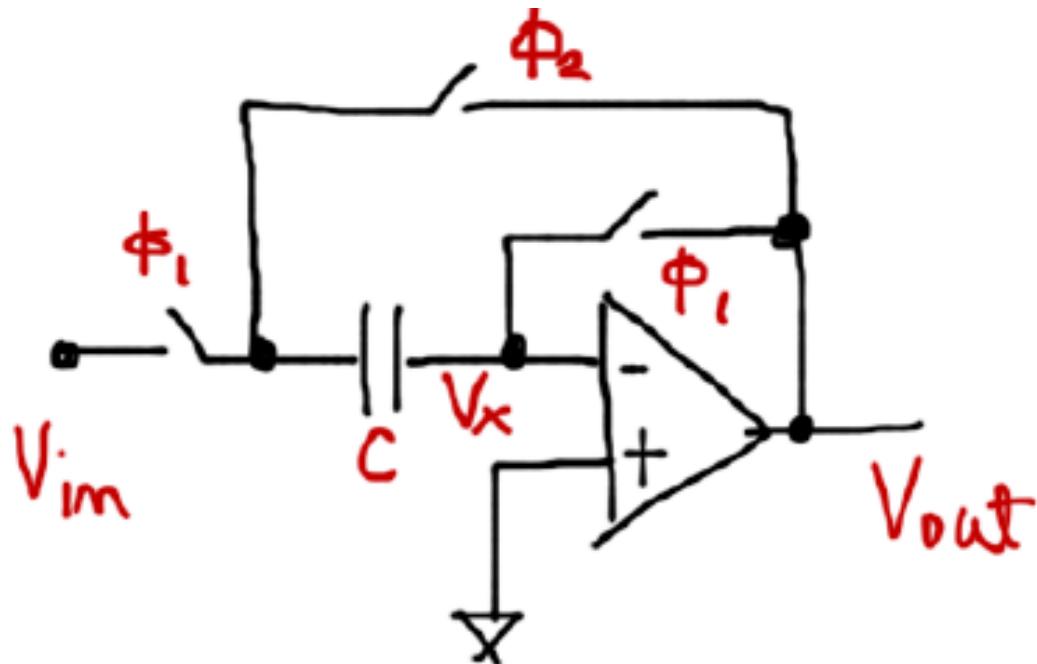
D flip-flop – can delay the input digital signal by one non-overlapping clock cycle.



# Circuit 1: Sample and Hold



- Samples the input voltage in one clock cycle and holds the sampled value during the next clock cycle – analog storage.

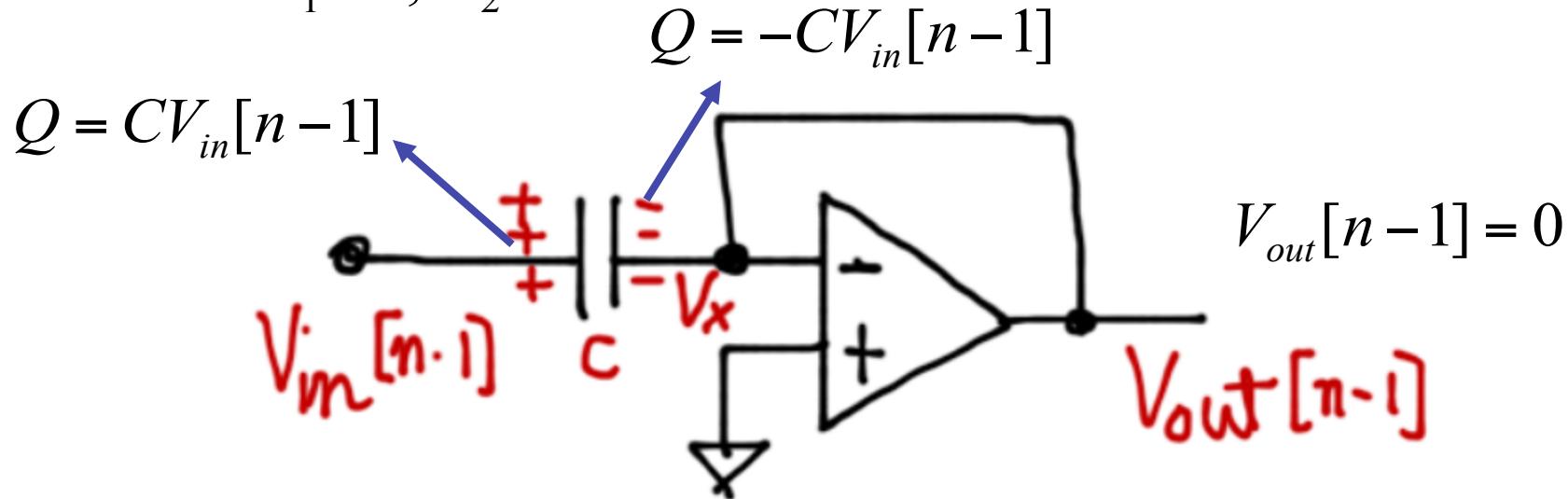


- Identify the equivalent circuit during each clock phase.  
 $\Phi_1 = 1, \Phi_2 = 0$   
 $\Phi_1 = 0, \Phi_2 = 1$

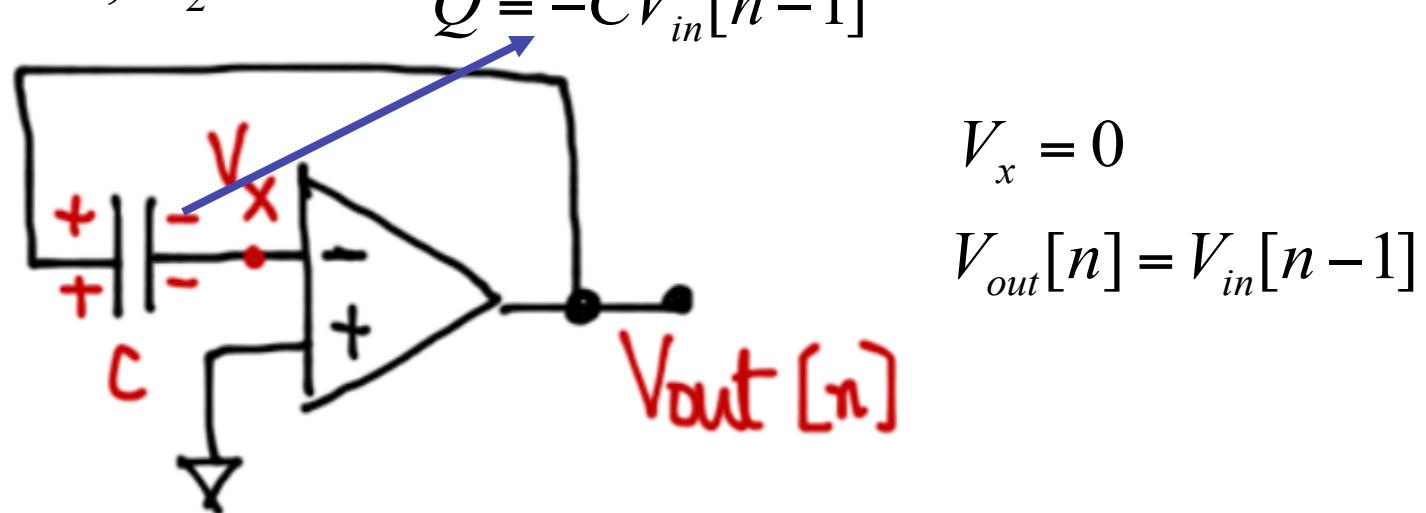
# Analysis



Phase 1:  $\Phi_1 = 1, \Phi_2 = 0$



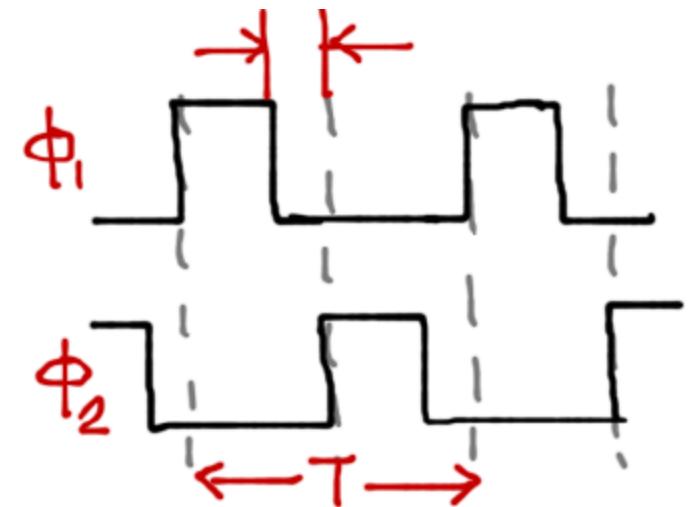
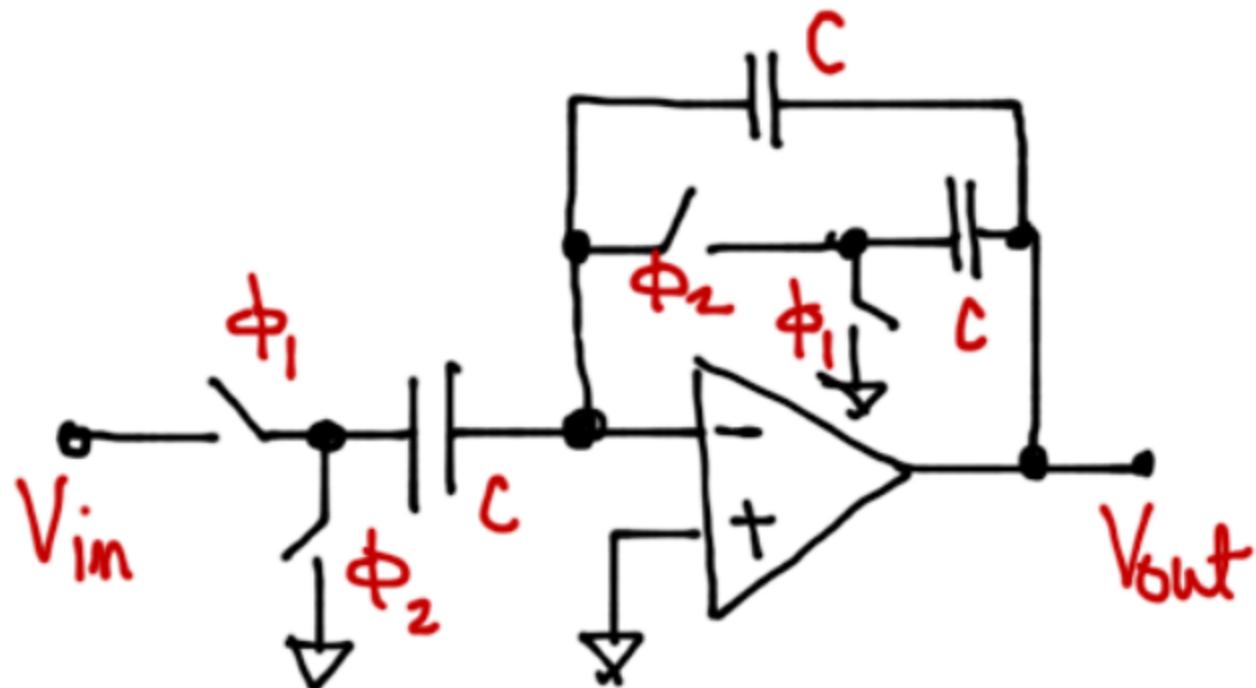
Phase 2:  $\Phi_1 = 0, \Phi_2 = 1$



# Circuit 2



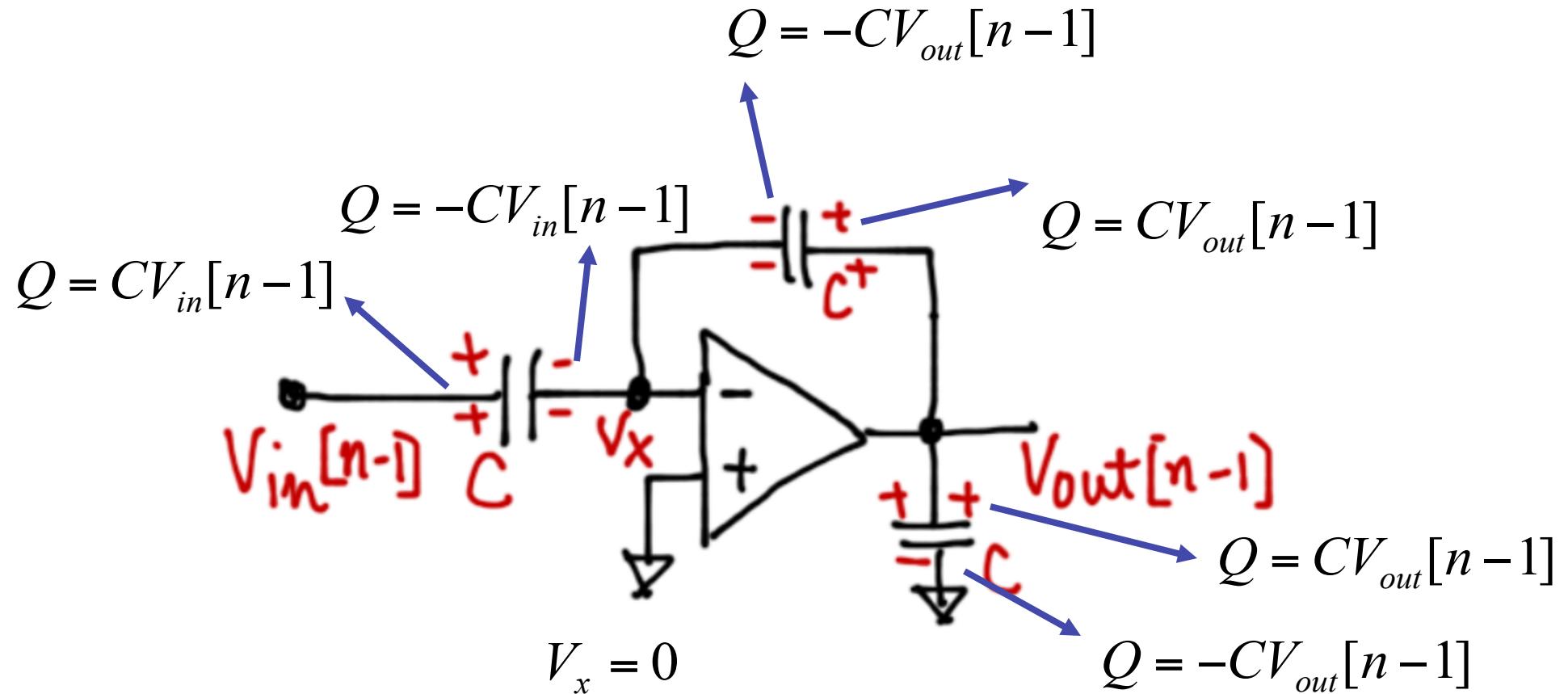
Find the relationship between  $V_{\text{out}}$  and  $V_{\text{in}}$ .



# Analysis



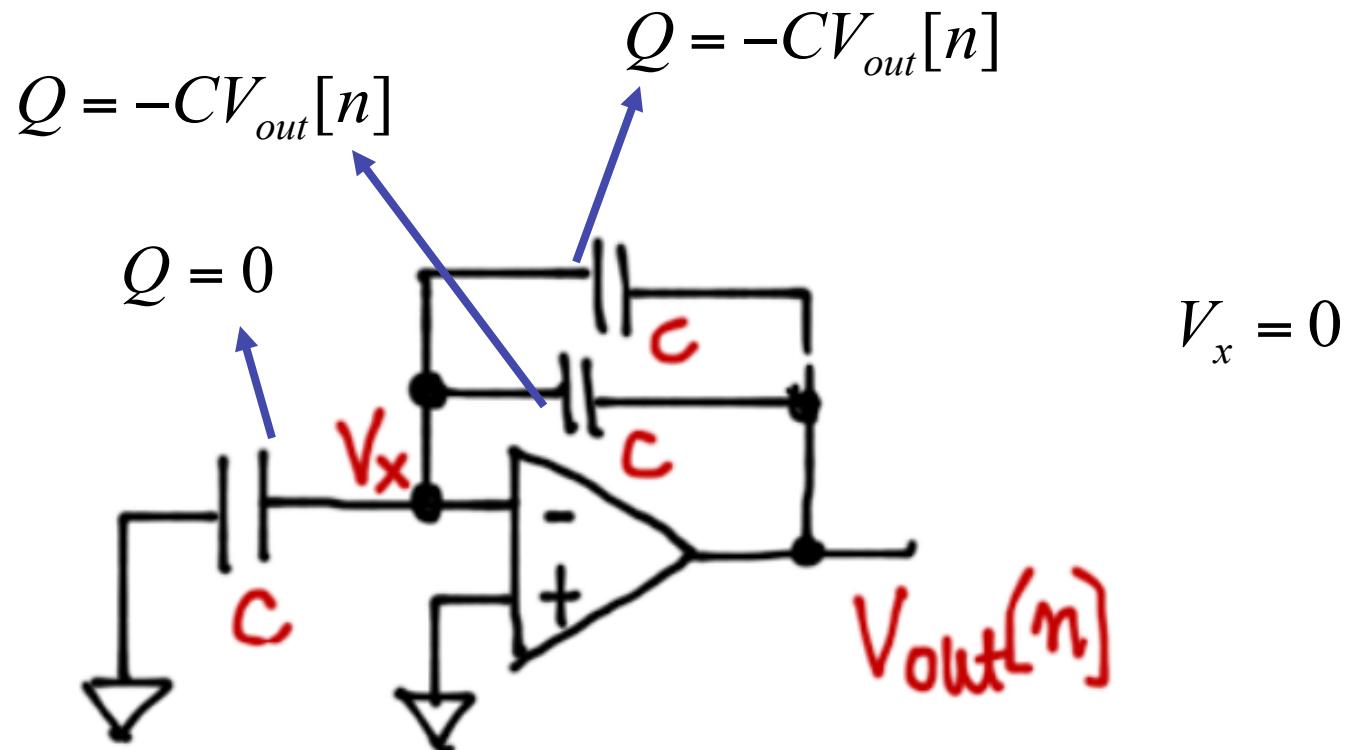
Phase 1:  $\Phi_1 = 1, \Phi_2 = 0$



# Analysis



Phase 2:  $\Phi_1 = 0, \Phi_2 = 1$



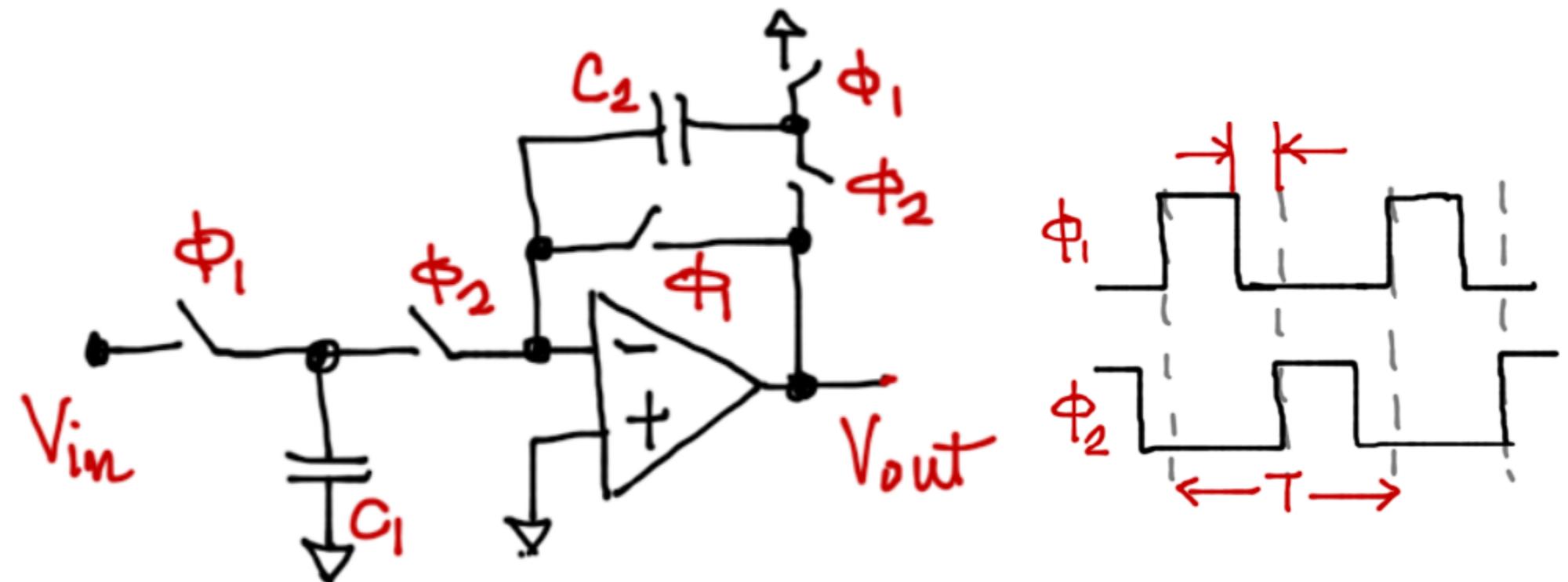
$$-CV_{out}[n] - CV_{out}[n] = -CV_{in}[n-1] - CV_{out}[n-1]$$

$$V_{out}[n] = \frac{1}{2} (V_{in}[n-1] + V_{out}[n-1])$$

$$V_{out}(s) = \frac{V_{in}(s)}{(1 + sT)}$$



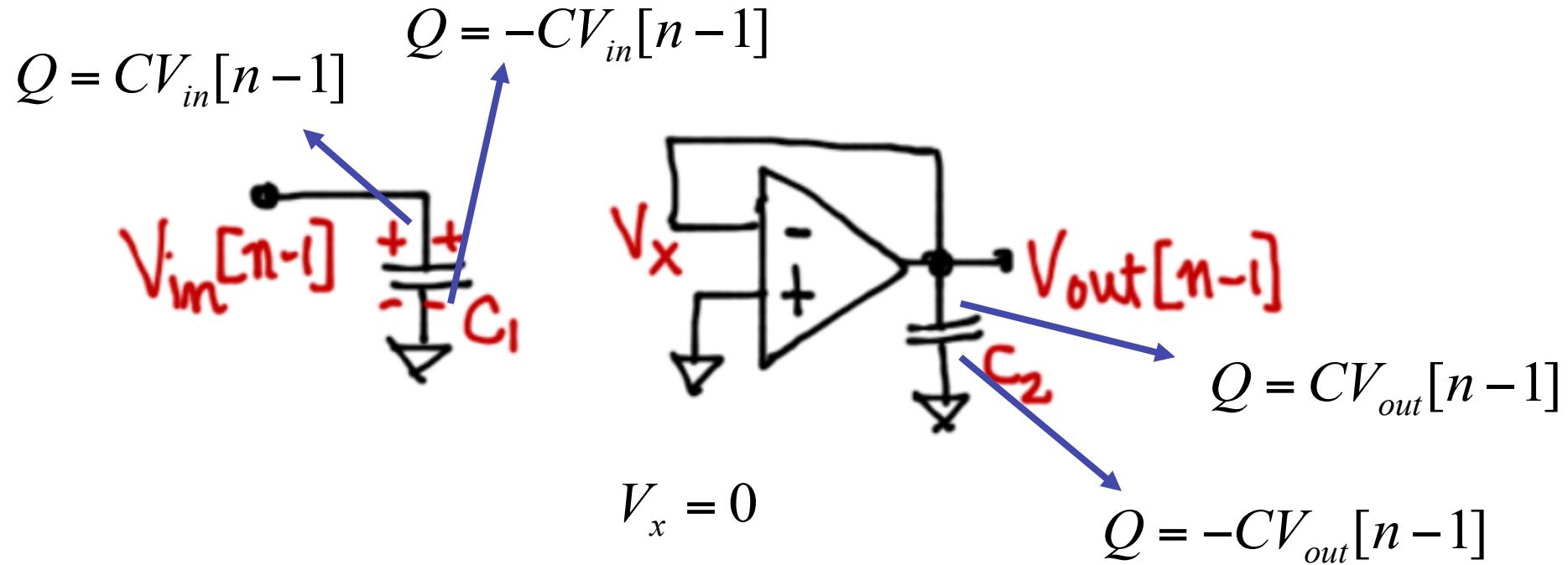
# Circuit 3: Gain Circuit



# Analysis



Phase 1:  $\Phi_1 = 1, \Phi_2 = 0$

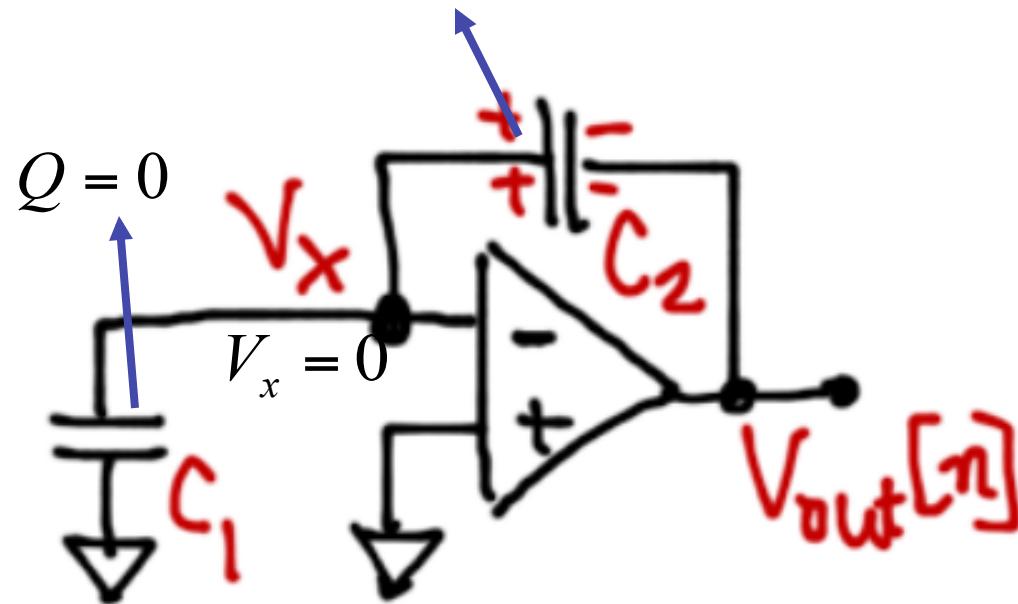


# Analysis



Phase 2:  $\Phi_1 = 0, \Phi_2 = 1$

$$Q = -CV_{out}[n]$$



$$-C_2 V_{out}[n] = C_1 V_{in}[n-1]$$

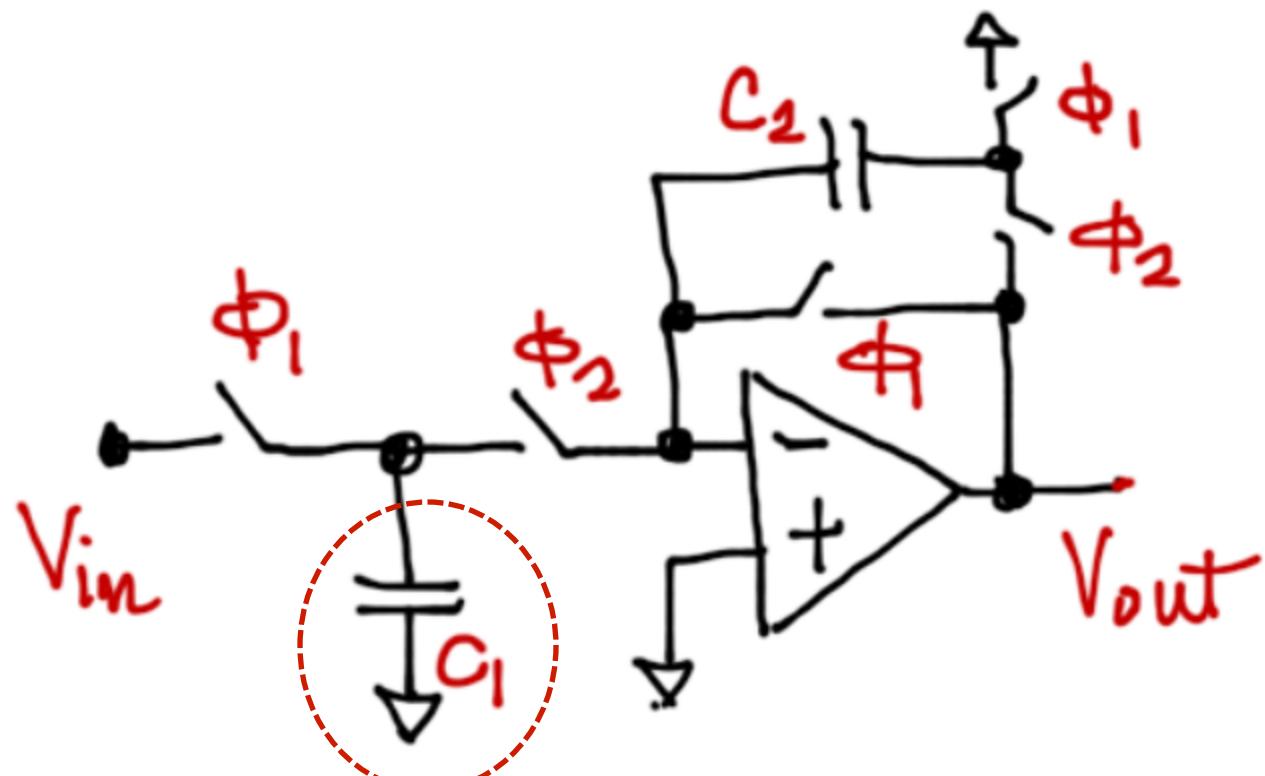
$$V_{out}[n] = -\frac{C_1}{C_2} V_{in}[n-1]$$



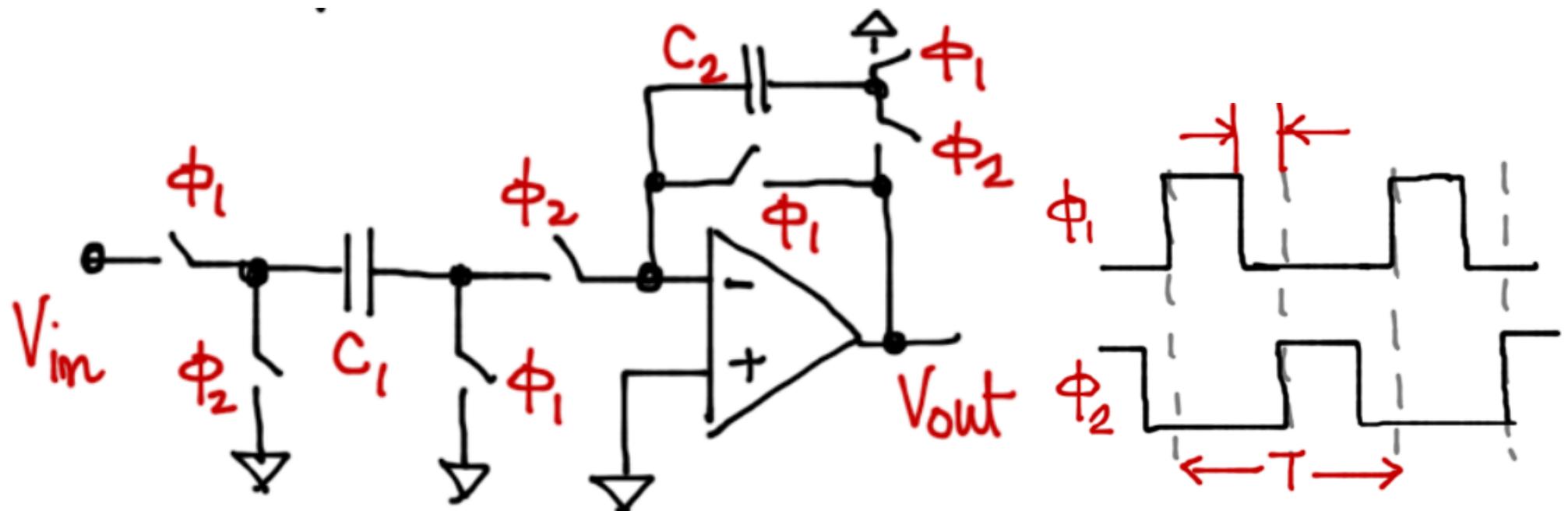
# Effect of non-ideal switches



Charge injection in  $C_1$  makes the amplifier gain non-linear.



# Improved Gain Circuit

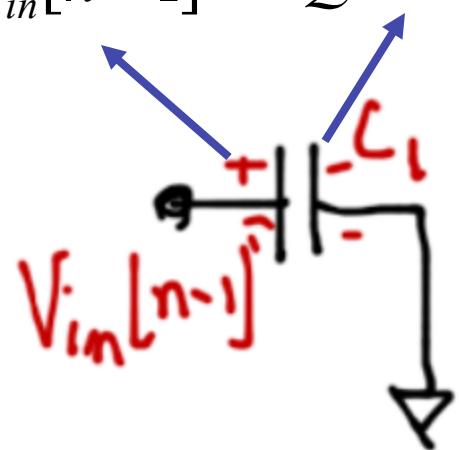


# Analysis

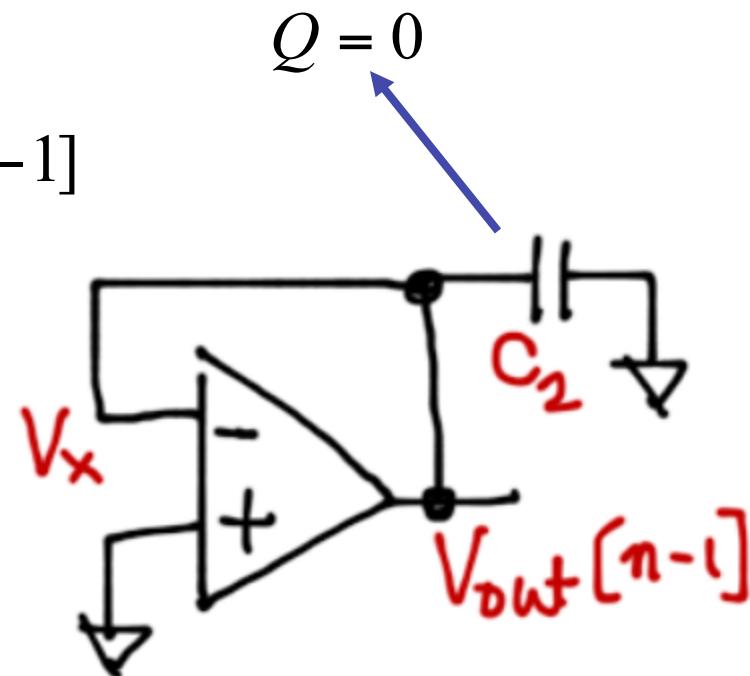


Phase 1:  $\Phi_1 = 1, \Phi_2 = 0$

$$Q = CV_{in}[n-1]$$



$$Q = -CV_{in}[n-1]$$



$$V_x = 0$$

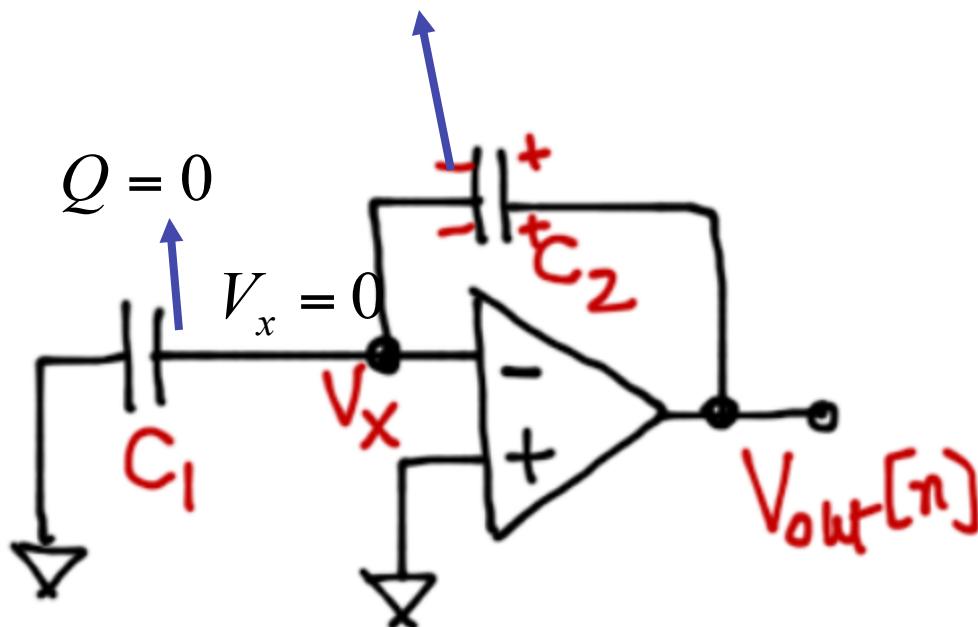


# Analysis



Phase 2:  $\Phi_1 = 0, \Phi_2 = 1$

$$Q = -CV_{out}[n]$$

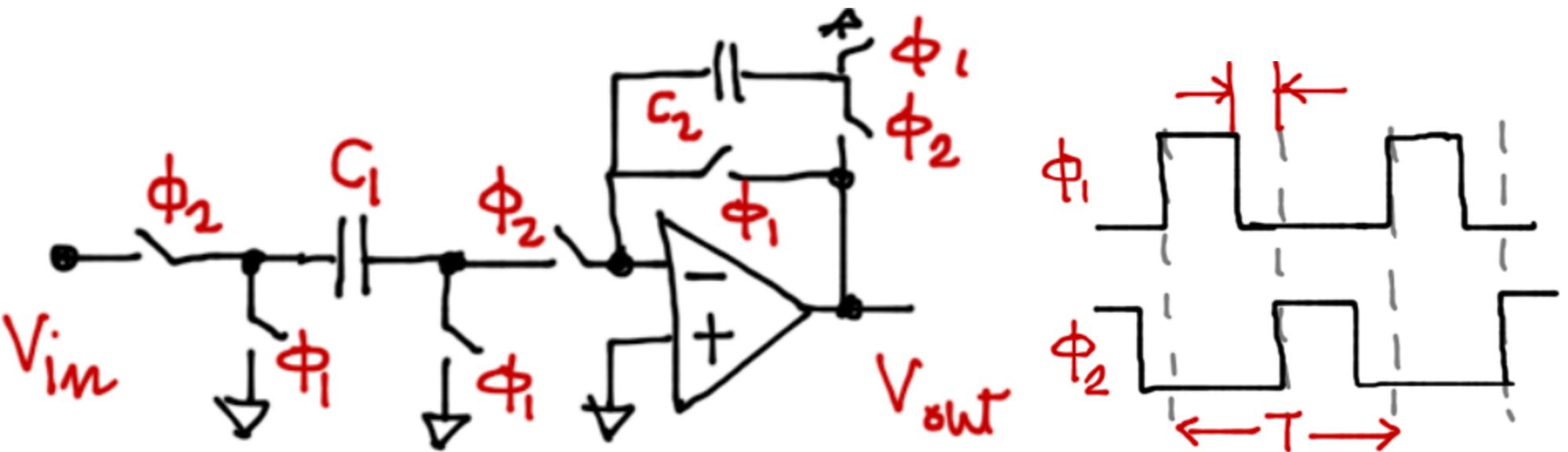


$$-C_2 V_{out}[n] = -C_1 V_{in}[n-1]$$

$$V_{out}[n] = \frac{C_1}{C_2} V_{in}[n-1]$$



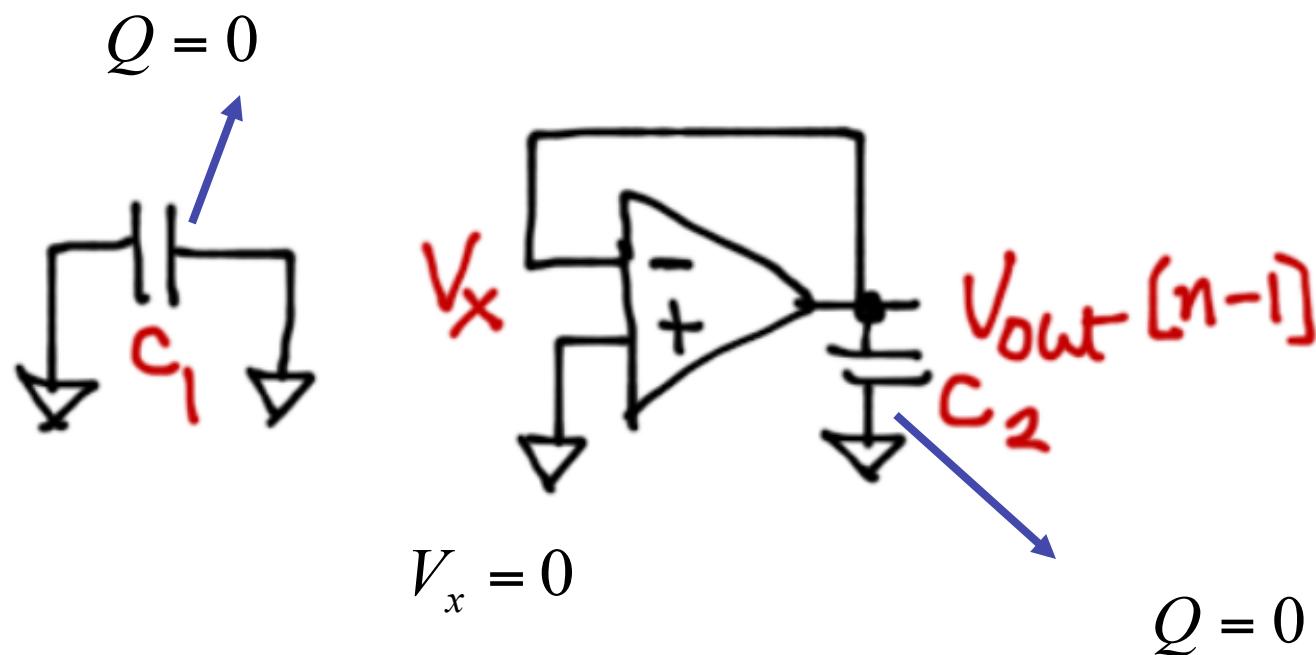
# Inverting amplifier



# Analysis



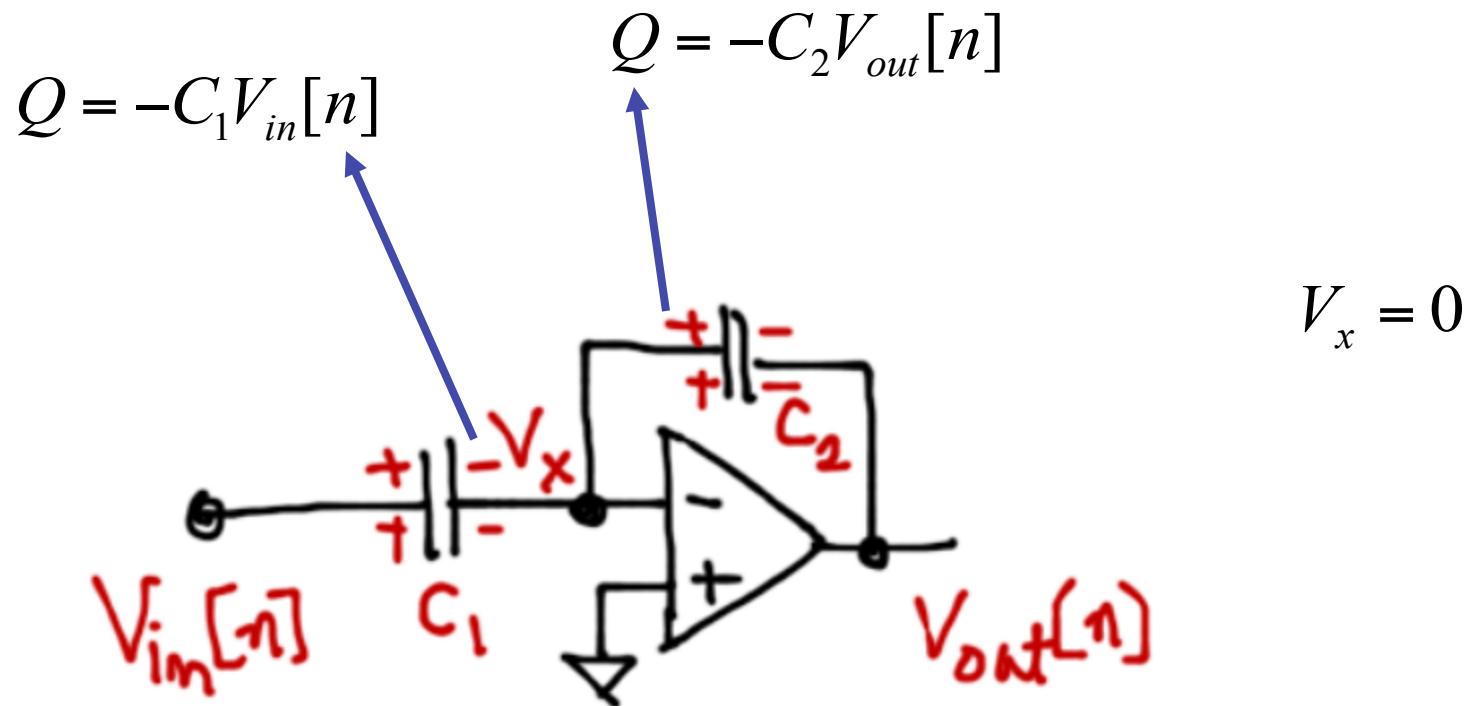
Phase 1:  $\Phi_1 = 1, \Phi_2 = 0$



# Analysis



Phase 2:  $\Phi_1 = 0, \Phi_2 = 1$

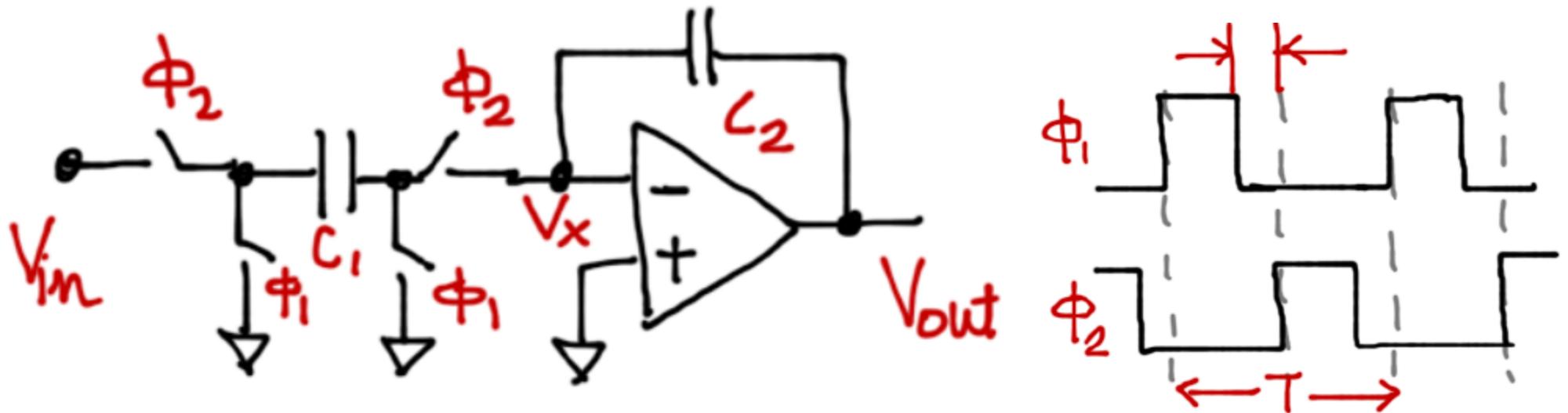


$$-C_1 V_{out}[n] - C_2 V_{in}[n] = 0$$

$$V_{out}[n] = -\frac{C_1}{C_2} V_{in}[n - 1]$$



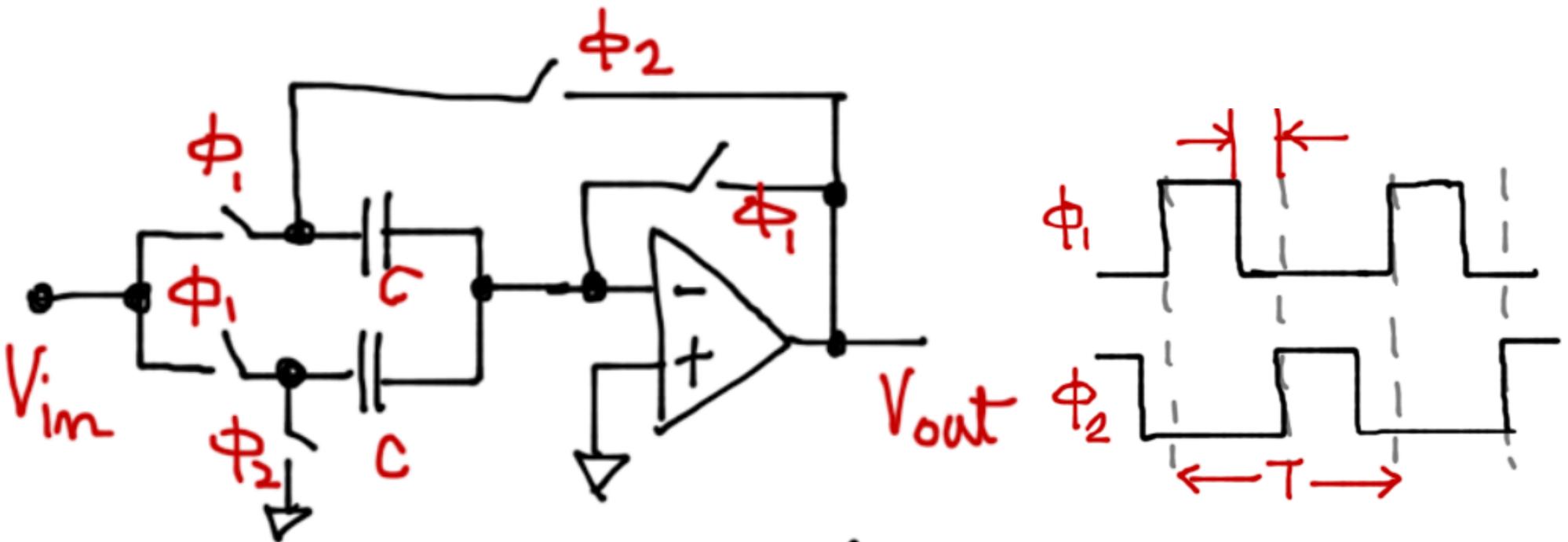
# Switched Capacitor Integrator



# Worksheet



# Multiply x 2 circuit



# Worksheet



# Worksheet

