Data Converters

CSE562M: Analog Integrated Circuits

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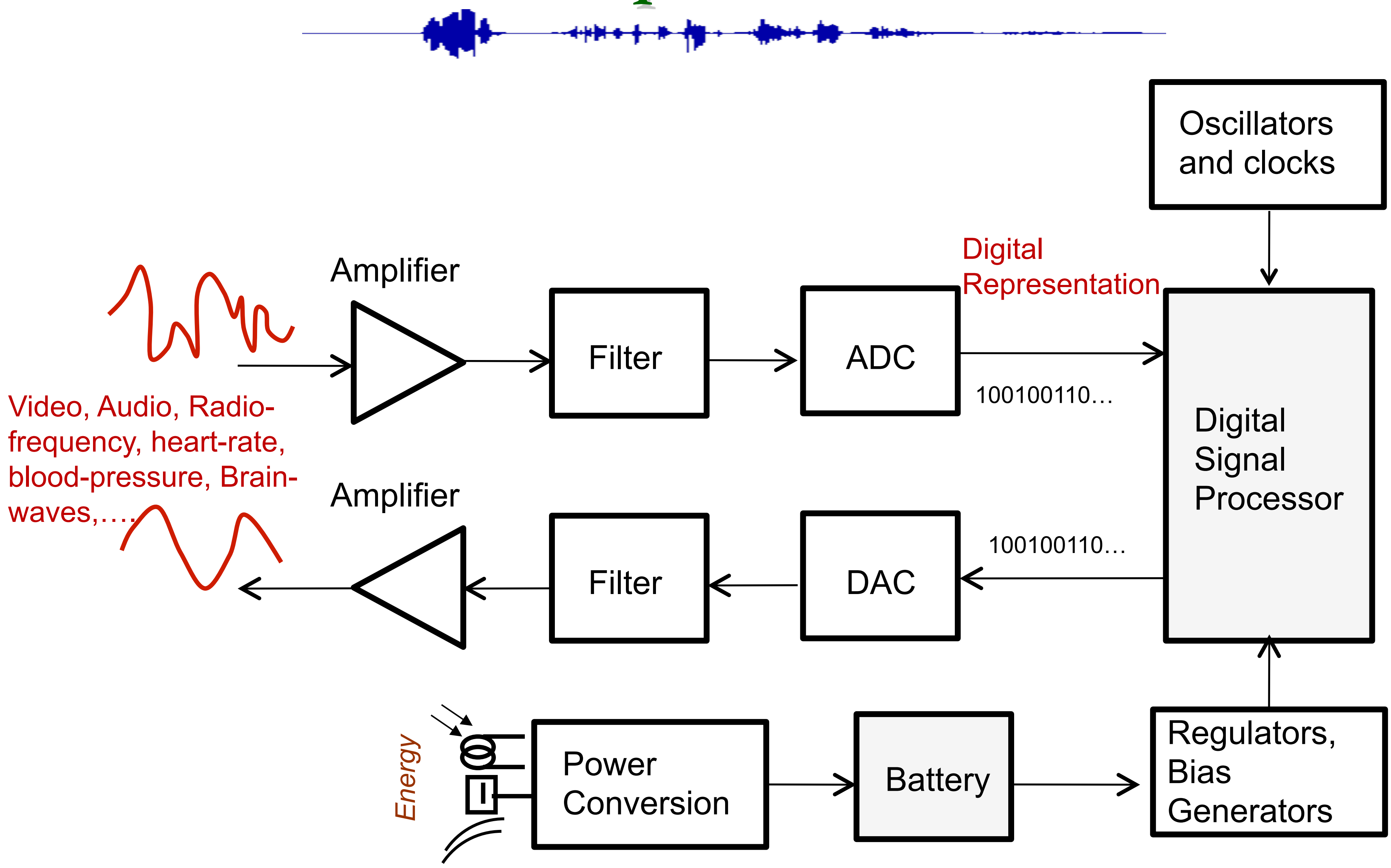
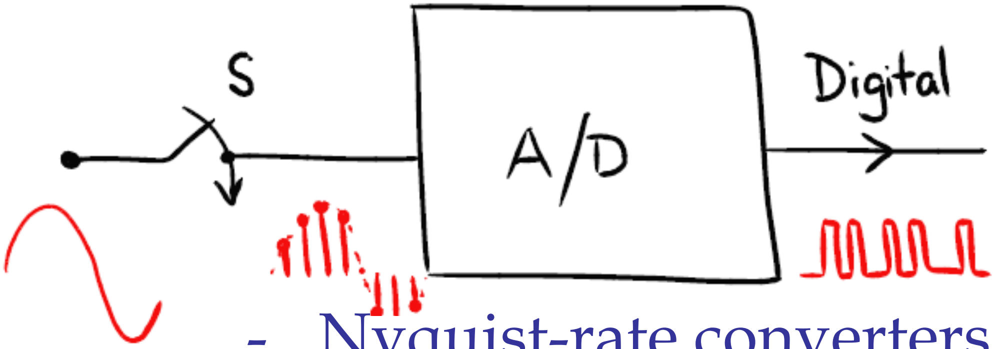
One of the most important blocks

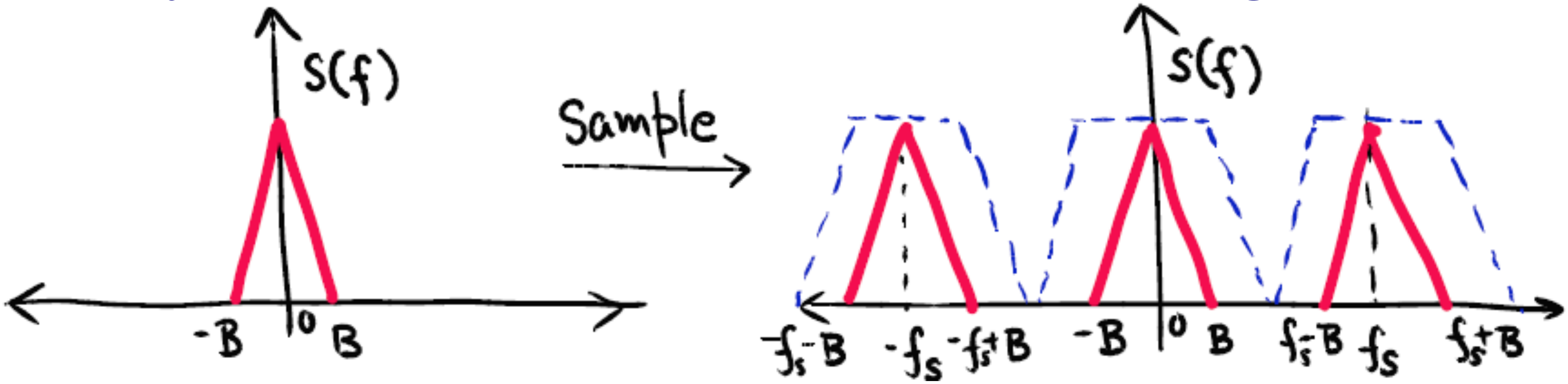


Classification of Data Converters

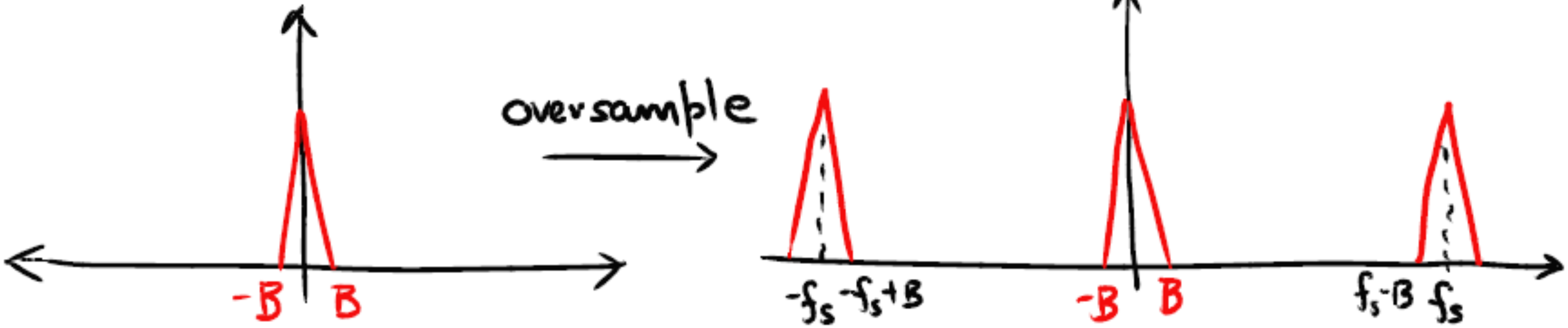


- Classification based on rate of sampling of the analog signal.

- Nyquist-rate converters f_s = 2-10 times signal bandwidth (B)

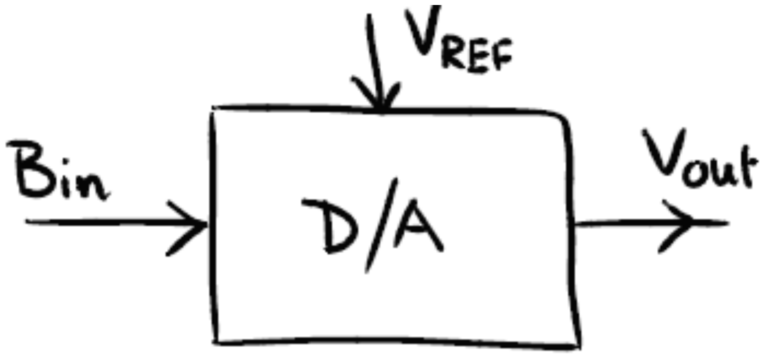


- Oversampling converters $f_s >> 2B$



Digital to analog conversion

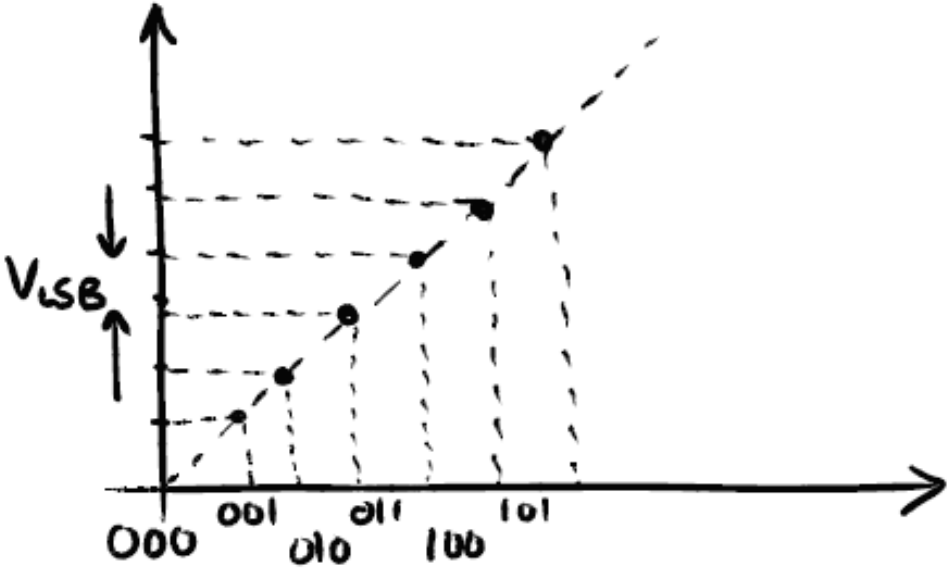
- Different binary representations (minimal code, thermometer code, gray code, signed, twos complement, …).



$$V_{out} = f(b_1, b_2, ..., b_N) V_{ref}$$

$$B_{out} = 2^{-1} b_1 + 2^{-2} b_2 + \ldots + 2^{-N} b_N$$

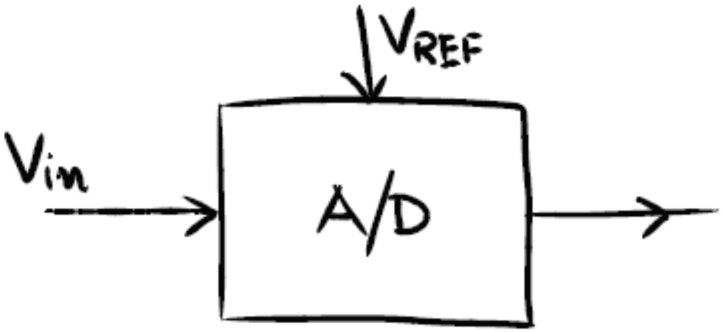
MSB LSB



- For each binary input, an ideal DAC produces a unique analog signal output.
- Resolution of the DAC.

$$V_{LSB} = 2^{-N} V_{ref}$$

Analog to Digital Conversion



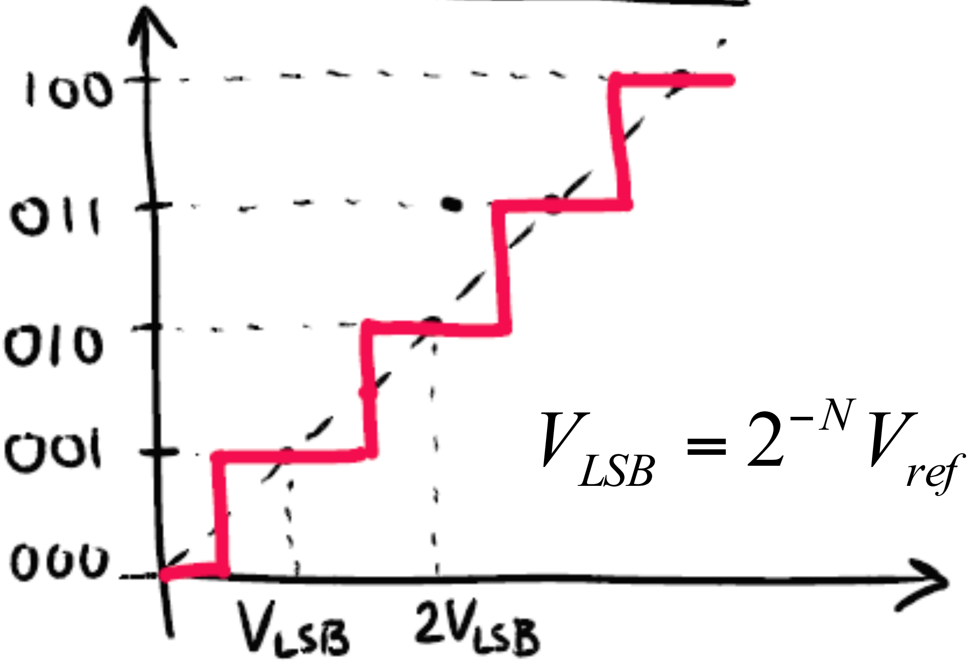
$$B_{out} = 2^{-1}b_1 + 2^{-2}b_2 + \ldots + 2^{-N}b_N$$

MSB LSB

$$V_{in} \approx f(b_1, b_2, .., b_N)V_{ref}$$

- For a set of analog input an ideal ADC produces a unique binary output.
- 3 bit ADC.

$$-\frac{1}{8}V_{ref} < V_{in} < \frac{7}{8}V_{ref}$$



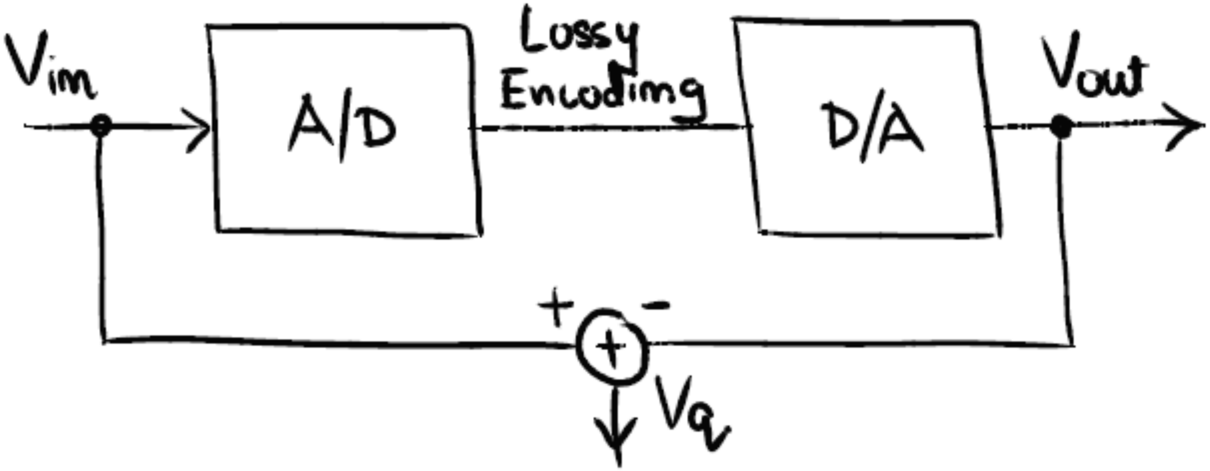
$$V_{LSB} = 2^{-N}V_{ref}$$

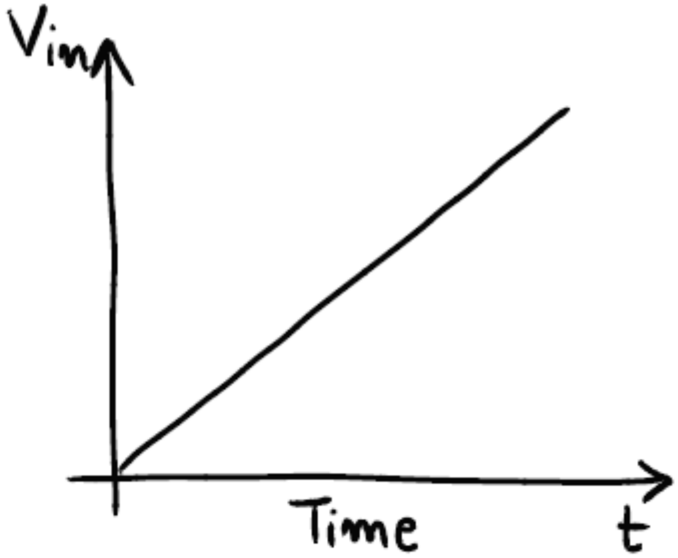
- Approximation or resolution of an ideal ADC

$$-\frac{1}{2}V_{LSB} < V_{in} - f(b_1, b_2, .., b_N)V_{ref} < \frac{1}{2}V_{LSB}$$

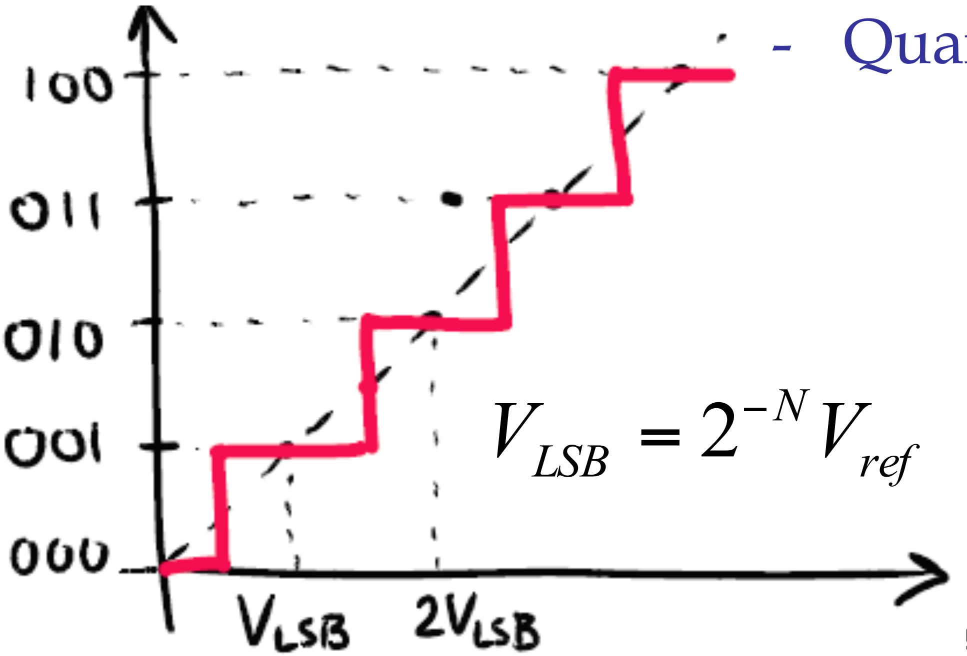
Quantization Noise

$$V_q = V_{in} - f(b_1, b_2, .., b_N)V_{ref}$$



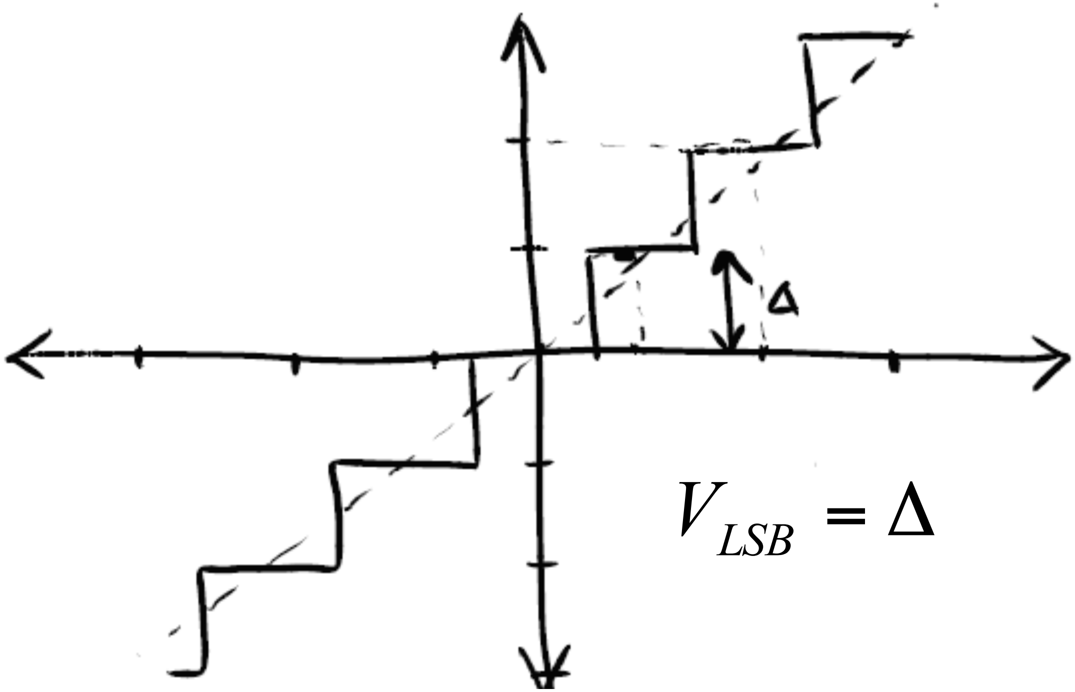


- Quantization error is bounded



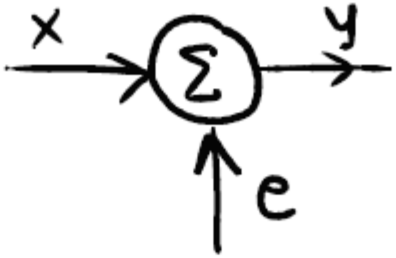
$$V_{LSB} = 2^{-N}V_{ref}$$

Quantization Noise Statistics

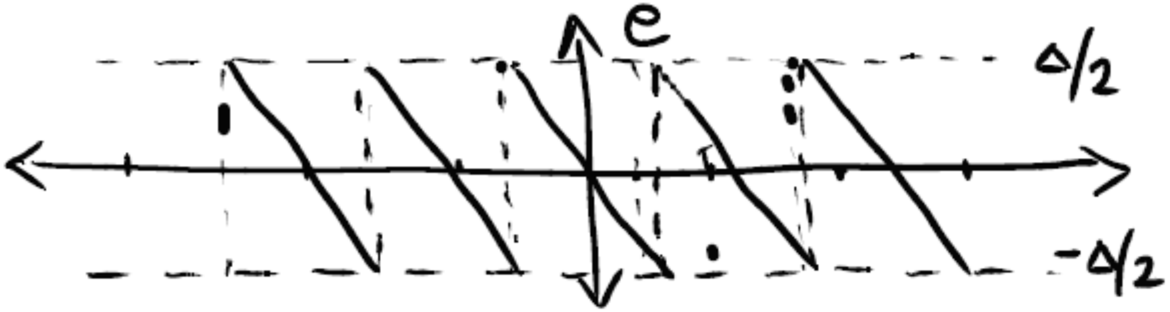


$V_{LSB} = \Delta$

$$e = y - f(b_1, b_2, \ldots, b_N)V_{ref}$$

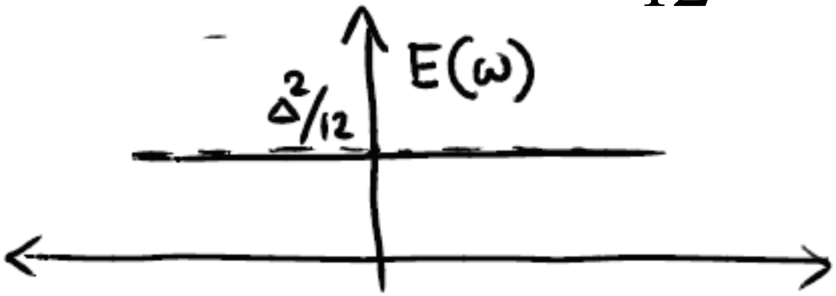


- Random input signal, then quantization noise follows a uniform distribution and a white noise statistics.



$\bar{e} = 0$

$$\bar{e}^2 = \frac{\Delta^2}{12}$$



Data Converter Metrics

- Signal to quantization noise ratio $V_{LSB} = 2^{-N} V_{ref}$

$$SNR = 20\log_{10}\left(\frac{V_{ref}}{\sqrt{12}} \bigg/ \frac{V_{LSB}}{\sqrt{12}} \right) = 6.02N$$

- Increasing the resolution by 1 bit increases the SNR by 6dB
- Estimating resolution from measurements

- For random input

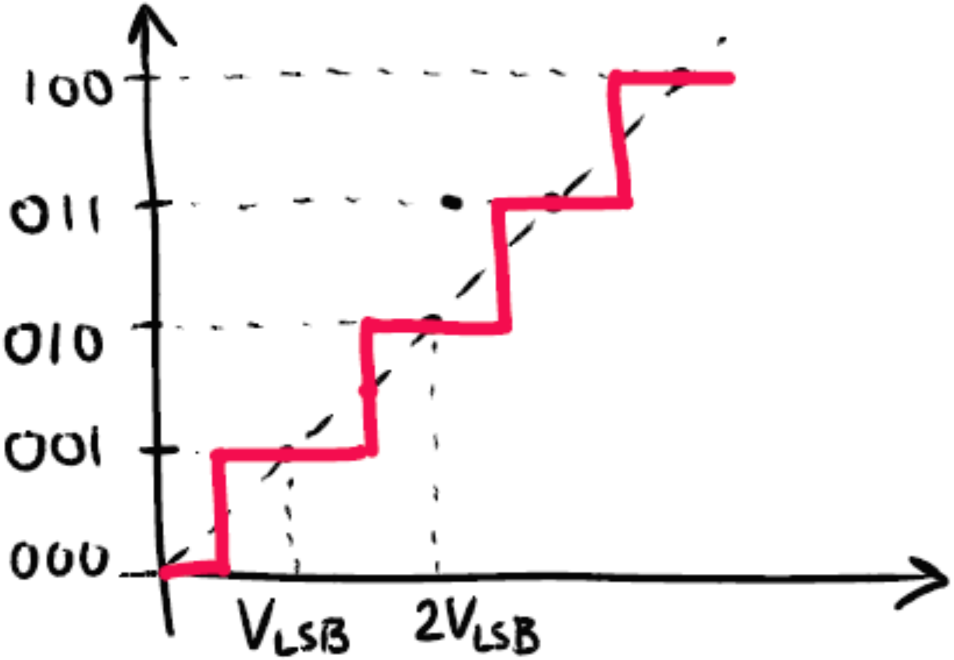
$$ENOB = \frac{SNR_{measured}}{6.02}$$

- For sinusoidal input

$$ENOB = \frac{SNR_{measured} - 1.76}{6.02}$$

- Dynamic Range: $DR = \dfrac{Signal(RMS)}{Noise(RMS) + Distortion(RMS)}$

Data Converter Metrics



- Offset error

$$e_{off(ADC)} = \frac{V_{00..1}}{V_{LSB}} - \frac{1}{2}$$

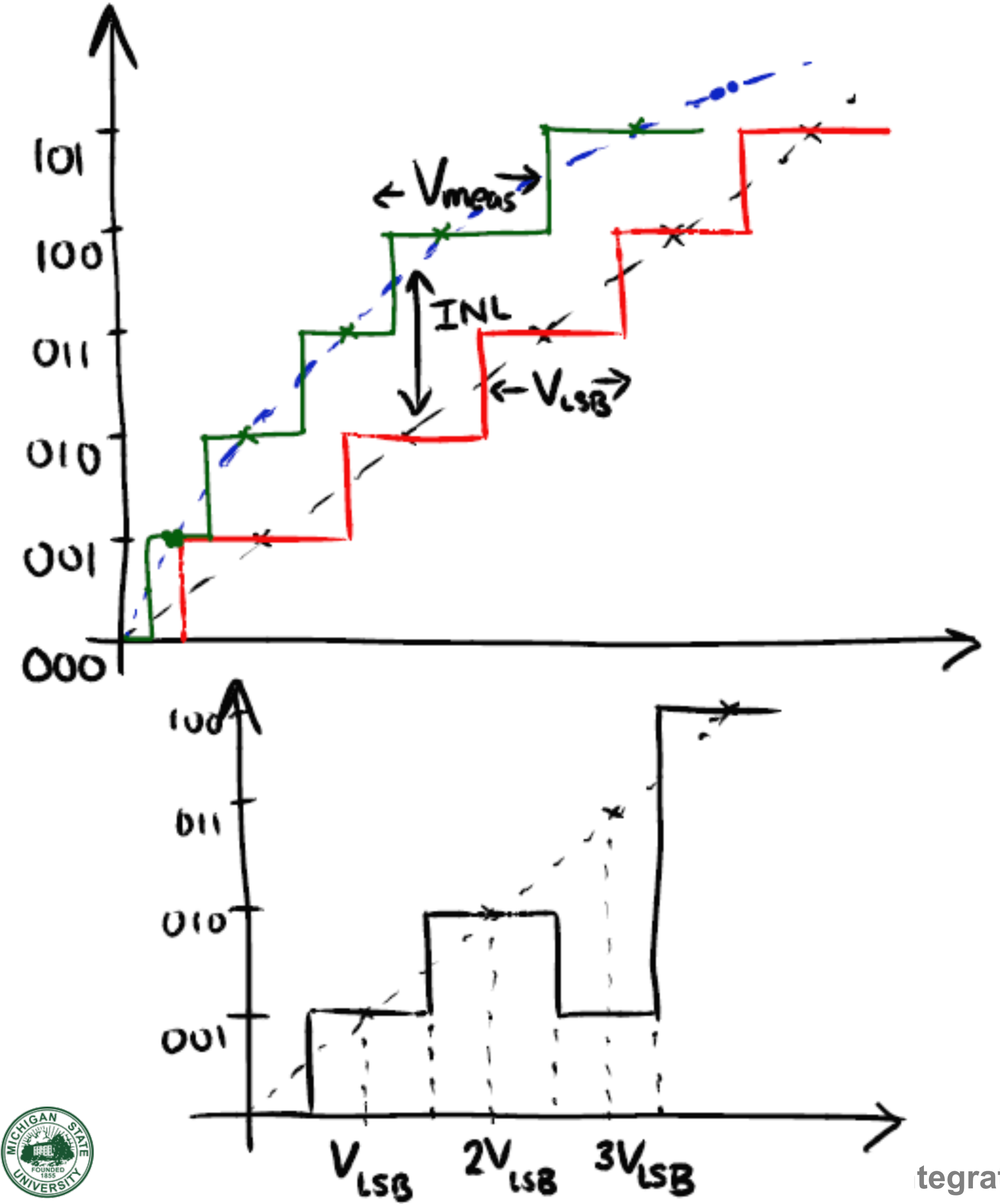
$$e_{off(DAC)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{V_{in}=0}$$

- Gain error

$$e_{gain(DAC)} = \left[\left.\frac{V_{out}}{V_{LSB}}\right|_{V_{in}=11..1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{V_{in}=00..0}\right] - (2^N - 1)$$

$$e_{off(ADC)} = \left[\frac{V_{11..1}}{V_{LSB}} - \frac{V_{00..0}}{V_{LSB}}\right] - \left(2^N - 2\right)$$

Data Converter Metrics



- Integral Non-Linearity (INL)

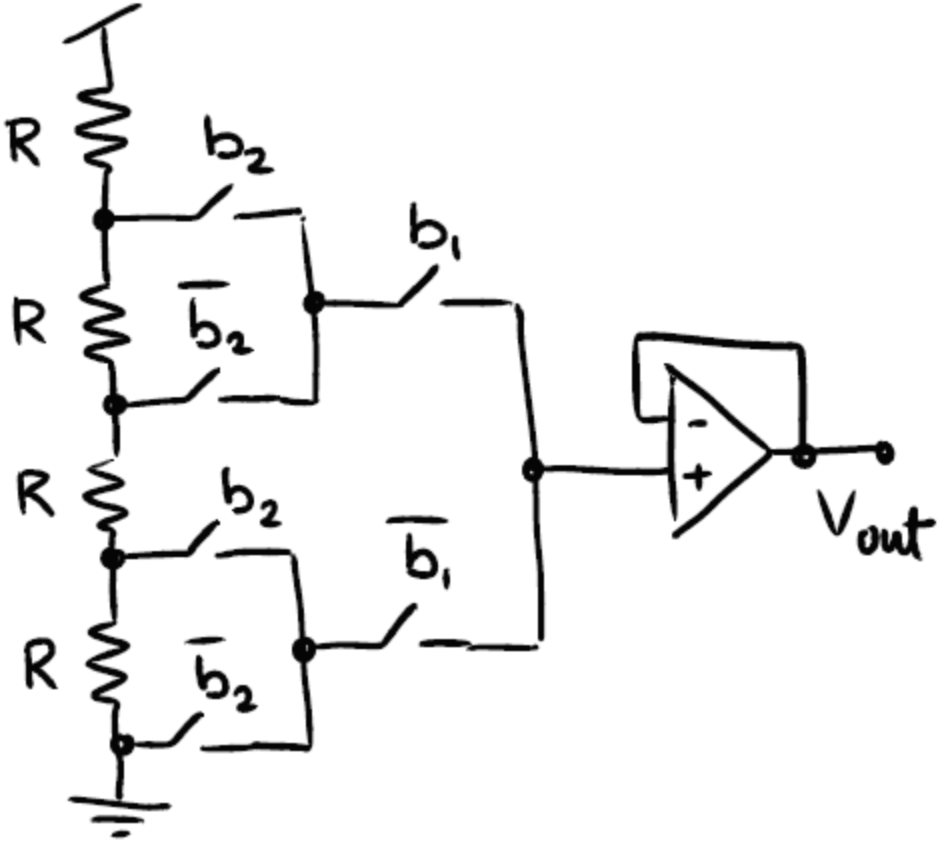
$$INL = \max_{\{00..0-11..1\}} \frac{|V_{meas} - V_{ideal}|}{V_{LSB}}$$

- Differential Non-linearity

$$DNL = \max_{\{00..0-11..1\}} \frac{|\Delta V_{meas} - V_{LSB}|}{V_{LSB}}$$

- Monotonicity
- Missing output codes
- Speed of ADC – acquisition time + measurement time
- Speed of DAC – time for the output to settle down to $0.5V_{LSB}$

Nyquist-rate DACs



- Tree based decoding

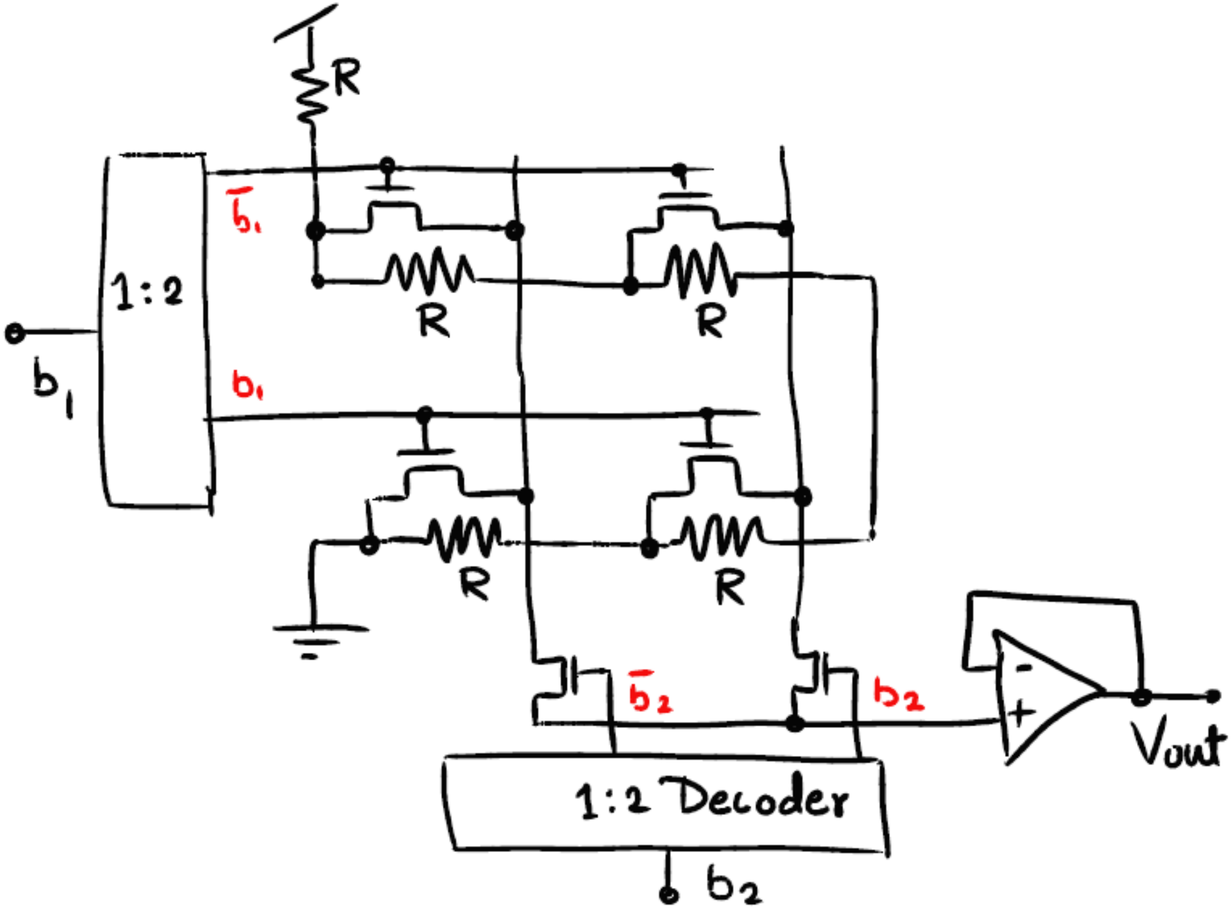
$$B_{out} = 2^{-1} b_1 + 2^{-2} b_2$$

- <u>Advantages</u>
- Guaranteed monotonicty
- Resistive matching (up to 10 bits)

- <u>Disadvantages:</u>
- Speed ?
- Size ?

Nyquist-rate DACs

- Folded resistor network



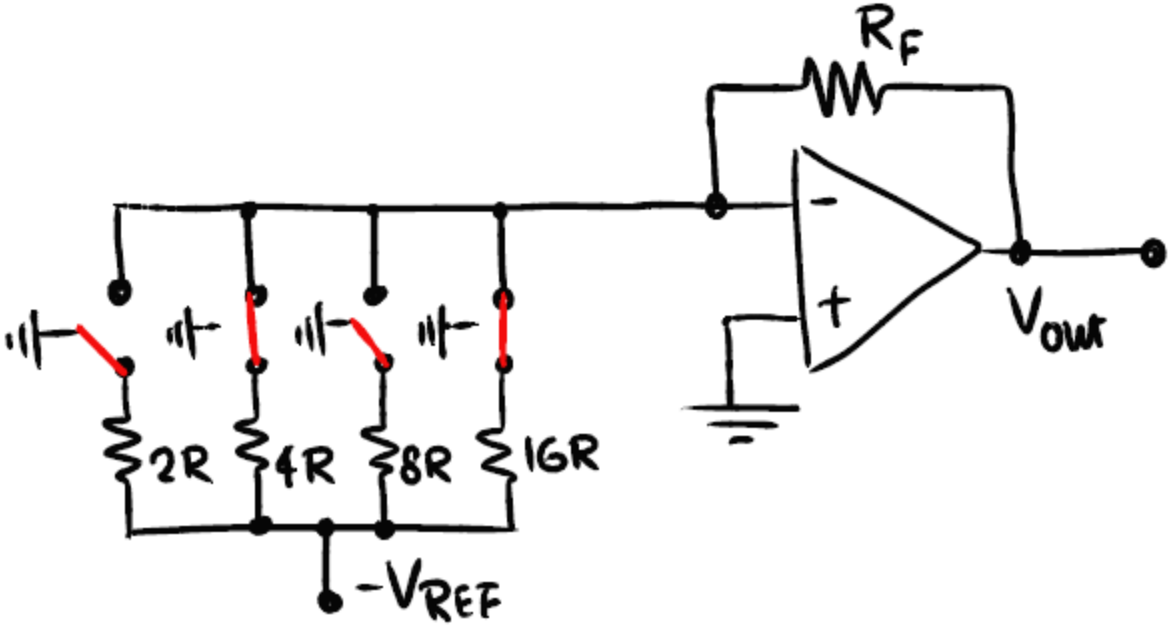
$$B_{out} = 2^{-1} b_1 + 2^{-2} b_2$$

- Advantages
- Lower capacitance at the input of the opamp.
- Disadvantages:
- Size ?

Nyquist-rate DACs

- Ladder architecture

$$V_{out} = \frac{R_F}{R} V_{ref} \left(2^{-1} b_1 + 2^{-2} b_2 + \ldots + 2^{-N} b_N\right)$$



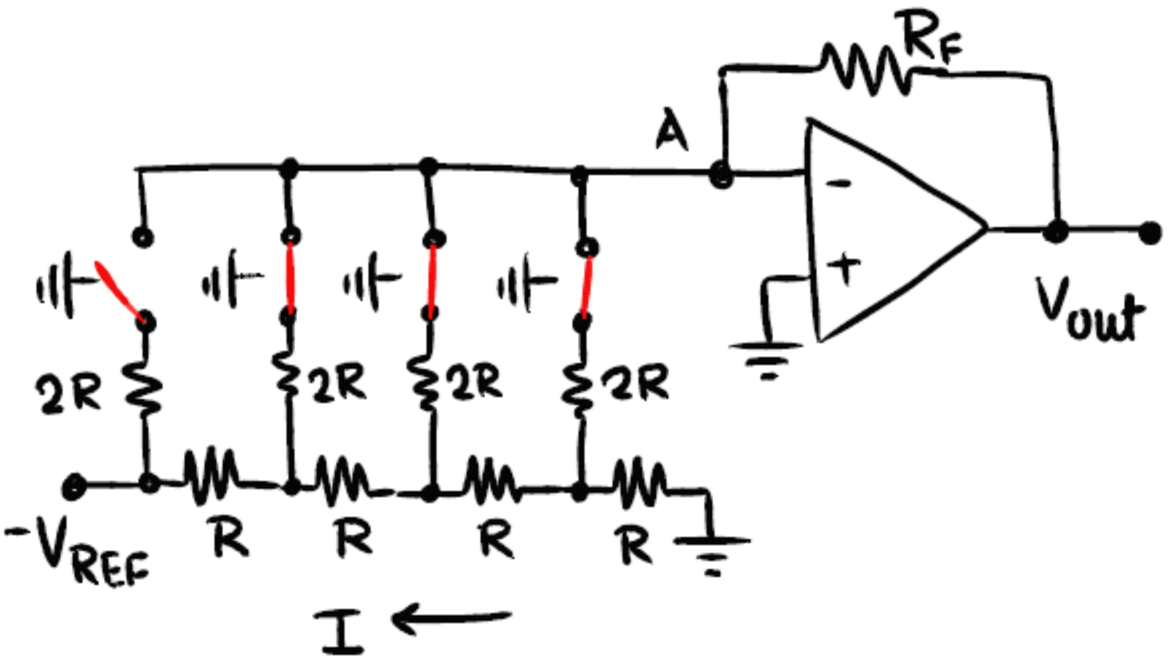
- Advantages
- Simplicity.

- Disadvantages:
- Size ?

Nyquist-rate DACs

- Ladder architecture

$$V_{out} = \frac{R_F}{R} V_{ref} \left(2^{-1} b_1 + 2^{-2} b_2 + \ldots + 2^{-N} b_N \right)$$



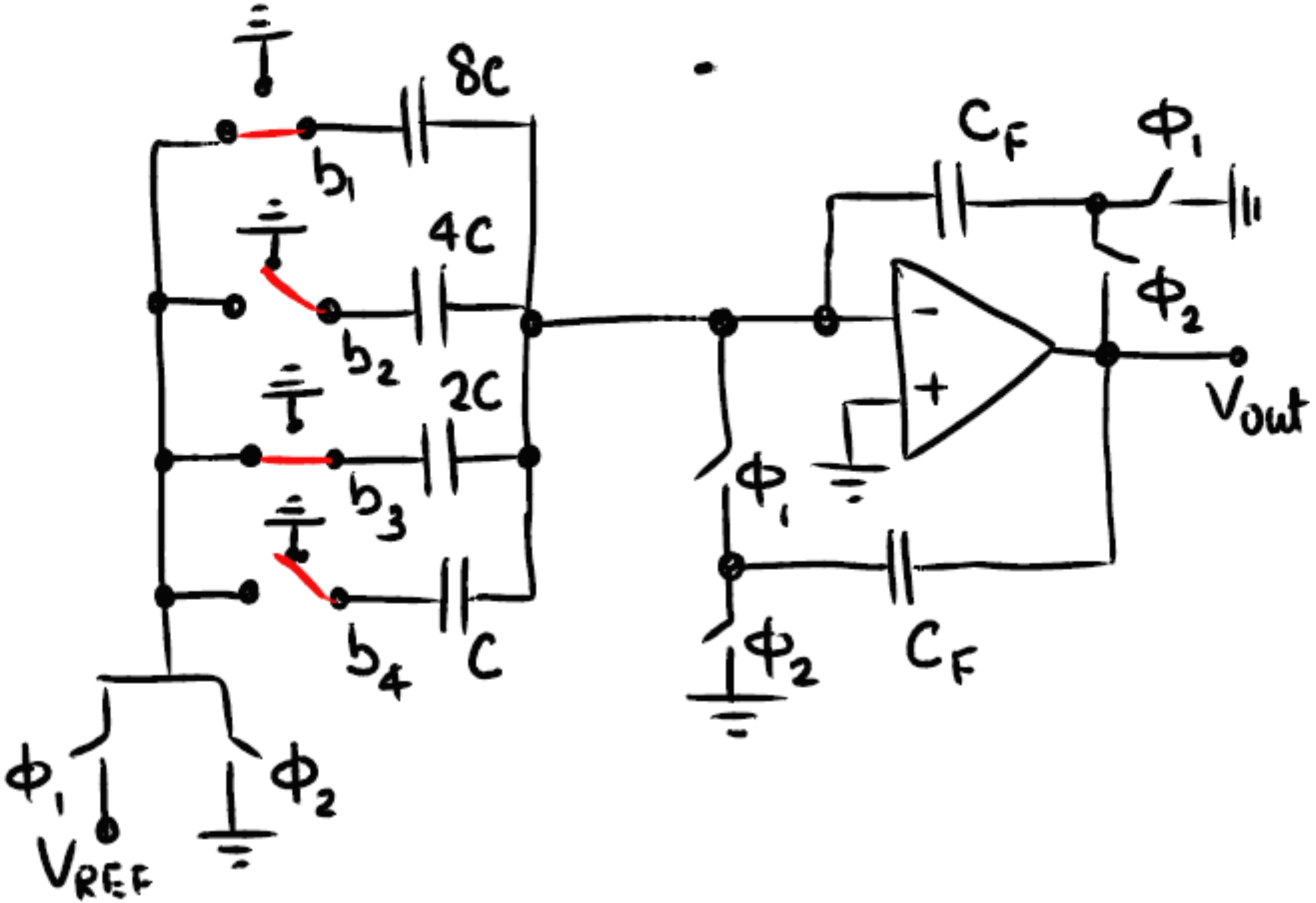
- Advantages
- Simplicity.
- Size

- Disadvantages:
- Speed ?

Nyquist-rate DACs

- Switched capacitor converters

$$V_{out} = \frac{C}{C_F} V_{ref} \left(2^{-1} b_1 + 2^{-2} b_2 + \ldots + 2^{-N} b_N \right)$$



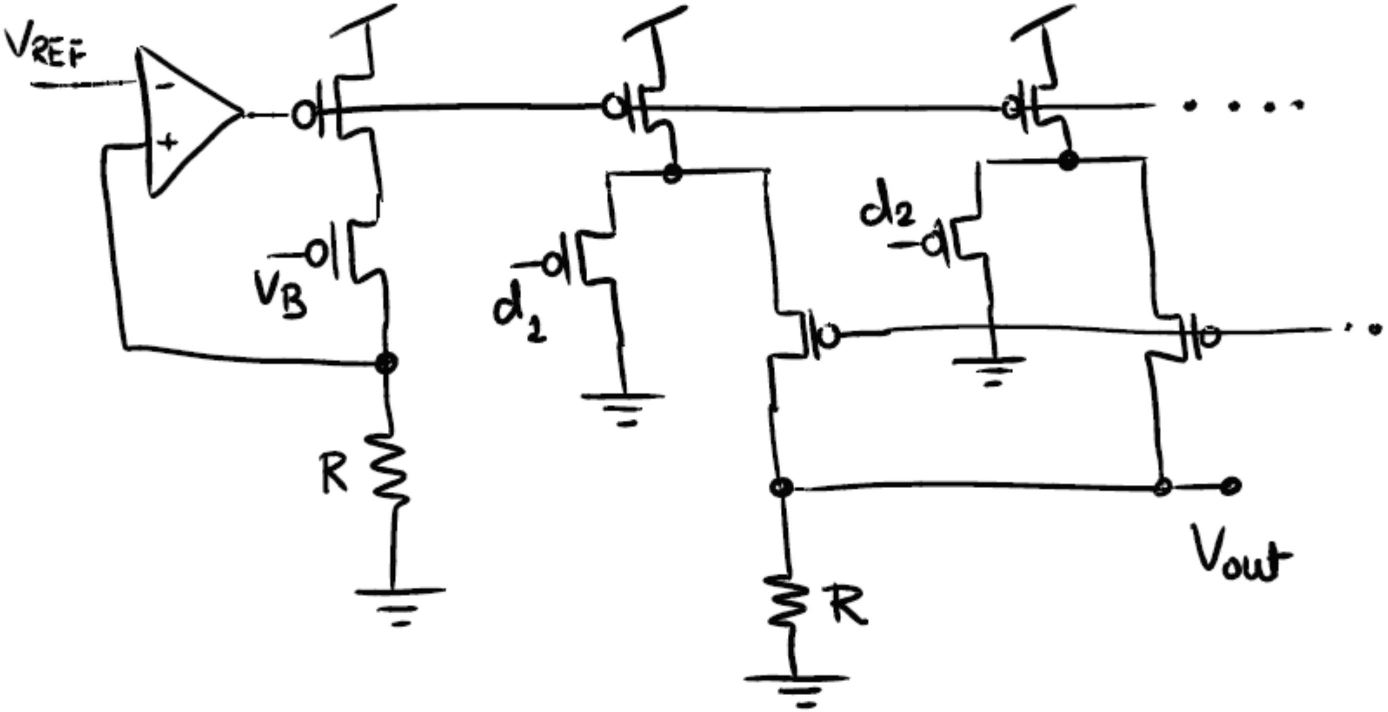
- <u>Advantages</u>
- Simplicity.
- Matching

- <u>Disadvantages:</u>
- Sampling ?

Nyquist-rate DACs

- Current mode thermometer code

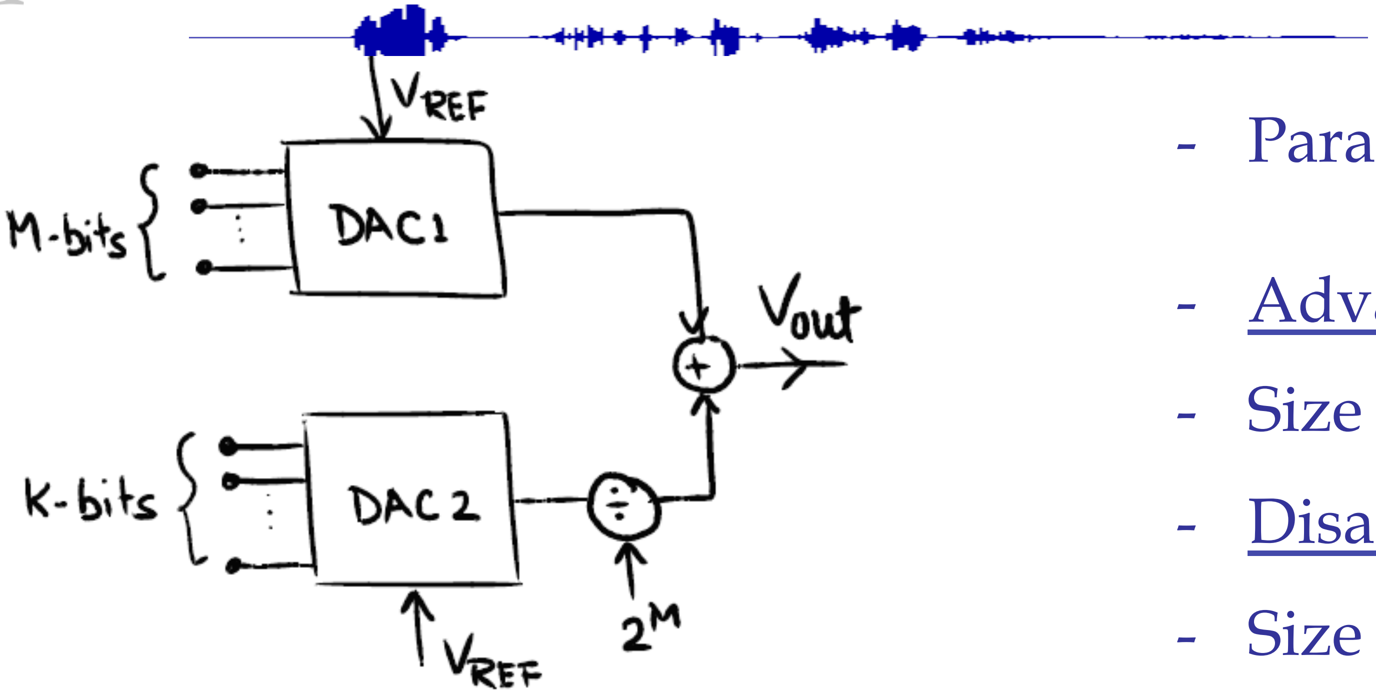
$$V_{out} = V_{ref}\left(d_1 + d_2 + \ldots + d_N\right)$$



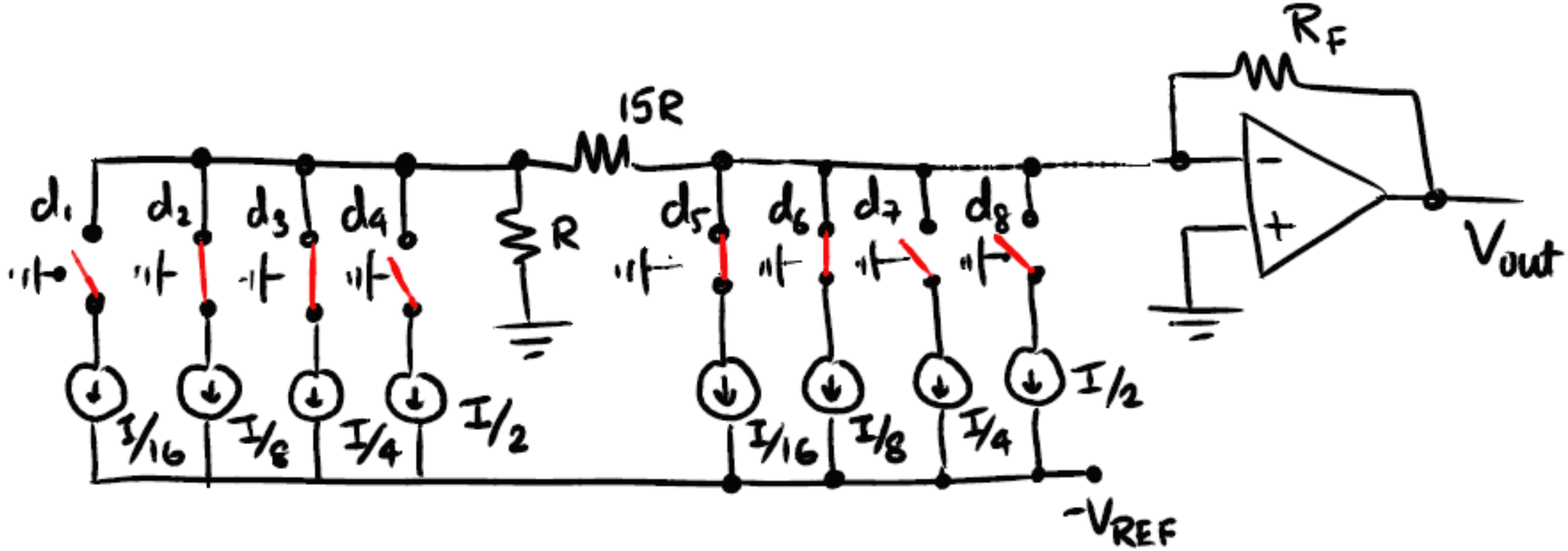
- <u>Advantages</u>
- Avoids glitching.
- Simplicity
- Matching

- <u>Disadvantages:</u>
- Size ?

Nyquist-rate DACs

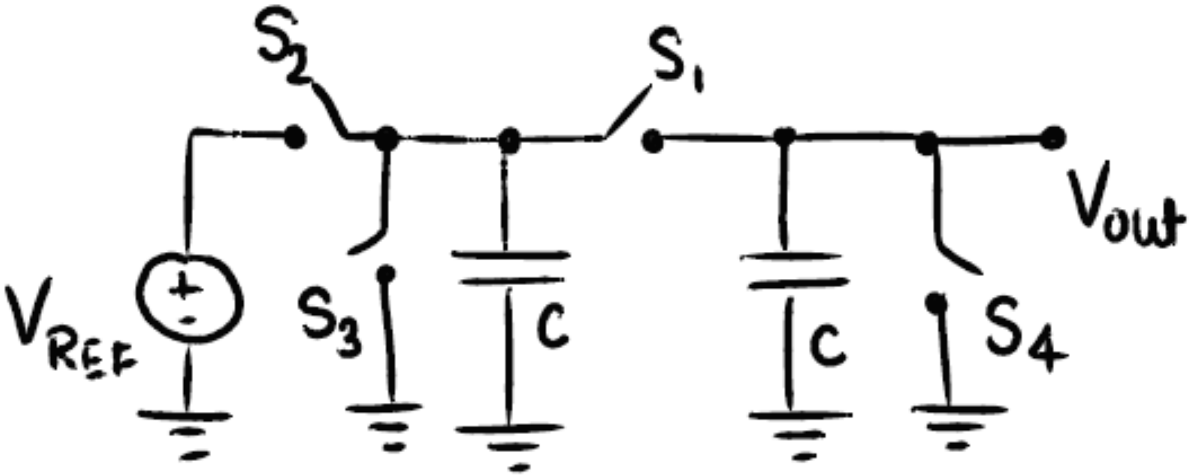


- Parallel DAC
- Advantages
- Size
- Disadvantages:
- Size ?



Nyquist-rate Serial DACs

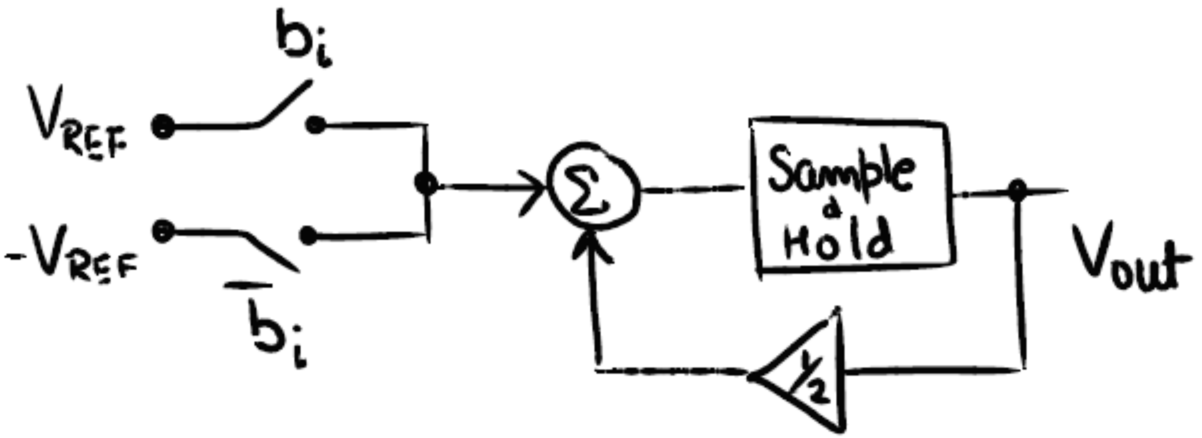
- Charge distribution DACs



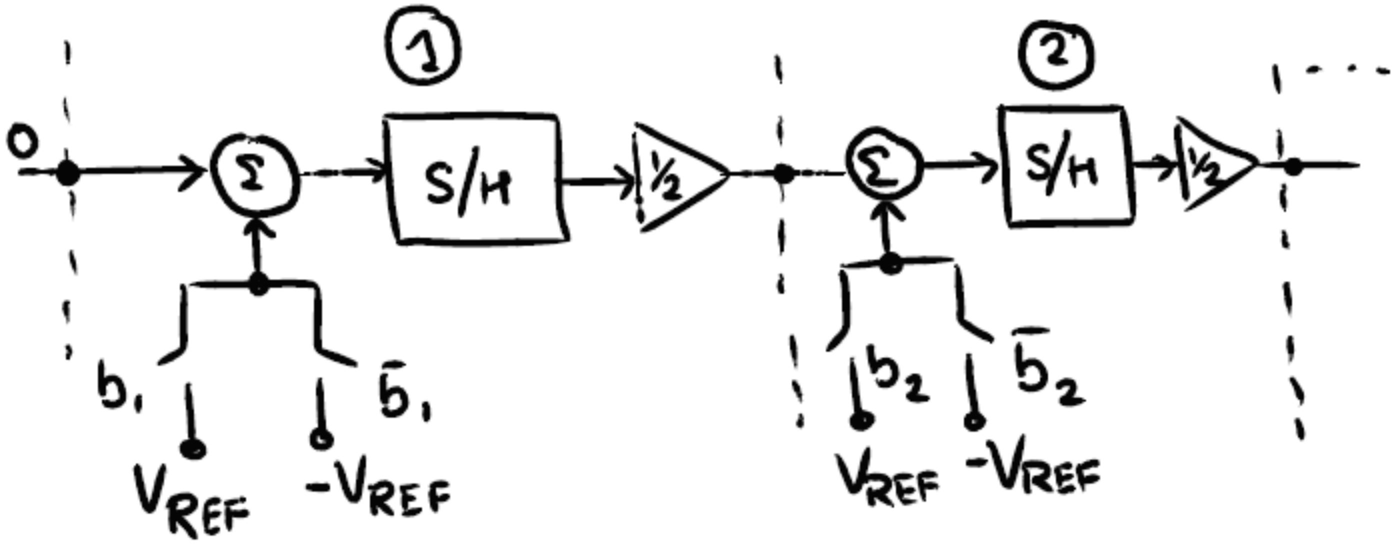
- S_4 turns ON only once before the conversion begins.
- S_2 turns ON if bit is 1 otherwise S_3 turns ON
- S_1 turns ON
- Repeat

Nyquist-rate Algorithmic DACs

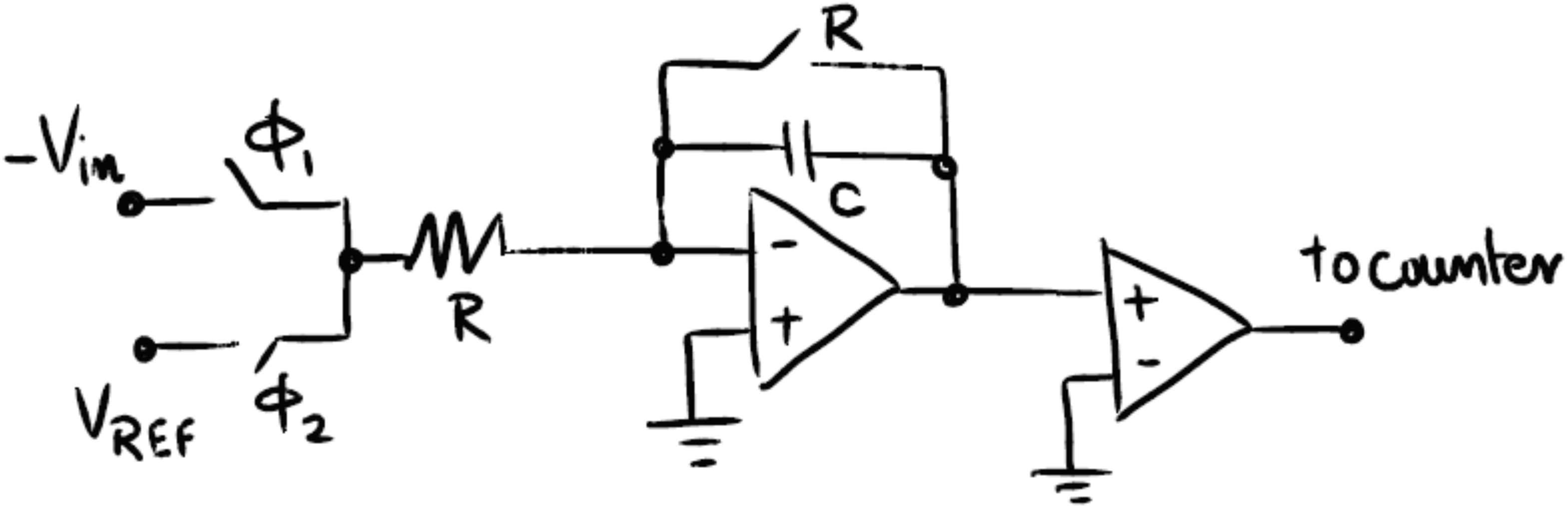
- Bit serial configuration

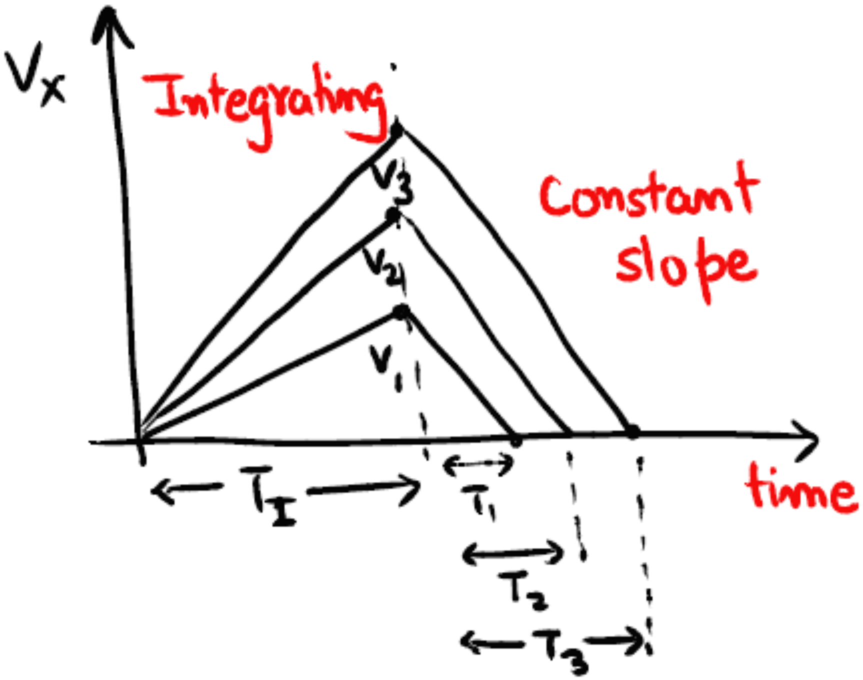


- Pipelined configuration



Nyquist-rate Integrating ADC





- Dual-slope ADC

$$T_1 = T_I \frac{V_{in}}{V_{ref}}$$

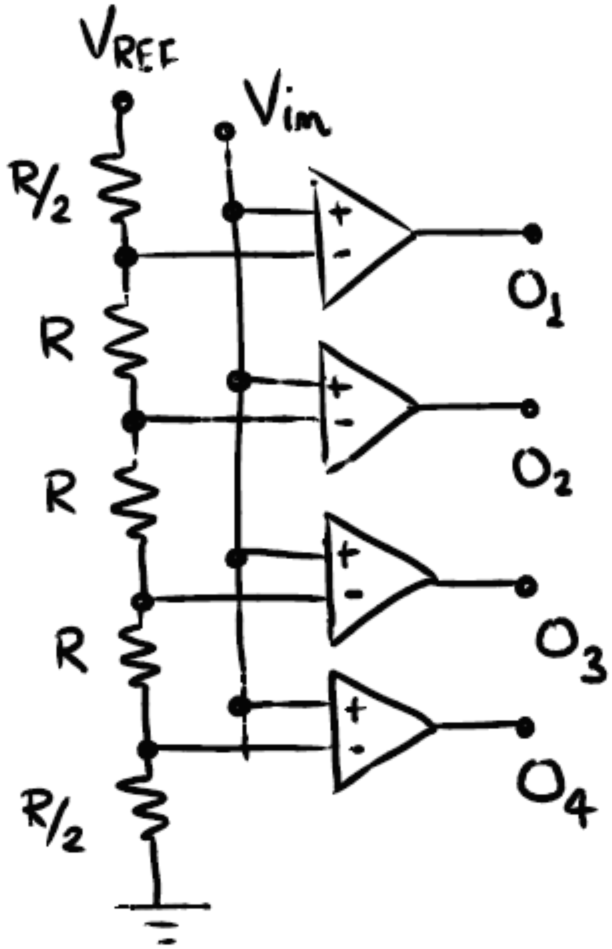
Nyquist-rate ADC

- Algorithmic ADC

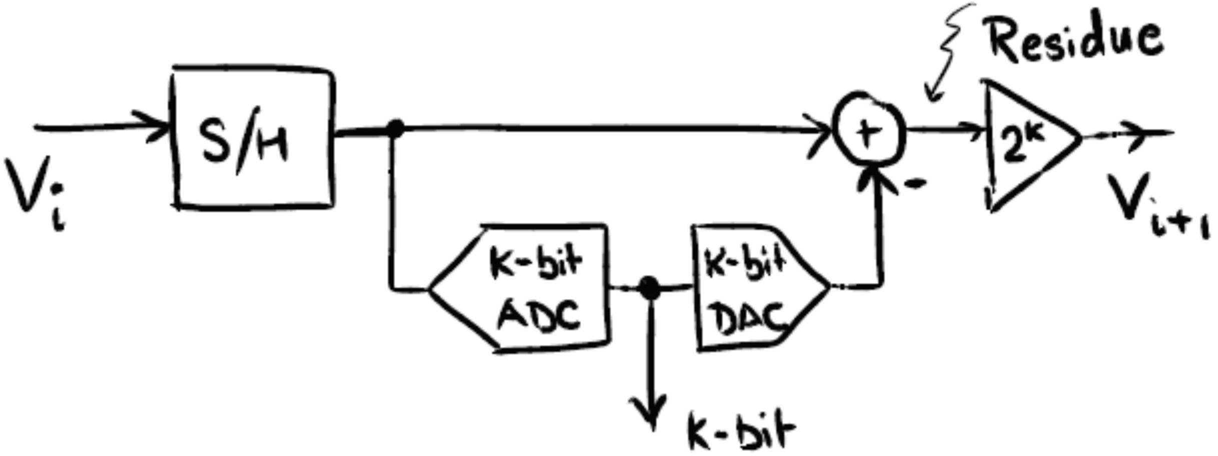
$$V_0 = V_{in};\, b_i = Cmp(V_{i-1})$$

$$V_i = 2V_{i-1} - b_i V_{ref}$$

- Flash ADC

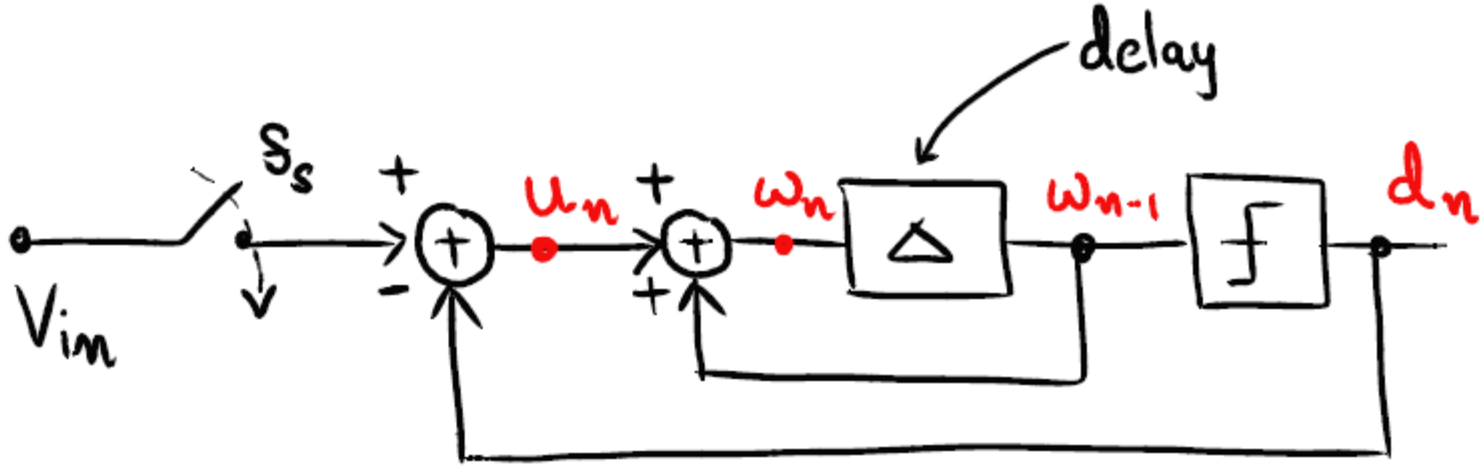


- Pipelined ADC



Oversampling ADC

- First order Sigma-Delta Modulator

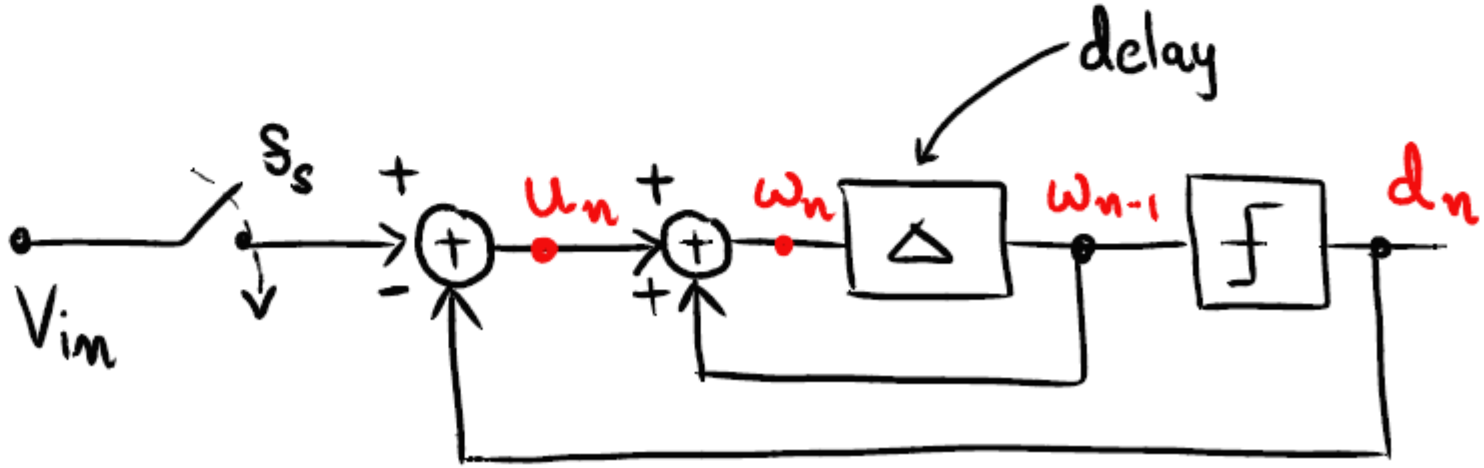


- Worksheet -

$$\omega_n = \omega_{n-1} + \left(V_{in} - D_n V_{ref}\right)$$

Oversampling ADC – Time domain analysis

- First order Sigma-Delta Modulator



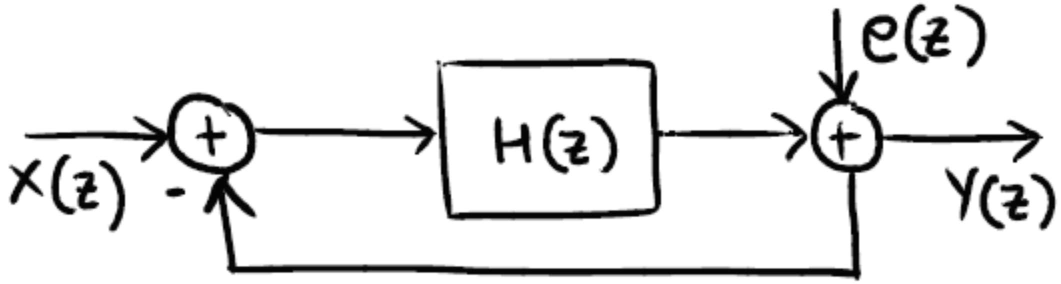
$$\omega_n = \omega_{n-1} + \left(V_{in} - D_n V_{ref}\right)$$

$$\omega_N = \omega_0 + \left(N V_{in} - \sum_n D_n V_{ref}\right)$$

$$\frac{1}{N}\omega_N = V_{in} - \frac{1}{N}\sum_n D_n V_{ref}$$

$$\boxed{\frac{1}{N}\sum_n D_n V_{ref} \rightarrow V_{in}}$$

Oversampling ADC – Frequency analysis



$$Y(z) = e(z) + H(z)[X(z) - Y(z)]$$

$$Y(z) = \left[\frac{H(z)}{1 + H(z)}\right] X(z) + \left[\frac{1}{1 + H(z)}\right] e(z)$$

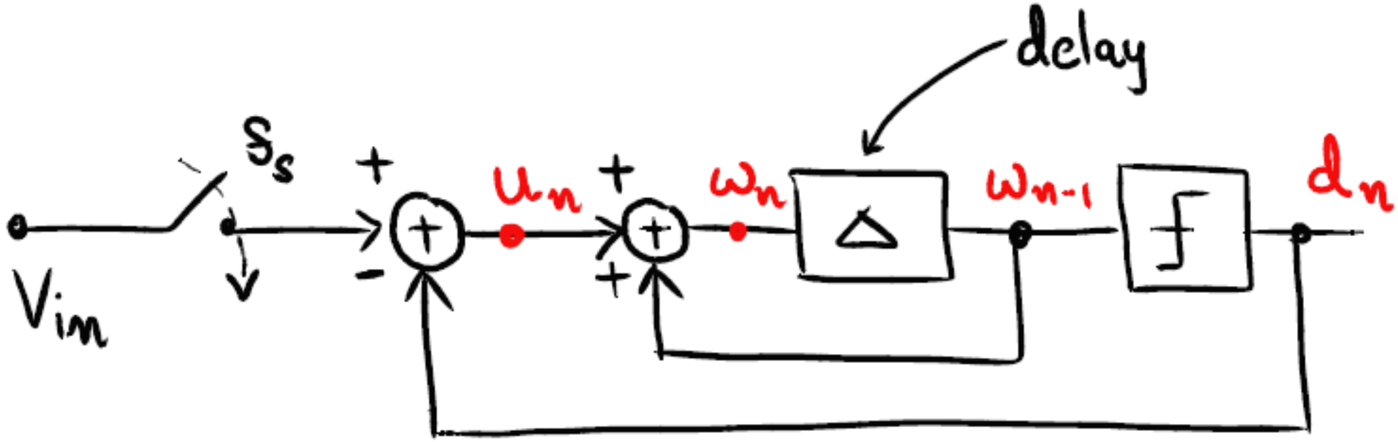
Signal Transfer Function (STF) Noise Transfer Function (NTF)

$$H(z) = \frac{1}{z - 1}$$

$$Y(z) = z^{-1} X(z) + (1 - z^{-1}) e(z)$$

$$NTF = e[n] - e[n-1]$$

Oversampling ADC – Frequency analysis



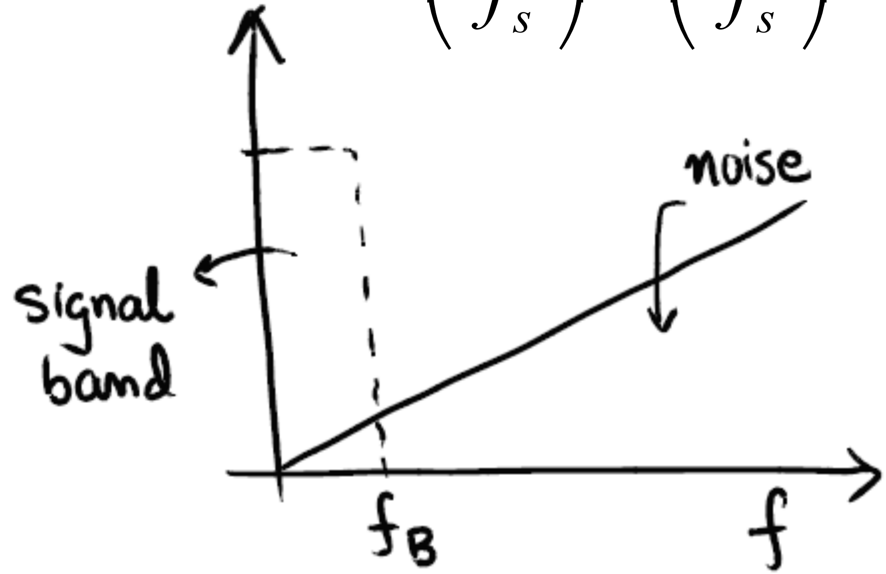
$$Y(z) = z^{-1}X(z) + (1 - z^{-1})e(z)$$

$$NTF(f) = 1 - e^{-j2\pi f/f_s}$$

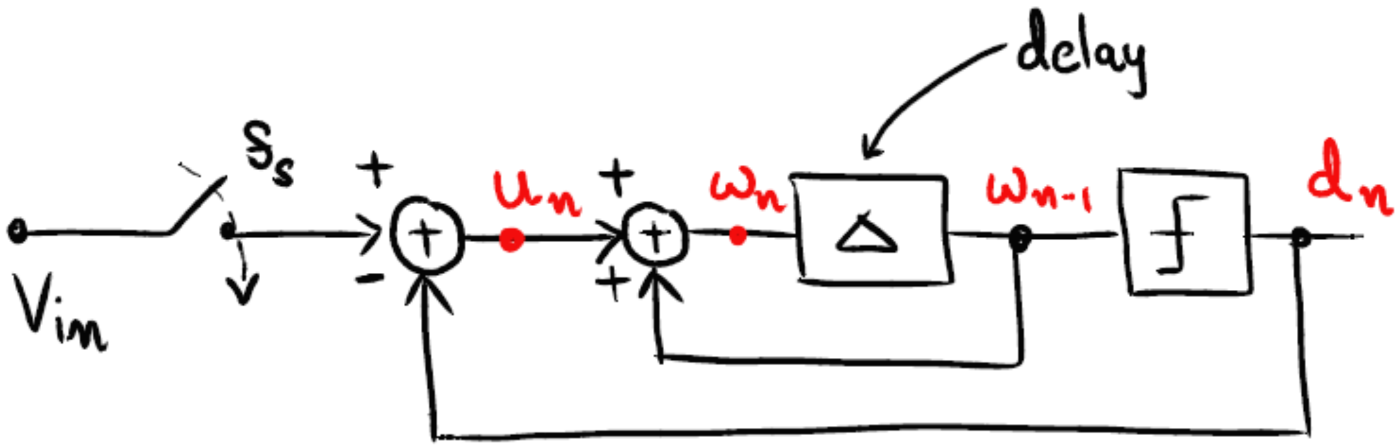
$$\sin\left(\frac{\pi f}{f_s}\right) \approx \left(\frac{\pi f}{f_s}\right)$$

$$NTF(f) = \sin\left(\frac{\pi f}{f_s}\right) 2je^{j\pi f/f_s}$$

$$|NTF(f)| = 2\sin\left(\frac{\pi f}{f_s}\right)$$



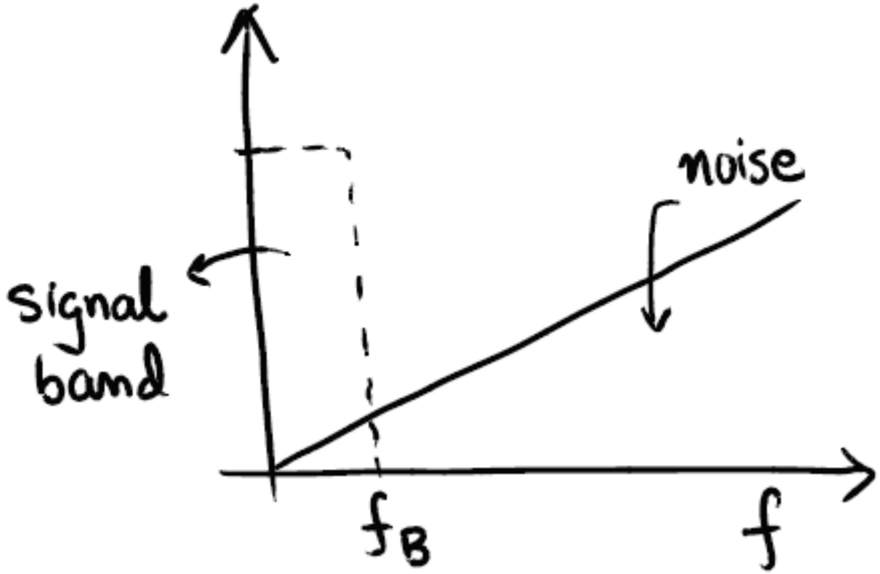
Oversampling ADC – Frequency analysis



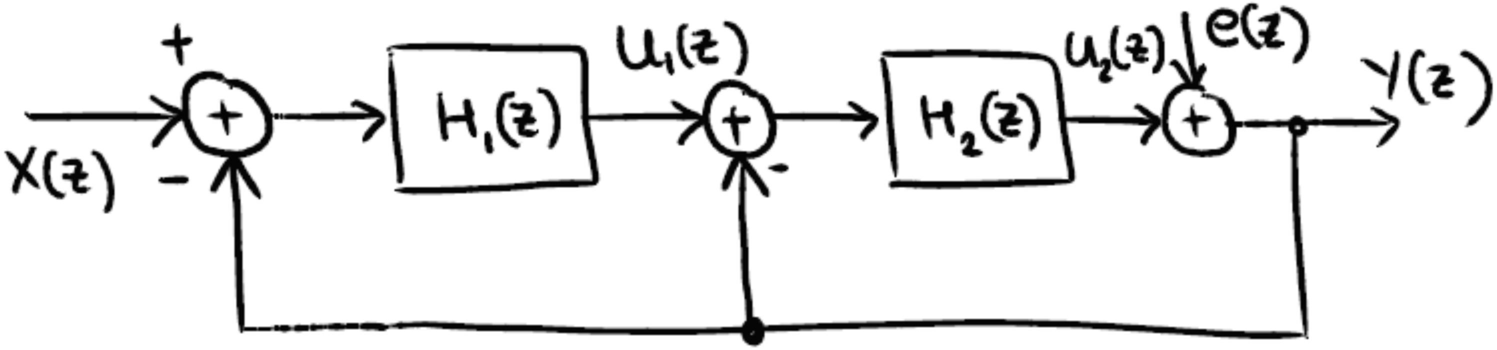
$$P_e = \int_{-f_0}^{f_0} S_e(f)\,|NTF(f)|^2\,df$$

$$P_e = \int_{-f_0}^{f_0} \frac{\Delta^2}{12 f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df$$

$$P_e = \frac{\Delta^2\pi^2}{36}\left[\frac{2 f_0}{f_s}\right]^3 = \frac{\Delta^2\pi^2}{36}\left[\frac{1}{OSR}\right]^3$$



Higher order Sigma-Delta Modulator



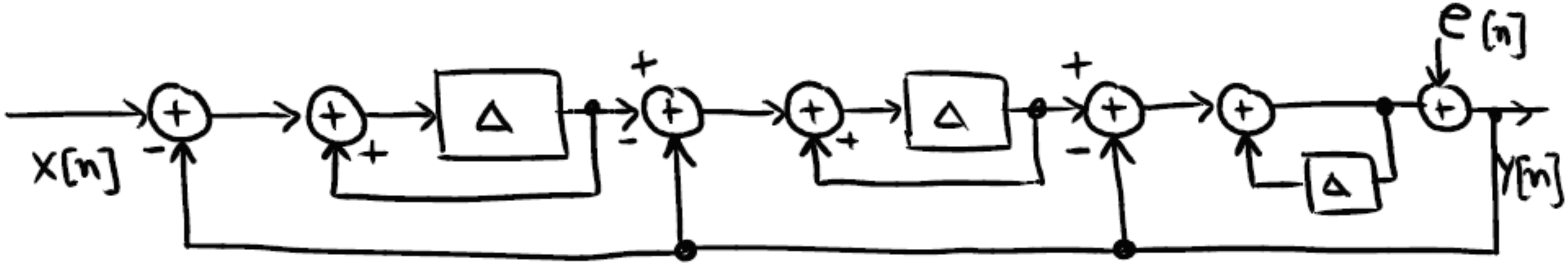
$$P_e = \int_{-f_0}^{f_0} S_e(f)\,|\,NTF(f)\,|^2\,df$$

$$H_1(z) = \frac{1}{z-1} \qquad H_2(z) = \frac{z}{z-1}$$

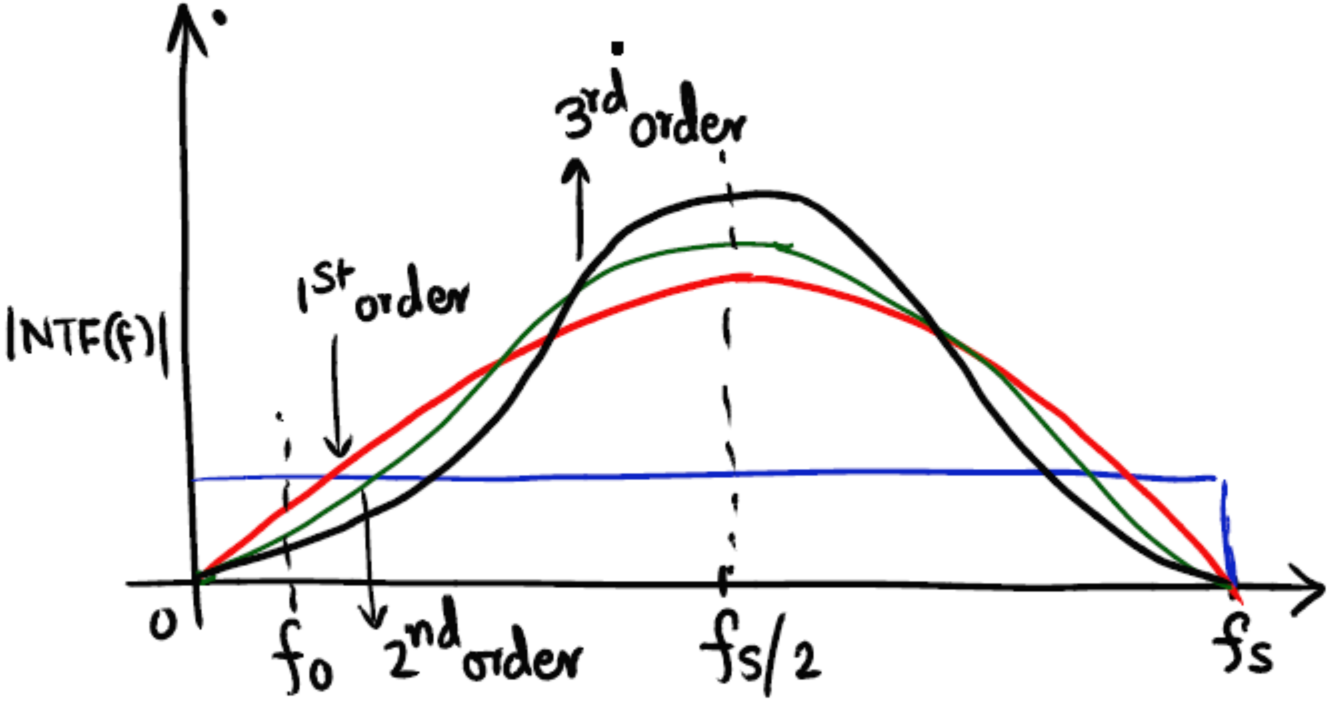
$$P_e = \frac{\Delta^2 \pi^4}{60}\left[\frac{1}{OSR}\right]^5$$

$$SNR = 10\log P_{sig} + 110\log OSR + const.$$

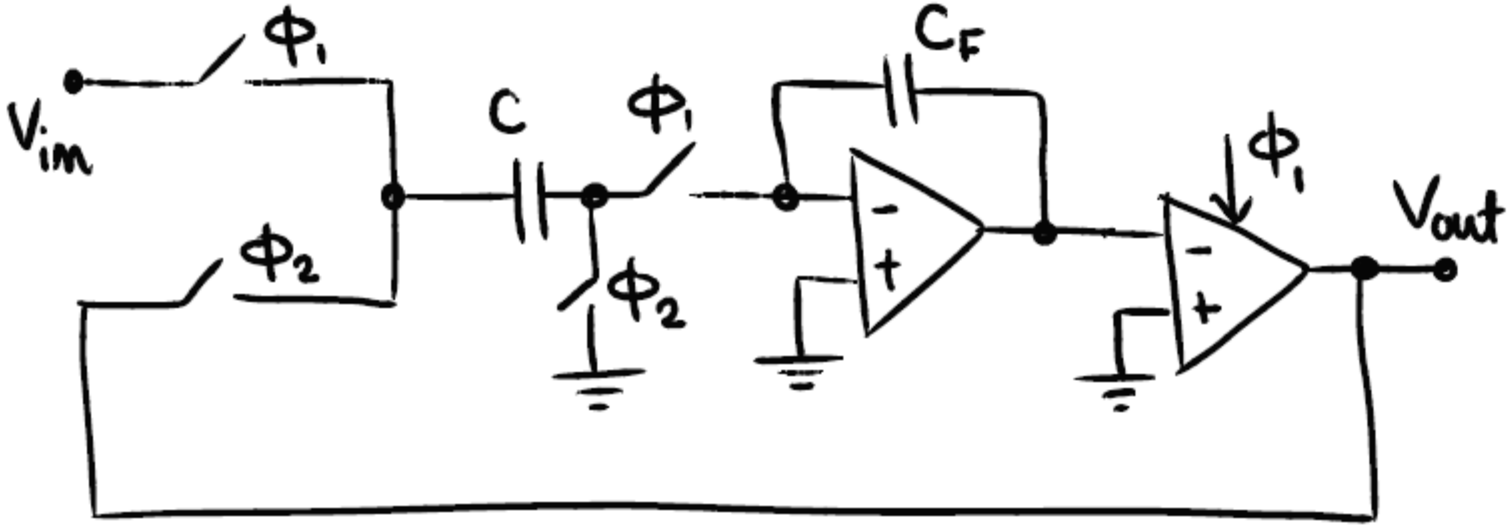
L^{th} order Sigma-Delta Modulator

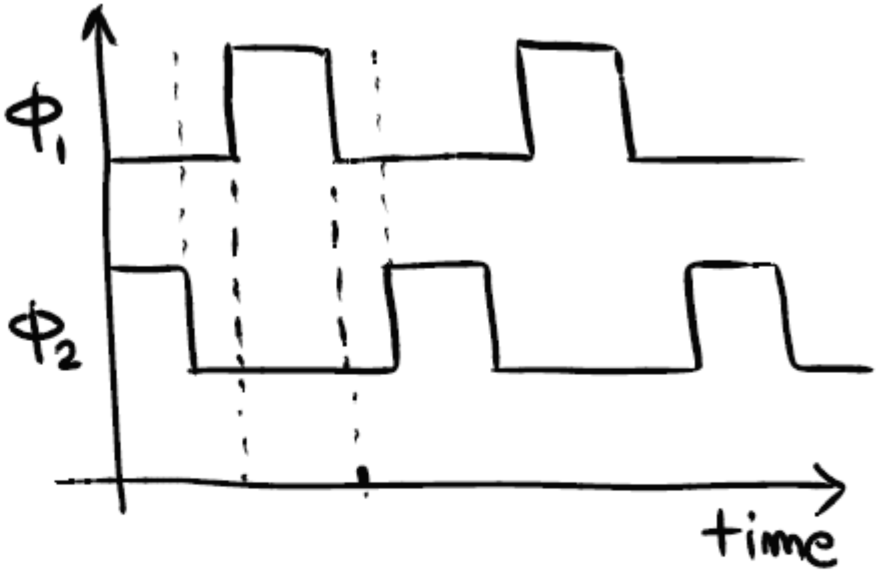


$$SNR = 10\log P_{sig} + (2L+1)10\log OSR + const.$$



Oversampling ADC – Implementation





ADC Comparison