



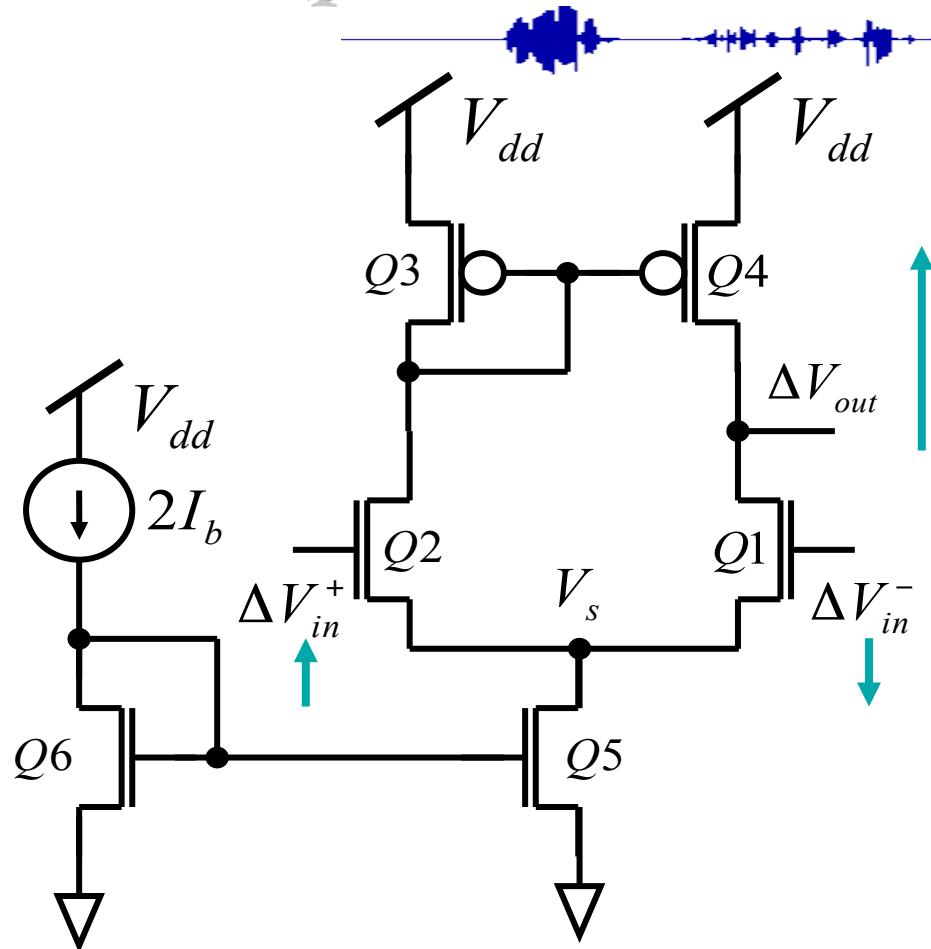
Basic Analog Circuits: AC Analysis



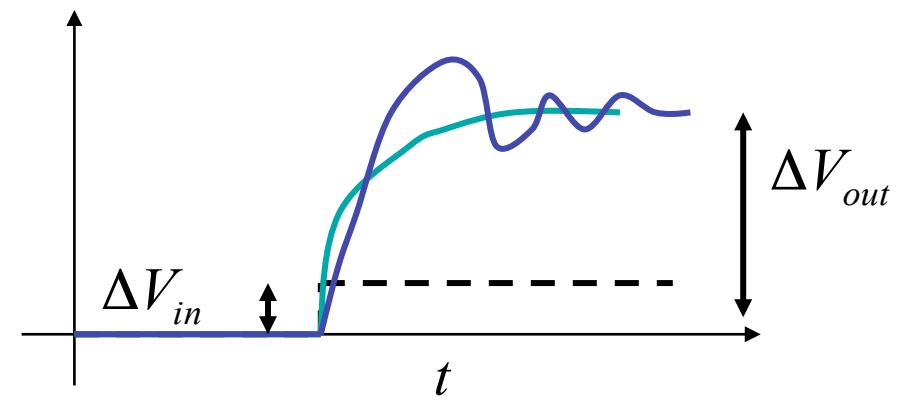
CSE562M: Analog Integrated Circuits
Shantanu Chakrabarty



DC Response and Transient Response



Till now we calculated small signal DC gain: When the input signal changes by an increment, by how much does the output voltage change.

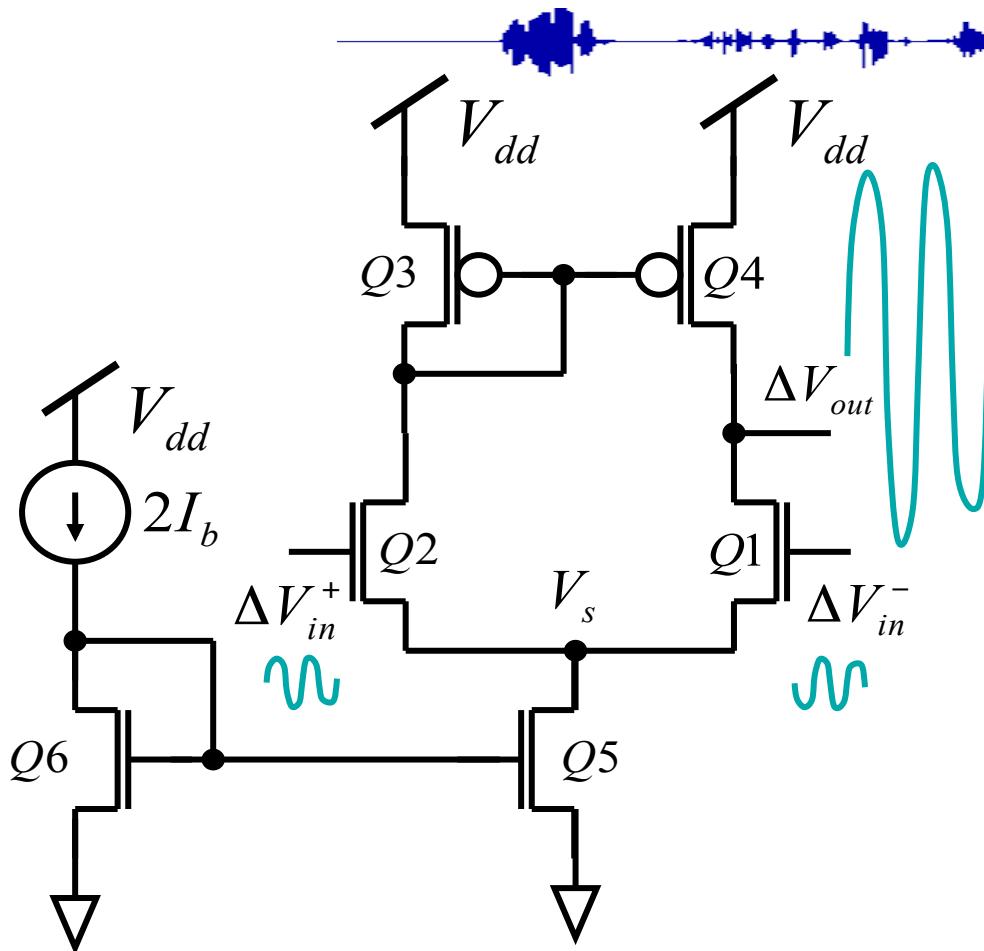


Gain

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}^+ - \Delta V_{in}^-} = -g_m(r_{ds1} \parallel r_{ds2})$$

Not concerned about speed, bandwidth and settling behavior of the amplifier.

DC Gain and AC Gain



AC gain of the amplifier is defined as a small signal gain at a particular frequency.

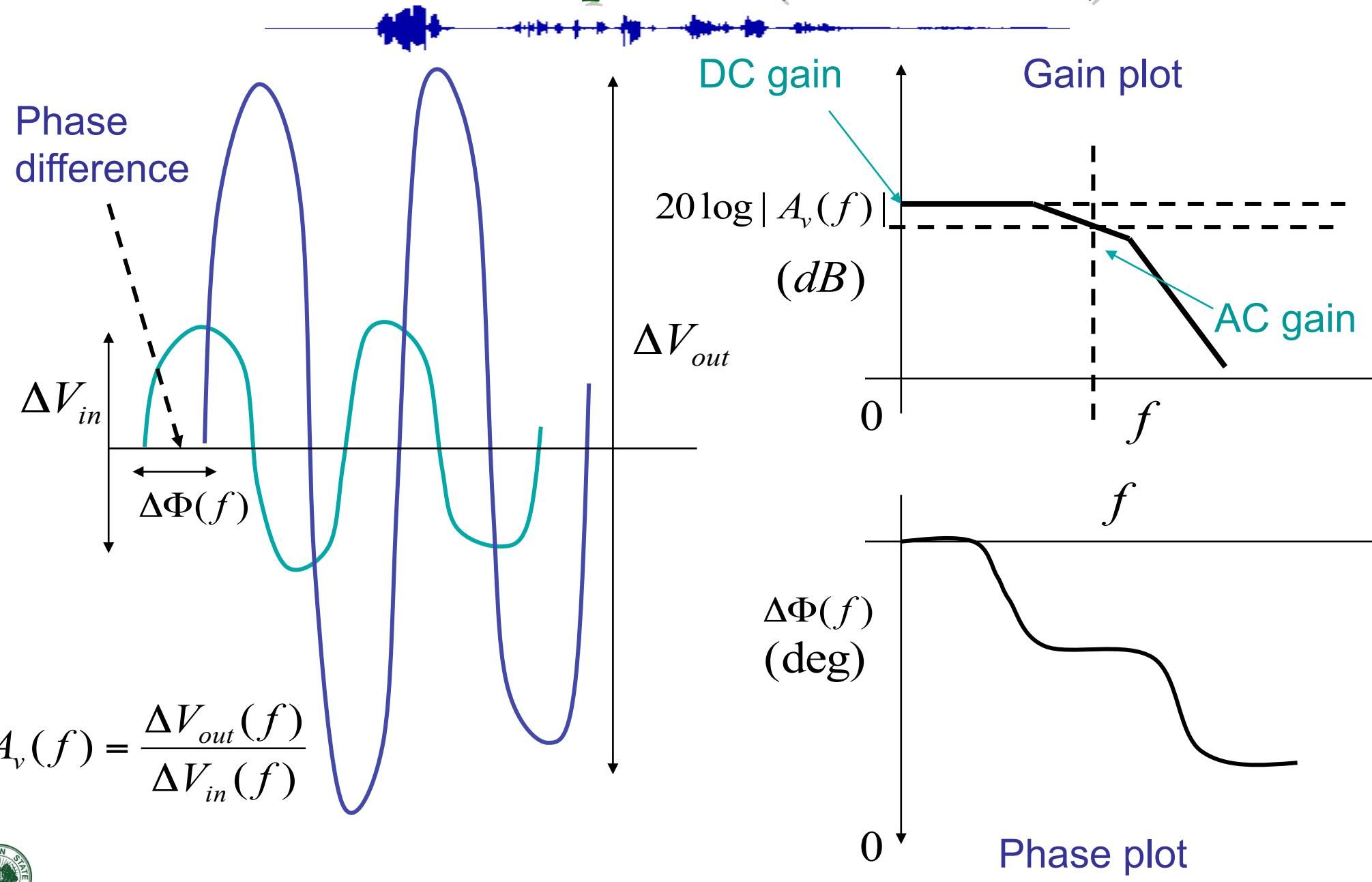
For a small signal model, if the input of the amplifier is a sinusoid, is the output a sinusoid ?

AC gain is defined as the ratio of the amplitude of the output sinusoid versus the amplitude of the input sinusoid.

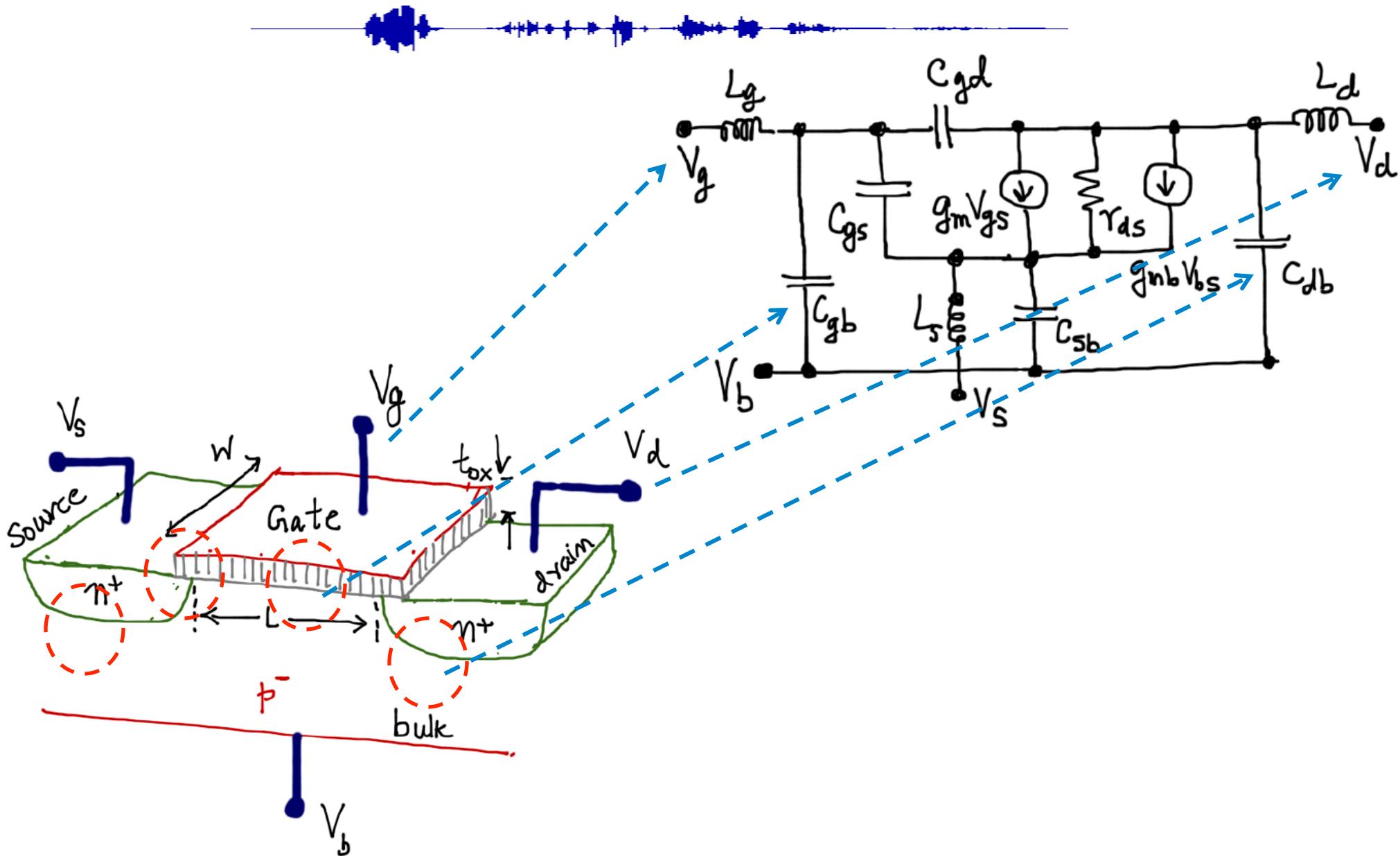
Gain

$$A_v(f) = \frac{|\Delta V_{out}(f)|}{|\Delta V_{in}(f)|}$$

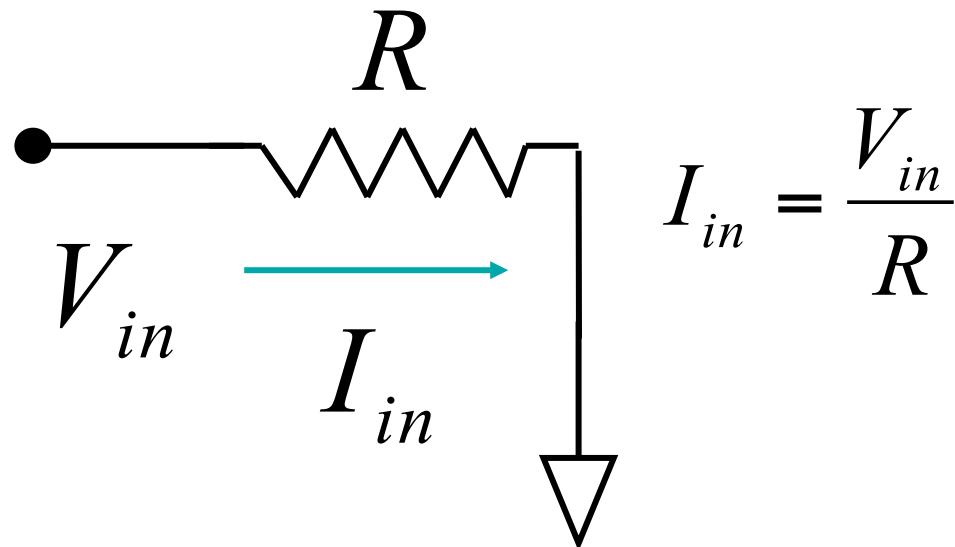
Gain and Phase Response (Bode Plots)



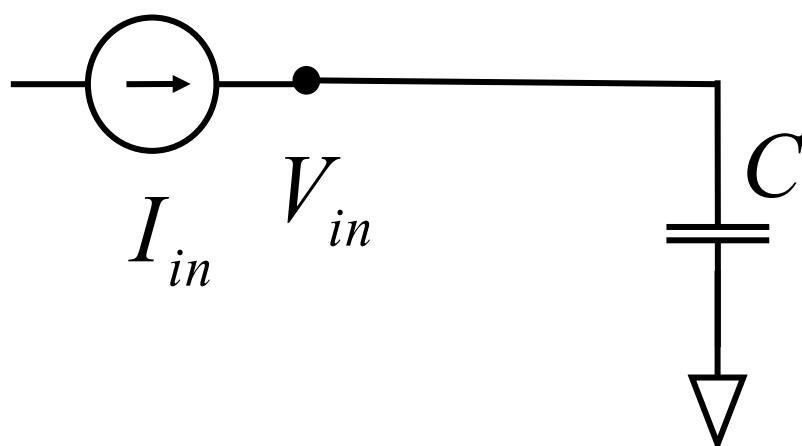
AC Model of MOSFET Transistor



Fundamentals of Frequency Analysis



The relationship is independent of time. When the input voltage changes instantaneously, the current through a resistor changes instantaneously (without any delay).

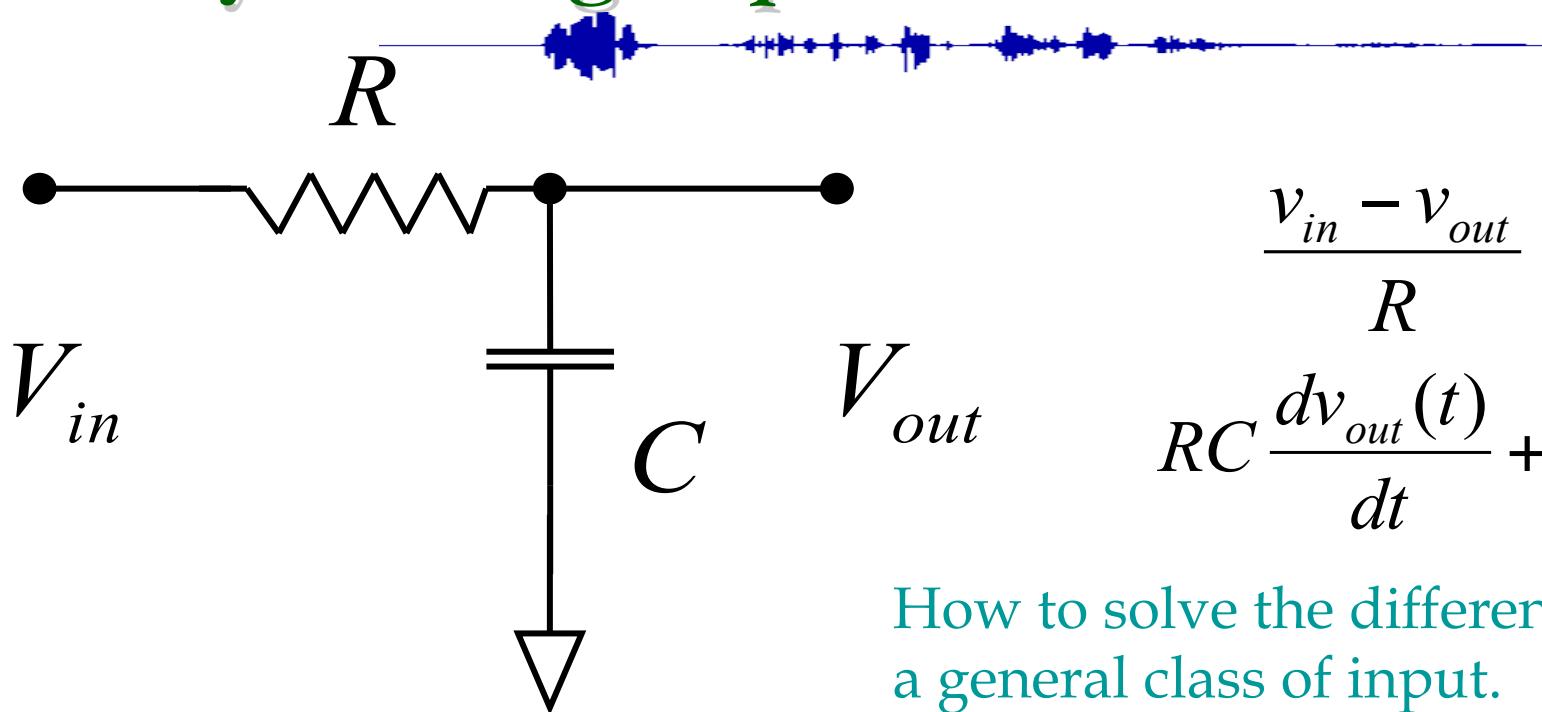


Voltage across a capacitor can NOT change instantaneously.

DC current through a capacitor = 0

We will not consider inductors at this point. (But is important for radio-frequency integrated circuits).

Analysis using Laplace Transforms



$$\frac{v_{in} - v_{out}}{R} = C \frac{dv_{out}}{dt}$$

$$RC \frac{dv_{out}(t)}{dt} + v_{out}(t) = v_{in}(t)$$

How to solve the differential equation for a general class of input.

$$RCsV_{out}(s) + V_{out}(s) = V_{in}(s)$$

Laplace transform for solving differential equations.

$$V_{out}(s) = \frac{1}{(1 + RCs)} V_{in}(s)$$

System transfer function

Output response

Input stimulus



Laplace Transform Tables



$$v_{in}(t) = \begin{cases} 1 & t > 0 \\ 0 & t \leq 0 \end{cases} \quad V_{in}(s) = \frac{1}{s}$$

$$v_{in}(t) = e^{-at} \quad V_{in}(s) = \frac{1}{s + a}$$

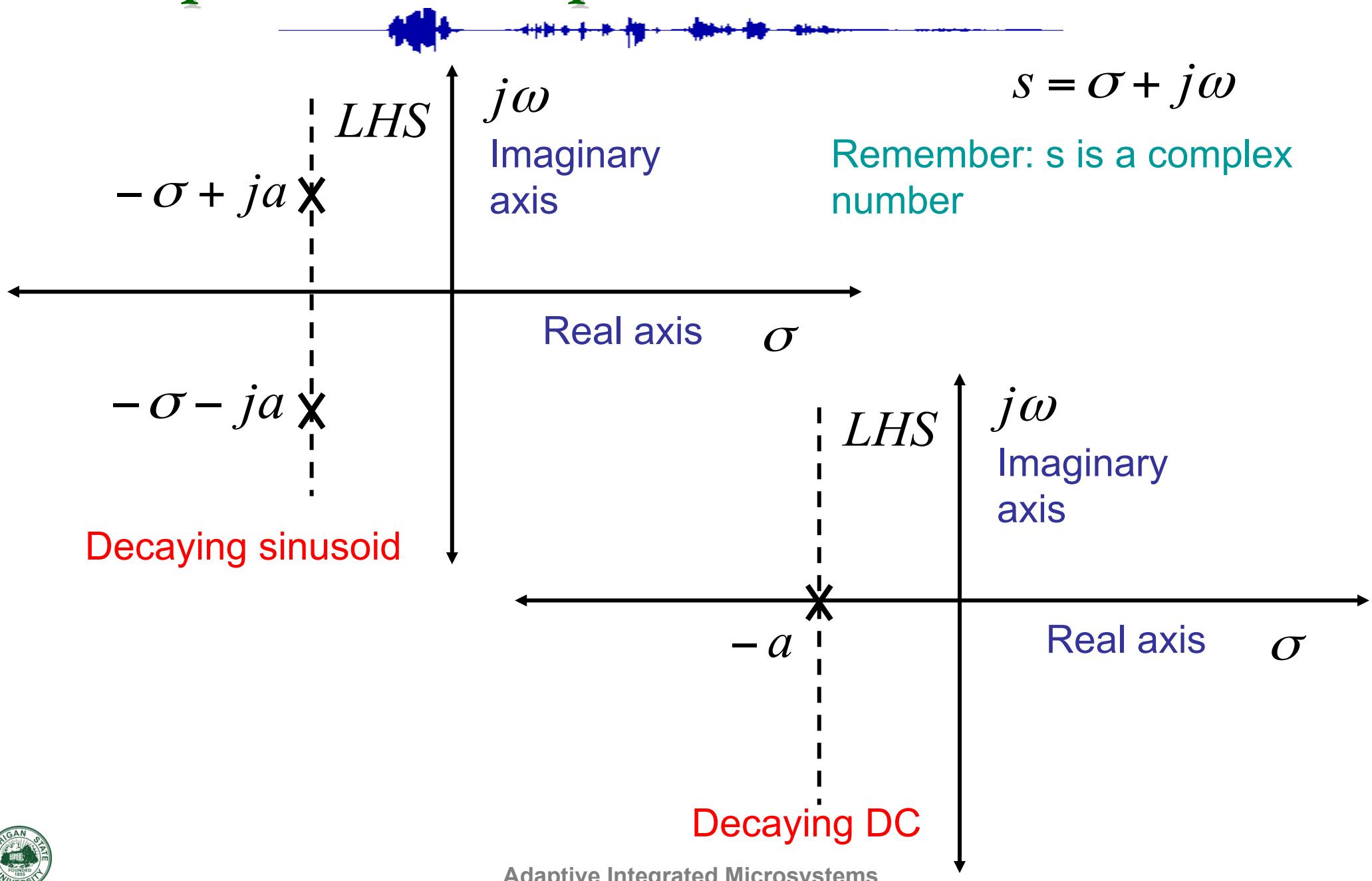
$$v_{in}(t) = \sin(at) \quad V_{in}(s) = \frac{a}{s^2 + a^2}$$

$$v_{in}(t) = \cos(at) \quad V_{in}(s) = \frac{s}{s^2 + a^2}$$

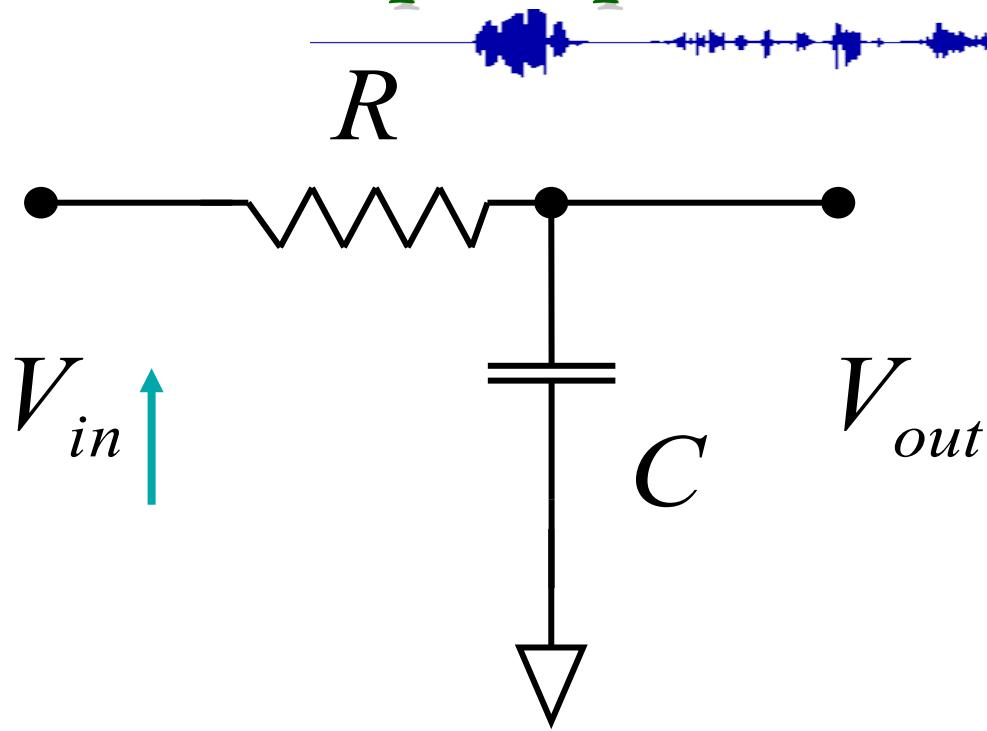
Laplace transform maps functions into a rational polynomials.
Manipulation of polynomial is easy (requires only algebraic
multiplications and additions).



Interpretation of s-plane



Circuit Step-response



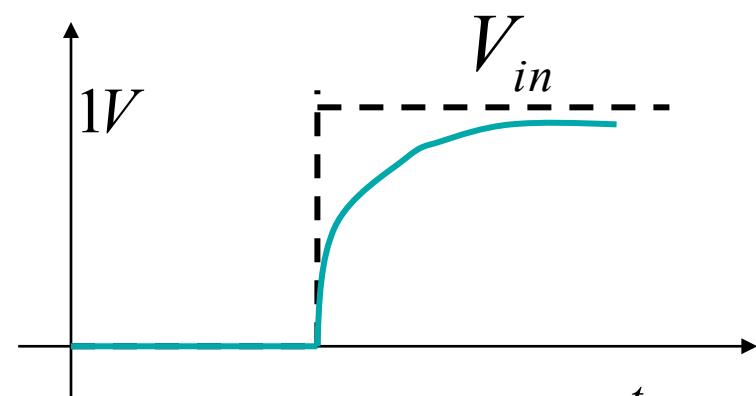
Capacitor charges up exponentially at a rate equal to time-constant RC .

Larger the resistance and capacitance, slower is the charging rate..

In steady-state the voltage across the capacitor is constant and the dc current is equal to zero.

$$V_{in}(s) = \frac{1}{s}$$

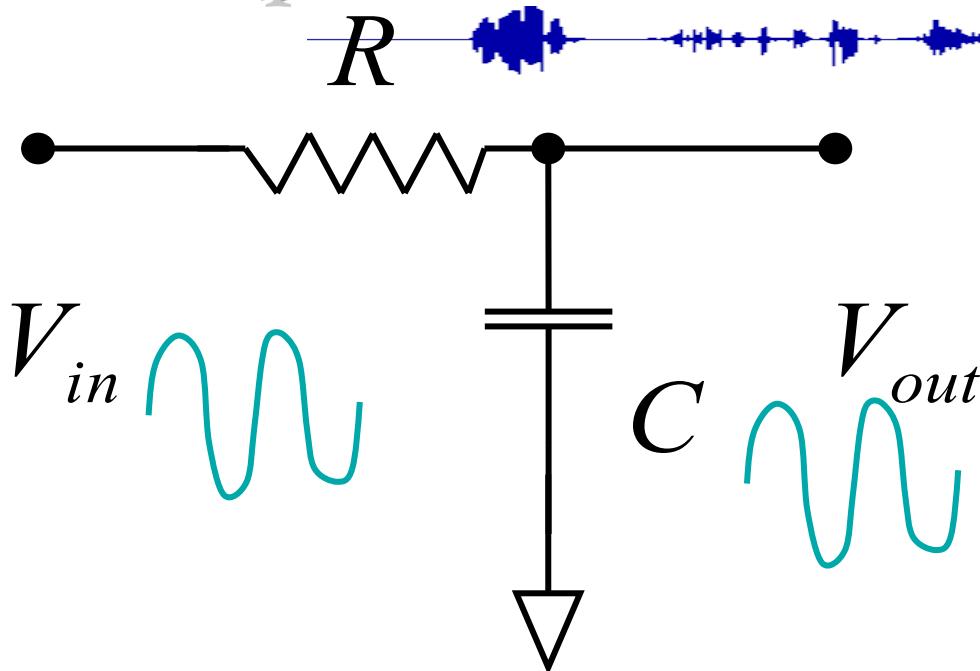
$$V_{out}(s) = \frac{1}{s(1 + RCs)}$$



$$V_{out}(t) = 1 - e^{-\frac{t}{RC}}$$



AC Response



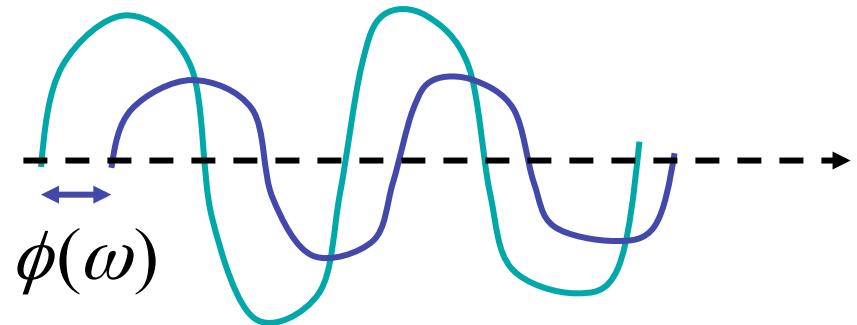
Input is a sinusoid, output is also a sinusoid with an amplitude that is dependent on frequency.

Phase difference between the input and output sinusoid is also frequency dependent.

REMEMBER: Frequency of the input and output is the SAME for a linear system.

$$V_{in}(s) = \frac{\omega}{s^2 + \omega^2}$$

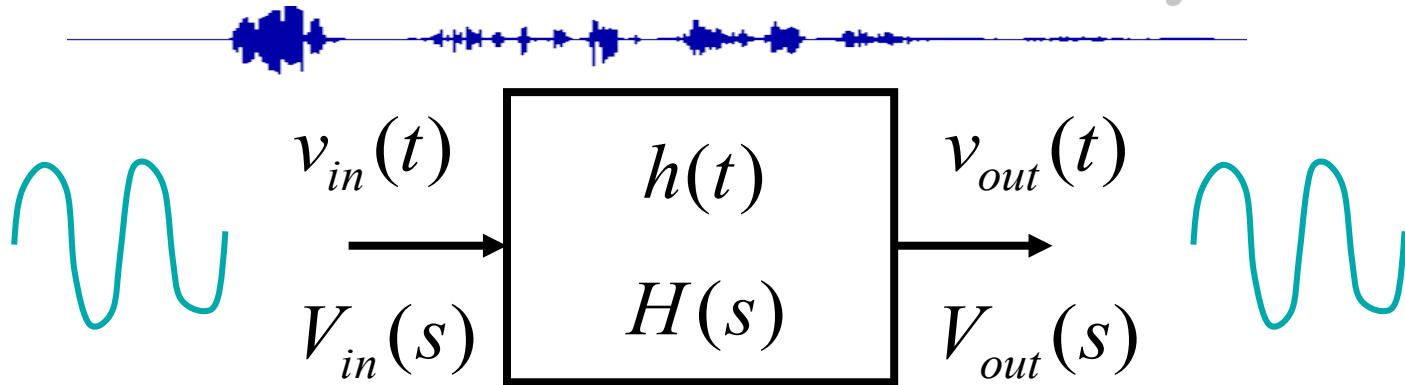
$$V_{out}(s) = \frac{\omega}{(s^2 + \omega^2)(1 + RCs)}$$



$$\frac{|V_{out}(\omega)|}{|V_{in}(\omega)|} = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}}$$

$$\phi(\omega) = -\tan^{-1}(\omega RC)$$

Model of a Linear Time-invariant System



$$H(s) = K \frac{(s - z_1)(s - z_2) \dots (s - z_M)}{(s - p_1)(s - p_2) \dots (s - p_N)}$$

z_i Zeros of the transfer function (frequencies where the output is zero).

p_i Poles of the transfer function (frequencies where the output is infinity).

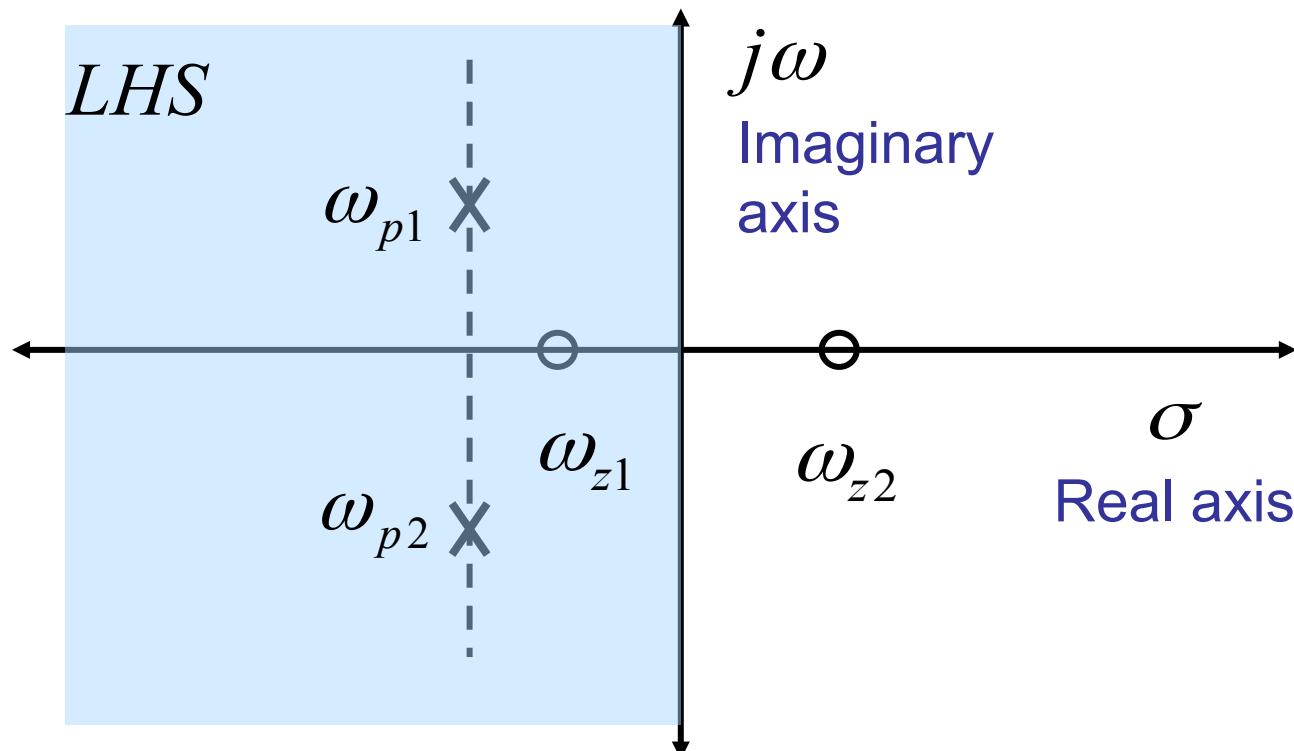
Poles of a stable system are always located in the left-hand side of the s-plane (remember: s is a complex number).



System Transfer Function on an s-plane

$$H(s) = K \frac{(1 + \frac{s}{\omega_{z1}})(1 - \frac{s}{\omega_{z2}})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$
$$s = \sigma + j\omega$$

Remember: s is a complex number

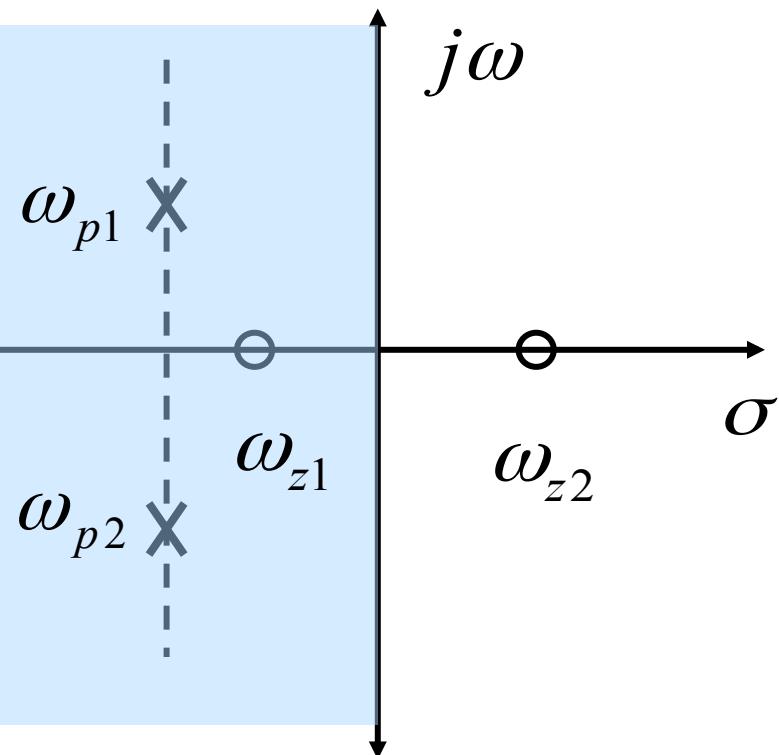


LHS Poles mean stable system. Zeros can be on the RHS.

Properties of Stable Realizable LTI Systems



LHS



Complex poles and zeros always appear in conjugate pairs.

Singular poles can only be located on the real axis.

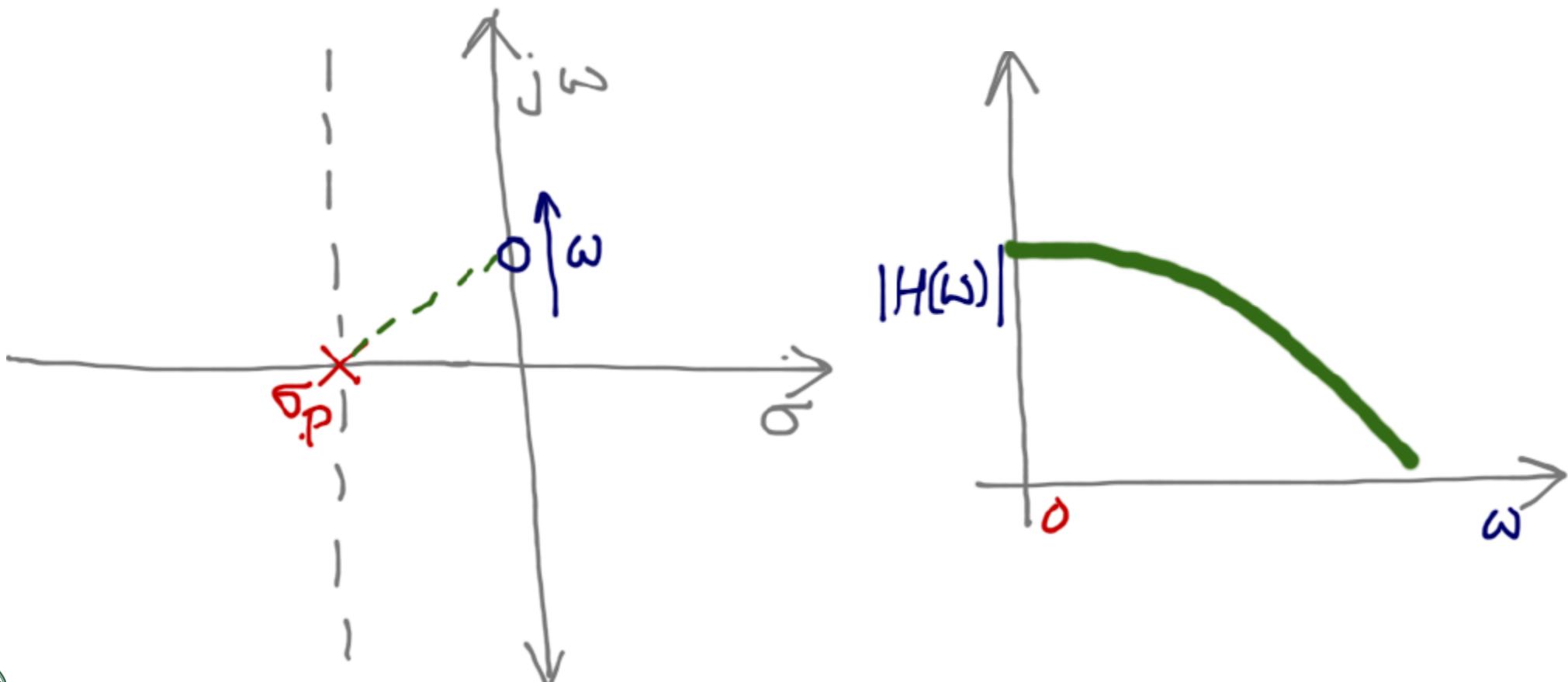
Is there a conceptual interpretation of s-plane mapping other than mathematical convenience ?



Conceptual Interpretation of s-plane

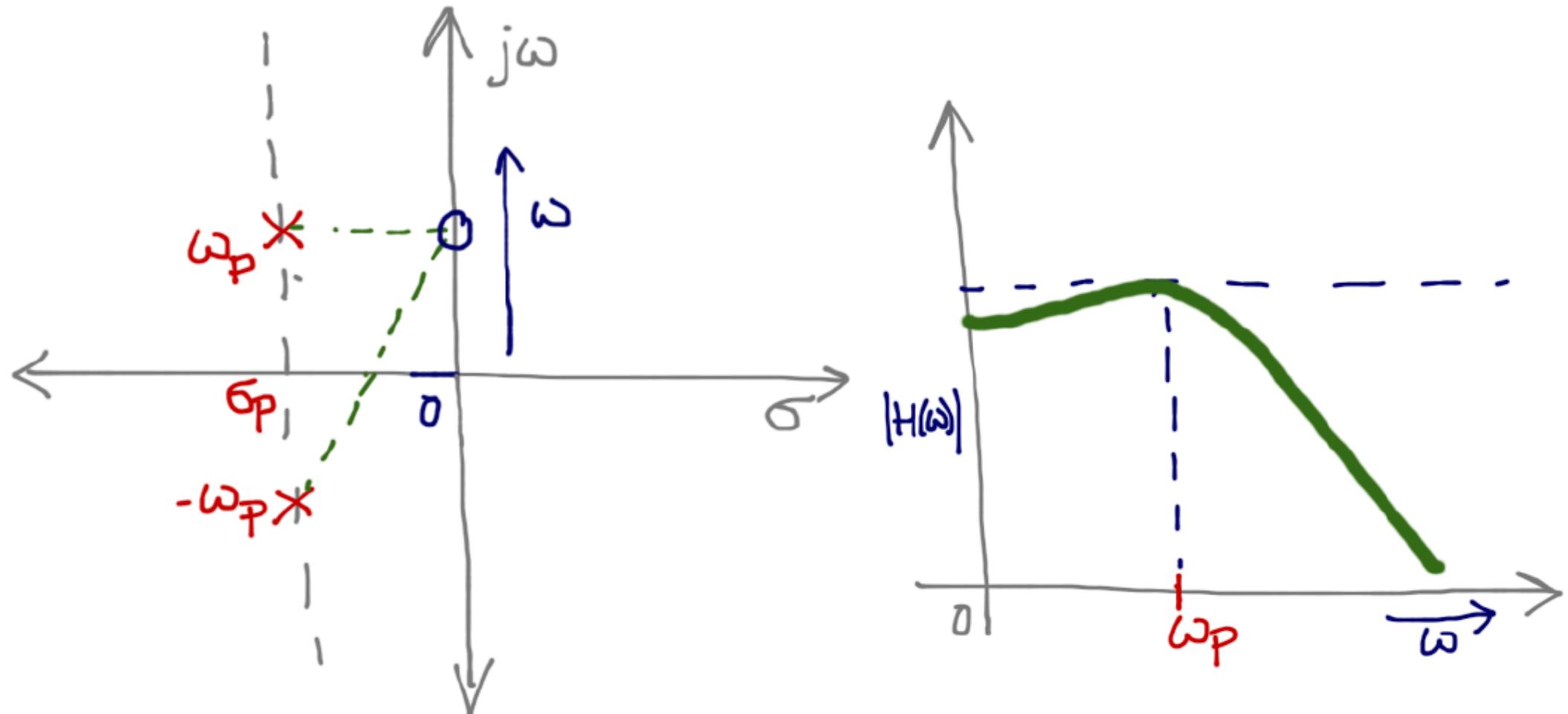


- Frequency sweep is equivalent to traversing along the $j\omega$ axis.
- Proximity near a pole increases the magnitude of the output.
Proximity near a zero decreases the magnitude of the output.



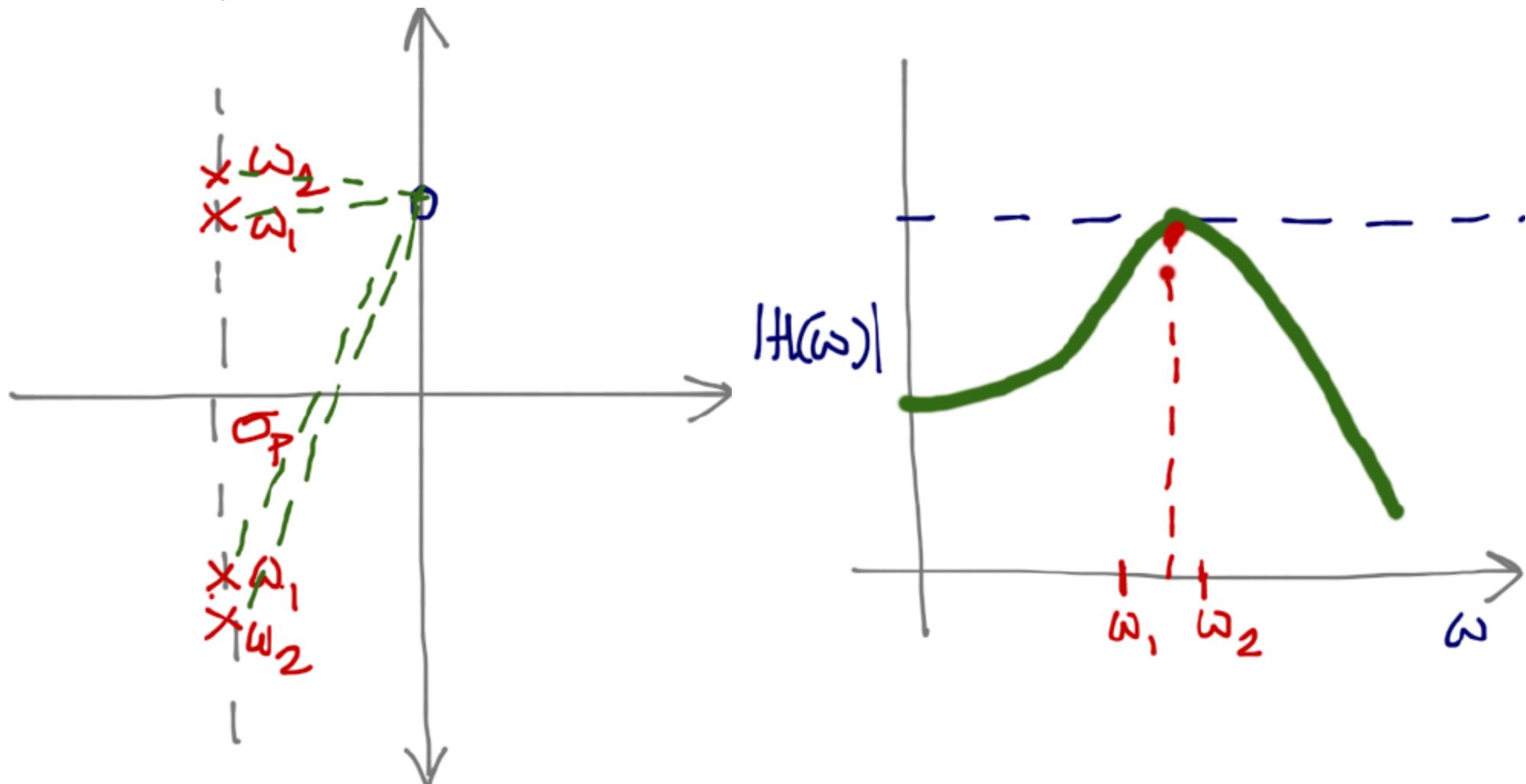
Conceptual Interpretation of s-plane

- Complex and conjugate poles enhances the gain a specific frequency.



Conceptual Interpretation of s-plane

- Complex poles close to each other enhances the gain at the frequency at which the poles are located.



How to Approximate the System Gain

$$H(s) = K \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 - \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

$$s = \sigma + j\omega$$

Remember: s is a complex number

We want to find out the magnitude of a sinusoidal signal with frequency ω rad/sec.

Evaluate $H(s)$ at $s = j\omega$

$$|H(j\omega)| = K \frac{\left|\left(1 + \frac{j\omega}{\omega_{z1}}\right)\left(1 - \frac{j\omega}{\omega_{z2}}\right)\right|}{\left|\left(1 + \frac{j\omega}{\omega_{p1}}\right)\left(1 + \frac{j\omega}{\omega_{p2}}\right)\right|}$$

Magnitude of the system response.



How to Approximate the System Gain



Compute the log-magnitude where multiplications/ divisions translate to additions and subtractions.

$$20 \log |H(s)| = 20 \log K + 10 \log\left(1 + \frac{\omega^2}{\omega_{z1}^2}\right) + 10 \log\left(1 + \frac{\omega^2}{\omega_{z2}^2}\right) - 10 \log\left(1 + \frac{\omega^2}{\omega_{p1}^2}\right) - 10 \log\left(1 + \frac{\omega^2}{\omega_{p2}^2}\right)$$

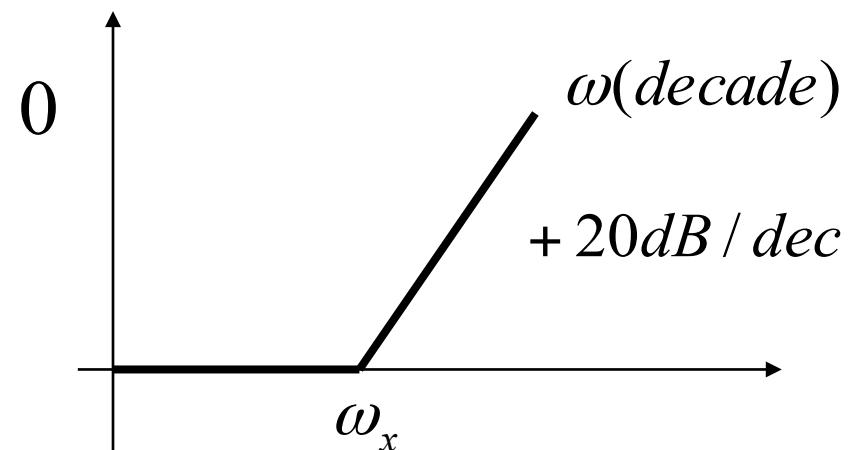
↑ ↑ ↑ ↑ ↑

DC response 1st zero 2nd zero 1st pole 2nd pole

Basic operation

$$10 \log\left(1 + \frac{\omega^2}{\omega_x^2}\right) = \begin{cases} 0; \omega \ll \omega_x \\ 20 \log \frac{\omega}{\omega_x}; \omega \gg \omega_x \end{cases}$$

Adaptive Integrated Microsystems



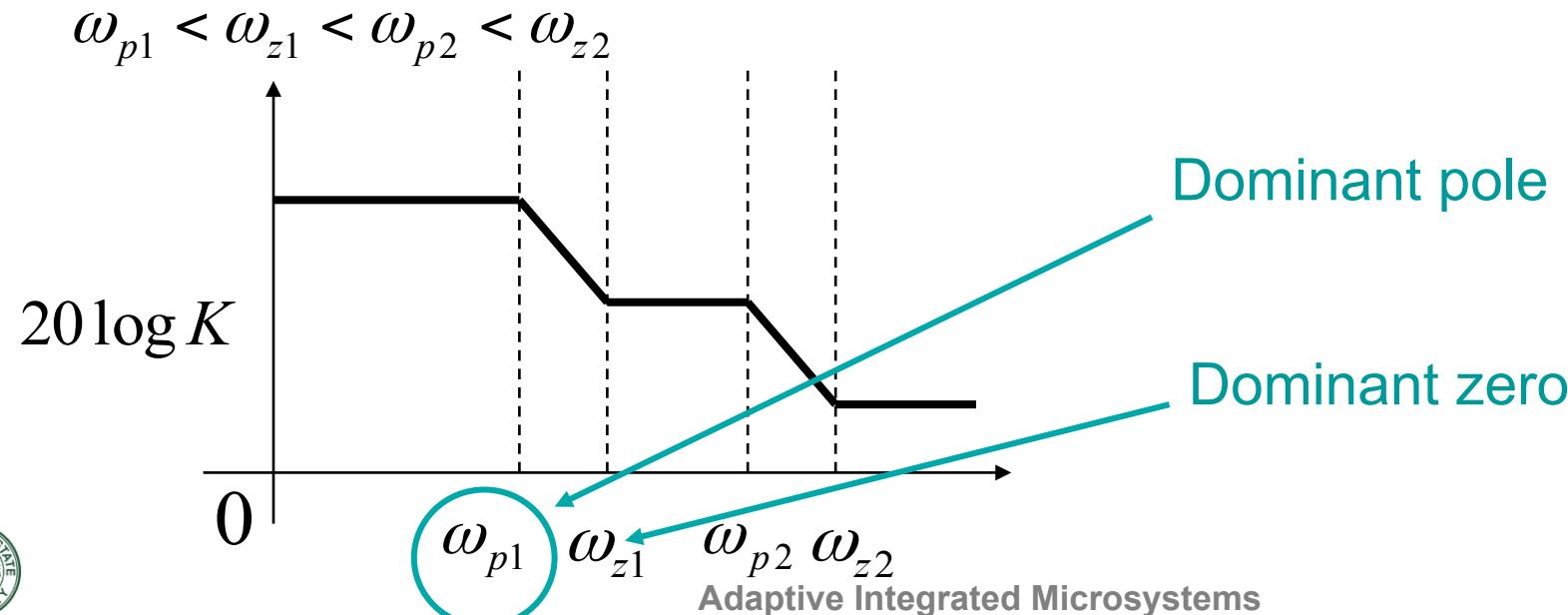
How to Approximate the System Gain


$$20 \log |H(s)| = 20 \log K + 10 \log\left(1 + \frac{\omega^2}{\omega_{z1}}\right) + 10 \log\left(1 + \frac{\omega^2}{\omega_{z2}}\right) - 10 \log\left(1 + \frac{\omega^2}{\omega_{p1}}\right) - 10 \log\left(1 + \frac{\omega^2}{\omega_{p2}}\right)$$

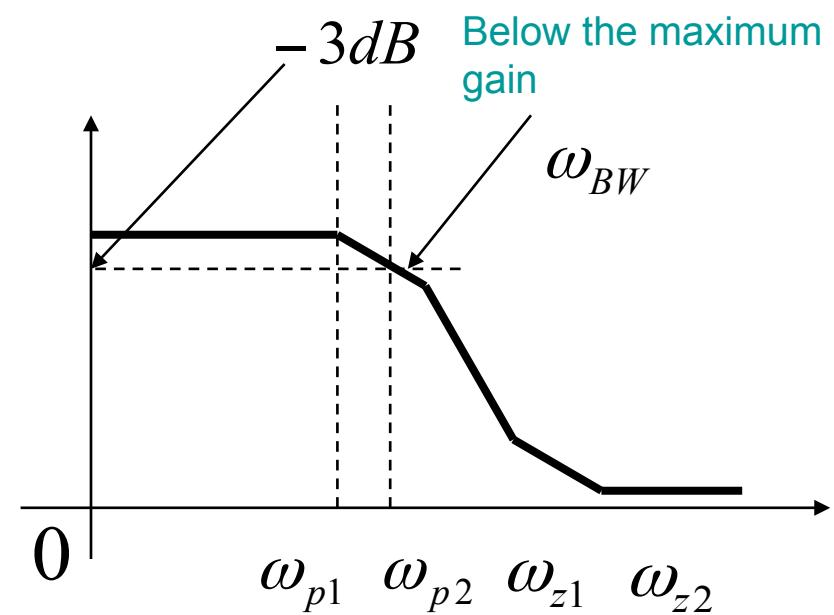
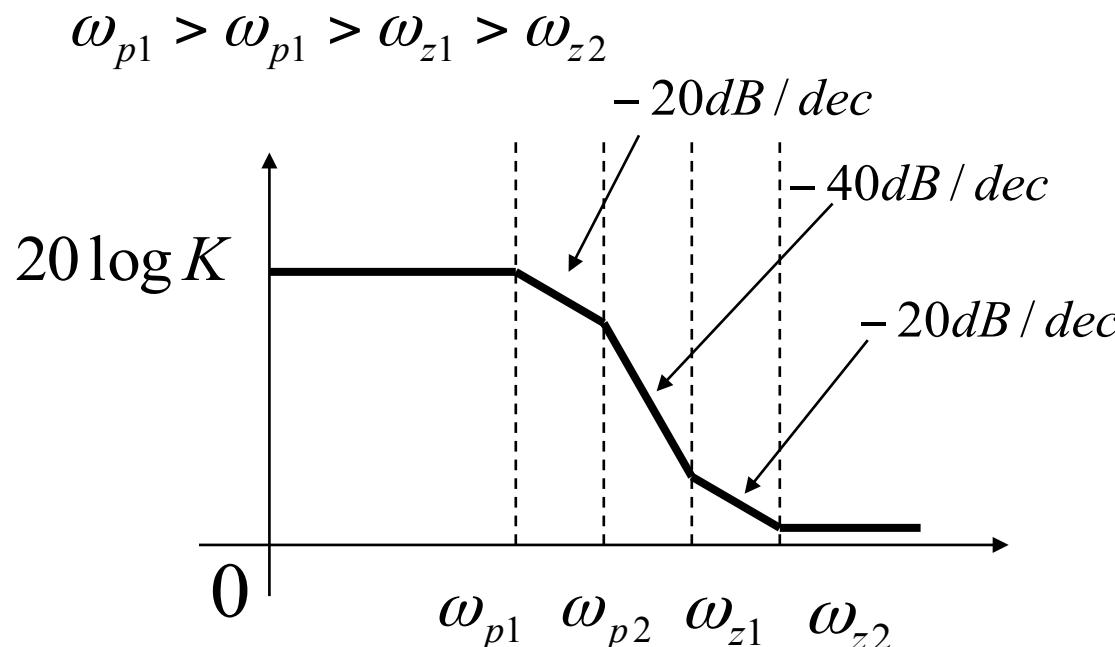
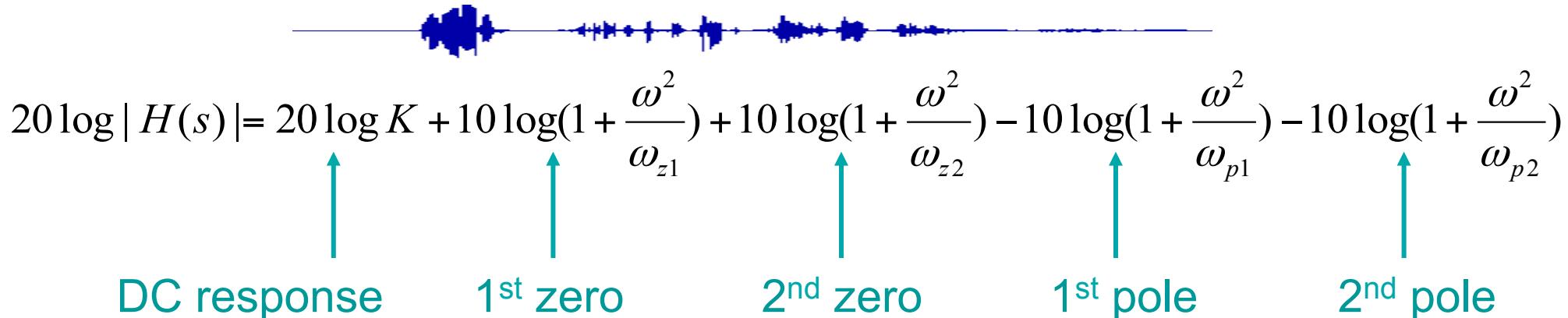
DC response 1st zero 2nd zero 1st pole 2nd pole

After a zero the gain changes by +20dB/dec.

After a pole the gain changes by -20dB/dec.

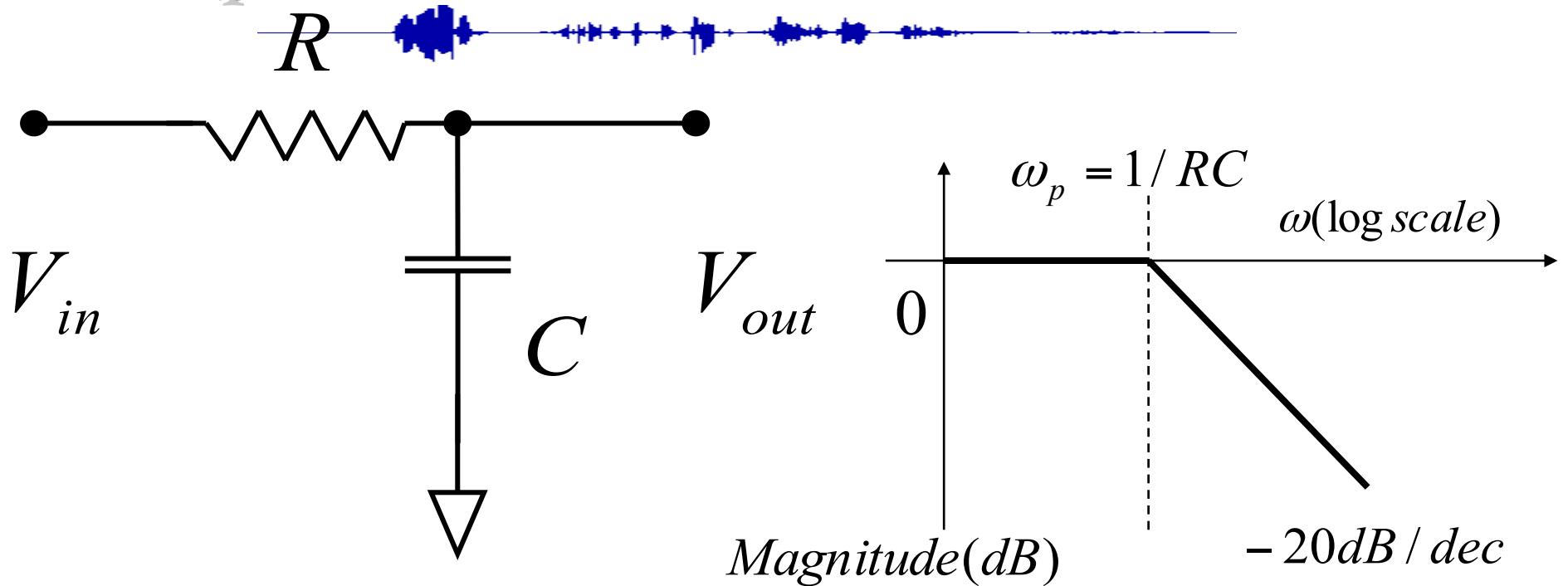


3dB Bandwidth



Bandwidth is defined as the frequency at which the gain reduces by 3dB from the maximum.

AC Response



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(1 + RCs)}$$

Only ONE pole.

$$R = 1M\Omega$$

$$H(\omega) = \frac{1}{(1 + j\omega RC)}$$

$$C = 1pF$$

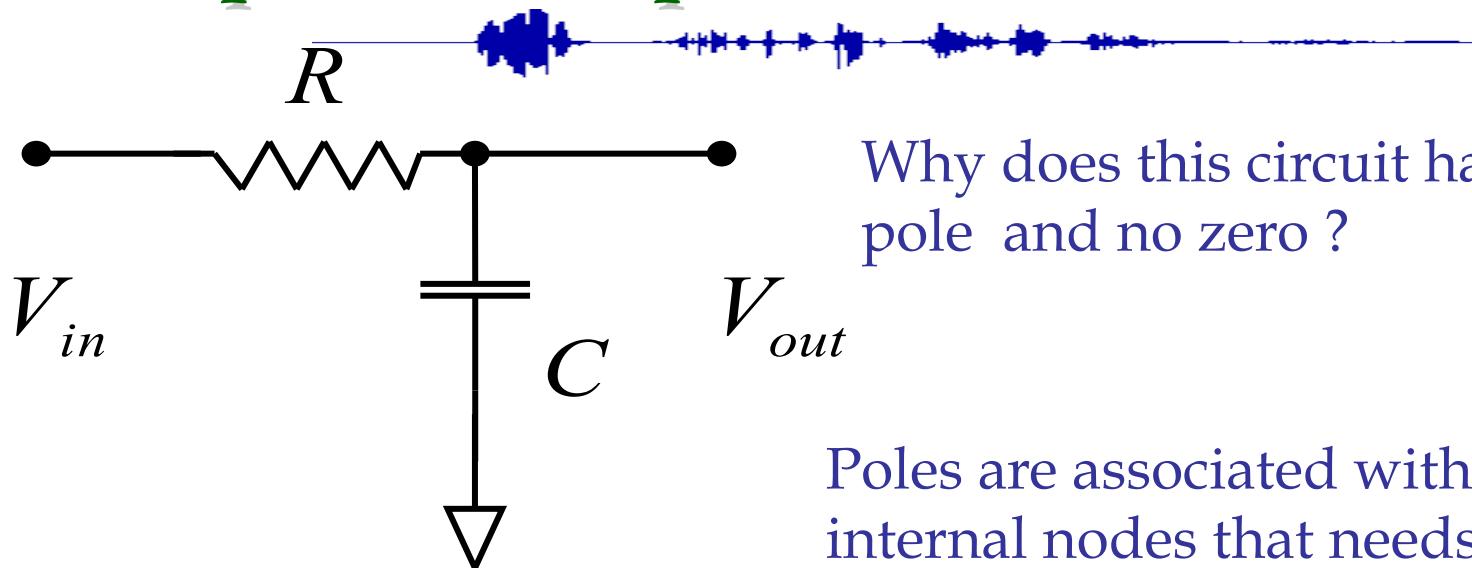
$$H(\omega) = \frac{1}{(1 + j\frac{\omega}{1/RC})}$$

$$\omega_p = 10^6 \text{ rad/s}$$

$$f_p = \frac{\omega}{2\pi} \text{ Hz}$$

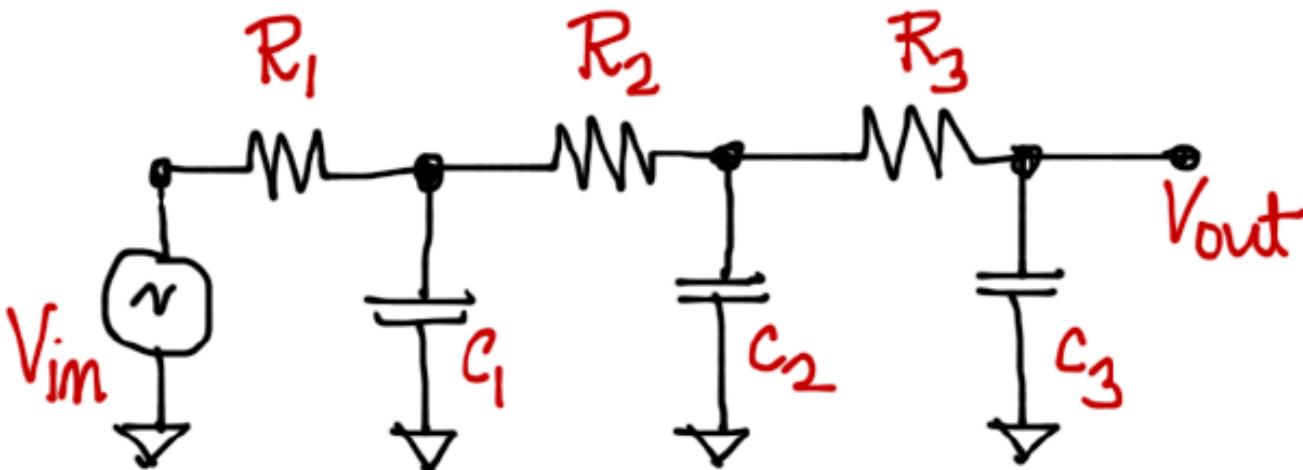


Conceptual Interpretation of Poles and Zeros



Why does this circuit have only one pole and no zero?

Poles are associated with number of internal nodes that needs to be charged in the circuit.

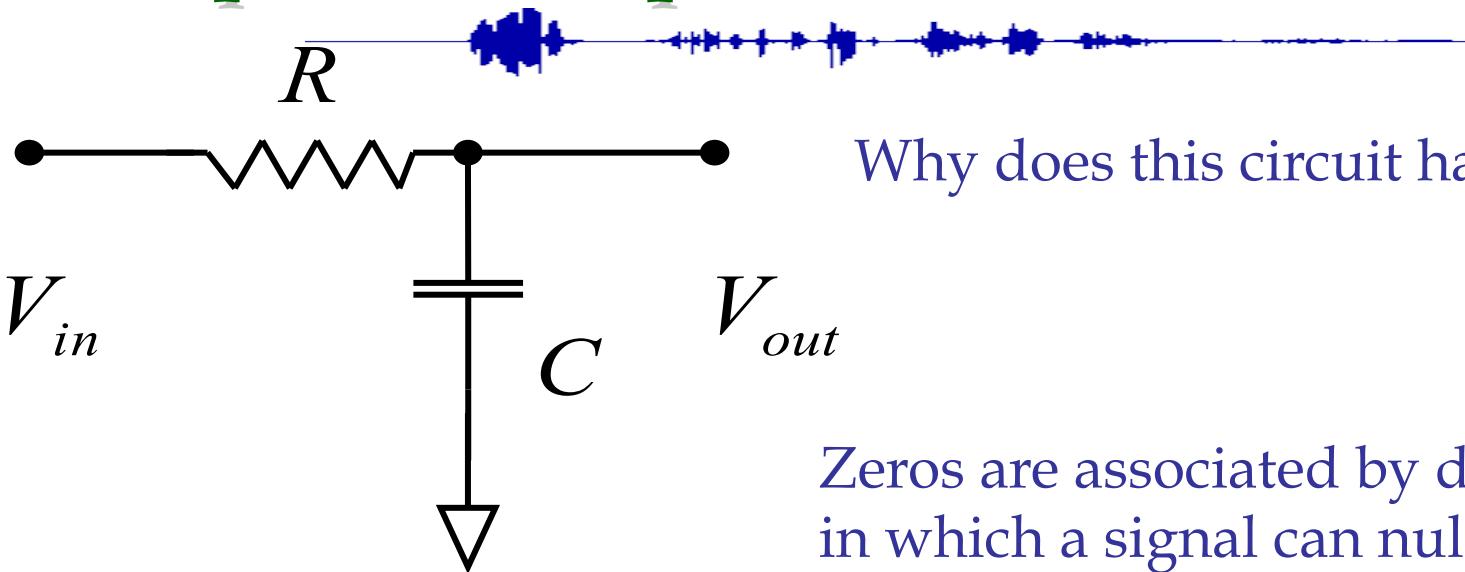


Why does this circuit have three poles?

Three internal nodes.
Still no zeros at $V_{out}!!!$

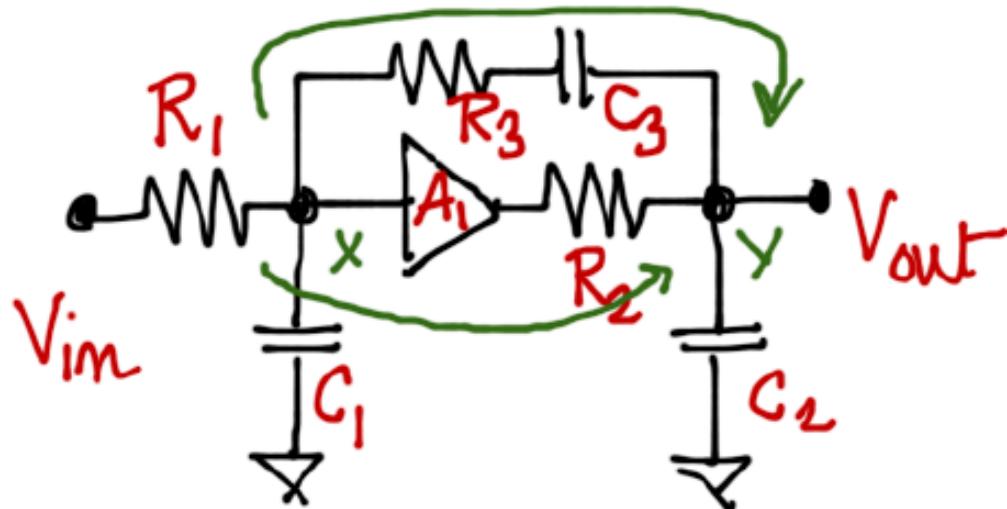


Conceptual Interpretation of Poles and Zeros



Why does this circuit have no zeros ?

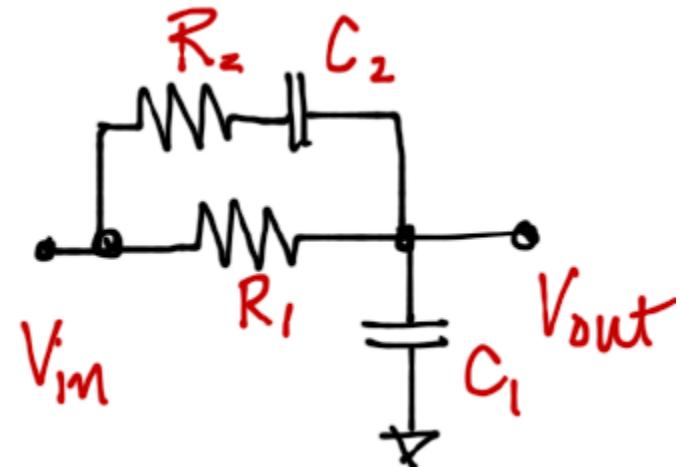
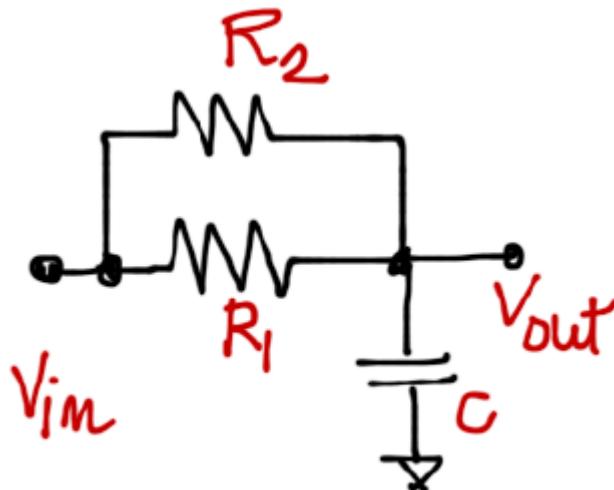
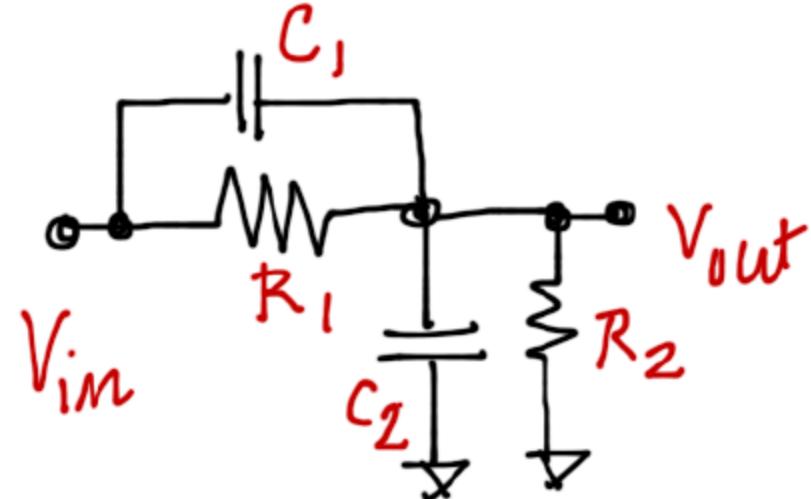
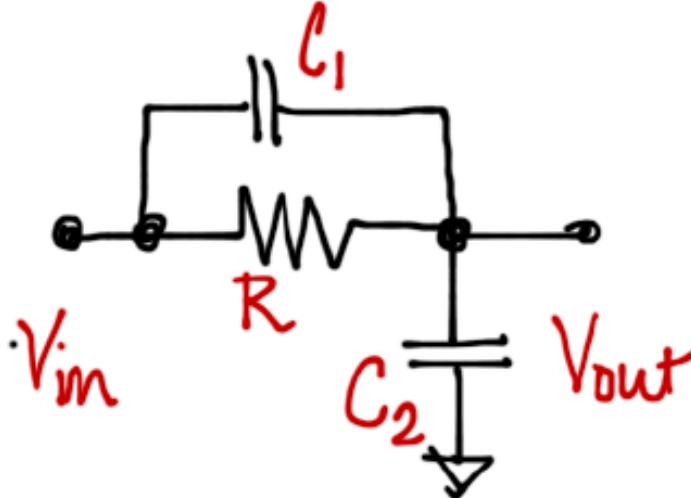
Zeros are associated by different ways in which a signal can nullify itself at the output.



How many zeros would this circuit have ?

One possible way to cancel the signal at the output. Therefore has one zero !!!!

How many poles and zeros ?



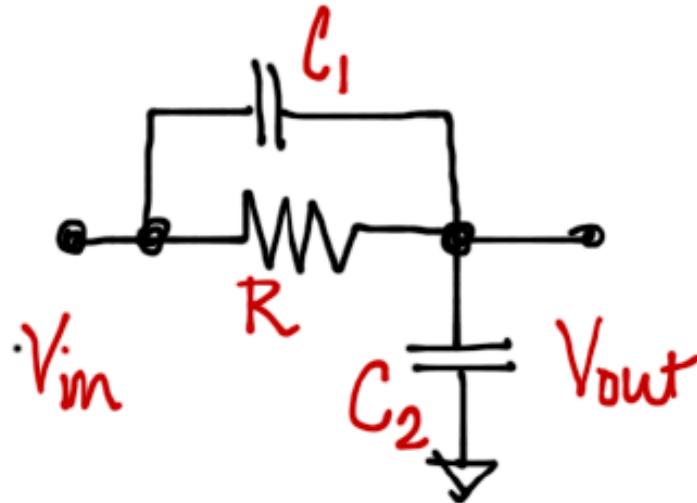
Worksheet



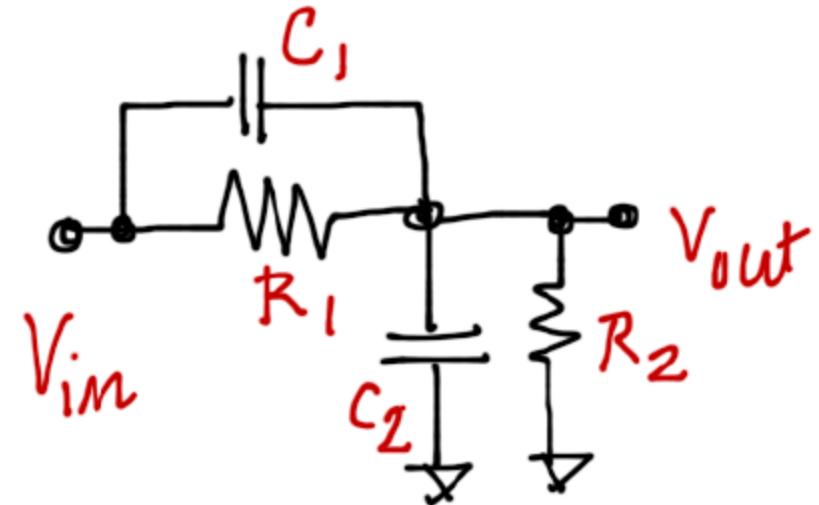
Frequency location of poles and zeros



- Location of the poles is determined by the delay in charging or discharging the internal nodes in the circuit. Worst-case delay determines the bandwidth of the system (frequency is inverse of the delay).
- Location of zeros is determined by frequency at which the signal cancels out at the output.



$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(1 + sRC_1)}{(1 + R[C_1 + C_2]s)}$$



$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1 + R_2} \frac{(1 + sRC_1)}{(1 + [R_1 \parallel R_2][C_1 + C_2]s)}$$

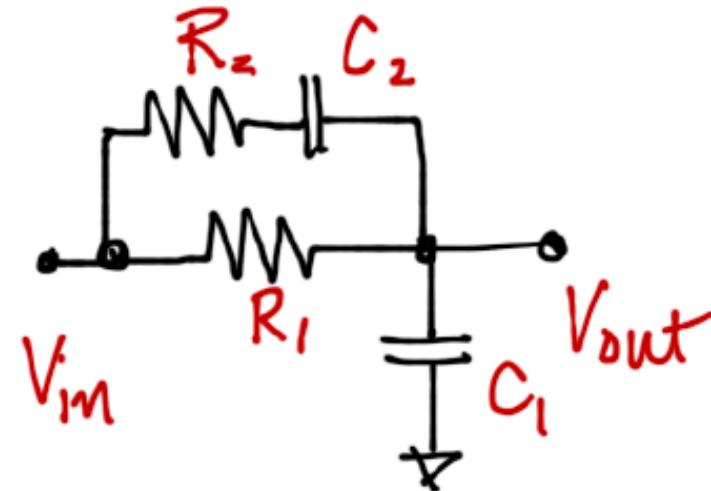
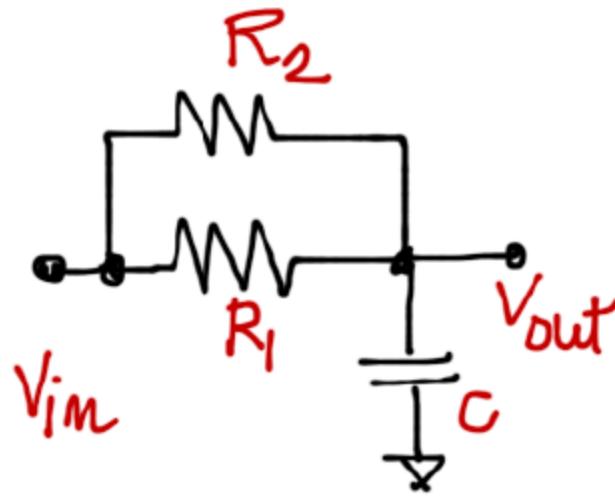
Worksheet



Frequency location of poles and zeros



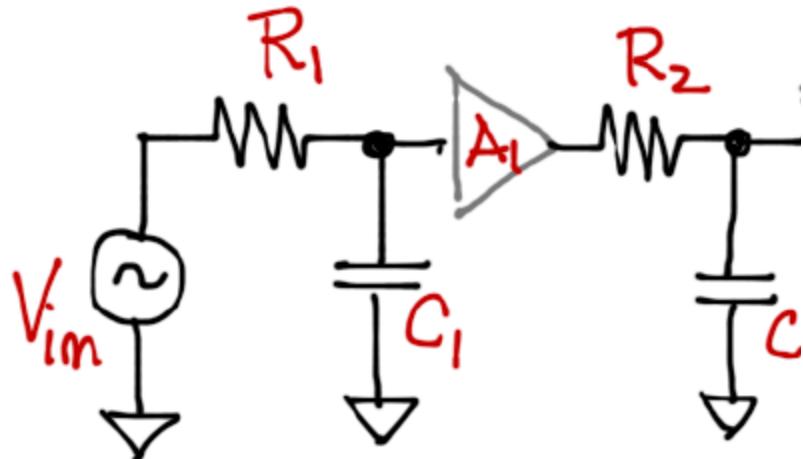
- For an RC network, location of the poles is determined by the RC delay in the circuit.
- For an RC network, the phase delay between two paths determine if a zero is present or not.



Worksheet

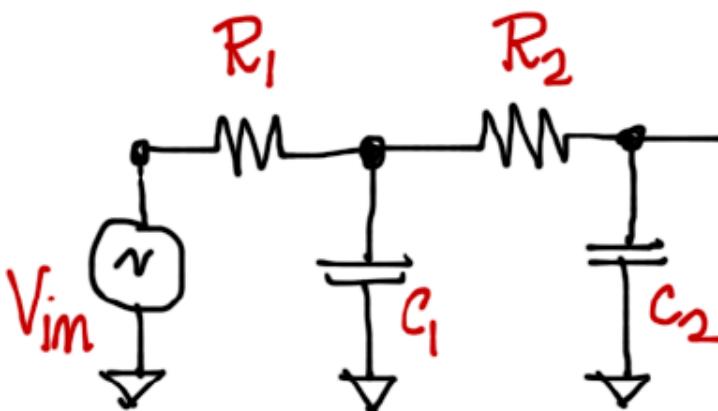


Non-independent Interactive Poles



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(1 + R_1 C_1 s)} \frac{A_1}{(1 + R_2 C s)}$$

- Two poles behave independently of each other.
- Mathematically – Denominator can be factored.
- Non-independent poles occur when poles effect each other.



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(1 + sC_2R_2 + sC_1R_1 + sC_2R_1 + s^2C_1R_1C_2R_2)}$$

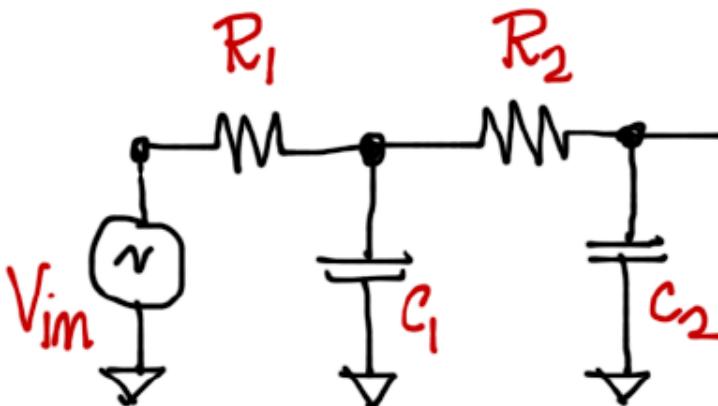


Method of open-circuit time-constants



- Used for determining the high-frequency bandwidth of a system with interactive poles and no zeros.
- For an RC network, the bandwidth (worst-case delay) is determined by the RC delay due to all the poles.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(1 + sC_2R_2 + sC_1R_1 + sC_2R_1 + s^2C_1R_1C_2R_2)}$$



- At low-frequencies the higher order frequency terms can be ignored.

$$H(s) \approx \frac{1}{(1 + sC_2R_2 + sC_1R_1 + sC_2R_1)}$$
$$\omega_1 \approx \frac{1}{(C_2R_2 + C_1R_1 + C_2R_1)}$$

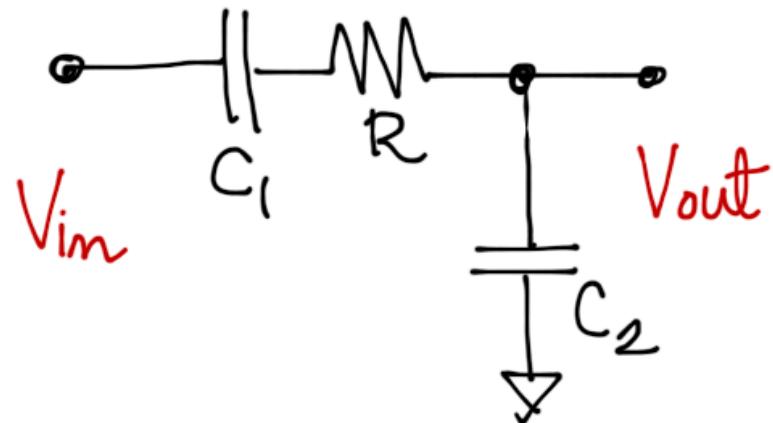
Bandwidth Estimation



- For a given capacitor (ignore all other capacitors) – check which resistances charge up the capacitor.
- For each of the resistance compute the RC delay and add them up.
- Repeat procedure 1 and 2 for all other capacitors and add them up to the total RC delay.
- The inverse of the RC delay will give you the approximate bandwidth.



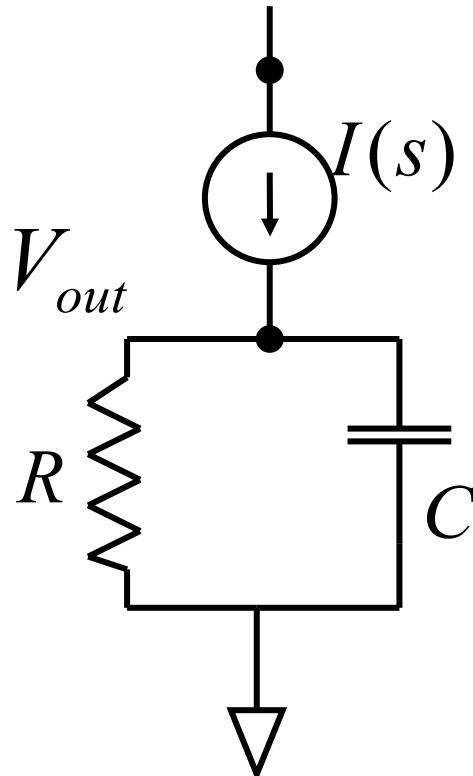
Caveats: How many poles and zeros ?



Location of Poles and Zeros



Frequency analysis of most analog circuit can be mapped onto three basic topologies.



$$V_{out}(s) = \frac{RI(s)}{(1 + RCs)}$$

A current source charging a parallel combination of resistance and capacitance leads to a pole.

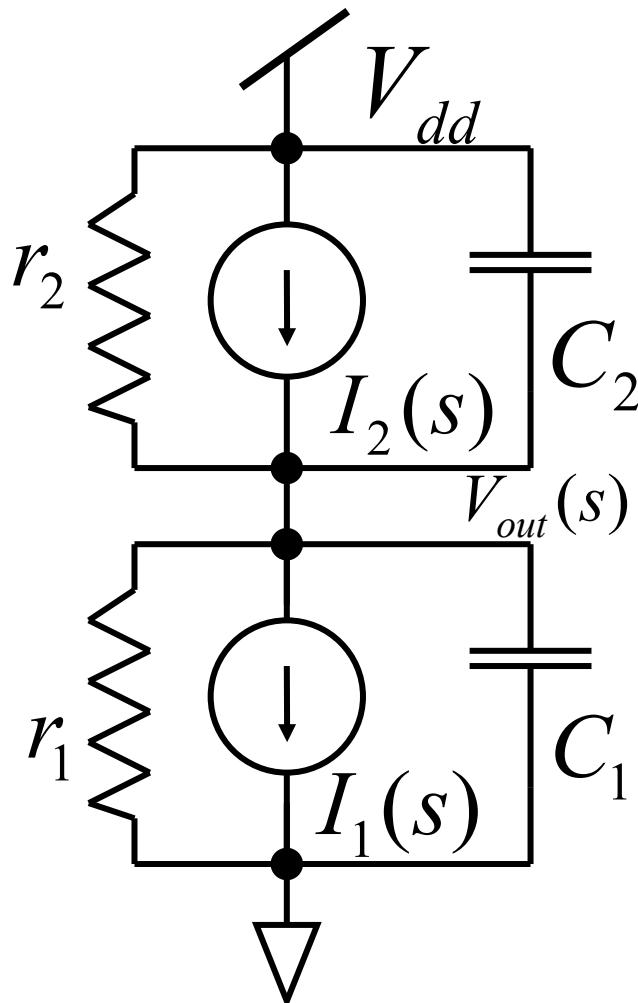
Location of the pole is dependent on R and C.

$$s = -\frac{1}{RC}$$
$$\omega_p = \frac{1}{RC}$$

This is equivalent to frequency



AC Equivalent Circuit of an Amplifier



$$V_{out}(s) = \frac{(r_1 \parallel r_2)[I_2(s) - I_1(s)]}{(1 + (r_1 \parallel r_2)(C_1 + C_2)s)}$$

The output voltage is dependent on the difference of the two currents.

The location of the pole is dependent on the total resistance at the output node and total capacitance at the output node.

$$s = -\frac{1}{(r_1 \parallel r_2)(C_1 + C_2)}$$

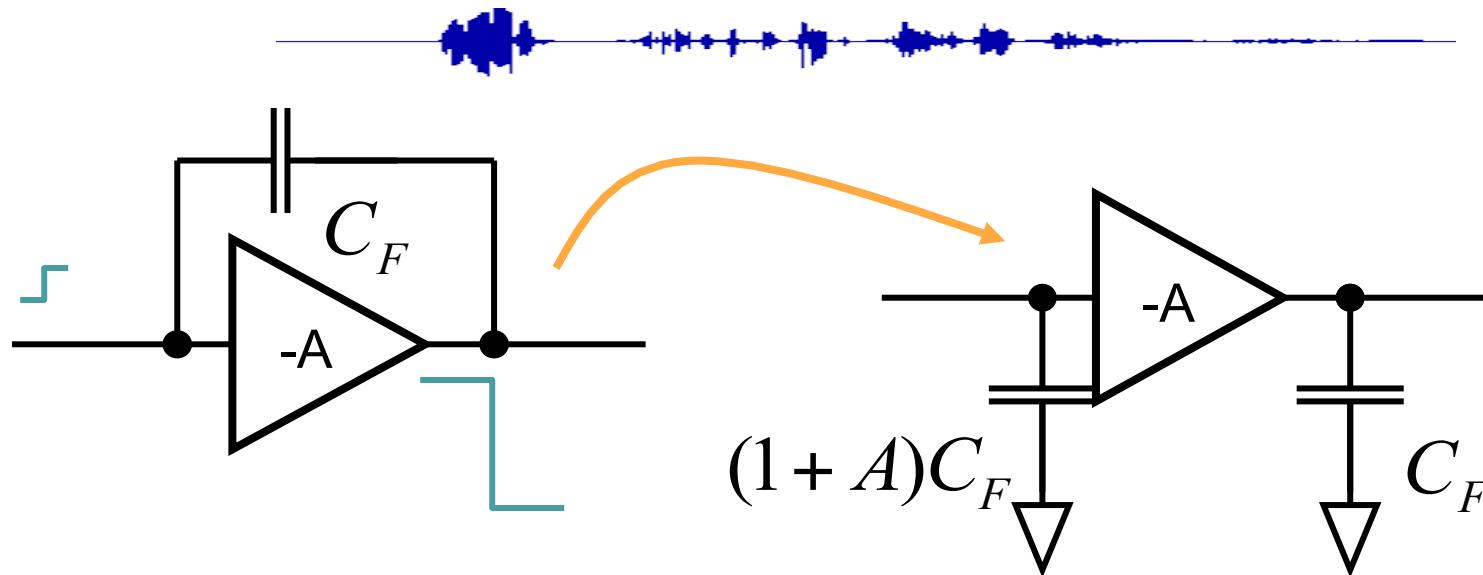
$I_1(s) = I_2(s)$ leads to a zero.



Worksheet



Miller Theorem



A capacitor across an inverting amplifier can be decomposed into two capacitors.

The input capacitance gets amplified by the gain of the amplifier. The output capacitance remains unchanged. Makes it easy to calculate the location of the poles.

Only an approximation ! Ignores the zero introduced due to the feedback capacitor.



Worksheet



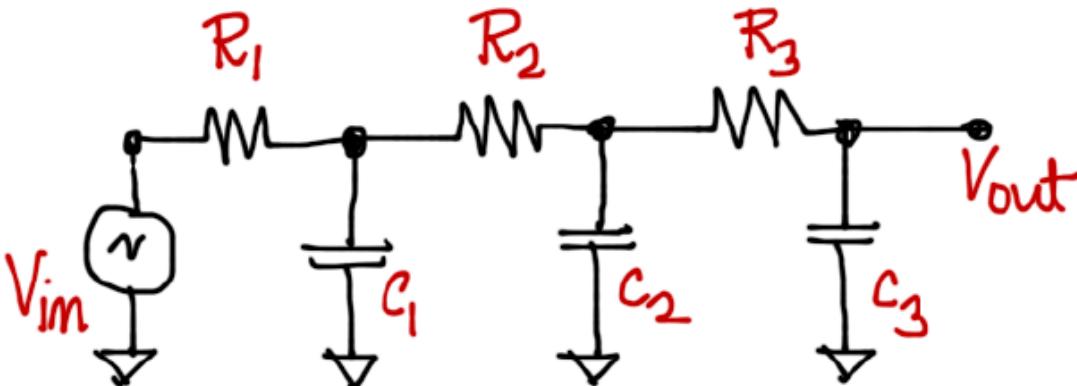
Conceptual Interpretation of Poles and Zeros



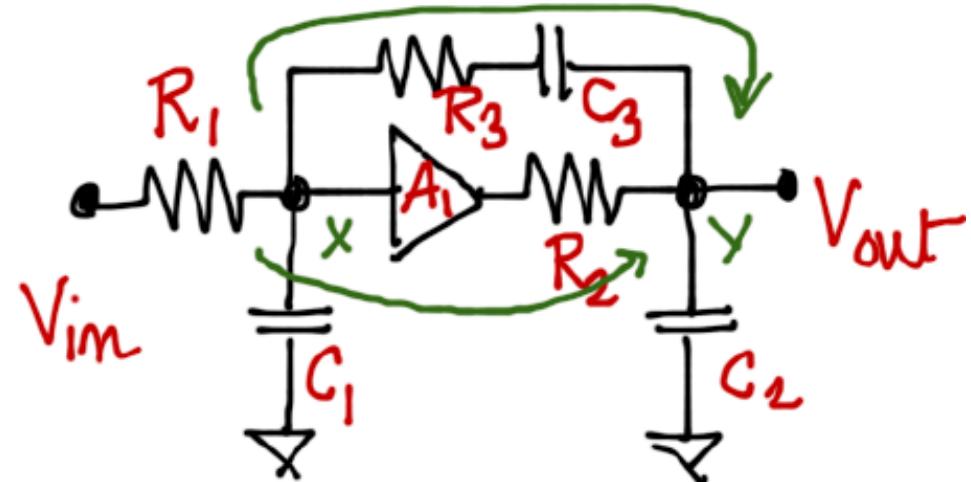
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Zeros are associated by different ways in which a signal can nullify itself at the output.

This circuit has three poles.



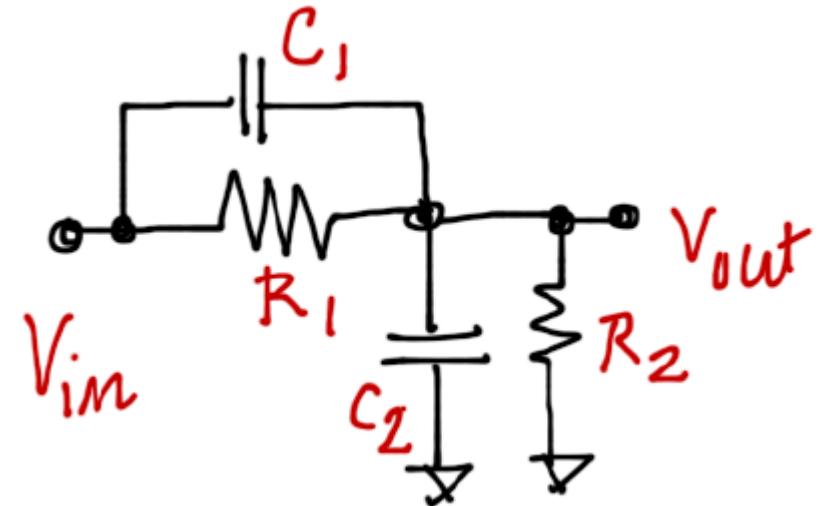
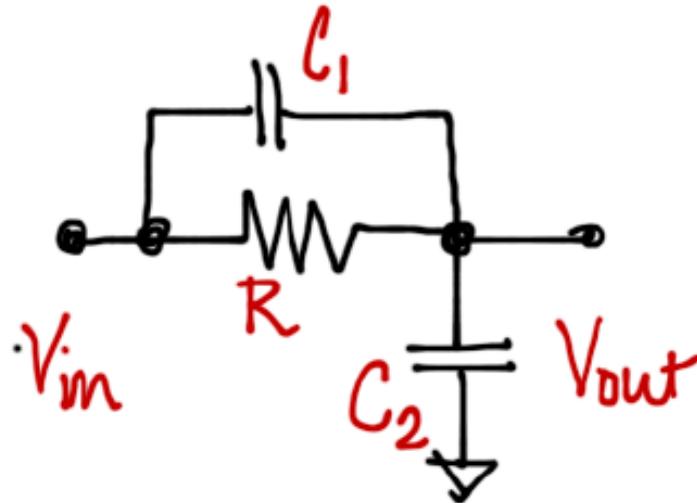
This circuit has one zero.



Frequency location of poles and zeros



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- Location of zeros is determined by frequency at which the signal cancels out at the output.

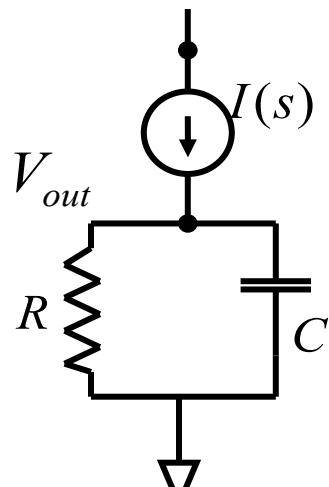


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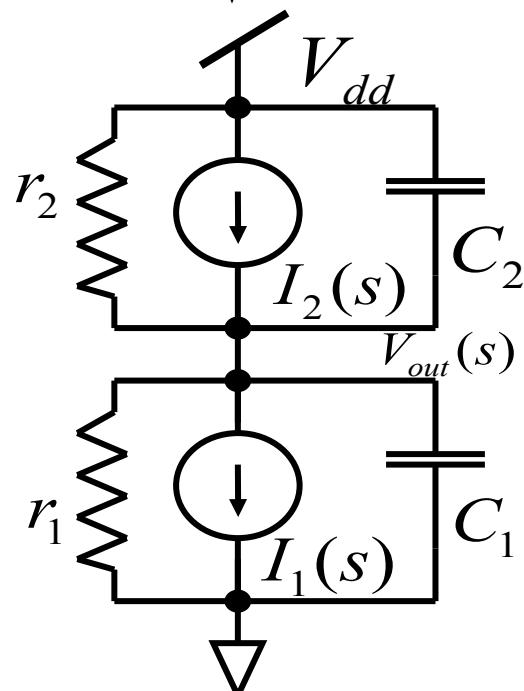


Important Concepts for Amplifier Analysis

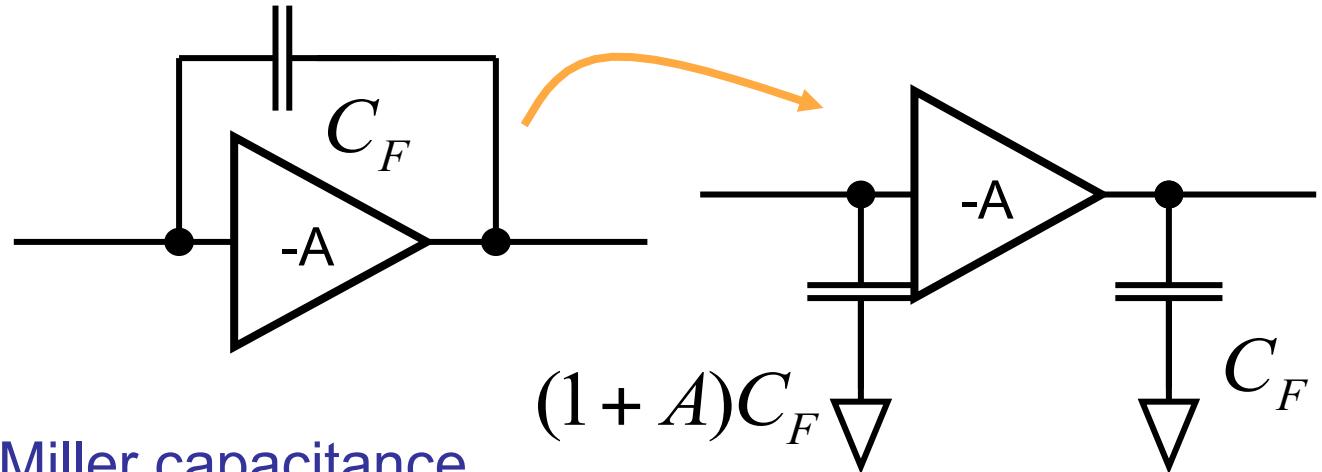


$$V_{out}(s) = \frac{RI(s)}{(1 + RCs)}$$

A current source charging a parallel combination of resistance and capacitance leads to a pole.



$$V_{out}(s) = \frac{(r_1 \parallel r_2)[I_2(s) - I_1(s)]}{(1 + (r_1 \parallel r_2)(C_1 + C_2)s)} \quad \text{Topology leads to a pole and a zero.}$$

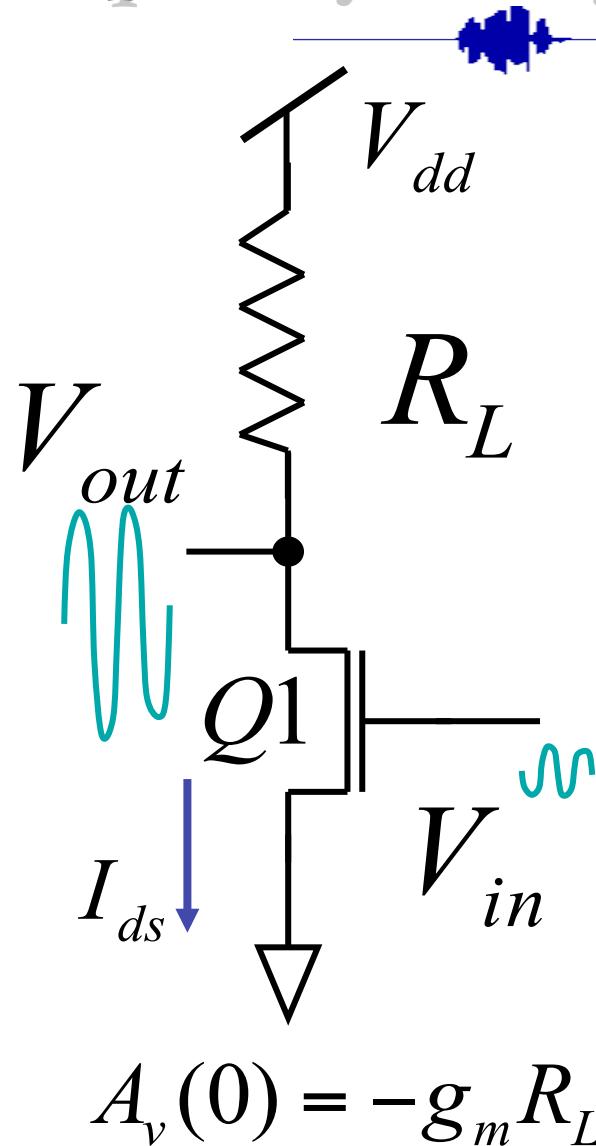


Miller capacitance

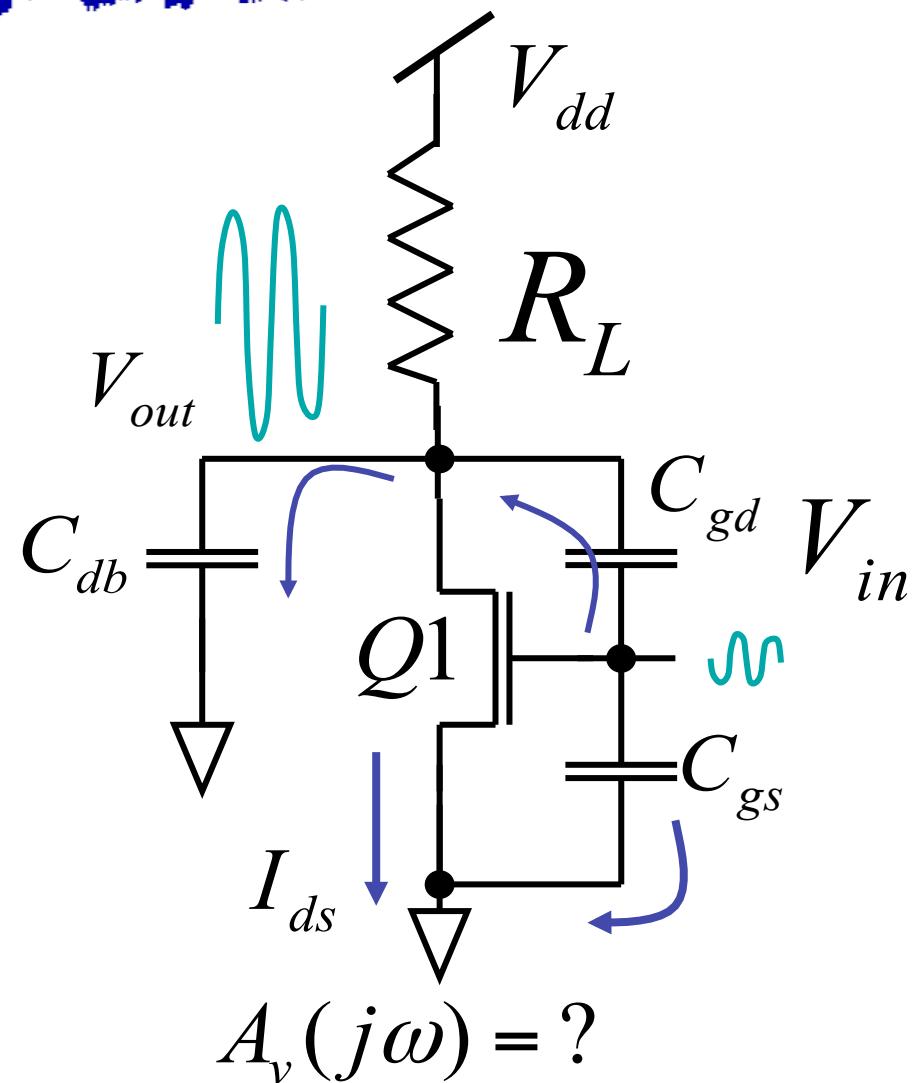
$$(1 + A)C_F$$

$$C_F$$

Frequency Analysis of Common Source Amp.



In previous analysis current can not flow into the gate.



Analysis complicated by the gate current.

Conceptual solution of poles and zeros



Miller capacitance due to C_{gd} and capacitance C_{gs} in parallel

$$C_{Vx} = (1 - A)C_{gd} + C_{gs}$$

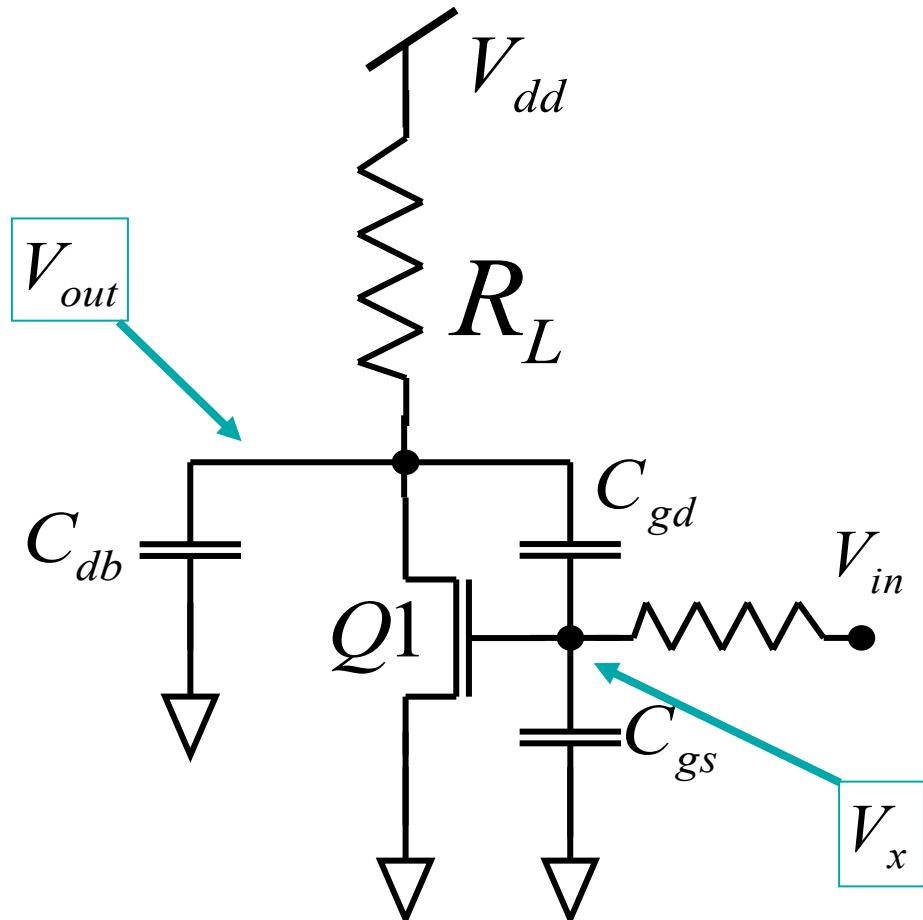
Where A is the gain of the amplifier.

$$C_{Vx} = (1 + g_m R_L)C_{gd} + C_{gs}$$

Resistance at node V_x is R_{in}

Location of the pole at V_x

$$\omega_{p1} = \frac{1}{R_{in}[(1 + g_m R_L)C_{gd} + C_{gs}]}$$



Conceptual solution of poles and zeros



Calculate the impedance at the output node
 (REMEMBER: for calculation you have to keep the input terminal constant!).

Capacitance at the output node

$$C_{out} = C_{db} + \frac{C_{gd}C_{gs}}{C_{gd} + C_{gs}}$$

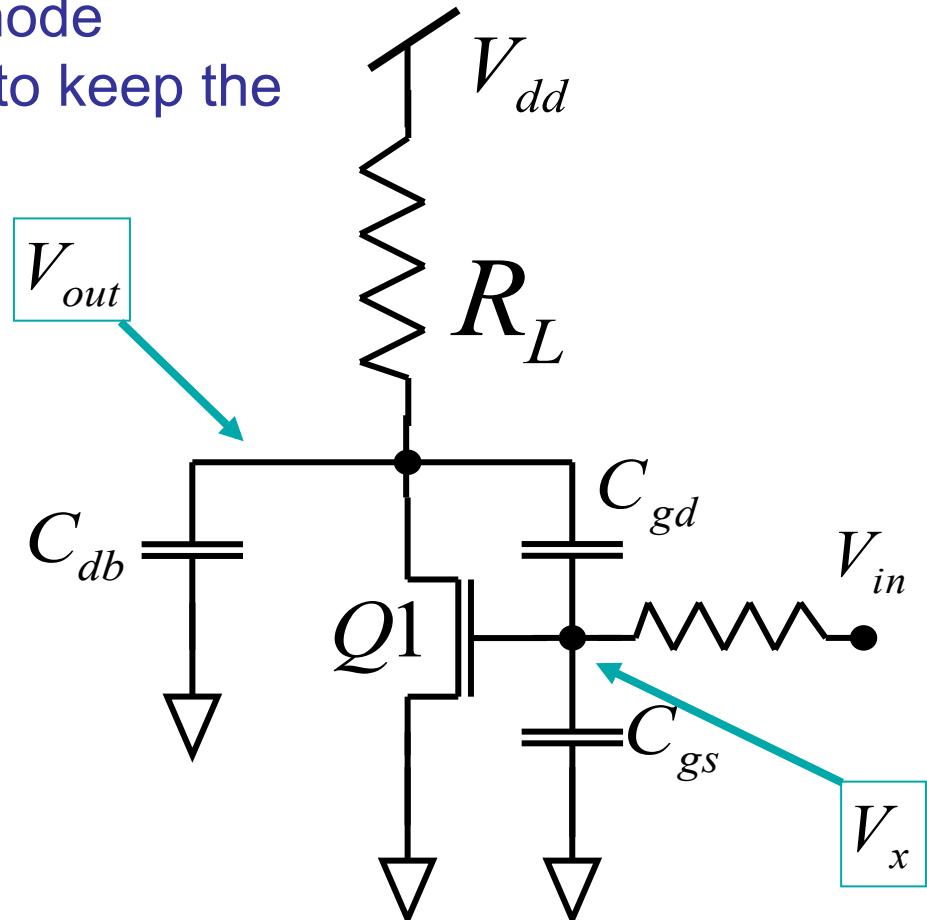
Calculate the RESISTANCE at the output node.

$$\Delta I_{out} = \frac{1}{R_I} \Delta V_{out} + g_m \frac{C_{gd}}{C_{gd} + C_{gs}} \Delta V_{out}$$

$$R_{out} = R_L \parallel \frac{C_{gd} + C_{gs}}{g_m C_{gd}}$$

Location of the output pole

$$\omega_{p2} = \frac{1}{R_{out} C_{out}}$$



Conceptual solution of poles and zeros



To calculate the zeros of the circuit find the paths converging at the output node

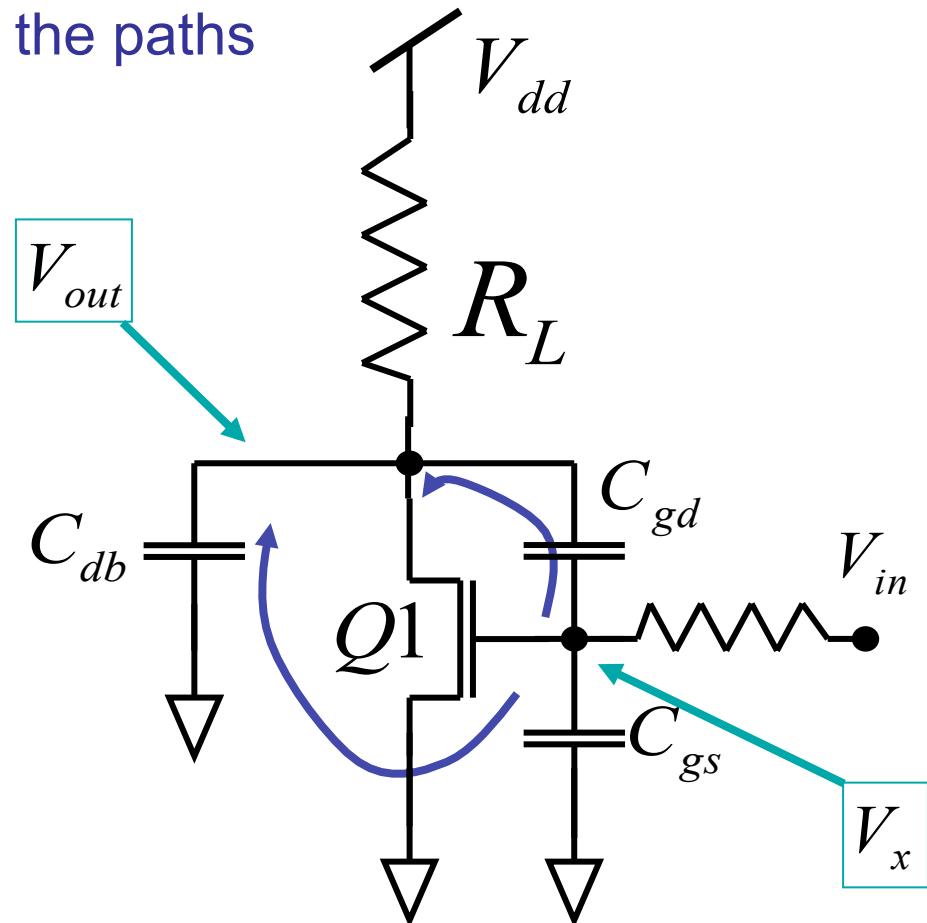
At the zero, the output voltage is = 0.

That is possible if the currents through alternate paths cancel

$$g_m V_x = sC_{gd} V_x$$

Location of the zero

$$s = \frac{g_m}{C_{gd}}$$



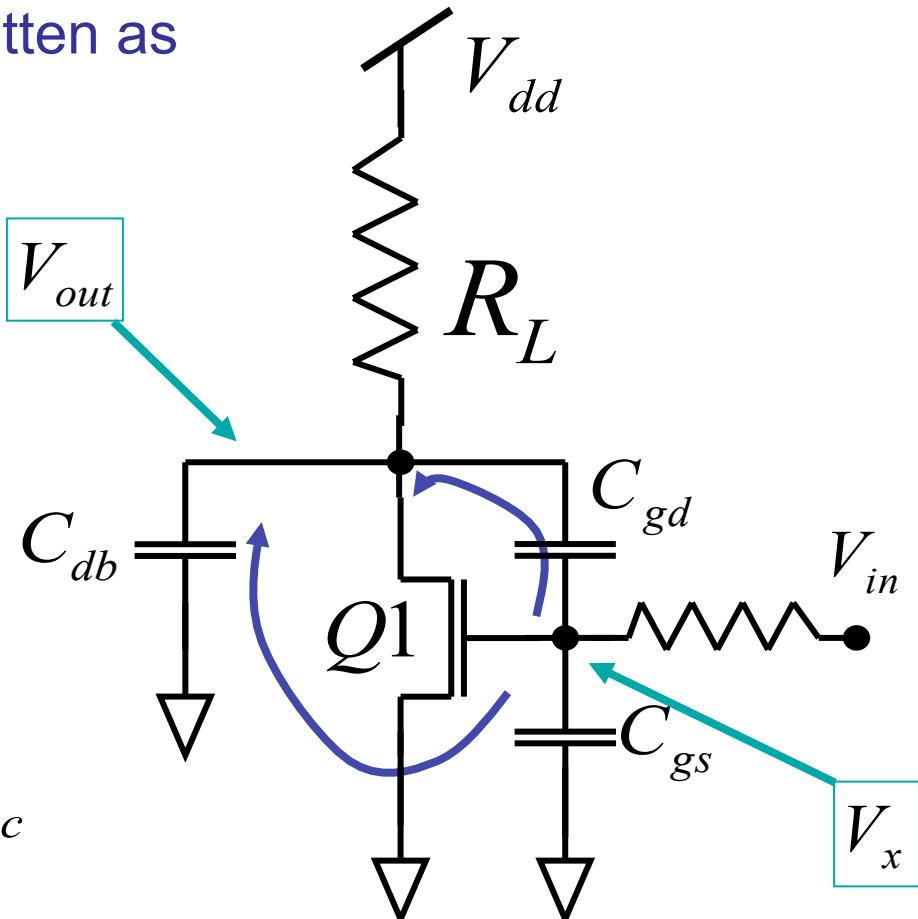
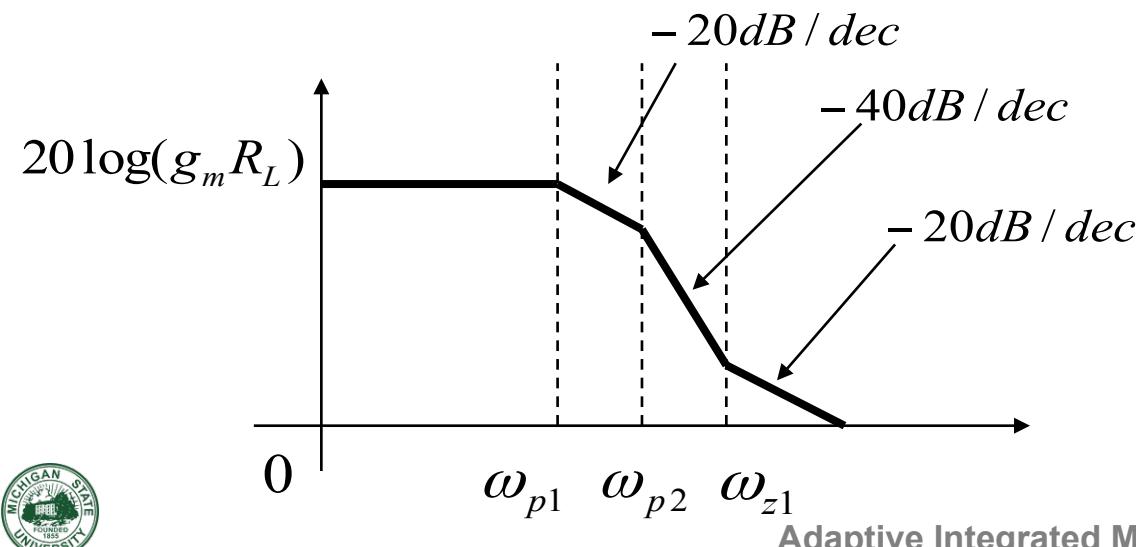
Conceptual solution of poles and zeros



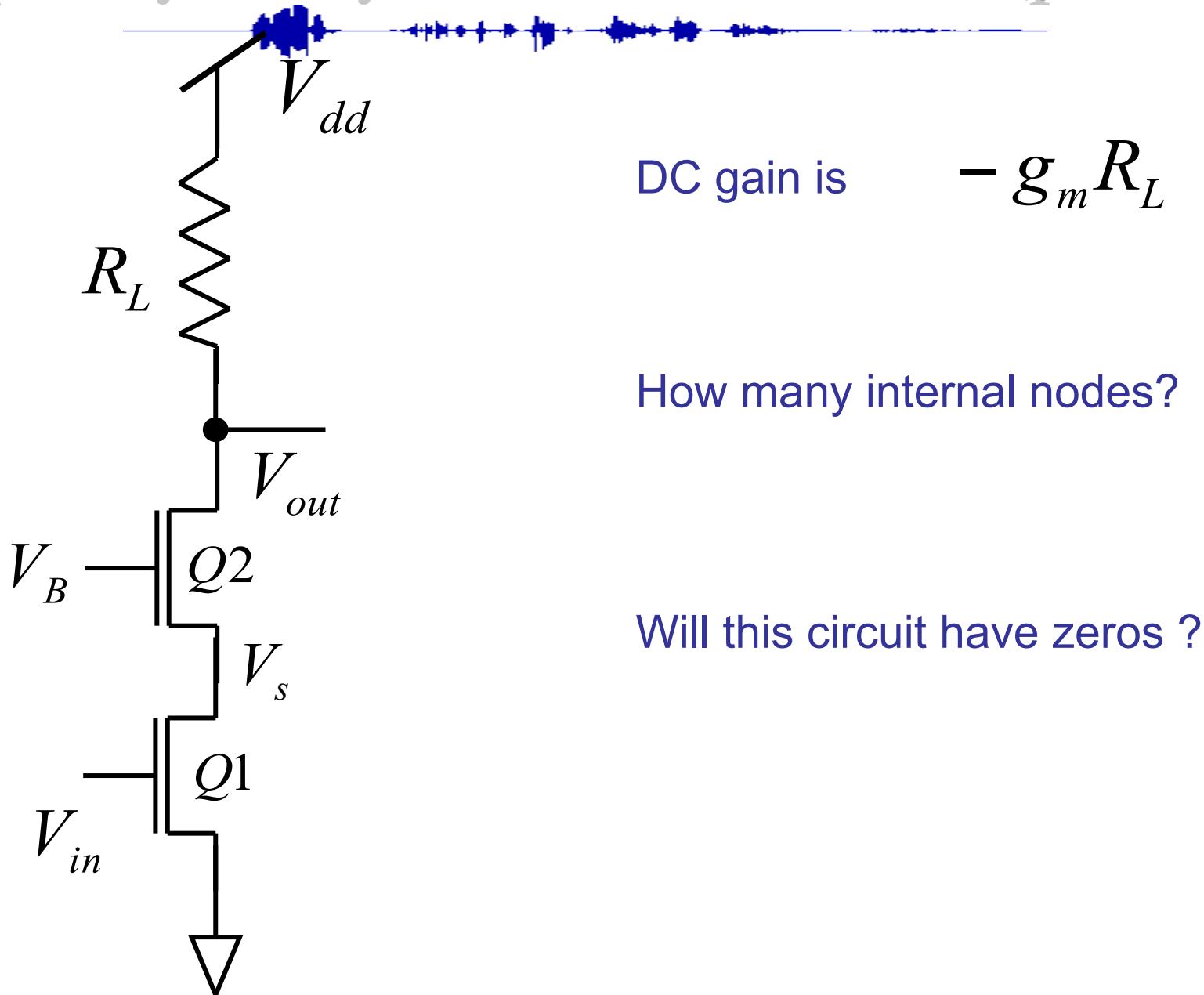
The system transfer function can be written as

$$\frac{V_{out}(s)}{V_{in}(s)} = -g_m R_L \frac{(1 - \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

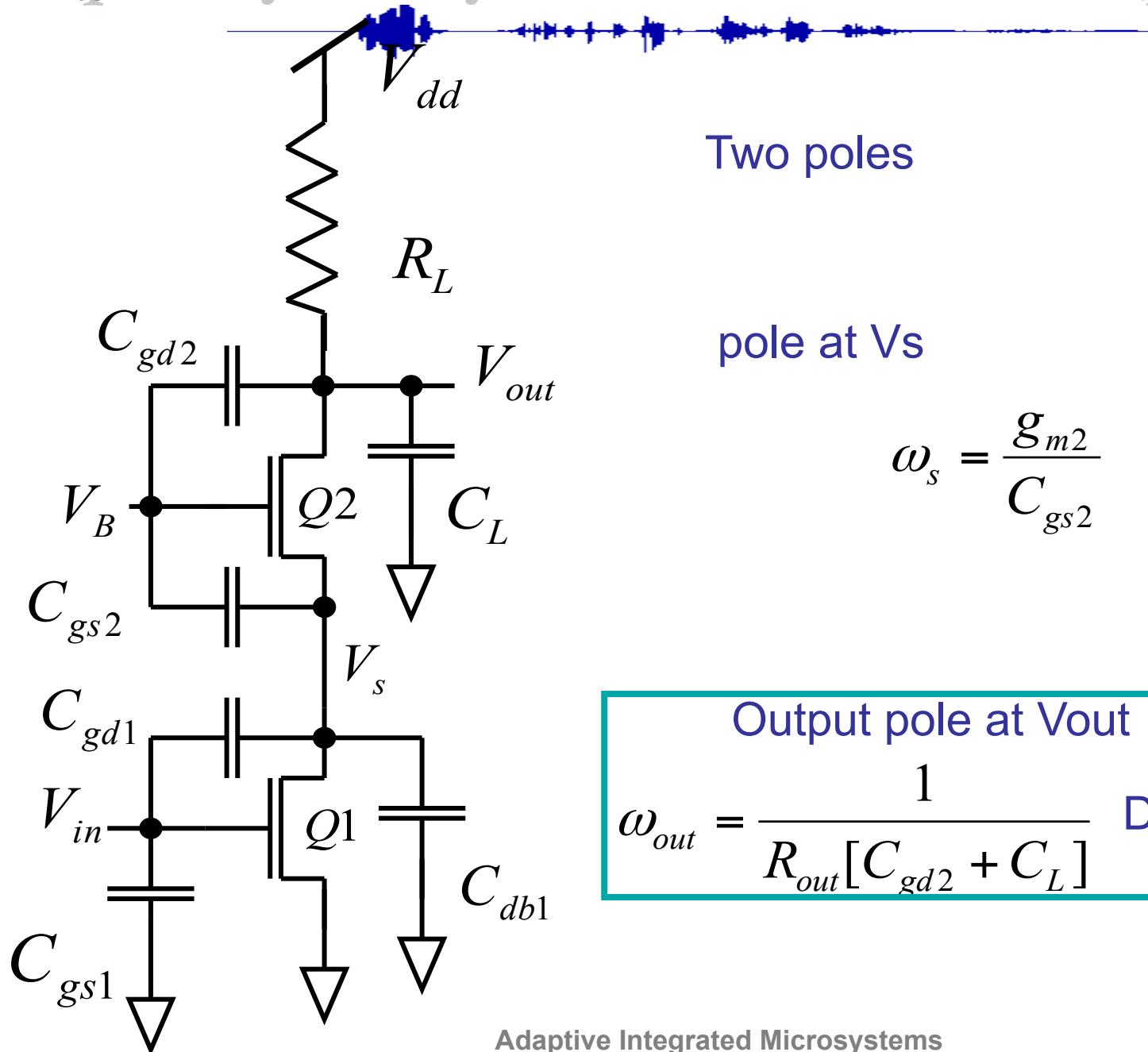
↑
DC gain



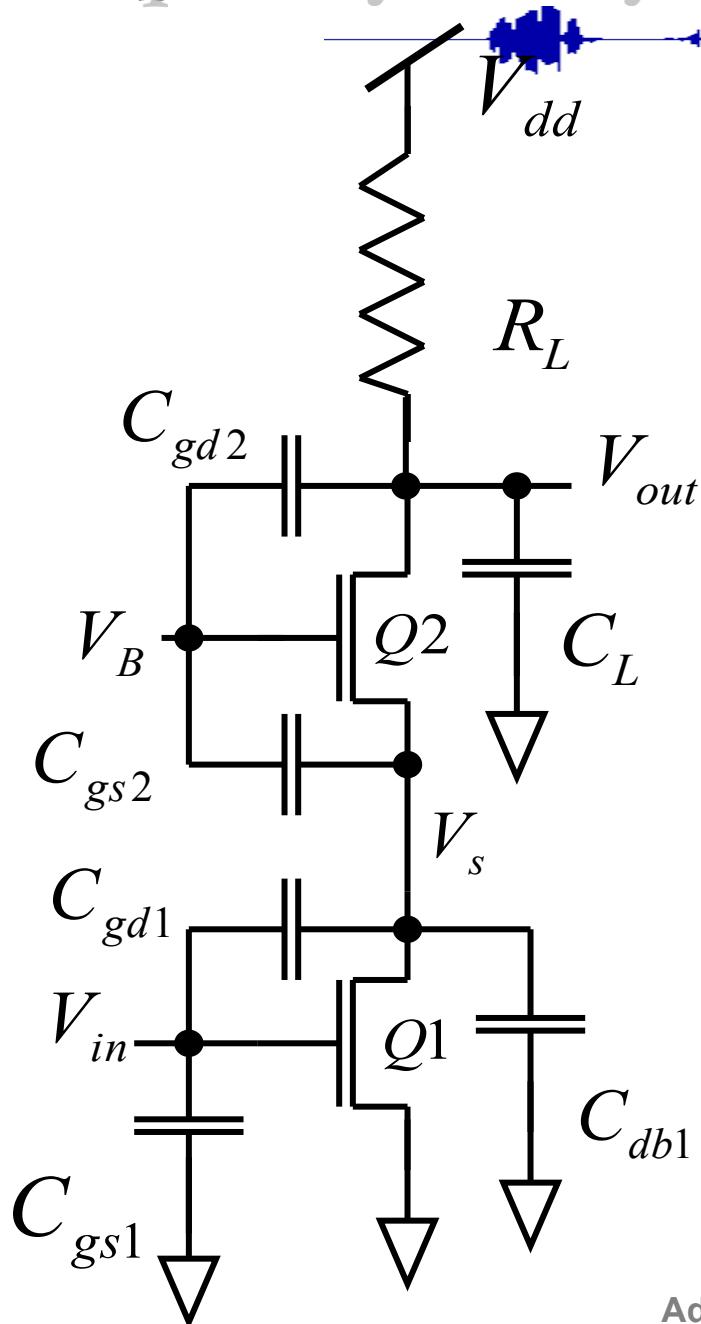
Frequency Analysis of Cascoded Amplifier



Frequency Analysis of Cascoded Amplifier



Frequency Analysis of Cascoded Amplifier



Bandwidth is determined by the dominant pole.

$$\omega_{out} = \frac{1}{R_{out}[C_{gd2} + C_L]} \quad \text{Dominant pole}$$

$$R_{out} = R_L$$

Very high output impedance and high output capacitance implies large time-constants and hence reduces the speed of the amplifier.

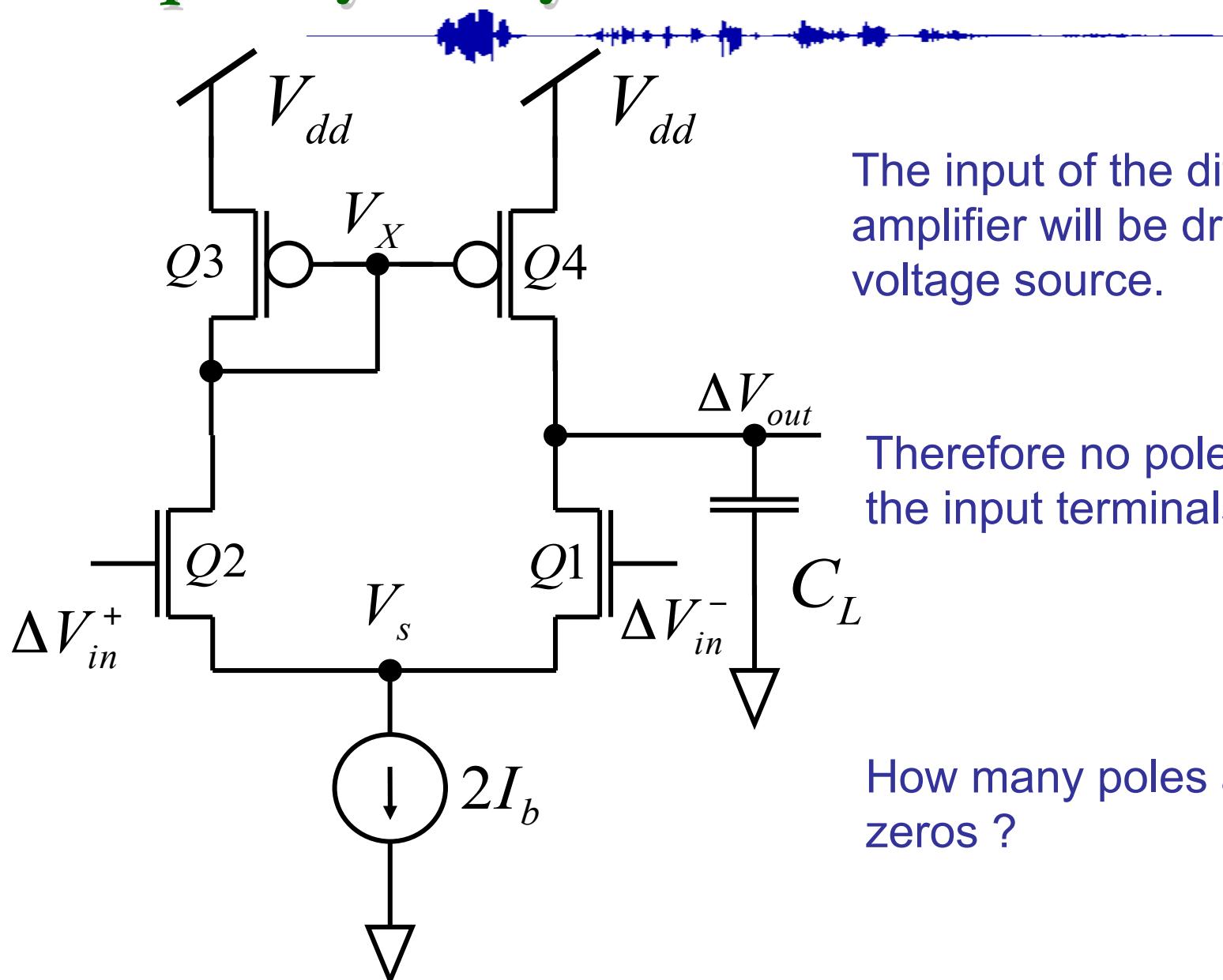
Design of amplifier implies controlling the location of poles to match speed-gain specification.

Increased gain leads to decreased speed/bandwidth.

Worksheet



Frequency Analysis of Differential Amplifiers

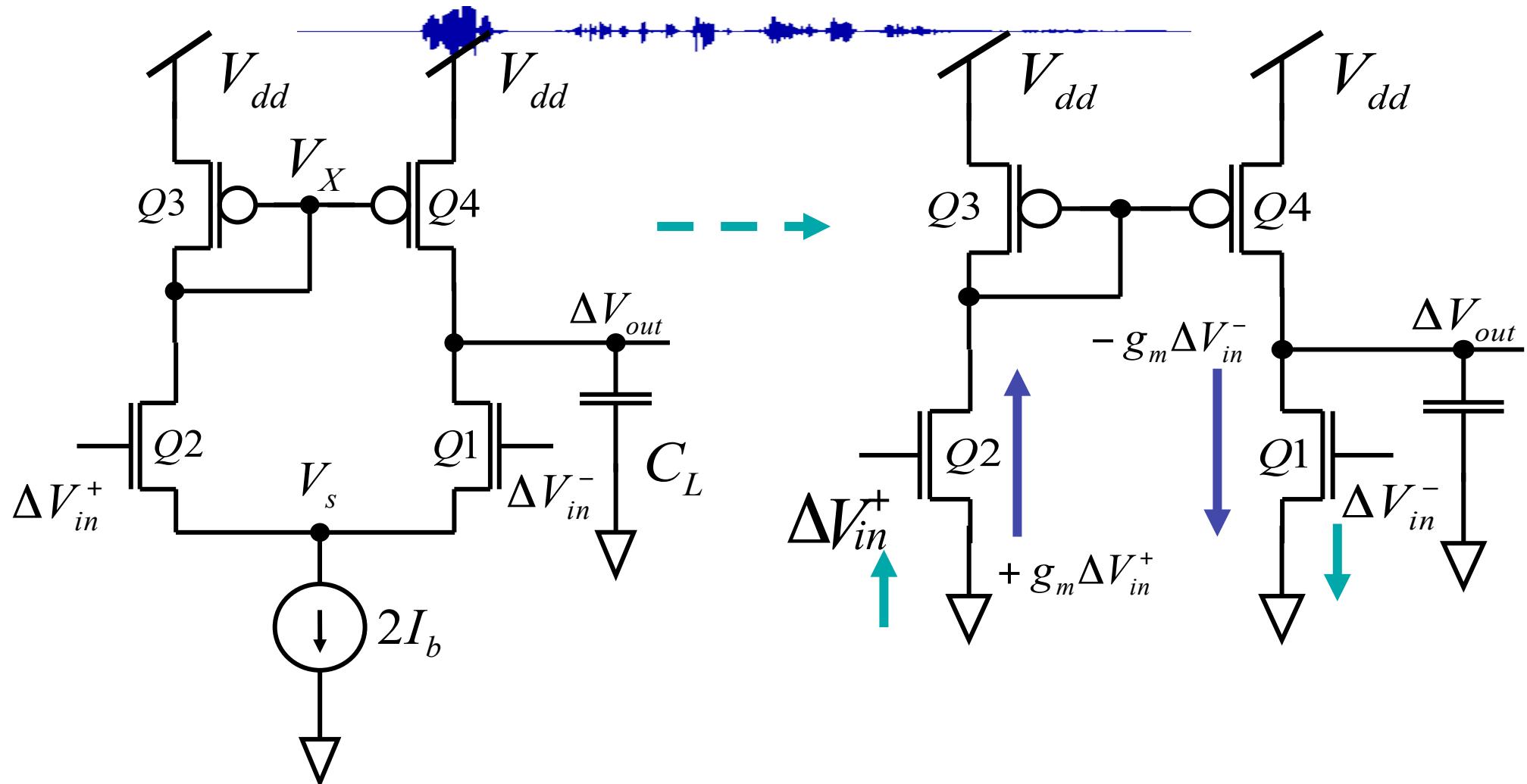


The input of the differential amplifier will be driven by an ideal voltage source.

Therefore no poles associated with the input terminals.

How many poles and how many zeros ?

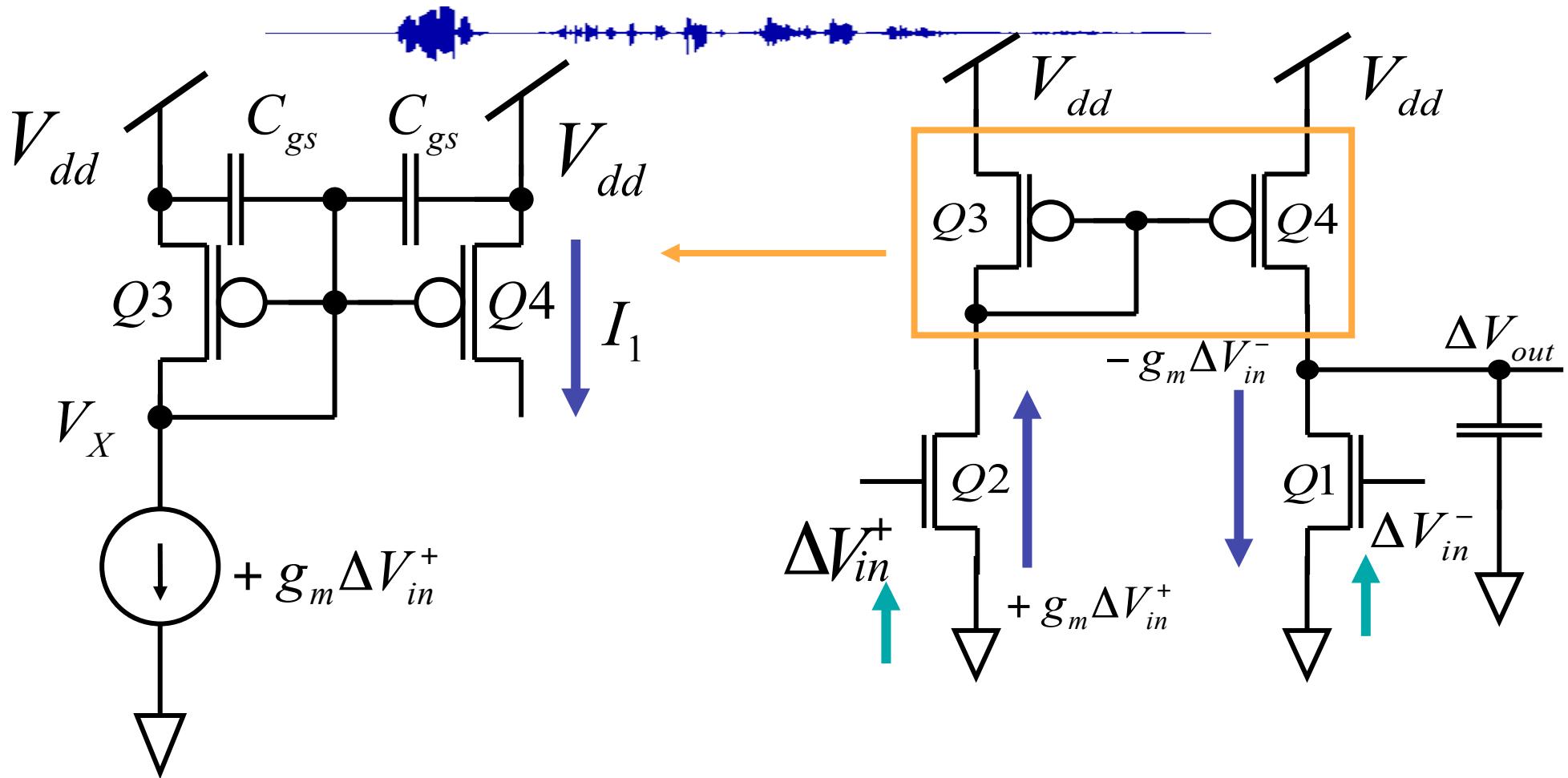
Location of Poles and Zeros



Use symmetry at node V_s

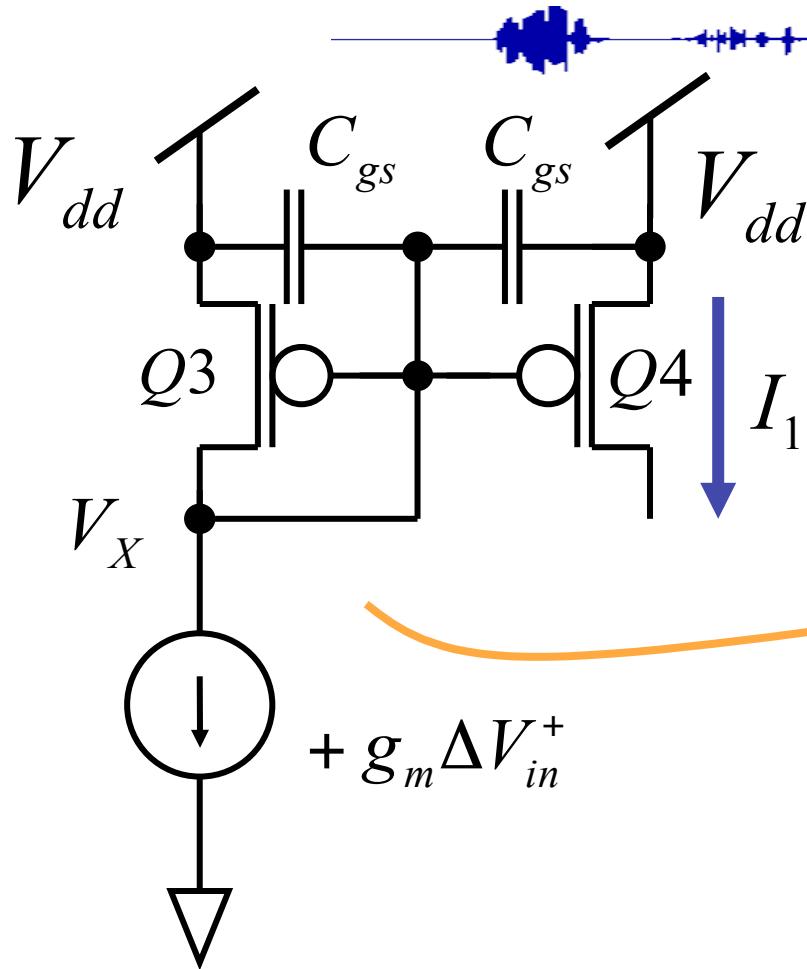
Remember we assumed that input voltage sources are ideal which means that input voltage changes instantaneously.

Location of Poles and Zeros

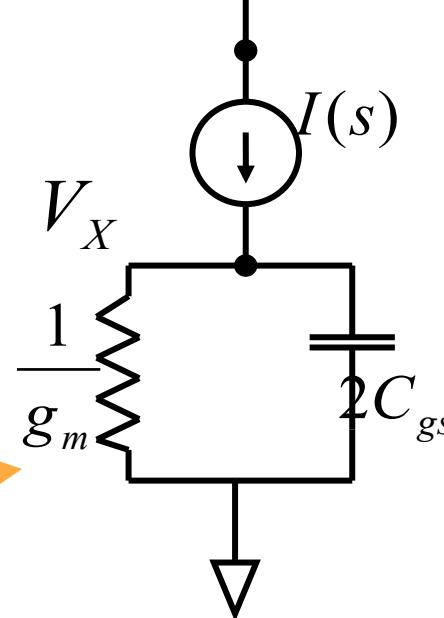


The change in current charges the capacitor through the resistance seen at node V_x . The voltage V_x decreases. Q4 transforms the change in V_x into an output current I_1 .

Pole due to Current Mirrors



$$+ g_m \Delta V_{in}^+$$



$$V_X(s) = -\frac{\frac{1}{g_m} I(s)}{(1 + \frac{2C_{gs}}{g_m} s)}$$

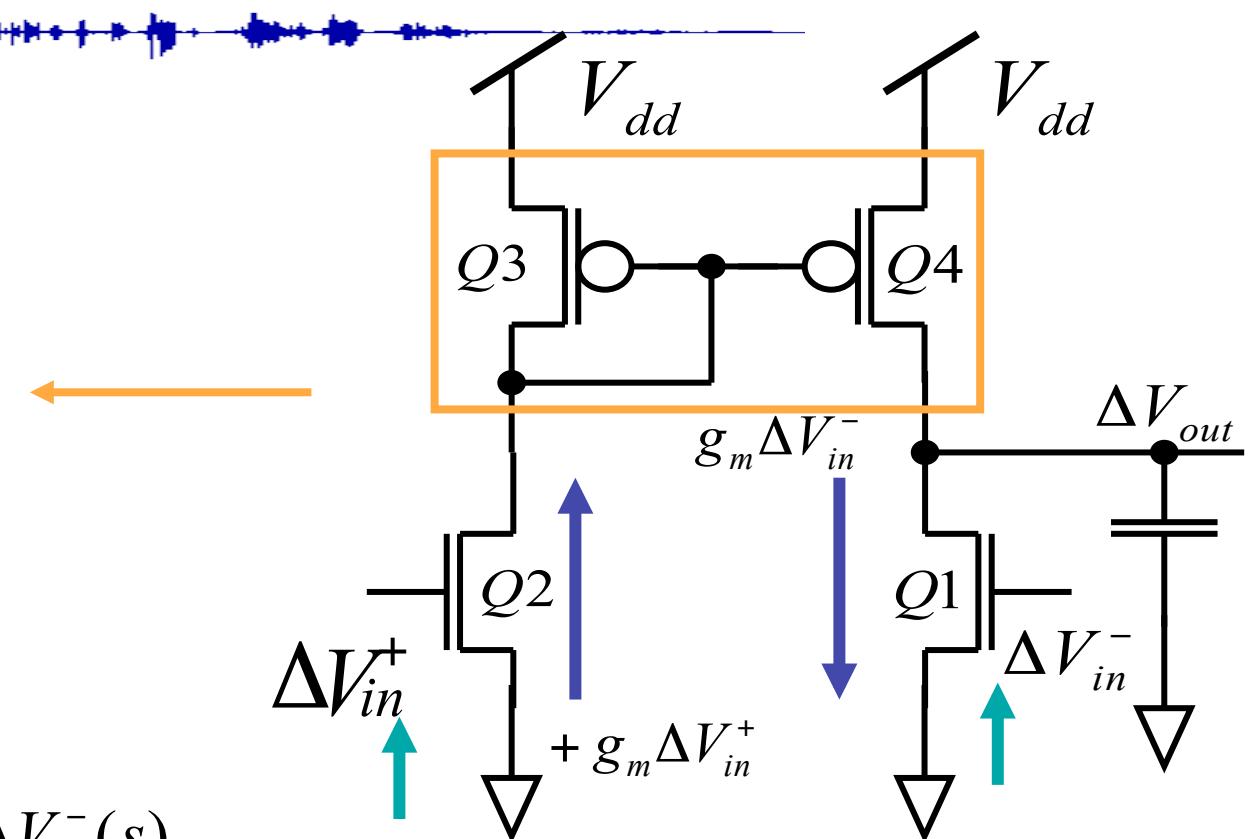
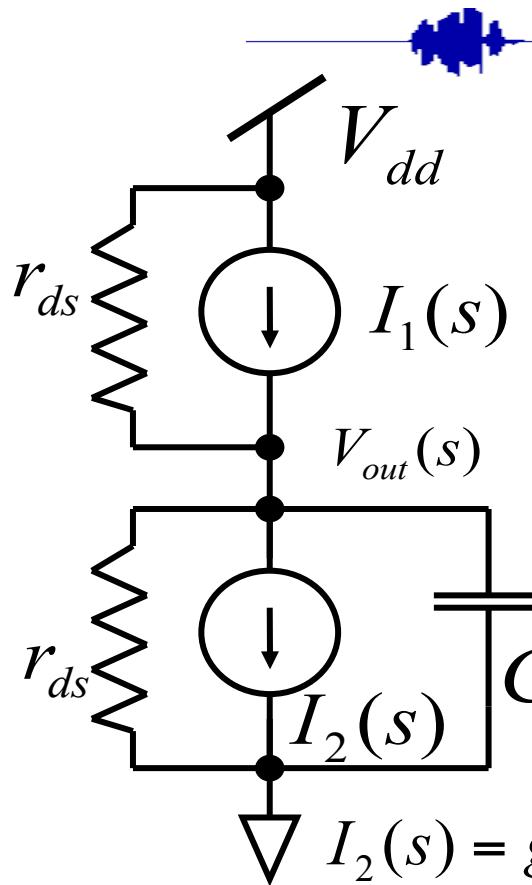
The voltage V_X changes slowly and leads to a pole.

$$I_1(s) = -g_m \Delta V_X(s)$$

$$I_1(s) = \frac{I(s)}{\left(1 + \frac{2C_{gs}}{g_m}\right)} \quad \text{Mirror pole}$$



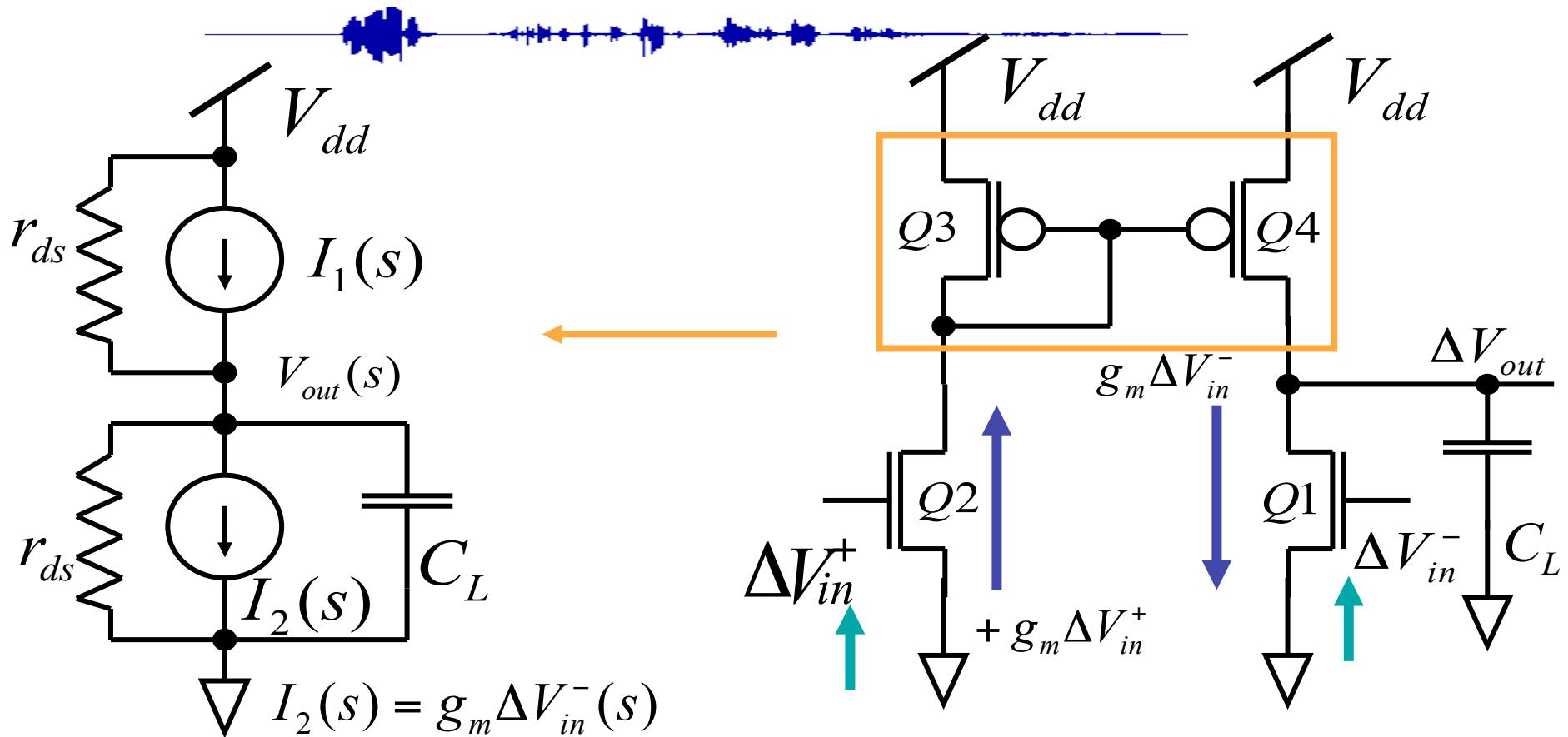
Location of Poles and Zeros



Two time varying currents are compared at the output node and the difference in current flows through load capacitor and the load resistor.



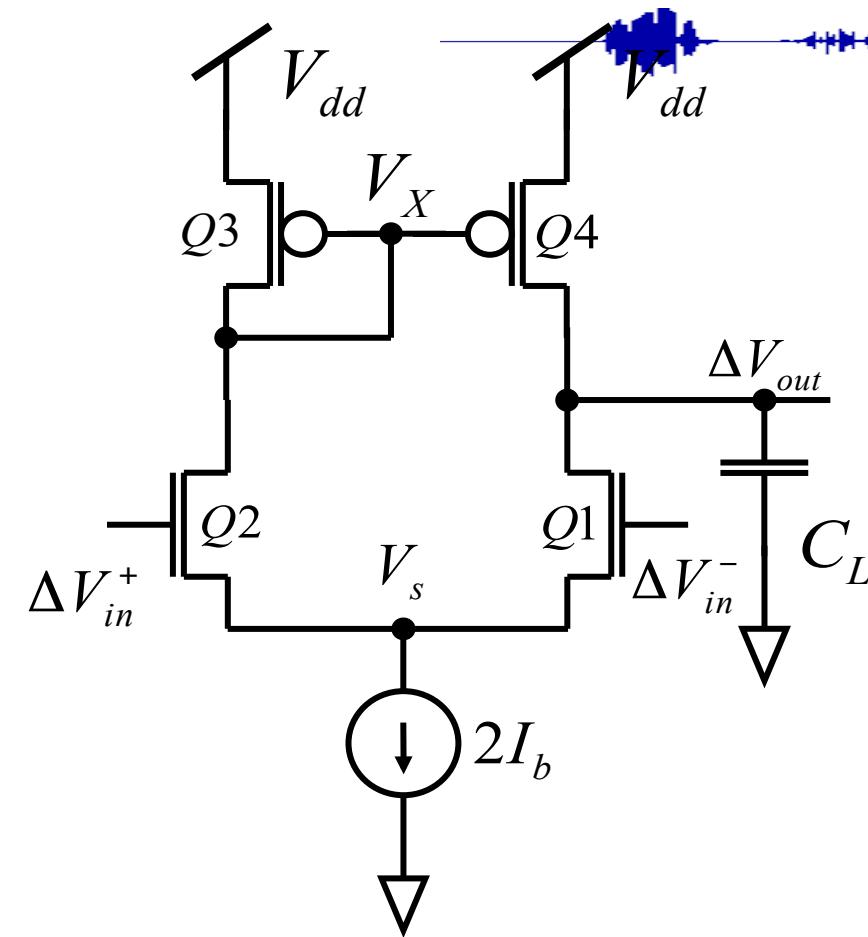
Location of Poles and Zeros



$$V_{out}(s) = \frac{(r_{ds} \parallel r_{ds})[I_2(s) - I_1(s)]}{(1 + (r_{ds} \parallel r_{ds})C_L s)}$$

$$\Delta V_{in}^+(s) = \Delta V(s) \quad \& \quad \Delta V_{in}^-(s) = -\Delta V(s)$$

Location of Poles and Zeros



$$\frac{V_{out}(s)}{2\Delta V(s)} = \frac{g_m(r_{ds} \parallel r_{ds})(2 + \frac{2C_{gs}}{g_m}s)}{2(1 + (r_{ds} \parallel r_{ds})C_Ls)(1 + \frac{2C_{gs}}{g_m}s)}$$

Two poles and one zero.

Poles due to output node and due to mirror.

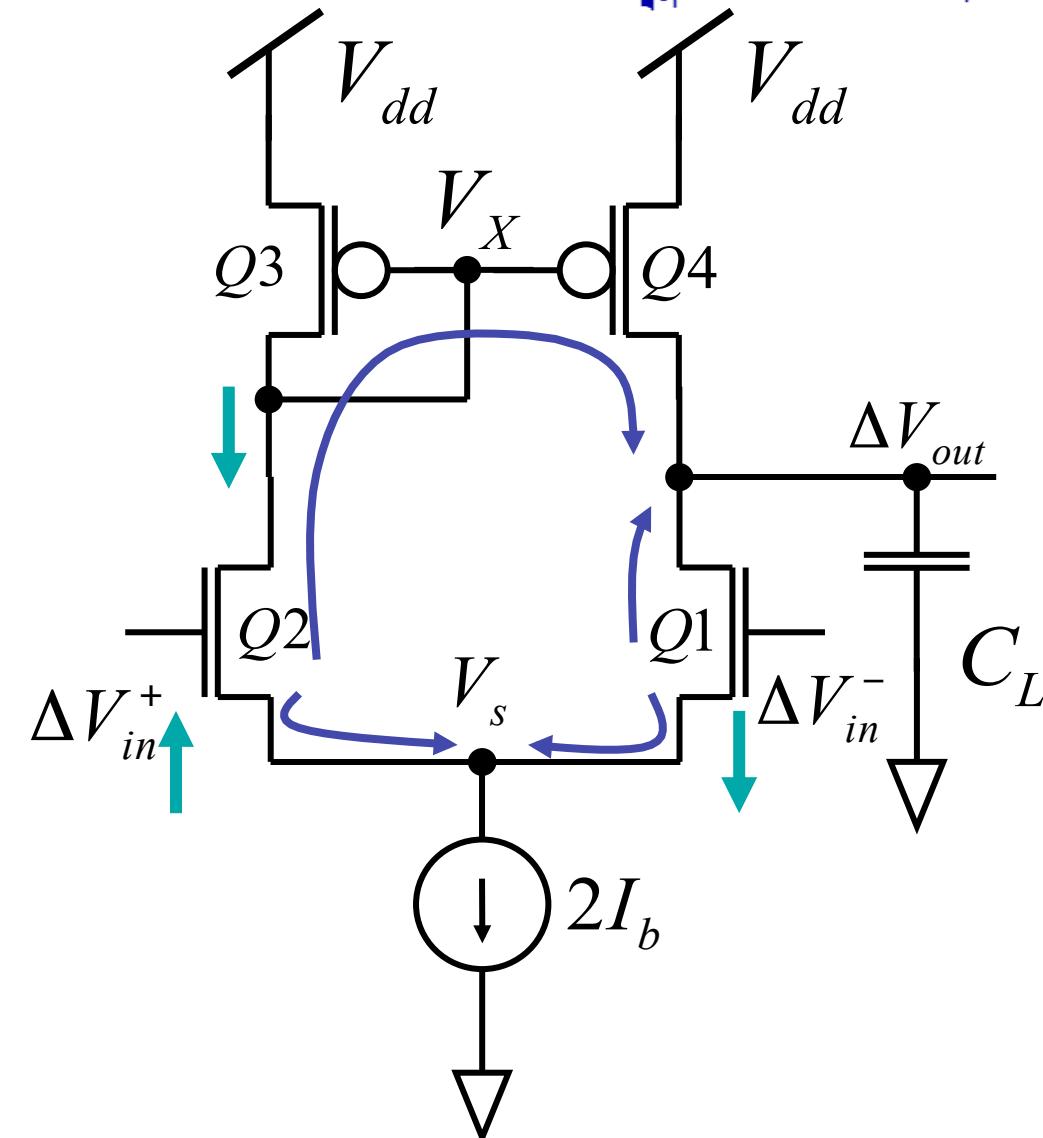
$$\omega_{p1} = \frac{2}{r_{ds}C_L} \quad \omega_{p2} = \frac{g_m}{2C_{gs}}$$

Dominant pole is the output pole.

Location of zero is twice the frequency of the second pole.

$$\omega_z = \frac{g_m}{C_{gs}}$$

Conceptual Analysis



Conceptual operation for frequency analysis.

All nodes have internal capacitances.

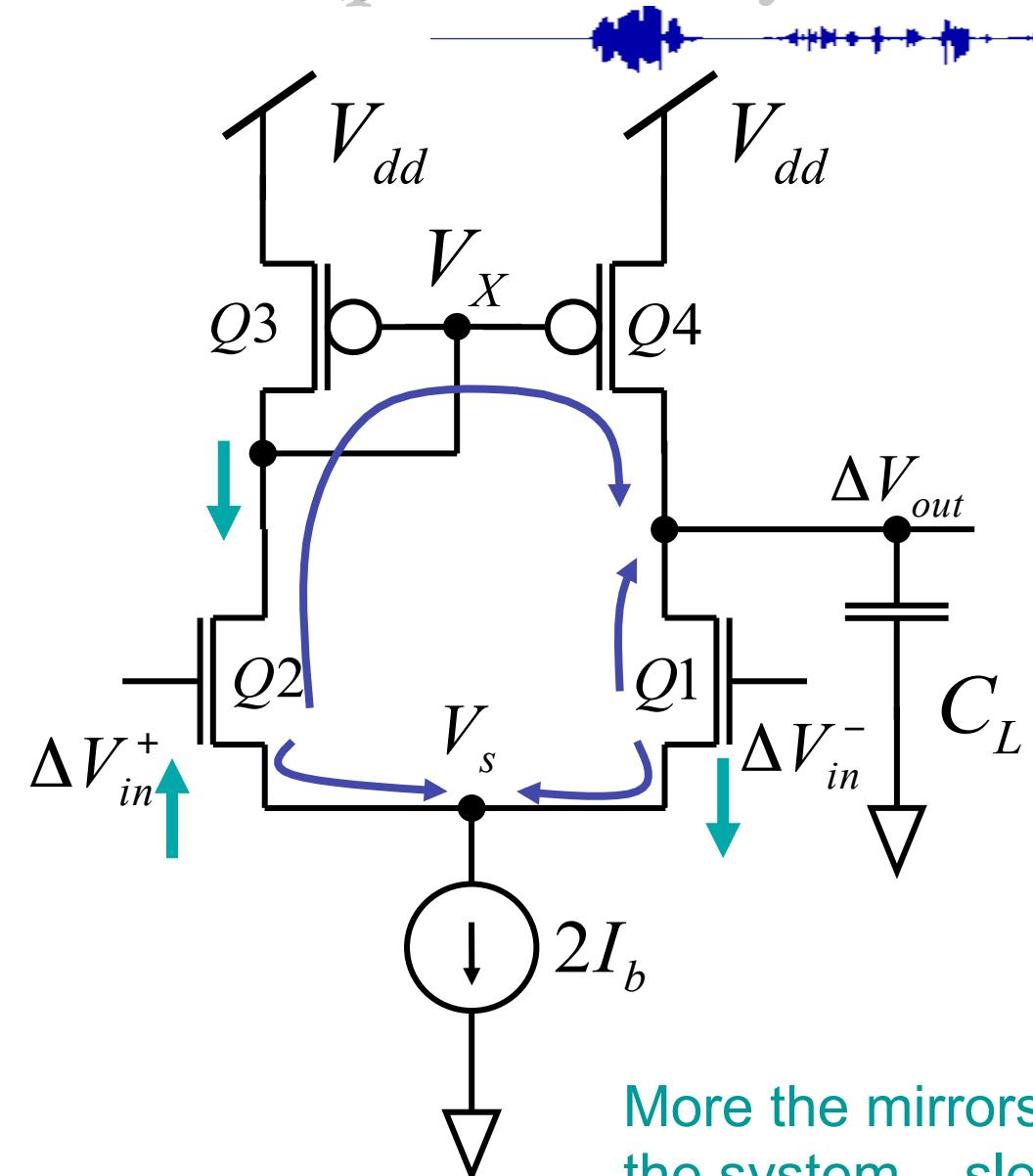
When the gate of Q2 increases, the current through Q2 will instantaneously increase (Voltage controlled current source).

The current will slowly discharge the node V_x (pole).

The current through Q4 will increase slowly.



Conceptual Analysis



At the same time the gate of Q_1 decreases which will instantaneously change the current through Q_1 .

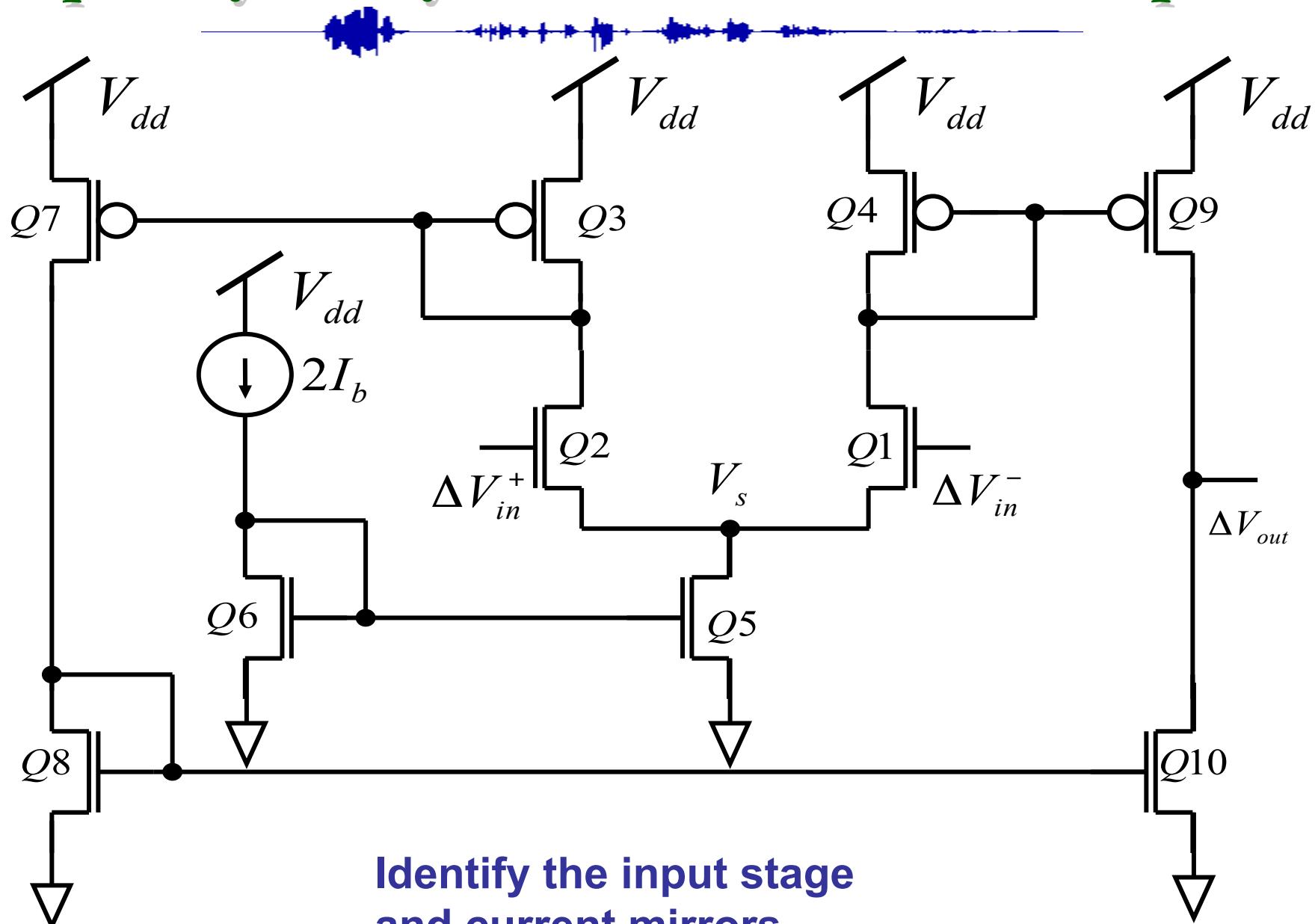
The current through Q_1 will be compared with current through Q_4 at the output node.

If the currents don't cancel each other (zero) then the extra current will slowly charge the output node (pole).

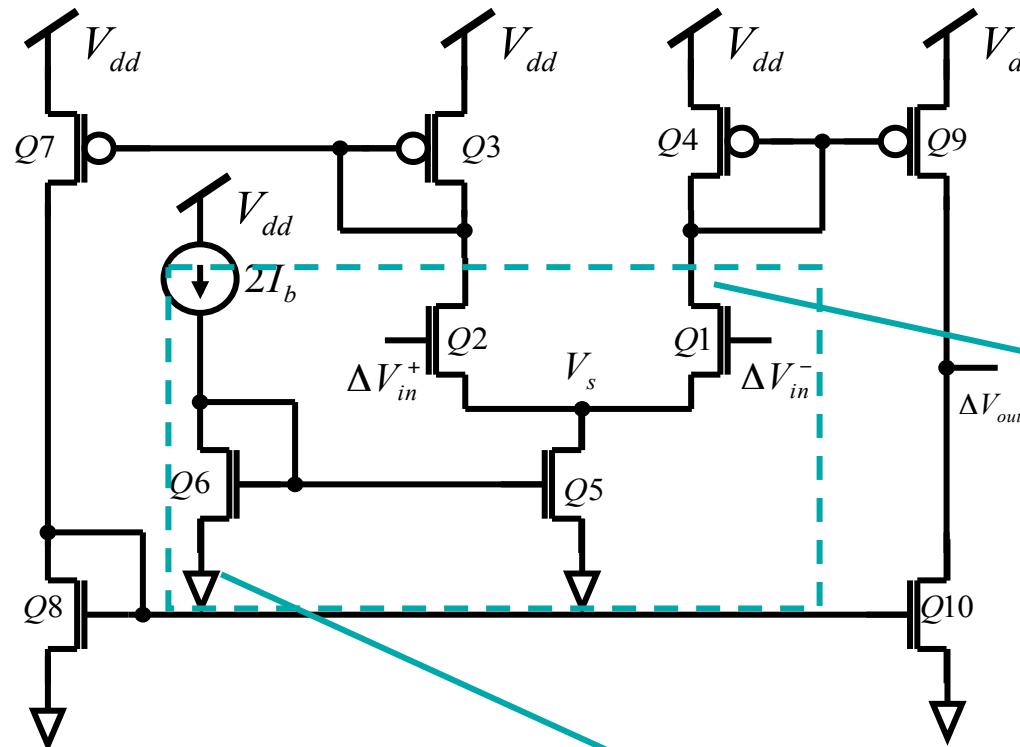
At the node V_s , the signal always cancels out if Q_1 and Q_2 are symmetrical.

More the mirrors – more poles in the system – slower the circuit.

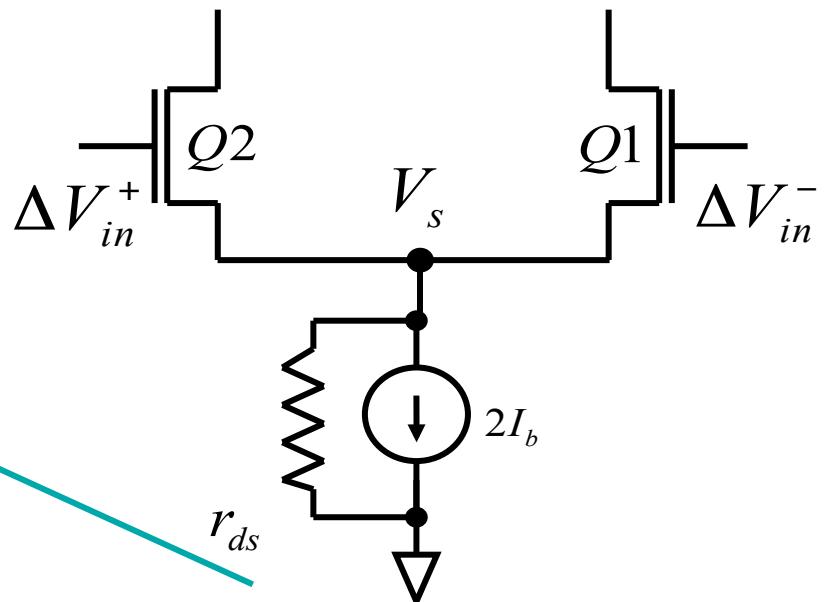
Frequency Analysis of Multi-mirror Amplifier



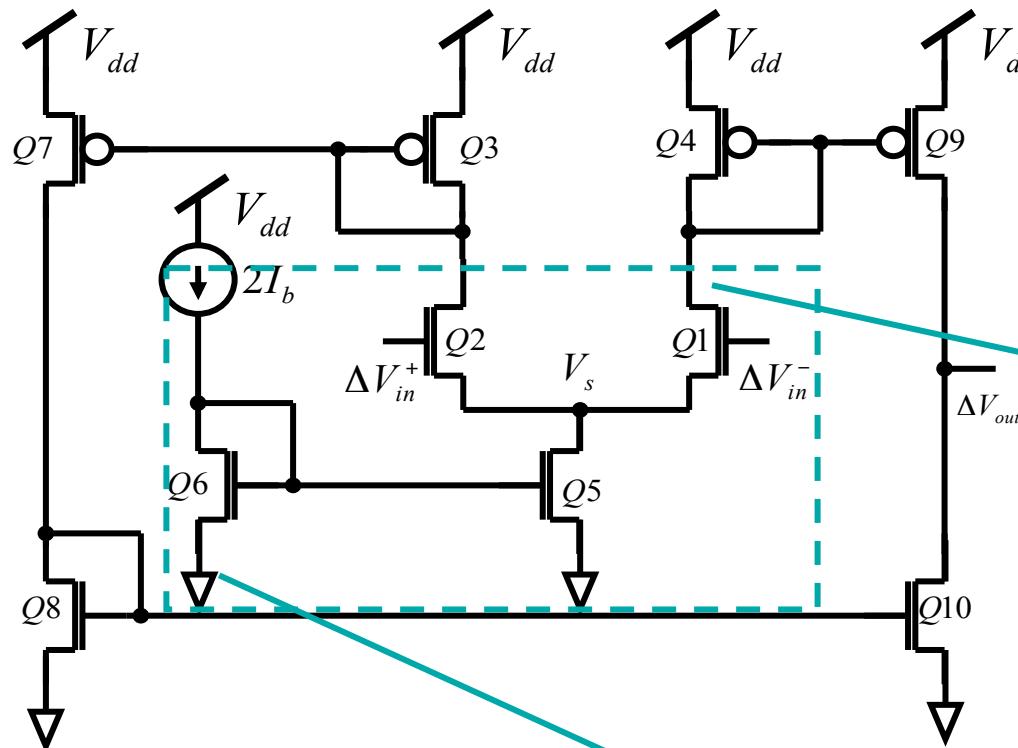
Input stage and Symmetry



Input stage is again a differential pair.

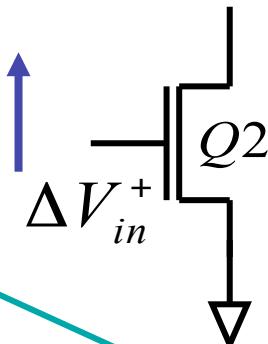


Compute the change in input current

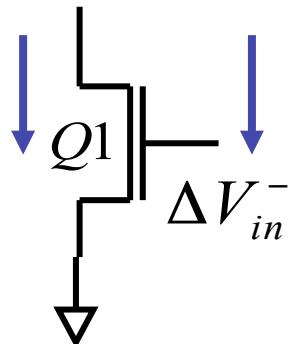


Use symmetry and note the differential output current for differential input voltage.

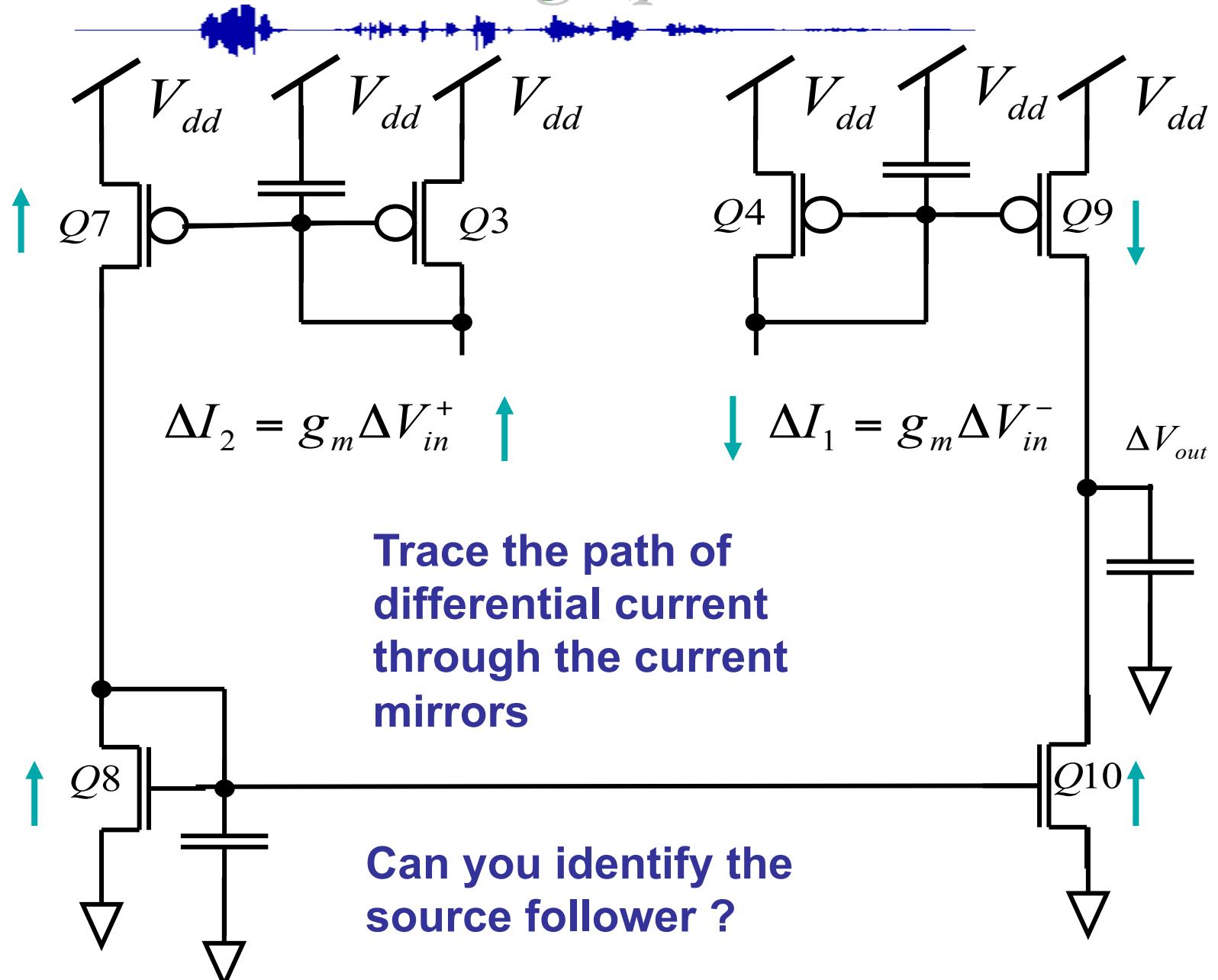
$$\Delta I_2 = g_m \Delta V_{in}^+$$



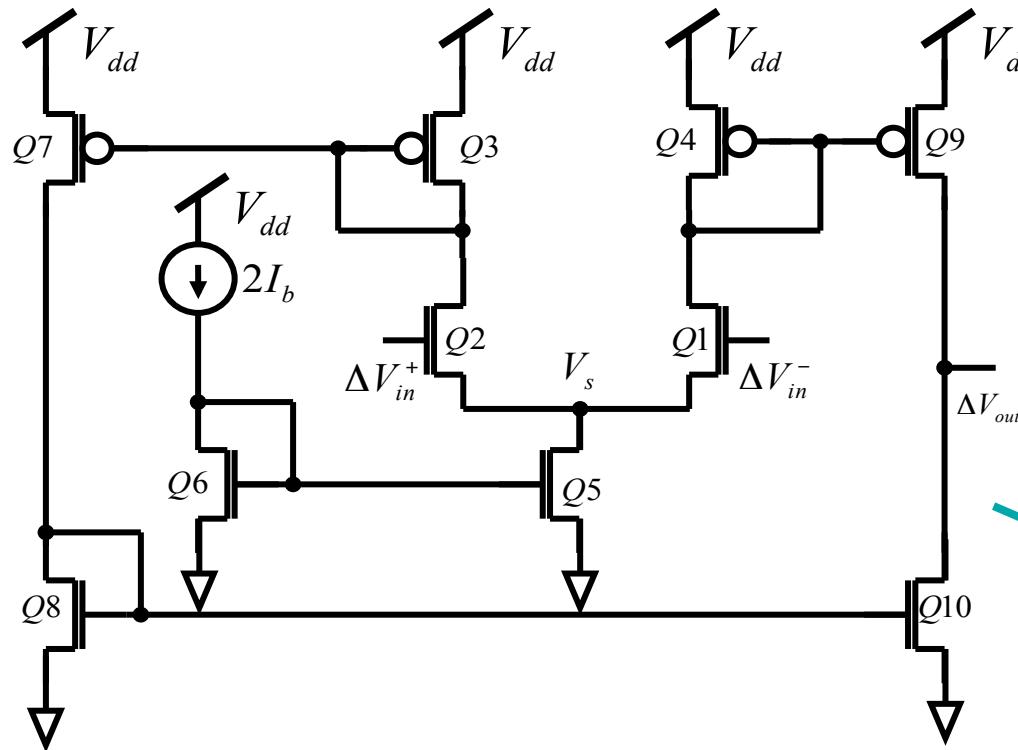
$$\Delta I_1 = g_m \Delta V_{in}^-$$



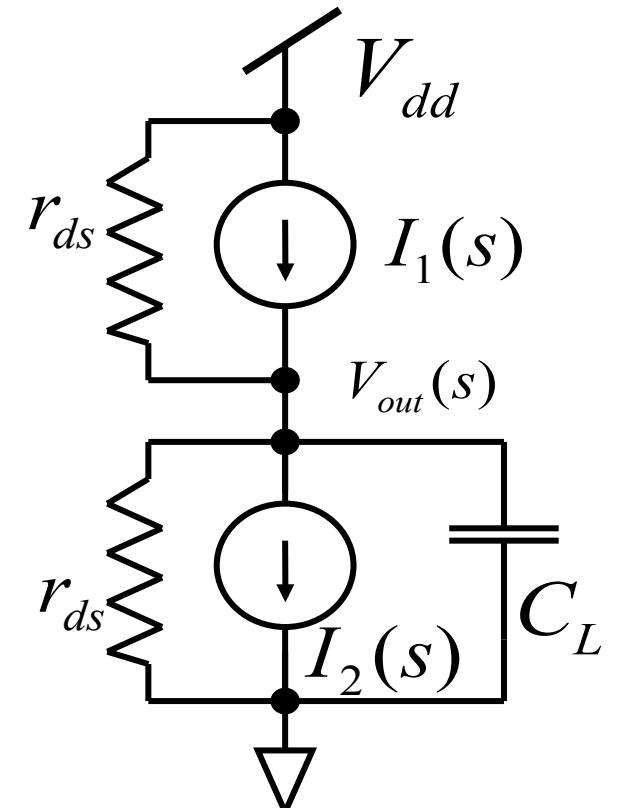
Trace the current through poles



Generate amplifier equivalent model



The equivalent circuit is again two current comparators with a load connected to the output.



Worksheet

