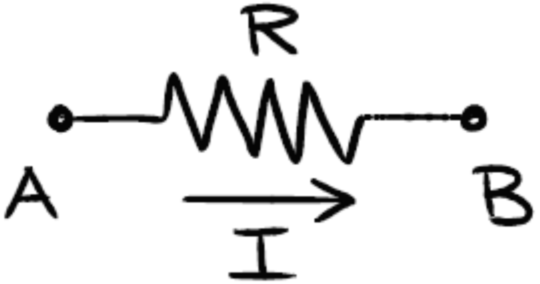
Power Dissipation

CSE562: Analog Integrated Circuits

Shantanu Chakrabartty

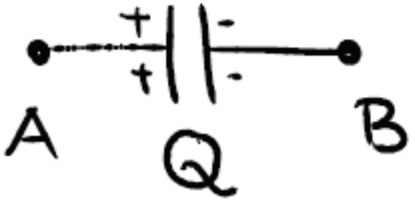
Adaptive Integrated
Microsystems
(AIM)
Laboratory

Power dissipation in basic circuits



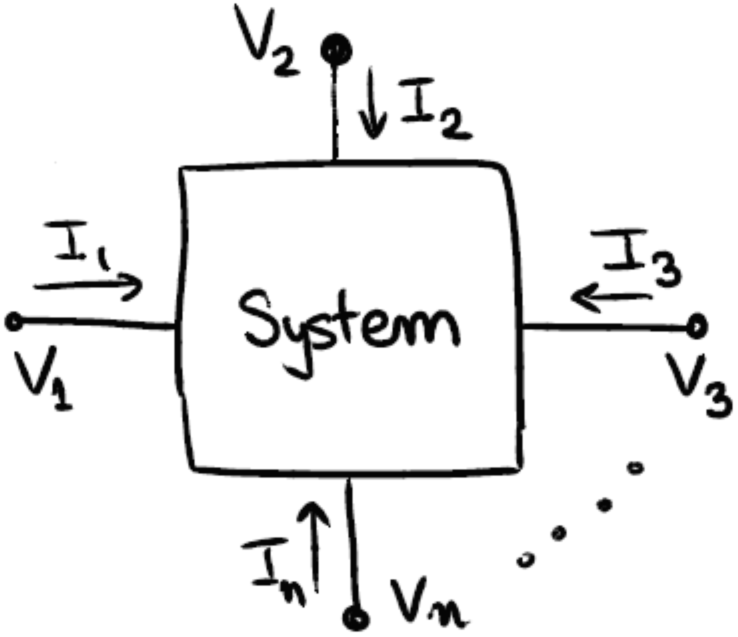
- Power dissipation Resistor

$$P_{diss} = V.I = I^2 R = V^2 / R$$



- Energy stored in a capacitor

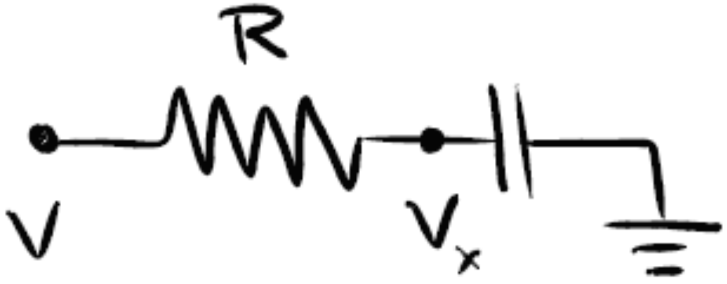
$$E_{stored} = \frac{1}{2} C V^2 = \frac{Q^2}{2C}$$

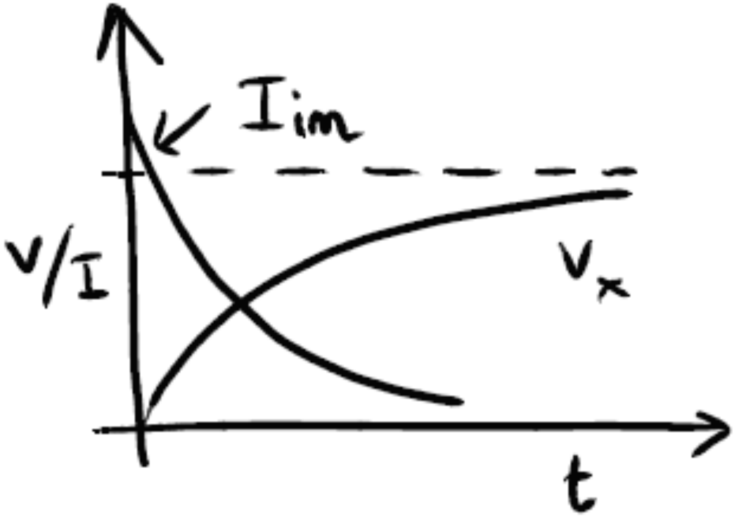


- Energy dissipated in a generic system

$$P_{diss} = \sum_{i=1}^{N} \mathrm{Re}\{V_i I_i\}$$

Power dissipation





- Power dissipation occurs only when voltage and current are in phase.

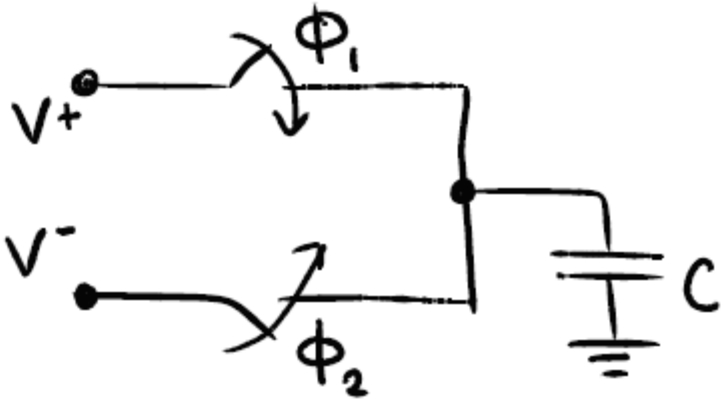
$$E_{diss} = \int_0^\infty \frac{1}{R}\left[V - V_x(t)\right]^2 dt$$

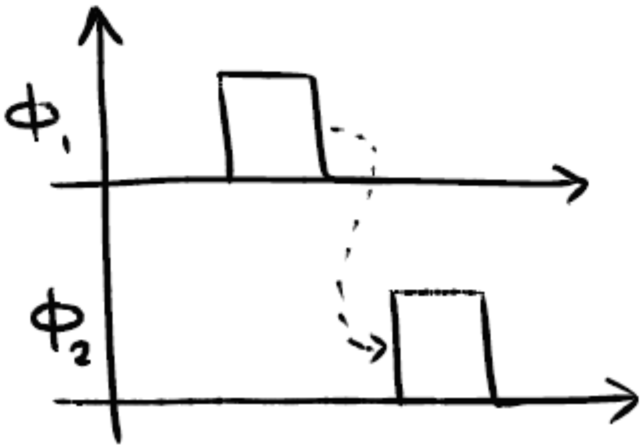
$$E_{diss} = \frac{1}{2}CV^2$$

- Total energy dissipated through the resistor is the energy stored on the capacitor and independent of the resistor – Why ?

$$P_{trans} = \frac{dE}{dt} = CV\frac{dV}{dt} = V\frac{dQ}{dt} = V.I$$

Energy dissipated in switched capacitor circuits

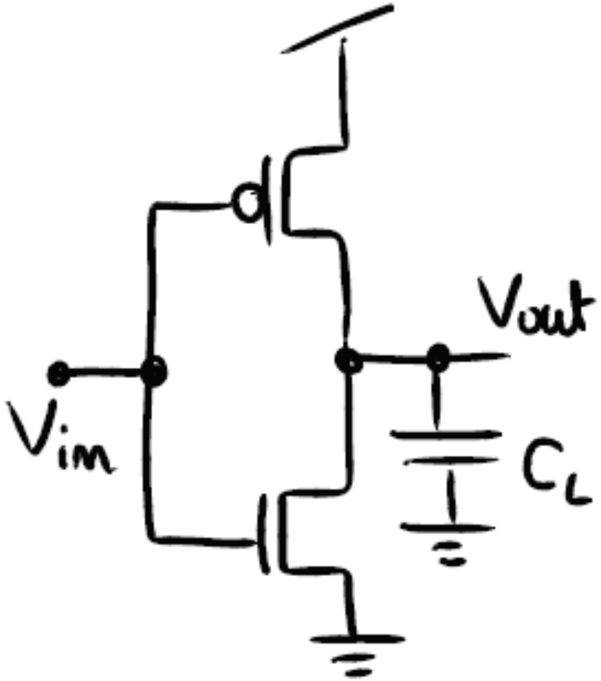




- Power dissipation occurs only when voltage and current are in phase – or when stored energy is dissipated to the ground.

$$E_{diss} = \frac{1}{2}C\left(V^{+} - V^{-}\right)^{2} = \frac{1}{2}C\Delta V^{2}$$

Energy dissipation in digital circuits



$$P_{diss} = P_{static} + P_{transient}$$

- Static power dissipation
  - Junction leakage (diodes)
  - Sub-threshold leakage
- Transient power dissipation
  - Dynamic power dissipation – charge or discharge load capacitance.
  - Shoot-through power dissipation – both pmos and nmos active.

$$P_{av} = P_{switching} + P_{short-circuit} + P_{leakage}$$

$$P_{av} = \alpha_{0\to 1} C_L V_{dd}^2 f_{clk} + I_{sc} V_{dd} + I_{leakage} V_{dd}$$

Energy Optimization

- Power optimization at different levels
  - Technology level
  - Circuit level and layout level
  - Logic level
  - System and architectural level
  - Algorithmic level

- At higher levels more degrees of freedom available to optimize energy dissipation. Most important – algorithmic optimization.

Technology Level Optimization

- Reduce supply voltage

$$P_{diss} \propto C_{gs} V_{dd}^{2} \qquad\qquad T_{d} \propto \frac{C_{gs}}{V_{dd}}$$

  - Reduce supply voltage by factor of 2, power dissipation reduces by a factor of 4, delay increases by a factor of 2.
  - Reduce feature size (gate capacitance) by a factor of 2, power dissipation reduces by a factor of 2, delay reduces by a factor of 2.
  - For the same delay, a reduced feature size (smaller process) leads to 8 times reduction in power if the supply voltage is reduced by 2.
  - Trade-off is noise-margin reduces with reduction in supply voltage.

Technology Level Optimization

- Threshold voltage optimization

$$I_{lk} = I_0 \exp\left(-\frac{V_{th}}{U_T}\right)\exp\left(\kappa\frac{V_g}{U_T}\right)\exp\left(-\frac{V_s}{U_T}\right)$$

  - Reduce threshold voltage reduces noise margin but increases sub-threshold leakage current – increases static power dissipation.

  - Same process allows fabrication of transistors with different threshold voltages. E.g. stanford ultra-low-power CMOS or silicon-on-sapphire technology.

Technology Level Optimization

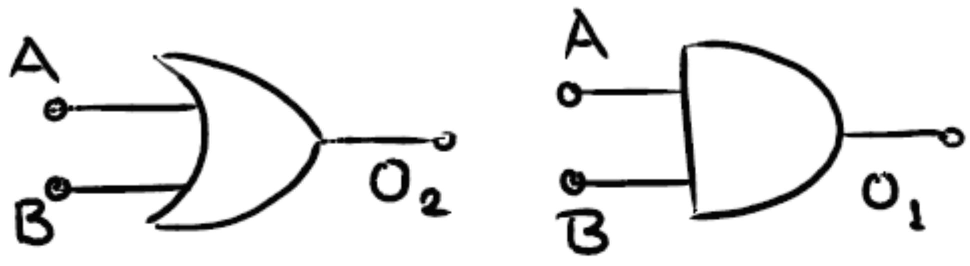
- Reduction in leakage currents
  - Each transistor which is turned off - conducting approximately current of 10pA. A billion transistor IC would consume a current of 10mA – power dissipation of 10mW @ 1V.

$$\frac{I_{d1}}{I_{d2}} = \exp\left(\kappa \frac{V_{g1} - V_{g2}}{U_T}\right) \qquad \Delta V_g = \frac{U_T}{\kappa} \log 10$$

  - Sub-threshold slope determines how effectively the transistor can be shut off. Maximum sub-threshold slope is 60mV/dec when k = 1.
  - Silicon-on-sapphire technology can get close to the theoretical limit.

Circuit level optimization

- Reduce the capacitance of the line which has the highest switching activity.
- Which of the output lines O_1 or O_2 should be connected to a shorter interconnect ? Assume the inputs A and B are random.

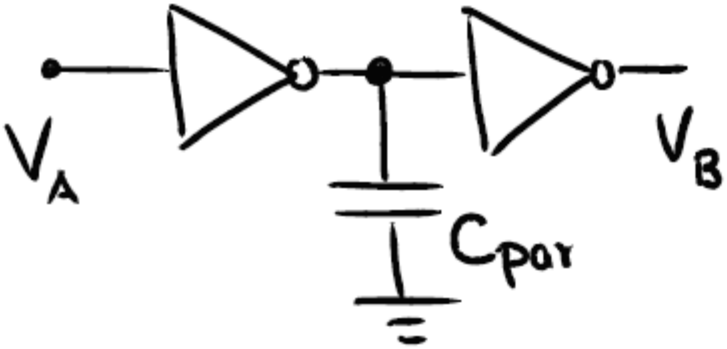


- Transistor size optimization.
- N = (W/L), C_p = parasitics

$$T_d \propto \frac{C_P + NC_{gs}}{NC_{gs}} \frac{V_{dd}}{\left(V_{dd} - V_{th}\right)^2} \propto \frac{\left(1 + \frac{\alpha}{N}\right)}{V_{dd}}$$

$$V_{dd}^{''} = \frac{\left(1 + \frac{\alpha}{N}\right)}{\left(1 + \alpha\right)} V_{dd}$$

$$P_d = \left(C_P + NC_{gs}\right) V_{dd}^{''2} f$$



$$F \propto \frac{N\left(1 + \frac{\alpha}{N}\right)^3}{\left(1 + \alpha\right)^3}$$

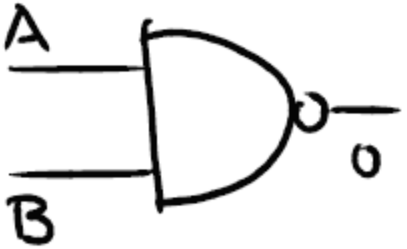
- Significant parasitics increase in transistor sizes reduces power dissipation – otherwise NO !

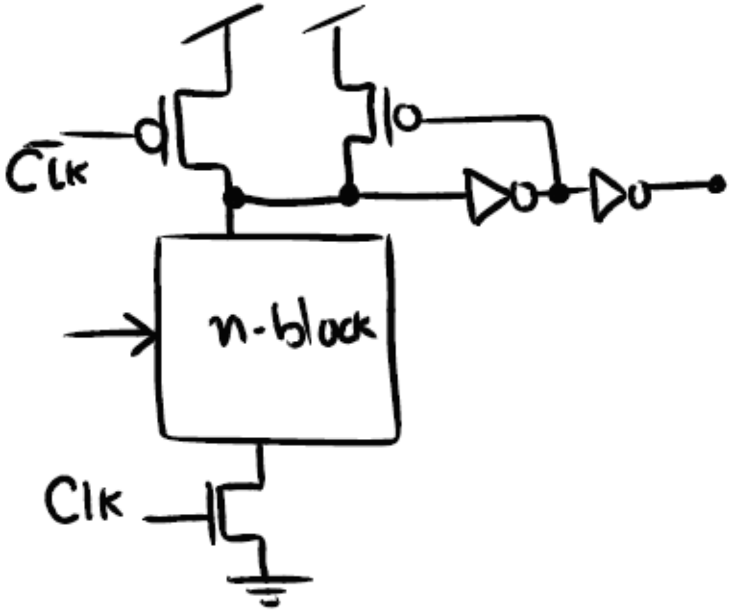
Circuit Level Optimization

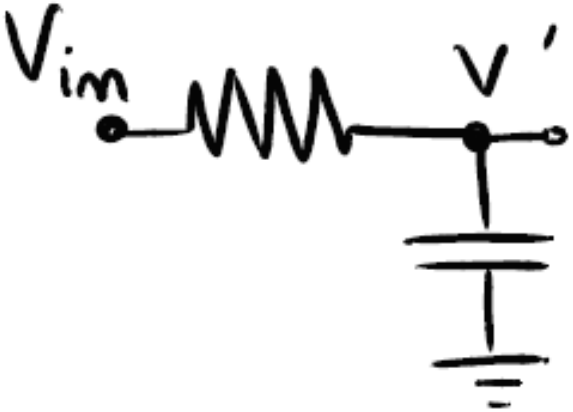
- Reduce switching activity
  - Minimize the number of transistors in a function.
  - Power off inactive blocks (power management).

Logic optimization: Dynamic or static or adiabatic

- NAND – Output is high 25% of time.
- Adiabatic logic – asymptotically zero power.

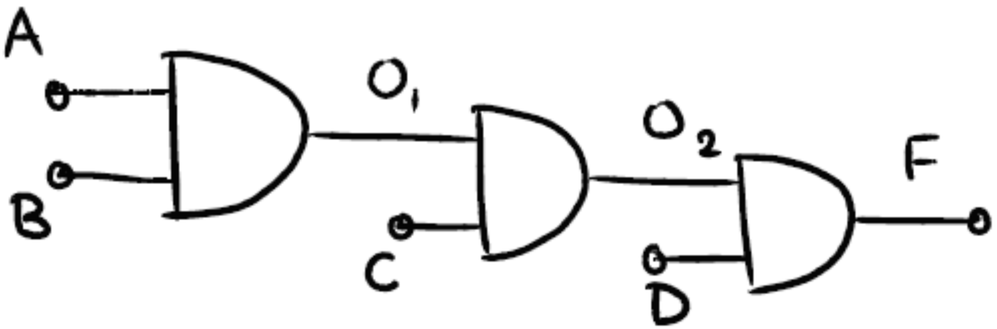


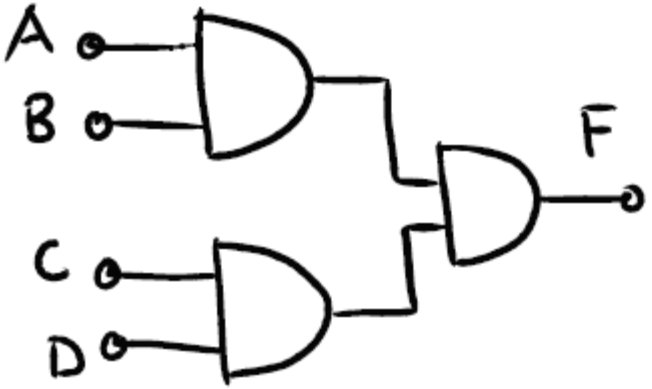




Circuit Level Optimization

- Logic topology
  - For the two logic circuits which output shows the most switching activity ?
  - What are the advantages and disadvantages of each of the logic topologies ?





- Clock gating or power off inactive blocks
  - For e.g. for a comparator A > B, gate the rest of the circuit if MSB of A > MSB of B.

Architecture Level Optimization

- Parallel hardware
  - Break a task in ``n" independent components, that can be performed in parallel.
  - Reduce the frequency of operation by a factor of ``n".
  - Reduce the supply voltage by a factor of ``n" – same speed
  - Area increases by a factor of ``n".

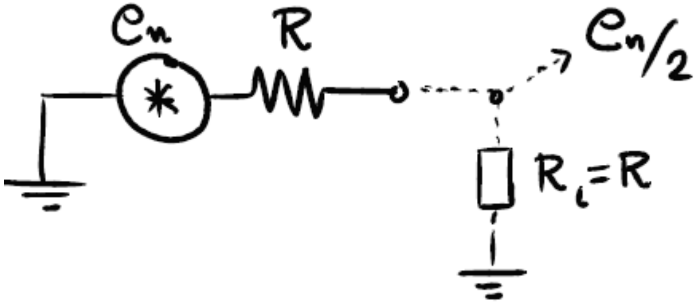
$$P_{diss} = n \times \alpha_{0\rightarrow 1} C_L \left(\frac{V_{dd}}{n}\right)^2 \left(\frac{f_{clk}}{n}\right)$$

- Number representation
  - Use gray codes instead of binary codes.
  - Order the inputs such that correlated signals appear in the system.

$$\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 1 \\ 0 & 1 & 0 \\ 1 & 1 & 0 \\ & \vdots & \end{bmatrix}$$

Algorithm Level Optimization

- Minimize the number of operations (e.g. use binary search instead of a linear search)
- Use signal statistics
- Multiplication with a constant (use shift operation or a look-up table approach).
- Use finite precision algorithms.

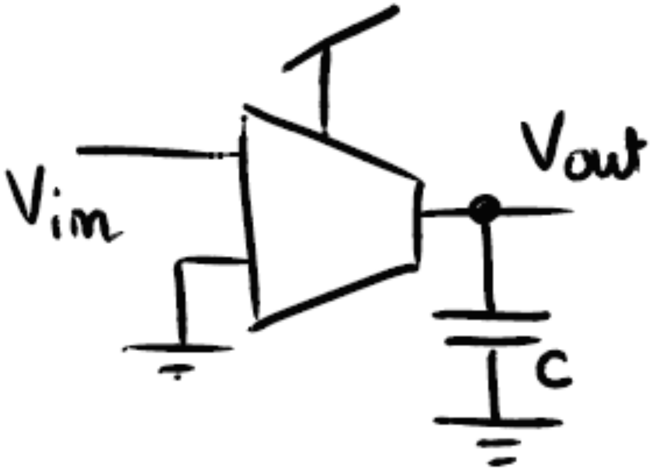


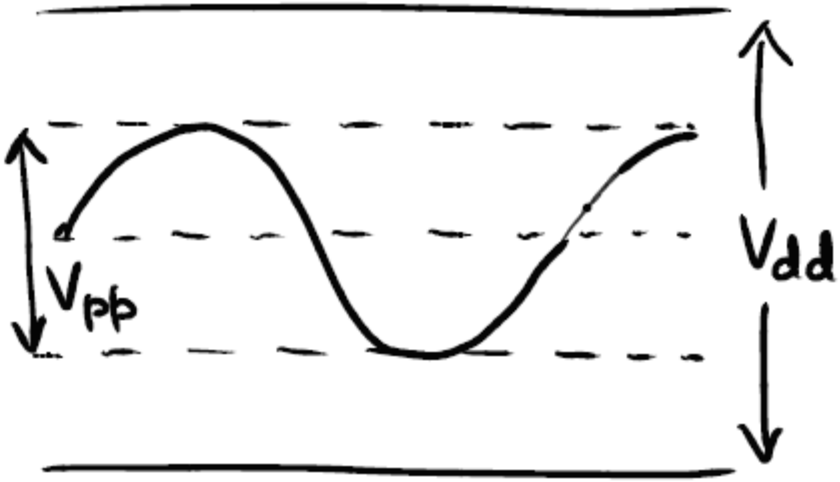
- Fundamental limits of power dissipation
  - Viewed as energy transfer problem – need to transfer more energy than thermal energy.
  - Logic gate resistance – R. Thermal noise: $e_n^2 = 4KTR\Delta f$
  - Power transferred $P_{th} = \dfrac{e_n^2}{4R}$ $\quad P_s > P_{th} = KT\Delta f$
  - Fundamental limit for a logic transition: $E_S > KT$

Power Estimation and Optimization: Analog

For analog circuits the power dissipation is determined by:

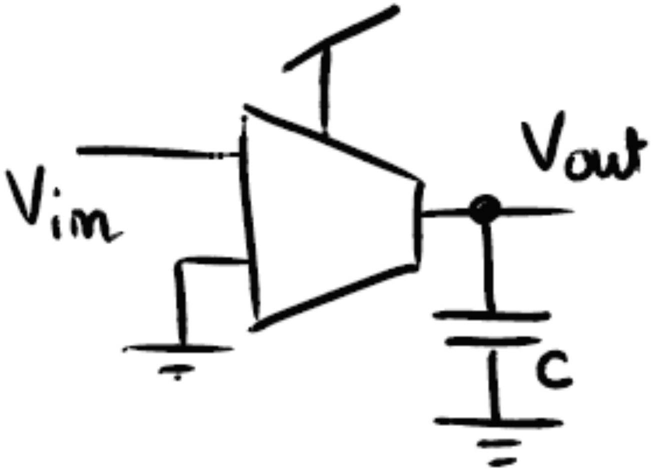
- Signal-to-noise ratio
- Frequency of operation or bandwidth
- Fundamental limit determined by power consumption per pole.

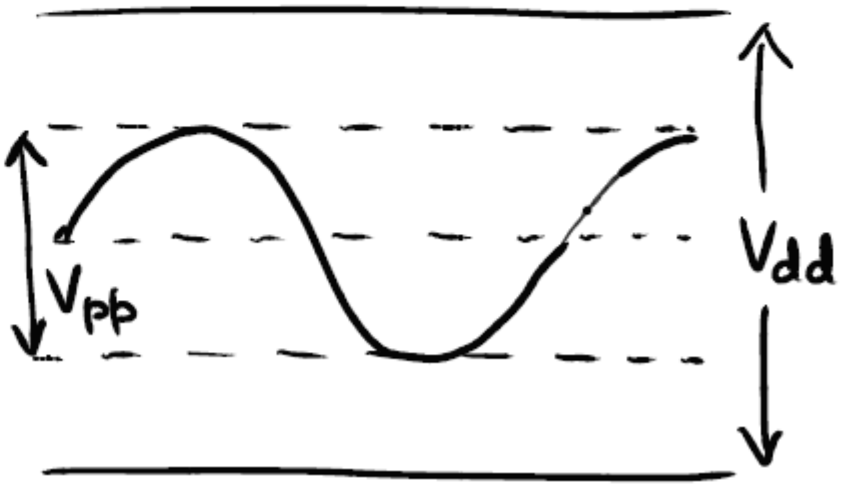




Aim: Maintain the signal above the noise floor.

Power Estimation and Optimization: Analog





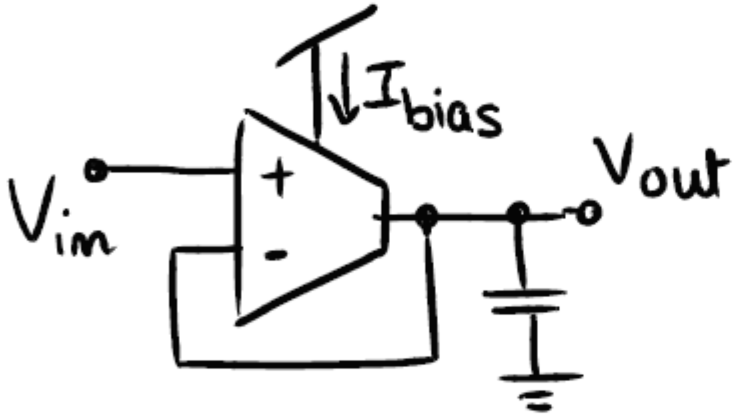
- Signal-to-noise ratio: $SNR = \dfrac{V_{pp}^2 / 8}{KT / C}$
- Power consumed to maintain a target voltage level. $P = V_{dd} fCV_{pp} = fCV_{pp}^2 \dfrac{V_{dd}}{V_{pp}}$
- Power per pole: $P_d / pole = 8KTf \; SNR \dfrac{V_{dd}}{V_{pp}}$
- For $V_{pp} = V_{dd}$

$P_d / pole = 8KTf \;\; SNR$ - Compare with digital fundamental limit.

Analog Power Optimization Rules

- Reduce the number of capacitances. Capacitances increases the power dissipation to achieve a specific bandwidth – use more capacitances ONLY if it reduces the noise power by the same amount.
- Optimize the power for the bias circuitry. Inadequate bias schemes increase the noise and power dissipation (e.g. cascoding optimizes the bias).
- Maintain rail-to-rail signal at internal nodes.
- Reduce additional sources of noise, unnecessary transistors or devices.
- Low power dissipation and low precision.
- Use sub-threshold biasing when speed is not critical.

Fundamental limits using power-delay product

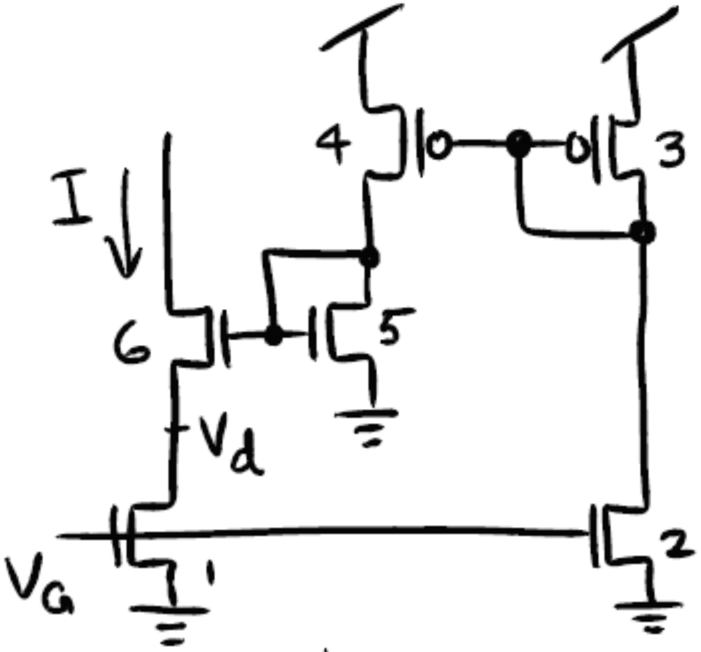


- Time constant: $\tau = C / g_m$
- Power dissipation: $P = V_{dd} I_{bias}$
- Power-delay product: $P\tau = \dfrac{I_{bias}}{g_m} C V_{dd}$

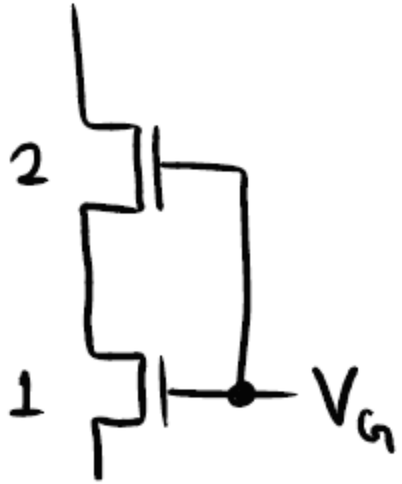
- Increase $\dfrac{g_m}{I_{bias}}$
- Use sub-threshold biasing $\dfrac{g_m}{I_{bias}} = \dfrac{\kappa}{U_T}$

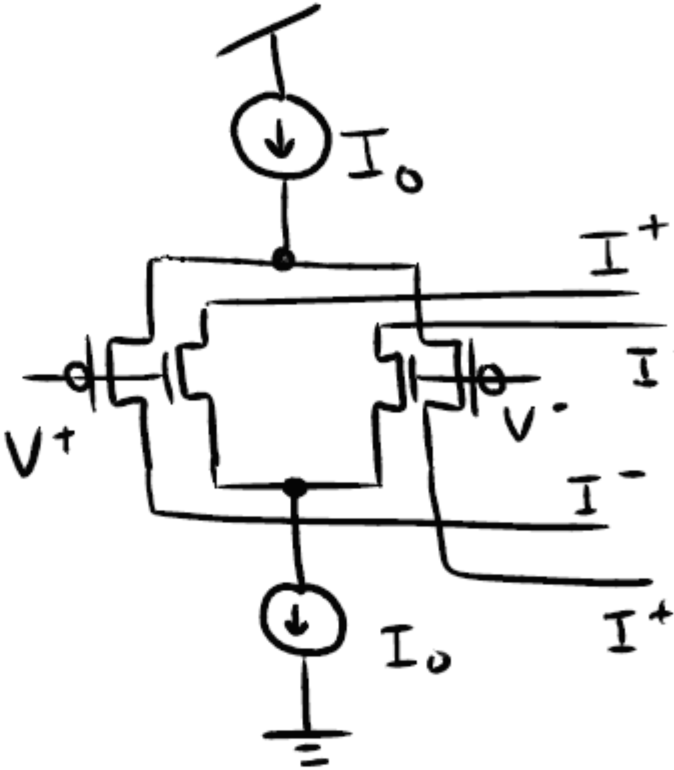
- Reduce V_{dd} and C – determined by the KT/C noise and the input/output dynamic range.
- Use compressive signaling at the capacitor (log-domain).

Low-voltage techniques

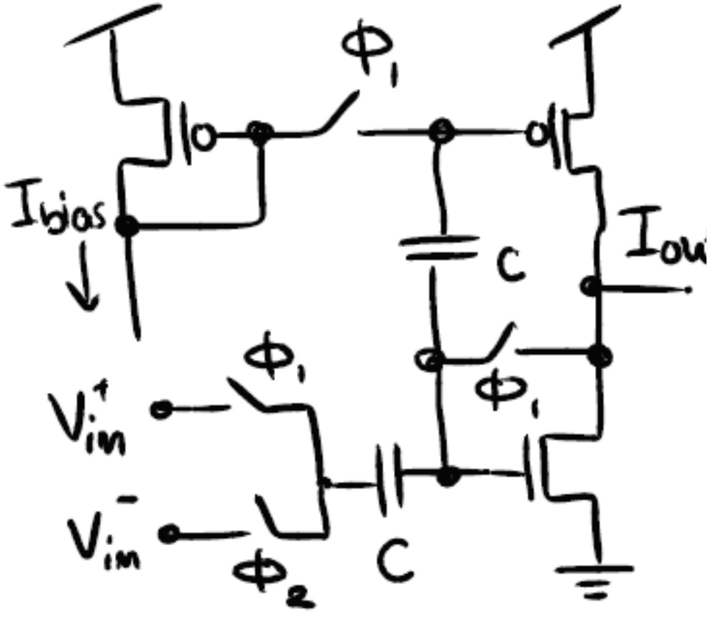


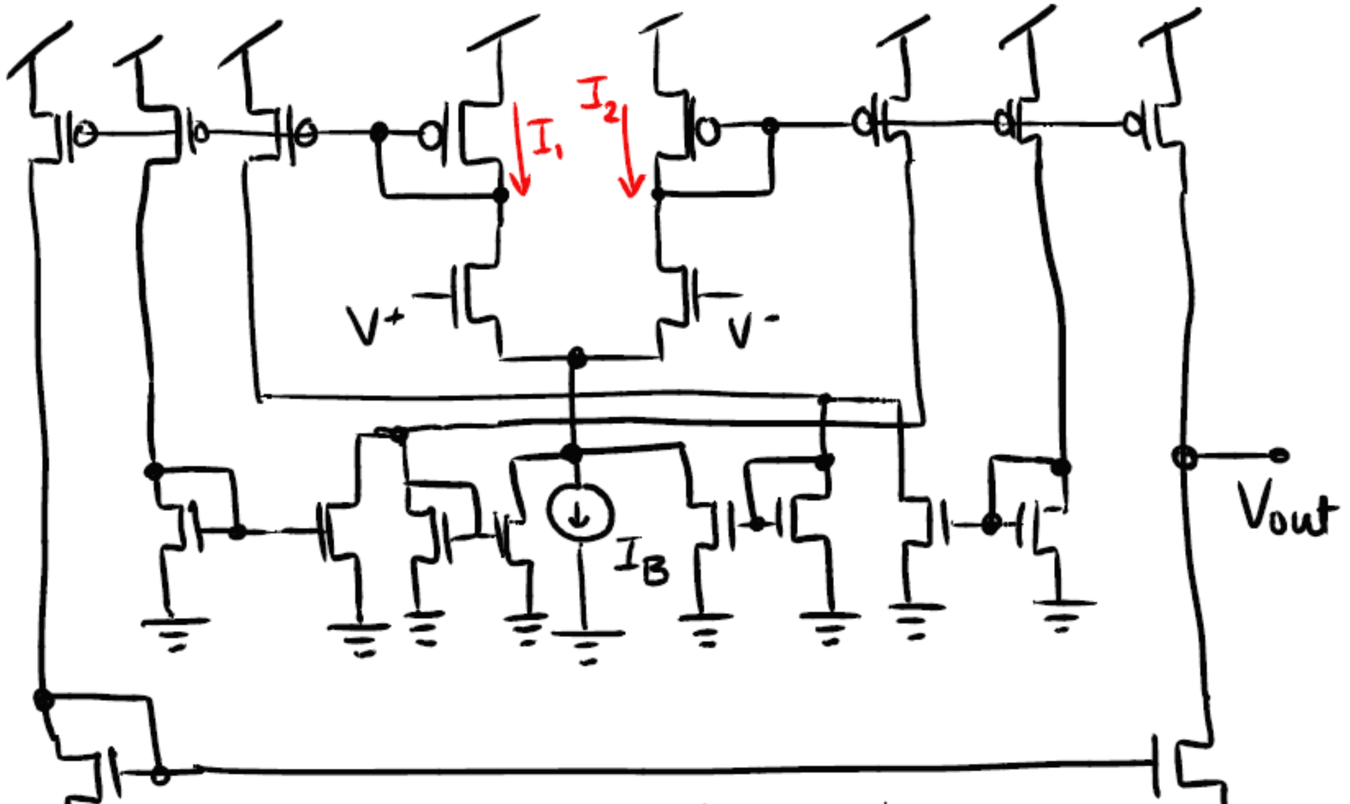
- Low-voltage cascodes
- Eliminate gate-voltage drops
- Maintain transistors on the verge of saturation to maximize output swing.

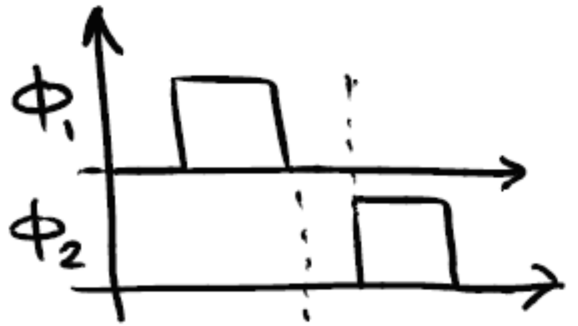


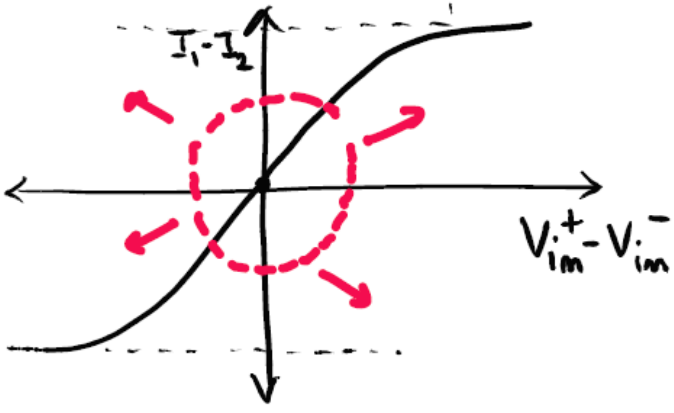


Dynamic Biasing Techniques


Φ1
Ibias
C
Iout
Φ1
Φ1
V_{in}^{+}
V_{in}^{-}
Φ2
C


I1
I2
V+
V-
IB
Vout




I1-I2
$V_{in}^{+}-V_{in}^{-}$