An Efficient First Order Sigma Delta Modulator Design

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ABSTRACT

An efficient first order sigma delta modulator has been designed in circuit level, considering the possible non-idealities in 65 nm CMOS technology. This study at first determines the non-idealities of sigma delta modulator. The non-idealities investigated here are clock jitter noise that effects the input signal and increases total error power; then the thermal noise of switches caused by the random fluctuation of carrier that increases the total noise power. Thereafter, circuit leakage causes the limited DC gain and affects signal to noise ratio. Moreover, limited slew rate and gain bandwidth of op-amp, which are both regarded as non-linear gain, reduce signal to noise sum distortion ratio. Based on optimum circuit simulation, the non-idealities are reduced by using folded cascode op-amp at integrator stage with DC gain of 65 dB, slew rate of 3.76 V/μs, and gain bandwidth with 40 MHz. Finally, a first order sigma delta modulator with 8 bit resolution, 64 oversampling ratio as well as power supply of ±2.5 V is successfully designed using PSPICE simulation tool, which can be implemented for practical usage.

1. INTRODUCTION

Nowadays, the sigma delta modulator has gained importance because of the developments in digital VLSI technologies which provide the practical means to implement the large digital signal processing circuitry. The increasing use of digital techniques in communication and audio application has also contributed to the recent interest in cost effective high precision A/D converters. A requirement of analog-to-digital (A/D) interfaces is compatibility with VLSI technology, in order to provide for monolithic integration of both the analog and digital sections on a single die. As the Greek letter-Δ (delta) is used to show the deviation or small incremental change, the process came to be known as "delta modulation". Delta modulation is based on quantizing the change in the signal from sample to sample rather than the absolute value of the signal at each sample. Sigma stands for summing or integrating, which is performed at the input stage on the digital output with the input signal before the delta modulation. Hence the analog to digital conversion of this technique is called sigma-delta modulation.

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The 1st order sigma-delta modulator design consists of mainly an integrator, a comparator and a D/A converter. The single-bit feedback D/A converter (DAC) output is subtracted from the analog input signal in the summing amplifier. The resultant error signal from the summing amplifier output is low-pass filtered by the integrator and the integrated error signal polarity is detected by the single comparator. This comparator is effectively a 1-bit A/D converter (ADC). This architecture achieves a wide range of resolution and a higher bandwidth. Settling time is an important parameter which determines the resolution of an ADC. It is defined as a small amount of time required for an ADC to reach certain accuracy and stay within the specified range of accuracy. If the settling time is linearly dependent on the input signal, a high-resolution performance can be achieved even if the integrator does not settle to the full resolution of the converter. Due to the saturation of the input stage and slew rate limitation of the output stage, the settling error in the converter can be nonlinear which can be a dominant factor in limiting its performance. One way to avoid saturation limitations in the input stage is to use a large overdrive voltage for the input transistors of the differential pair in the operational amplifier, which cannot be afforded for low voltage design.

In this paper, the non-idealities of sigma delta modulator have been investigated first and then a first order sigma delta modulator is designed using 65 nm CMOS technology. The modulator uses folded cascode op-amp to design integrator and comparator at an operating power supply of ± 2.5 V. The final circuit is constructed using the PSPICE simulation tools.

2. INVESTIGATION OF THE NON IDEALITIES

2.1. Clock Jitter

The operation of a SC circuit depends on complete charge transfers during each of the clock phases. In fact, the variation of the clock period has no direct effect on the circuit performance, because the SC circuit is a sampled-data system. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal and is independent of the

structure or order of the modulator. Sampling clock jitter result in non-uniform sampling and increases the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal to the converter. In this case, the total error power will be reduced by the oversampling ratio [1].

2.2. Thermal Noise of Switches

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidths of op-amps. Therefore, it must be taken into account for both the switches and the op-amps in an SC circuit [2].

2.3. DC Gain of Integrator

In practice, however, the gain is limited by circuit constraints. The consequence of this integrator "leakage" is that only a fraction of the previous output of the integrator is added to each new input sample. The transfer function of the integrator with leakage becomes [1]:

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \qquad (1)$$

The dc gain *Ho* becomes therefore:

$$H(0) = \frac{1}{1 - \alpha} \qquad (2)$$

The limited gain at low frequencies increases the in-band noise.

2.4. Bandwidth and Slew Rate

The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain. The slew-rate and bandwidth limitations produce harmonic distortion reducing the total signal-to-noise plus distortion ratio (SNDR) of the sigma delta modulator [1].

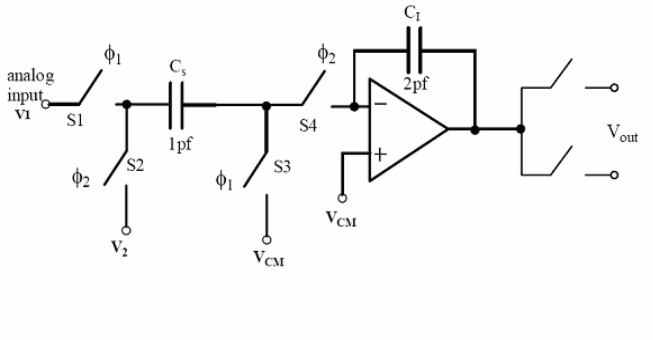

Fig. 1. Conventional non-inverting integrator

3. INTEGRATOR DESIGN

The SC integrator consists of an op-amp, a sampling capacitor CS, an integrating capacitor CI, and four MOS transistor switches as can be seen in the reference circuit in Fig. 1[3]. The common mode voltage VCM is halfway between the mixed signal systems high reference voltage (+2.5 V) and low reference voltage (-2.5 V). Hence the common mode voltage, V_{CM} is 0 V.

During the interval, when clock phase Φ1 is high, switches S1 and S3 operate and serve to charge the sampling capacitor, C_S to a voltage that is equal to the input voltage. Subsequently, clock signal Φ1 falls. Then clock signal Φ2 rises, causing switches S2 and S4 to turn on and the sampling capacitor C_S to be connected between the inverting op-amp input, which is sometimes called the summing node, and ground. If the op-amp is ideal, the resulting change in the summing-node voltage causes the op-amp output to change, so that the summing-node voltage is driven back to ground. After the transient has gone to completion, the voltage across C_S is driven to zero.

To find the relationship between the input and output, a charge-conservation analysis is used. After switch S1 opens, the charge on the plates of the capacitors connected to node top and the inverting op-amp input is conserved until switch S1 closes again. Now, we define two points [n] and [n+1/2] as the time indices at which Φ1 and Φ2 first fall. Point [n+1] is defined as the next time index at which Φ1 falls. The points [n] and [n+1] are separated by one clock period T. If the switches and the op-amp are ideal, the charge stored at time index [n] is given by the following equation. [3]

$$Q[n] = (0\text{-}VS[n])\, C_S + (0\text{-}VO[n])CI \qquad (3)$$

Where, VS represents the input voltage at the end of Φ1 and VO represents the output voltage at the end of Φ2. Here, if the op-amp is ideal, the voltage Vi from the inverting op-amp input to ground is driven to zero by negative feedback during Φ2. At the same conditions, the charge stored at time index [n+1/2] is as the following equation.

$$Q[n+1/2] = (0)\, C_S + (0\text{-}VO\,[n+1/2])CI \qquad (4)$$

For charge conversation, Q[n+1/2] = Q[n]. Also, the charge stored on CI is constant during Φ1under these conditions, therefore, VO [n+1] = VO [n+1/2]. Combining these equations gives,

$$VO\,[n+1] = VO\,[n] + (C_S/CI)\, VS[n] \qquad (5)$$

Thus, one complete clock cycle results in a change in the integrator output voltage that is proportional to the value of the input voltage and to the capacitor ratio. The above equation is used to find the frequency response of the integrator by using the fact that the signal is delayed by a

clock period T in the time domain. The equation in z-domain results in the following equation.

$$v_0(z)(1-z^{-1}) = \frac{C_S}{C_i}\left(v_i(z).z^{-1} - v_2(z).z^{1/2}\right) \quad (6)$$

The transfer function of the DAI with the output connected to the Φ1 switches is given by [4],

$$v_0(z) = \frac{C_s}{C_i}.\frac{\left(v_1(z).z^{-1} - v_2(z).z^{1/2}\right)}{1-z^{-1}} \quad (7)$$

Note that if v2 (*z*) =VCM, this equation can be written as [4],

$$v_{out}(z) = \frac{C_s}{C_i}.\frac{1}{1-z^{-1}}.v_1(z) \quad (8)$$

The equation above is used for the integrator in the design of modulator. Choosing C_S = 1 pF and CI = 2 pF, the gain of the integrator becomes 0.5. Here the gain is kept less than 1 to make the first order modulator loop stable and also to avoid the integrator from saturating. The capacitance ratio is important than the individual values of the capacitors. Even smaller capacitances can be used, but to avoid charge leakage problem they are taken high.

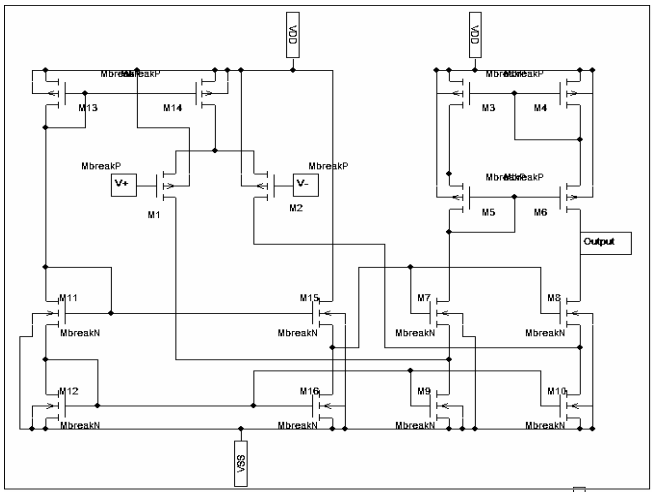

Fig. 2. Circuit design of the folded cascode op-amp

Therefore, the folded cascode (FC) amplifier is a good choice for the amplifier design as a wide-band, fast settling operational amplifier in today's deep sub-micron CMOS technology. In particular, it provides high gain, easier frequency compensation. Moreover, unlike the two stage op-amp it does not suffer from frequency degradation of the power supply rejection ratio. The folded cascode op-amp design is shown in Fig. 3. The differential in Fig. 3 is formed by p-channel MOSFETs, M1 and M2, whereas M3-M6 and M7-M10 are p- and n-type cascode load devices for the op-amp. The transistors M15 and M16 are to perform level shift to bias transistors M9 and M10. Finally, the op-amp is simulated using PSPICE simulator. The characteristics of the op-amp, such as the DC gain and slew rate are found to be 65 dB and 3.7 V/μs, respectively. The approximate gain bandwidth is found to be 40 MHz, whereas the input offset is 0.276 mV.

4. COMPARATOR DESIGN

The architecture selected for this comparator is the one with n-channel MOSFET as input driver, which are the transistors M1 and M2 in Fig. 3. If the output of the previous stage in first order modulator, i.e. integrator's output, is greater than the reference voltage then the comparator has to give an output of '1'. If the integrator output is less than the reference voltage, then the output of the comparator should be '0'.

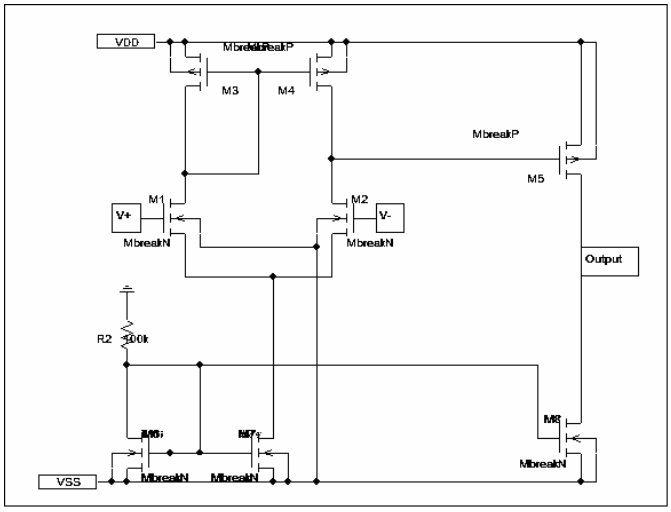

Fig. 3. Comparator design with N-channel input driver

5. 1-BIT DAC DESIGN

The present 1-bit digital-to-analog converter has two reference voltages as shown in Fig. 4, such as a positive reference voltage of +VREF and a negative reference voltage of -VREF. The corresponding voltages of +VREF and -VREF are +2.5 V and -2.5 V, respectively.

There are following two cases:

Case 1: If the digital input = '1', then DAC output = +VREF

Case 2: If the digital input = '0', then DAC output = -VREF

The DAC here is designed using transmit ion gate, which are different topologies that are used in integrator and comparator.

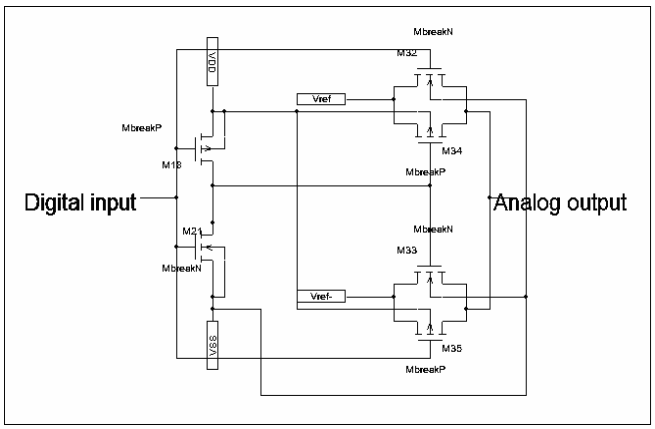

Fig. 4. Circuit diagram for 1-bit DAC

6. SIMULATION RESULT

The modulator receives an input of a 1.5 kHz sine wave of peak-to-peak amplitude of 2 V. The clock input is a square wave at 250 kHz frequency and amplitude of -2.5 V to +2.5 V. The power supply voltages are given as VDD (+2.5V) and VSS (-2.5 V). The simulated result is shown in Fig. 5.

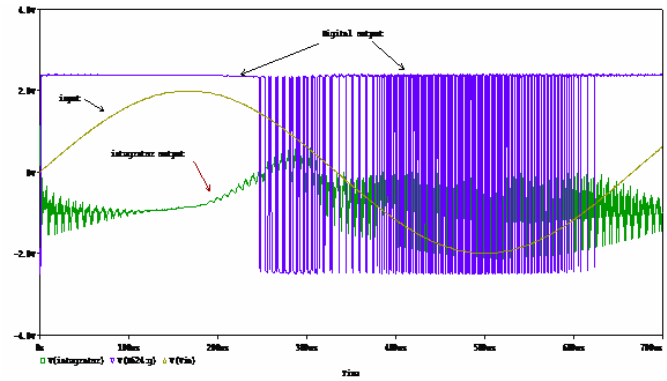

Fig. 5. Simulation result of first order sigma delta modulator

From the result, it can be seen that the digital output is different with the theoritical output, but the characteristics of the modulator still follows the trend. The main cause for this output may due to the integrator. As stated earlier, the integrator is the critical path of the modulator and the function of integrator is used to sum up the input signal with the quantization noise, therefore the non-idealities effect the output result. Besides, the integrator is formed by the RC circuit, therefore the output signal will also be effected by the uncompensated capasistor value.

7. CONCLUSIONS

A first order delta modulator with 8 bit resolution has been designed using SC intergrator with folded cascode op-amp, n-channel MOSFET input comparator and 1-bit DAC using transmition gate of 65 nm CMOS technology. The non-idealities of sigma delta modulator has been investigated and taken into account, which helps to design the right topology of the first order sigma delta modulator. The non-idealities that have been investigated are clock jitter, thermal noise of the switches, DC gain of op-amp as well as limited slew rate and bandwidth. Basesd on the accounted non idealities, the integrator is designed using folded cascode topology with DC gain of 65 dB, slew rate of 3.76V/µs and gain bandwidth with 40 MHz to minimize the non idealities' effects. Finally, the modulator circuit is designed in PSPICE simulation tool with convincing results and can be recommended for practical implimentation.

8. REFERENCES

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