Digital and Analog Computing Circuits

CSE562M: Analog Integrated Circuits

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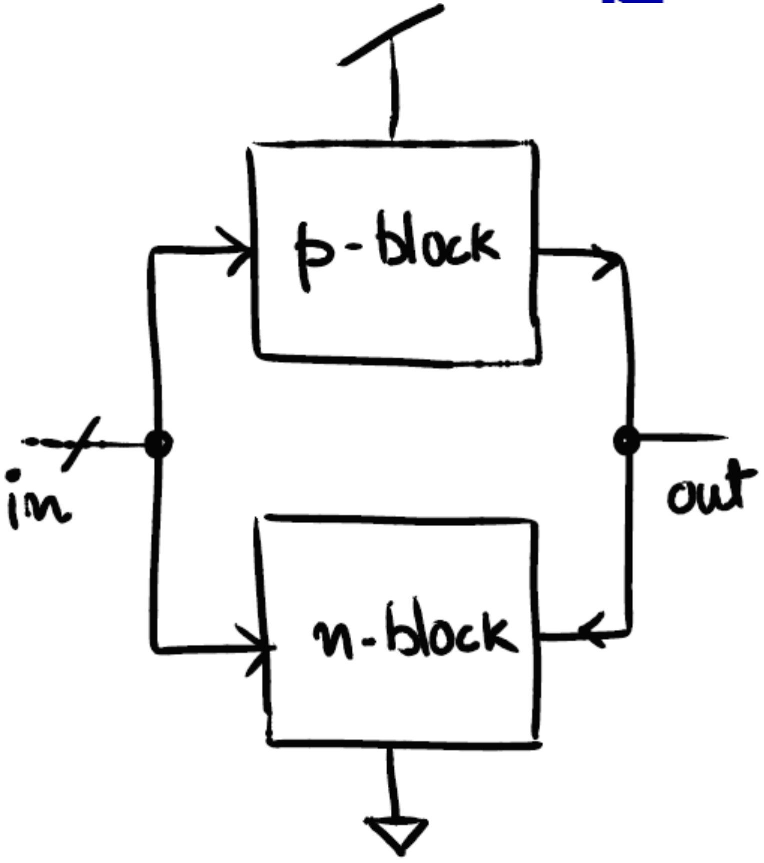
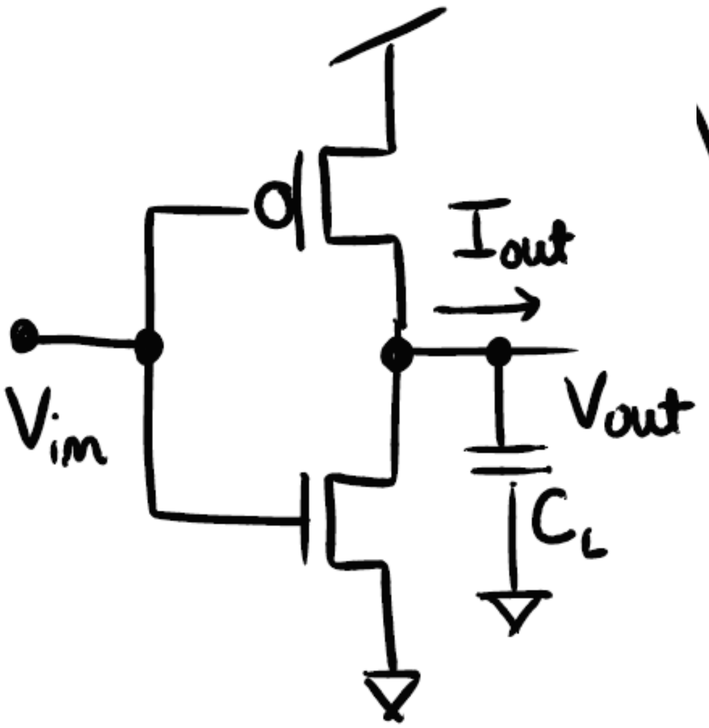
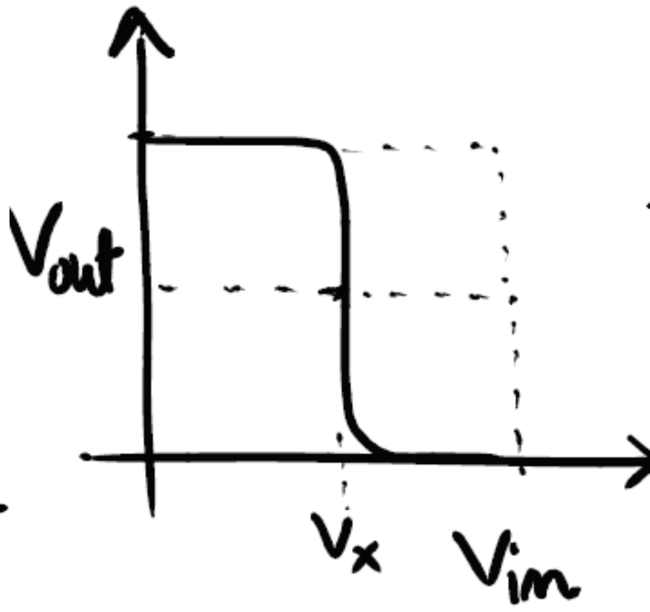
Digital computing circuits

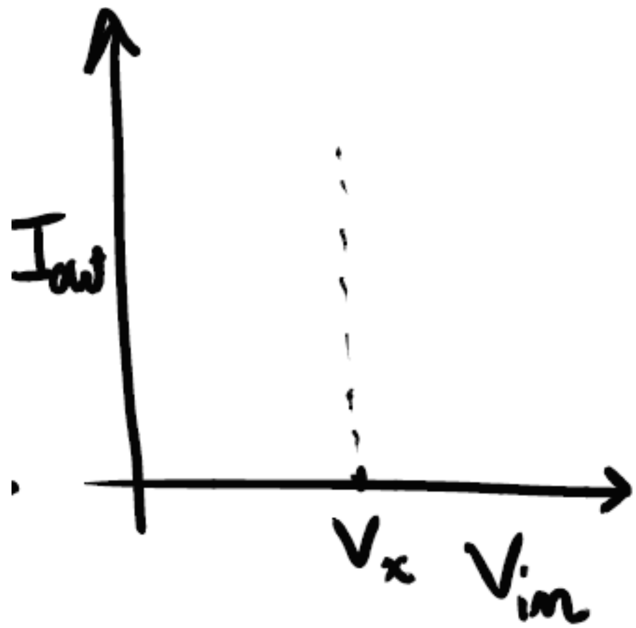
- Complementary logic
- Pass transistor logic
- Dynamic logic
- Sequential logic
- Asynchronous logic
- Adiabatic logic

Complementary logic







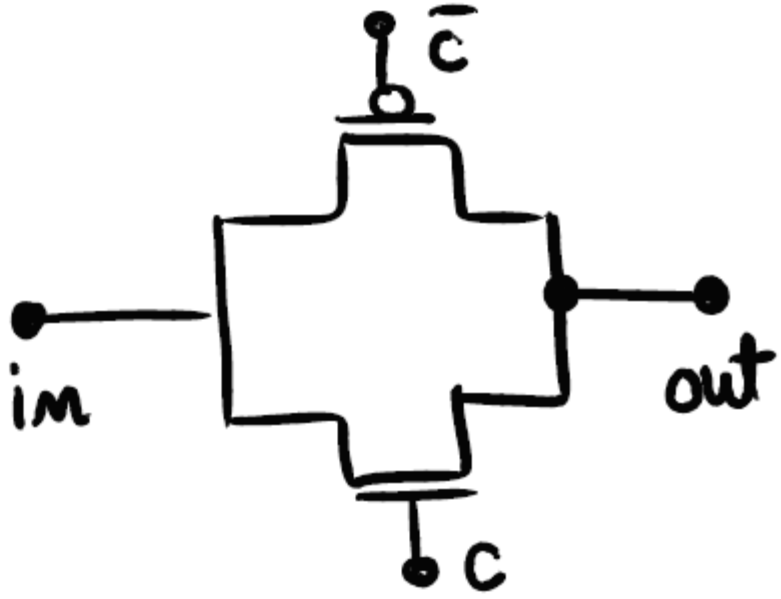


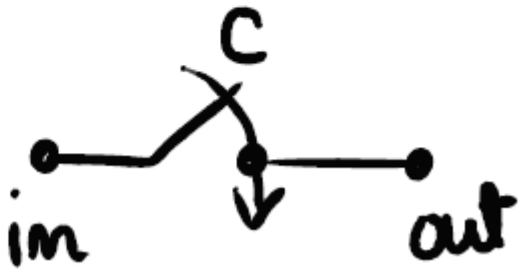
- Simplest complementary logic implementation

Power-speed trade-off

- Power Dissipation
  - Static Dissipation – Sub-threshold leakage
  - Dynamic Dissipation – $f \times C_L \times V_{dd}^2$
- Speed – rise/fall time $$\tau \approx \frac{C_L}{C_{ox}\mu \frac{W}{L} V_{dd}}$$
- Reduce V_{dd} by a factor of 2, Power = ?; Speed = ?
- Reduce C_L by a factor of 2, Power = ?; Speed = ?
- Reduce f by a factor of 2, Power = ?; Speed = ?

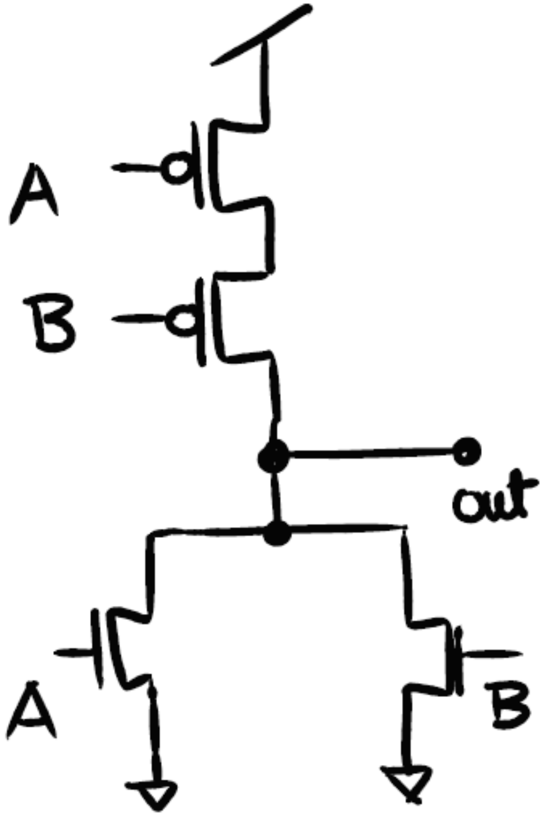
Pass transistor logic: Switch

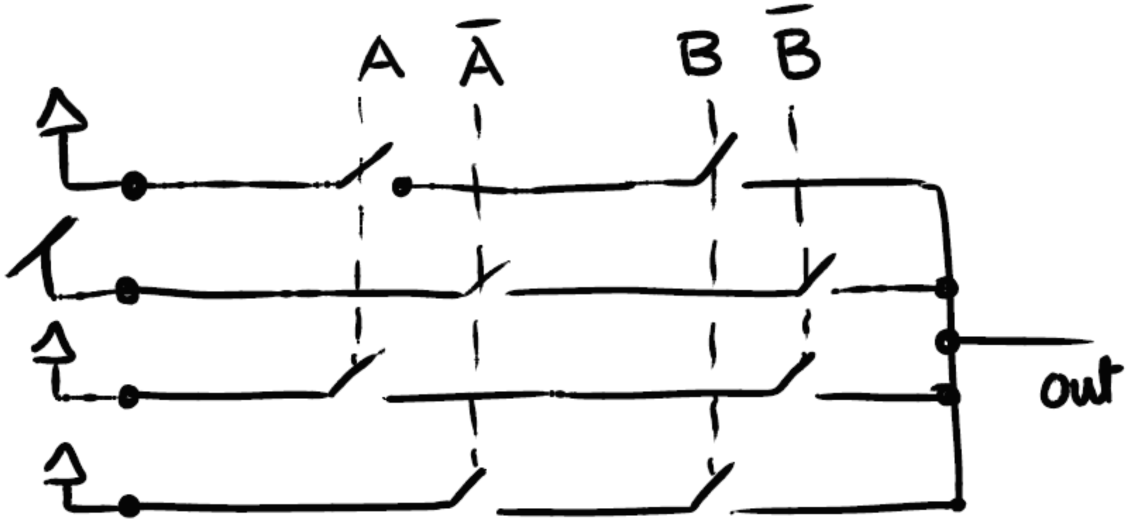




- R-C effect
- Long chains of pass transistors requires buffering.

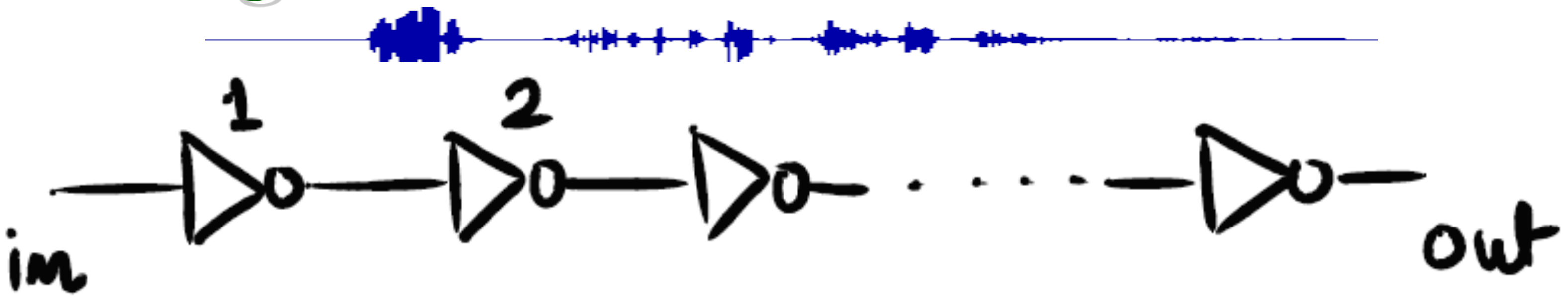
Example: NOR logic



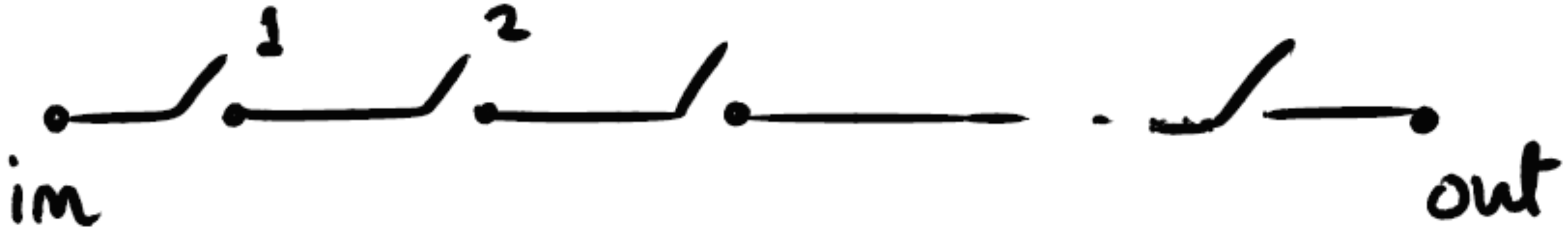


- **Complementary logic**
  - Hi-Z input
  - Low-Z output
- **Pass transistor logic**
  - Low-Z input
  - Low-Z output

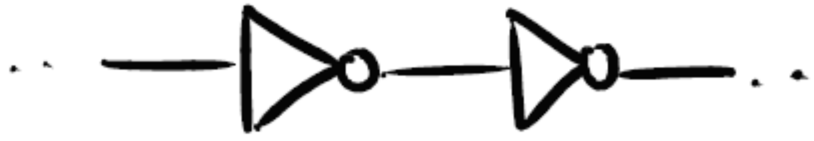
Cascading effect



- Complementary logic: $Delay = N \times \tau_{stage}$

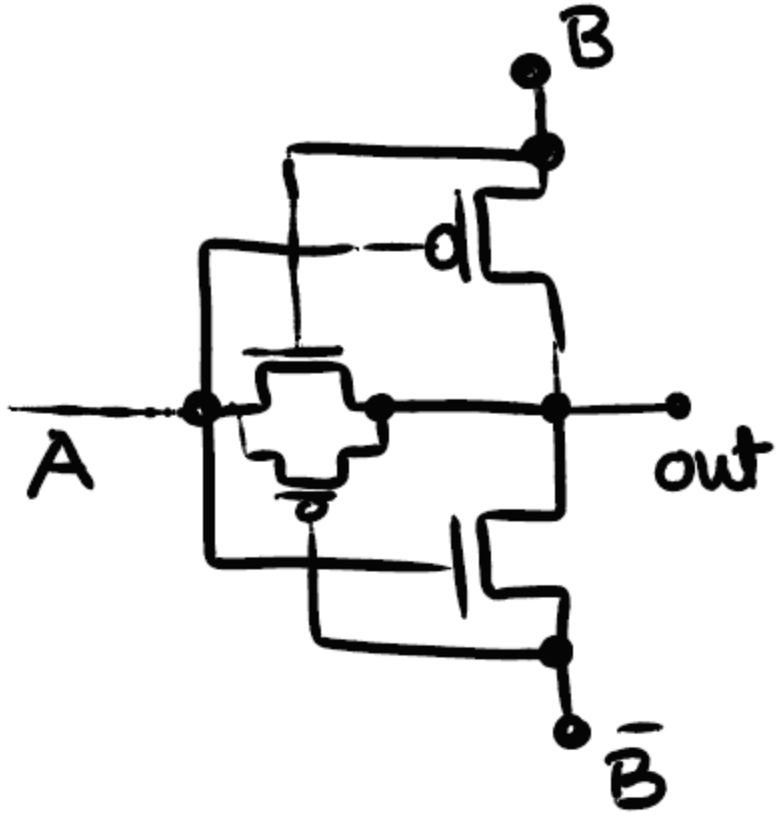


- Pass transistor logic: $Delay = N^2 \times \bar{\tau}_{stage}$
- But: $\tau_{stage} > \bar{\tau}_{stage}$
- Introduce buffers every four stages of pass transistor logic.



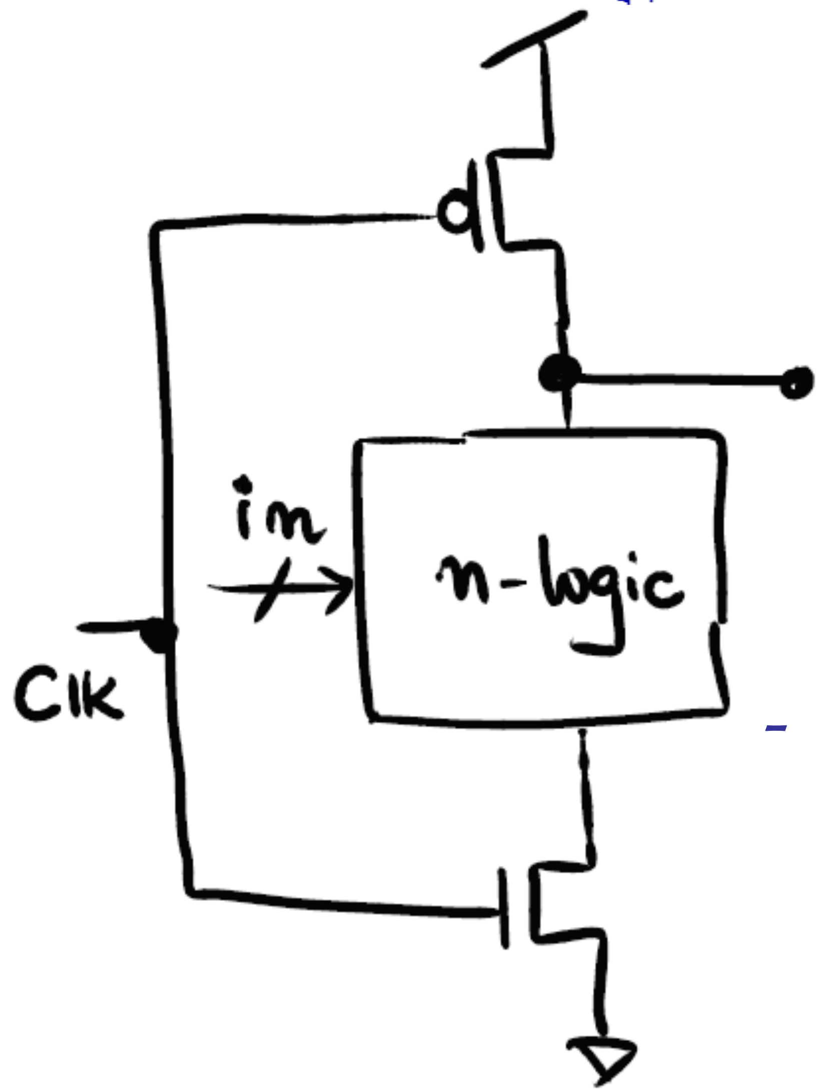
Hybrid logic

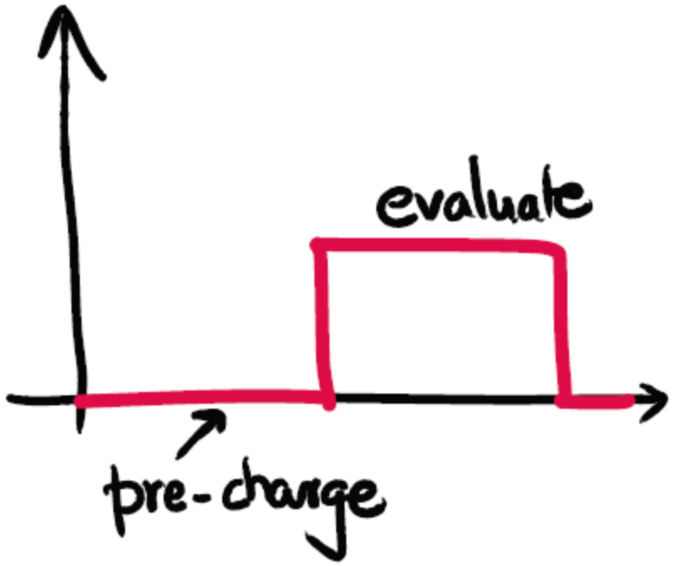
- What logic does this circuit implement ?



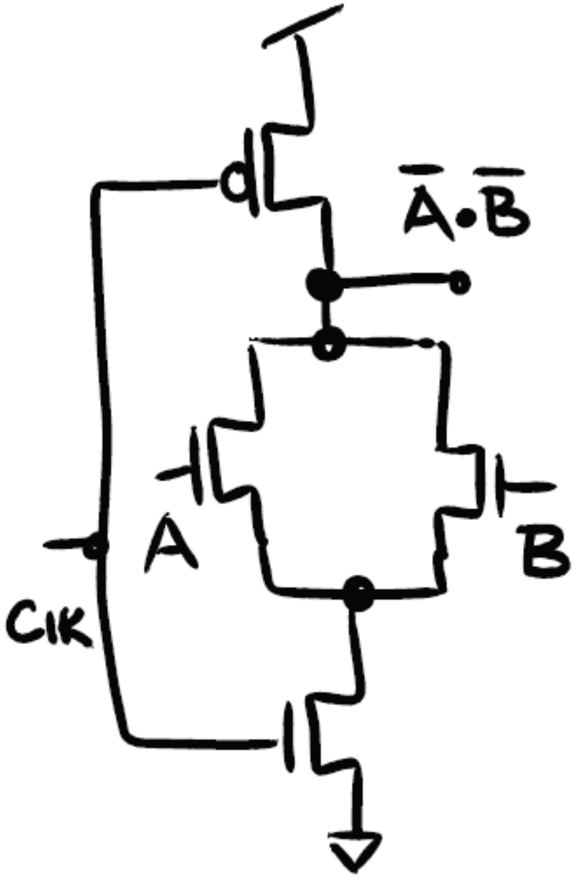
- Is this a better logic than complementary and pass transistor logic ?

Dynamic Complementary logic

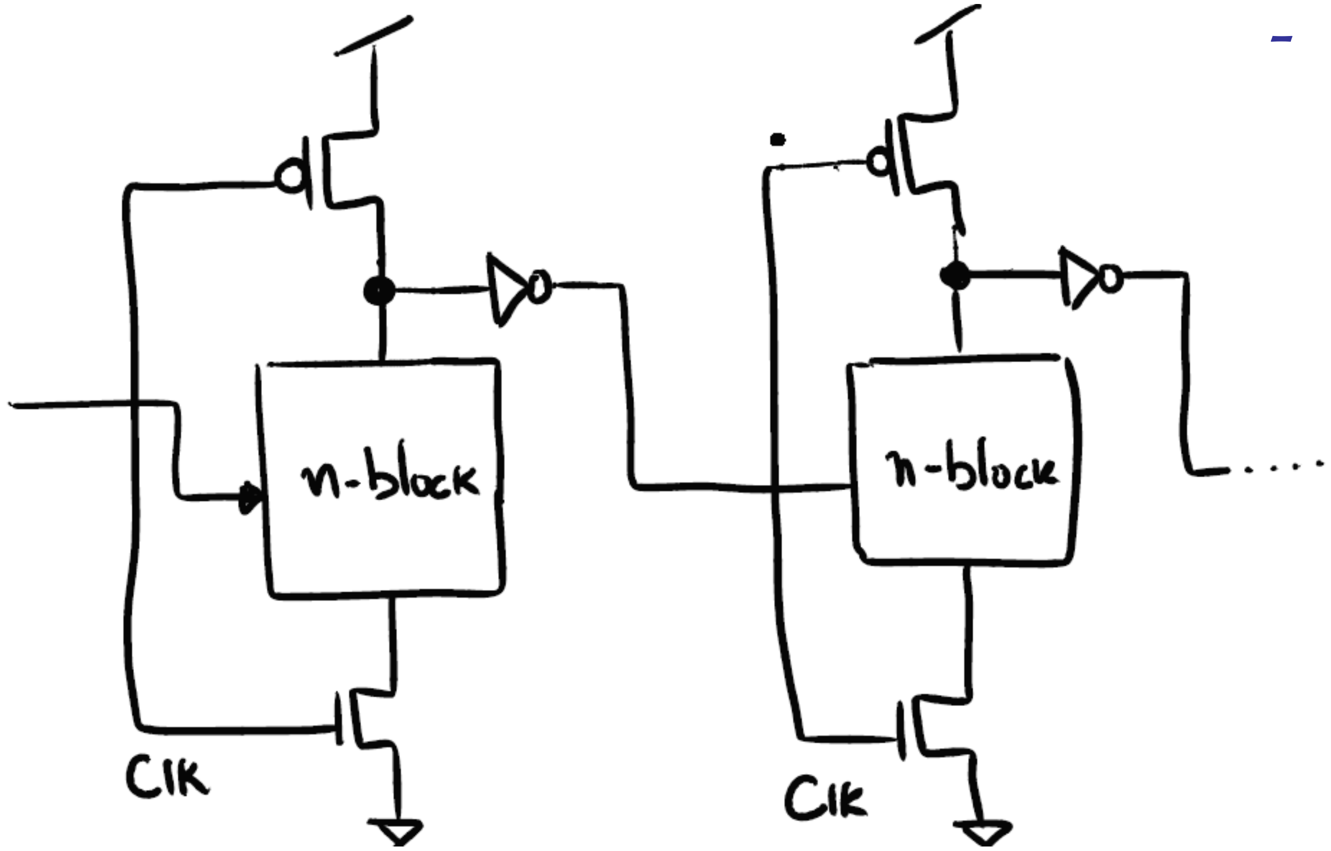




- Inputs and outputs are enabled only during the evaluate phase of the clock.

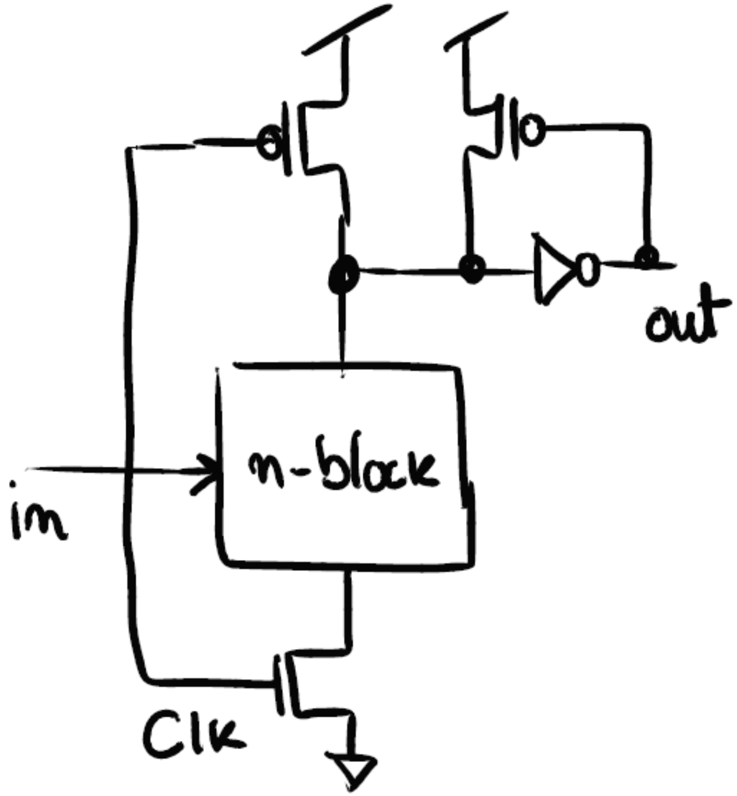


CMOS Domino logic



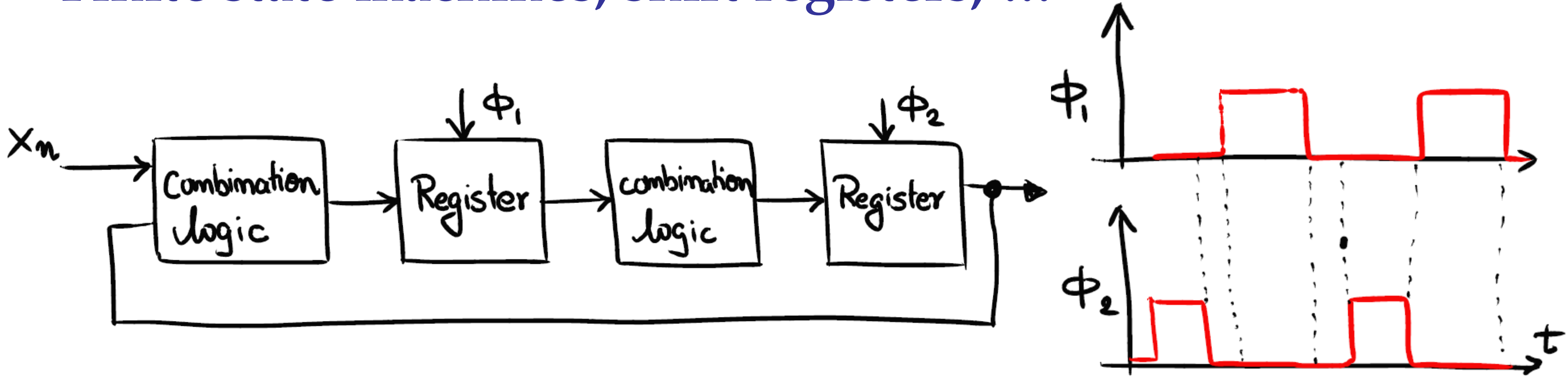
- Can be used to implement cascaded logic functions.

- Use positive feedback to speed up evaluate phase.

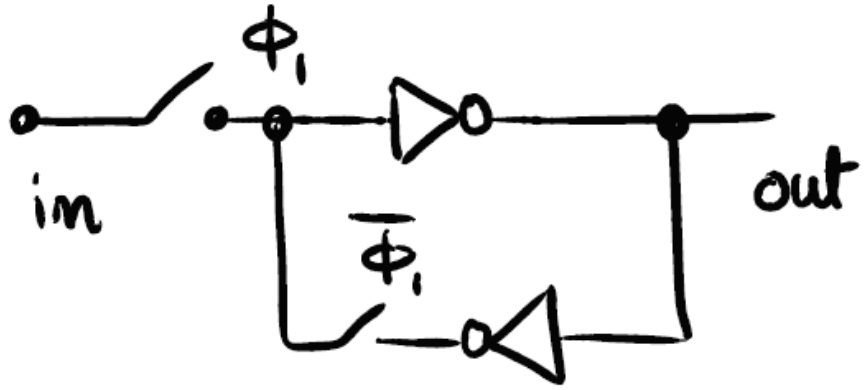


Sequential logic

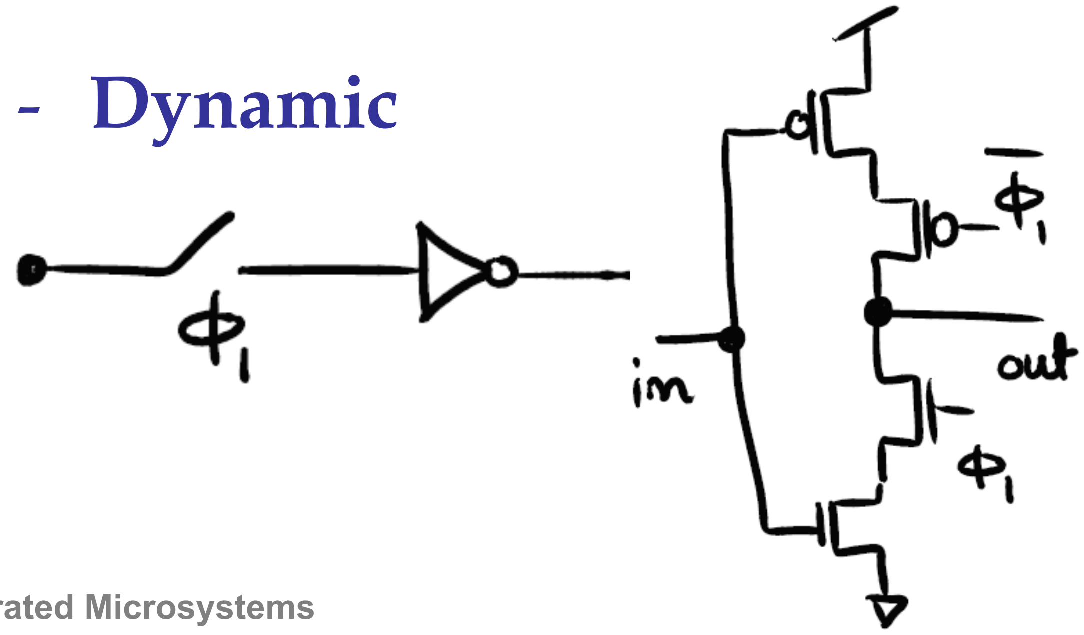
- Finite state machines, shift registers, …



- Static

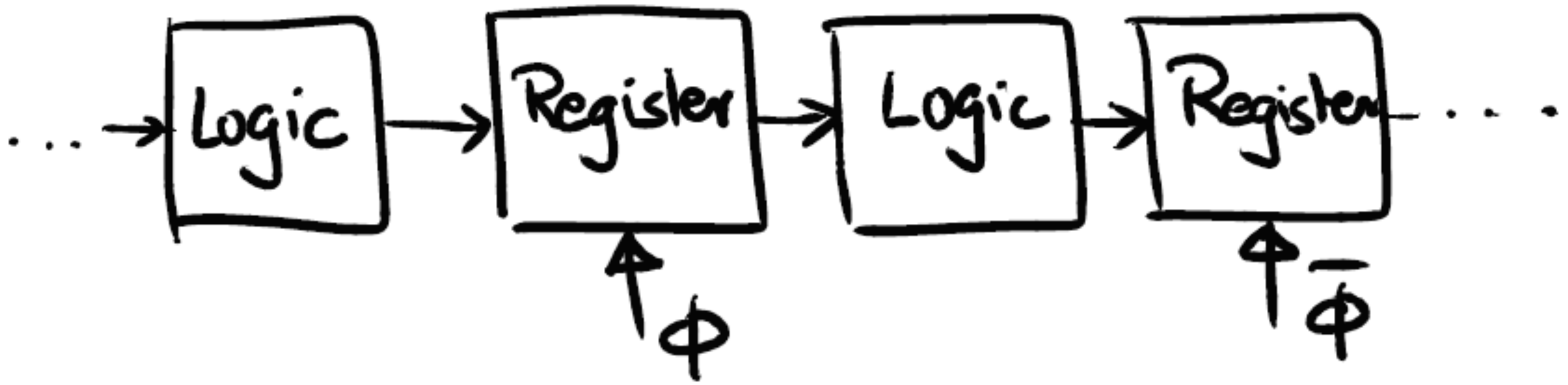


- Dynamic

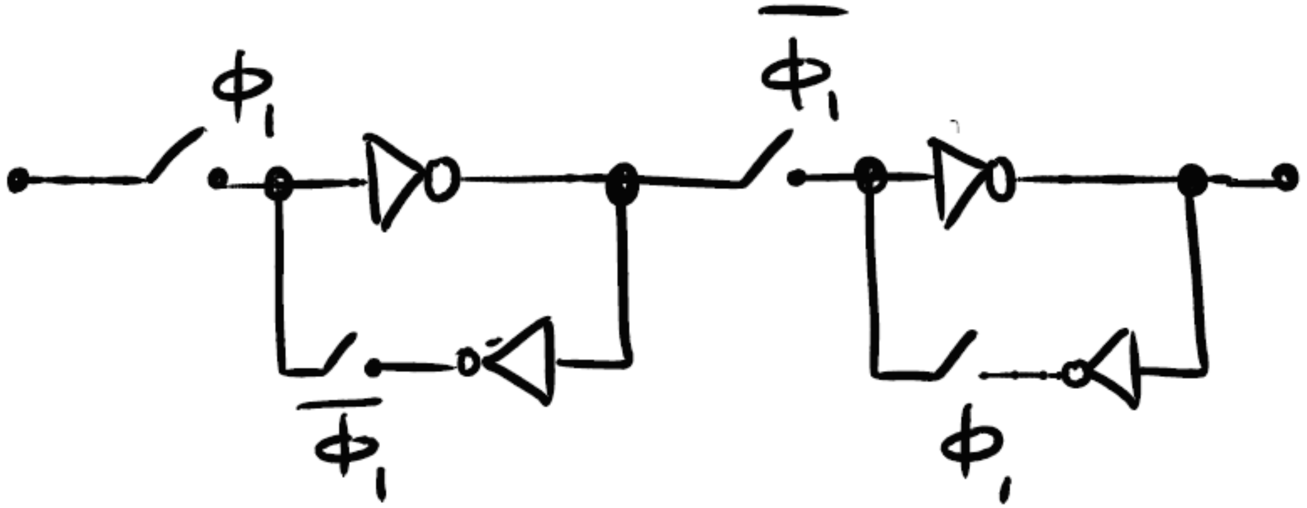


Pipelining

- Increasing throughput by sequential logic decomposition



- Simplest example: Shift register



Analog computing circuits

- **Precision not important**
- **Pattern recognition systems**
- **Ultra-low-power**
- **Ultra-high-speed – where analog-to-digital converters are too power hungry.**
- **Fewer transistors or high computational density**
- **Parallel implementations**
- **Example:** Most biological computations are ``analog" in nature.

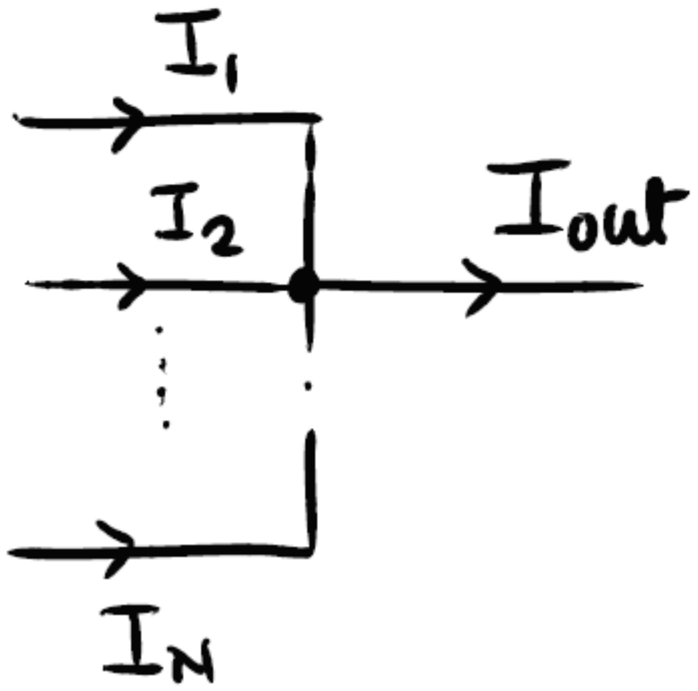
Principles of analog computing

- Represent numbers as physical quantities – current, voltage, impedance, charge, time, ratios,…
- Use the physics of the device for implementing mathematical functions.
- User conservation laws to achieve scalability and portability.

Analog adders

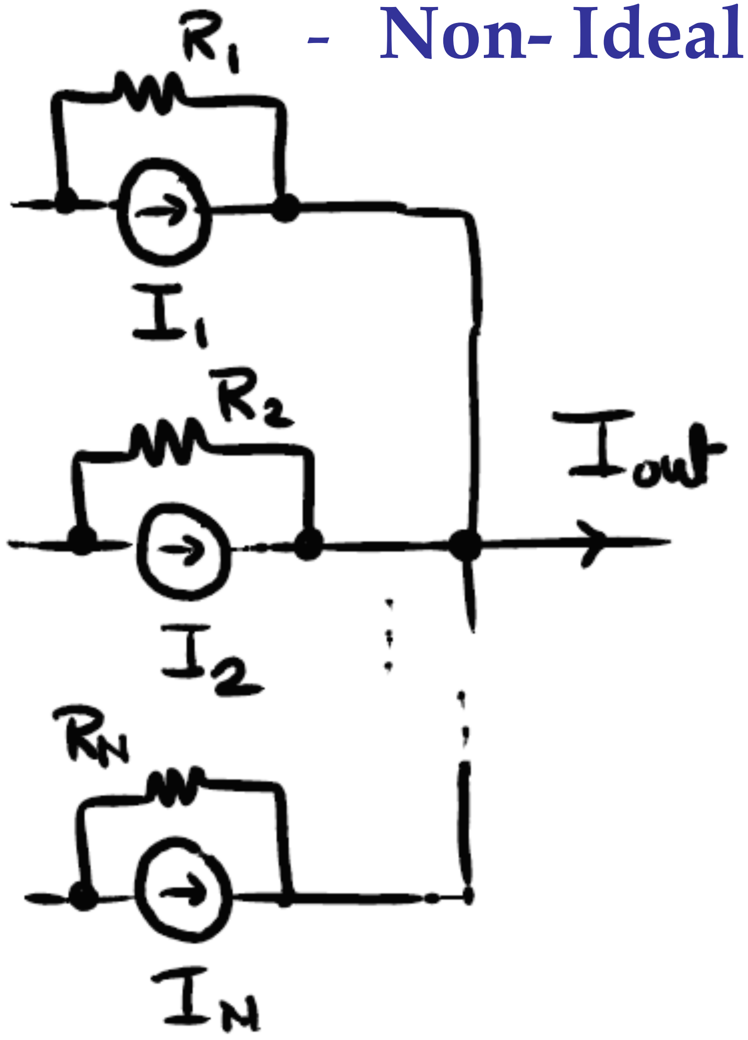
- Conservation of current or charge.

- Ideal



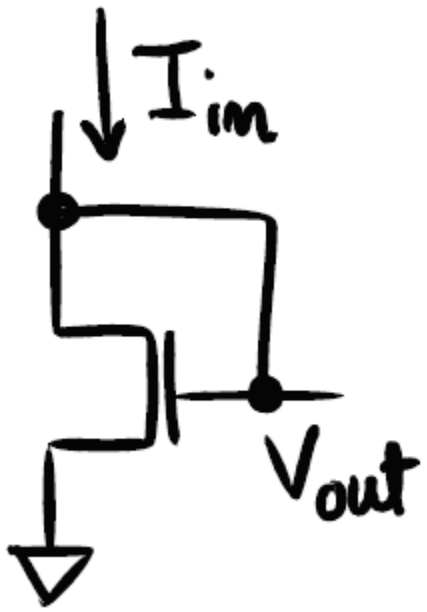
$$I_{out} = \sum_{k=1}^{N} I_k$$

- Non- Ideal



Single transistor as a computer

- Sub-threshold: $I_d \propto \exp\left(\frac{\kappa V_G}{U_T}\right)\exp\left(\frac{-V_S}{U_T}\right) \approx \exp\left(\frac{V_{GS}}{U_T}\right)$
- Exponential function ``practically" for free.



- What function does this circuit implement where I_{in} is the input ?
- What happens if the transistor is biased in above threshold ?
- Can we ignore the effect of the drain terminal ?
- What is the disadvantage of such implementation ?

Representations

- **Voltages:** Easy to distribute but requires dissipates more energy. Lower dynamic range

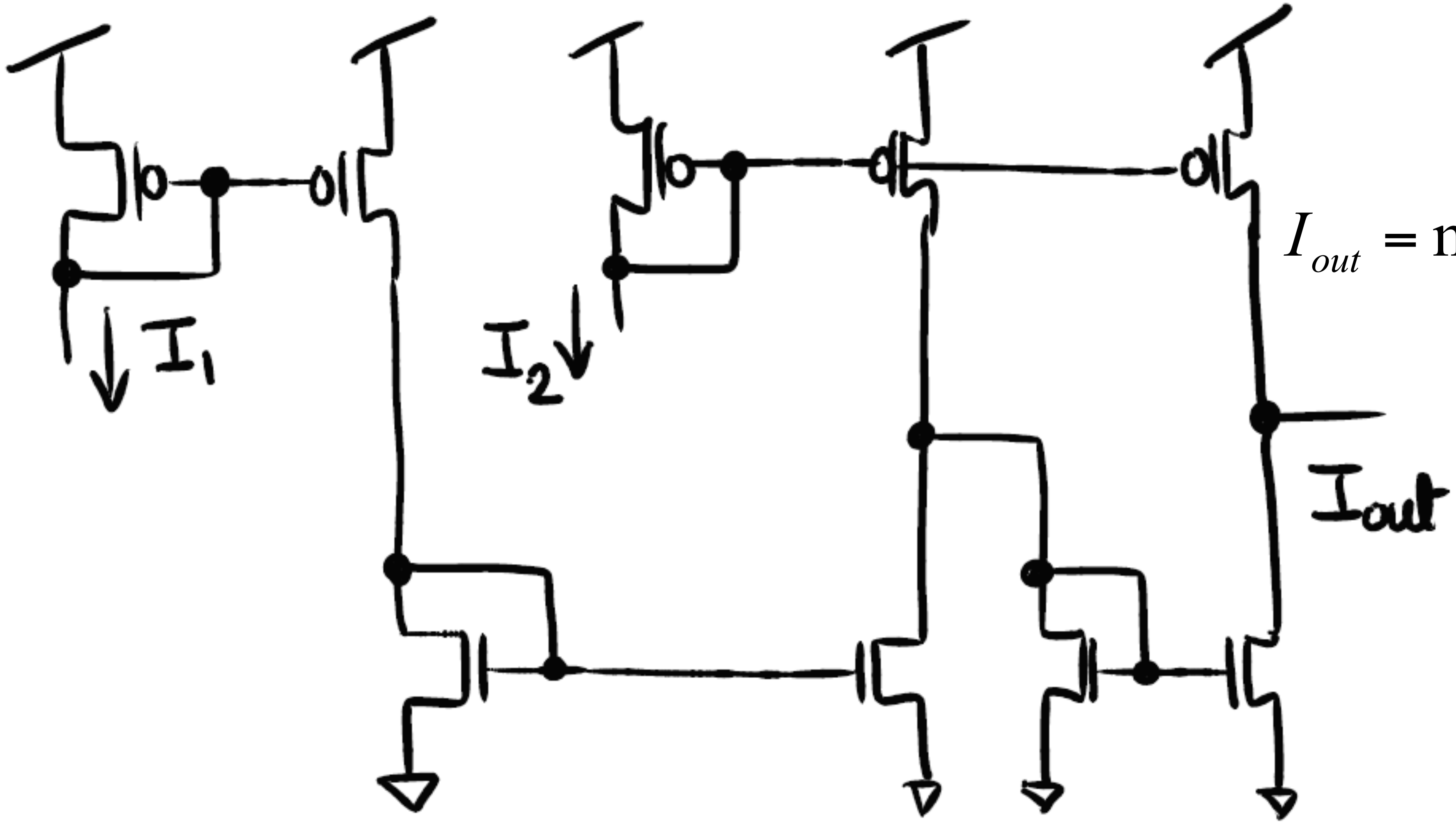
- **Current:** Easy to sum but difficult to distribute. Higher dynamic range. Sub-threshold current: 100fA – 100nA.

- **Charge:** Best only for linear functions – even charge-mode multiplication is complicated.

- **Time:** Easy to transmit and is more robust – but difficult to compute with (Biological computation is time-based)

Scalable Analog Computing

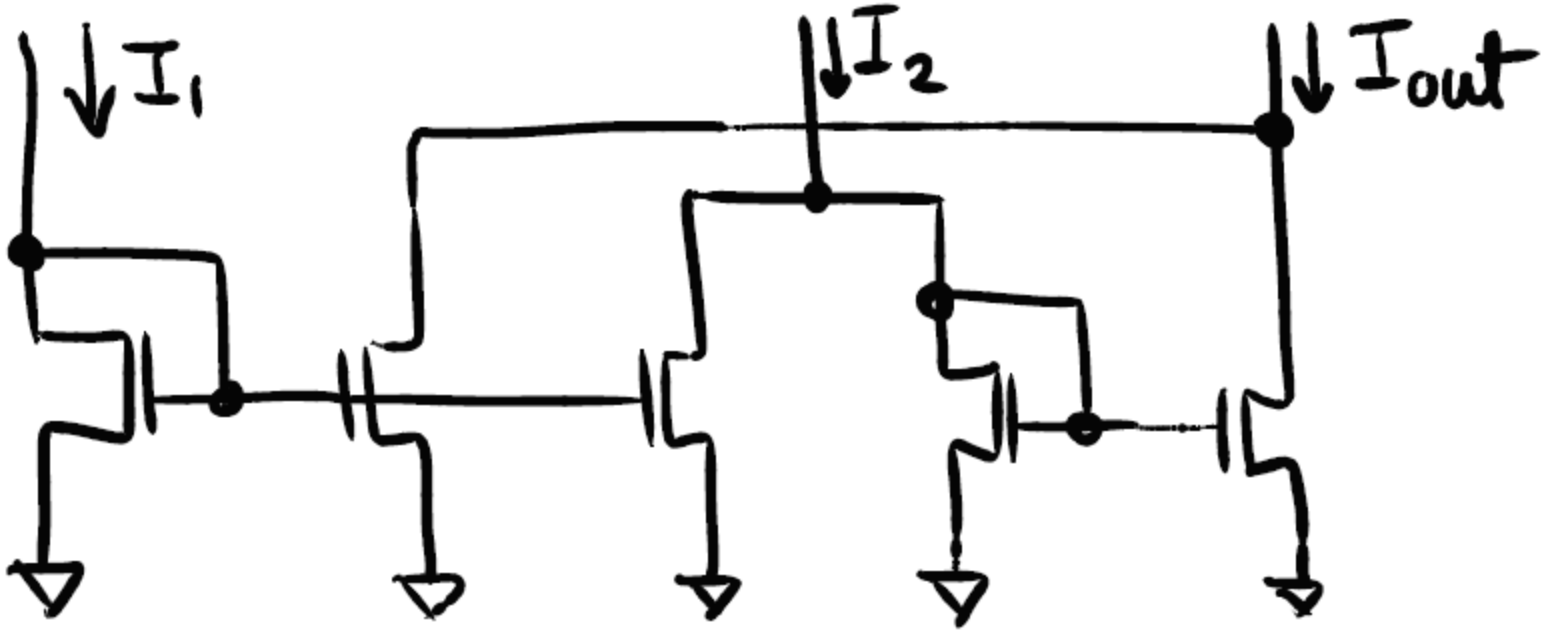
- Only relies of conservation laws: KCL, KVL or charge conservation.



$$I_{out} = \min(I_1, I_2)$$

Scalable Analog Computing

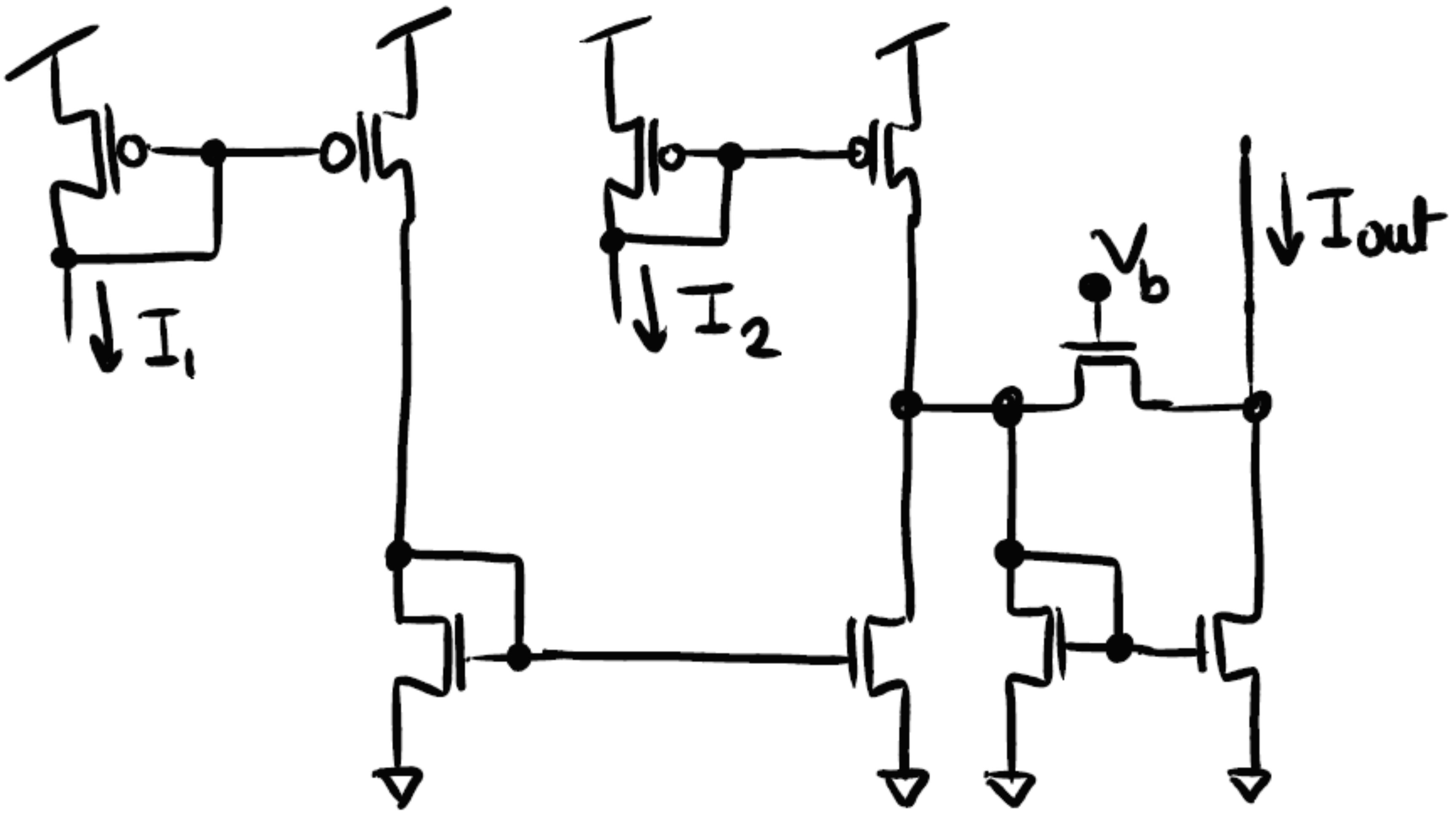
$$I_{out} = \max(I_1, I_2)$$



- How to implement $I_{out} = |I_1 - I_2|$

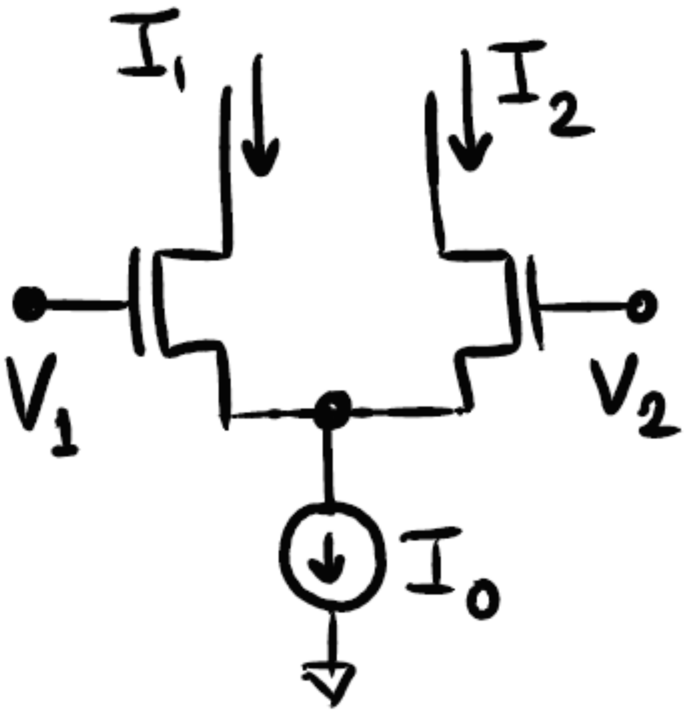
Scalable Analog Computing

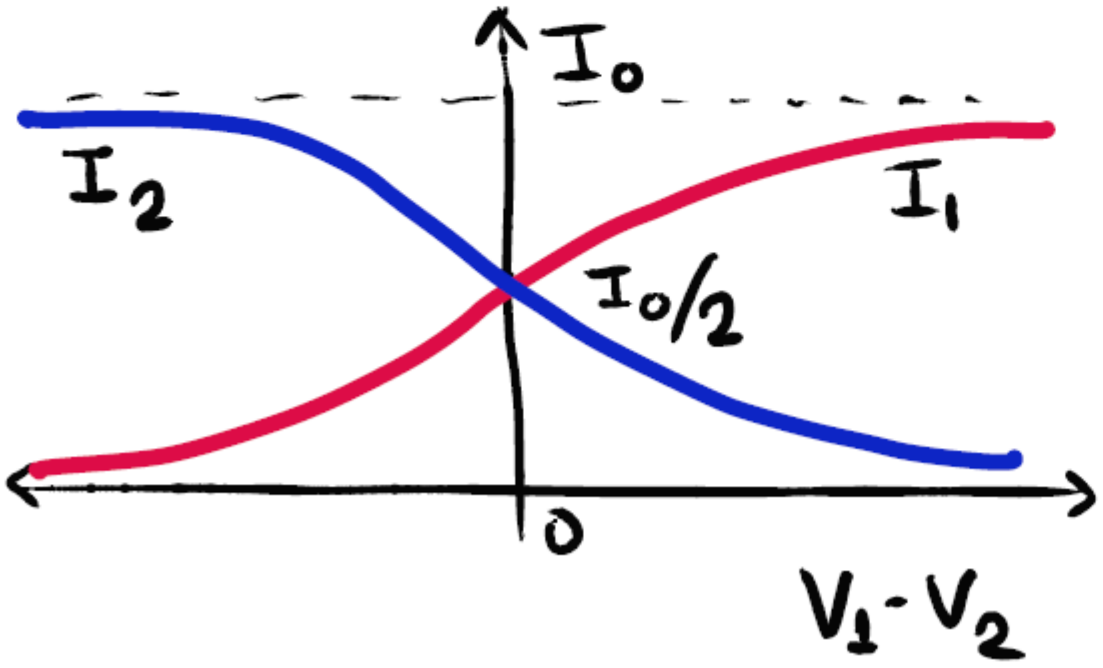
- What function does this circuit implement ?



How to build an analog search engine ?

Compressive functions: Sigmoid or Tanh

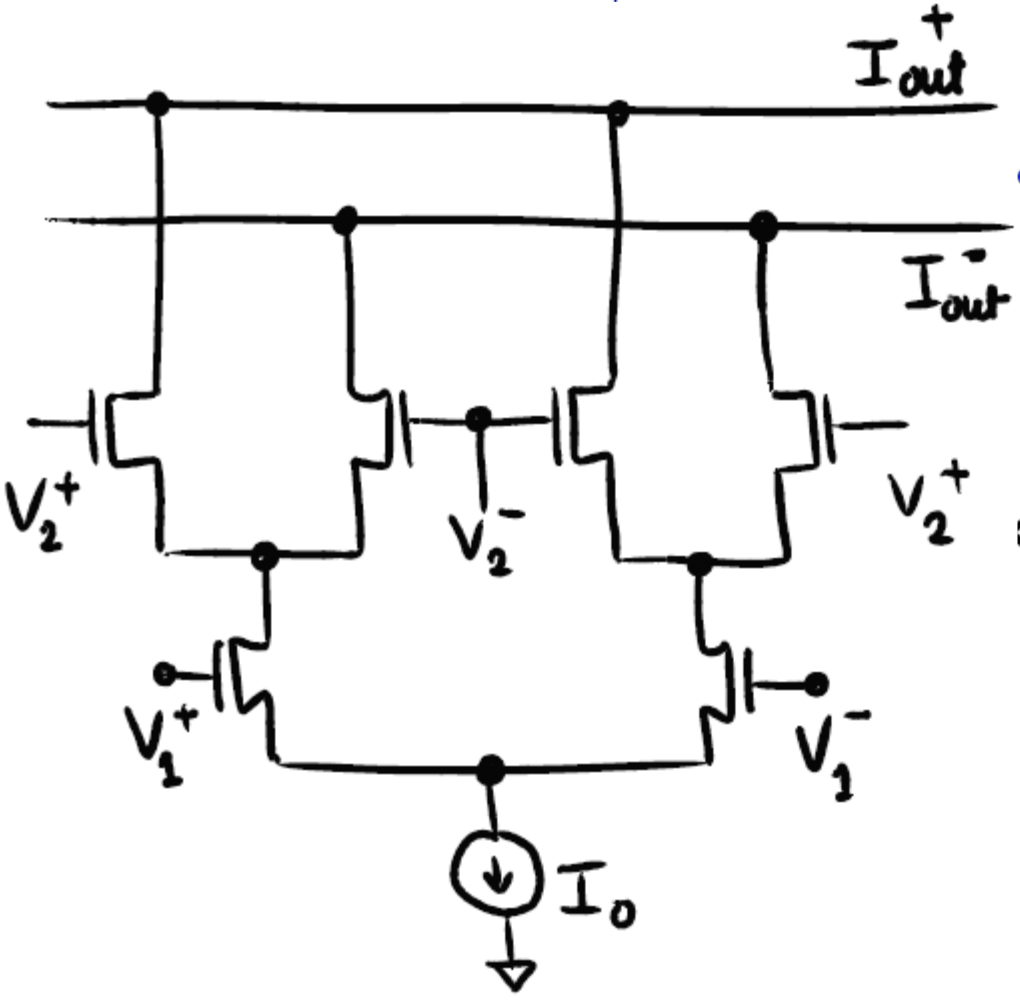


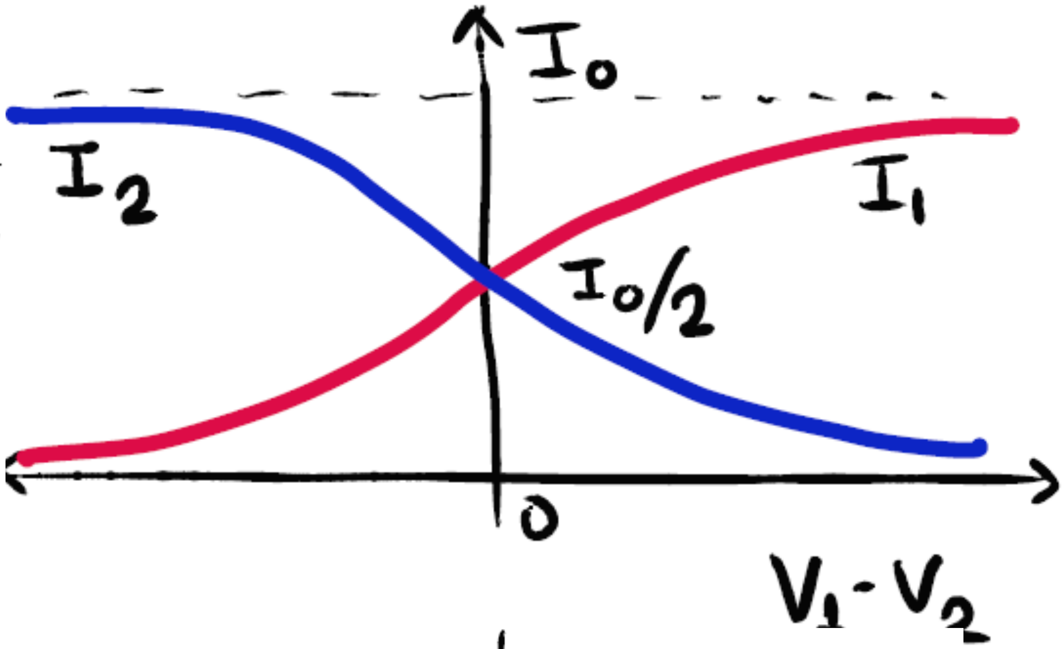


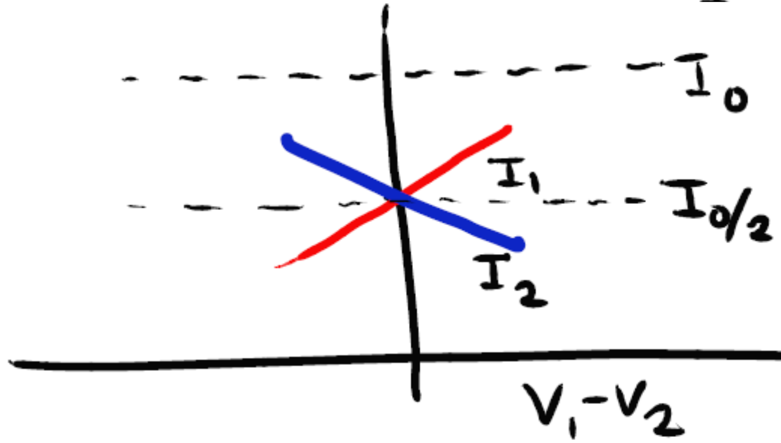
- **Transistors biased in sub-threshold.**

$$I_1 = I_0 \frac{1}{1 + \exp\left(-\kappa \frac{V_1 - V_2}{U_T} \right)}$$

Gilbert multiplier



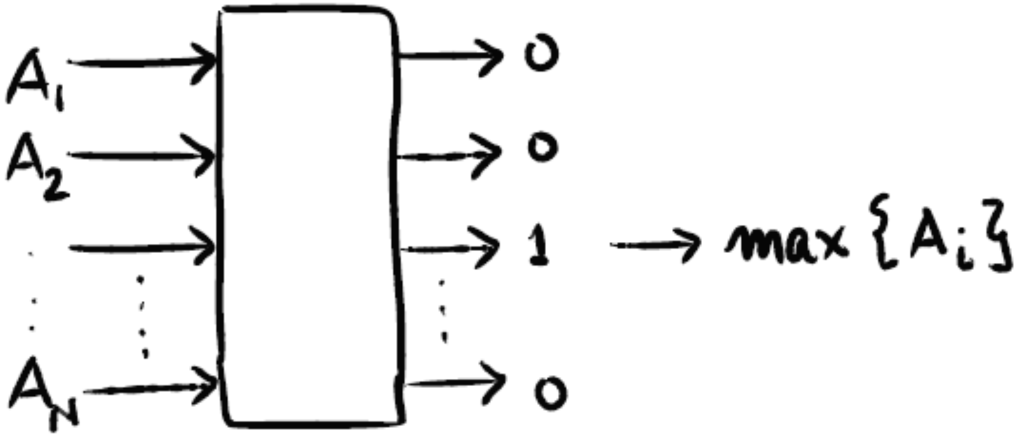


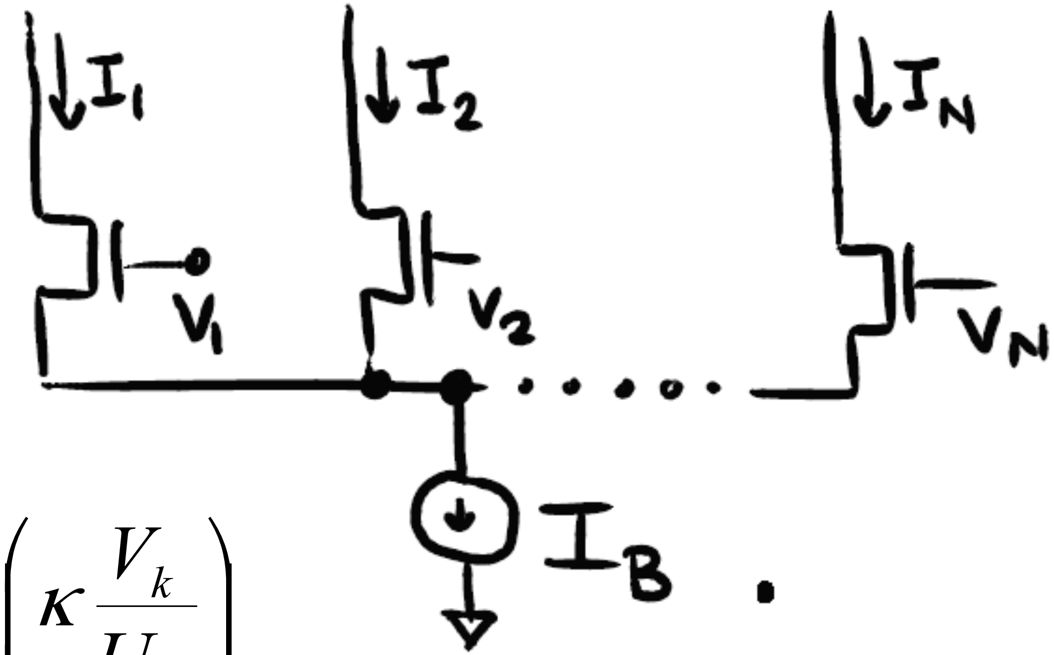


$$I_{out}^+ - I_{out}^- \propto \left(V_1^+ - V_1^-\right)\left(V_2^+ - V_2^-\right)$$

Winner-take-all

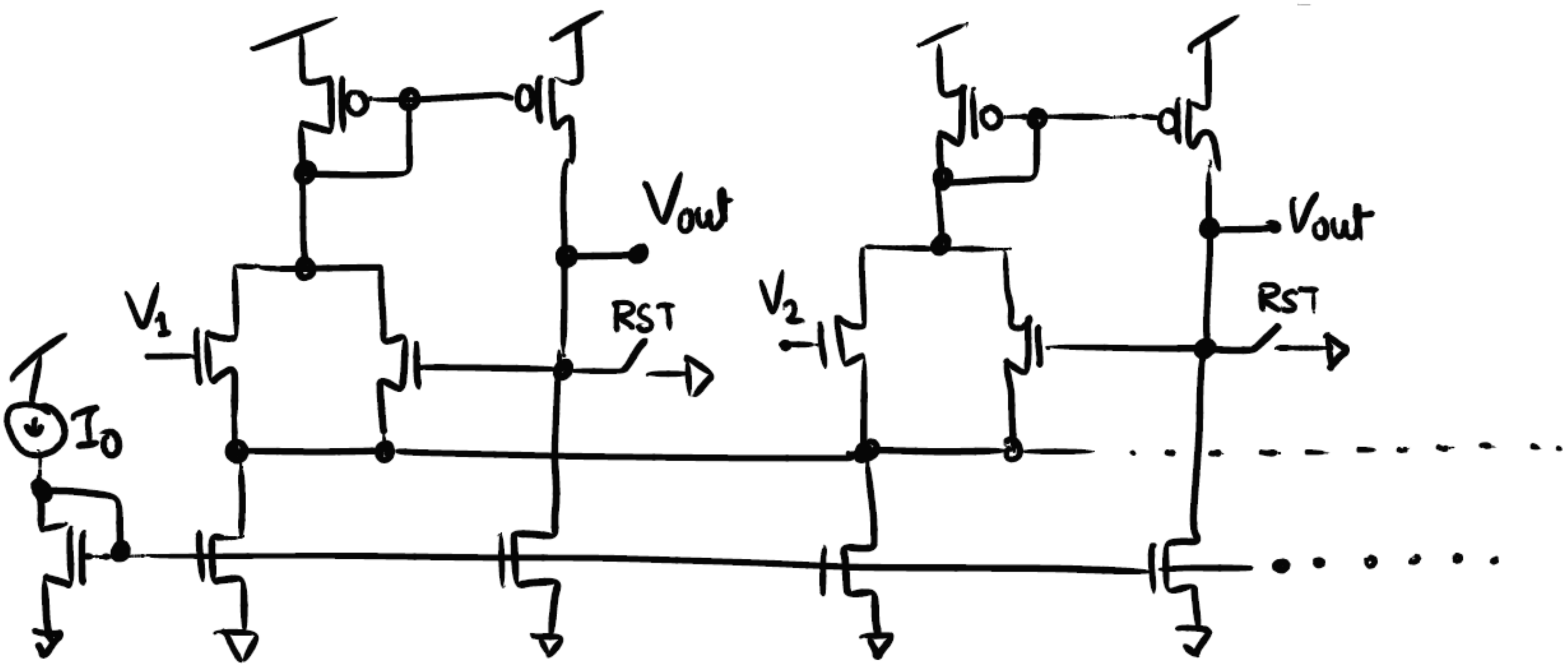
- Only one of the output is high and corresponds to the maximum of the input – digital encoding.





$$I_k = I_B \frac{\exp\left(\kappa \frac{V_k}{U_T}\right)}{\sum_{p=1}^{N} \exp\left(\kappa \frac{V_p}{U_T}\right)}$$

Better Winner-take-all

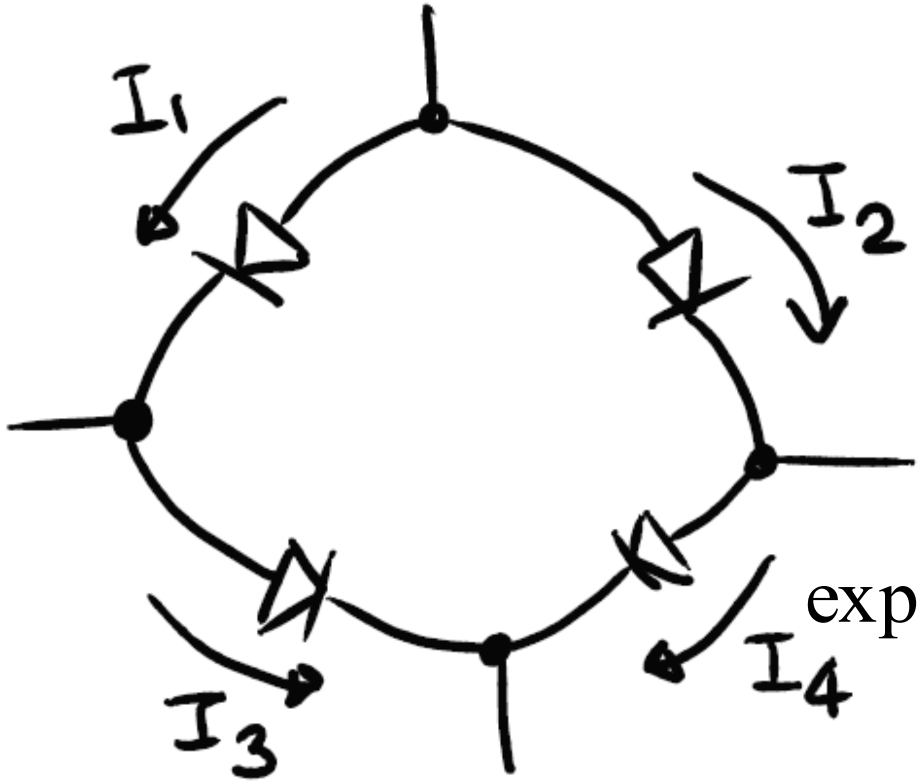


- Implements a parallel search – speed limited by the system time-constant.

Translinear principle

- Applies to circuit elements with a diode type behavior

$$I_k \approx I_S \exp\left(\frac{V_k}{U_T}\right)$$



$$V_1 + V_3 = V_2 + V_4$$

$$\exp\left(\frac{V_1 + V_3}{U_T}\right) = \exp\left(\frac{V_2 + V_4}{U_T}\right)$$

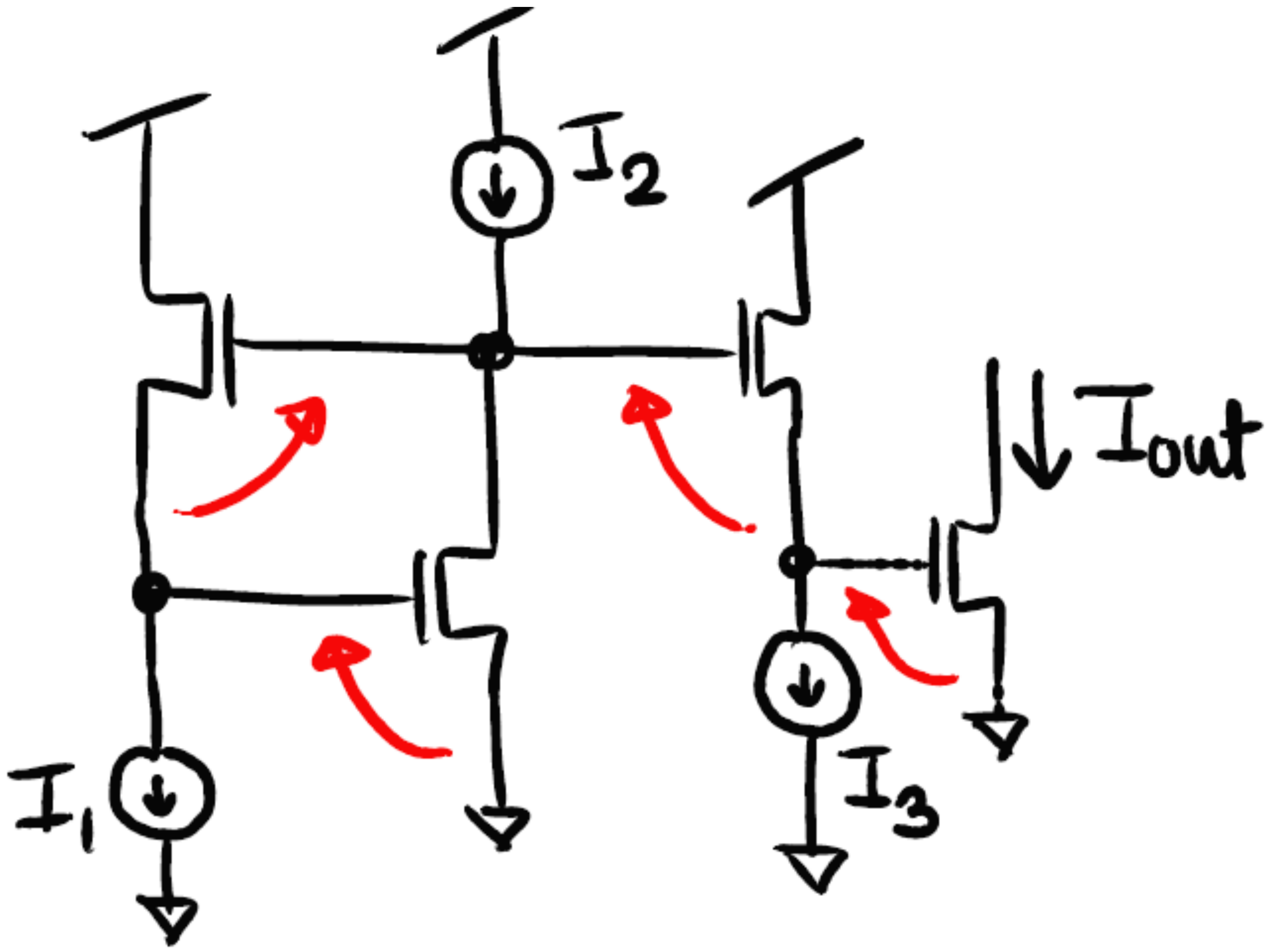
$$\exp\left(\frac{V_1}{U_T}\right)\exp\left(\frac{V_3}{U_T}\right) = \exp\left(\frac{V_2}{U_T}\right)\exp\left(\frac{V_4}{U_T}\right)$$

$$I_1 I_3 = I_2 I_4$$

MOSFET Translinear principle

- Drain current and gate-to-source voltage have a translinear relationship.

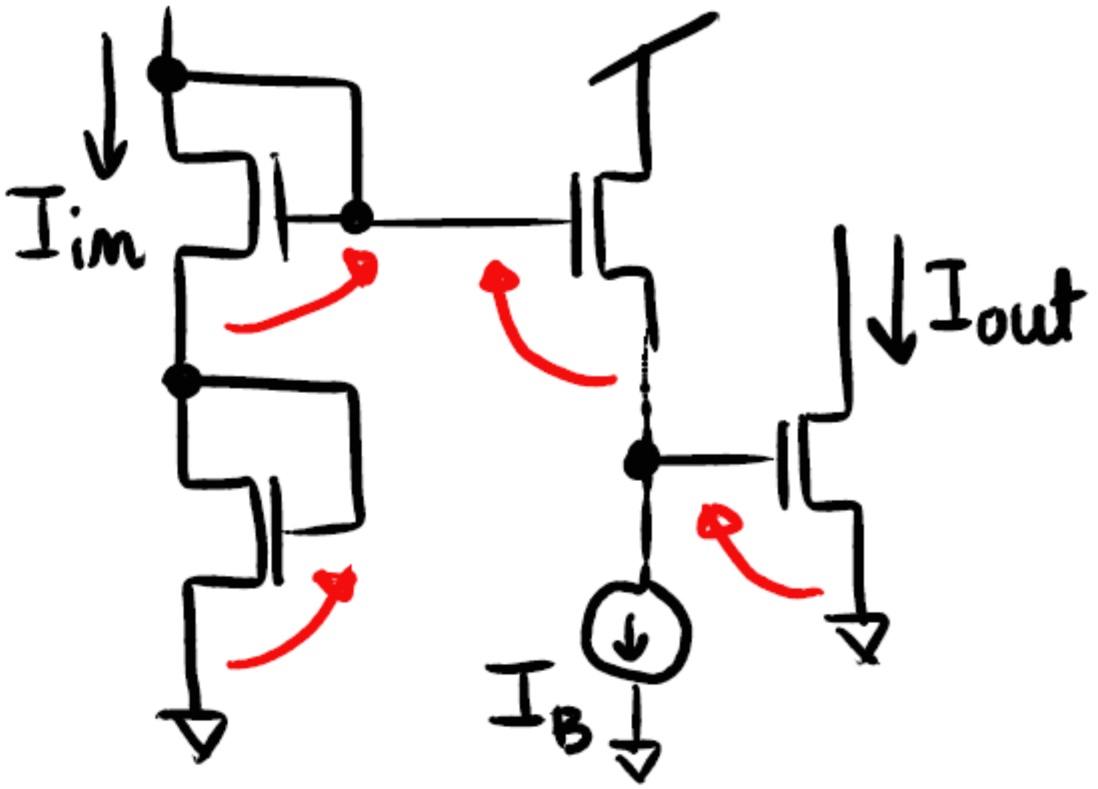
$$I_d \approx I_S \exp\left(\frac{V_{GS}}{U_T}\right)$$



$$I_1 I_2 = I_3 I_{out}$$

$$I_{out} = \frac{I_1 I_2}{I_3}$$

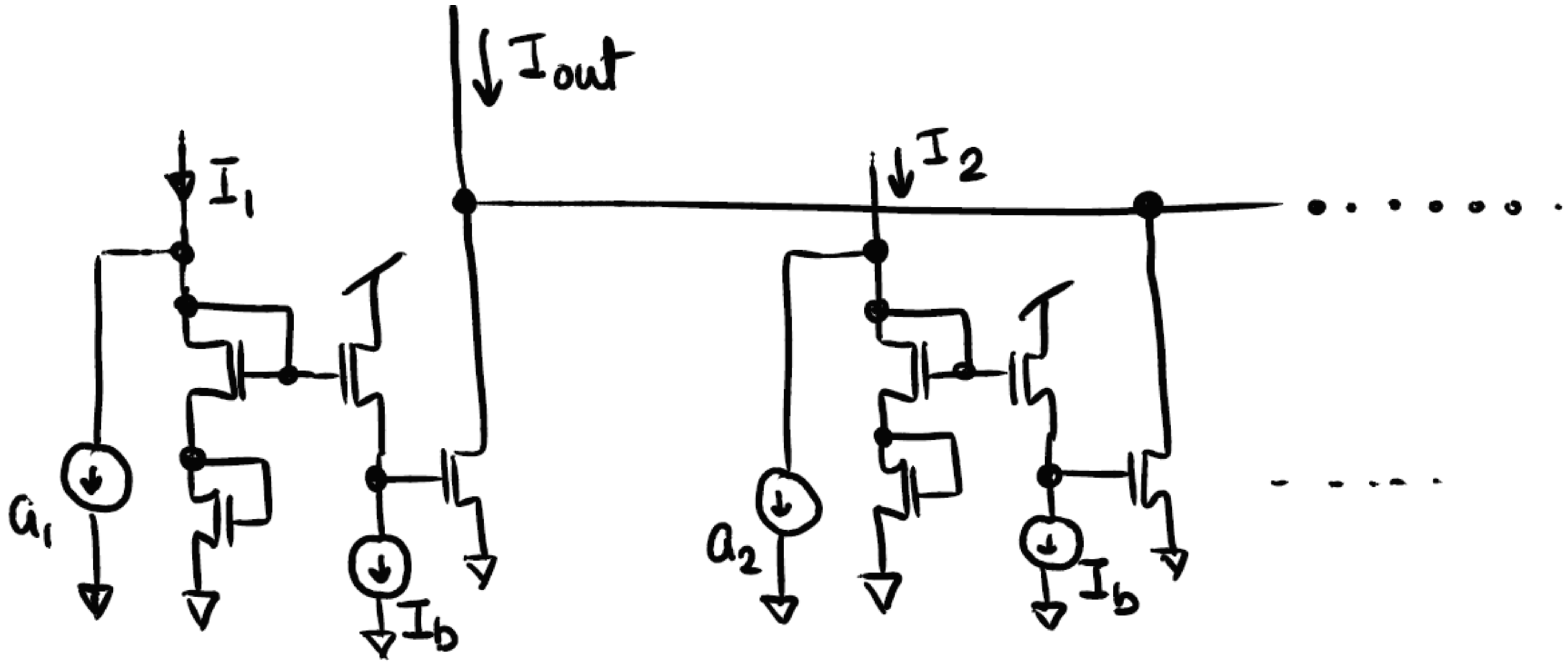
Squaring circuit



$$I_{in} I_{in} = I_B I_{out}$$

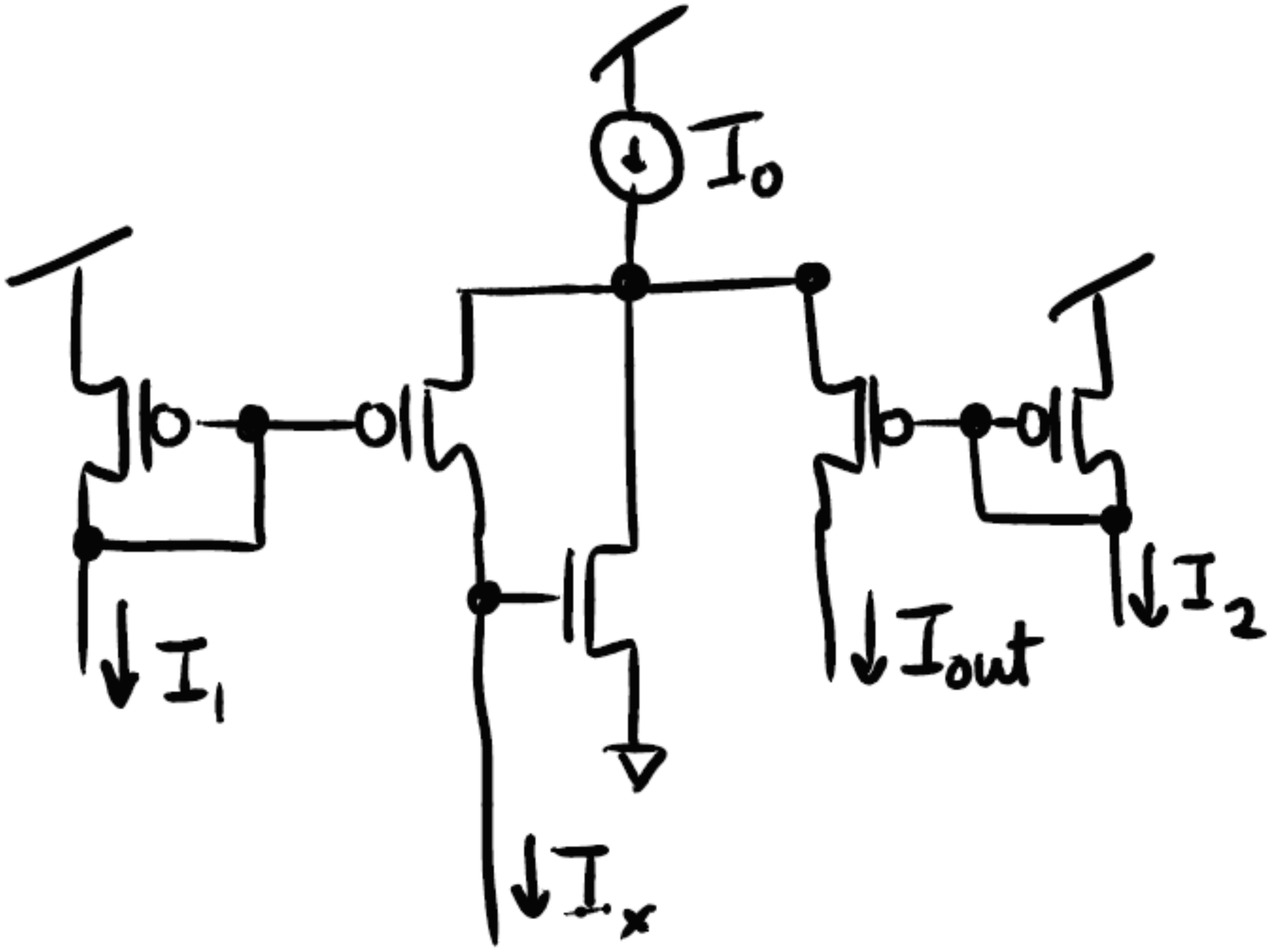
$$I_{out} = \frac{I_{in}^2}{I_B}$$

Yet another analog search engine …



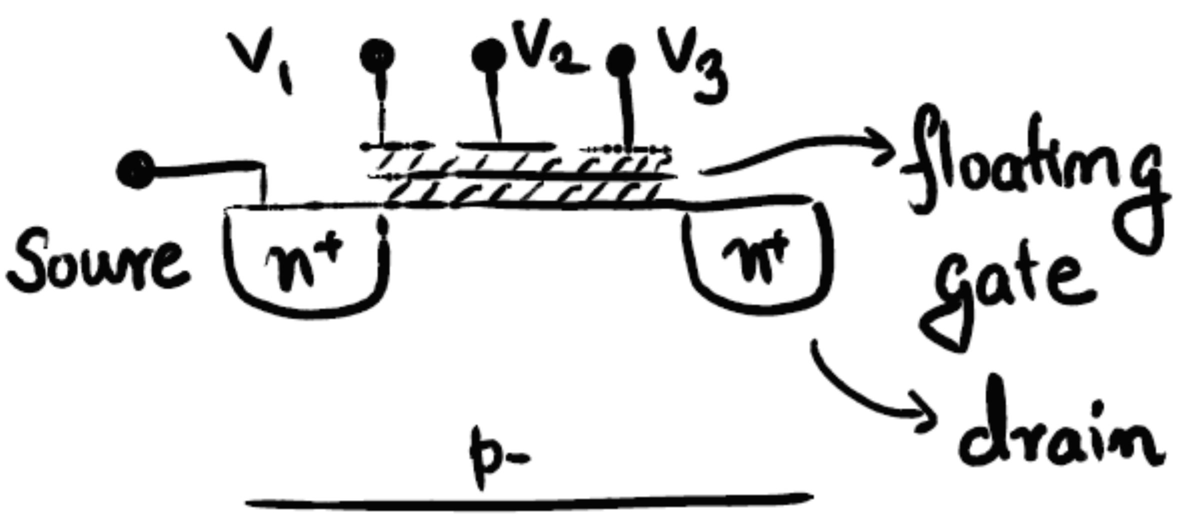
pMOS translinear circuits

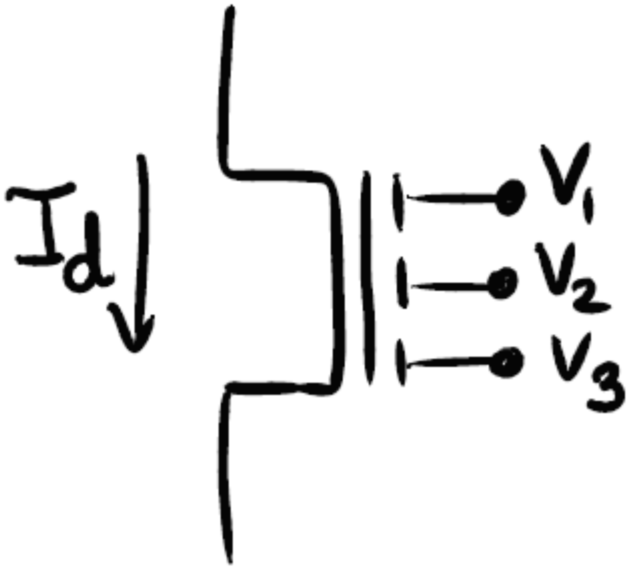
- What about this circuit ?



Floating-gate translinear circuits

- Gate of the transistor – floating.



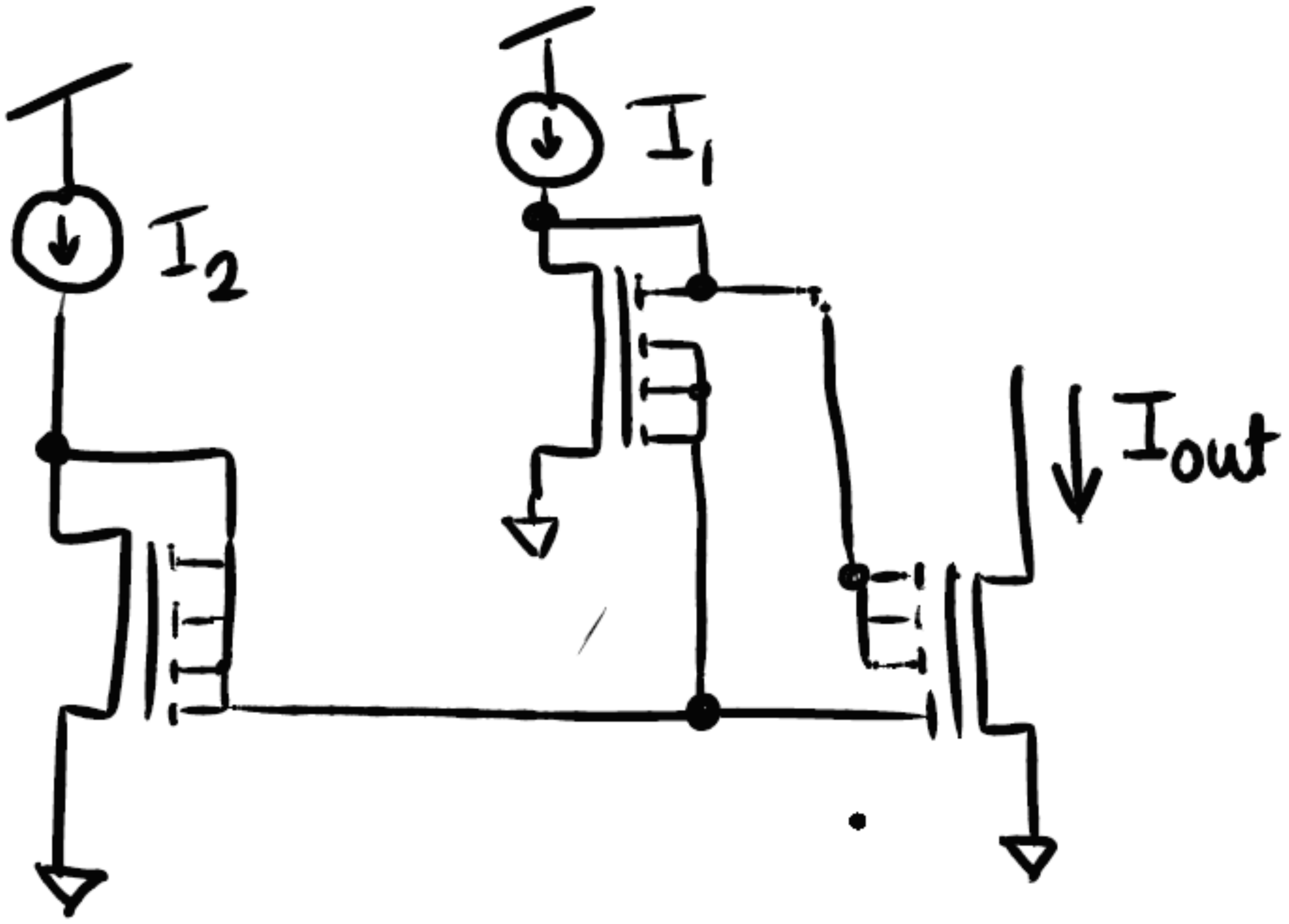


- Multiple inputs capacitively couple to the gate.

$$I_d \approx I_S \exp\left(\kappa \frac{V_1 + V_2 + V_3}{U_T}\right) \exp\left(\frac{-V_s}{U_T}\right)$$

- The charge on the floating-gate needs to be zeroed post fabrication.

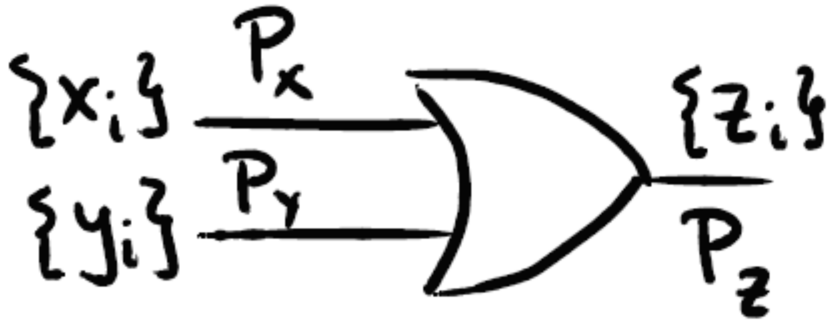
What function does this circuit implement ?



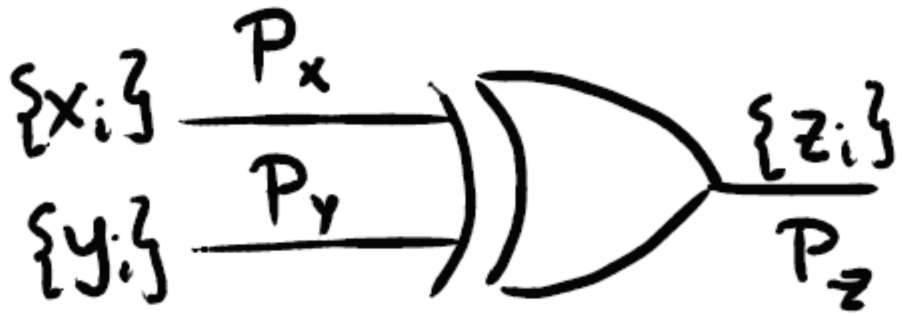
Stochastic analog computing

- Value encoded as Bernoulli probabilities.
- 0.2 = {0 0 0 1 1 0 0 0 0 0…} or {0 1 0 0 0 1 0 0 0 0 …}

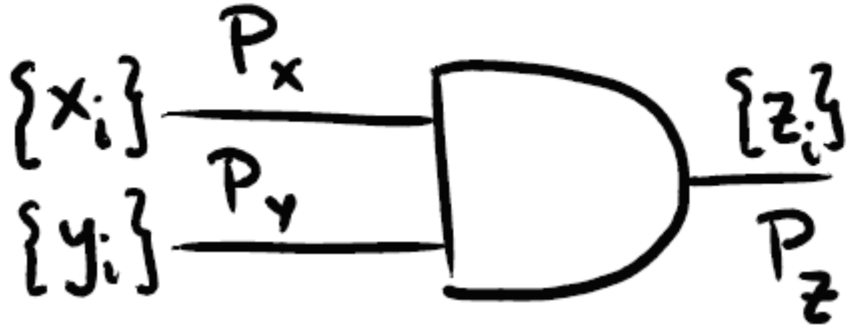
- Addition



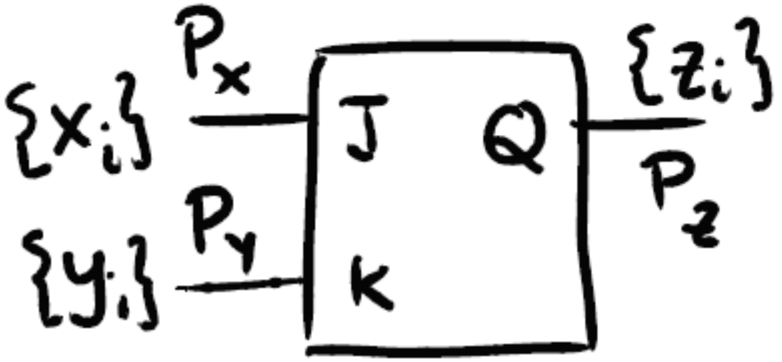
- Matching



- Multiplication



- Division



$\{x_i\}$
P_x
$\{y_i\}$
P_y
J
K
Q
$\{z_i\}$
P_z