Parametric Analysis in ADE L environment

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1 Introduction

In this tutorial, we will use Virtuoso Parametric analysis to plot different Vgs' for an NMOS transistor.

2 NMOS Test Circuit

Inside the library manager, select the course library and create a new cell view inside. Call it “nmos curves". Create a schematic like figure 1.

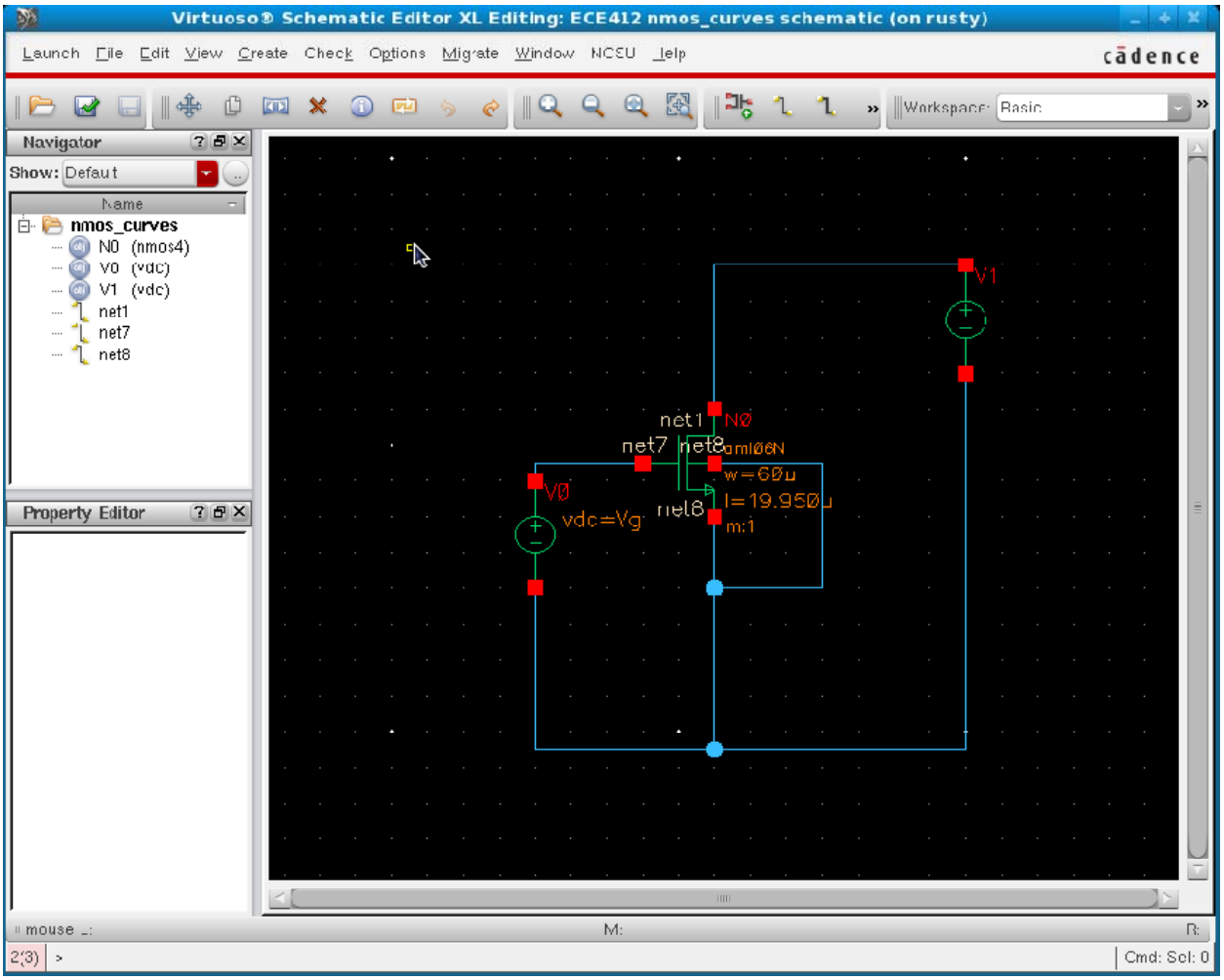

Figure 1 NMOS test circuit

The two voltage sources are “vdc" from analogLib. The gate voltage should be set to a variable called “Vg" as shown in figure 2.

Note that the voltage source connected to the drain is currently blank and will be used later for DC analysis.

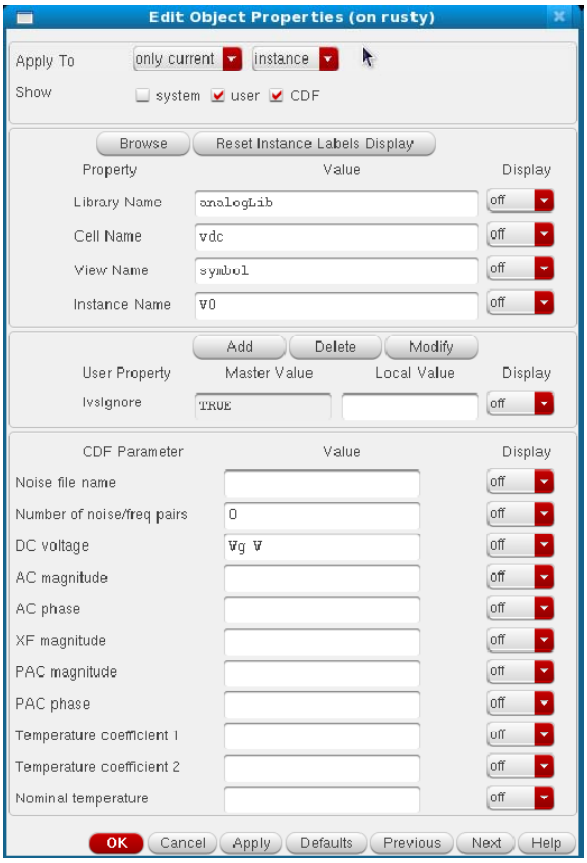

Figure 2 Vgs voltage set to a variable Vg

3 Simulation

Launch ADE L and conduct a DC analysis as discussed in the previous tutorials.
Under Sweep variable check Component Parameter then click on “Select Component". Go to the schematic window if it is not in front of you, now select the voltage source connected to the Drain (V1) by clicking on it and choose DC voltage parameter. For sweep range we will swing the drain voltage from 0 to 3 using 0.1 steps. The DC analysis is shown in figure 3.

Add a new output to be plotted on schematic and select the negative red terminal of the Drain voltage. Remember, that clicking on the blue wire plots the Voltage and clicking on the red terminal plots the Current. Here we are interested in the current flowing through the transistor, so, click on the terminal to get “/V1/MINUS".

In the ADE L window, add the variable Vg to Design Variable list box in the left hand side by hitting **Variables ➔ Copy From Cellview** submenu item. Then go to **Tools ➔ Parametric Analysis** and you should see the window shown in figure 4.

Enter “Vg” in the Variable Name box, and set its range from 0 to 3 volts in the From / To boxes respectively. Change the step type to Linear Steps from the Step Control drop-down box. Set the Step Size to 0.5. To run the simulation, in the same window “Parametric Analysis”, go to **Analysis ➔ Start.** Your resulting plot should look like the plot in figure 5.

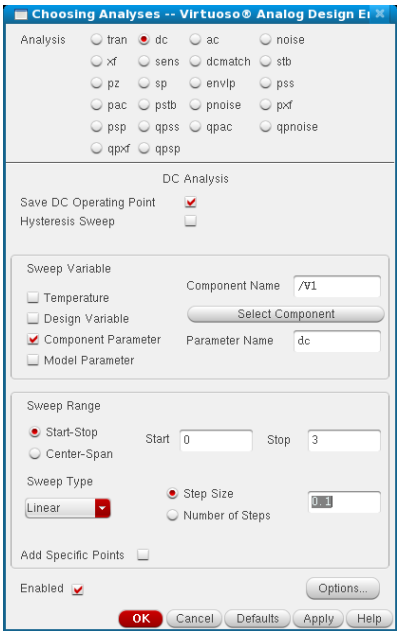

Figure 3 NMOS DC Analysis

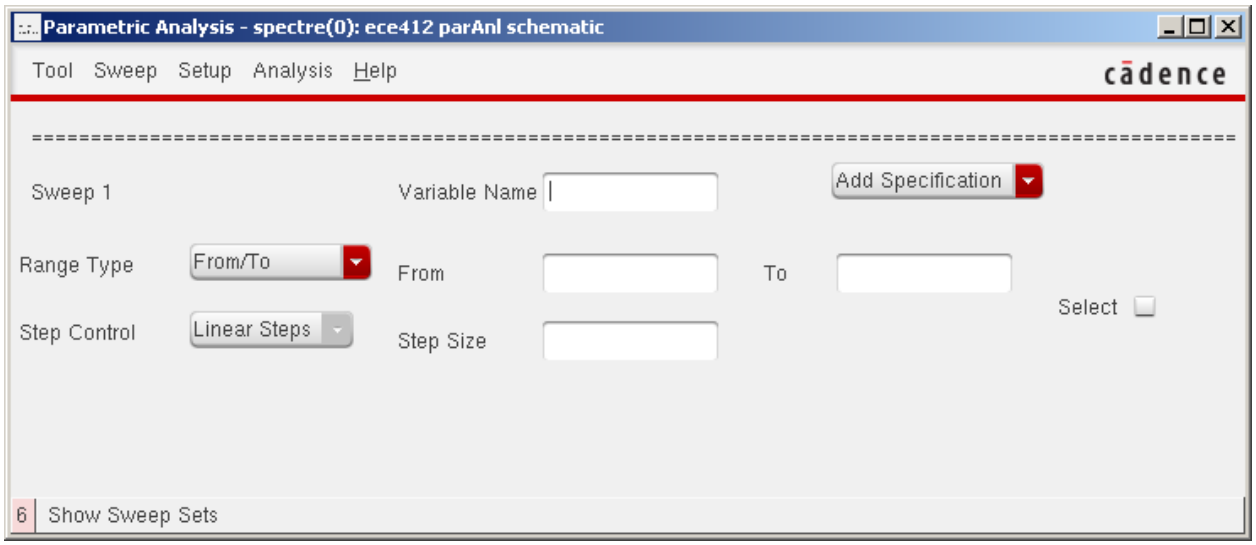

Figure 4 Parametric Analysis

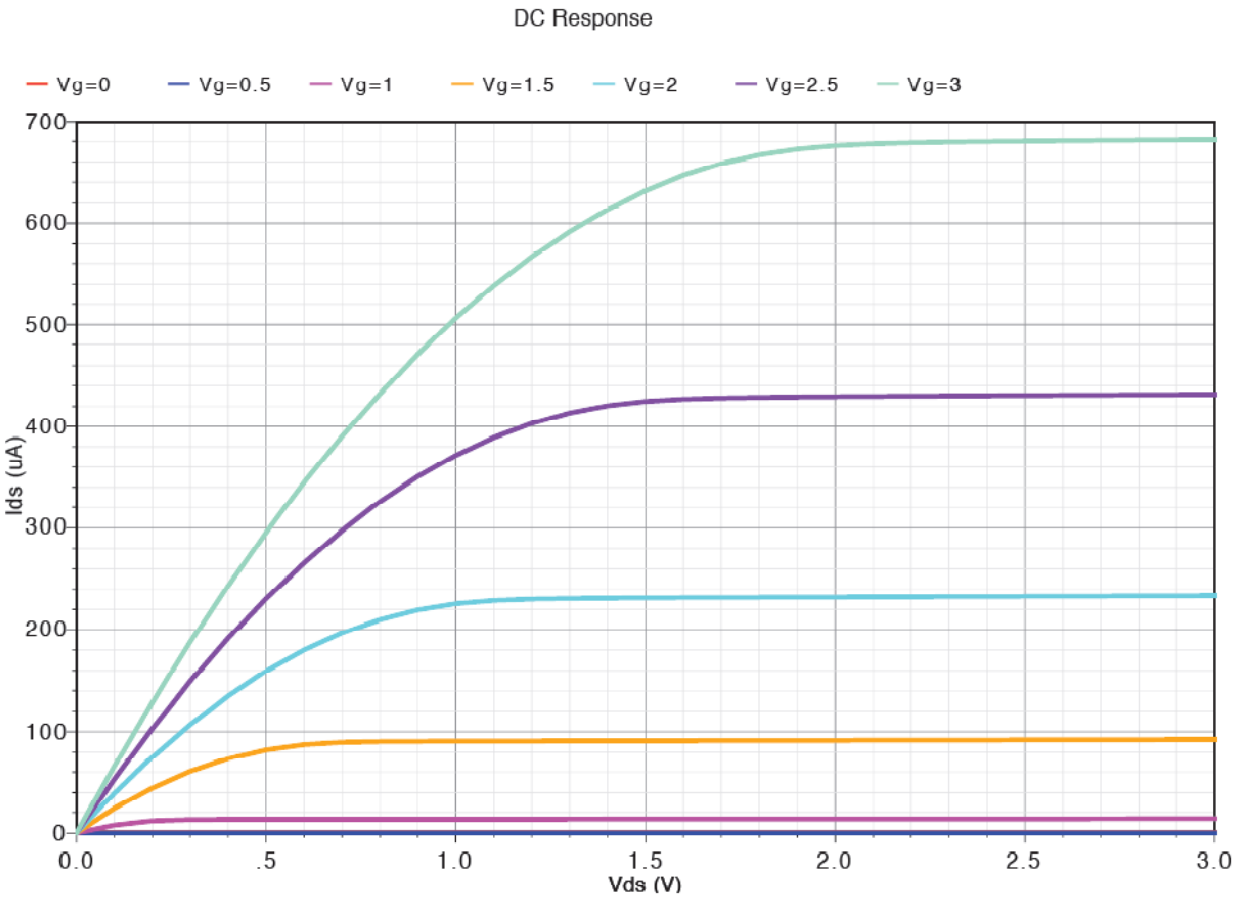

Figure 5 Vds vs Ids for different gate voltages.