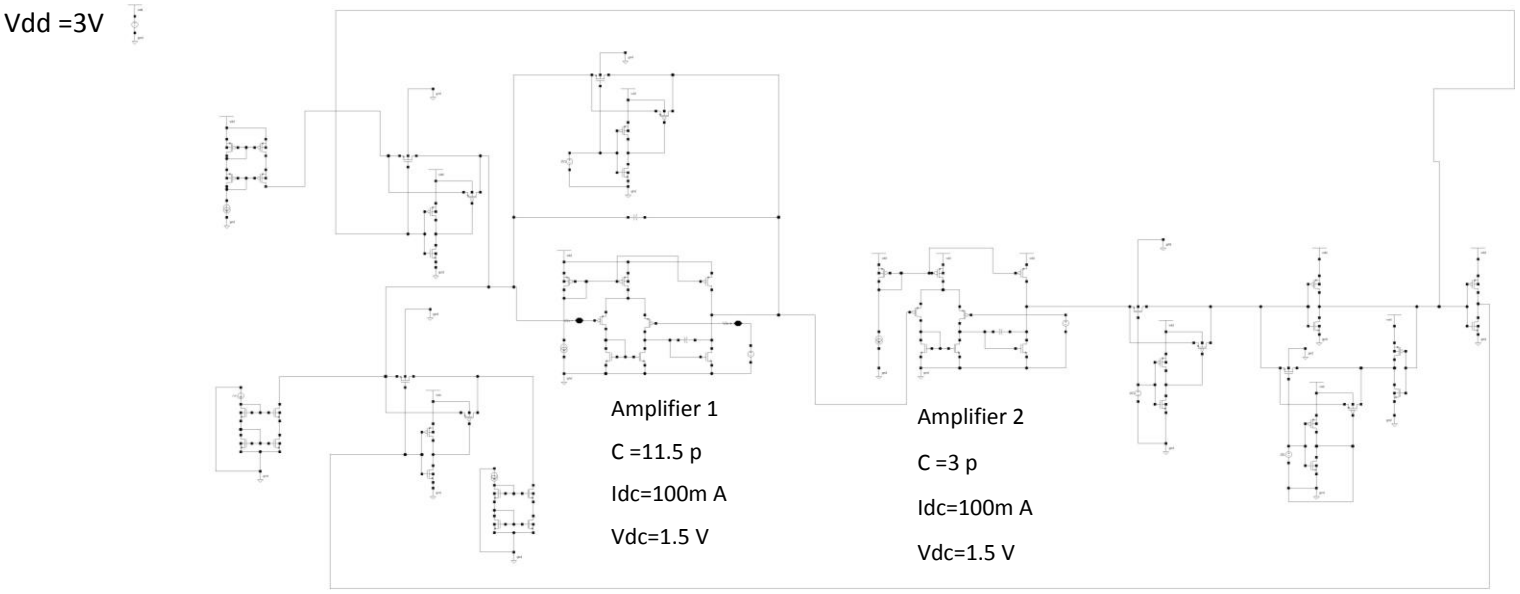
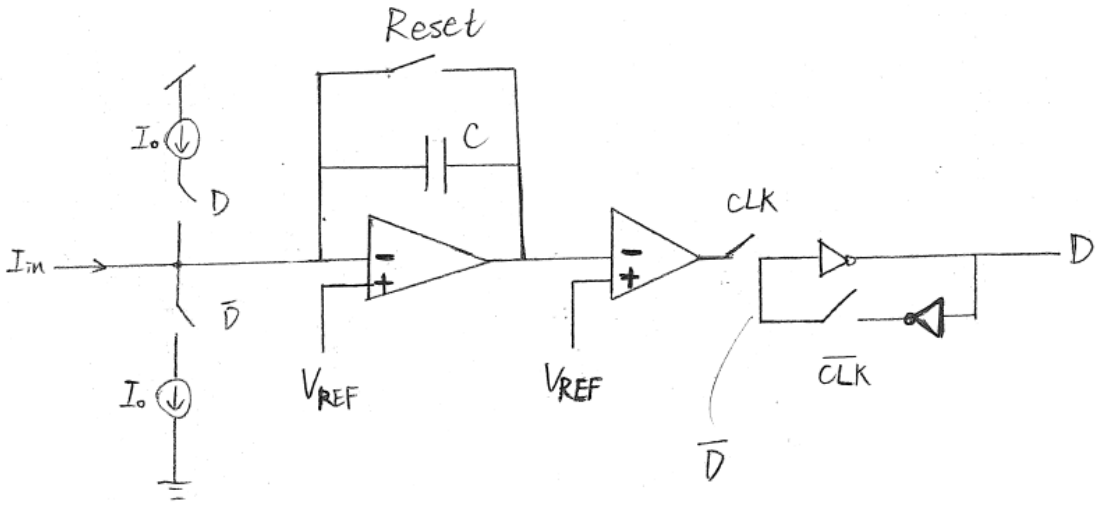
ESE 562_Project 3

Po Hsu Chen, 448031

System level architecture with component values (C, Io, CLK, VREF, VCMP)



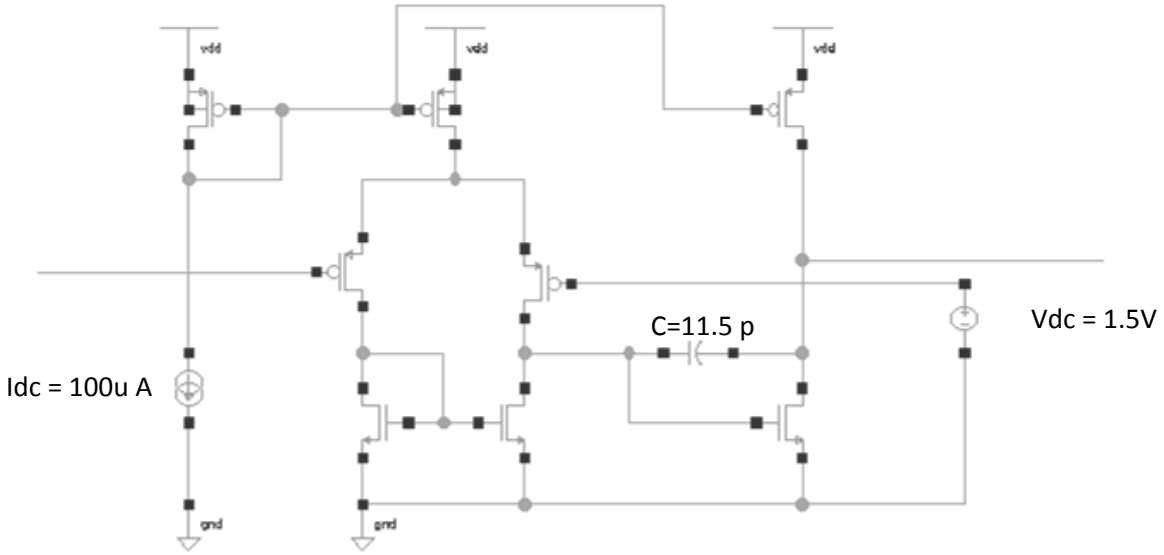


C	Io	CLK	V_{ref}	V_{CMP}
3p	130n A	V pulse 0 ~ 3V (3~0V)	1.5 V	1.5 V
		Pulse width 20u s		
		Period 40u s		

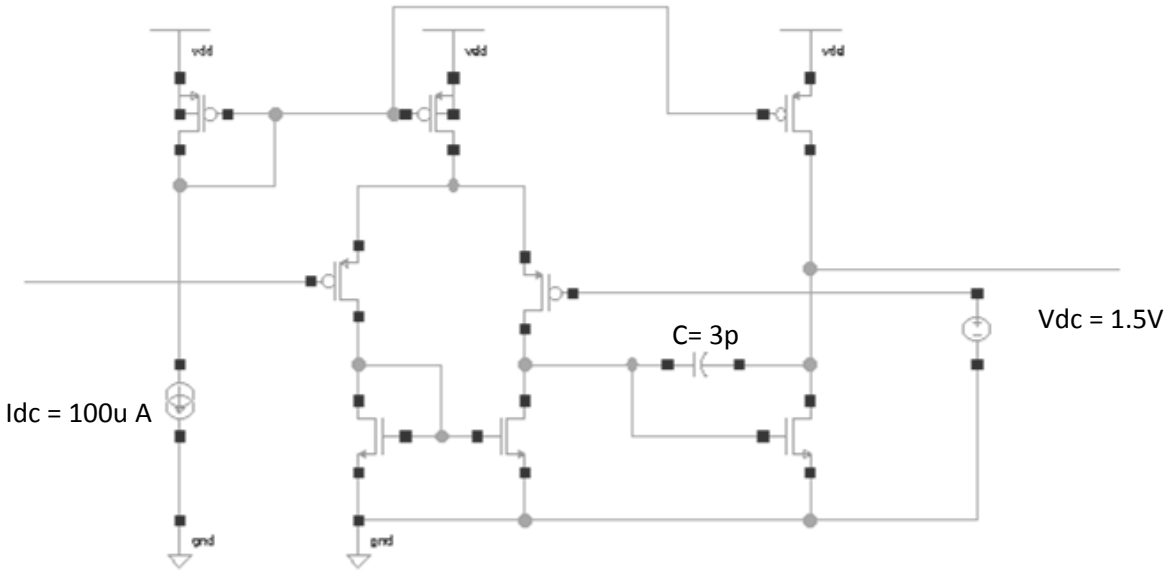
Amplifier Implementation

I chose the amplifier as the one in project 1.

Amplifier 1.

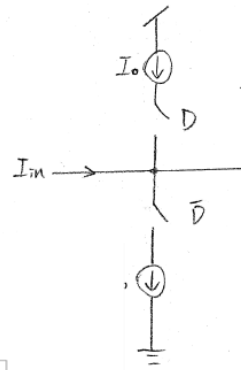


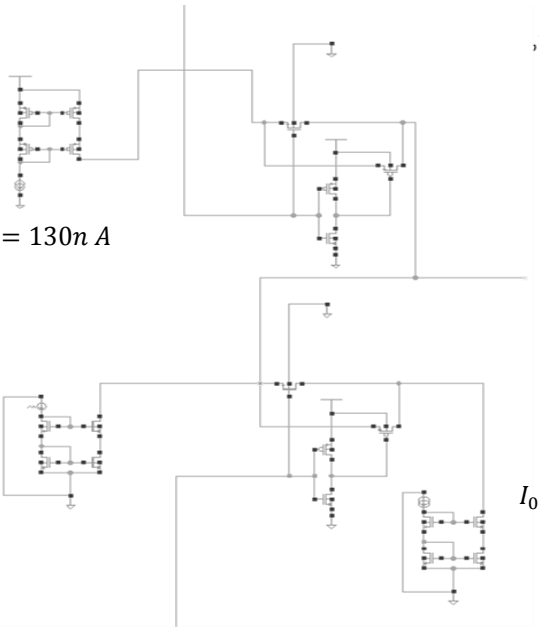
Amplifier 2.



Implementation

Current Source and Sink

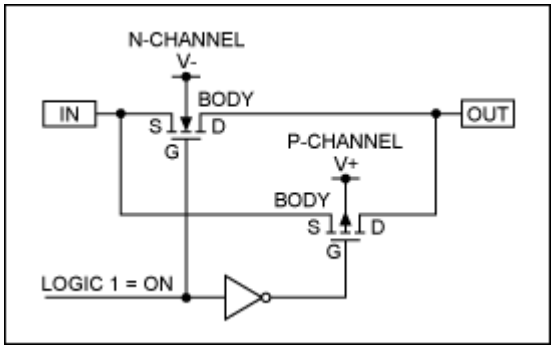


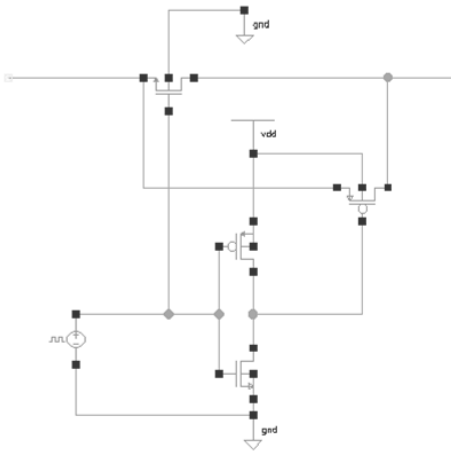


$I_0 = 130n\ A$

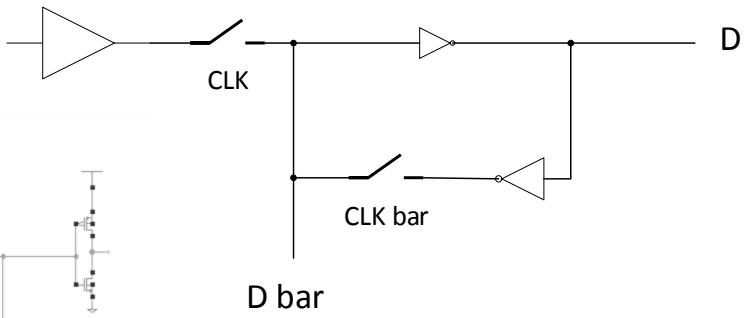
$I_0 = 130n\ A$

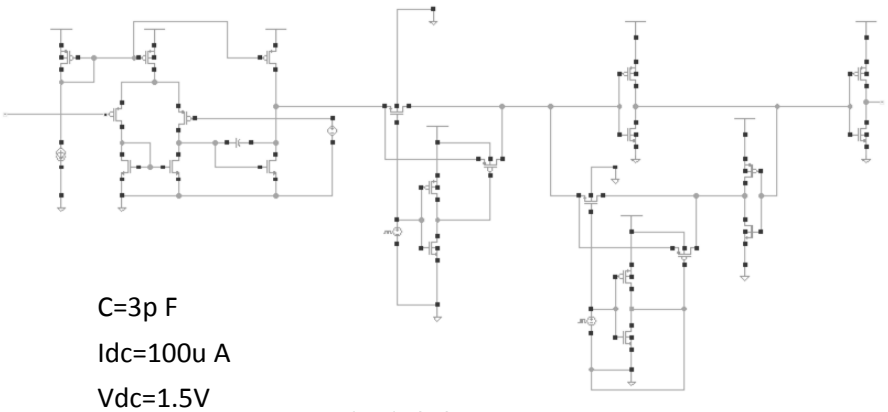
CMOS Switch





Latched Comparator





C=3p F

Idc=100u A

Vdc=1.5V

CLK is 0~3V

Pulse width 20u s

Period 40u s

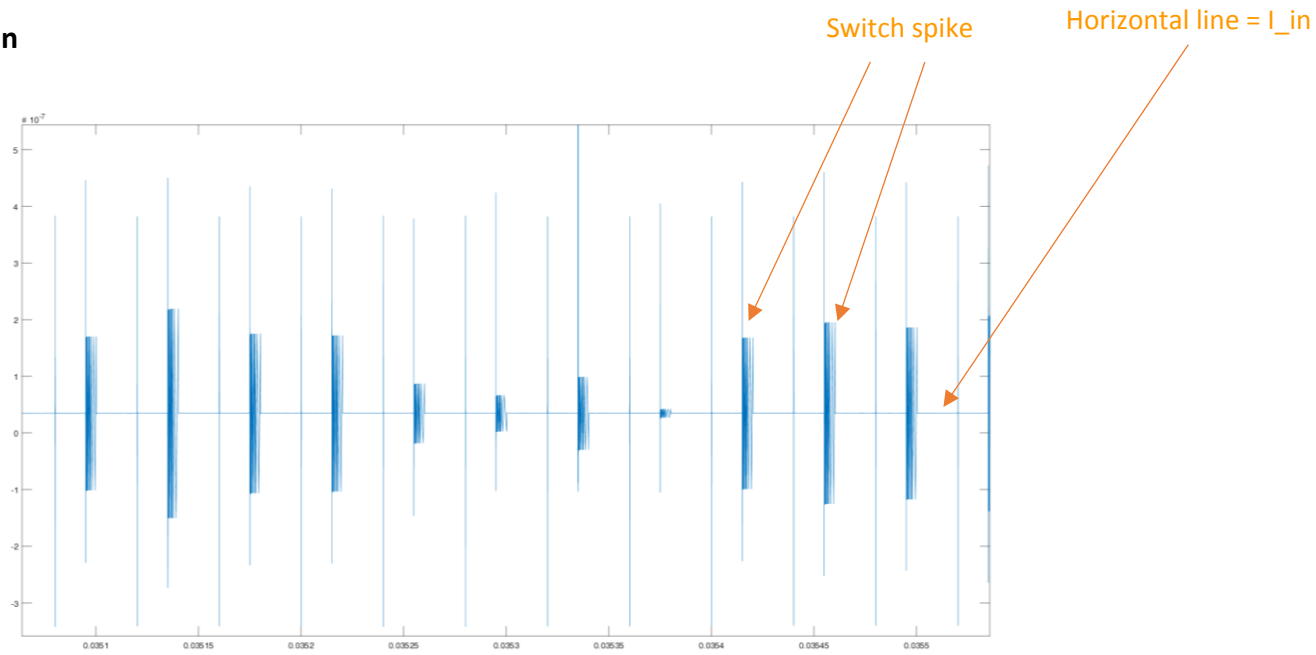
CLK is 3~0V

Pulse width 20u s

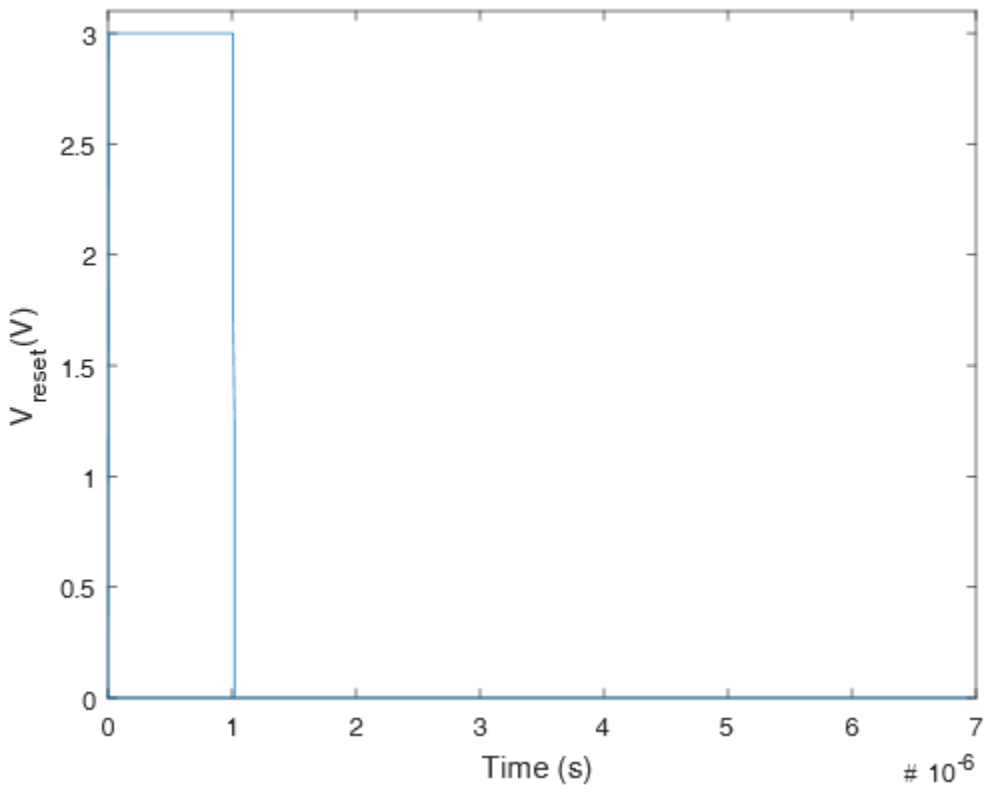
Period 40u s

Output of the modulator and voltage Vx

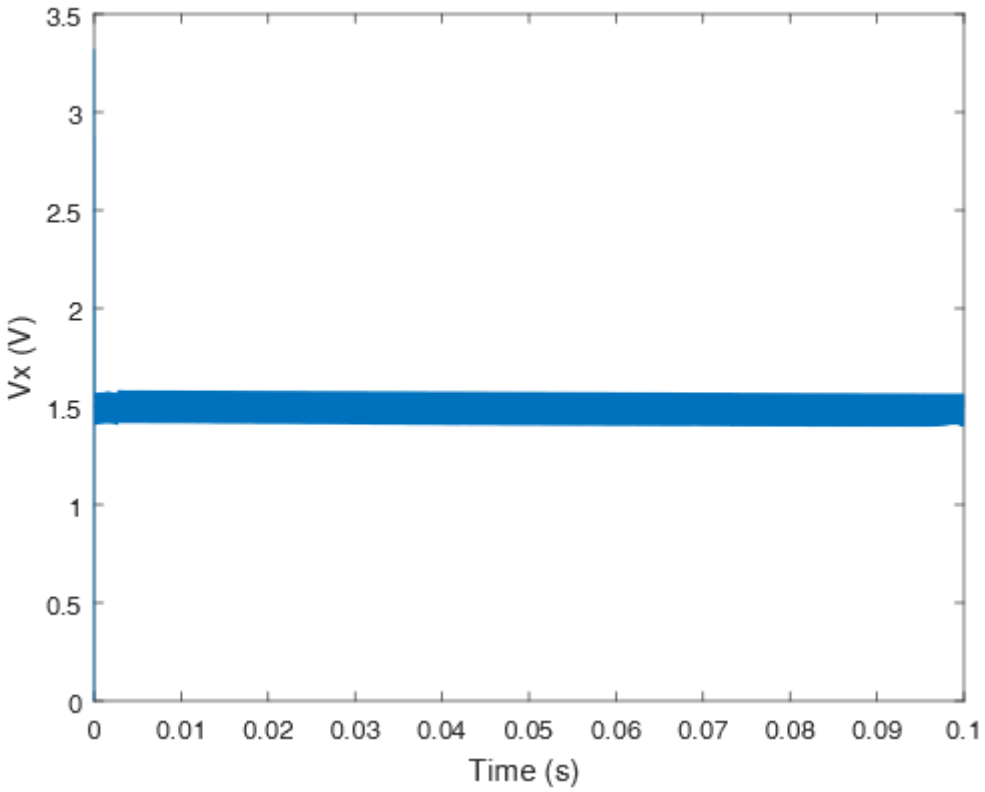
Iin



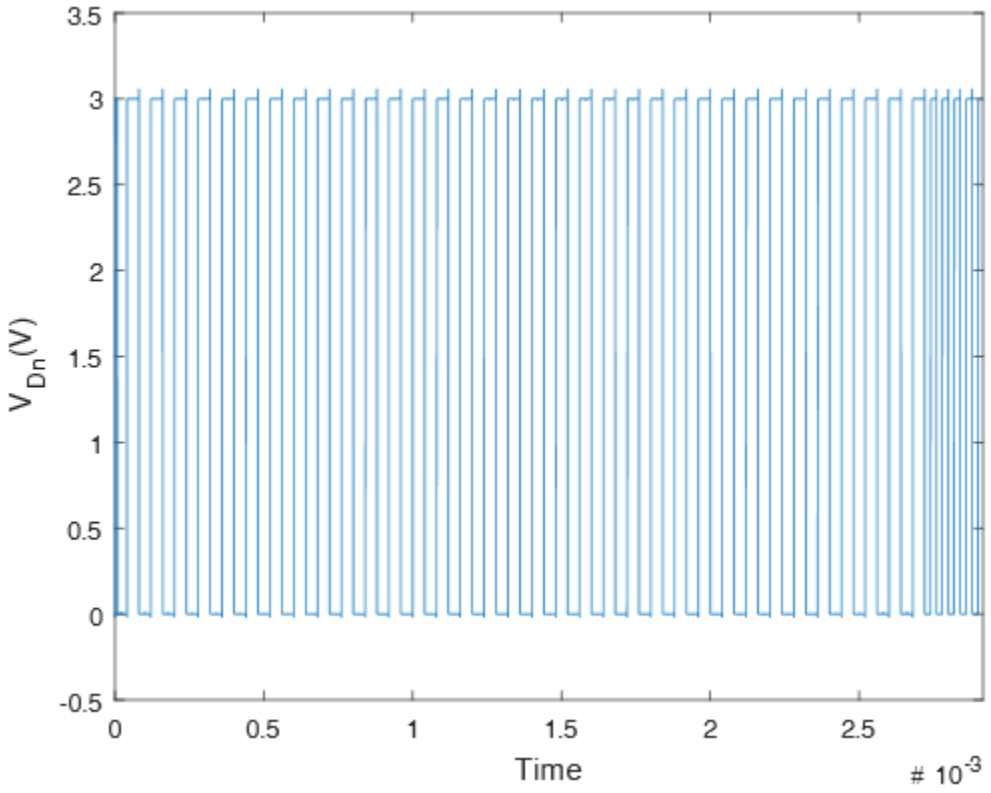
V_reset:

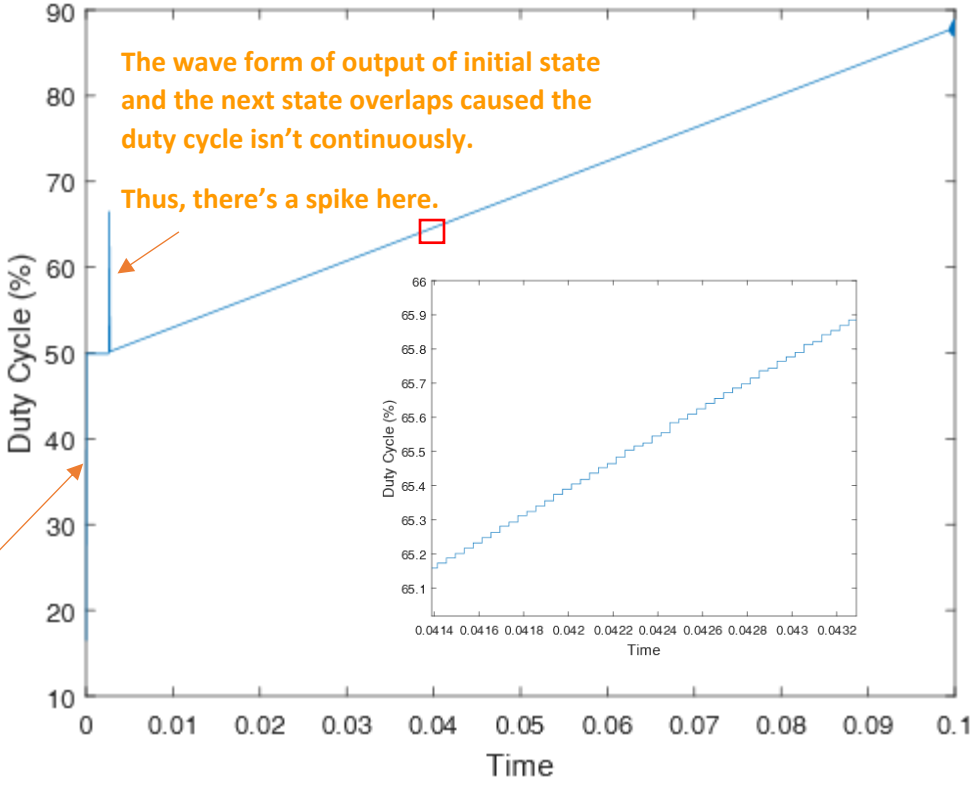


Vx


3.5
3
2.5
2
1.5
1
0.5
0
Vx (V)
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)

V_Dn and Duty Cycle





The wave form of output of initial state and the next state overlaps caused the duty cycle isn't continuously.

Thus, there's a spike here.

Reset spike

Speed:

CLK is 0~3V and 3~0V

Pulse width 20u s

Period 40u s

Resolution:

Since there are 2410 data points in duty cycle.

$log_2 2410 = 11.2348174$

=>The resolution is 11.2 bit.

Power Dissipation:

P = I*V

P = 399u A* 3 V = 1.2m Watt