



OPERATIONAL AMPLIFIERS

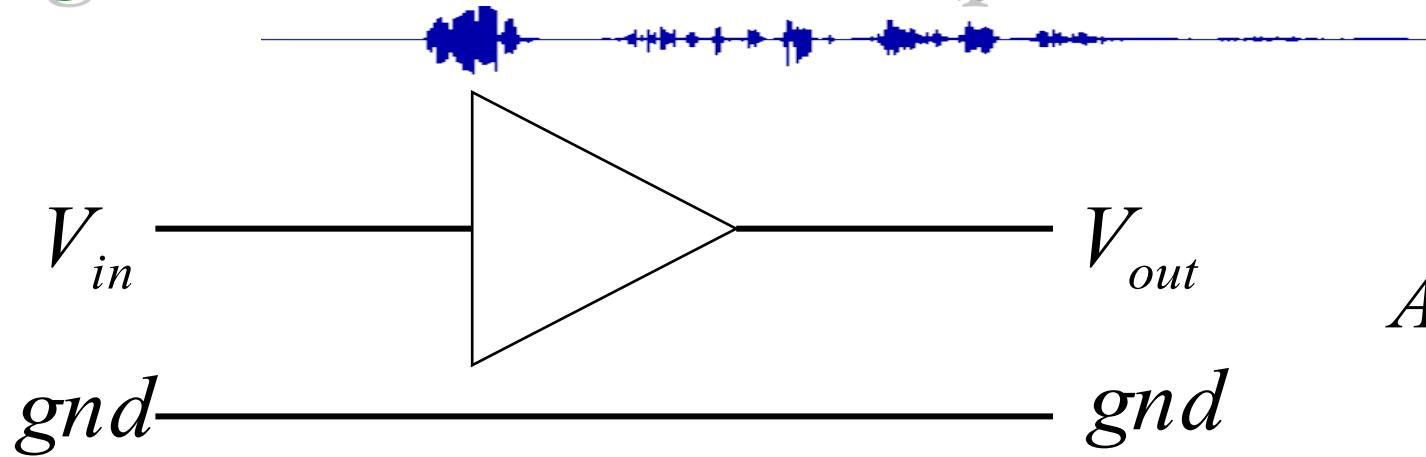
Operational Amplifier Design



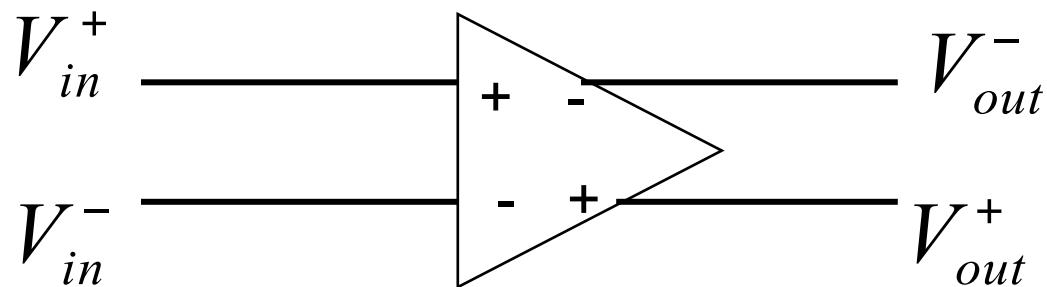
CSE562: Analog Integrated Circuits
Shantanu Chakrabartty



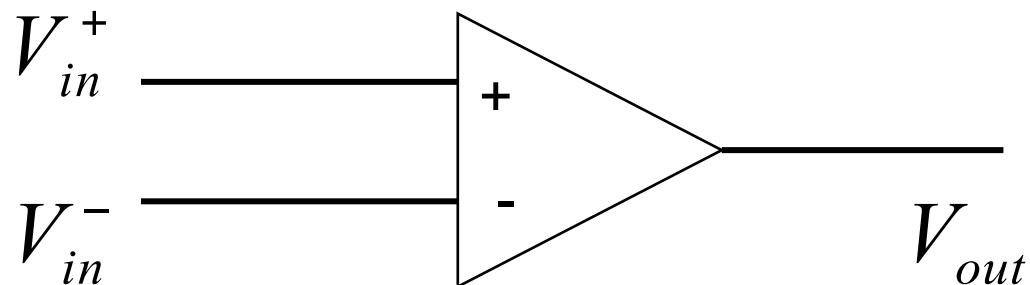
Single and differential amplifiers



$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}}$$



$$A_v = \frac{\Delta V_{out}^+ - \Delta V_{out}^-}{\Delta V_{in}^+ - \Delta V_{in}^-}$$

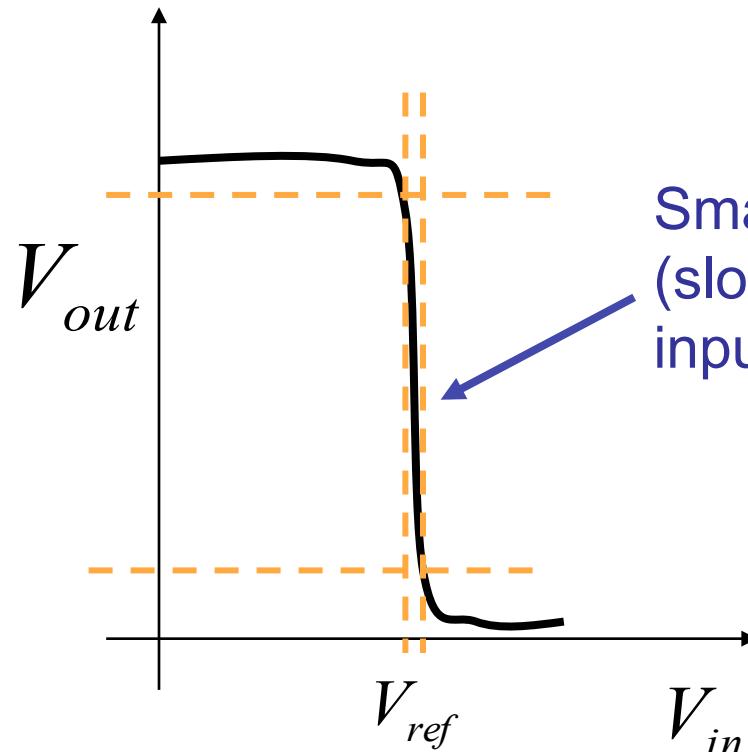
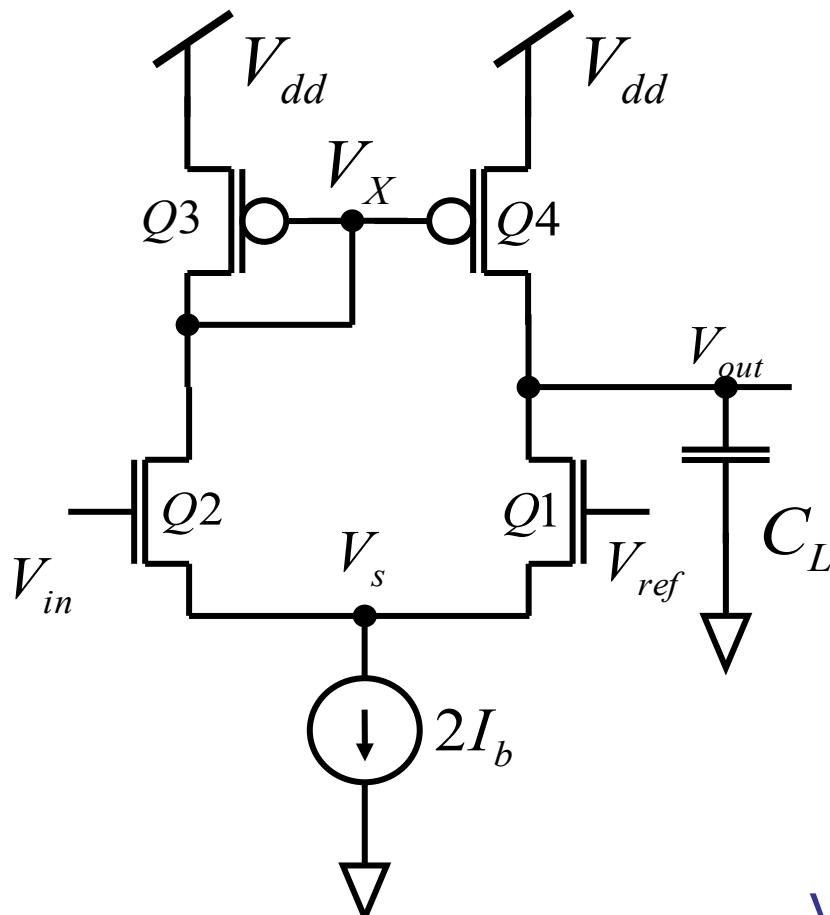


$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}^+ - \Delta V_{in}^-}$$

Feedback



Even though we have applied small signal model for calculating gain of an amplifier, CMOS amplifier is inherently non-linear.

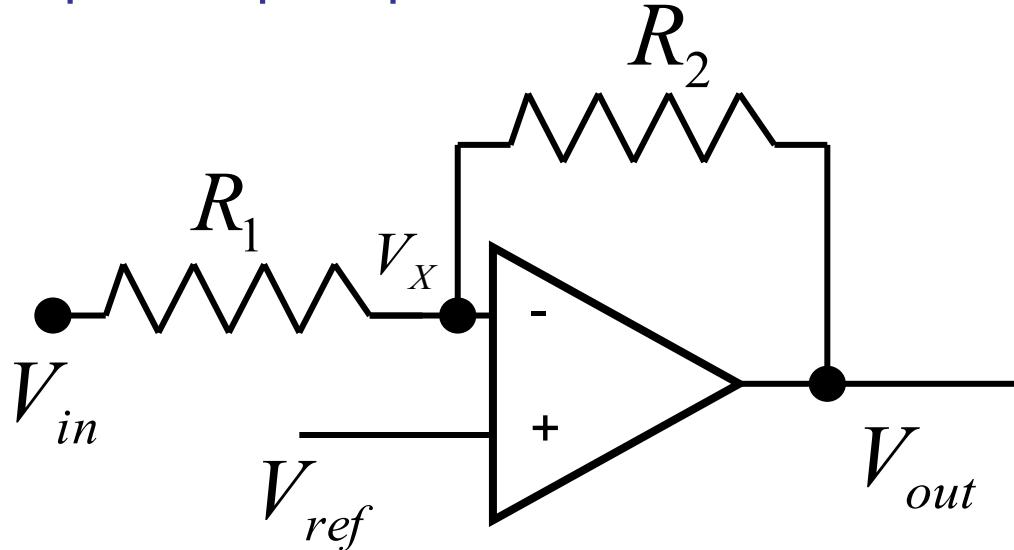


Variation in gain could be more than 100%

Feedback



Open loop amplifiers are seldom used for precise amplification.



$$A \gg (1 + \frac{R_2}{R_1})$$

$$\Delta V_{out} = -\frac{R_2}{R_1} \Delta V_{in}$$

$$\frac{V_{in} - V_X}{R_1} = \frac{V_X - V_{out}}{R_2}$$

$$V_{out} = A(V_{ref} - V_X)$$

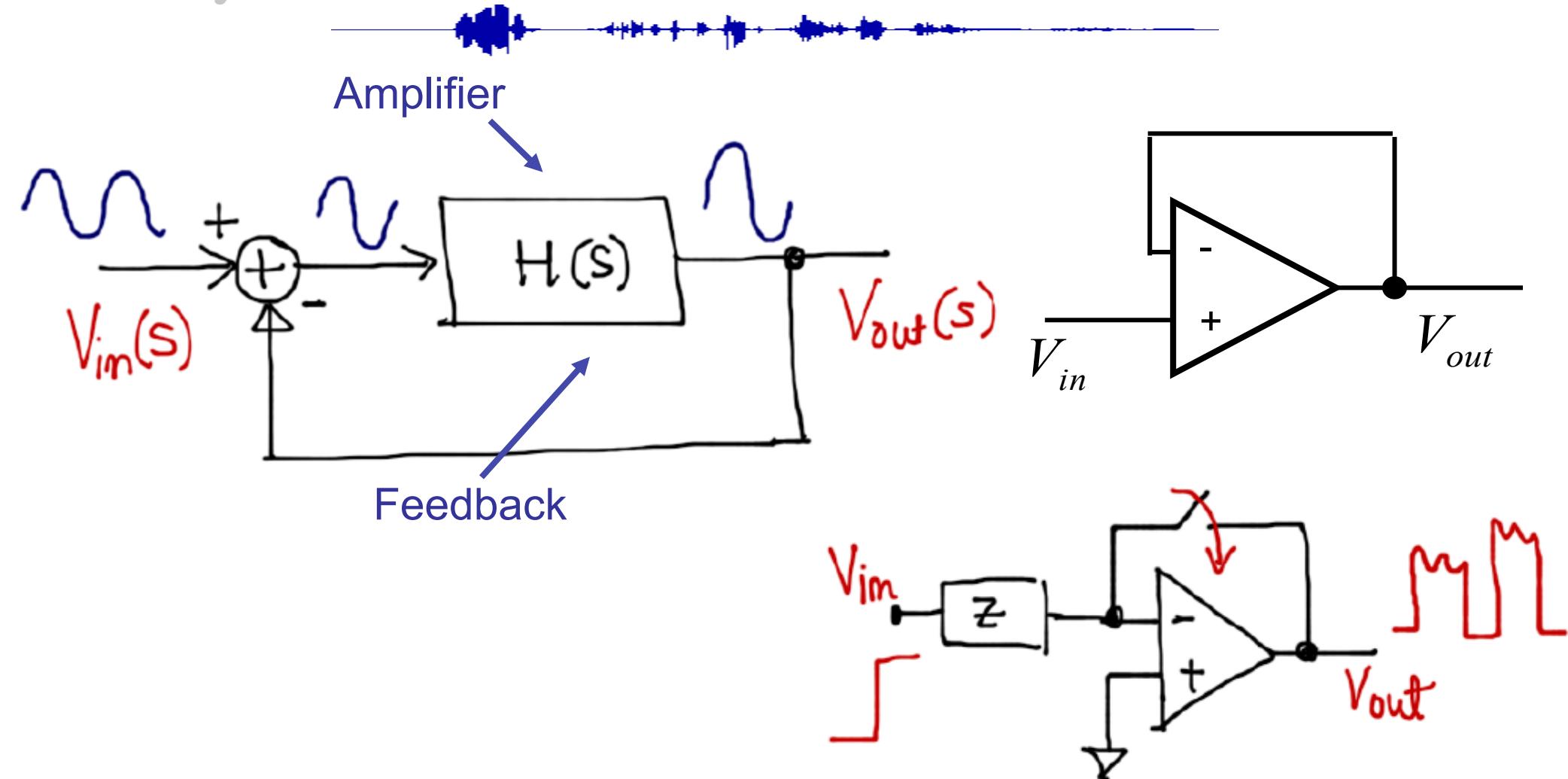
$$\Delta V_{out} = \frac{-\frac{R_2}{R_1} \Delta V_{in}}{\left[1 + \frac{1}{A} \left(1 + \frac{R_2}{R_1}\right)\right]}$$

Easy to design amplifiers with high gain (precision not required)

Linearity and precision determined by ratio of resistors.

The amplifier tries to fix the voltage V_X WITHOUT DRAWING ANY CURRENT.

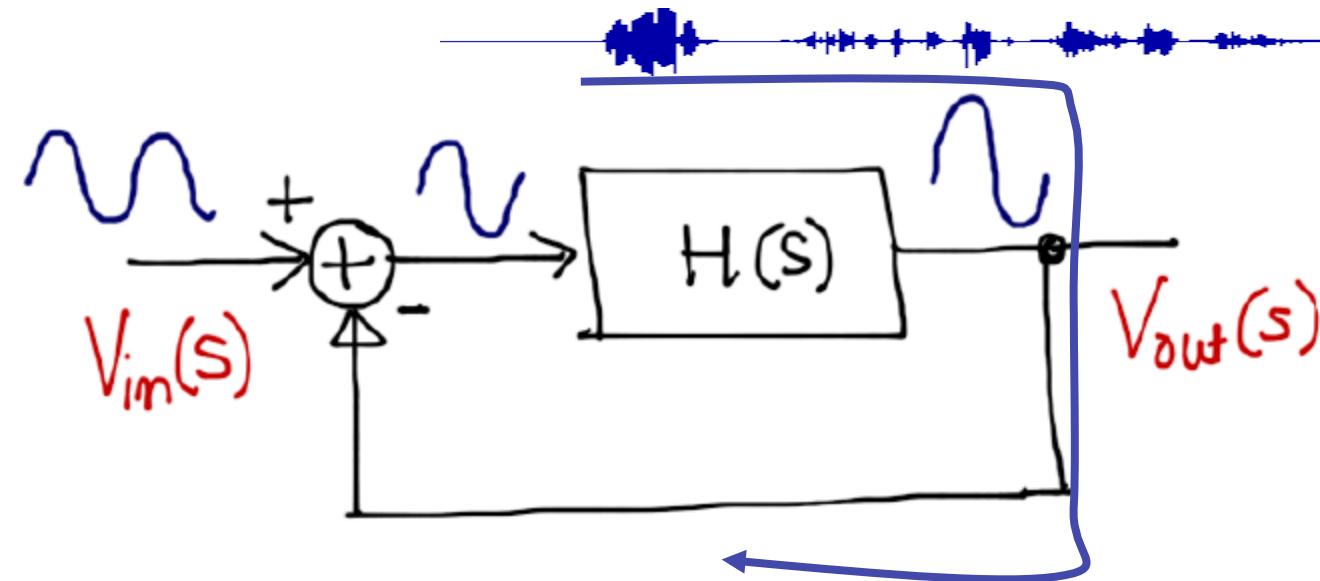
Analysis of Feedback Network



For oscillations/instability a 180 degrees phase shift is required at the negative feedback terminal. The feedback signal adds in phase with the input signal (could be noise) and leads to oscillation build up.



Barkhausen's Criterion



$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)}$$

The negative feedback system may oscillate at a frequency ω if

1. Phase shift around the loop at this frequency becomes less than -180 degrees.

$$\angle H(j\omega) \leq -180^\circ$$

2. The loop gain is large enough to allow signal build up.

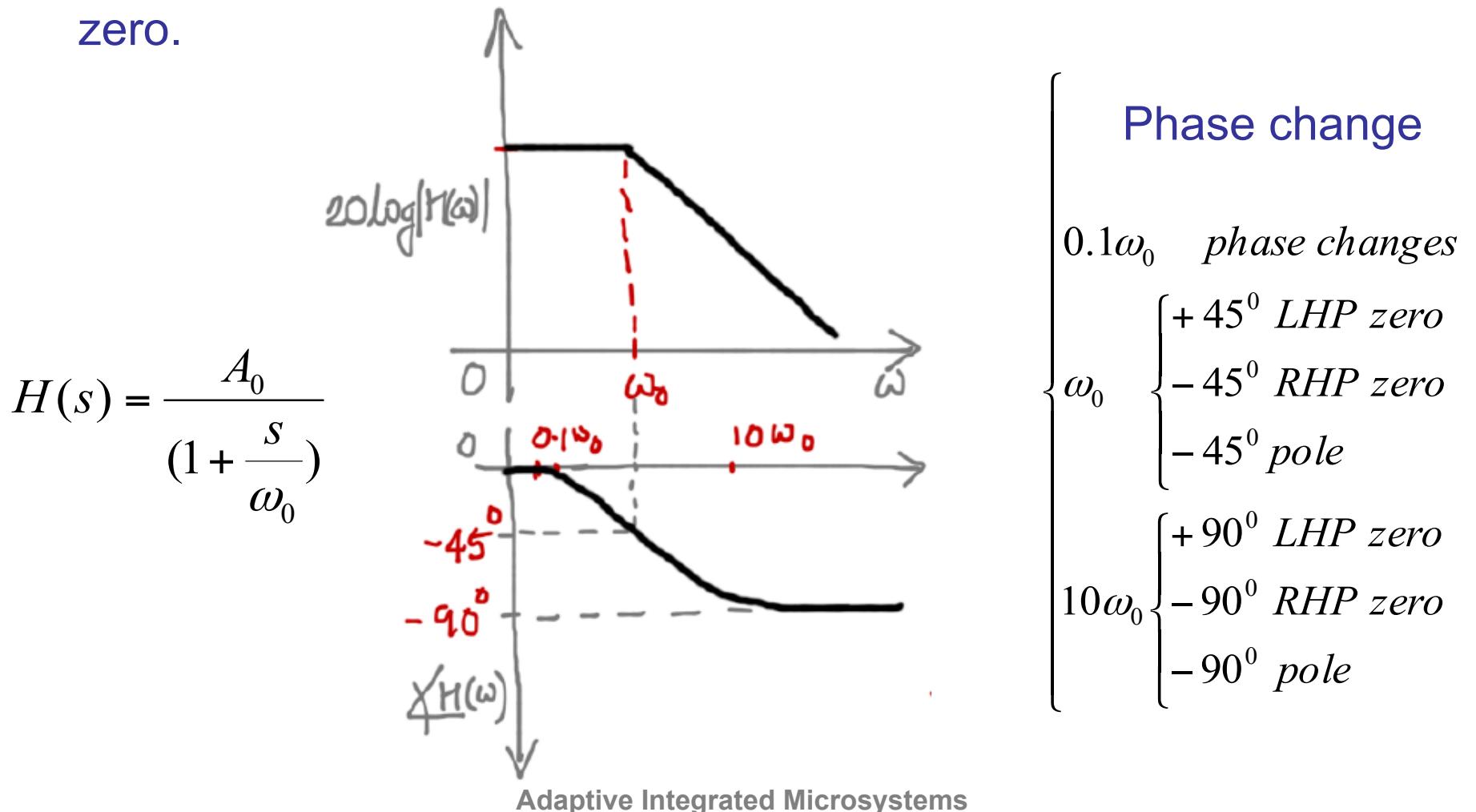
$$|H(j\omega)| > 1$$

How to calculate the phase-shift ?



Use bode plot to approximately calculate the magnitude and phase response.

Magnitude changes by -20dB/dec for a pole and by +20dB/dec for a zero.

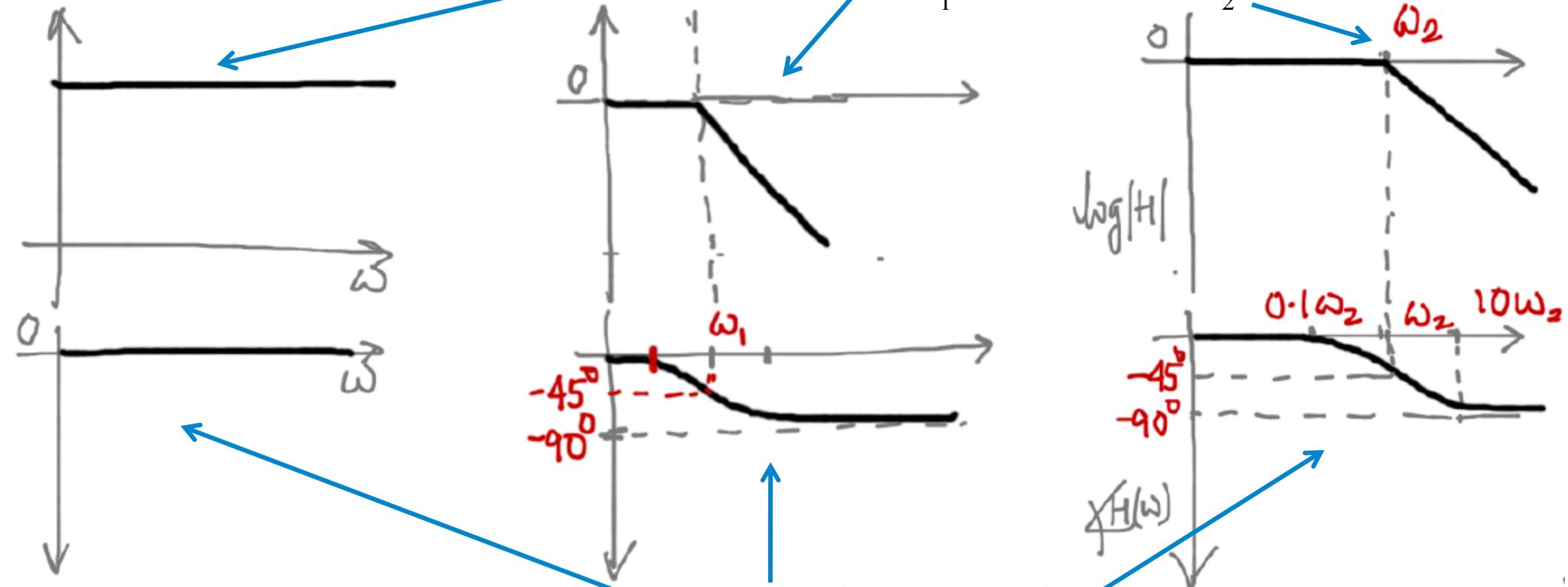


Multi-pole System



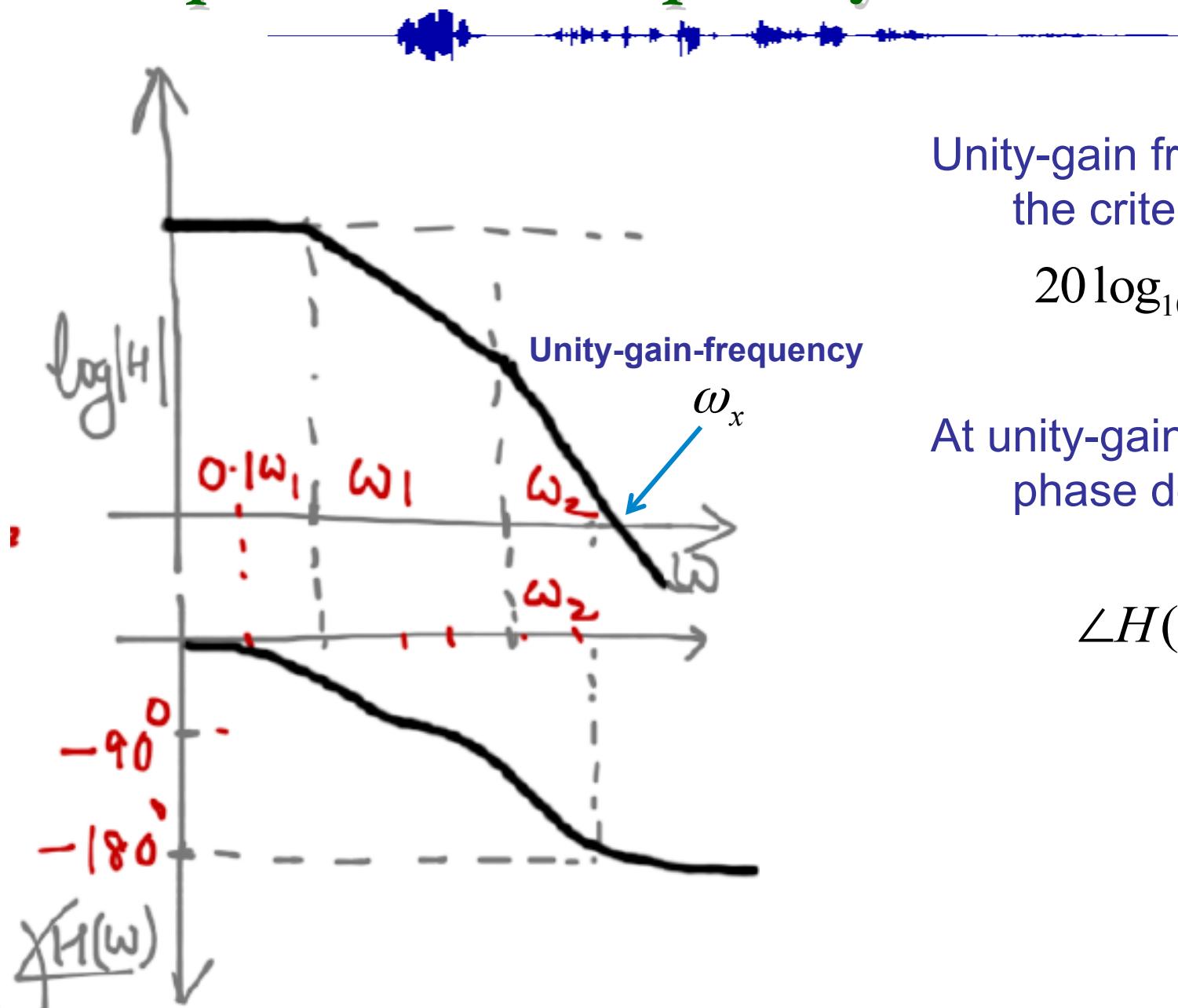
$$H(s) = K \frac{1}{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})}$$

$$20 \log |H(s)| = 20 \log K - 10 \log(1 + \frac{\omega^2}{\omega_1^2}) - 10 \log(1 + \frac{\omega^2}{\omega_2^2})$$



$$\angle H(s) = 0 - \tan^{-1}\left(\frac{\omega}{\omega_1}\right) - \tan^{-1}\left(\frac{\omega}{\omega_2}\right)$$

Bode-plots for multi-pole systems



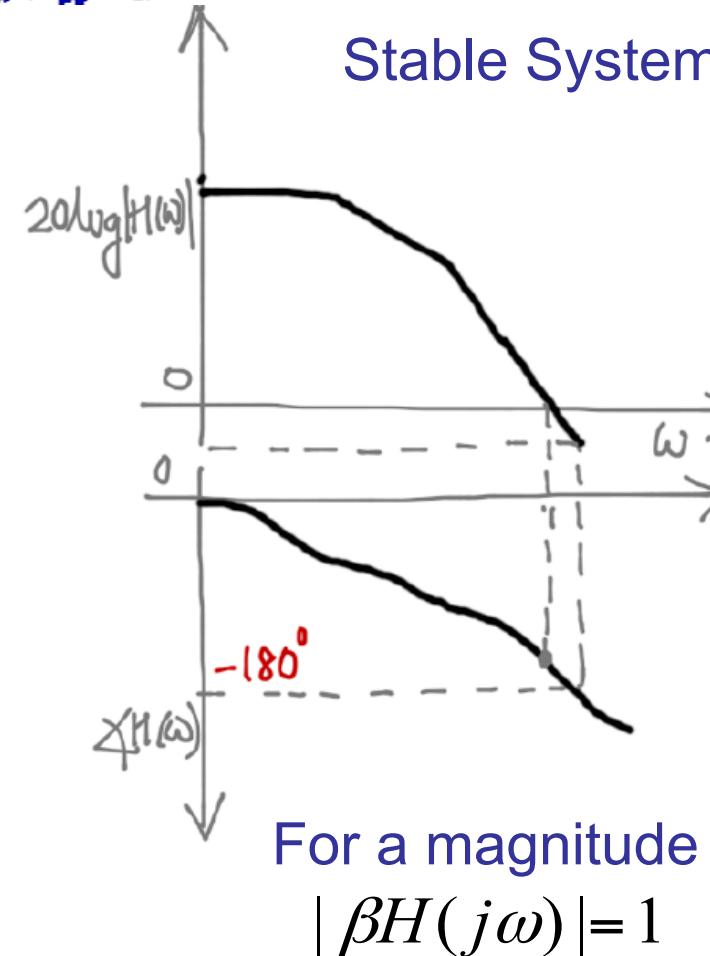
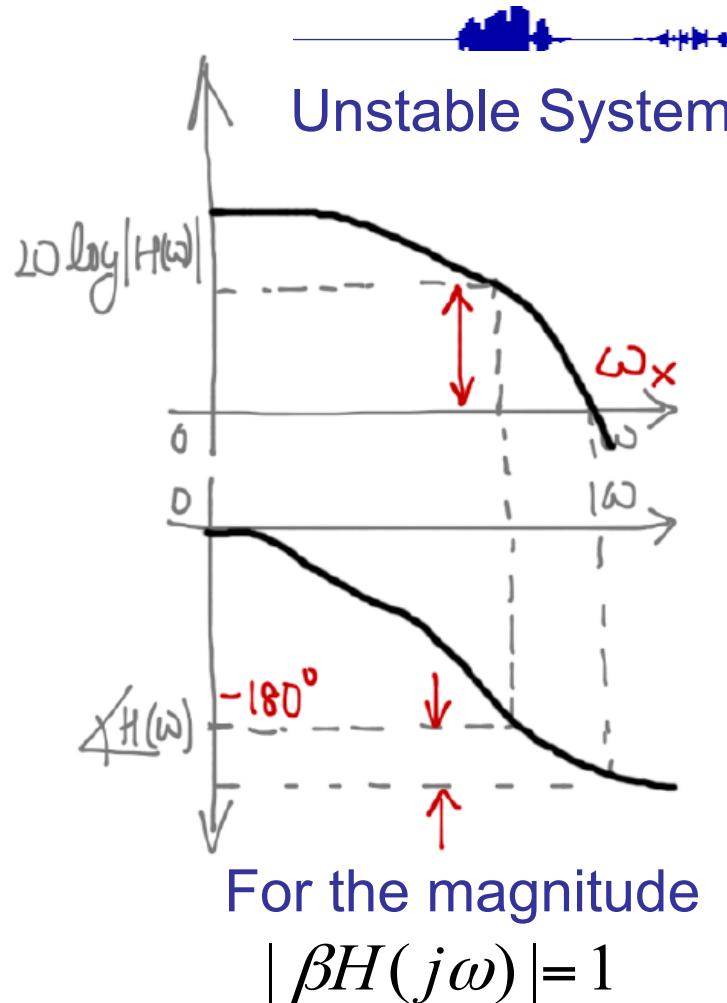
Unity-gain frequency satisfies the criterion

$$20 \log_{10} |H(j\omega)| = 0$$

At unity-gain frequency the phase delay is given by

$$\angle H(j\omega) \leq -180^\circ$$

Unstable and Stable Systems



Excess
phase

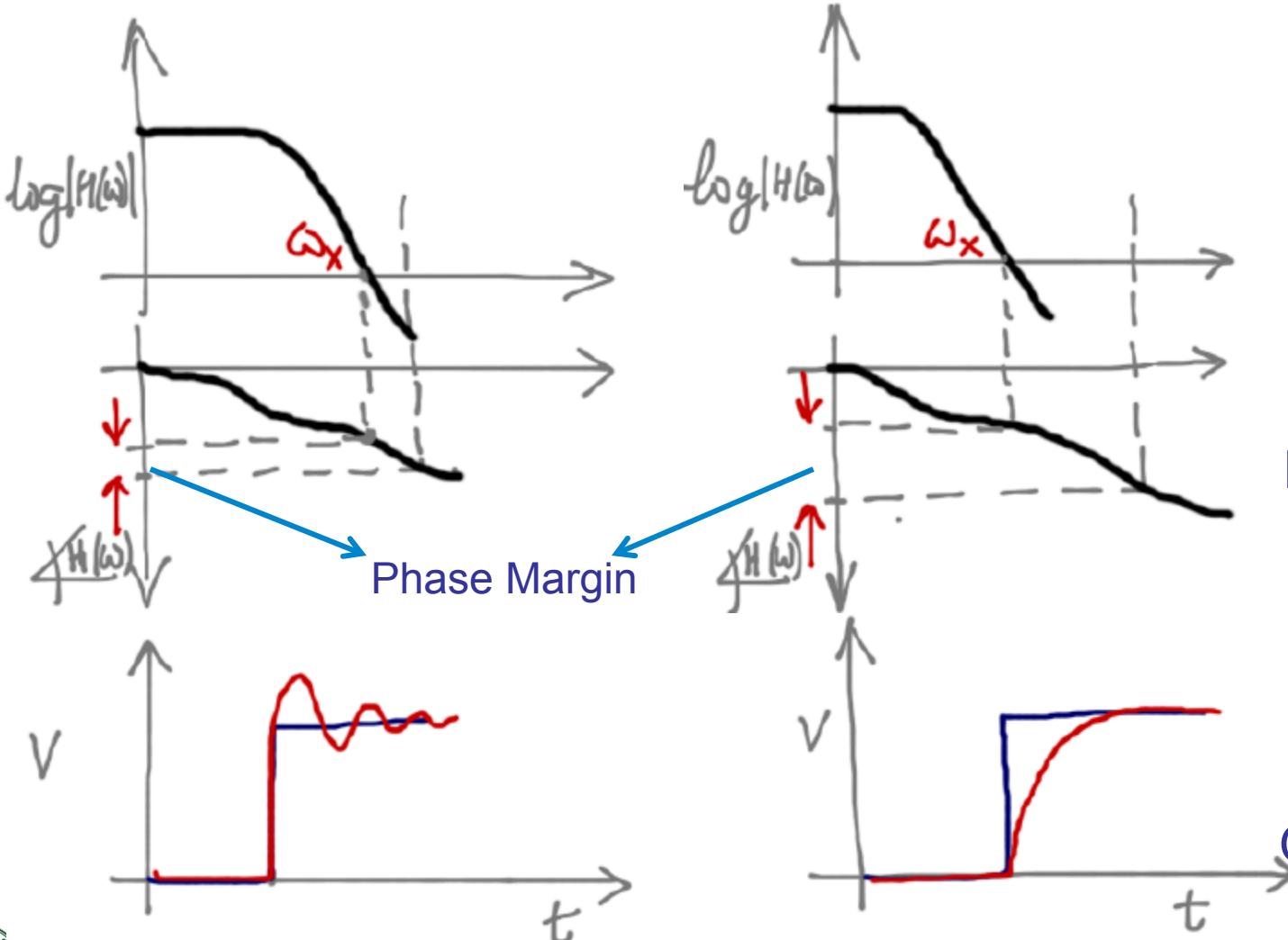
$$\angle \beta H(j\omega) \leq -180^\circ$$

$$\angle \beta H(j\omega) > -180^\circ$$



Phase Margin and Degree of Stability

Qualifies degree of stability of the system is measured by phase delay at gain cross over frequency – 180 degrees.



Larger the phase margin more stable is the system but increases the system delay.

Reduced phase-margin implies more ringing and oscillations in the step-response.

Optimal phase margin varies from 60 to 90 degrees.

Frequency Compensation

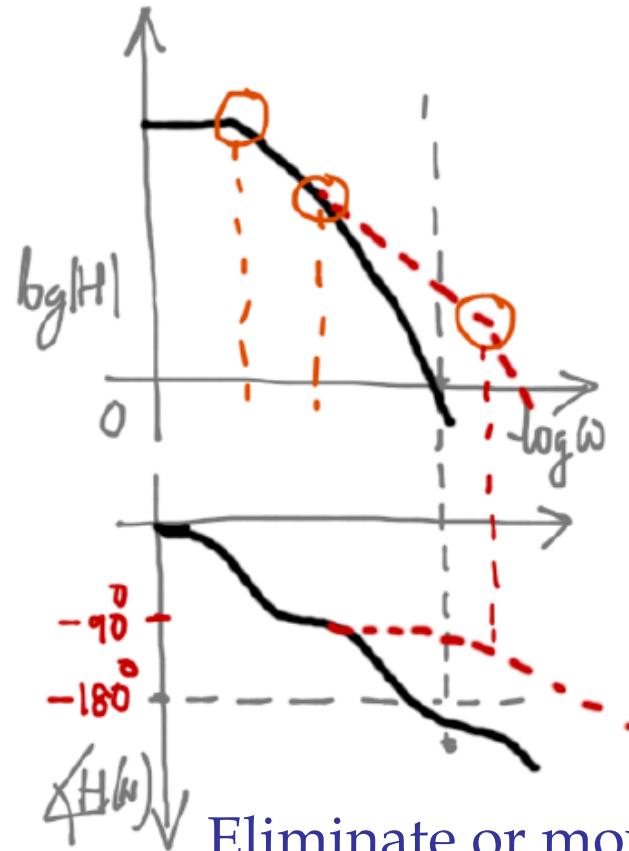


Frequency compensation implies modifying the open loop transfer function such that the closed loop feed-back system is stable.

Ensure that the log magnitude drops below zero before the phase delay reaches -180 degrees.

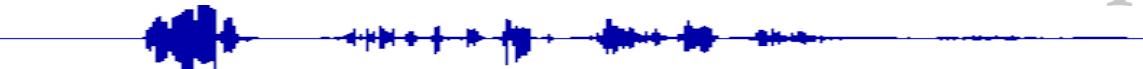


Move the dominant pole closer to the DC frequency.

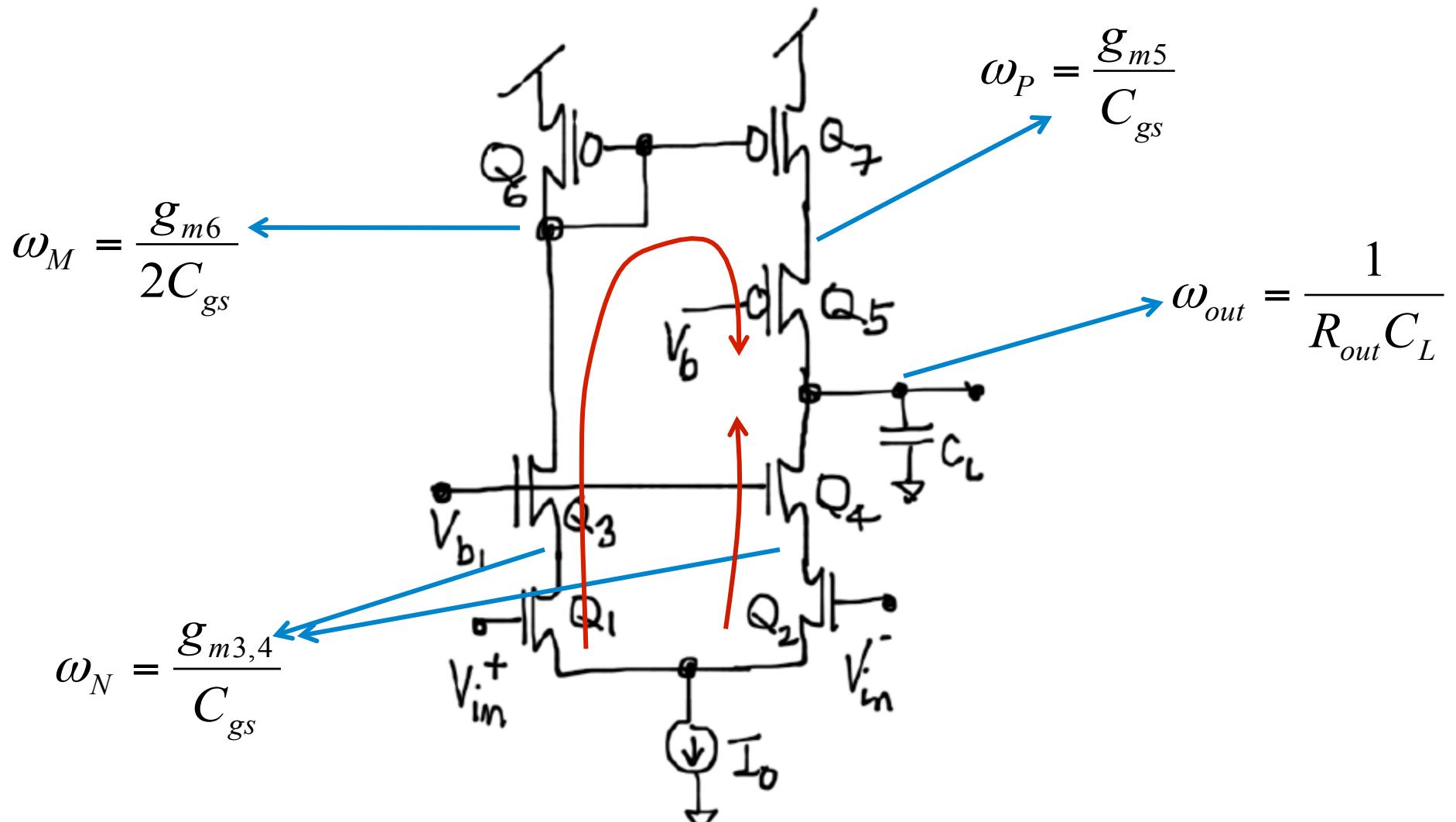


Eliminate or move the second dominant pole to a higher frequency.

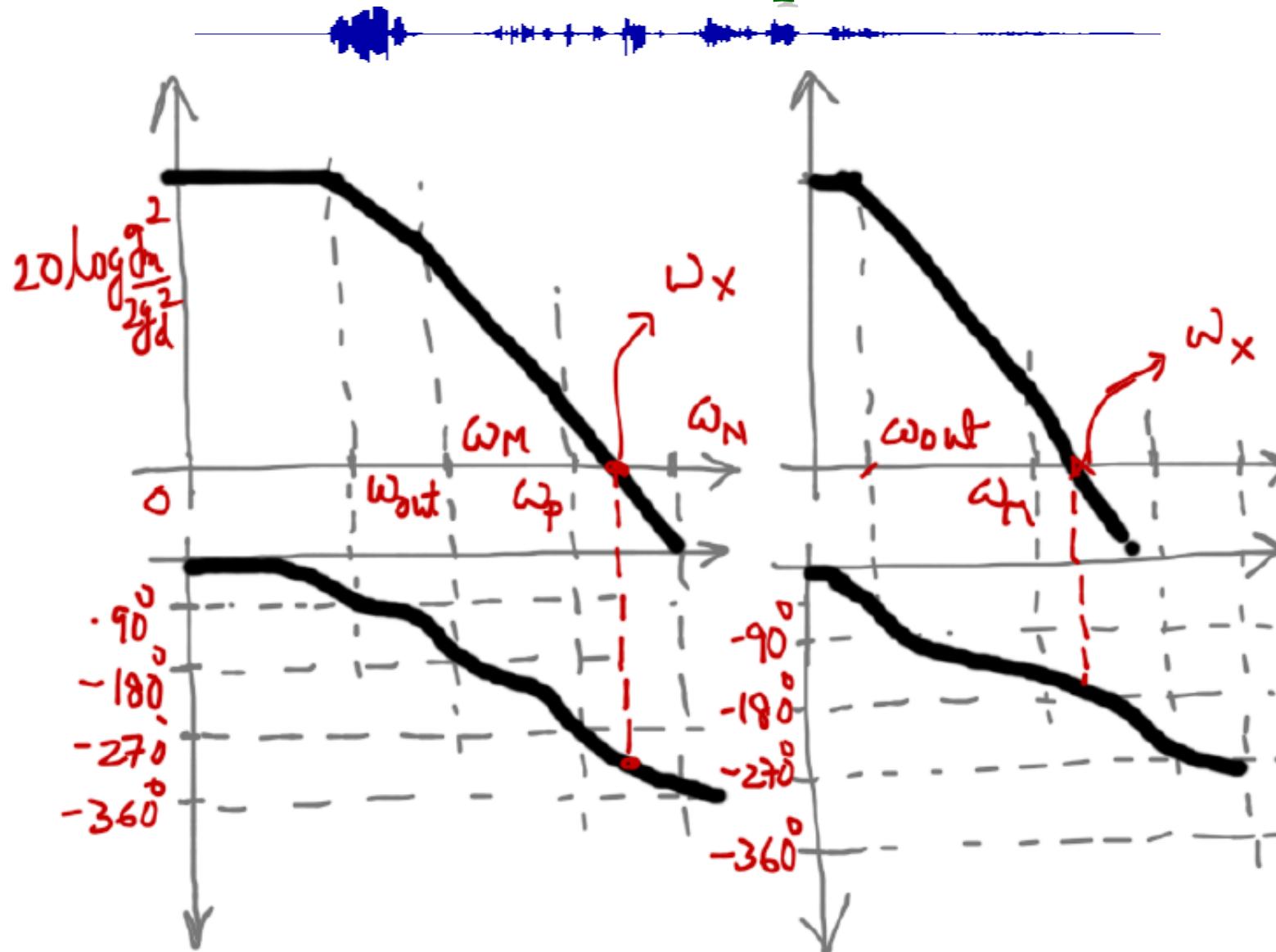
Example: Cascoded Differential Amplifier



Location of poles and zeros.



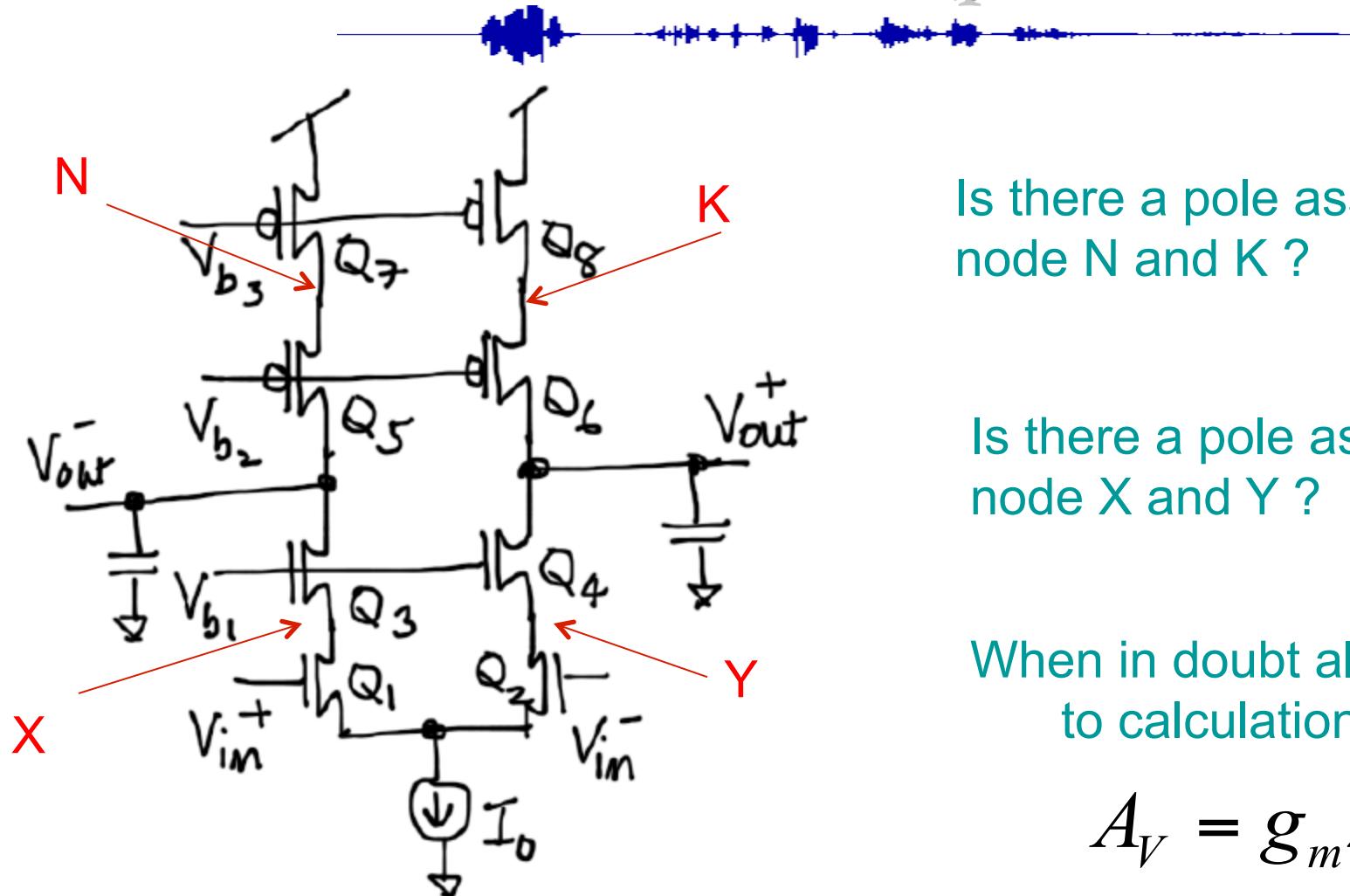
Cascoded Differential Amplifier



Add a load capacitor at the output stage.



Cascoded Differential Amplifier



Is there a pole associated with node N and K ?

Is there a pole associated with node X and Y ?

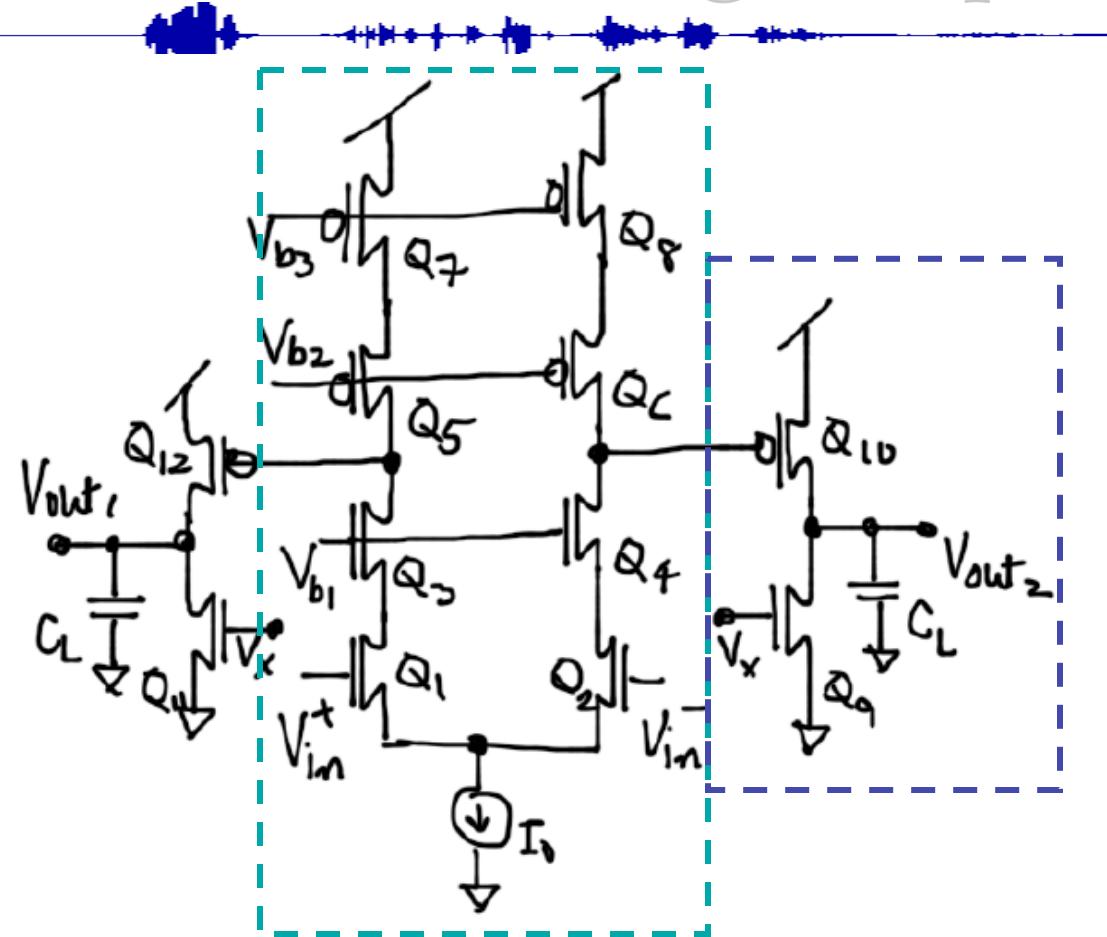
When in doubt always resort to calculations.

$$A_V = g_m Z_{out}$$

Eliminate the current mirror to improve the phase margin of the amplifier.



Compensation of Two-stage Amplifier



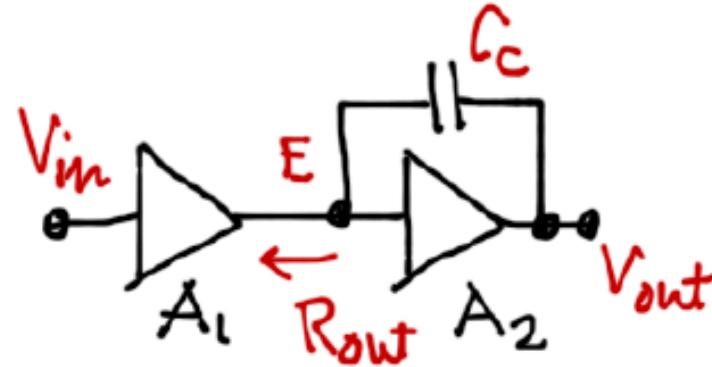
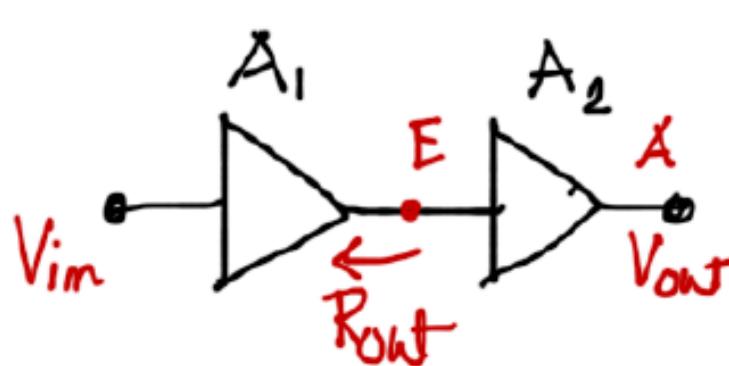
What is circuit is formed by transistors Q10 and Q9 ?

What is the gain of this circuit ?

How many poles and how many zeros does this amplifier have ?



Miller Compensation



$$Miller \ Effect \quad C_{eq} = C_E + (1 + A_{v2})C_C$$

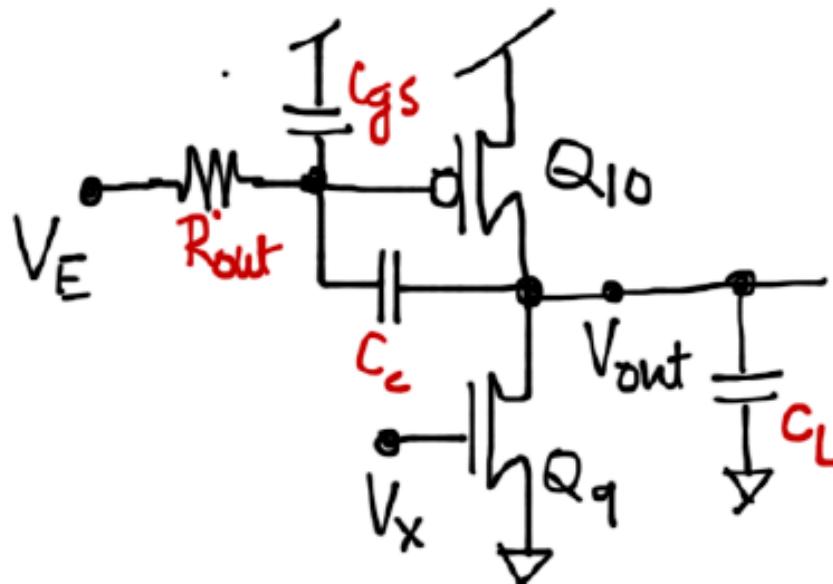
$$f_{pE} = \frac{1}{2\pi R_{out}[C_E + (1 + A_{v2})C_C]}$$

Increase the miller capacitance, which will move the location of the dominant pole towards the origin (increased phase margin).

Procedure known as miller compensation.



Compensation (cont.)



Coupling factor

$$f_{p,in} = \frac{1}{2\pi(R_{out}[C_E + (1 + g_m R_L)C_C] + R_L(C_C + C_L))}$$

$$f_{p,in} \approx \frac{1}{2\pi R_{out}[C_E + (1 + g_m R_L)C_C]}$$



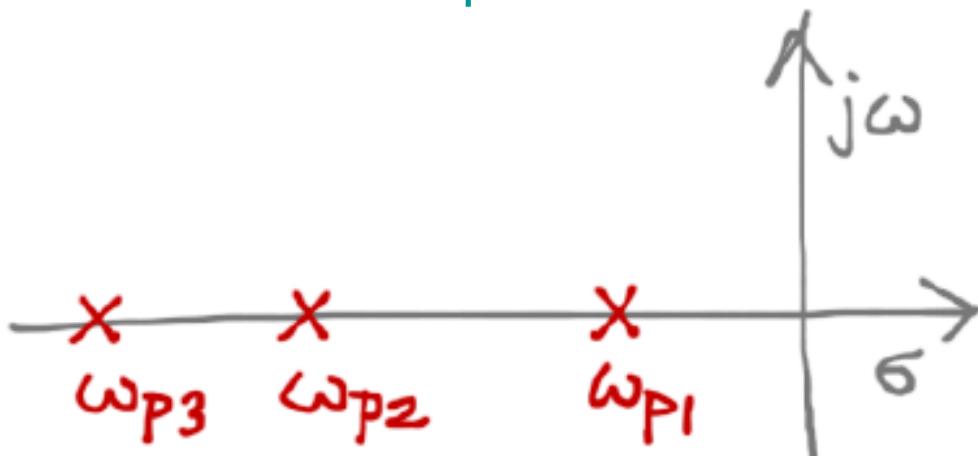
Compensation (cont.)



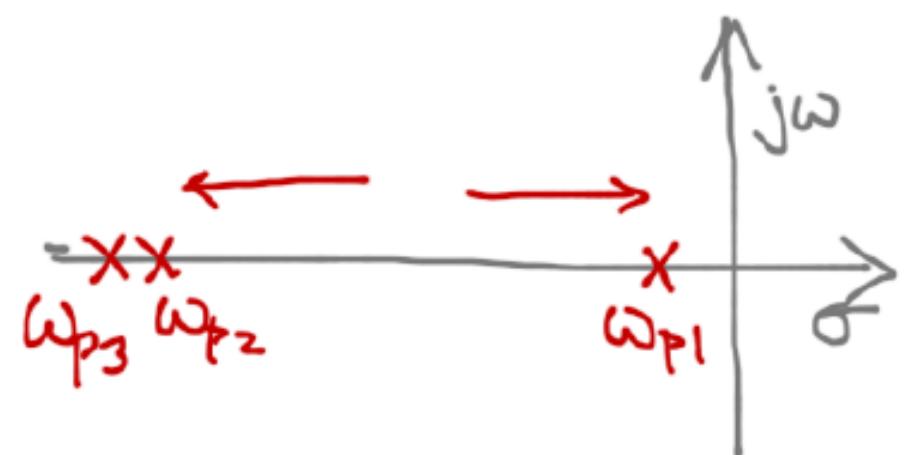
$$f_{p,out} = \frac{R_{out}(1 + g_{m9}R_L)C_C + R_{out}C_E + R_L(C_C + C_L)}{2\pi R_{out}R_L(C_EC_C + C_EC_L + C_CC_L)}$$

$$f_{p,out} \approx \frac{R_{out}g_{m9}R_LC_C + R_LC_C}{2\pi R_{out}R_L(C_EC_C + C_CC_L)} = \frac{g_{m9}}{2\pi(C_E + C_L)}$$

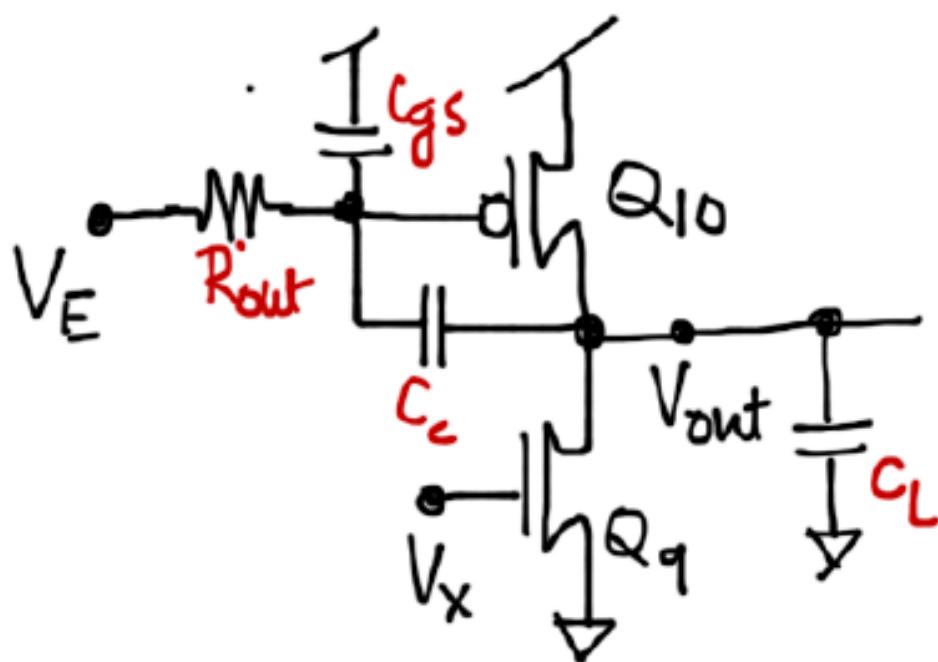
Before compensation



After compensation



Compensation (Cont.)



Miller compensation introduces a zero.

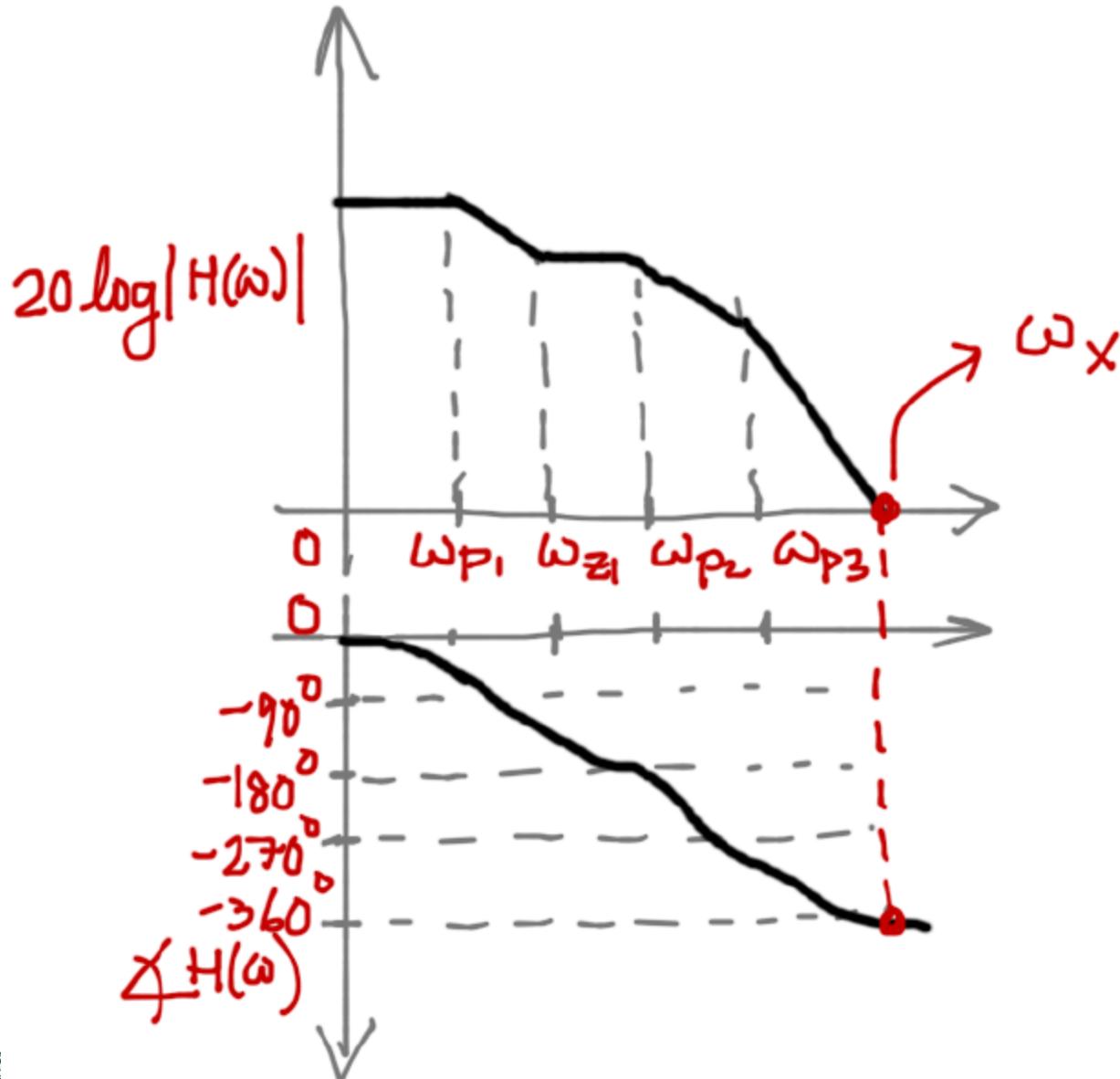
A zero due to the output stage which is located in the right hand plane.

Recall, transfer function includes
 $(1 - s / \omega_z)$ numerator term and

$$f_z(RHP) = \frac{g_{m9}}{2\pi C_C}$$

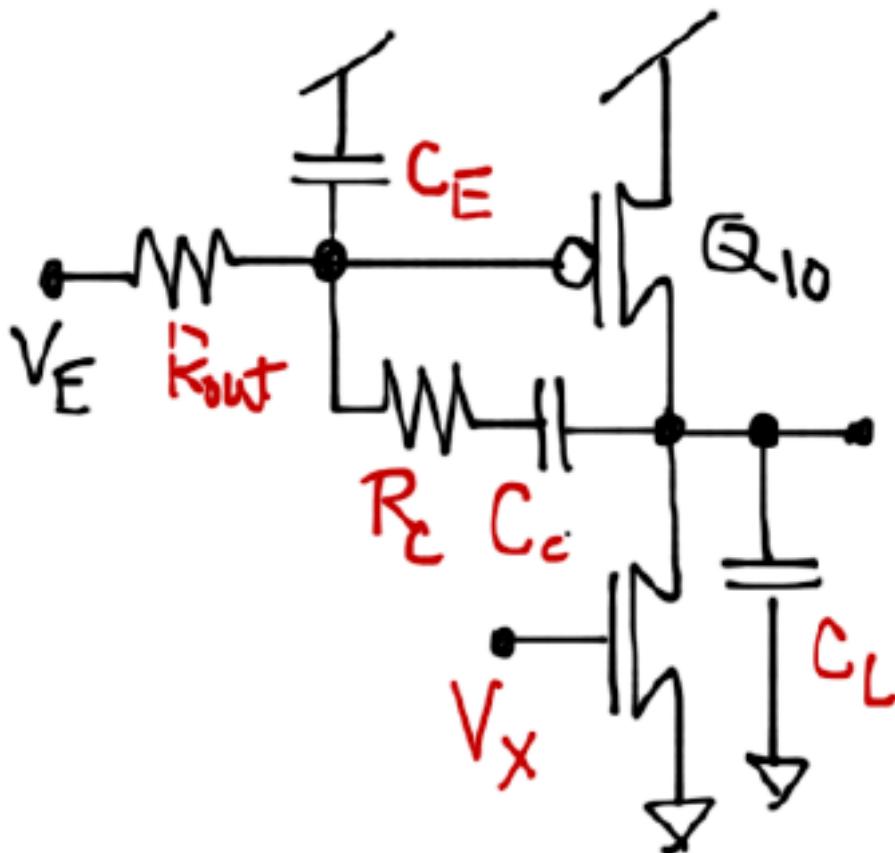


Phase and Magnitude of RHP Zero



Right hand zero creates stability problem because it causes a negative phase change.

Moving RHP zero to LHP



Add a compensation resistor along the miller path.

$$f_z = \frac{1}{2\pi C_C (1/g_{m9} - R_Z)}$$



Even better: Pole-zero cancellation



$$f_z = \frac{1}{2\pi C_C(1/g_{m9} - R_z)}$$

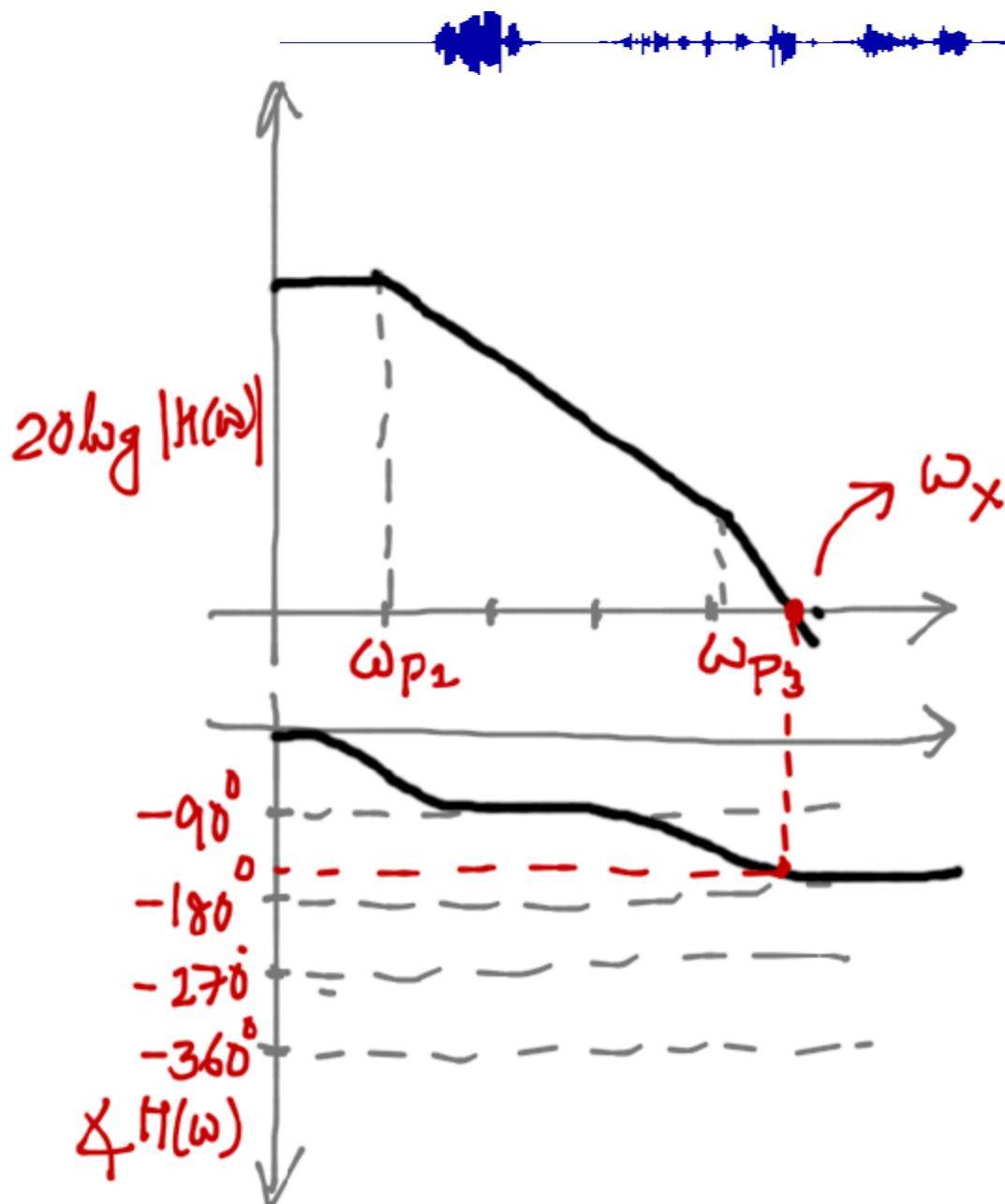
Could set $R_z = 1/g_{m9}$, or cancel
other non-dominant pole

$$\frac{1}{C_C(1/g_{m9} - R_z)} = \frac{-g_{m9}}{C_L + C_E}$$

$$R_z = \frac{C_L + C_E + C_C}{g_{m9} C_C} \approx \frac{C_L + C_C}{g_{m9} C_C}$$



Pole-zero Cancellation

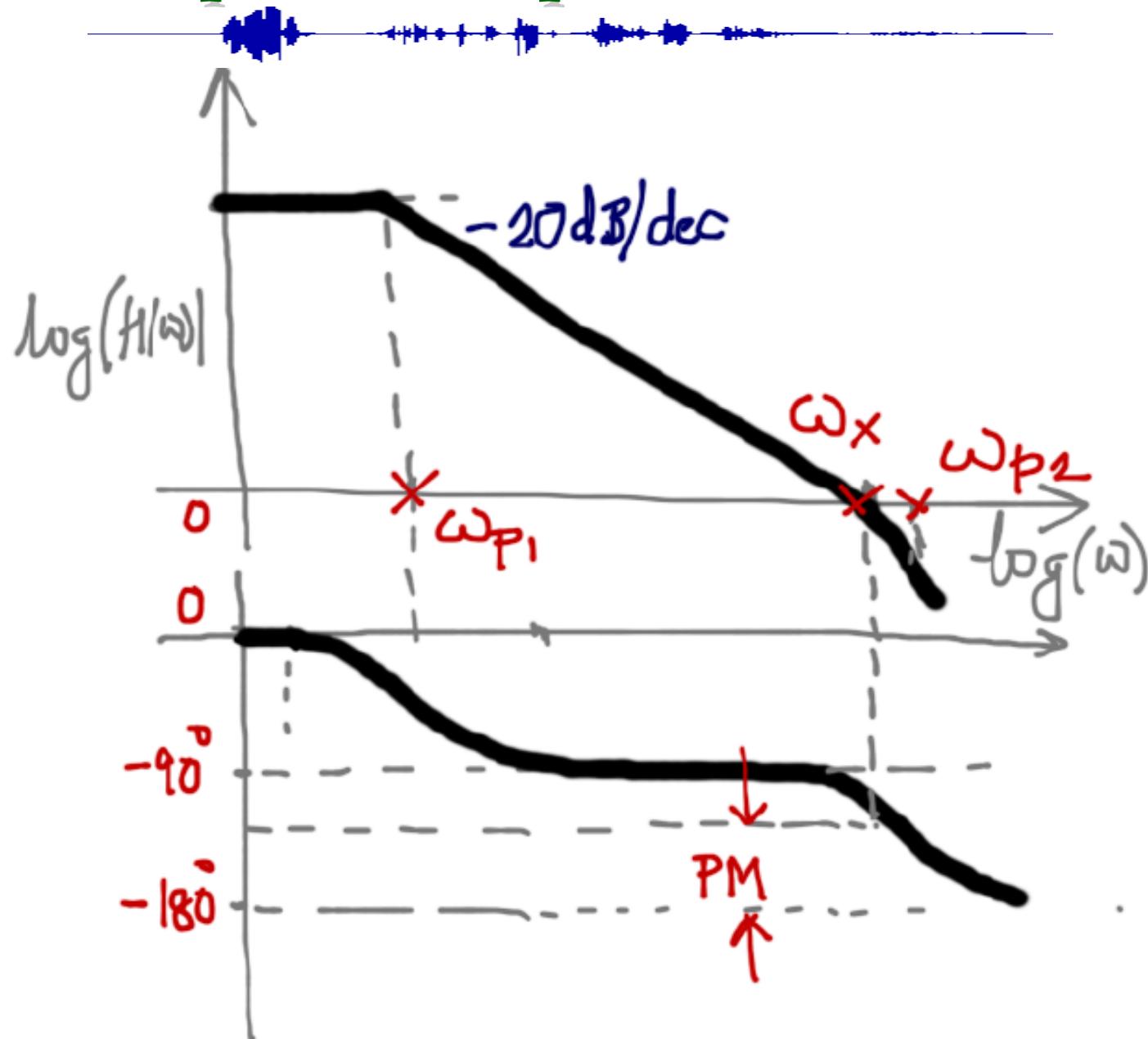


Move the zero to cancel the non-dominant pole.

Phase margin is now positive and the amplifier becomes stable.

Could increase the phase margin by moving the location of the remain pole to a higher frequency.

Desired Amplifier Response

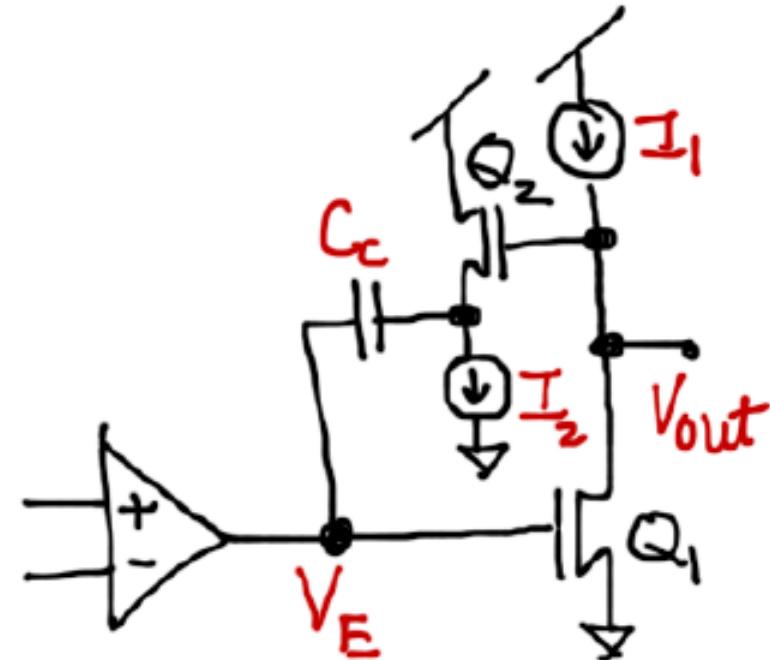
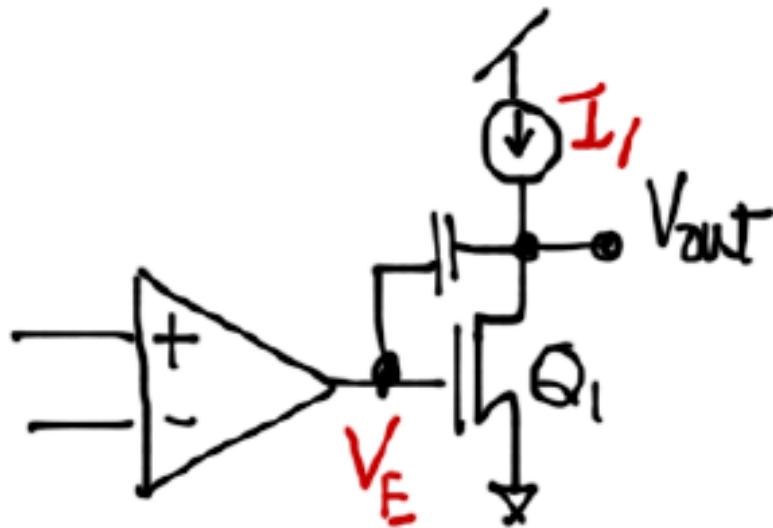


Other Compensation Techniques



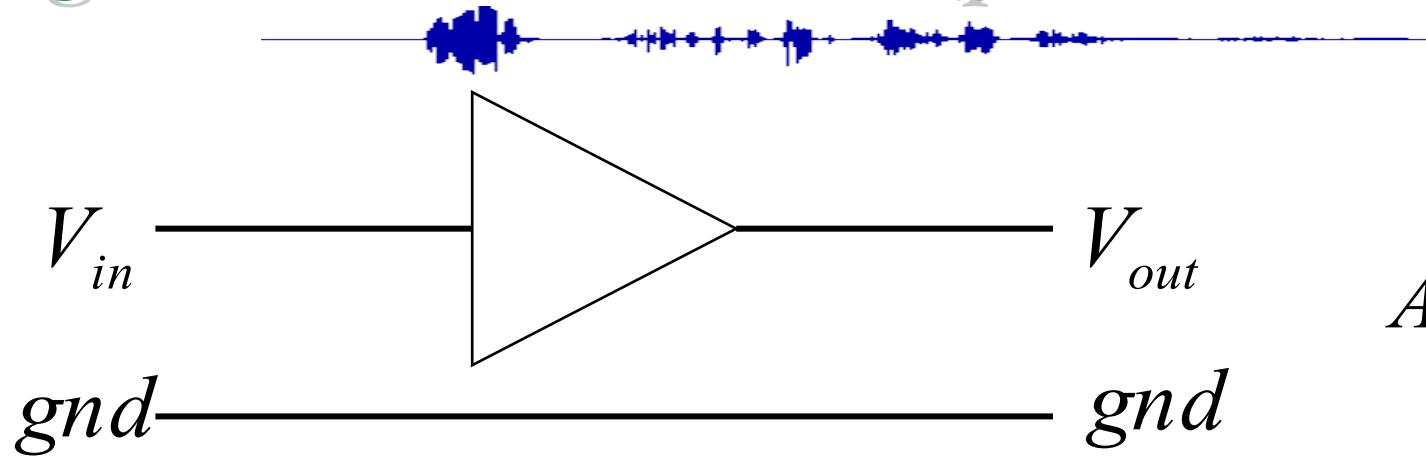
Compensation in two stage CMOS amplifier is difficult because of a feed-forward path formed by the compensation capacitor.

Eliminate the direct path from node X to the output node.

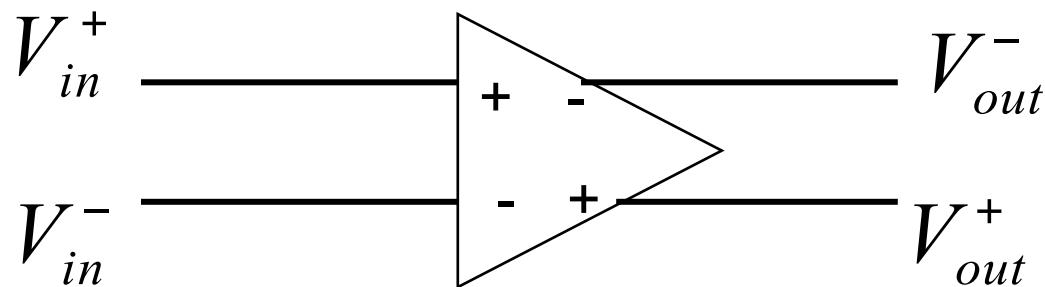


Moves the location of zero to high frequency.

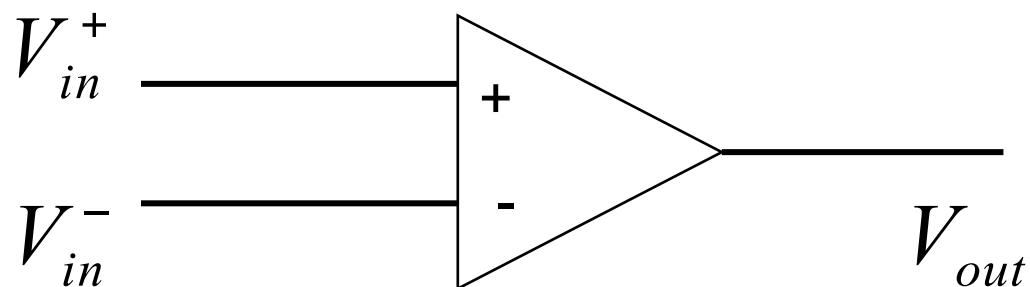
Single and differential amplifiers



$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}}$$



$$A_v = \frac{\Delta V_{out}^+ - \Delta V_{out}^-}{\Delta V_{in}^+ - \Delta V_{in}^-}$$



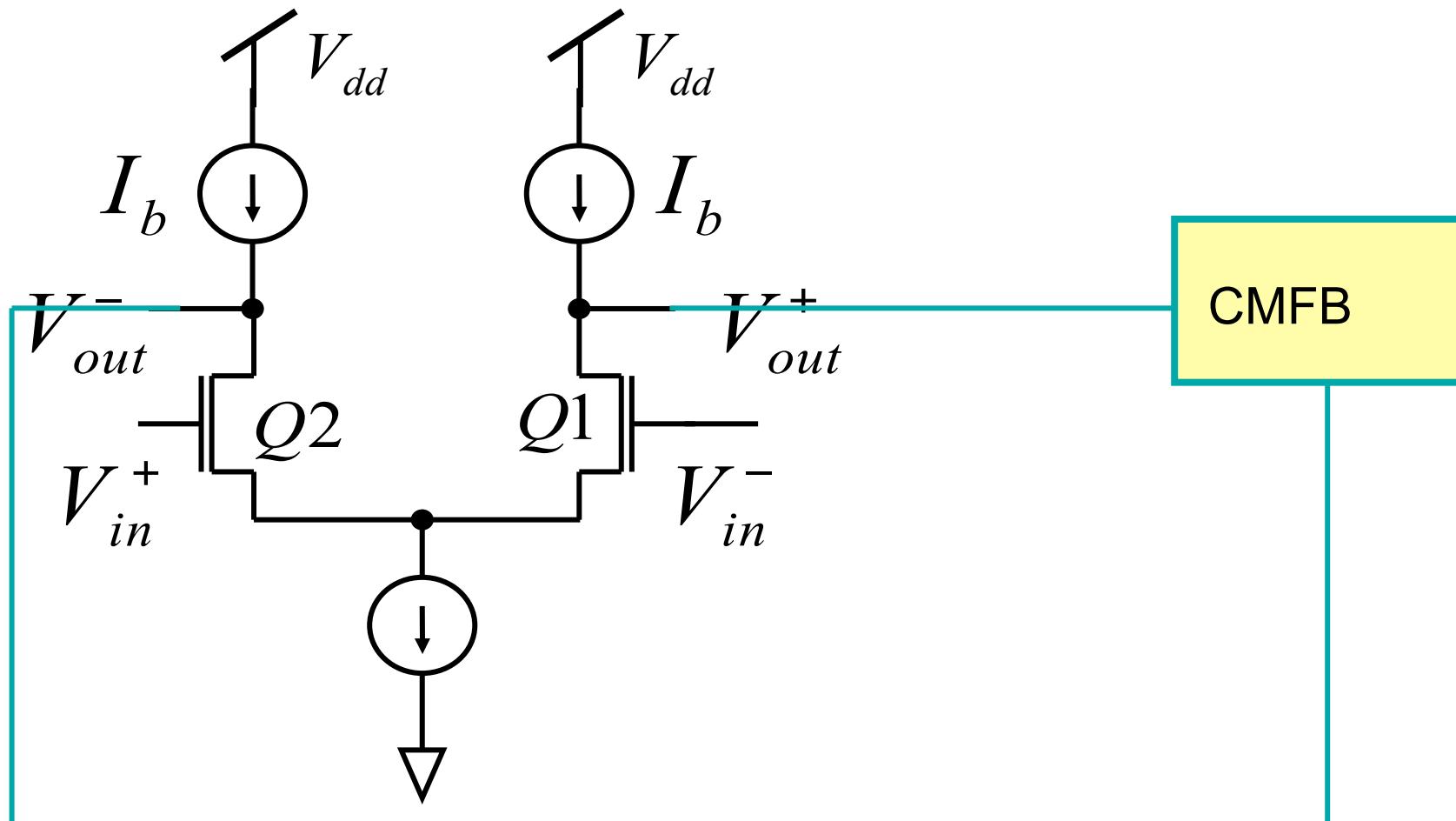
$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}^+ - \Delta V_{in}^-}$$



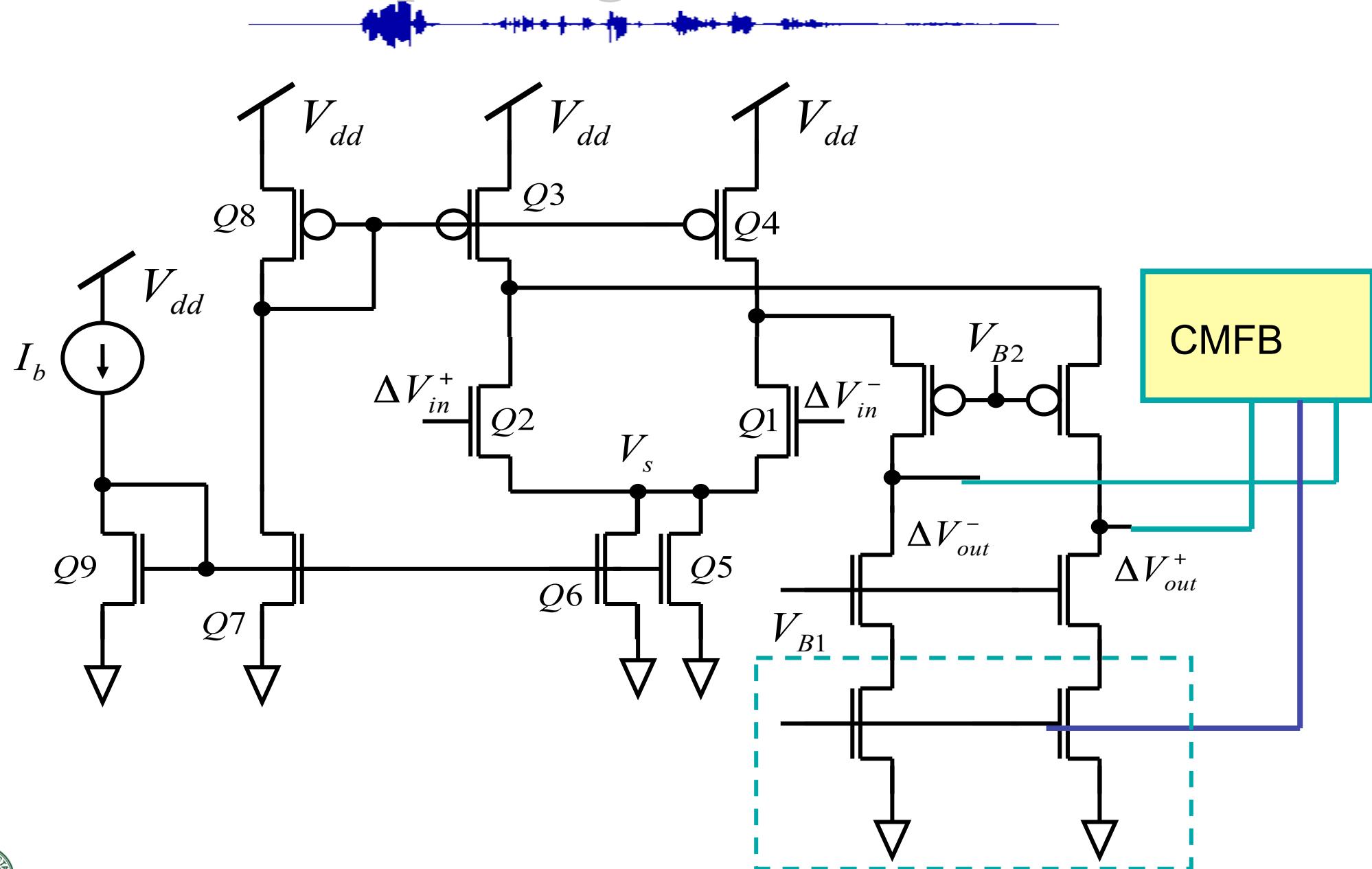
Common-mode Feedback

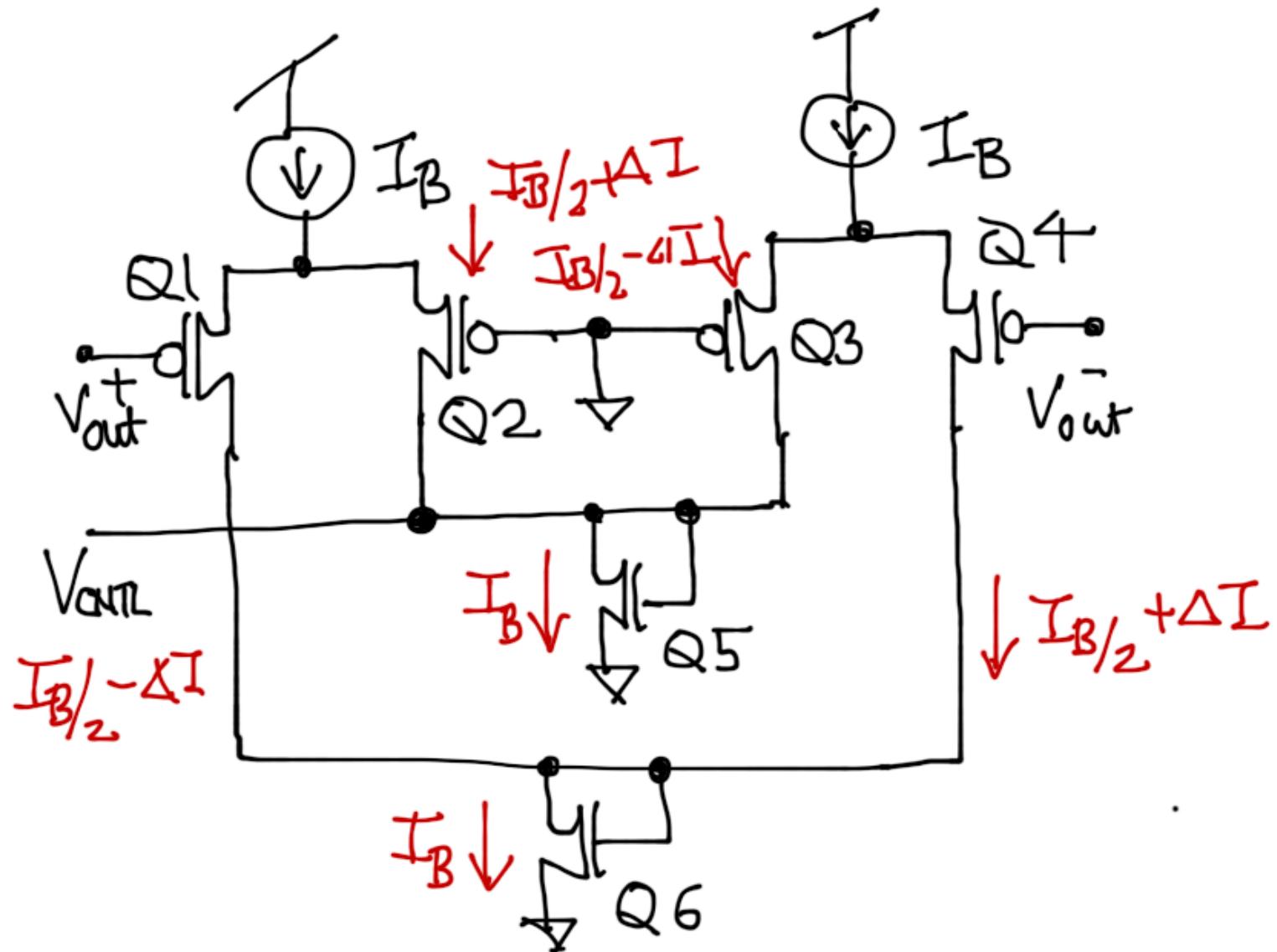
Purpose of CMFB is to fix the output common mode.

Cannot change the bias current of the input stage as this will change the gain



CMFB at Output Stage



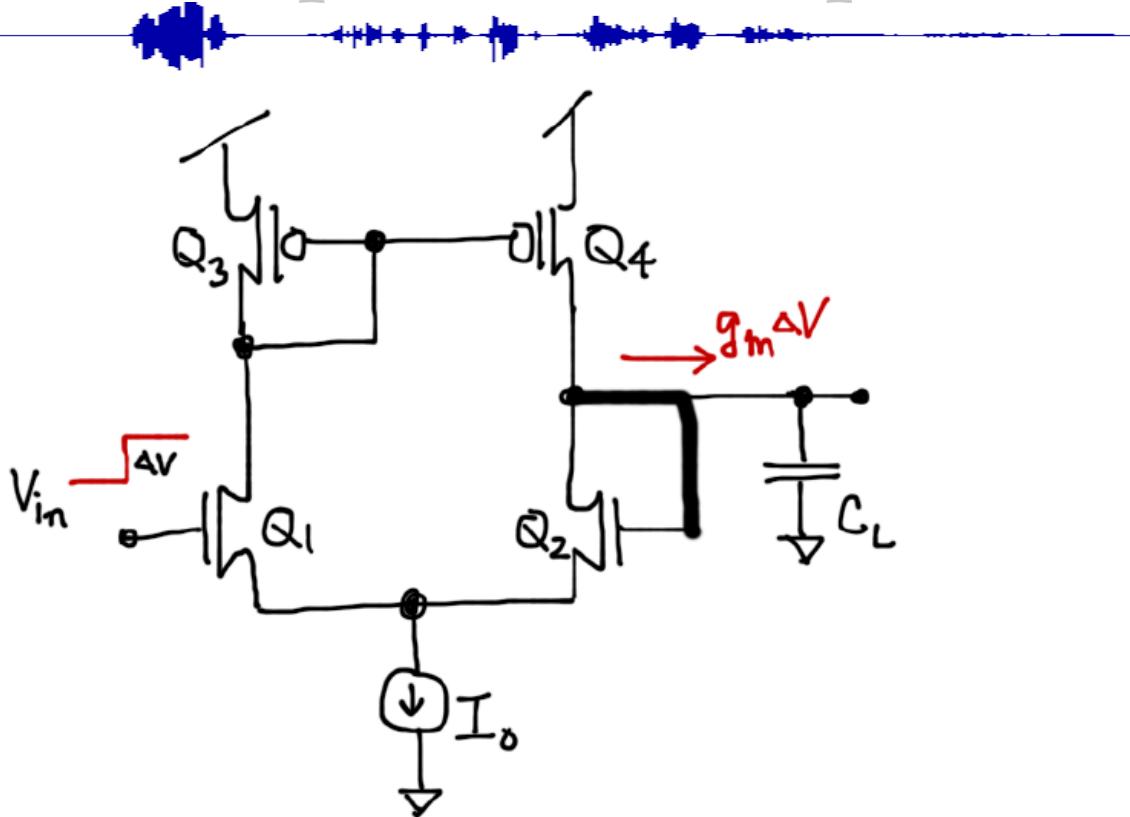


- Balanced signal on V_{out} does not affect V_{CNTL}
- Independent of small-signal analysis

Worksheet



Small-signal Response of Amplifier

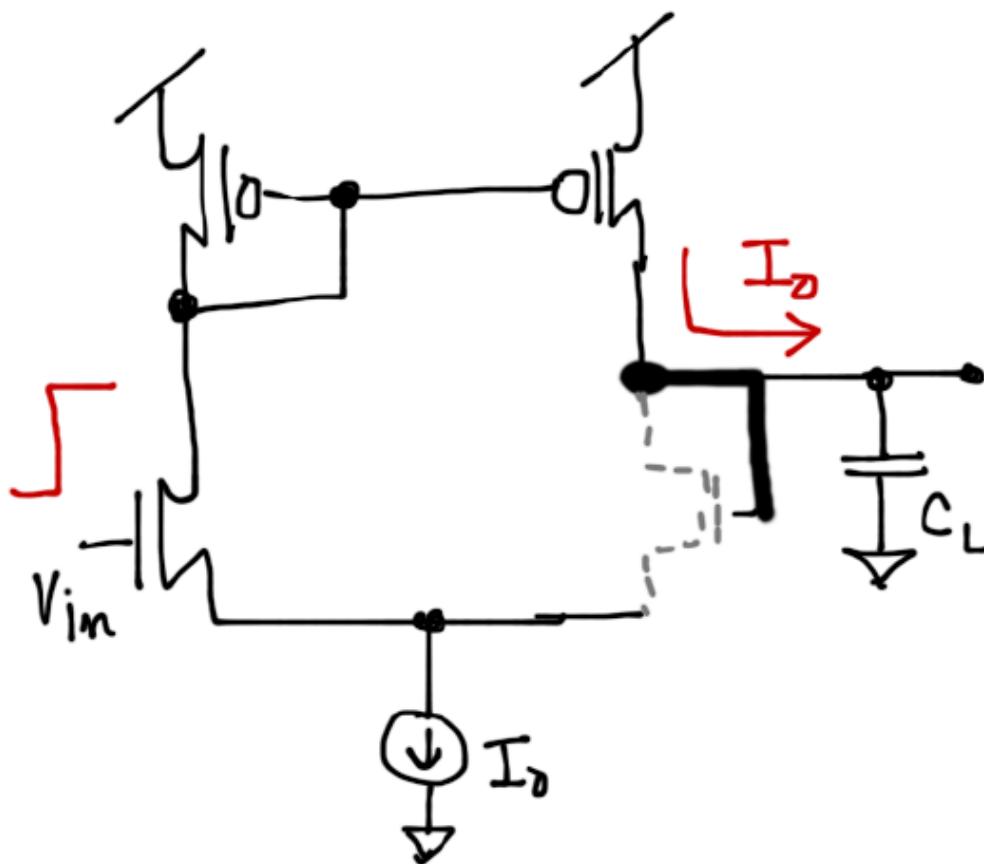


Till now we have considered frequency response of amplifiers based on small signal analysis.

Location of poles and zeros of a feedback amplifier is **FIXED** with respect to the amplitude of the signal.



Slew-rate of Amplifier



When one of the input undergoes a large change in amplitude the transistor will draw all the tail current (M2 will be off).

Under this condition the rate of increase in load capacitance is limited by the tail current.

$$SR = \frac{I_0}{C_L}$$

Slewing is a large signal phenomenon and determines how fast can the output signal change

Design of a Complete Amplifier



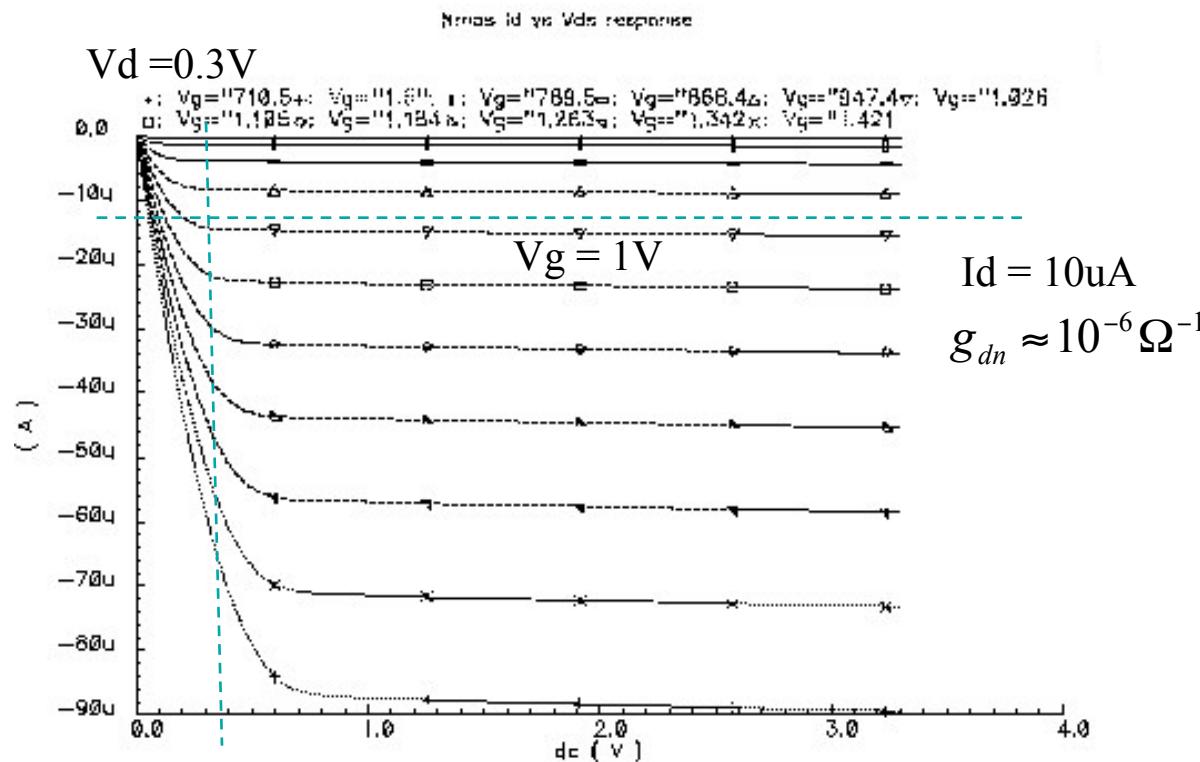
Parameters	Value
Gain	80dB
Output Voltage Swing	> 2.3 V
Supply Voltage	3V
Bandwidth	> 10 KHz @ 10pF load capacitance
Power Dissipation	< 100 uW
Phase margin	> 55 degrees



Single transistor simulations



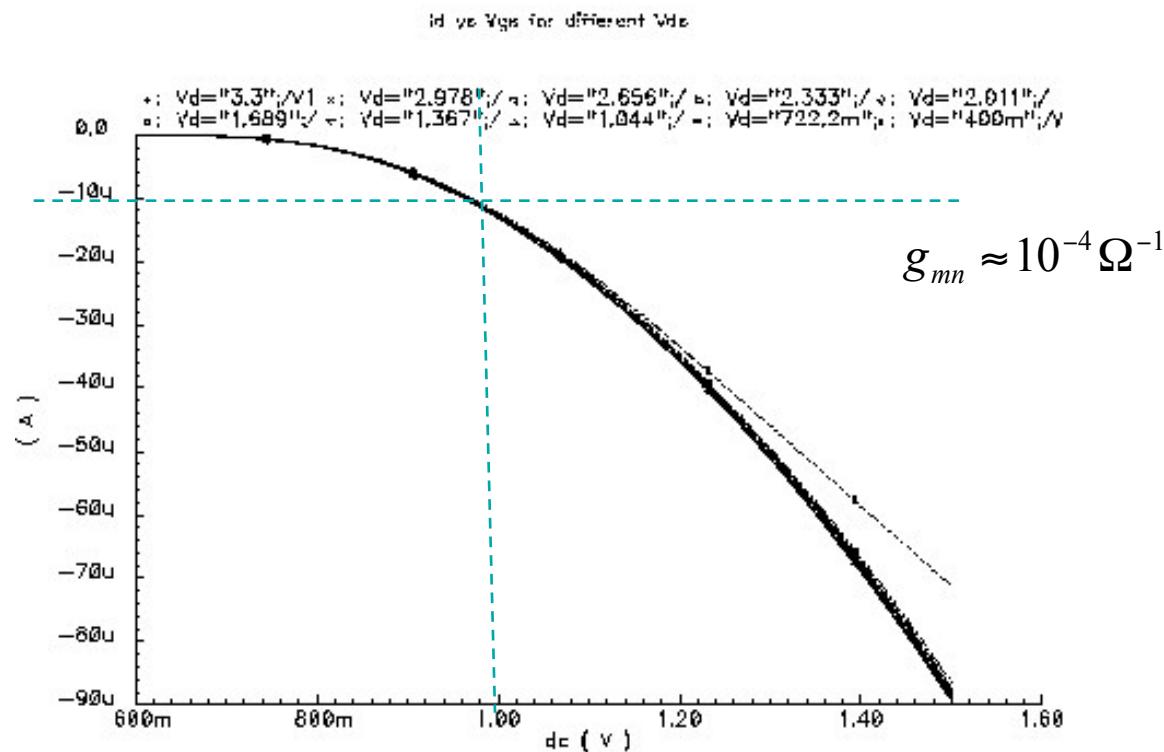
nMOS transistor plot: I_{ds} vs V_{drain} plot when V_{gate} is varied from 0.7V – 1.4V. The plot is inverted because the direction of current is negative.



Single transistor simulations



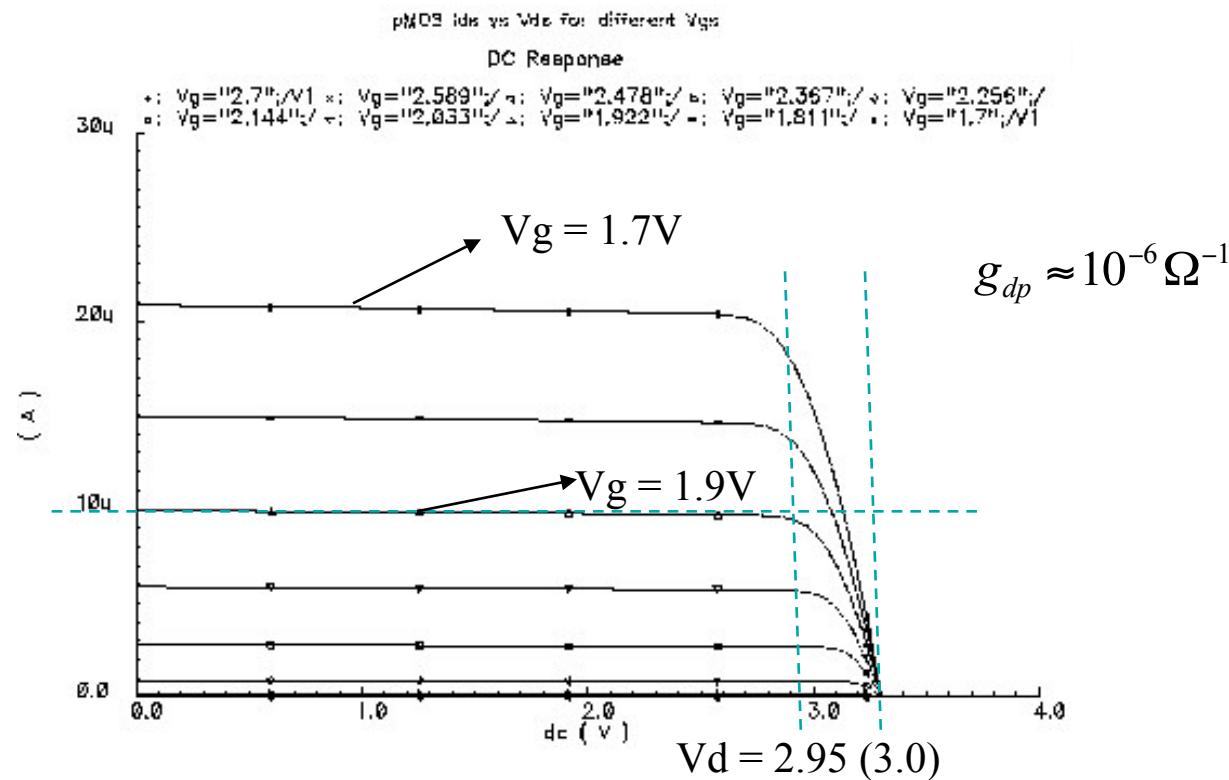
nMOS transistor plot: Ids vs Vgate plot when Vdrain is varied from 0.4V – 3.3V.



Single transistor simulations



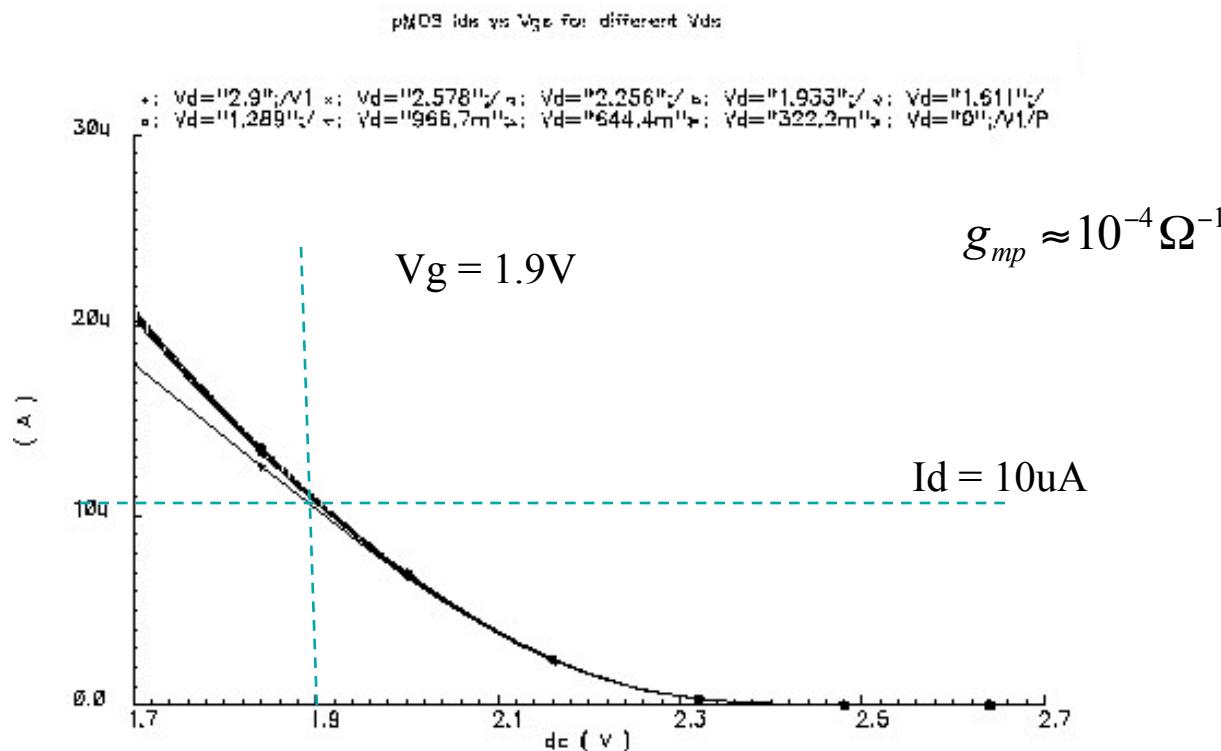
pMOS transistor plot: I_{ds} vs V_{drain} plot when V_{gate} is varied from 1.7 – 2.7V.



Single transistor simulation



pMOS transistor plot: I_{ds} vs V_{gate} plot when V_{drain} is varied from 0 – 2.9V.



Small signal and Biasing specifications



$$g_{mp} \approx 10^{-4} \Omega^{-1}$$

$$g_{mn} \approx 10^{-4} \Omega^{-1}$$

$$g_{dp} \approx 10^{-6} \Omega^{-1}$$

$$g_{dn} \approx 10^{-6} \Omega^{-1}$$

$$V_{dsat} \approx 300mV$$

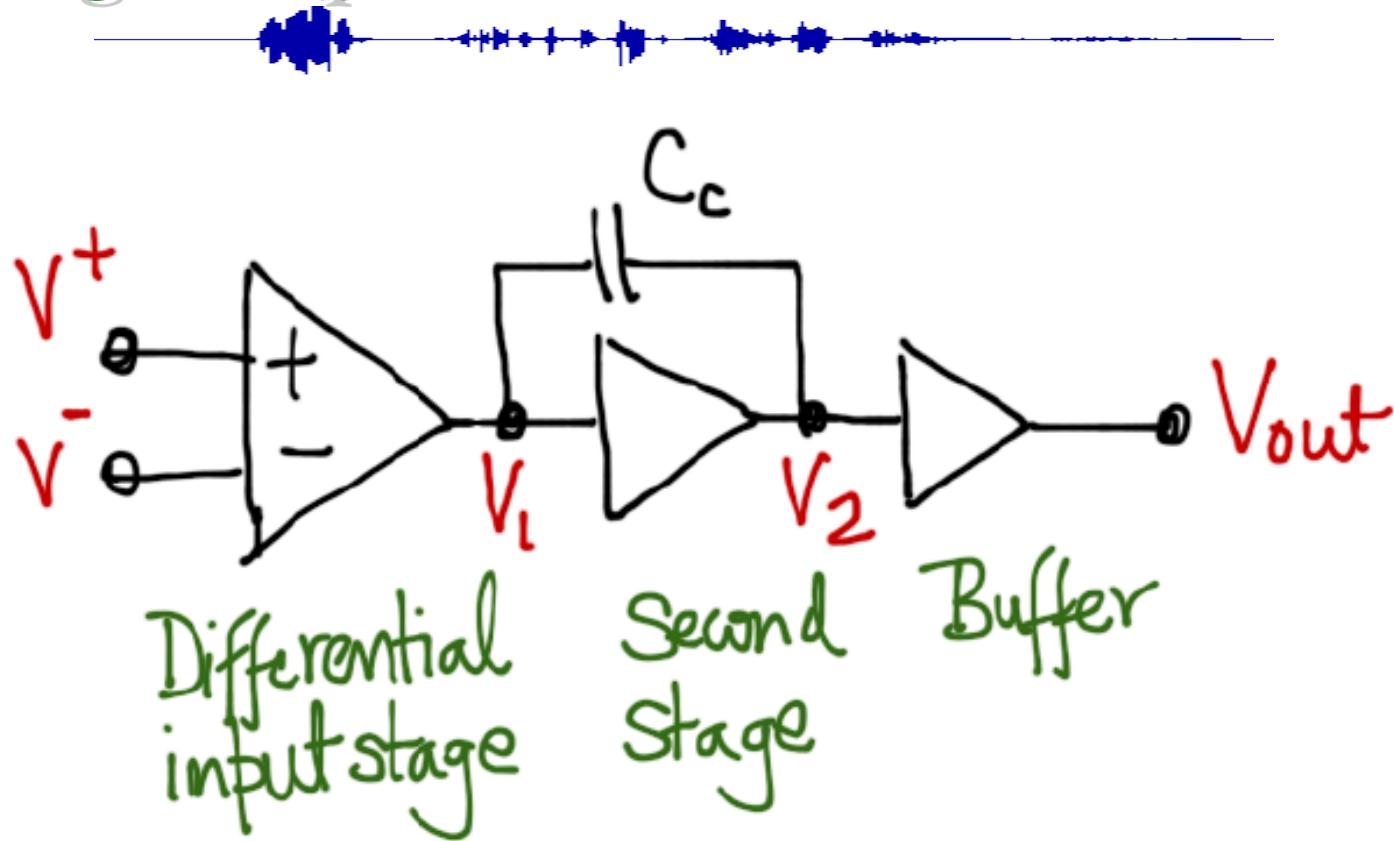
$$V_{bn} \approx 1V \quad \text{at } 10\mu A$$

$$V_{bp} \approx 1.9V \text{ at } 10\mu A$$

$$V_{th} \approx 800mV$$



Two-stage amplifiers

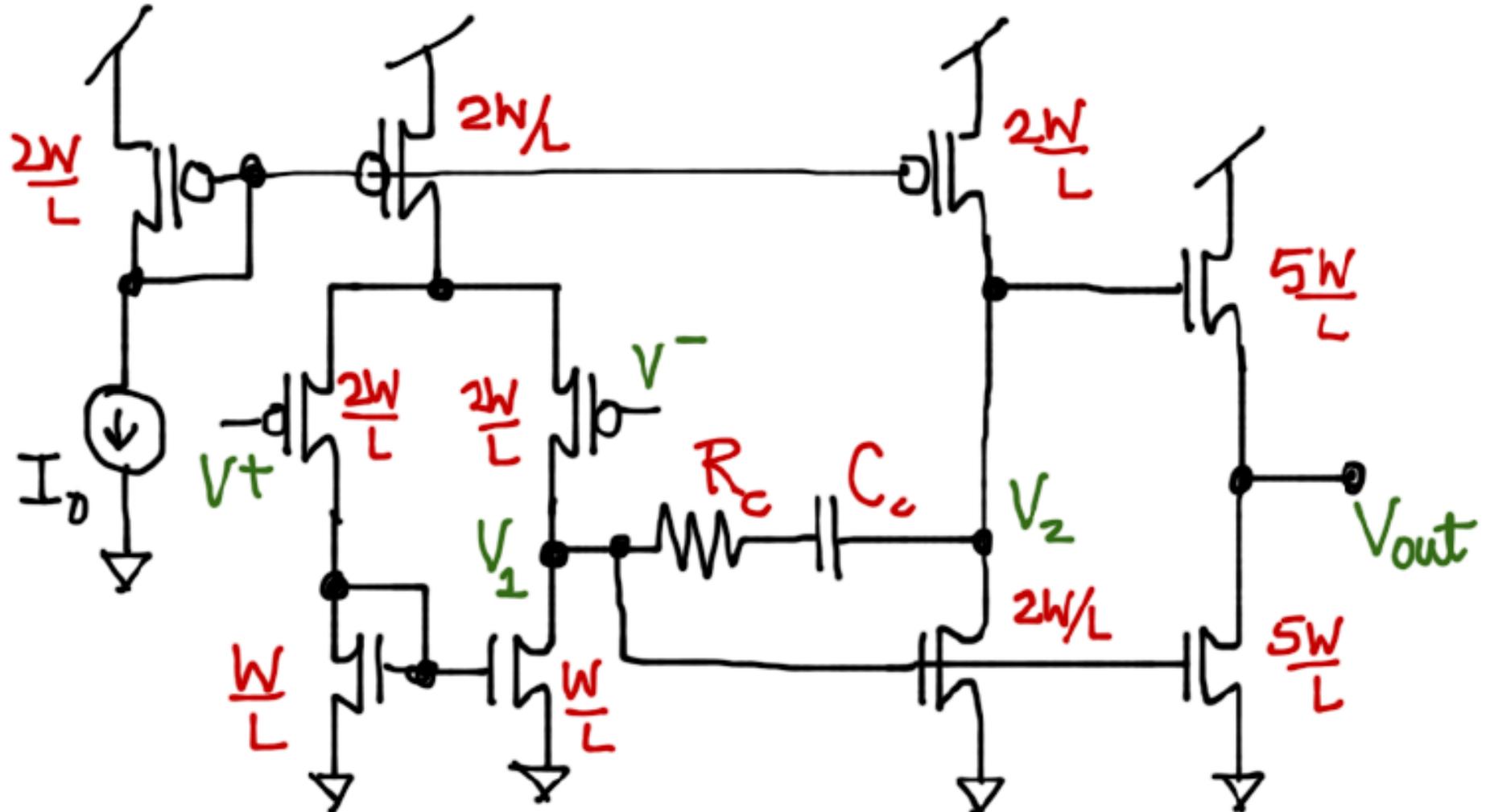


Miller capacitance for frequency compensation

Buffer to improve the load driving capability



Design of Complete Amplifiers



Design of Complete Amplifiers (cont..)



DC gain of the first stage

$$A_1 = -\frac{g_{mp}}{g_{dp} + g_{dn}}$$

DC gain of the second stage

$$A_2 = -\frac{g_{mp}}{g_{dp} + g_{dn}}$$

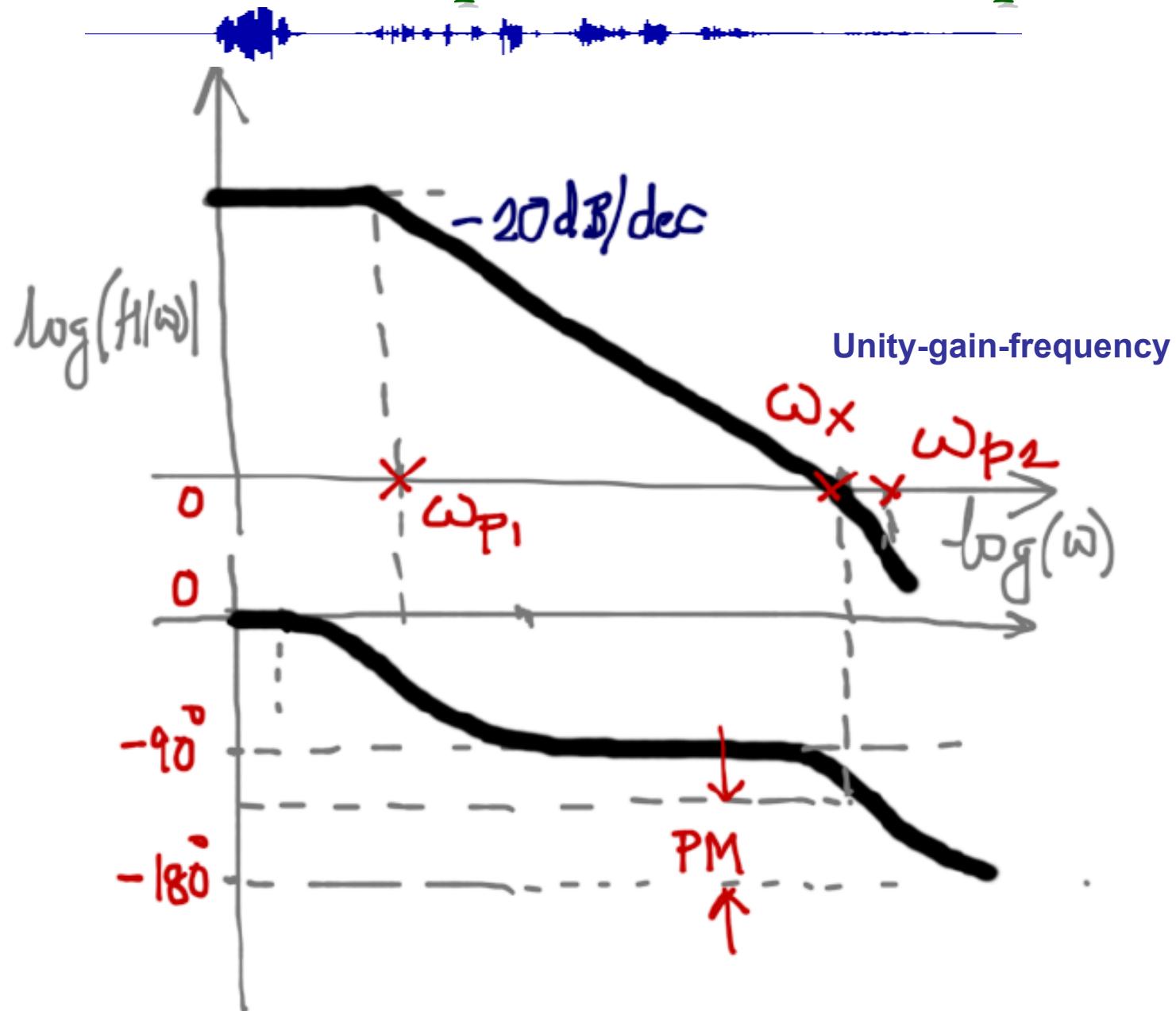
DC gain of the third stage (source follower)

$$A_3 \approx 1$$

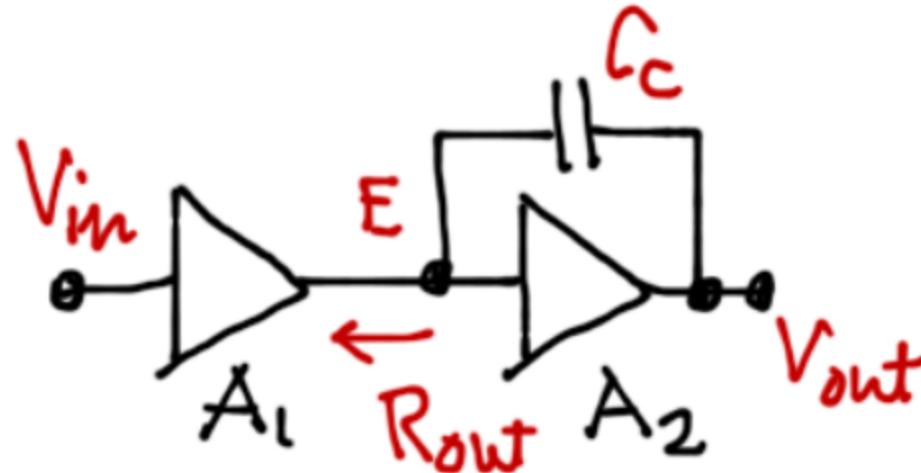
DC gain of the amplifier approximately 80dB.



Gain and Phase Response of the Amplifier



Calculate the Unity-gain-bandwidth



- Miller compensation

$$C_{eq} = C_E + (1 + A_2)C_C \approx A_2 C_C$$

- High-frequency gain

$$A_1(s) = -\frac{g_{mp}}{sC_{eq}} \quad A_1 A_2 = \frac{g_{mp}}{sC_c}$$

- Unity-gain-bandwidth $\omega_x = \frac{g_{mp}}{C_c}$



Slew-rate, Biasing and Unity-gain bandwidth



- Slew-rate of the amplifier $SR = \frac{I_0}{C_L} = V_{effp} \omega_x$
- Increase the slew-rate by increasing the effective voltage.
Reason for using a pMOS transistor as an input stage.
- Relationship between phase margin and location of the second pole.

$$\frac{\omega_x}{\omega_{p2}} \approx \tan(90^\circ - PM)$$

- 55 degrees PM implies the second pole should be located at 1.5 times the unity-gain bandwidth and will lead to a 13.3% overshoot.
- 75 degrees PM implies that second pole should be 4 times the unity-gain bandwidth and will lead to a 0.008% overshoot.



Compensating the Amplifier



- Choose an initial value of compensation capacitor and set the value of the compensation resistor to zero.
- Using simulations, find the unity-gain-frequency where one obtains a -180 + desired phase margin. Measure the gain **A** at that frequency.
- Scale the compensation capacitor by the gain **A**.
- Repeat previous two steps till convergence.
- Choose the compensation resistor value as $(1.2 \times \text{unity-gain-bandwidth} \times \text{compensation capacitor})^{-1}$.
- Using simulation find out the new phase margin.
- If phase margin is not sufficient then increase compensation capacitor while keeping the value of the compensation resistor unchanged.

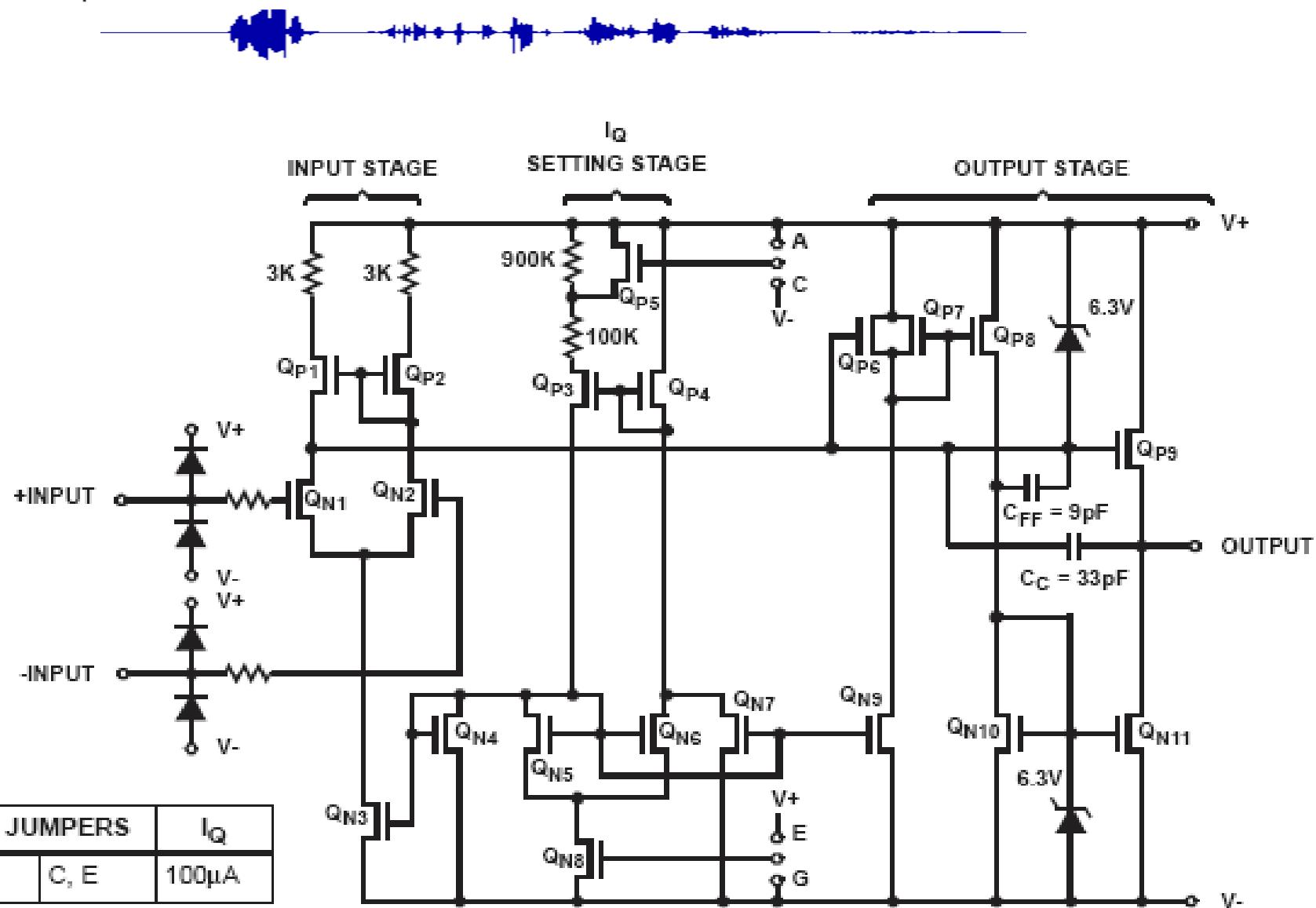




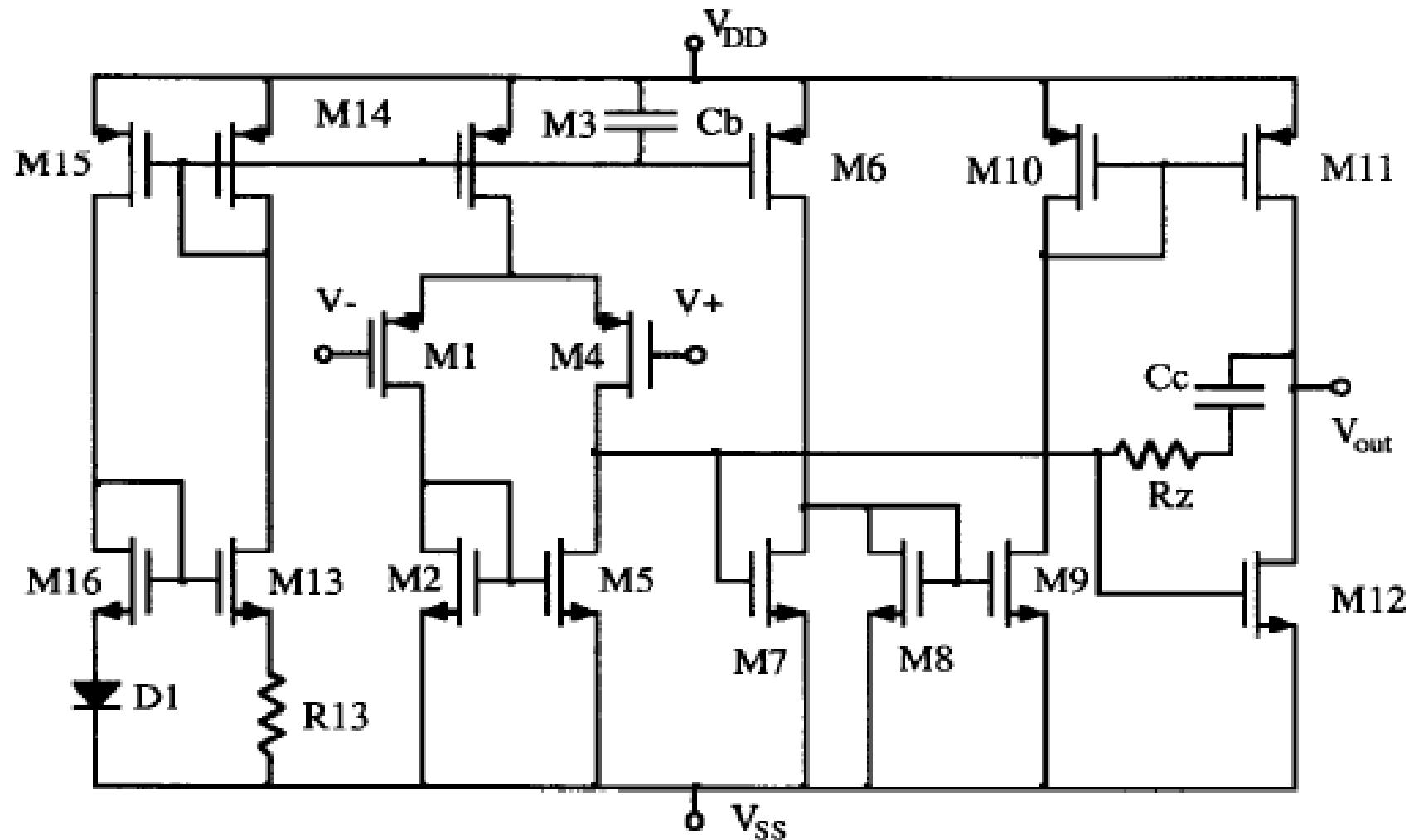
Electrical Specifications

 $V_{SUPPLY} = \pm 5V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7621B			ICL7621D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	5	-	-	15	mV
			Full	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	15	-	-	25	-	$\mu V/\text{°C}$
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	pA
			0 to 70	-	-	300	-	-	300	pA
			-55 to 125	-	-	800	-	-	800	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	pA
			0 to 70	-	-	400	-	-	400	pA
			-55 to 125	-	-	4000	-	-	4000	pA
Common Mode Voltage Range	V_{CMR}	$I_Q = 100\mu A$	25	± 4.2	-	-	± 4.2	-	-	V
Output Voltage Swing	V_{OUT}	$I_Q = 100\mu A, R_L = 100k\Omega$	25	± 4.9	-	-	± 4.9	-	-	V
			0 to 70	± 4.8	-	-	± 4.8	-	-	V
			-55 to 125	± 4.5	-	-	± 4.5	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 4.0V, R_L = 100k\Omega, I_Q = 100\mu A$	25	80	102	-	80	102	-	dB
			0 to 70	75	-	-	75	-	-	dB
			-55 to 125	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	$I_Q = 100\mu A$	25	-	0.48	-	-	0.48	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega, I_Q = 100\mu A$	25	70	91	-	70	91	-	dB
Power Supply Rejection Ratio ($V_{SUPPLY} = \pm 8V$ to $\pm 2V$)	PSRR	$R_S \leq 100k\Omega, I_Q = 100\mu A$	25	80	86	-	80	86	-	dB
Input Referred Noise Voltage	e_N	$R_S = 100\Omega, f = 1kHz$	25	-	100	-	-	100	-	nV/\sqrt{Hz}
Input Referred Noise Current	i_N	$R_S = 100\Omega, f = 1kHz$	25	-	0.01	-	-	0.01	-	pA/\sqrt{Hz}
Supply Current (Per Amplifier)	I_{SUPPLY}	No Signal, No Load, $I_Q = 100\mu A$	25	-	0.1	0.25	-	0.1	0.25	mA
Channel Separation	V_{O1}/V_{O2}	$A_V = 100$	25	-	120	-	-	120	-	dB
Slew Rate	SR	$A_V = 1, C_L = 100pF, V_{IN} = 8V_{P-P}, I_Q = 100\mu A, R_L = 100k\Omega$	25	-	0.16	-	-	0.16	-	$V/\mu s$
Rise Time	t_R	$V_{IN} = 50mV, C_L = 100pF, I_Q = 100\mu A, R_L = 100k\Omega$	25	-	2	-	-	2	-	μs
Overshoot Factor	OS	$V_{IN} = 50mV, C_L = 100pF, I_Q = 100\mu A, R_L = 100k\Omega$	25	-	10	-	-	10	-	%



Another amplifier



Yet another amplifier

