CSE562M: Analog Integrated Circuits Project1

In this assignment you need to simulate the DC and transient response of the following amplifier and complete the table shown below. You also have to choose the sizes of the transistors. As a starting point, you could choose the width and length of all the transistors to be 6 µm and 3 µm respectively. Assume V_{dd} = 3V and the maximum load connected to the output is 10pF.

1. Use DC analysis to determine the gain of the amplifier. Remember for DC analysis, set V_{in}^- to 1.5V and then sweep V_{in}^+ from 0 to 3V. The output of the amplifier should transition from a voltage close to zero to a voltage close to V_{dd} (around 1.5V). Zoom into the transition region and using the marker determine the maximum slope. The gain is 20 $\log_{10}$ (magnitude of the slope). Repeat this for bias current I_b values of 1nA ,10nA, 100nA, 1µA. The value of the capacitor C should not affect the DC analysis [5 point].

2. Using the amplifier create a voltage follower (buffer) as shown in Fig. 1 (right). Apply a 100mV step input (1.45V – 1.55V) (see Fig. 1(right)) and then plot the step response corresponding to the output of the amplifier. Estimate the settling time of the buffer (time for the output to stabilize to 90% of its steady-state value – see Fig. 1) and the voltage overshoot if any. Repeat this experiment for capacitance C values of 0pF, 0.1pF, 1pF and 10pF and bias current values I_b 1nA ,10nA, 100nA, 1µA [10 points].

3. Explain your observations based on the poles and zeros of the amplifier [5 points].

I_b	C	Gain(db)	Settling Time	Dynamic Range	Power

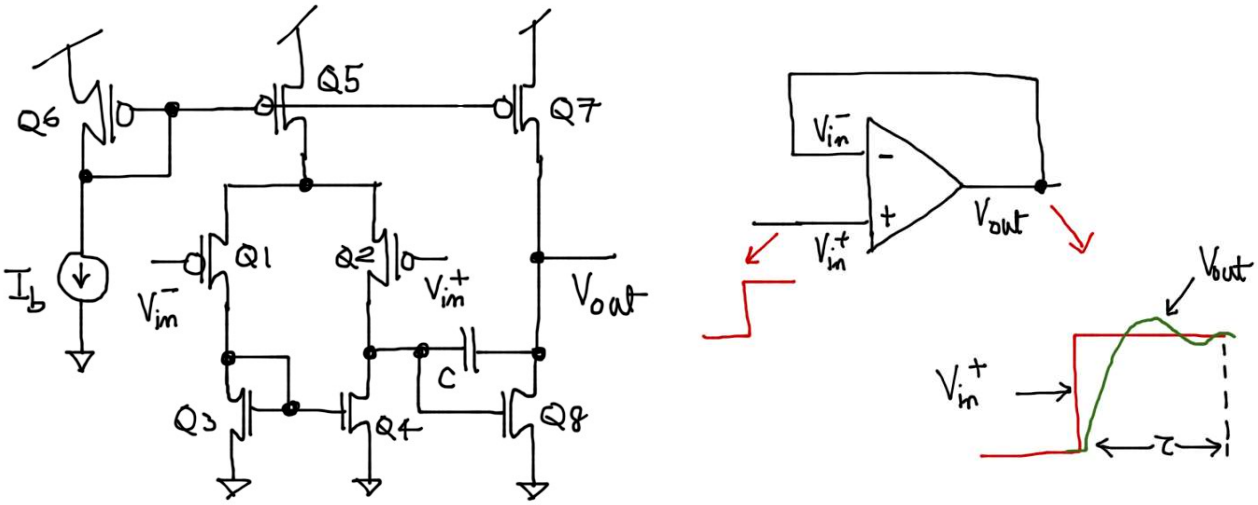

Fig. 1