



MOSFET Models

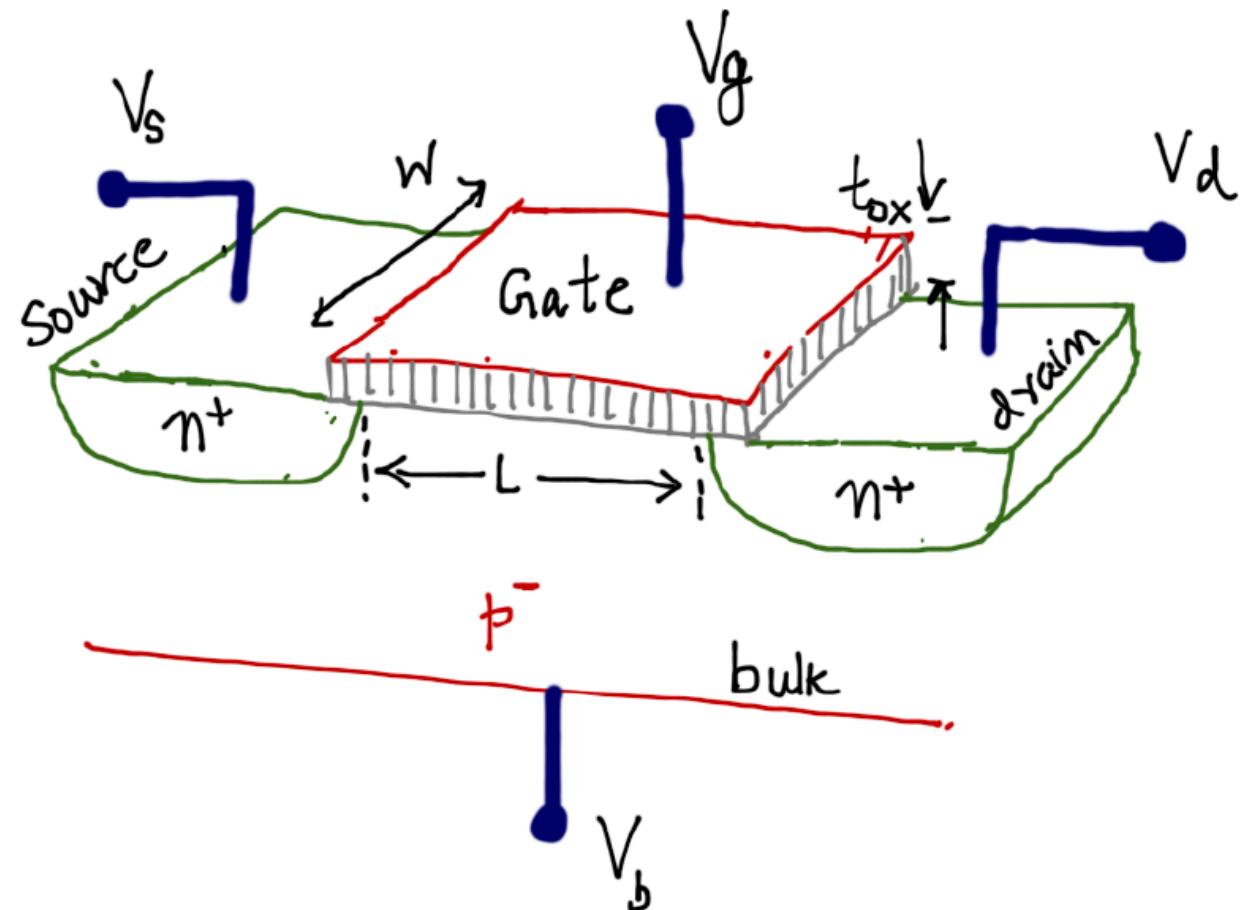


CSE562: Analog Integrated Circuit Design
Shantanu Chakrabartty



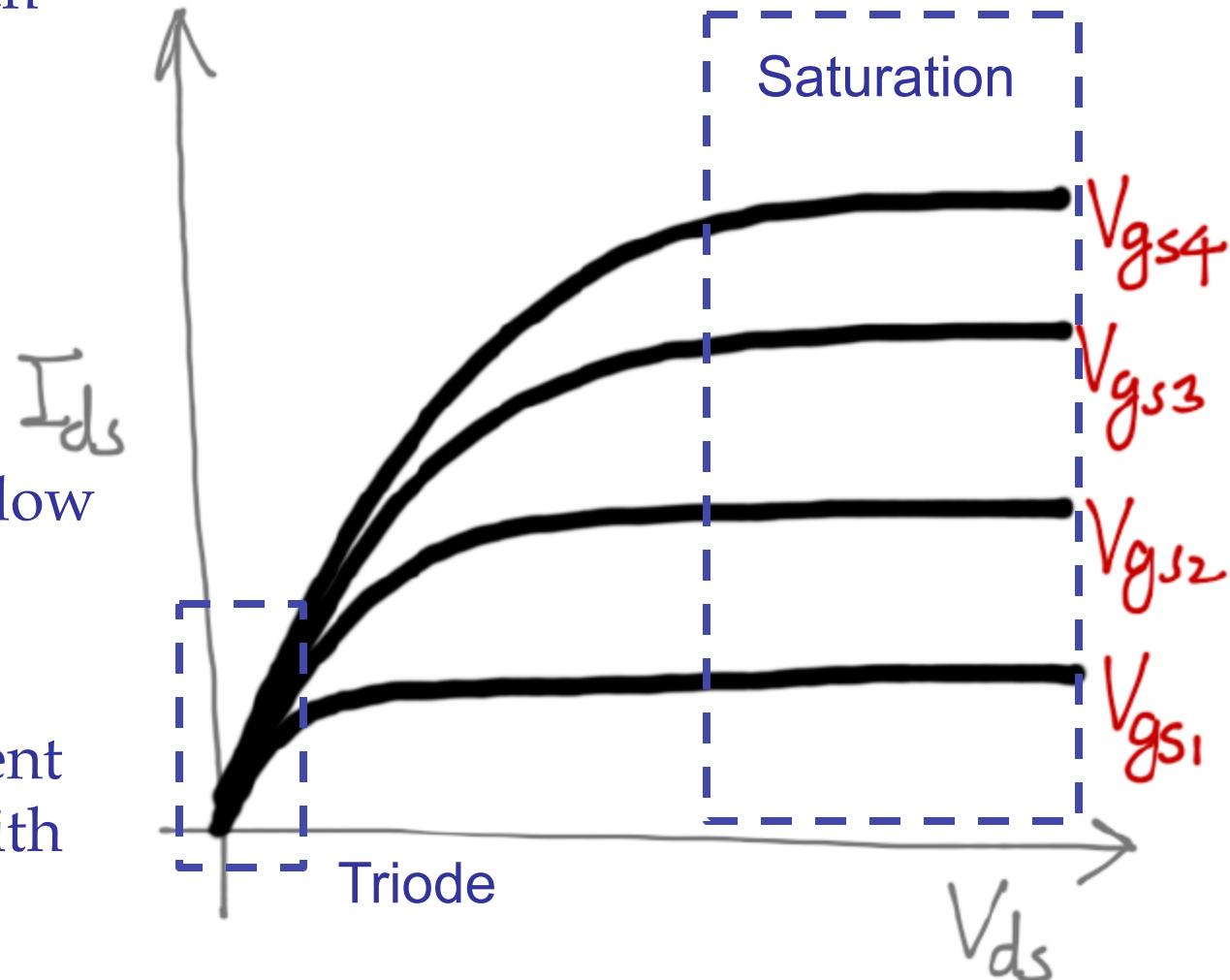
Structure of an n-type MOSFET (nMOS)

- Four terminals: source, drain, gate and bulk.
- Current (electrons) flow between the source and drain terminals.
- The gate terminal controls the flow.
- nMOS transistor: source and drain are formed by n^+ semi-conductor.
- Bulk connected to the lowest potential.



Ideal nMOS Large Signal Model

- Only will be dealing with accumulation mode MOSFETs.
- Current increases when drain-to-source voltage increases.
- **Triode region:** current flow increases linearly with drain-to-source voltage.
- **Saturation region:** current flow does not change with drain-to-source voltage.



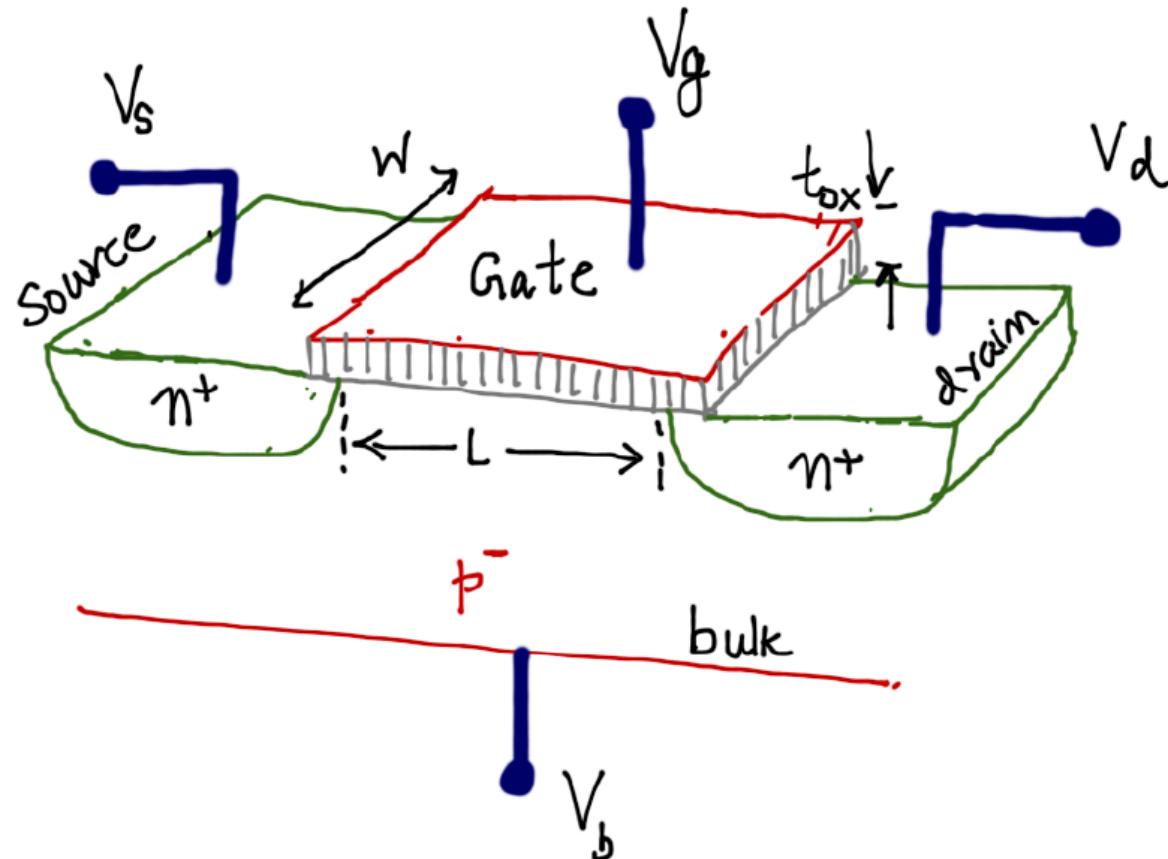
Derivation of Large-signal Model

W width of the gate

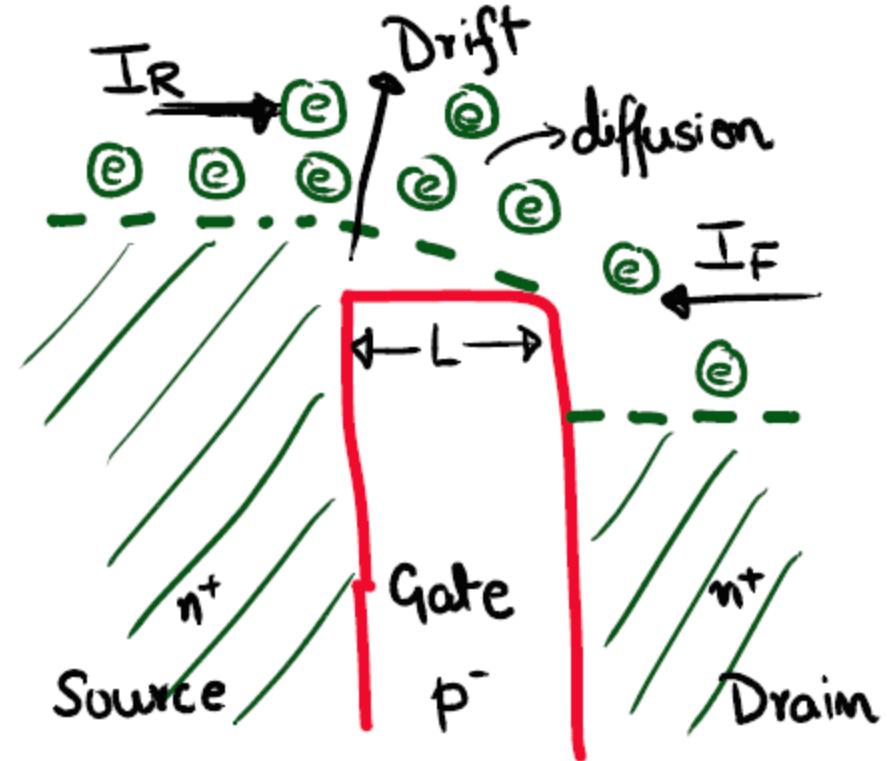
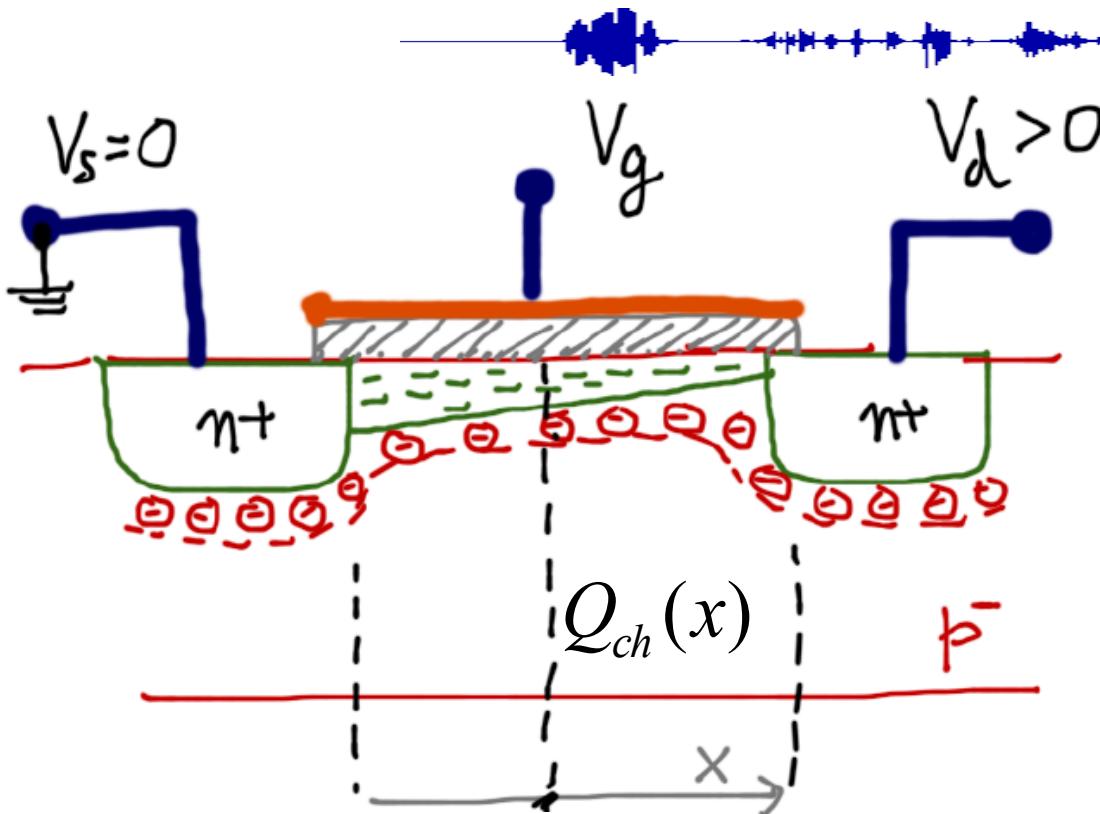
L Length of the channel (distance between source and drain)

V_{th} Threshold voltage

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$
 Gate capacitance per unit area



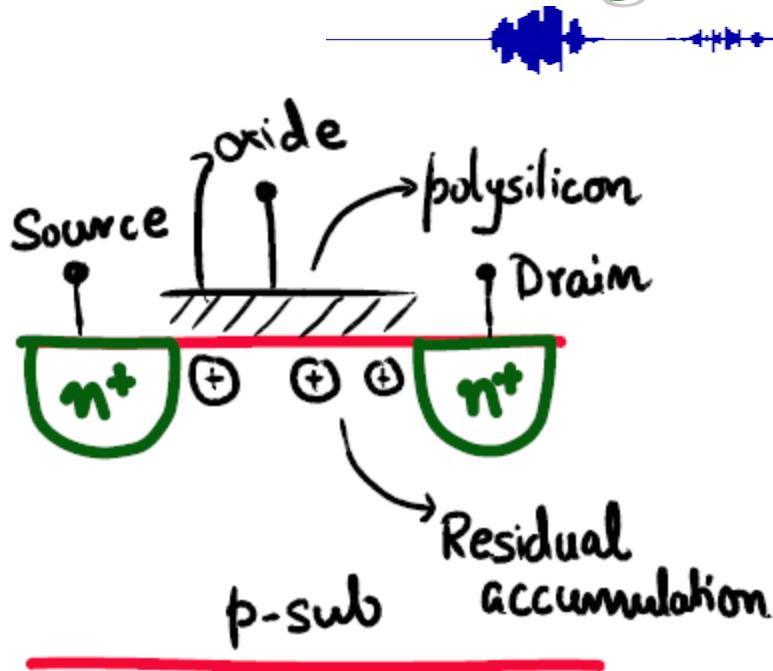
Derivation of MOSFET Large-signal Model



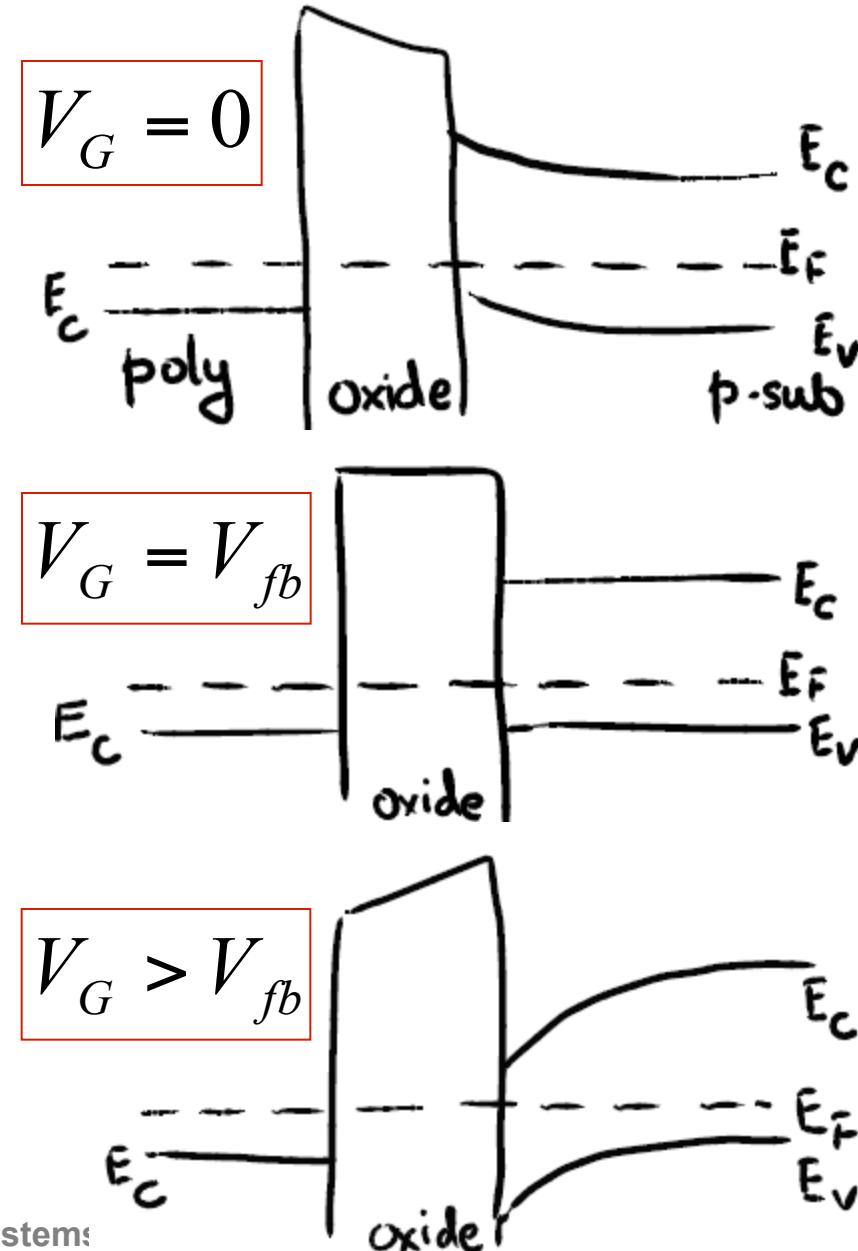
x Channel distance from the source along the channel length

$Q_{ch}(x)$ Channel charge per unit area at the distance x

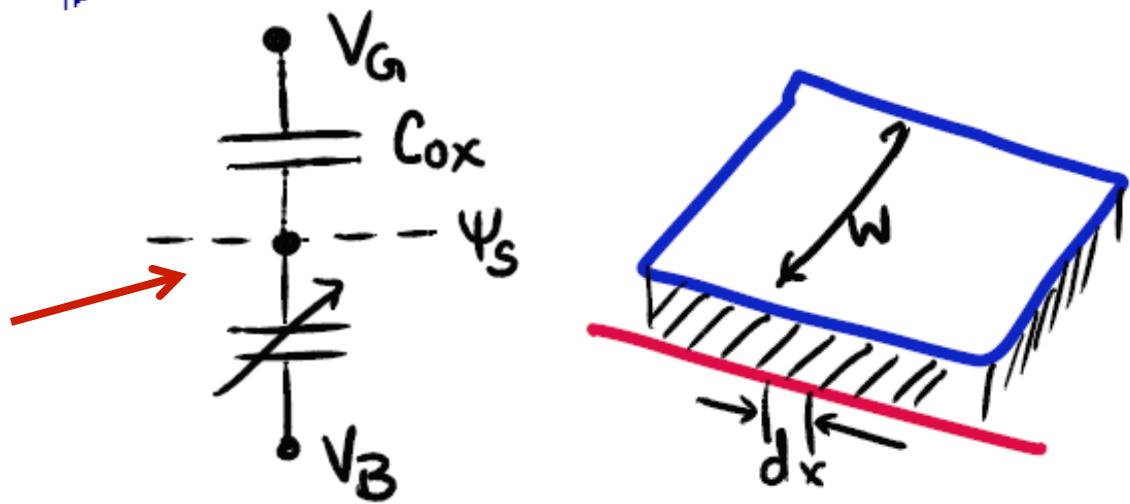
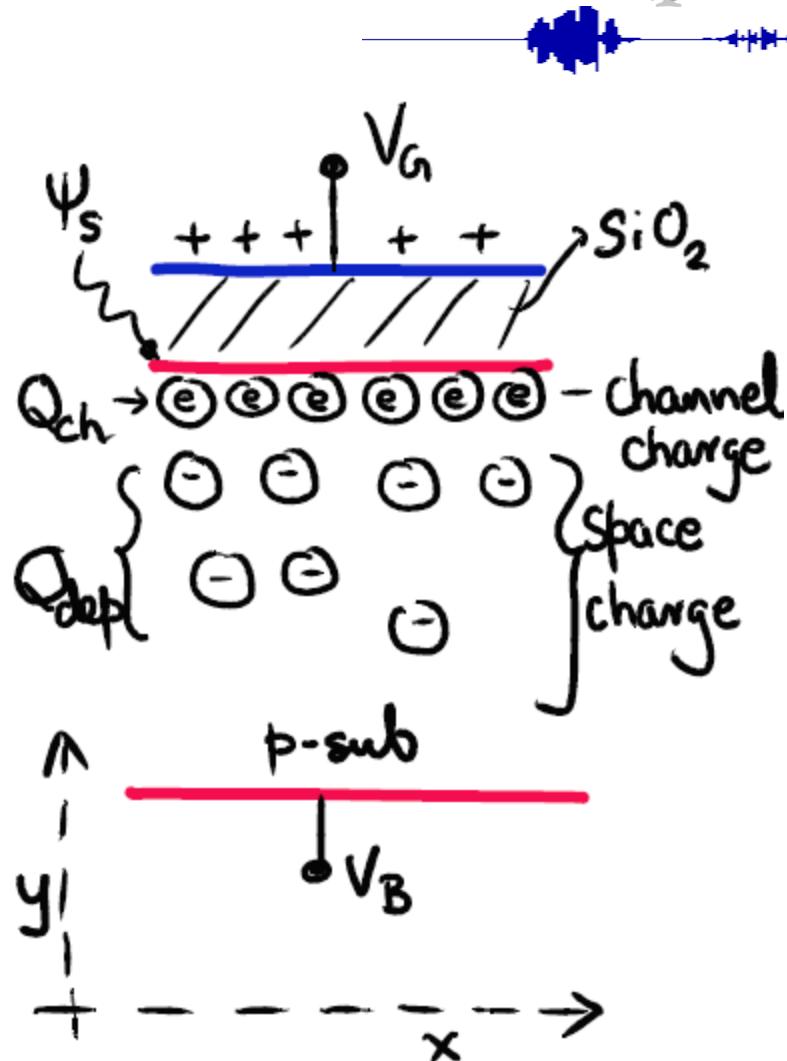
Flat-band voltage



- Work-function difference between polysilicon and p-type silicon leads to band-bending (residual charge) at the oxide-semiconductor interface.
- Extra voltage to reach the flat-band condition.



Channel and depletion charge



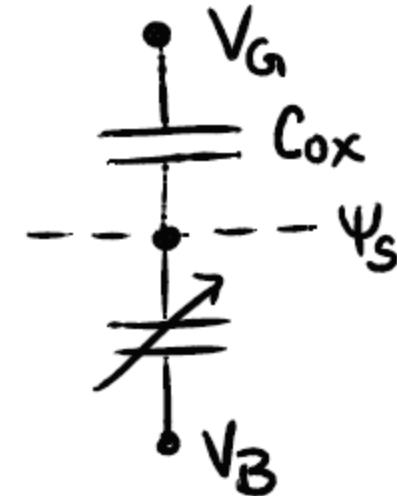
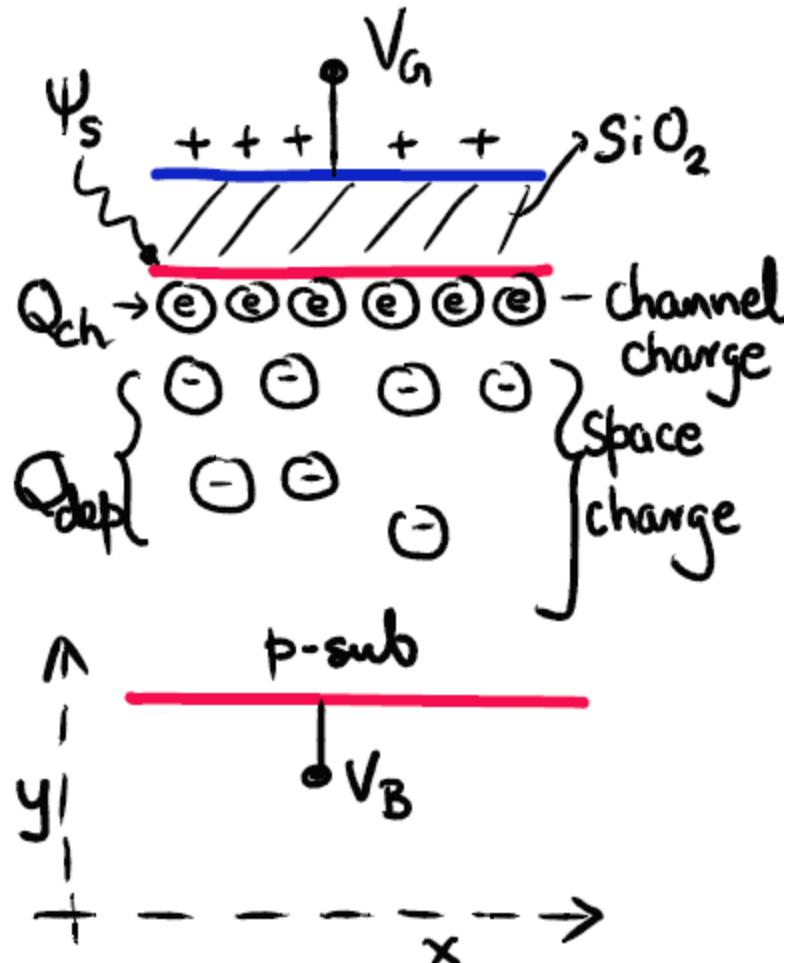
- Total charge on the gate

$$C_{ox}[V_G - V_{fb} - \psi_s] = Q_{ch} + Q_{dep}$$

- Differentiate with respect x.

$$-C_{ox} \frac{\partial \psi_s}{\partial x} = \frac{\partial Q_{ch}}{\partial x} + \frac{\partial Q_{dep}}{\partial \psi_s} \frac{\partial \psi_s}{\partial x}$$

MOSFET gate capacitance



- First Assumption

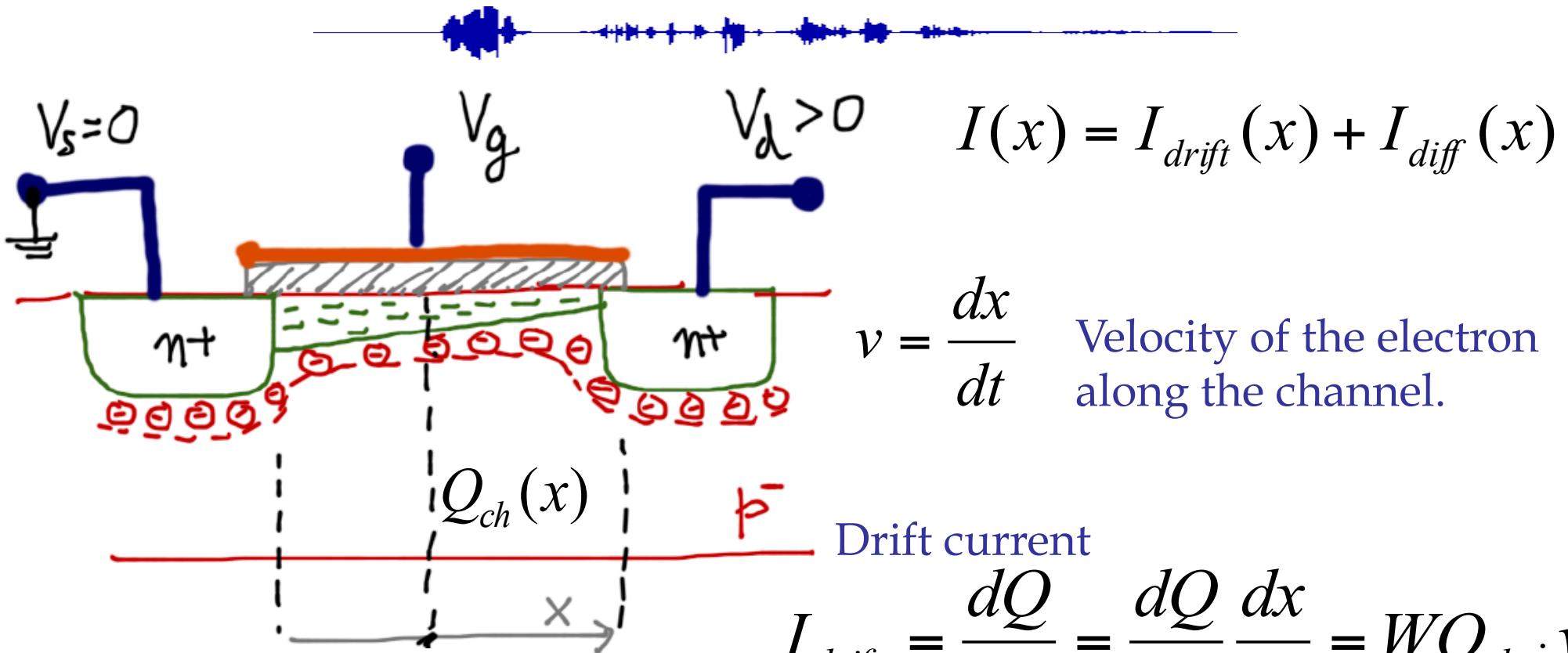
$$\frac{\partial Q_{dep}}{\partial \psi_s} = C_{dep}$$

$$\frac{\partial Q_{ch}}{\partial x} = -(C_{ox} + C_{dep}) \frac{\partial \psi_s}{\partial x}$$

- Total gate capacitance

$$\frac{\partial Q_{ch}}{\partial x} = -C_T \frac{\partial \psi_s}{\partial x}$$

Drift Current



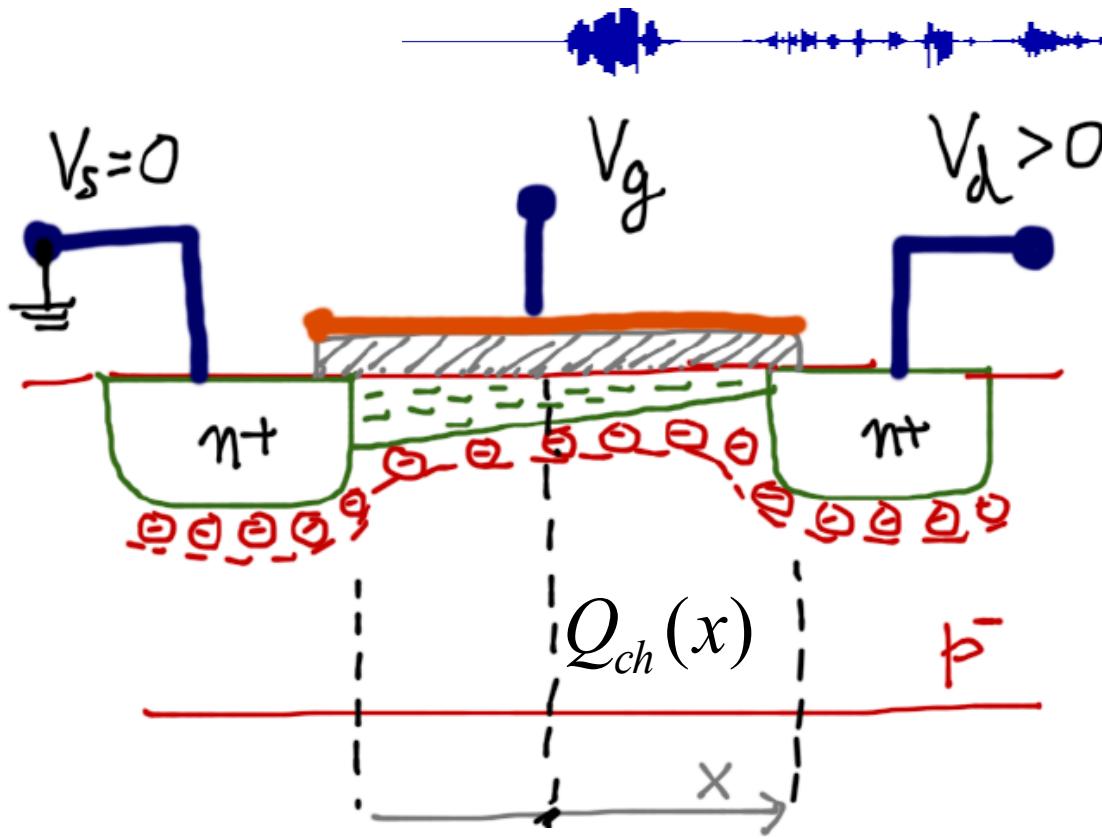
Two fundamental relations

$$v = \mu E(x) \quad \begin{matrix} \mu \\ E \end{matrix} \quad \begin{matrix} \text{Mobility of the electron} \\ \text{Electric field which is the gradient of the potential difference.} \end{matrix}$$

$$E(x) = -\frac{\partial \psi_s}{\partial x}$$

$$I_{drift}(x) = -W\mu Q_{ch} \frac{\partial \psi_s}{\partial x}$$

Diffusion Current



$$I(x) = I_{drift}(x) + I_{diff}(x)$$

$$I_{diff}(x) = DW \frac{\partial Q_{ch}}{\partial x}$$

Diffusion constant

Einstein's relationship

$$D = \mu \frac{KT}{e} = \mu U_T$$

T Temperature in Kelvin K Boltzmann's constant

U_T Thermal Voltage (25 mV at room temperature)

$$I_{diff}(x) = W\mu U_T \frac{\partial Q_{ch}}{\partial x}$$

Combining Expression

The diagram illustrates a MOSFET structure with the following labels:

- $V_s = 0$: Source voltage.
- V_g : Gate voltage.
- $V_d > 0$: Drain voltage.
- $I(x) = I_{drift}(x) + I_{diff}(x)$: Total current expression.
- η^+ : N+ source/drain regions.
- η^- : P- substrate.
- $Q_{ch}(x)$: Channel charge density.
- x : Position along the channel.

Red annotations show electron flow from the drain towards the source through the channel, with arrows indicating electron movement.

Equation 1: $I(x) = W\mu[-Q_{ch} \frac{\partial \psi_s}{\partial x} + U_T \frac{\partial Q_{ch}}{\partial x}]$

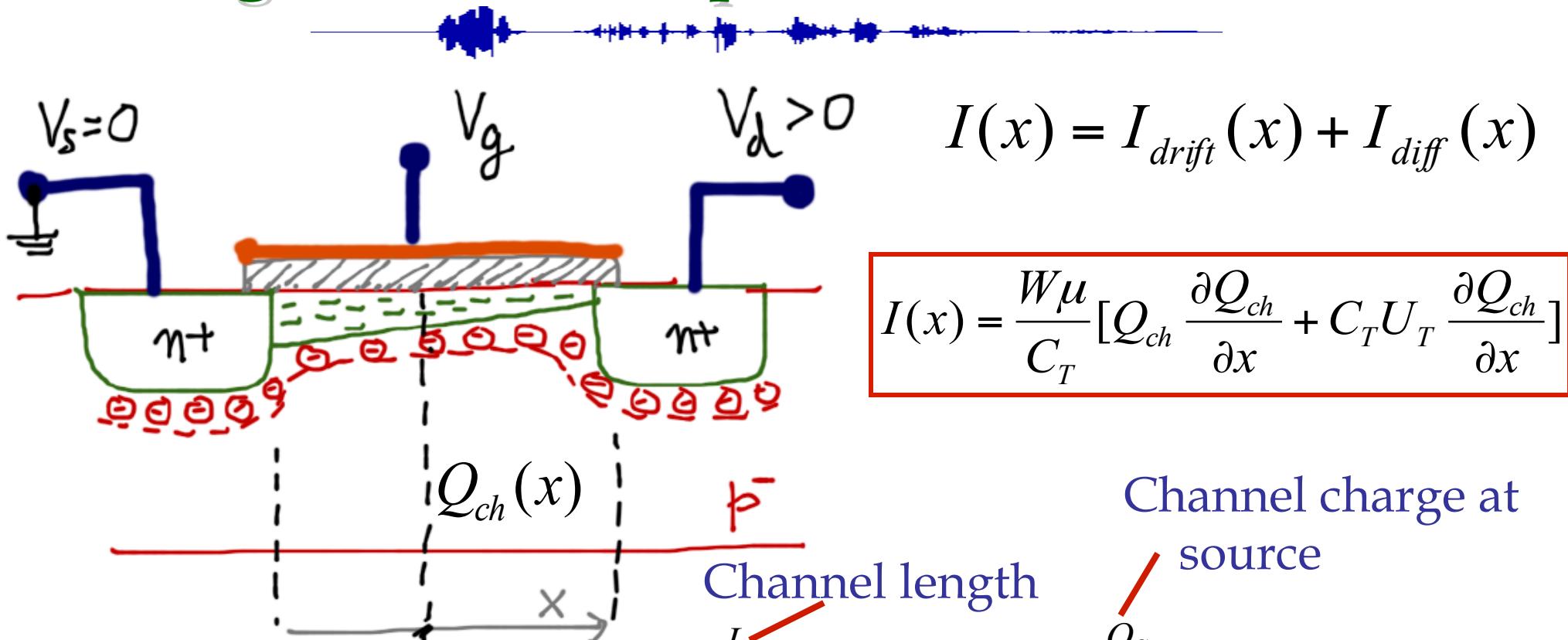
- Using gate capacitance expression

Equation 2: $I(x) = W\mu[\frac{1}{C_T} Q_{ch} \frac{\partial Q_{ch}}{\partial x} + U_T \frac{\partial Q_{ch}}{\partial x}]$

- Differential equation to be solved

$$I(x) = \frac{W\mu}{C_T} [Q_{ch} \frac{\partial Q_{ch}}{\partial x} + C_T U_T \frac{\partial Q_{ch}}{\partial x}]$$

Solving differential equation



- Assumption: $I(x) = \text{constant}$

$$\int_0^L I(x) dx = I_{ds} L$$

Channel charge at source

Channel length

$$\int_0^L I(x) dx = \frac{W\mu}{C_T} \int_{Q_D}^{Q_S} [Q_{ch} + C_T U_T] dQ_{ch}$$

Channel charge at drain

Charge-based expression



Forward Current I_F

$$I_{ds} = \frac{W\mu}{2C_T L} \left([Q_S^2 + 2C_T U_T Q_S] - [Q_D^2 + 2C_T U_T Q_D] \right)$$

Due to drift

Due to Diffusion

- Three regions of MOSFET operation

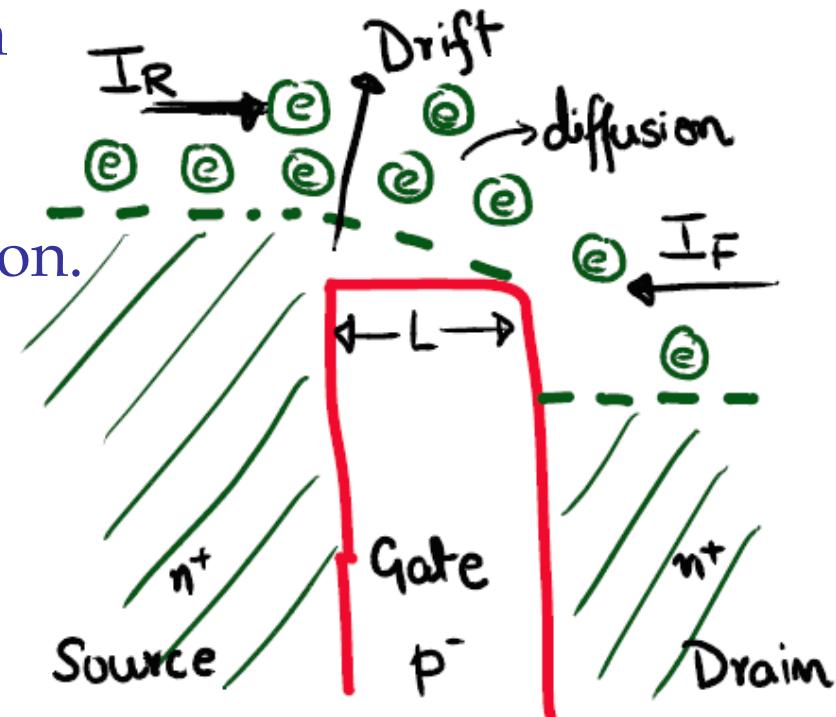
- Sub-threshold operation or weak inversion.

$$|Q_S| \ll 2C_T U_T$$

- Above-threshold or strong inversion.

$$|Q_S| \gg 2C_T U_T$$

- Moderate inversion $|Q_S| \approx 2C_T U_T$



Relating to terminal voltages

- Would like to link the drain-to-source current to the terminal voltages rather than terminal charges.

Forward Current

I_F

Reverse Current

I_R

$$I_{ds} = I_s [f(V_{GB}, V_{SB}) - f(V_{GB}, V_{DB})]$$

Gate to bulk voltage Source to bulk voltage Drain to bulk voltage

- Difficult to find a closed form solution – requires numerical techniques.
- However expressions for weak-inversion and strong-inversions can be separately determined.



Sub-threshold MOSFET current

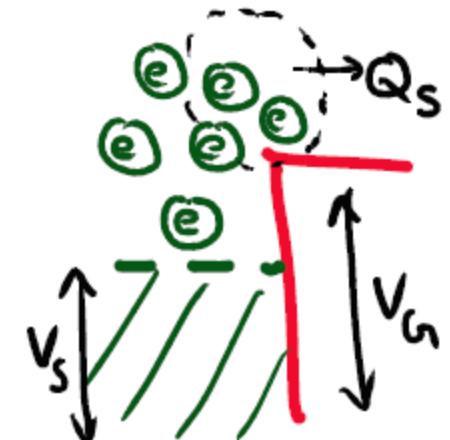


$$I_{ds} = \frac{W\mu}{2C_T L} \left([Q_S^2 + 2C_T U_T Q_S] - [Q_D^2 + 2C_T U_T Q_D] \right)$$

Sub-threshold criterion: $|Q_S| \ll 2C_T U_T$

$$I_{ds} = \frac{W\mu U_T}{L} (Q_S - Q_D)$$

Link Q_S Q_D V_S V_G V_D V_B



- Due to diffusion: $\Delta Q_{S,D} \propto Q_{S,D} \Delta V$

$$\frac{dQ_{S,D}}{Q_{S,D}} = \alpha dV$$

Proportionality constant

Sub-threshold MOSFET current



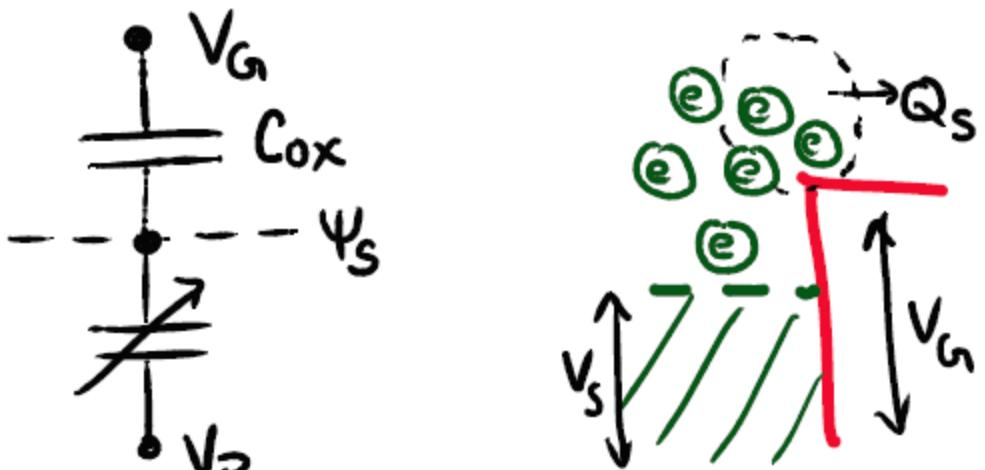
Expression for channel charge at the source and the drain terminal for sub-threshold biasing.

$$Q_{S,D} = \alpha \exp\left(\frac{\psi_s - V_{S,D}}{U_T}\right)$$

Surface potential expression:

$$\psi_s = \frac{C_{ox}}{C_{ox} + C_{dep}} V_G = \kappa V_G$$

$$\kappa = 0.7 \quad \text{Gate efficiency}$$



How to determine the proportionality constant α ?



Sub-threshold MOSFET current



Convenient to relate to threshold voltage. Remember: when the gate voltage equals threshold voltage, the MOSFET is transitioning from sub-threshold to above-threshold.

$$V_G = V_{th} \quad V_S, V_D = 0 \longrightarrow Q_S, Q_D = 2C_T U_T$$

$$Q_{S,D} = 2C_T U_T \exp\left(\frac{\kappa(V_G - V_{th}) - V_{S,D}}{U_T}\right)$$

$$I_{ds} = \frac{W\mu U_T}{L} (Q_S - Q_D)$$

$$I_{DS} = \frac{2\mu C_{ox} U_T^2}{\kappa} \frac{W}{L} \exp\left(\frac{\kappa(V_G - V_{th})}{U_T}\right) \left(\exp\left(\frac{-V_S}{U_T}\right) - \exp\left(\frac{-V_D}{U_T}\right) \right)$$



Sub-threshold Operating Regions



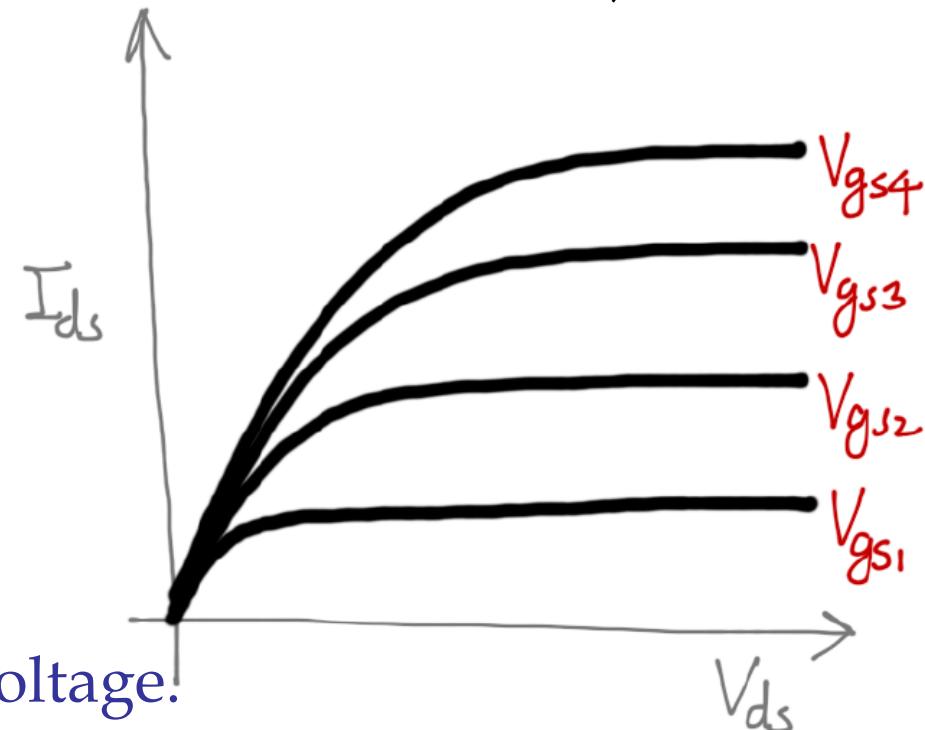
- Subthreshold current expression :

$$I_{DS} = I_S \frac{W}{L} \exp\left(\frac{KV_G}{U_T}\right) \left(\exp\left(\frac{-V_S}{U_T}\right) - \exp\left(\frac{-V_D}{U_T}\right) \right)$$

- Saturation region:

$$V_{DS} \geq 4U_T \approx 100mV$$

$$I_{DS} = I_S \frac{W}{L} \exp\left(\frac{KV_G}{U_T}\right) \exp\left(\frac{-V_S}{U_T}\right)$$



- Drain current independent of drain voltage!

Above-threshold MOSFET current

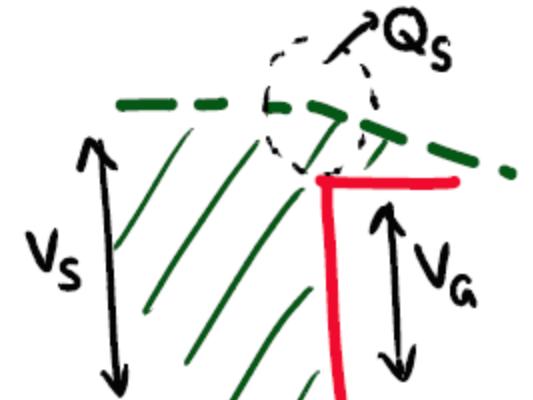


$$I_{ds} = \frac{W\mu}{2C_T L} \left([Q_S^2 + 2C_T U_T Q_S] - [Q_D^2 + 2C_T U_T Q_D] \right)$$

Sub-threshold criterion: $|Q_S| \gg 2C_T U_T$

$$I_{ds} = \frac{W\mu}{2C_T L} (Q_S^2 - Q_D^2)$$

Link Q_S Q_D V_S V_G V_D V_B



- Similar to a linear capacitor: $Q_{S,D} = C_T (K(V_G - V_{th}) - V_{S,D})$

$$Q_{S,D} = C_{ox} \left((V_G - V_{th}) - \frac{V_{S,D}}{K} \right)$$



Above-threshold MOSFET current



Drain current expression:

$$I_{ds} = \frac{\mu C_{ox}}{2\kappa} \frac{W}{L} [(K(V_G - V_{th}) - V_S)^2 - (K(V_G - V_{th}) - V_D)^2]$$

Gate efficiency $\kappa \approx 1.0$

Above-threshold:

$$I_{ds} = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{th})V_{DS} - \frac{1}{2} V_{DS}^2]$$



Worksheet



MOSFET Triode Region

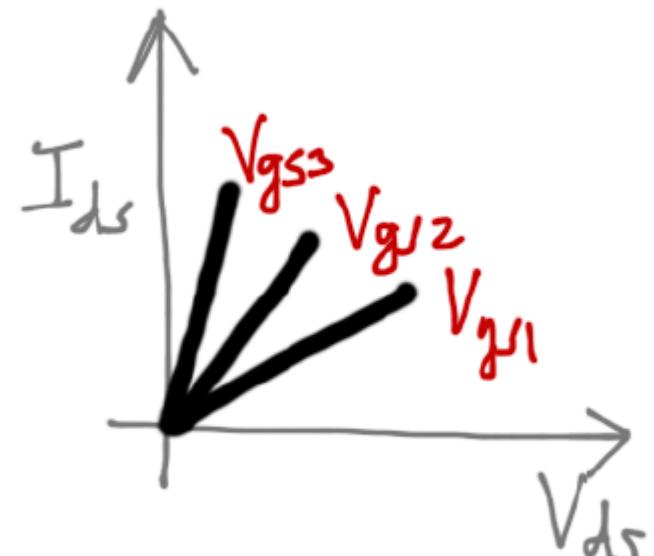
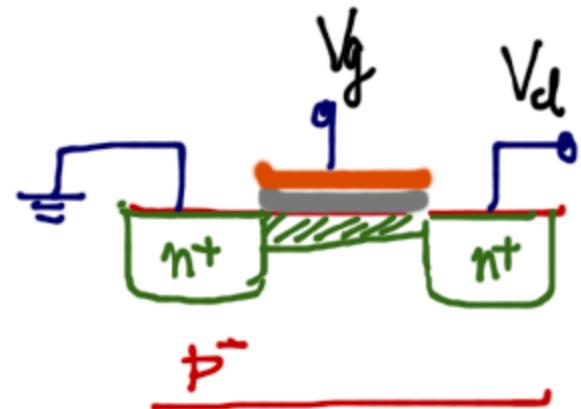


$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2]$$

$$V_{DS} \ll 2(V_{GS} - V_{TH})$$

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$



Pinch-off and Saturation



What happens when the drain voltage is increased ?

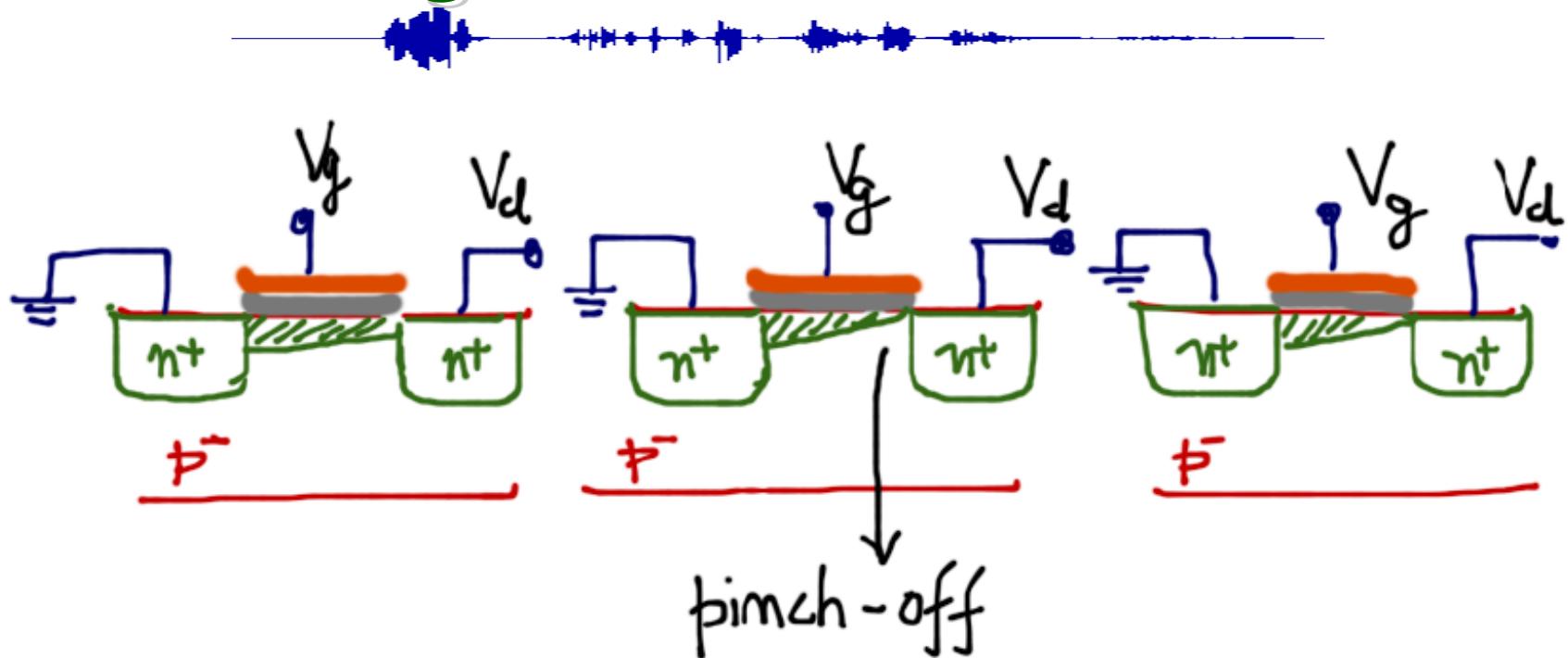
$V_{gd} = V_{th}$ → Channel at the drain disappears (pinched off).

$$V_{ds} = V_{gs} - V_{th}$$

The flow of current remains practically independent of drain-to-source voltage after pinch off.



Saturation Region



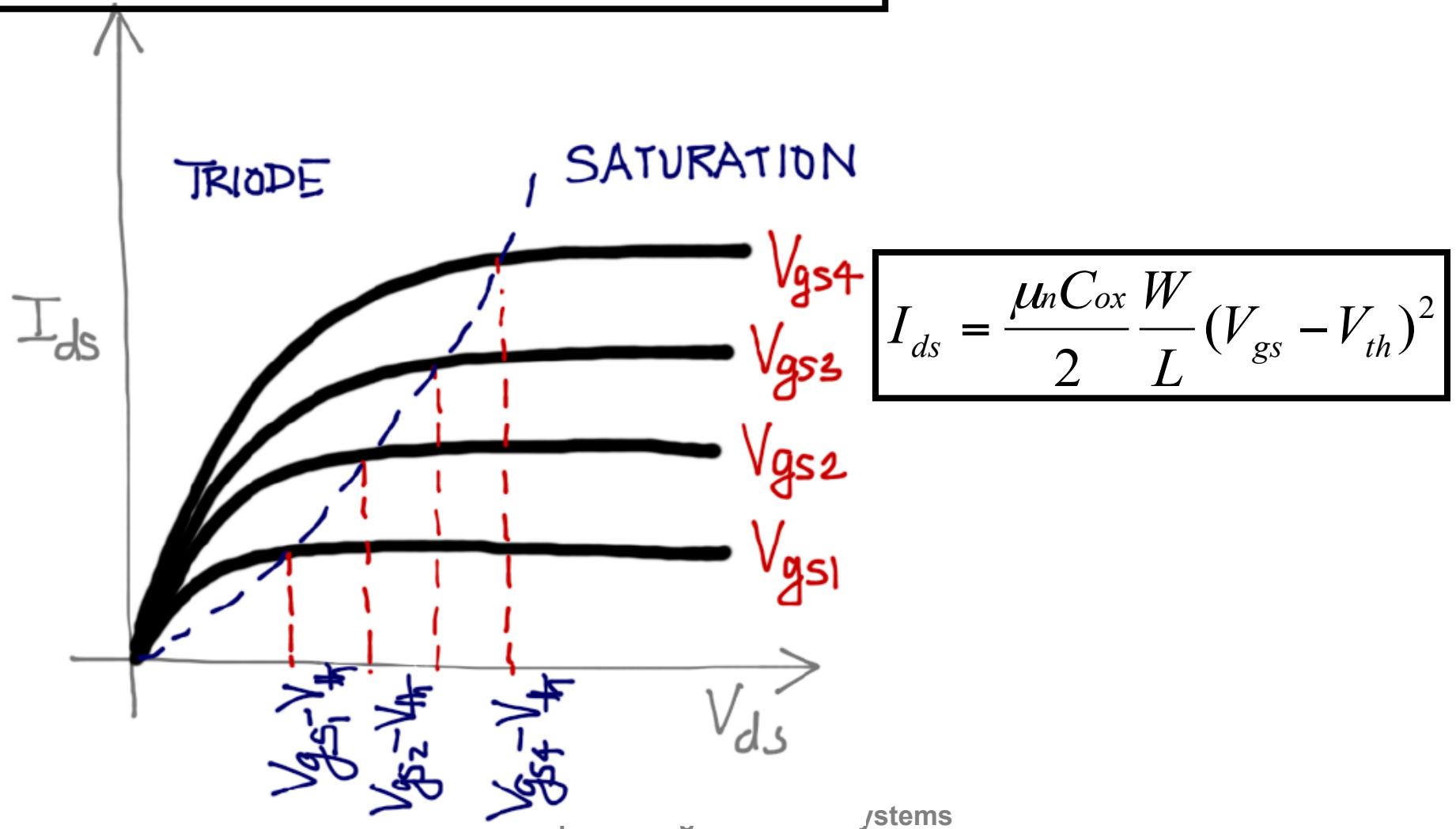
$$I_{ds} = \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2]$$

$$V_{ds} = V_{gs} - V_{th} \quad (\text{Pinch-off})$$

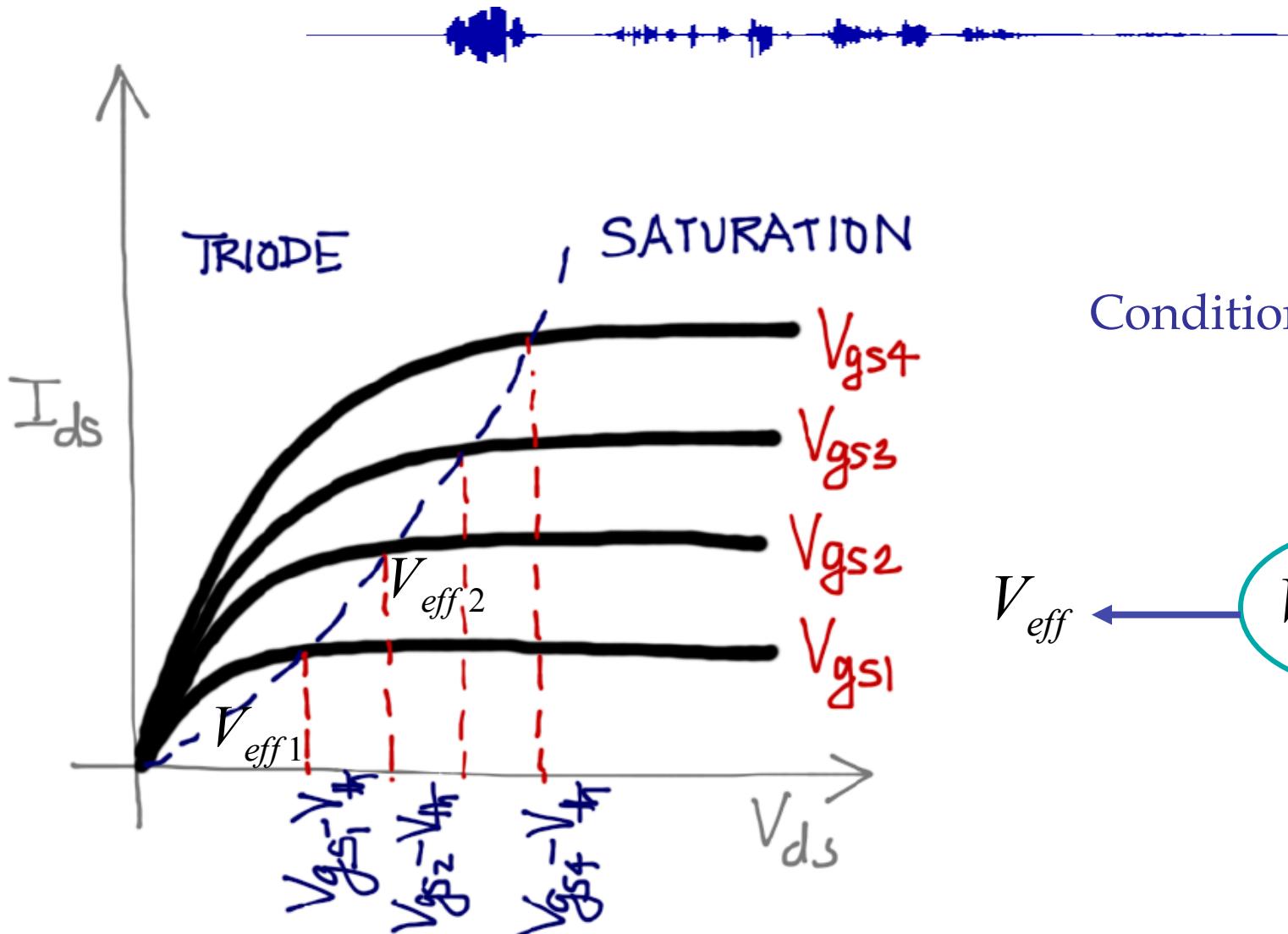
$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2$$

I-V Characteristics (cont.)

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2]$$



Condition for saturation



Condition for saturation

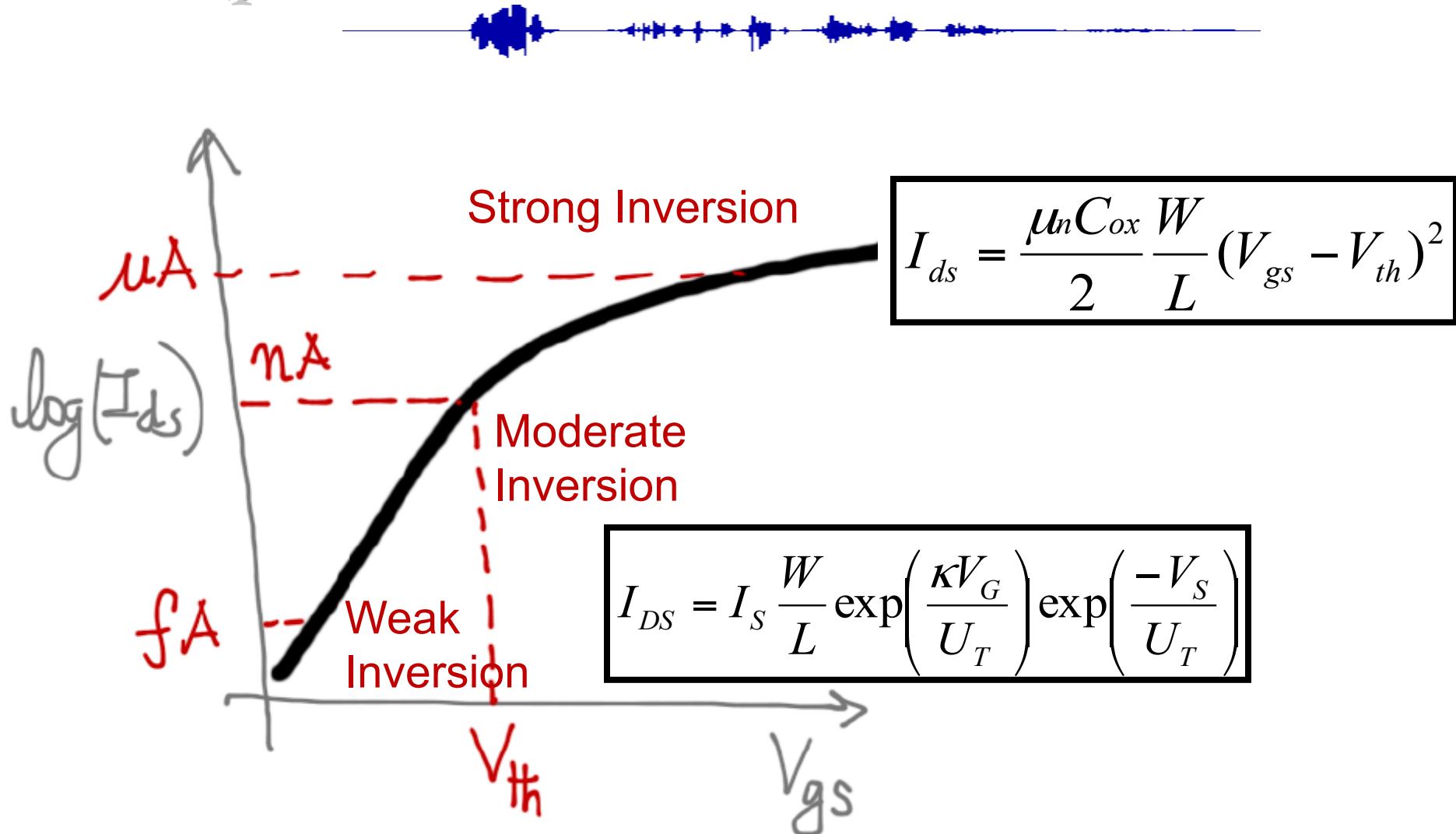
$$V_{gd} \leq V_{th}$$

$$V_{eff} \leftarrow V_{gs} - V_{th} \leq V_{ds}$$

Minimum drain to source voltage to maintain a transistor in saturation.

Typical value of $V_{eff} \approx 0.2V - 0.4V$

Interpolation models



- Interpolation model: Single analytical expression for different operating regions – EKV model and ACM model.

EKV MOSFET models


$$\log^2\left(1 + \exp\left[\frac{x}{2}\right]\right) \begin{cases} \exp(x) & x \ll 0 \\ \left(\frac{x}{2}\right)^2 & x \gg 0 \end{cases}$$

- Interpolates between exponential and square function based on the value of the input.

$$I_{ds} = I_s \log^2\left[1 + \exp\left(\frac{\kappa(V_G - V_{th}) - V_S}{2U_T}\right)\right] - I_s \log^2\left[1 + \exp\left(\frac{\kappa(V_G - V_{th}) - V_D}{2U_T}\right)\right]$$
$$I_{ds} = I_s [f(V_{GB}, V_{SB}) - f(V_{GB}, V_{DB})]$$



Worksheet



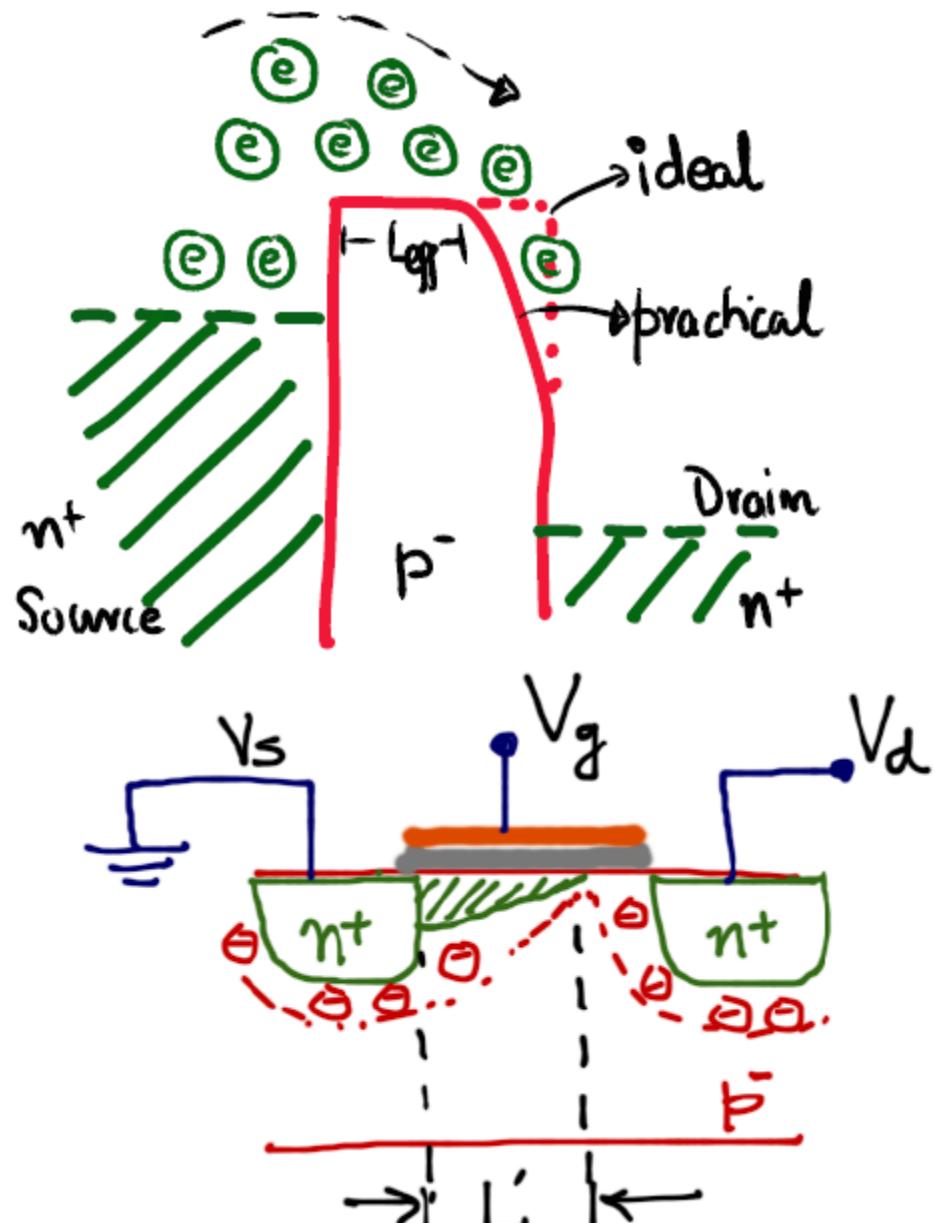
Channel Length Modulation

Remember: n⁺ and p⁻ junction forms a reverse biased diode. As V_d increases the depletion region around the drain increases which decreases the effective channel length. $L' = L - \Delta L$

Assuming the reduction in channel length is small.

$$1/L' = \frac{1}{L} (1 + \Delta L/L)$$

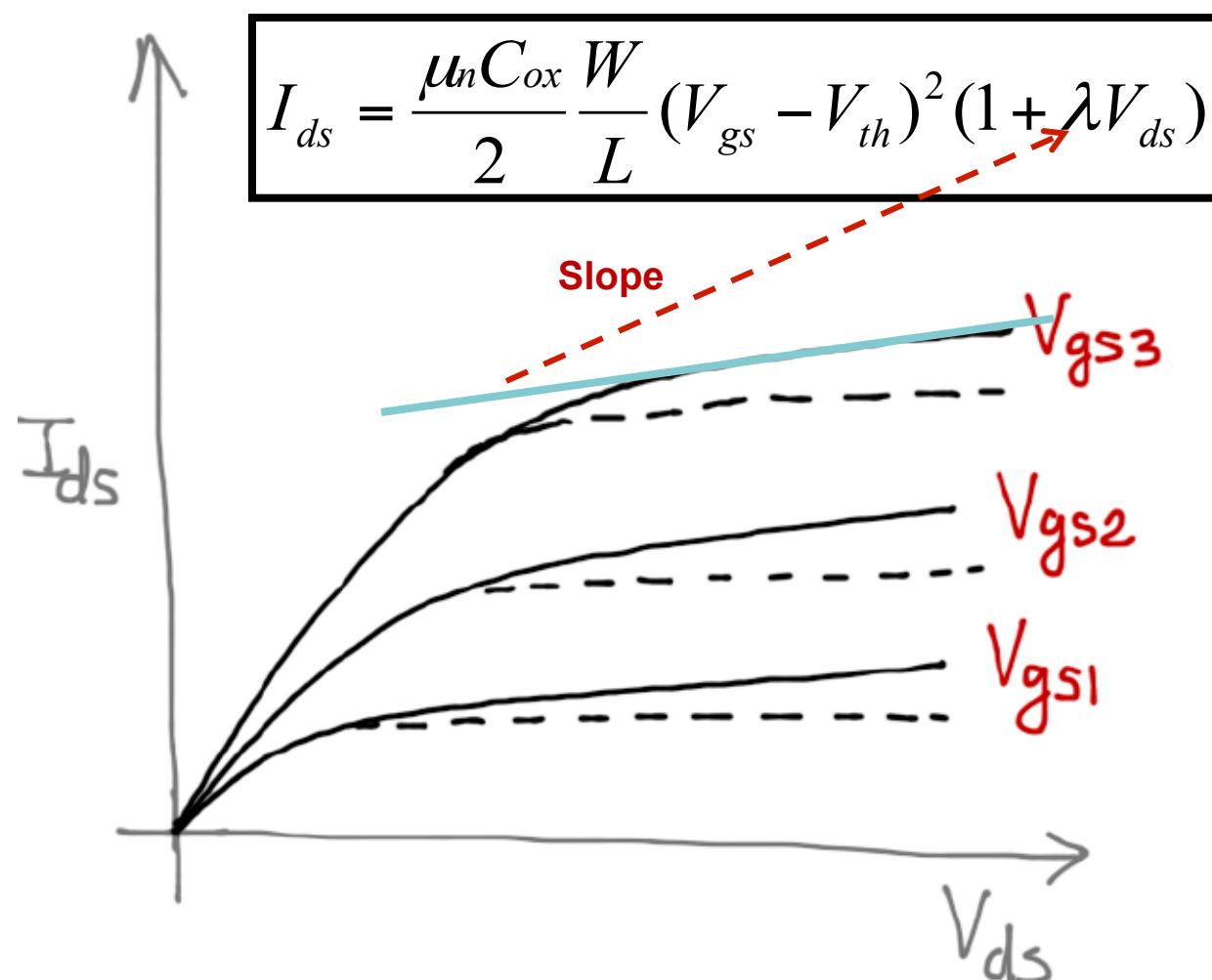
$$1/L' = \frac{1}{L} (1 + \lambda V_{ds}), \quad \lambda V_{ds} = \Delta L/L$$



Effect of channel length modulation

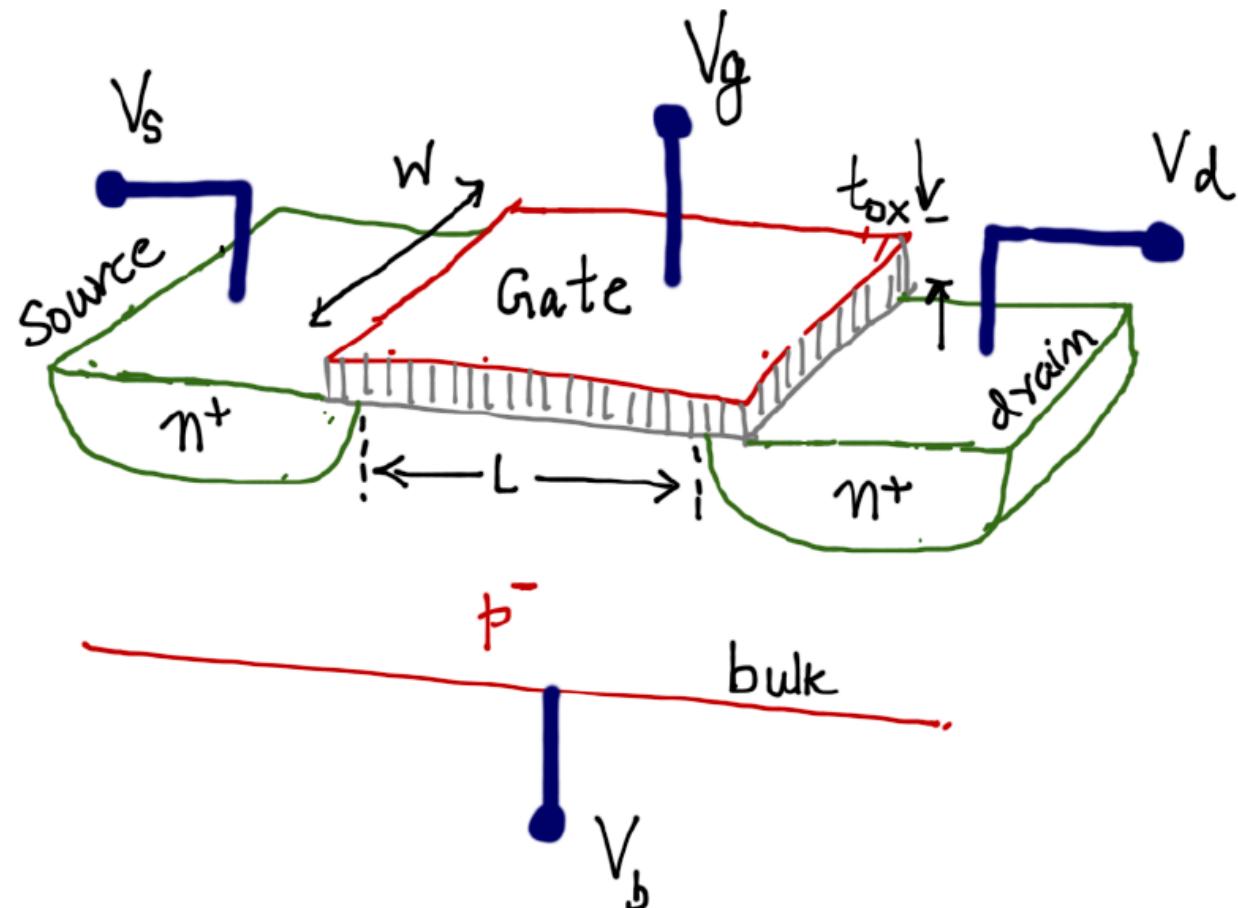


In saturation region, the drain current does vary (weakly) with the drain-to-source voltage.



Structure of an n-type MOSFET (nMOS)

- Four terminals: source, drain, gate and bulk.
- Current (electrons) flow between the source and drain terminals.
- The gate terminal controls the flow.
- nMOS transistor: source and drain are formed by n^+ semi-conductor.
- Bulk connected to the lowest potential.



Summary of nMOS Large Signal Models



Sub-threshold operation $V_{gs} < V_{th}$

$$I_{DS} = I_s \frac{W}{L} \exp\left(\frac{\kappa V_G}{U_T}\right) \left(\exp\left(\frac{-V_S}{U_T}\right) - \exp\left(\frac{-V_D}{U_T}\right) \right)$$

Above threshold Triode Region

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th}) V_{ds}]$$

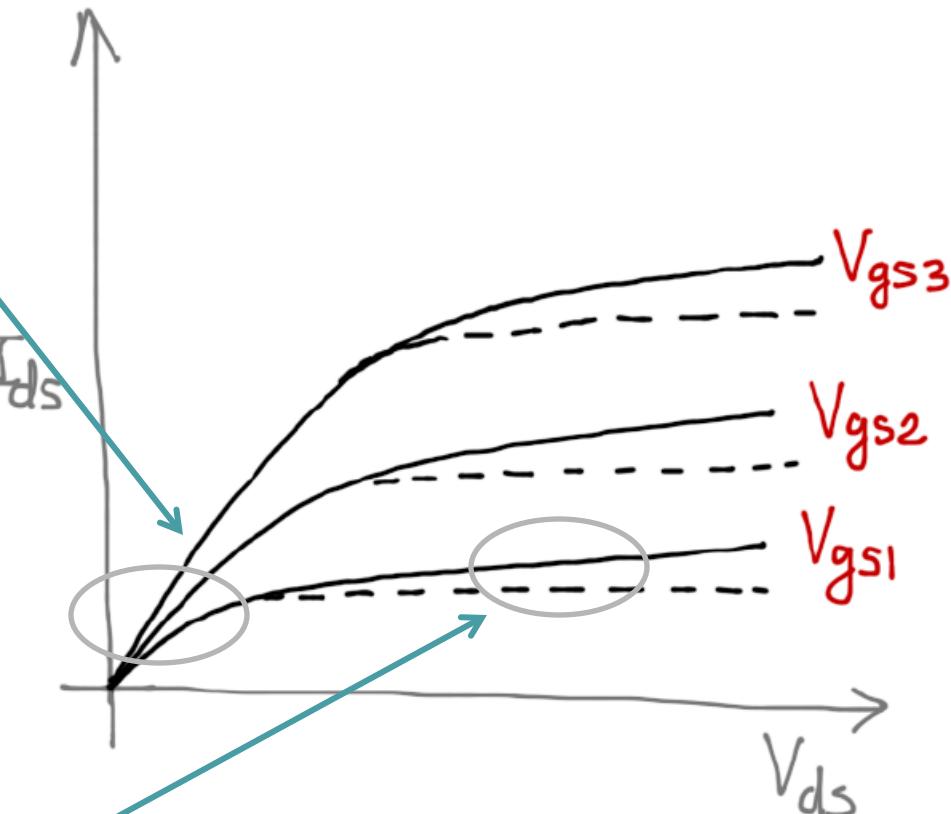
Sub-threshold Saturation Region $V_{ds} > 100mV$

$$I_{DS} = I_s \frac{W}{L} \exp\left(\frac{\kappa V_G}{U_T}\right) \exp\left(\frac{-V_S}{U_T}\right)$$

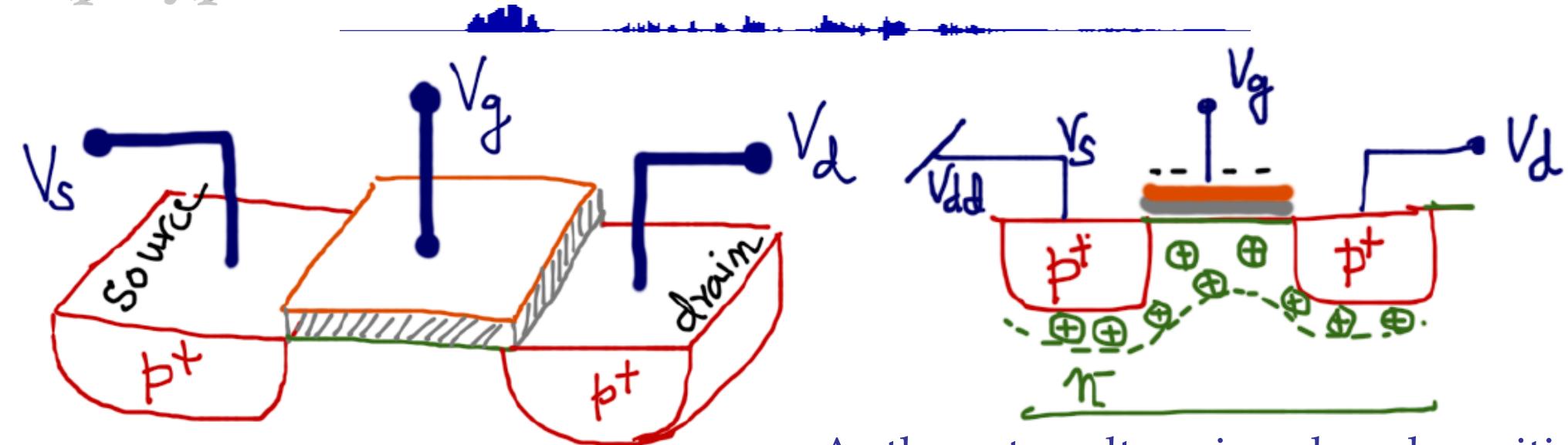
Above-threshold Saturation Region

$$V_g - V_d < V_{th}$$

$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$$



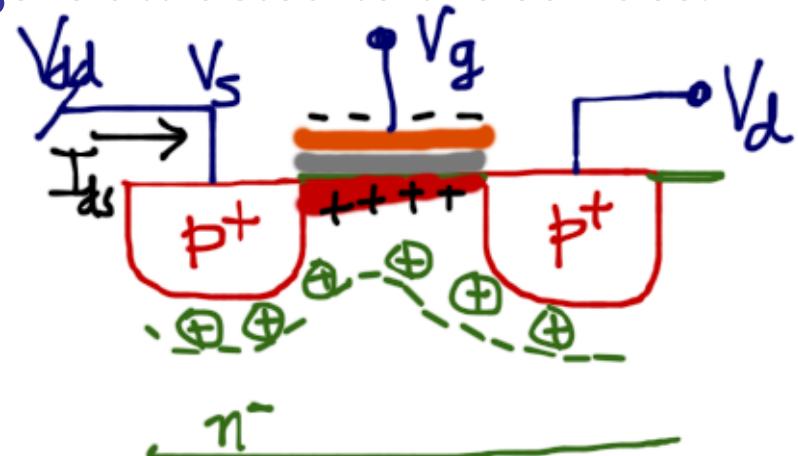
p-type MOSFET



Conduction based on holes.
Source and drain consists of
p⁺ semi-conductor.

Bulk connected to highest
potential.

As the gate voltage is reduced, positive charge is attracted to the surface.



Holes conduct current from the source to the drain.

pMOS Large Signal Model



Transistor conducts currently only
when $V_{sg} > |V_{th}|$

$$I_{ds} = -\mu_p C_{ox} \frac{W}{L} [(V_{sg} - |V_{th}|) V_{sd} - \frac{1}{2} V_{sd}^2]$$

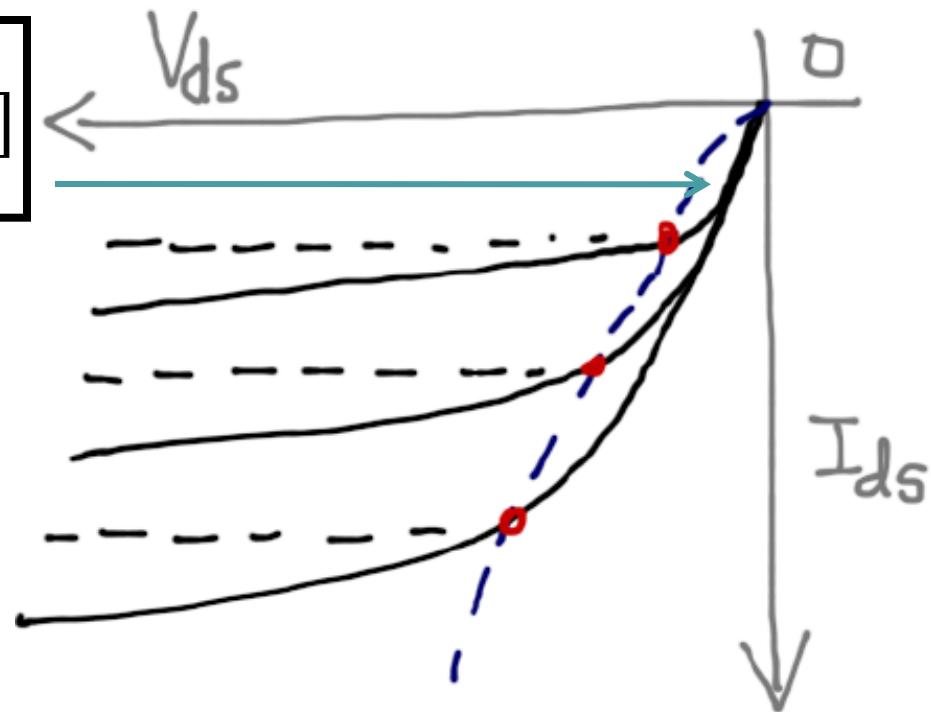
Transistor enters into saturation
when $V_d - V_g < |V_{th}|$

Saturation Region

$$I_{ds} = -\frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{sg} - V_{th})^2 (1 + \lambda V_{sd})$$

Sub-threshold model

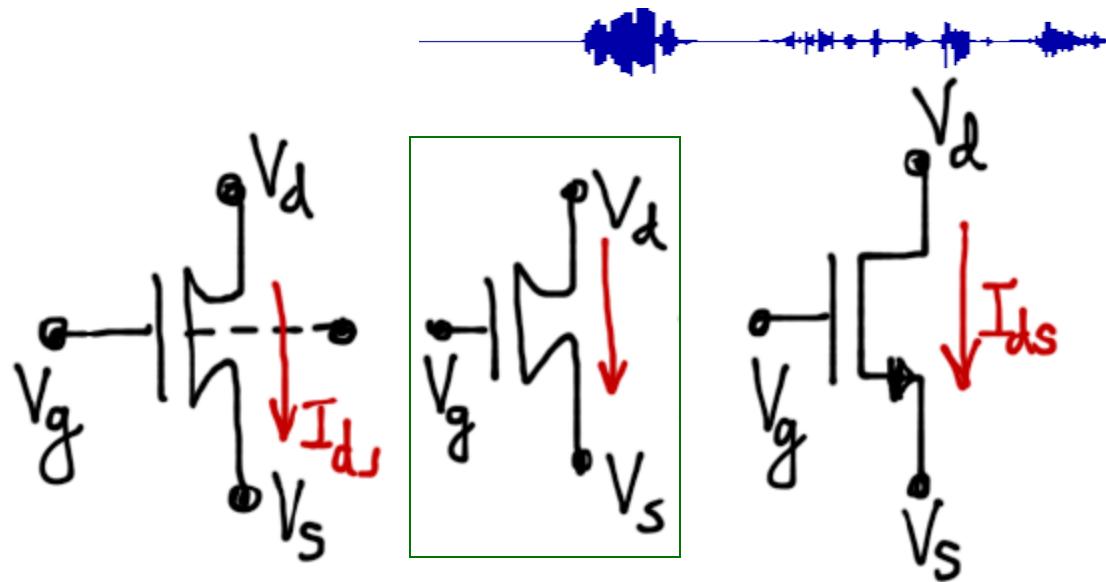
$$I_{DS} = I_s \frac{W}{L} \exp\left(\frac{-\kappa V_G}{U_T}\right) \left(\exp\left(\frac{V_S}{U_T}\right) - \exp\left(\frac{V_D}{U_T}\right) \right)$$



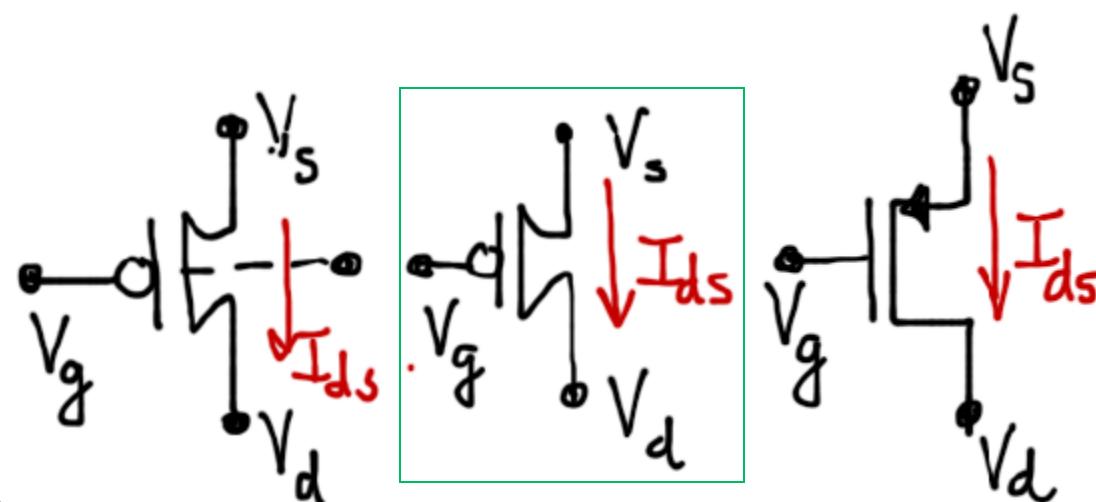
Sub-threshold saturation model

$$I_{DS} = I_s \frac{W}{L} \exp\left(\frac{-\kappa V_G}{U_T}\right) \exp\left(\frac{V_S}{U_T}\right)$$

MOSFET Circuit Symbols



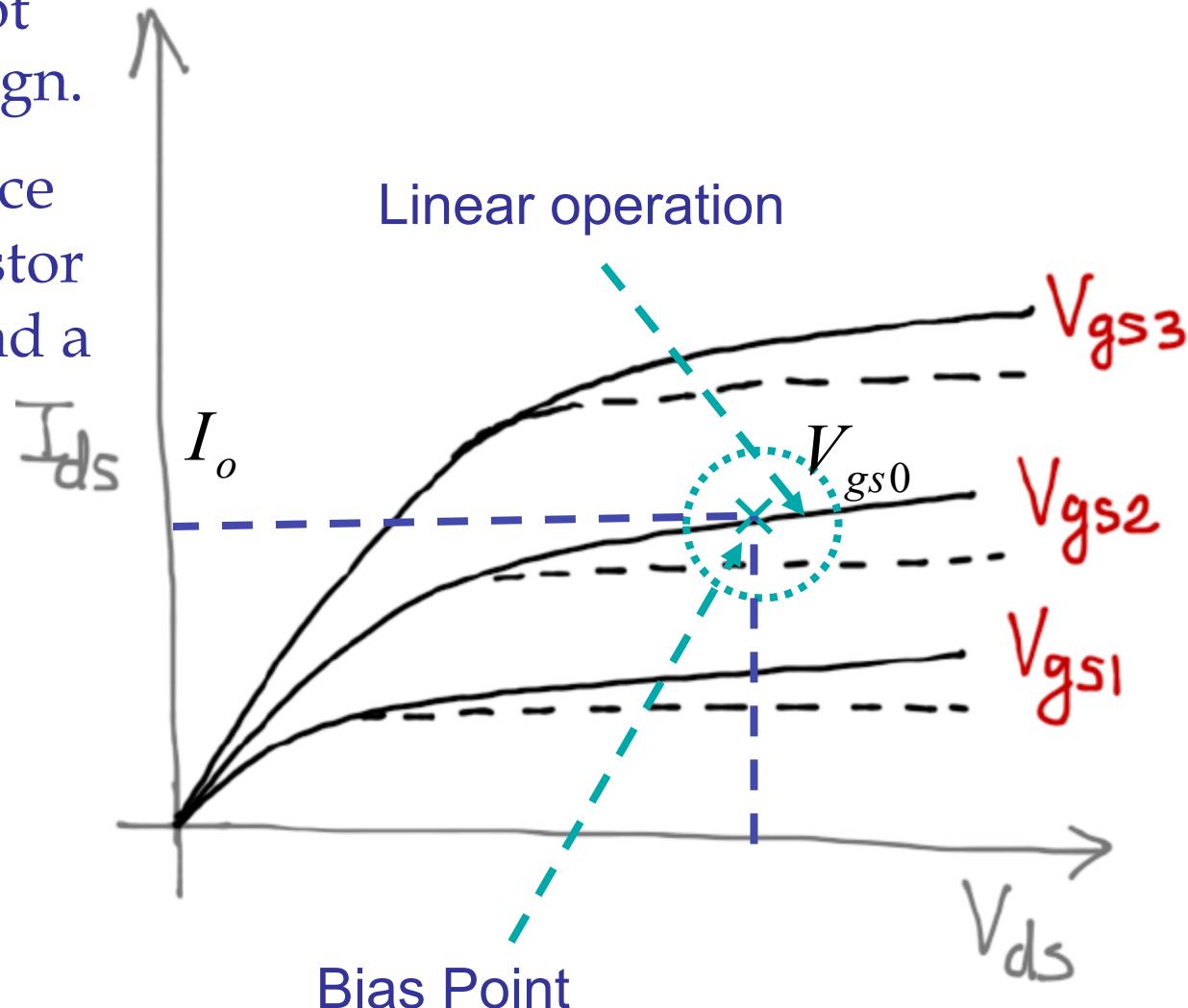
- Four terminals: source, drain, gate and bulk.
- nMOS: bulk will be connected to the lowest potential (gnd).
- nMOS: current will flow from the drain to the source.
- pMOS: bulk will be connected to the highest potential (vdd).
- pMOS: current will flow from the source to the drain.



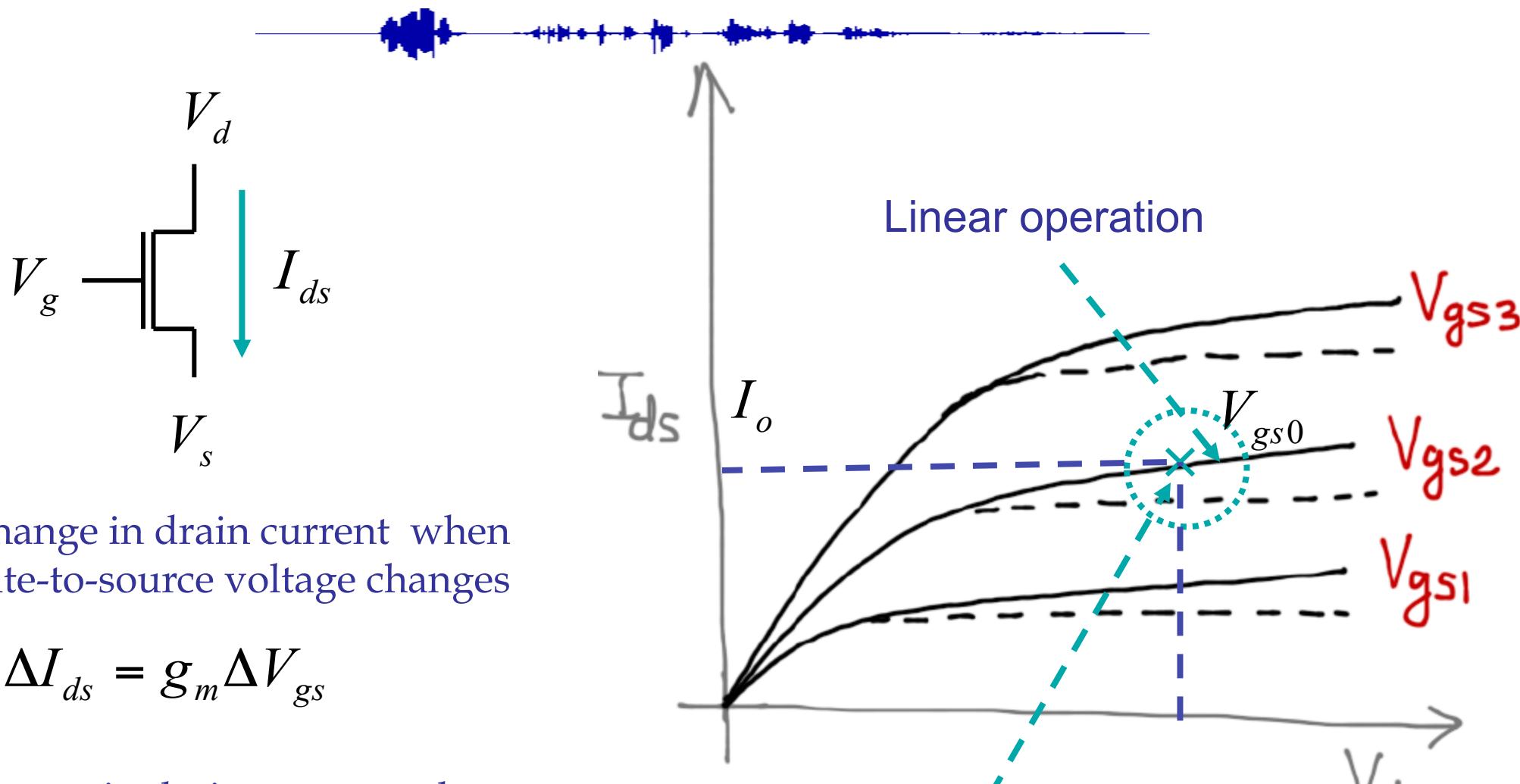
Bias point and Small-signal Models



- Large signal models are not useful in linear circuit design.
- Small signal models: Reduce the operation of the transistor about a small region around a bias point.
- Bias point of a transistor is determined by its drain current and the gate-to-source voltage.



Small-signal Models



Change in drain current when gate-to-source voltage changes

$$\Delta I_{ds} = g_m \Delta V_{gs}$$

Change in drain current when drain-to-source voltage changes

$$\Delta I_{ds} = g_d \Delta V_{ds}$$



Small-signal Parameters (Above-threshold)



Gate-to-source transconductance

$$g_m \approx \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{2I_o}{V_{gs} - V_{th}}$$

$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_0}$$

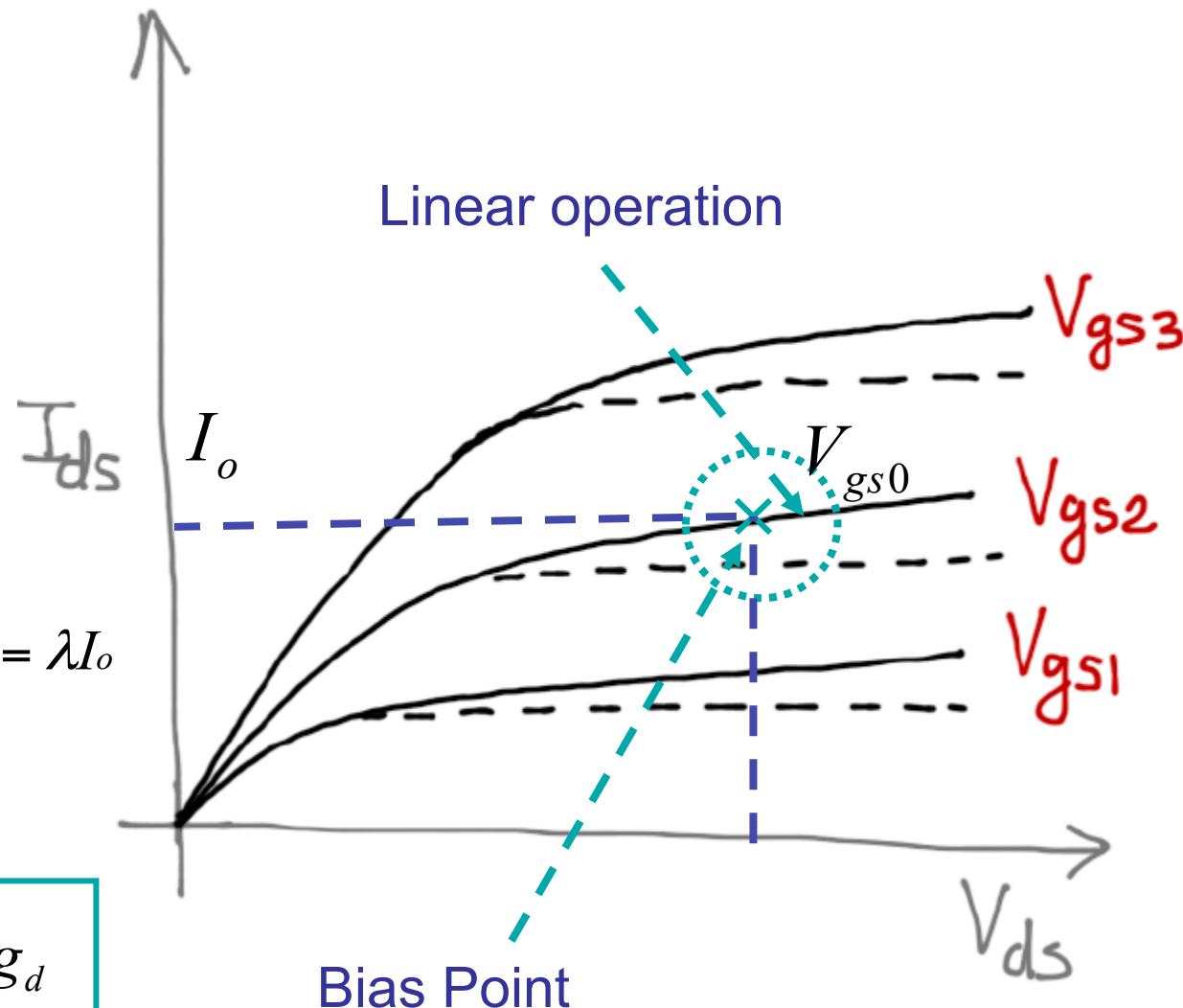
Drain transconductance

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda = \lambda I_o$$

$$g_m = 10^{-6} \Omega^{-1}$$

$$g_d = 10^{-8} \Omega^{-1}$$

$$g_m \gg g_d$$



Small-signal Parameters (Sub-threshold)



Gate-to-source transconductance

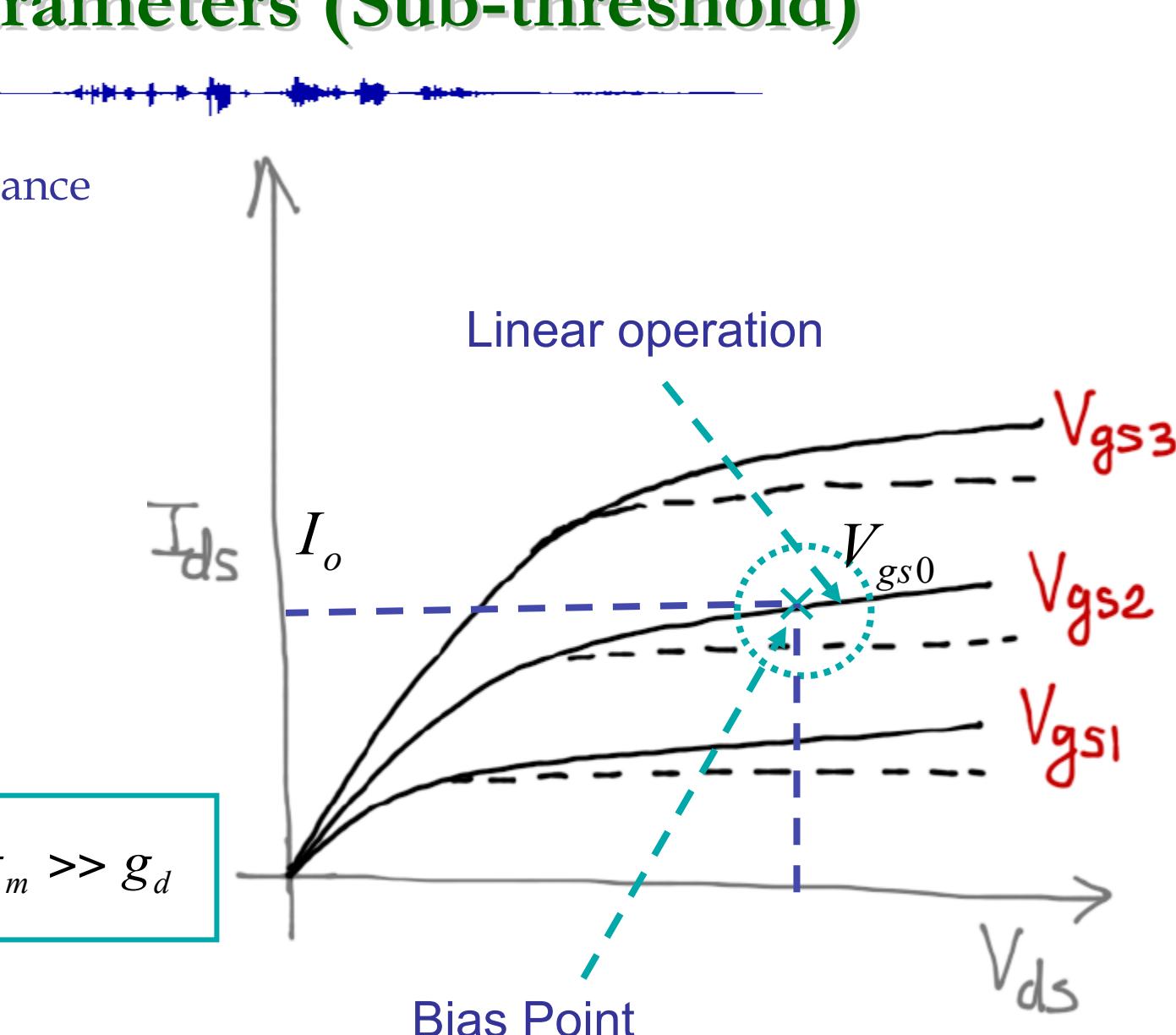
$$g_m \approx \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\kappa I_o}{U_T}$$

Drain transconductance

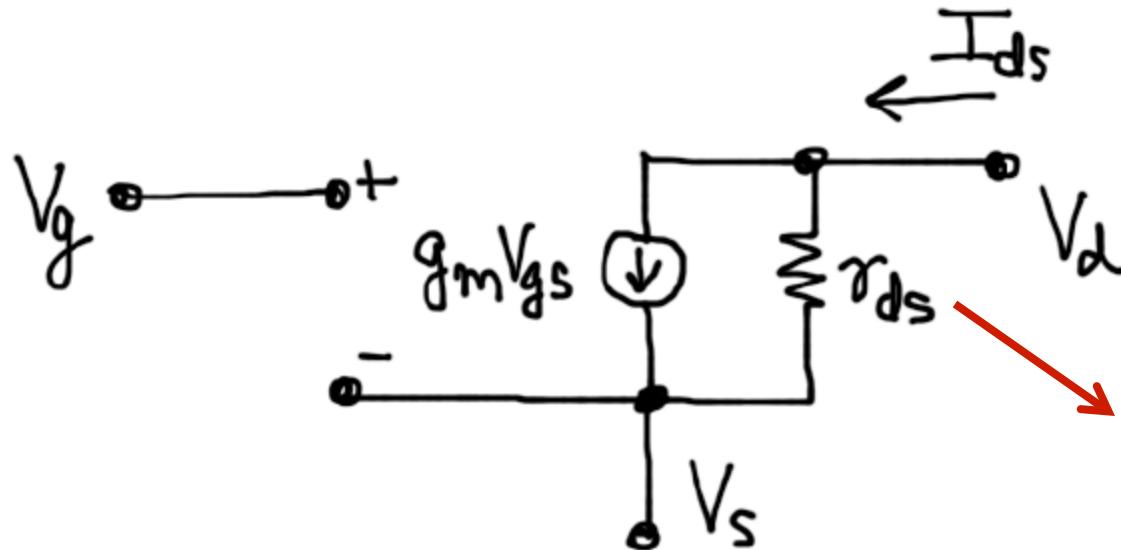
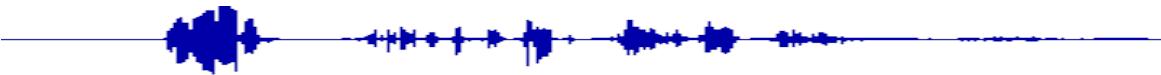
$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}} = \lambda I_o$$

$$g_m = 10^{-9} \Omega^{-1}$$

$$g_d = 10^{-11} \Omega^{-1}$$



Simplified Small-signal DC Model

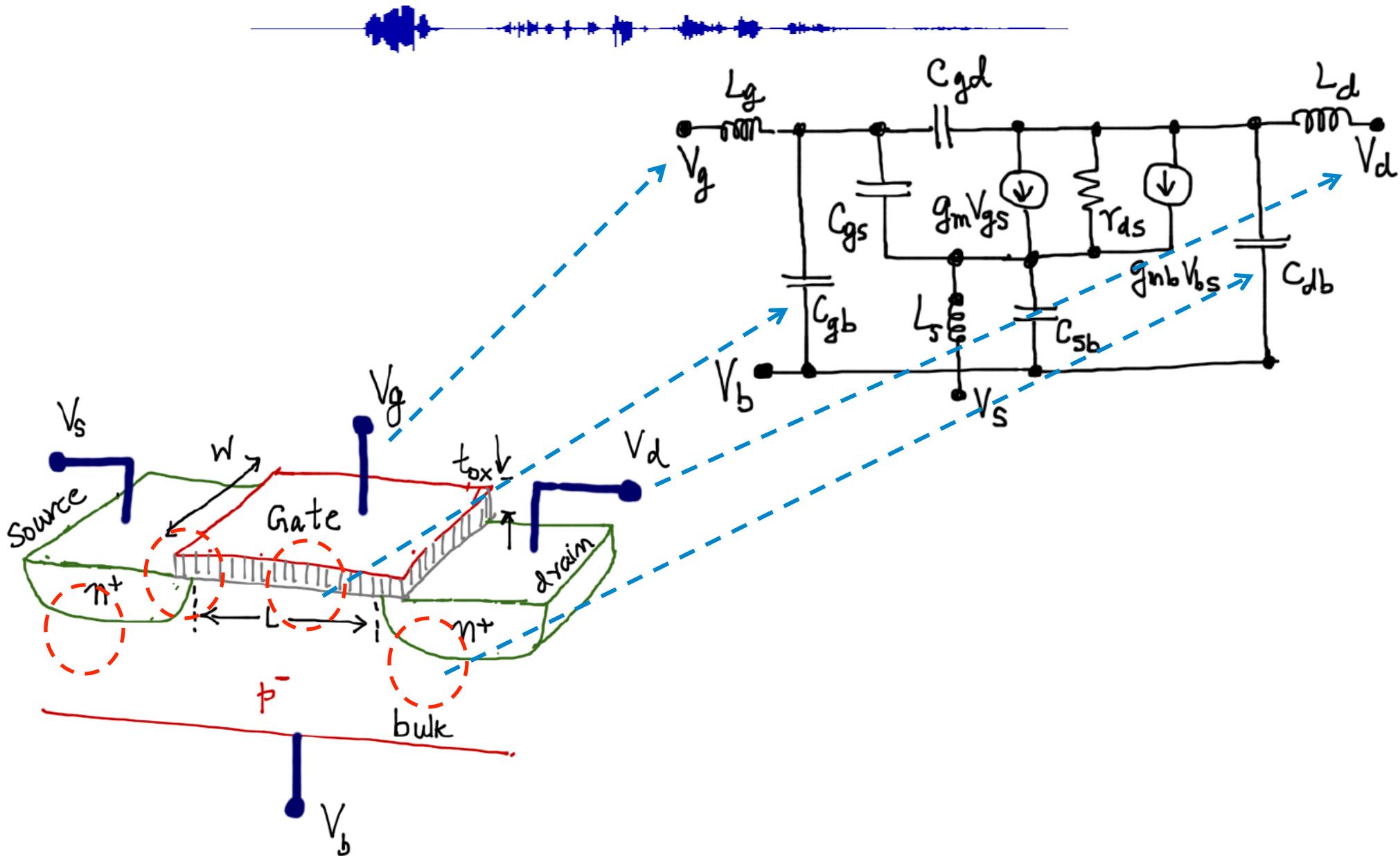


$$r_{ds} = \frac{1}{g_d}$$

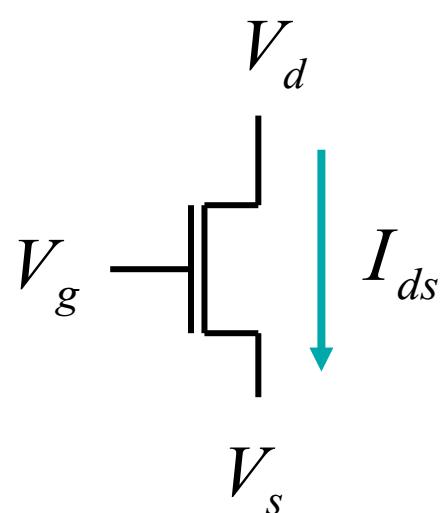
- Gate-to-source voltage controls the drain current through g_m
- Drain-to-source voltage controls the drain-to-source current through a resistor r_{ds} .



AC Model of MOSFET Transistor



Small-signal Model Revisited



$$\Delta I_{ds} = g_m \Delta V_{gs}$$

Change in drain current when gate-to-source voltage changes

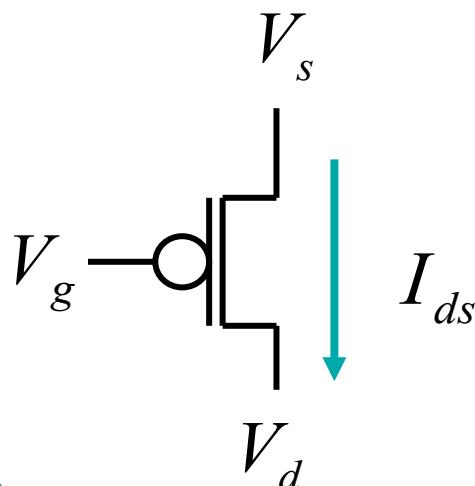
$$\Delta I_{ds} = g_d \Delta V_{ds}$$

Change in drain current when drain-to-source voltage changes

By superposition principle

$$\Delta I_{ds} = g_m \Delta V_{gs} + g_d \Delta V_{ds}$$

$$\Delta I_{ds} = g_m (\Delta V_g - \Delta V_s) + g_d (\Delta V_d - \Delta V_s)$$



$$\Delta I_{ds} = g_m \Delta V_g + g_d \Delta V_d - (g_m + g_d) \Delta V_s$$

$$\Delta I_{ds} = -g_m \Delta V_g - g_d \Delta V_d + (g_m + g_d) \Delta V_s$$



Conceptual Small-signal Model



For nmos transistor, increase in gate voltage leads to an increase in drain current.

For nmos transistor, increase in drain voltage leads to an increase in drain current.

For nmos transistor, increase in source voltage leads to a decrease in drain current.

$$g_m \gg g_d$$

For pmos transistor, increase in gate voltage leads to an decrease in drain current.

For pmos transistor, increase in drain voltage leads to an decrease in drain current.

For pmos transistor, increase in source voltage leads to a increase in drain current.

$$g_m \gg g_d$$

