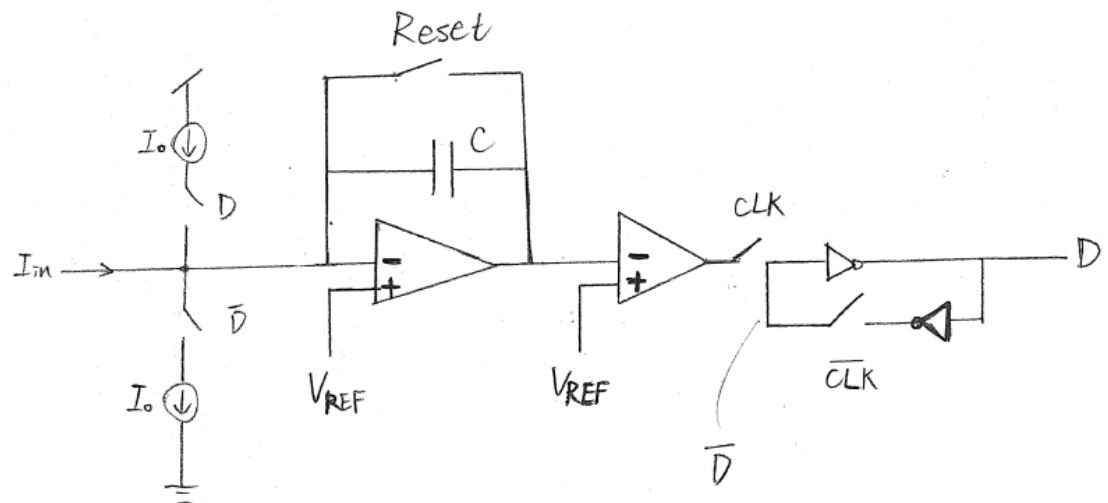
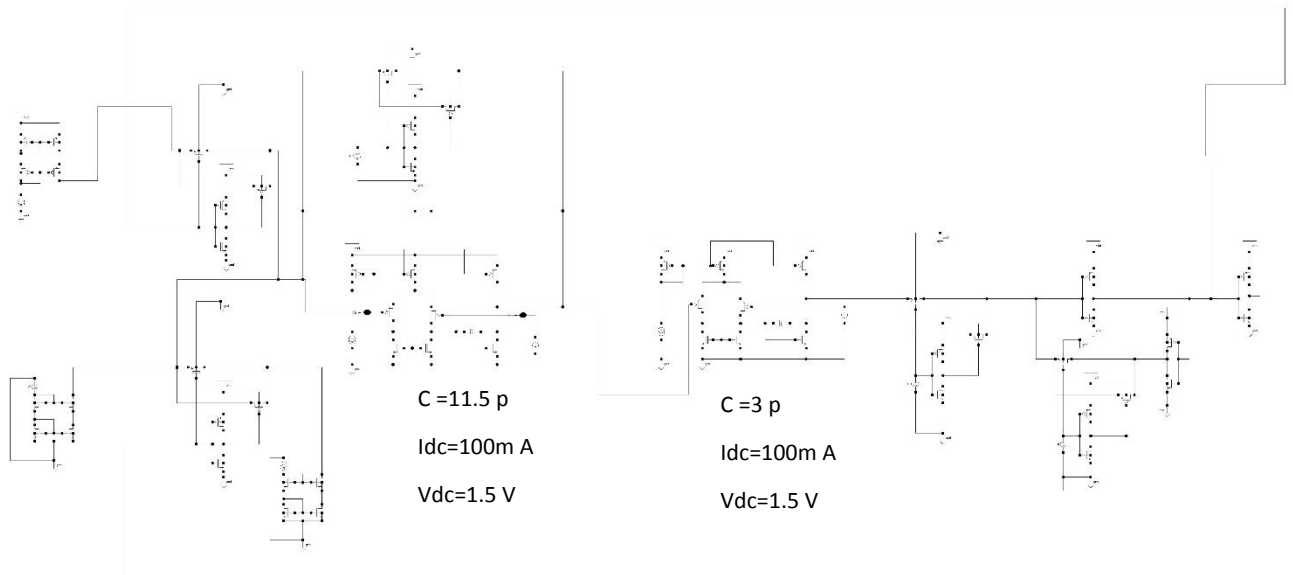


ESE 562\_Project 3

Po Hsu Chen, 448031

## System level architecture with component values (C, I<sub>o</sub>, CLK, V<sub>REF</sub>, V<sub>CMP</sub>)

V<sub>dd</sub> = 3V

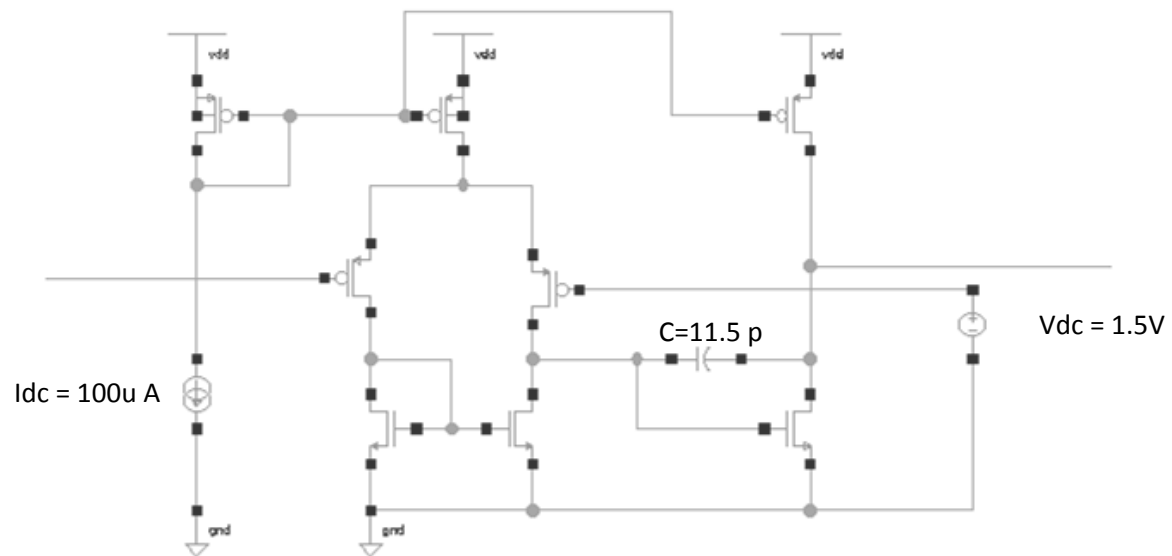


C	I <sub>o</sub>	CLK	V <sub>ref</sub>	V <sub>CMP</sub>
3p	130n A	V pulse 0 ~ 3V (3~0V)	1.5 V	1.5 V
		Pulse width 20u s		
		Period 40u s		

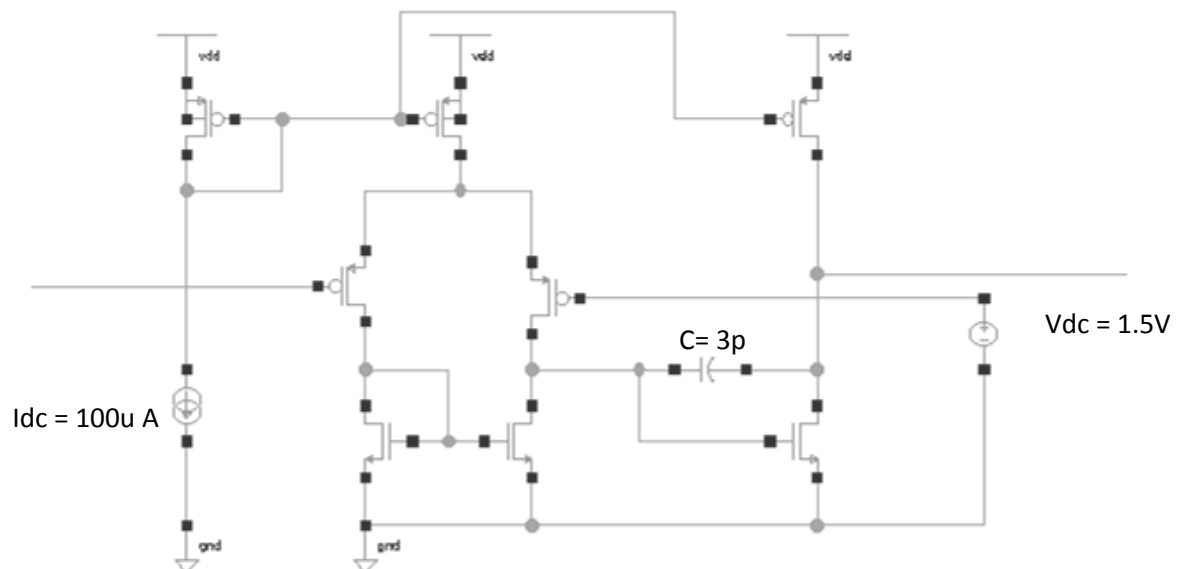
# Amplifier Implementation

I chose the amplifier as the one in project 1.

1.

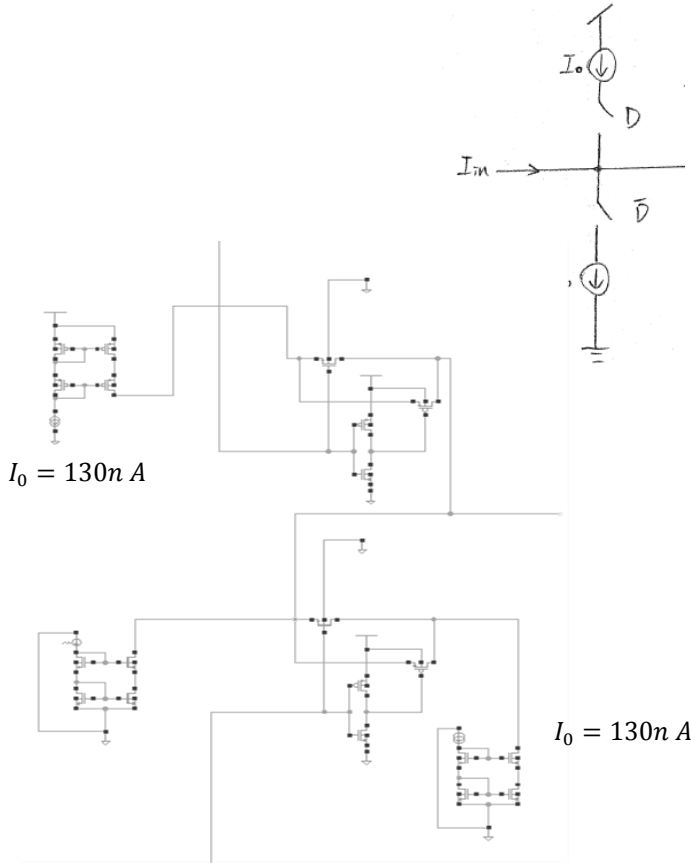


2.

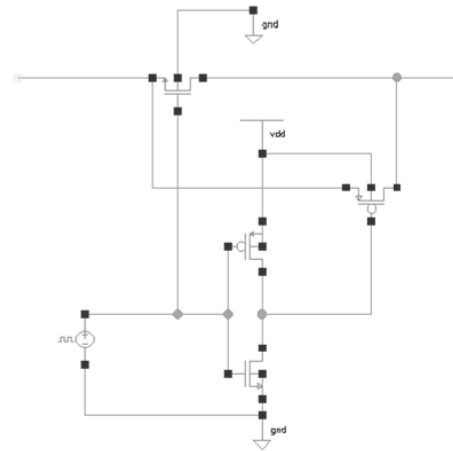
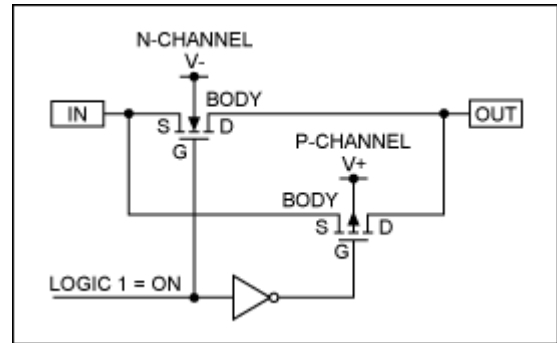


## Implementation

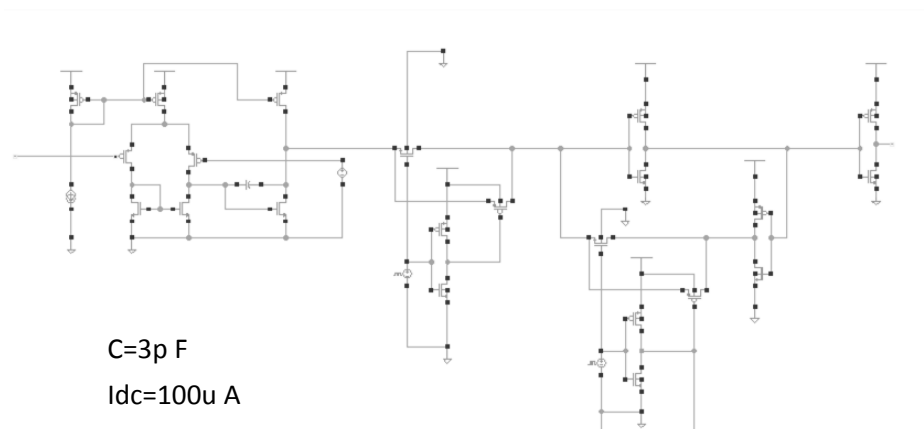
### Current Source and Sink



### CMOS Switch



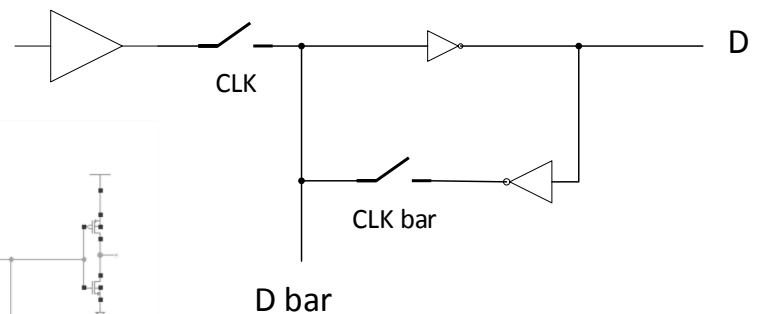
### Latched Comparator



$C=3pF$   
 $I_{dc}=100uA$   
 $V_{dc}=1.5V$

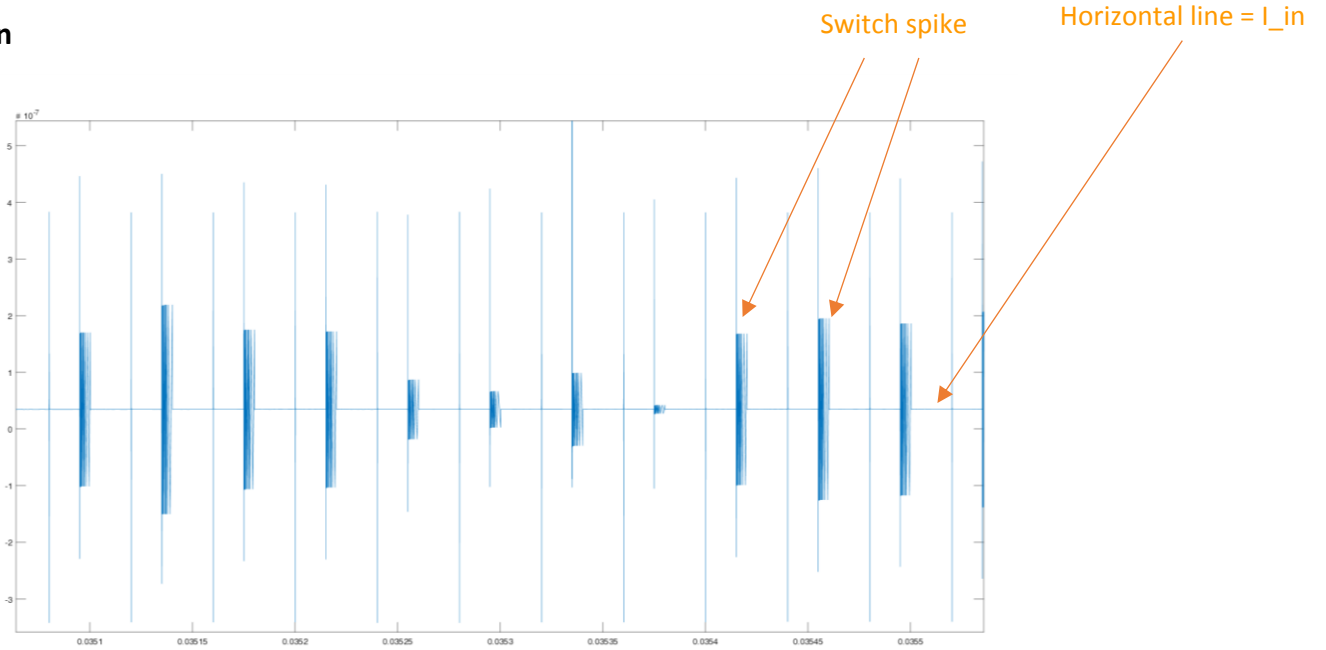
CLK is 0~3V  
 Pulse width 20u s  
 Period 40u s

CLK is 3~0V  
 Pulse width 20u s  
 Period 40u s

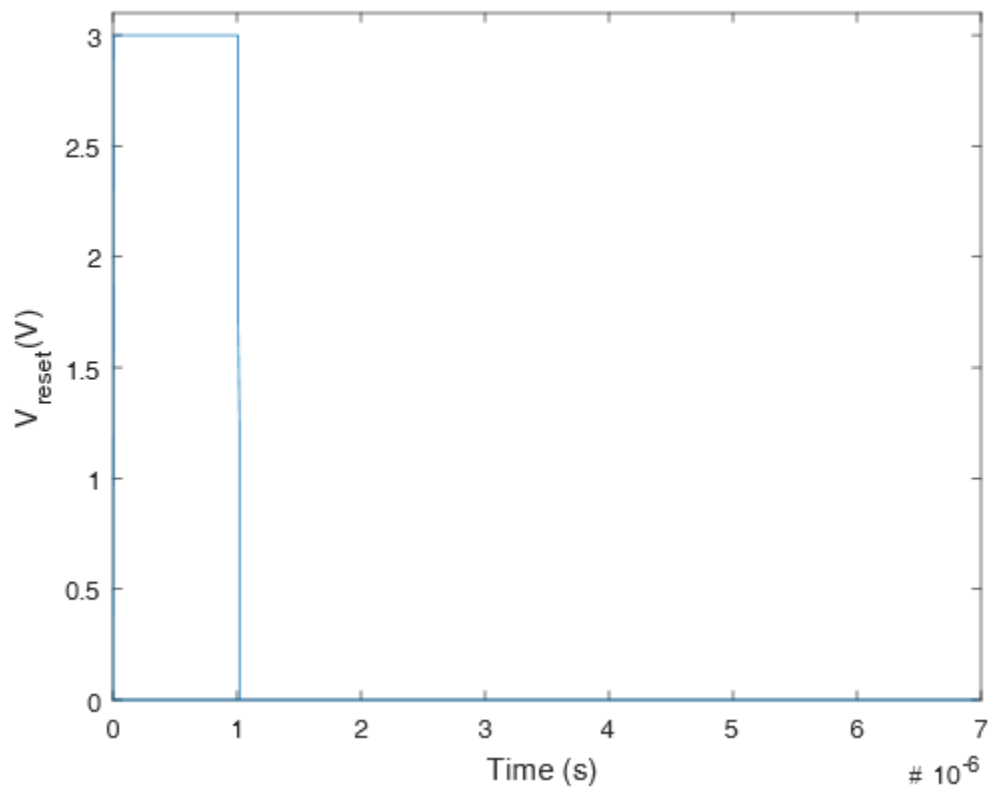


## Output of the modulator and voltage $V_x$

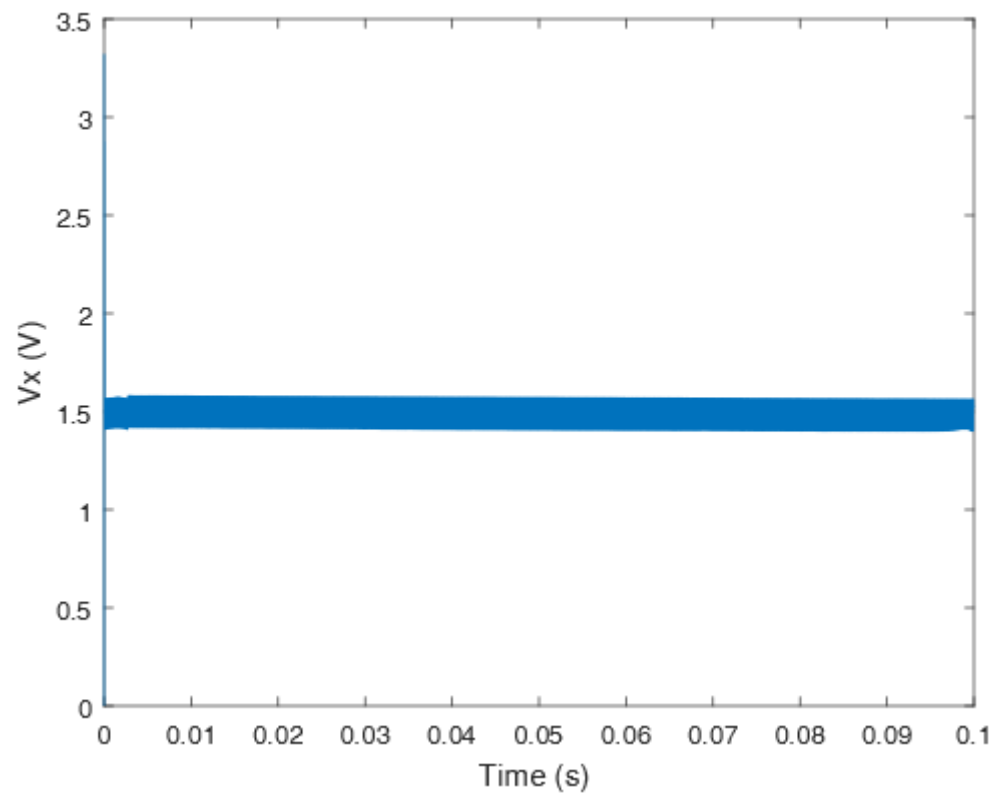
$I_{in}$



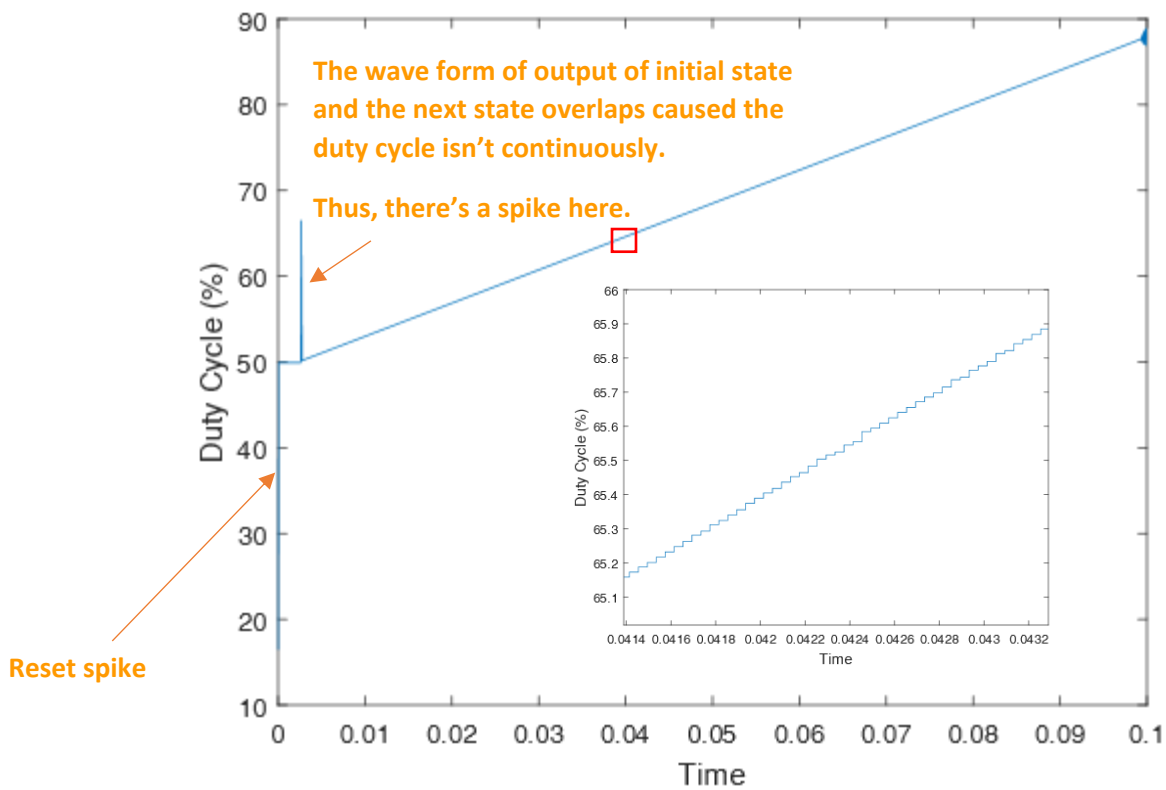
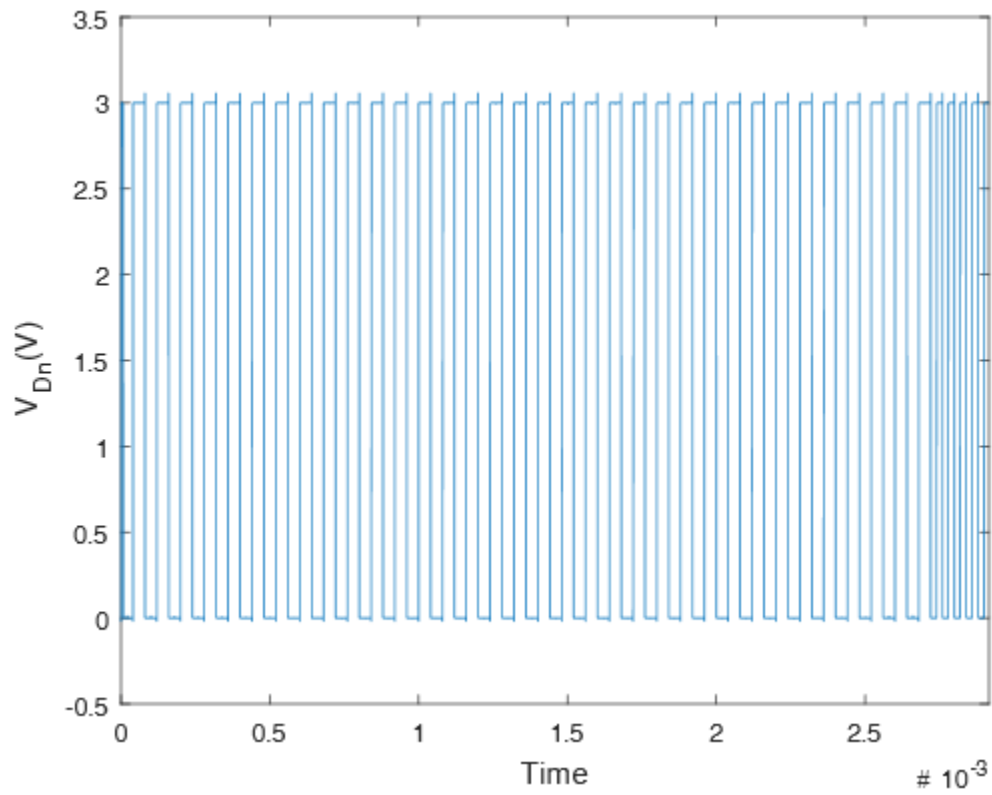
$V_{reset}$ :



**V<sub>x</sub>**



## V<sub>Dn</sub> and Duty Cycle



## Speed:

CLK is 0~3V and 3~0V

Pulse width 20u s

Period 40u s

## Resolution:

Since there are 2410 data points in duty cycle.

$$\log_2 2410 = 11.2348174$$

=>The resolution is 11.2 bit.

## Power Dissipation:

$$P = I * V$$

$$P = 399 \mu A * 3 V = 1.2 m Watt$$