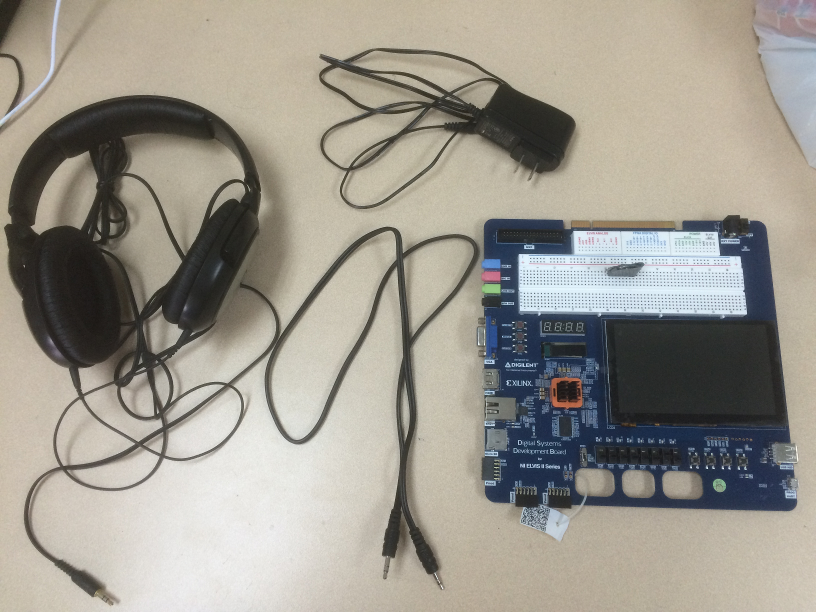
Instrument of DSDB Audio Example

# Hardware requirements



Headphone

Auxiliary cable

DSDB Board

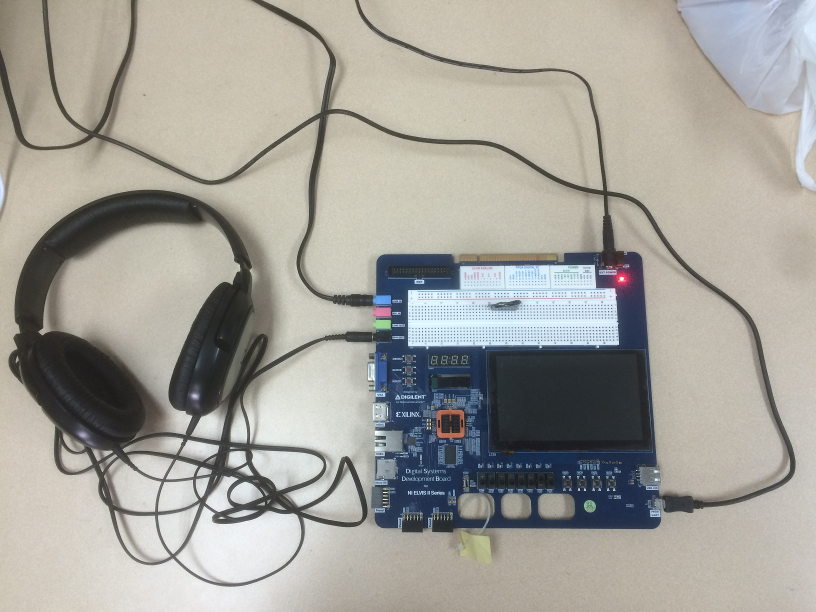
Power adapter

1. DSDB board.
2. 3.5mm auxiliary audio cable.
3. Headphone.
4. PC, used to output analog audio signal.

# Software requirements

1. LabVIEW.
2. LabVIEW FPGA Module.
3. Xilinx Compilation Tools for Vivado.
4. LabVIEW Support for Digital Systems Development Board.

# Hardware connection



Connect LINE IN to PC audio output.

Connect HPH OUT to Headphone.

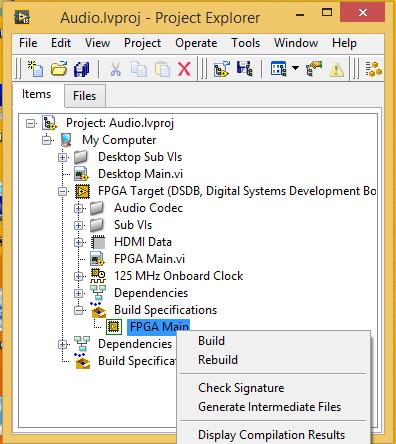
1. Connect PC audio output to DSDB LINE IN jack, via auxiliary cable.
2. Connect Headphone to DSDB HPH OUT jack (Headphone output).
3. 5V power supply is needed, and DSDB PROG port should connect to PC via USB cable.

# Run application

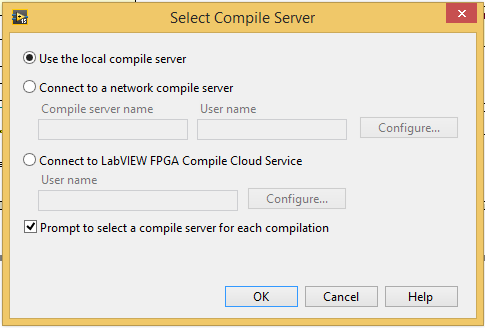
Audio application consist of two part: FPGA VI for implementing low level communication protocols, and Desktop VI for controlling FPGA VI.

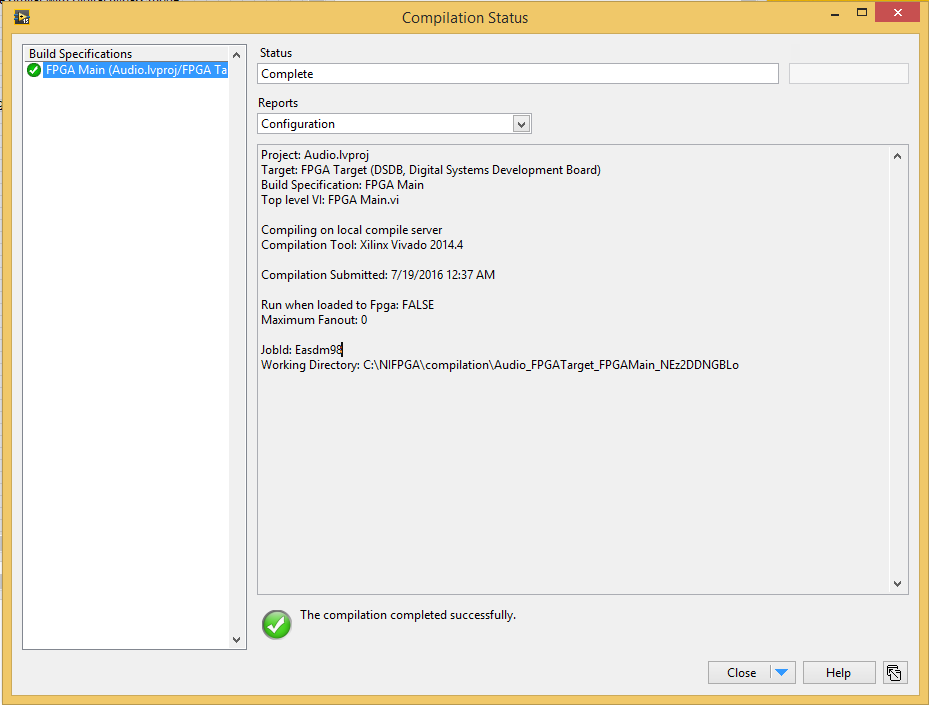
Steps for running application:

1. Turn on the DSDB power supply.
2. Compile FPGA Main VI. Open Audio.lvproj, and right-click the build spec named **FPGA Main** that under the Build Specifications of FPGA Target, then click build.

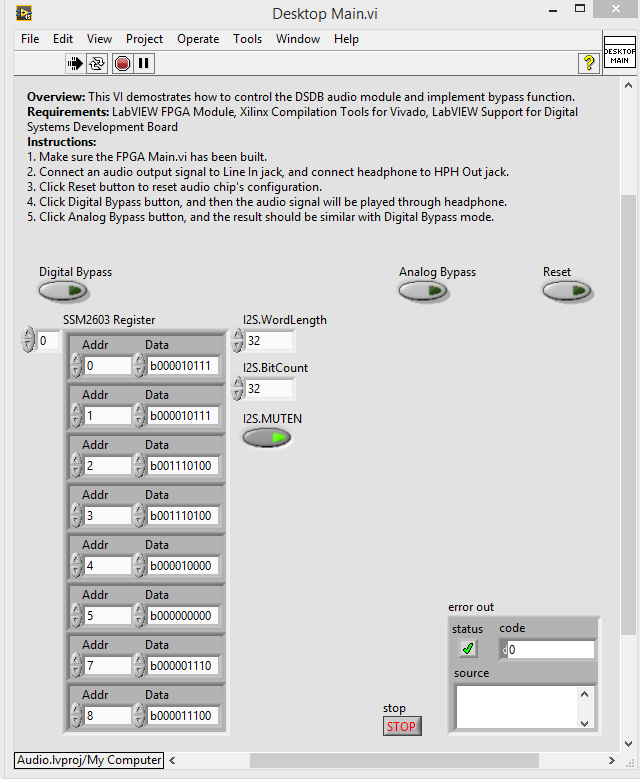


Then you will see a dialog to select compile server. By default, since you have already installed Xilinx compilation tool for Vivado, you can select “Use the local compile server”, and the click OK.





1. After FPGA Main compilation completed, open the Desktop Main.vi , and click run.



1. Reset audio chip. Click Reset button, FPGA will send a reset command to audio chip SSM2603, that will reset all SSM2603 registers value and disable signal output.
2. Enable audio signal bypass mode. Click “Digital Bypass” or “Analog Bypass” button, and play a song through your PC, then you will hear the song from headphone.

There are two types of bypass mode: digital bypass and analog bypass, both of them could transfer analog audio signal from LINE IN to HPH OUT jack. The difference is, in analog bypass mode, LINE IN directly connect to HPH OUT in audio chip like a wire, but in digital bypass mode, audio signal will firstly be converted to digital signal that read into FPGA, and then FPGA write the same signal data out to audio chip, finally audio chip convert digital data into analog audio signal and output via HPH OUT jack.

Since digital data will read into FPGA in Digital Bypass mode, it’s easy for users to adding additional audio signal process in FPGA code or generating custom audio signal.