CBUS FIRMWARE – New Parameter Structure – Issue 6

This is an updated version of the parameter structure issued in October 2015

This note provides an explanation of the Parameter Structure and some of the reasons for it. The main driver behind the need to improve the parameters is to allow the Bootloader in PC software, such as FCU, to make correct decisions on how to Bootload a module as new processor types are introduced. There was actually not enough information in the initial seven parameters to do this in anything like a reliable way, and it was not future proof.

The initial structure had 7 parameters and were at 0x0810 in the memory image, The previous version of this document updated this so that future firmware developments would place the parameters in an enhanced structure at 0x820 in the memory image. The new parameter structure allows space for up to 24 parameters in total. The total memory space reserved for the new parameter structure is 32 bytes.

The original 7 parameters were, in order (all a treated as an unsigned byte except where indicated

Parameters are read using the RQNPN Opcode. Index 0 always the number of parameters that are implemented.

The first 7 parameters (Index 1 to Index 7) are returned by the RQNP Opcode during setup.

index 0	Number of parameters
Index 1	Manufacturer's Id
Index 2	Minor Version (a character)
Index 3	Module Id
Index 4	No. of events
Index 5	No of Event Variables per event
Index 6	No of Node Variables
Index 7	Major version

The new structure always exists at 0x820 for 8 bit PIC microprocessors and reserves 32 bytes for the parameters. The first 7 parameters are the same as the original definition. Other processors can hold the parameters in any suitable location.

Index 8	Flags - this identifies the module class in the ls 2 bits - encoded, No Events = 0, Consumer = 1, Producer = 2, Combi = 3. It also includes the FLiM bit (bit 2) and the Bootable bit (bit 3) see below for more information.
Index 9	Processor Id - defines the processor, e.g. 2480, 25K80 the firmware was built for. Set to zero for non-PIC processors
Index 10	Interface protocol - the network type that the module uses, currently either CAN (1) or Ethernet (2)
Index 11-14	The load address for the new code, this is a 4 byte little endian address, this can vary depending on the module being loaded, the normal address for all PIC processor is 0x800 except for the CANCAB language modules which are loaded above the code area. Currently only used by PIC processors, other processors should set these parameters to zero
Index 15-18	Manufacturers processor code – this is a four-byte field, only the first two bytes are used for the PIC18F processor family, this must be read directly from the hardware when requested. Currently only used by PIC processors, if implemented. If not used, the parameters must be set to zero.
Index 19	Manufacturer code – this parameter identifies the manufacturer
Index 20	Beta release code – a non-zero value specifies the beta release version, zero indicates a normal release

When Bootloading, the FCU looks in the memory image of the new firmware for a valid parameter block at 0x820. If none is found at this location, then looks at 0x810 to check for the presence of any parameters. If the parameters are found at 0x0810, the FCU assumes the current processor is a PIC18F2480 and only the basic parameters are available for reading.

The parameters are zero filled up to and including 0x0837 allowing room for a total of 24 parameters.
The following information is included from 0x0838, but is not accessible as a readable parameter by index.

- The number of parameters implemented (2 bytes), the actual number of parameters between 0x0820 and 0x0837 inclusive (Note: it can be read as a parameter with Index 0).
- The little endian address of the module name string (4 bytes)
- A 2-byte checksum of the parameters

The Flags parameter is dynamic, when read using the Op Codes RQNPN or QNN and should be created dynamically if necessary, The Bootable flag is set by the firmware if the current Bootloader is compatible with the firmware. The flags parameter is also returned as part of the data in the PNN opcode and includes the extra FLiM mode and Bootable bits. PNN is the response to a QNN.

The Manufacturers processor code must be read at run time, 4 bytes are reserved for this parameter but only the first two are needed for PIC18F processors. Unused bytes must return zero.

For PIC18F processors these two bytes contain the DEVID1 and DEVID2 values read from addresses 0x3FFFFE and 0x3FFFFF respectively in configuration space.

The number of parameters can be accessed by software using the read parameter Op Code RQNPN with an index of 0. This allows any software to determine the parameter structure and hence what information is available.

The FCU uses various parameters during Bootloading, the Processor Id is used to check whether the new module code is compatible with the current module. The PIC18F2480 family is not completely binary compatible with the PIC18F66K80 family due to internal changes in the newer PIC family. The FCU will warn the User if an attempt is made to load incompatible firmware.

The load address determines where in the memory image the Bootloader should start the bootload process, this always 0x800 for firmware.

The use of full 4 byte addresses for the load address and the Module string name will allow the structure to be used with microprocessors with a different memory structure in the future.

All new firmware developments should use the new structure.

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July 2016