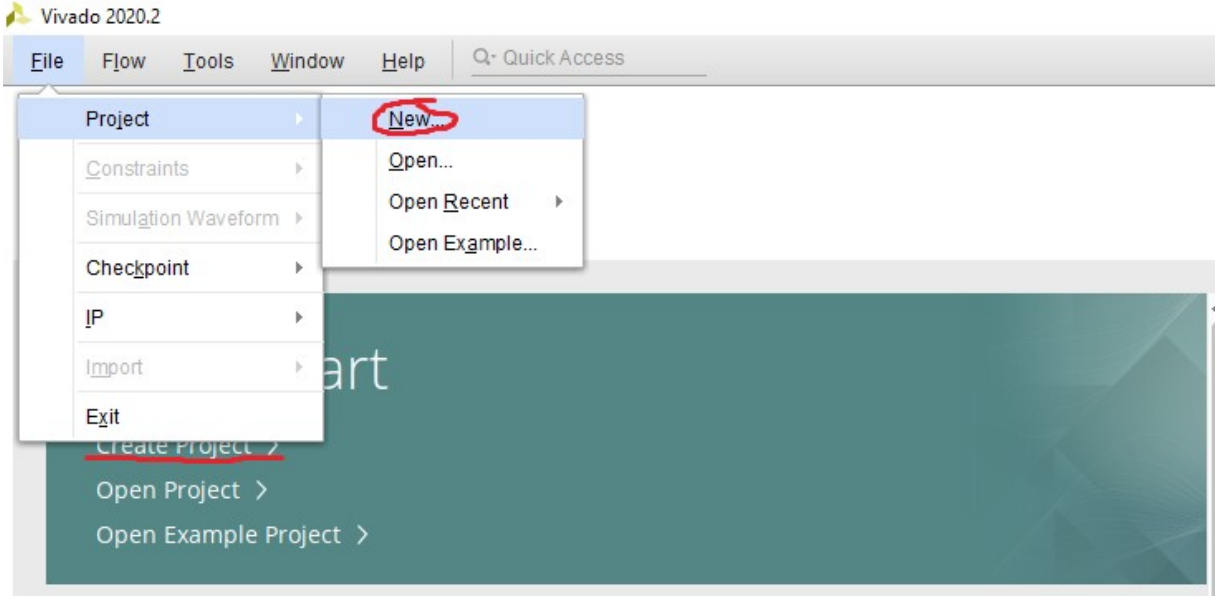
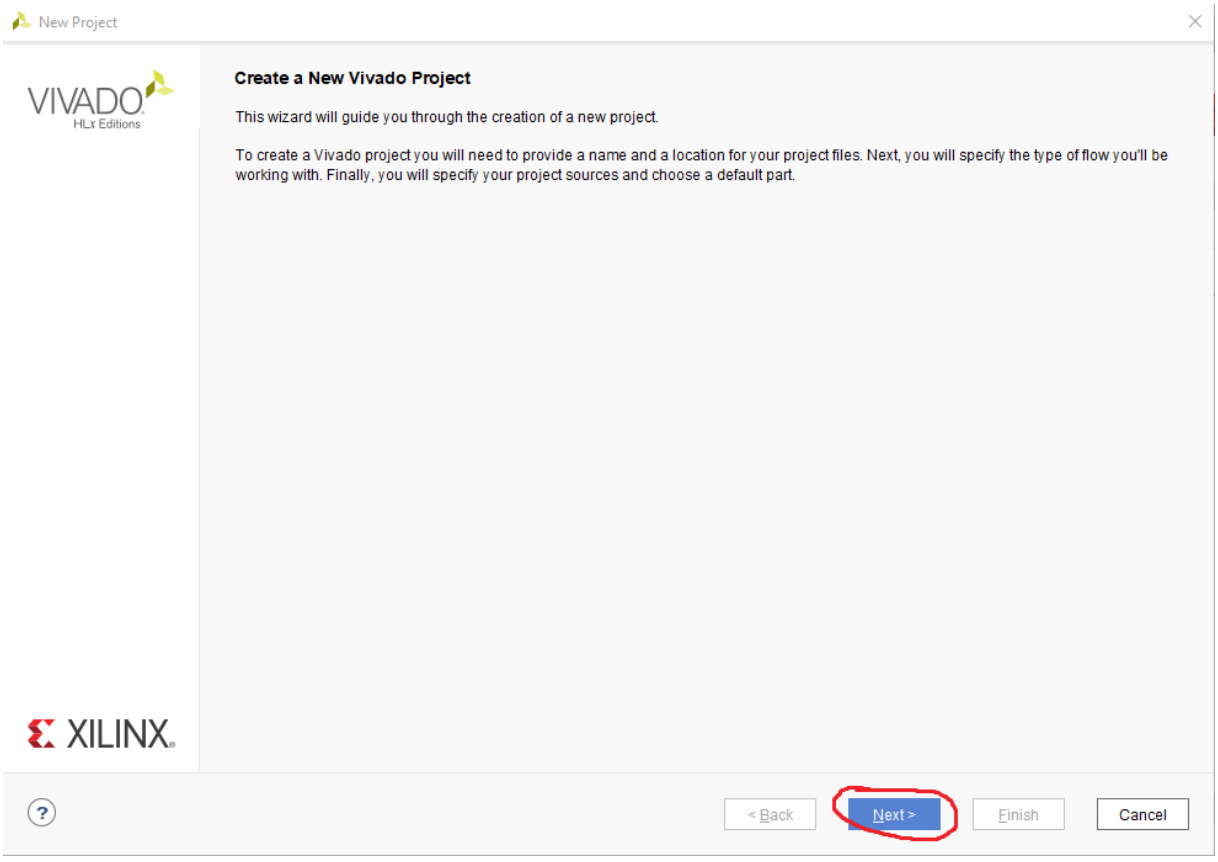
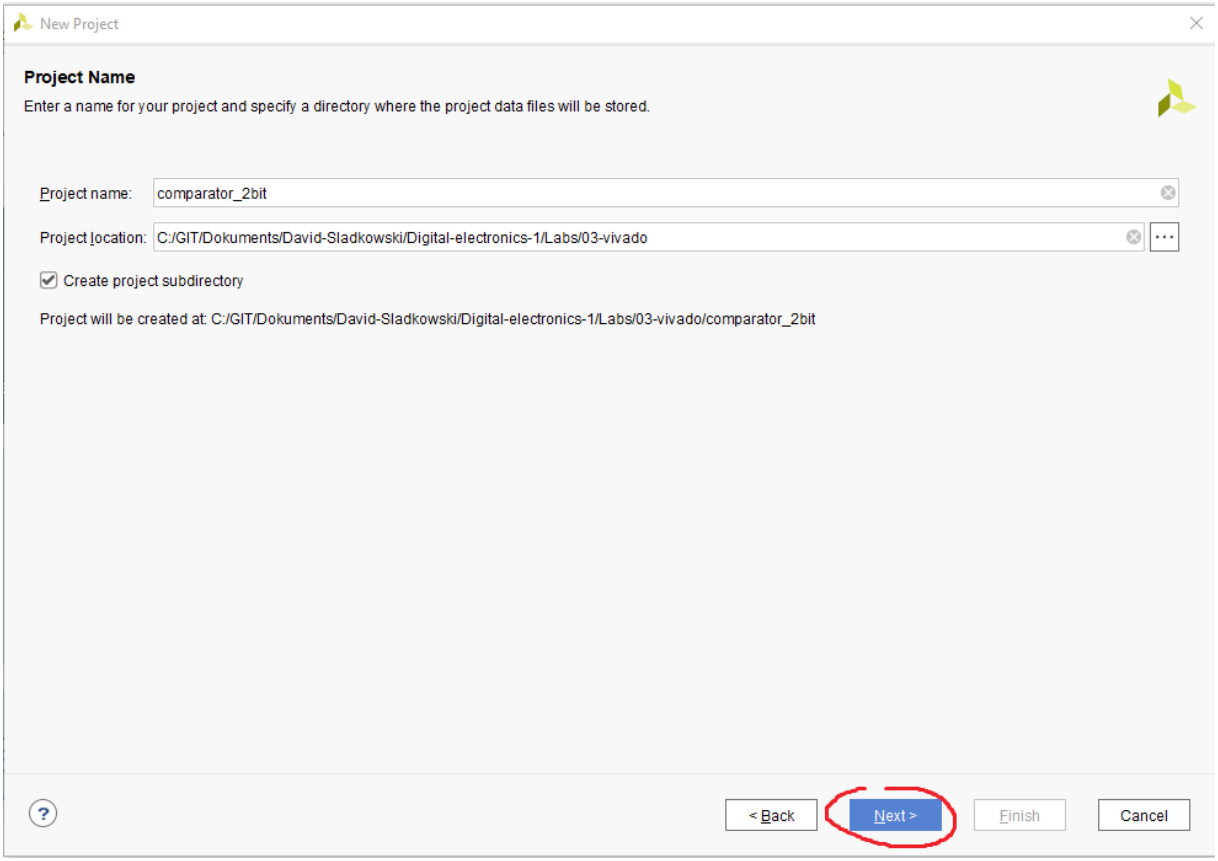
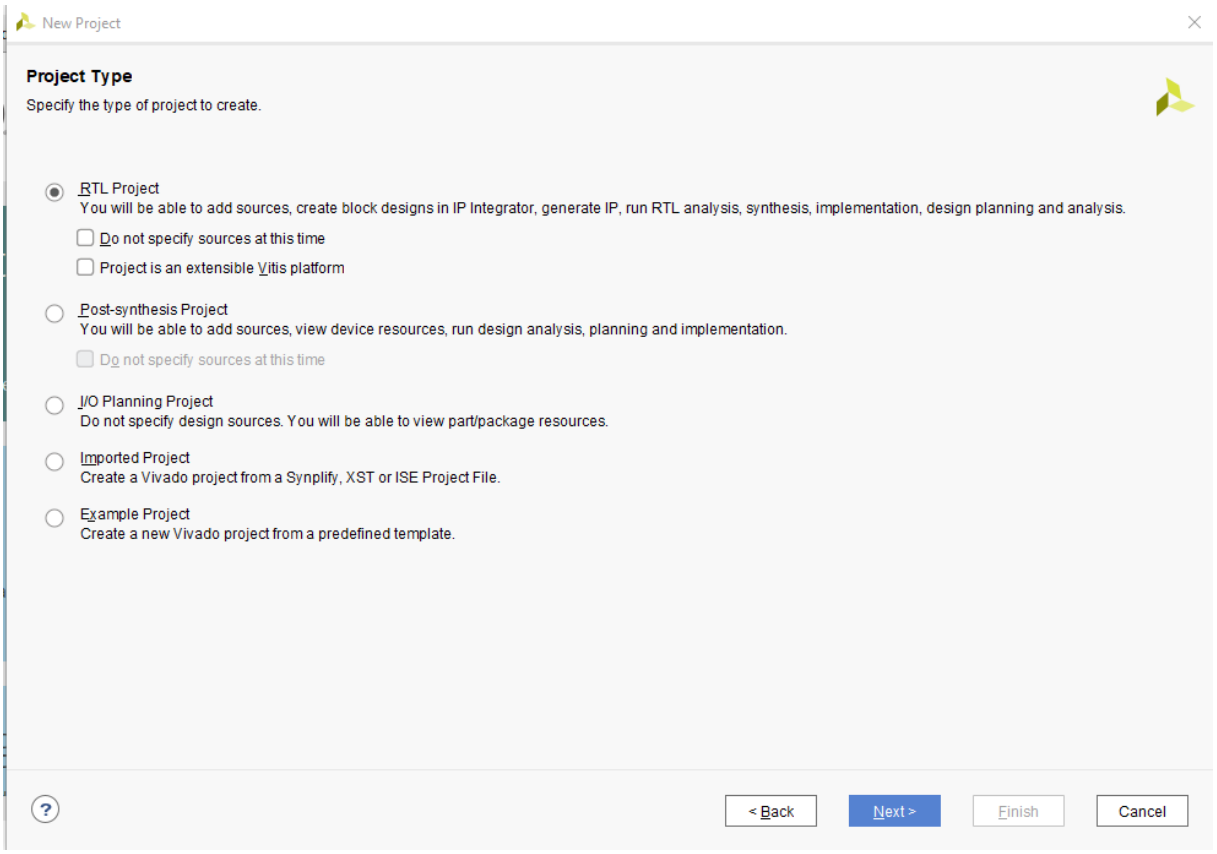
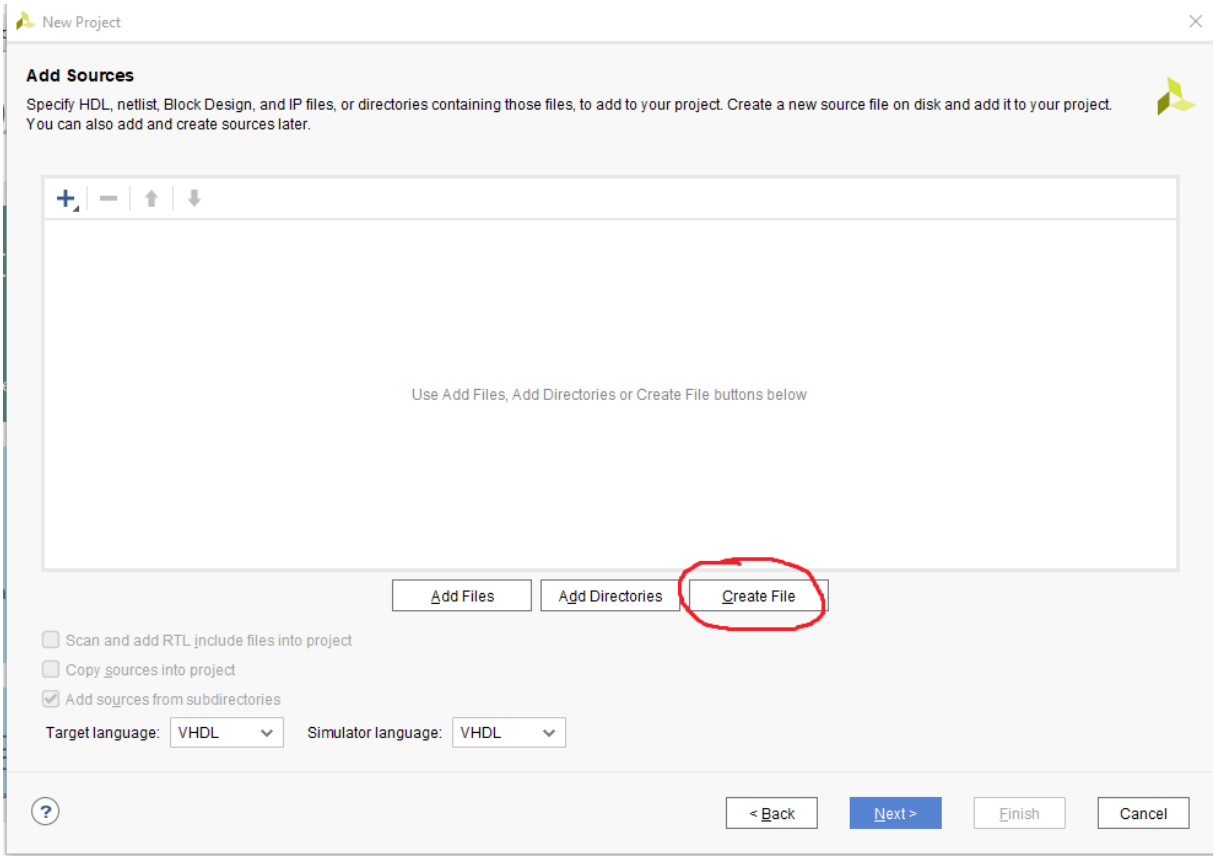
Založení projektu:

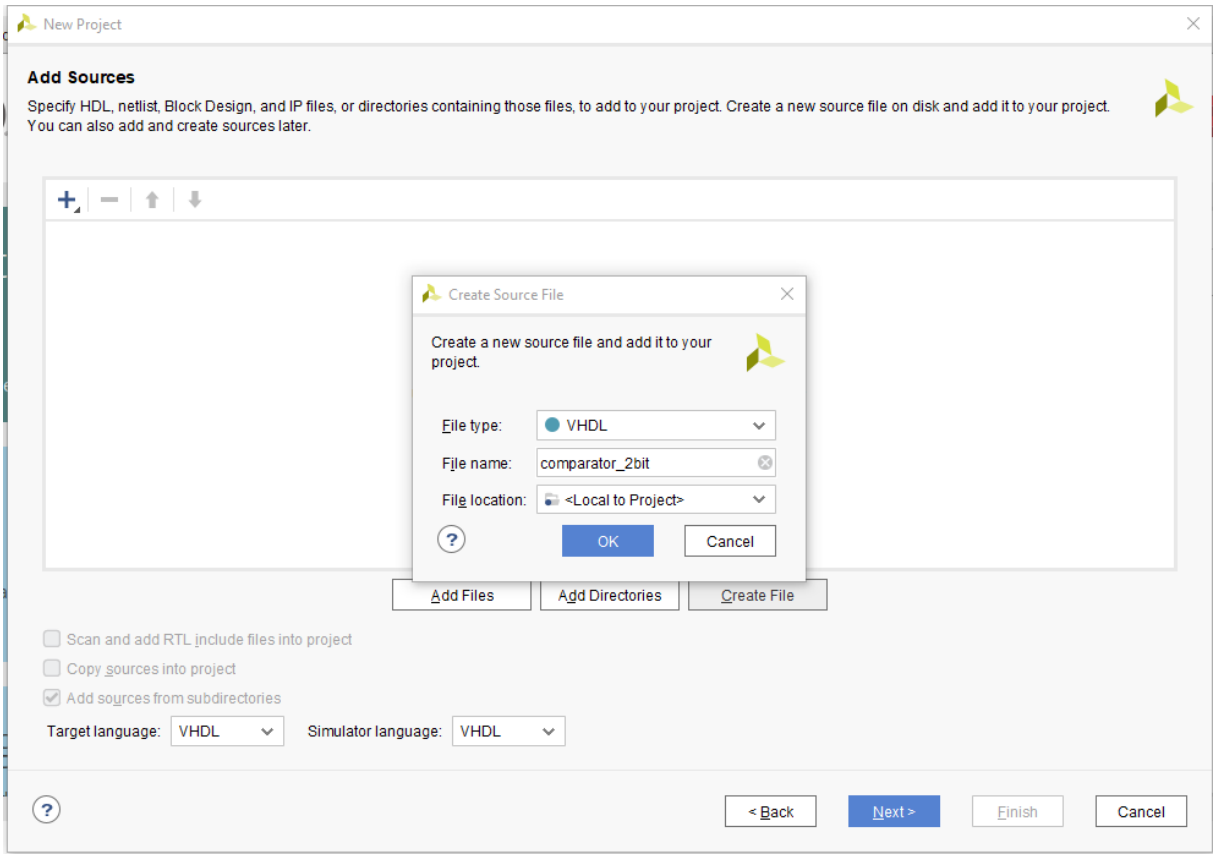


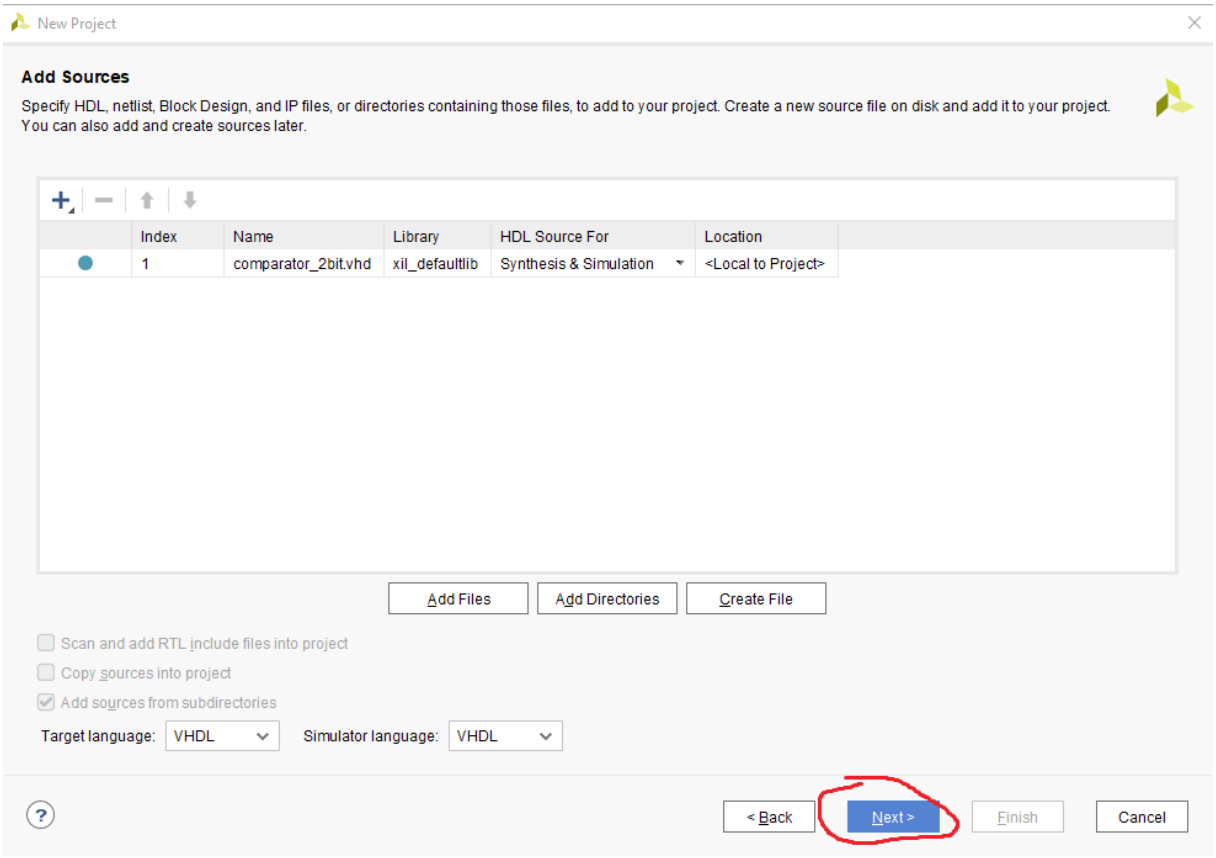


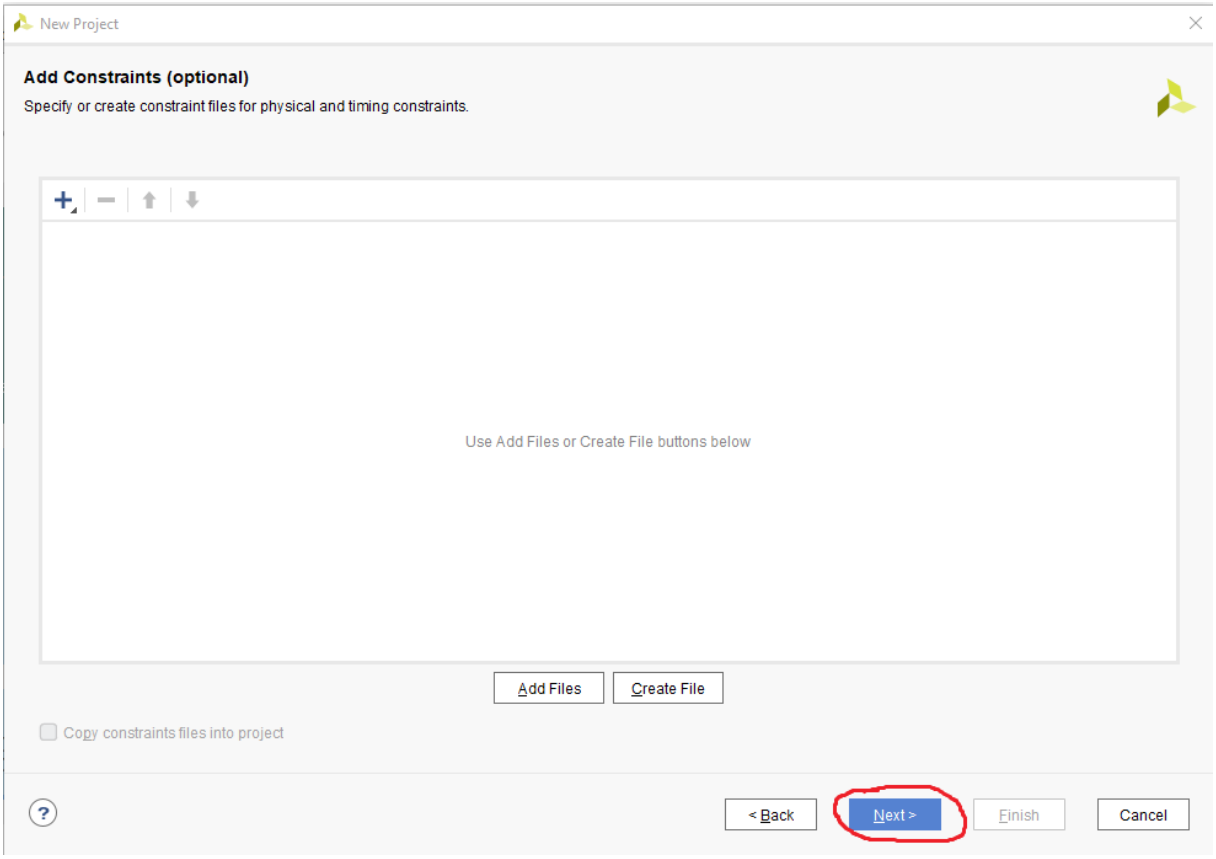

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
comparator_2bit
Project location:
C:/GIT/Dokuments/David-Sladkowski/Digital-electronics-1/Labs/03-vivado
Create project subdirectory
Project will be created at: C:/GIT/Dokuments/David-Sladkowski/Digital-electronics-1/Labs/03-vivado/comparator_2bit
< Back
Next >
Finish
Cancel

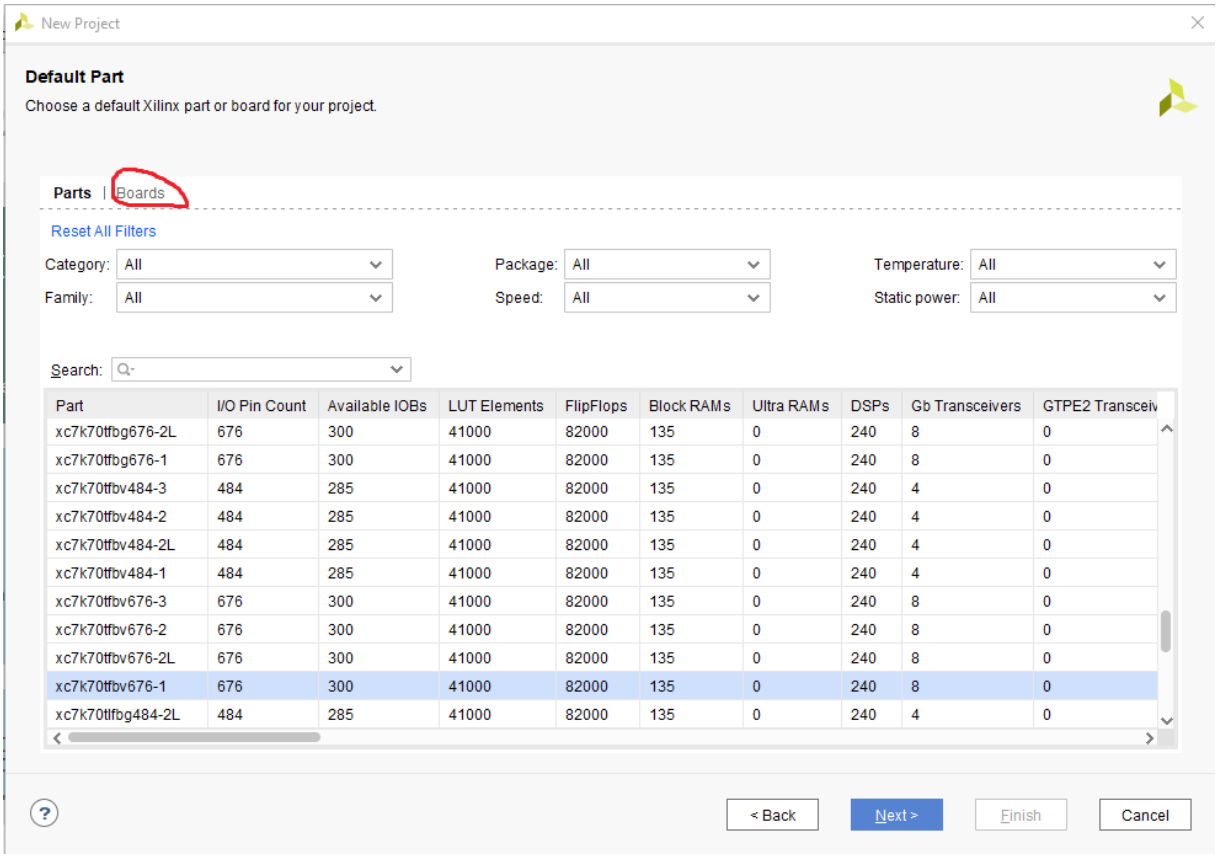

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

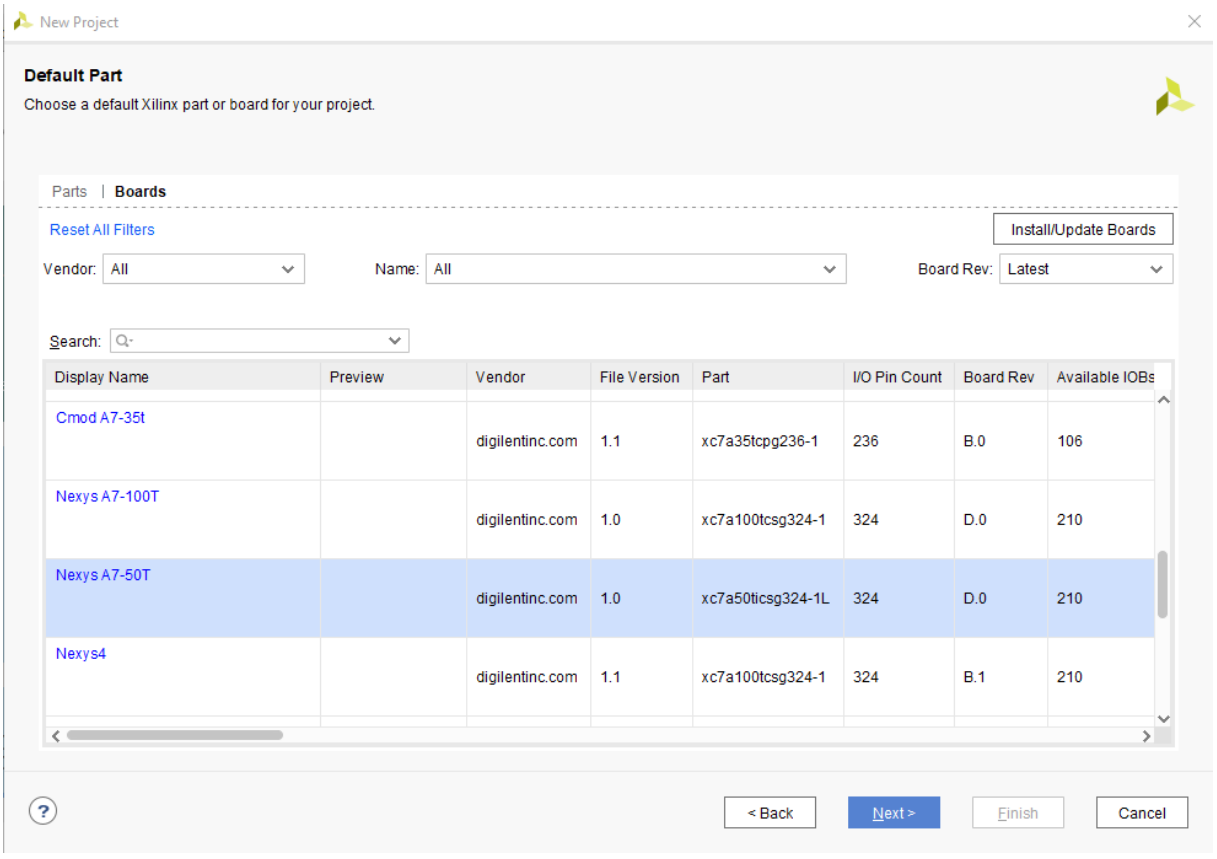

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project.
You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

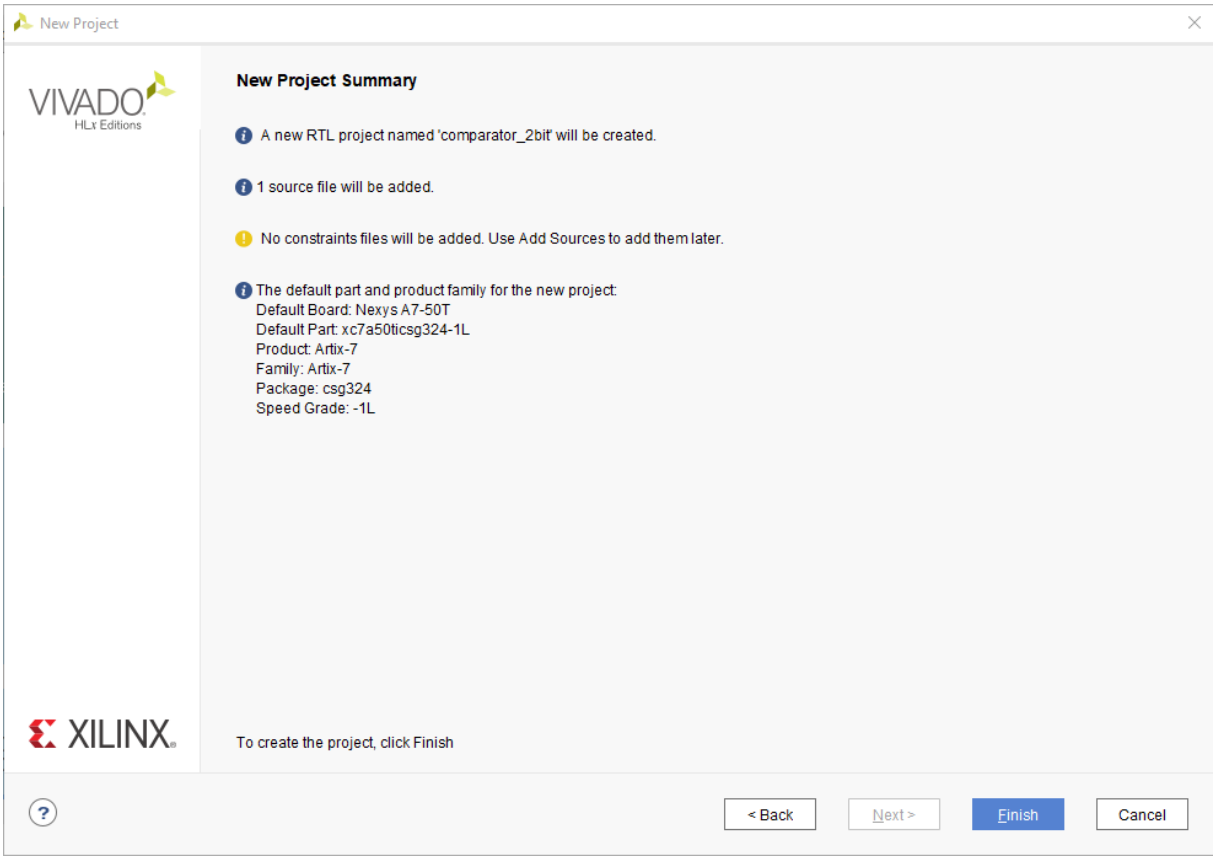

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project.
You can also add and create sources later.
Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: comparator_2bit
File location: <Local to Project>
OK
Cancel
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

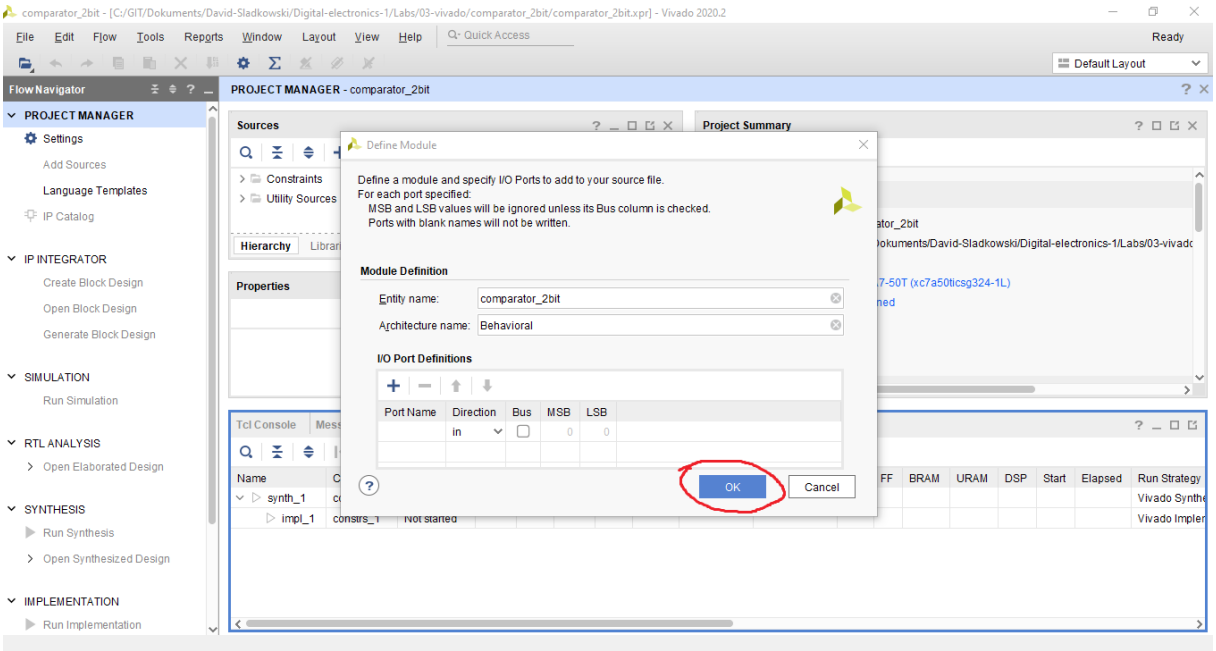

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project.
You can also add and create sources later.
Index
Name
Library
HDL Source For
Location
1
comparator_2bit.vhd
xil_defaultlib
Synthesis & Simulation
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language:
VHDL
Simulator language:
VHDL
< Back
Next >
Finish
Cancel

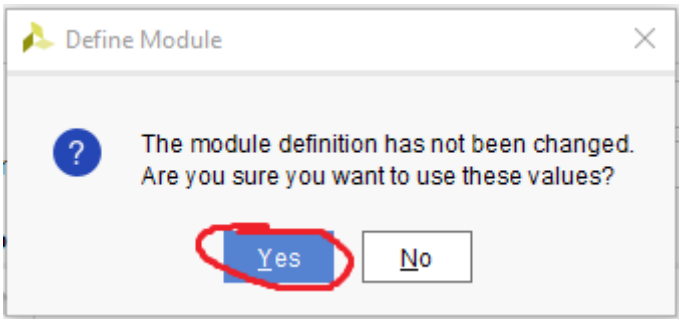

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

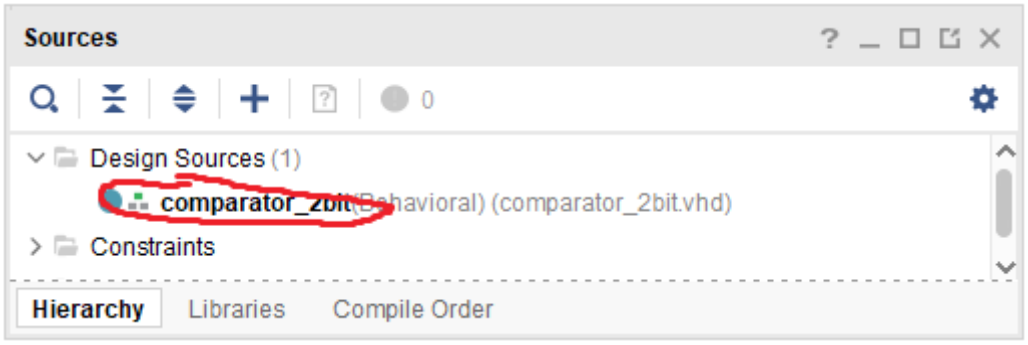

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: All
Family: All
Package: All
Speed: All
Temperature: All
Static power: All
Search:
Part | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra RAMs | DSPs | Gb Transceivers | GTPE2 Transceiv
xc7k70tfbg676-2L | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0
xc7k70tfbg676-1 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0
xc7k70tfbv484-3 | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0
xc7k70tfbv484-2 | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0
xc7k70tfbv484-2L | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0
xc7k70tfbv484-1 | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0
xc7k70tfbv676-3 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0
xc7k70tfbv676-2 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0
xc7k70tfbv676-2L | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0
xc7k70tfbv676-1 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0
xc7k70tlfbg484-2L | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0
< Back
Next >
Finish
Cancel

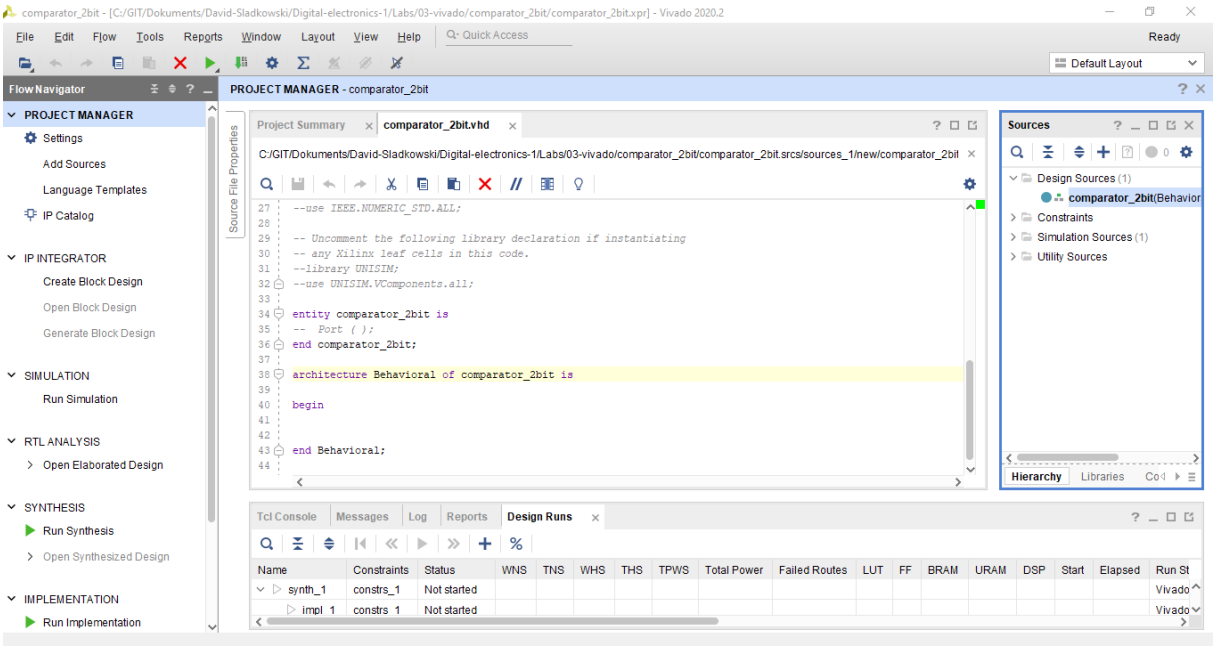

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name | Preview | Vendor | File Version | Part | I/O Pin Count | Board Rev | Available IOBs
Cmod A7-35t | digilentinc.com | 1.1 | xc7a35tcpg236-1 | 236 | B.0 | 106
Nexys A7-100T | digilentinc.com | 1.0 | xc7a100tcsg324-1 | 324 | D.0 | 210
Nexys A7-50T | digilentinc.com | 1.0 | xc7a50ticsg324-1L | 324 | D.0 | 210
Nexys4 | digilentinc.com | 1.1 | xc7a100tcsg324-1 | 324 | B.1 | 210
< Back
Next >
Finish
Cancel


New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'comparator_2bit' will be created.
1 source file will be added.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Board: Nexys A7-50T
Default Part: xc7a50ticsg324-1L
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1L
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel

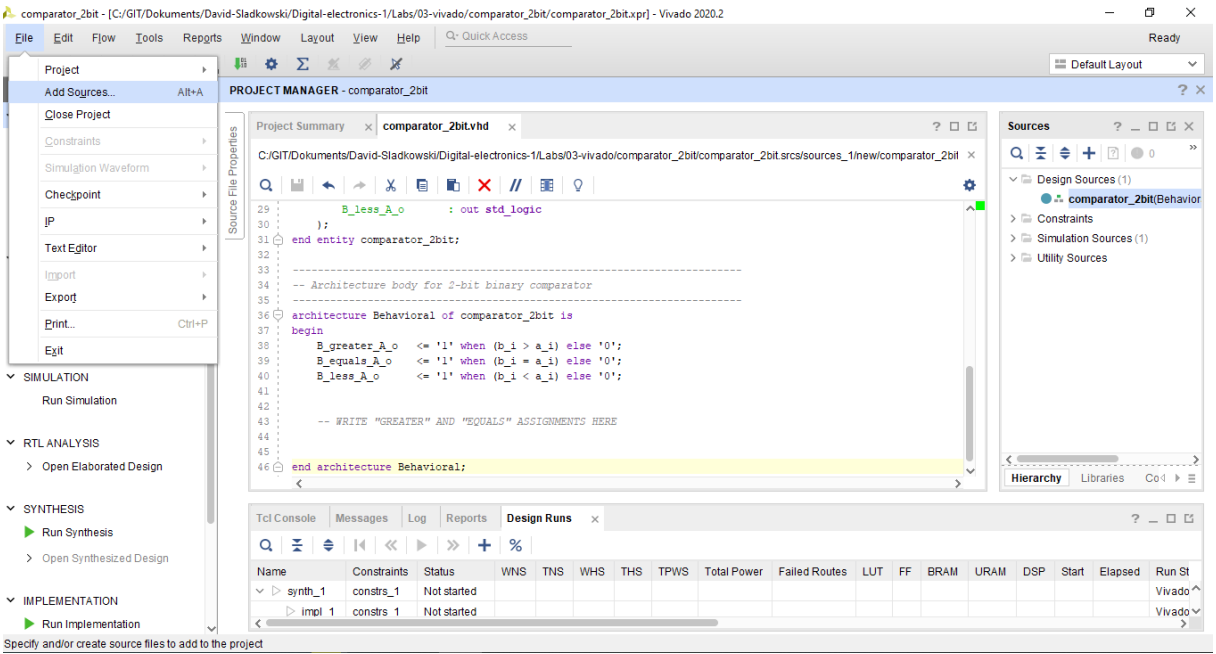

File Edit Flow Tools Reports Window Layout View Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
PROJECT MANAGER - comparator_2bit
Sources
Constraints
Utility Sources
Hierarchy
Properties
Project Summary
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name: comparator_2bit
Architecture name: Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
OK
Cancel
Tcl Console
Name
synth_1
impl_1
Run Strategy

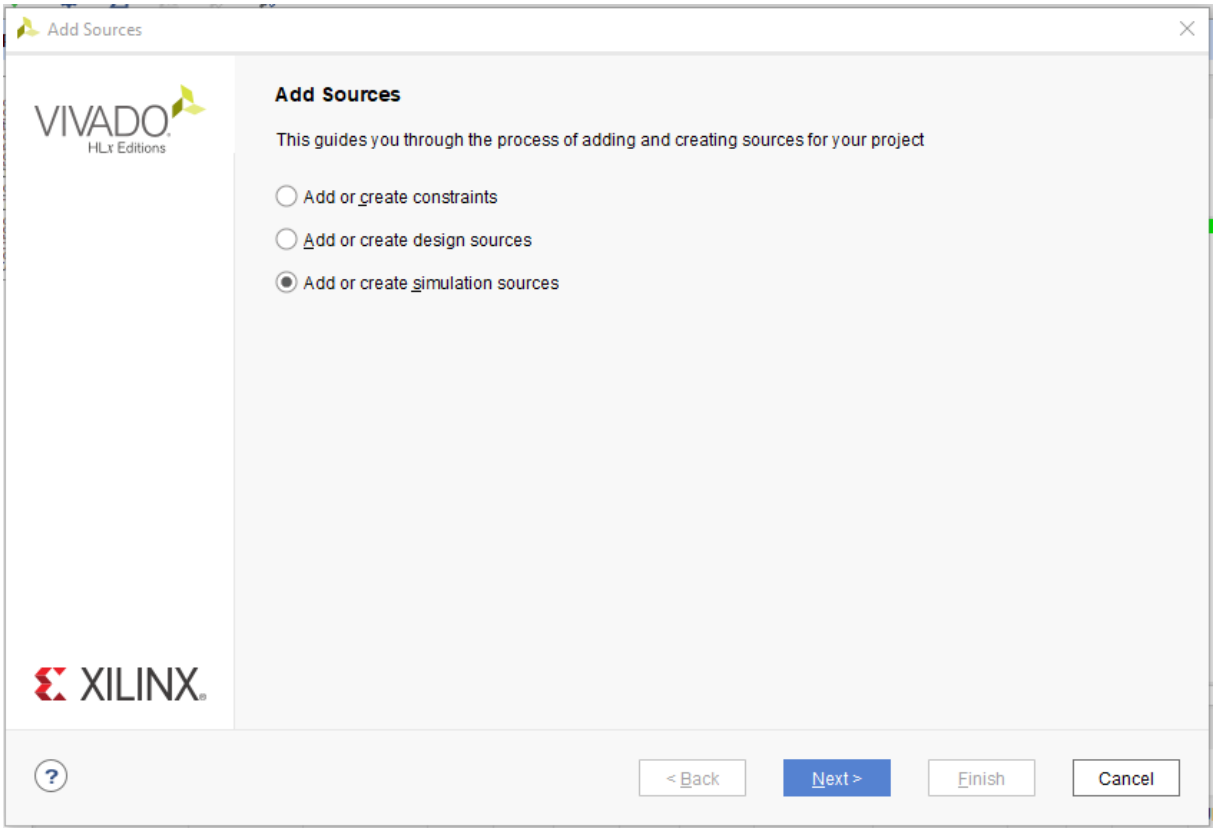

Define Module
The module definition has not been changed.
Are you sure you want to use these values?
Yes
No

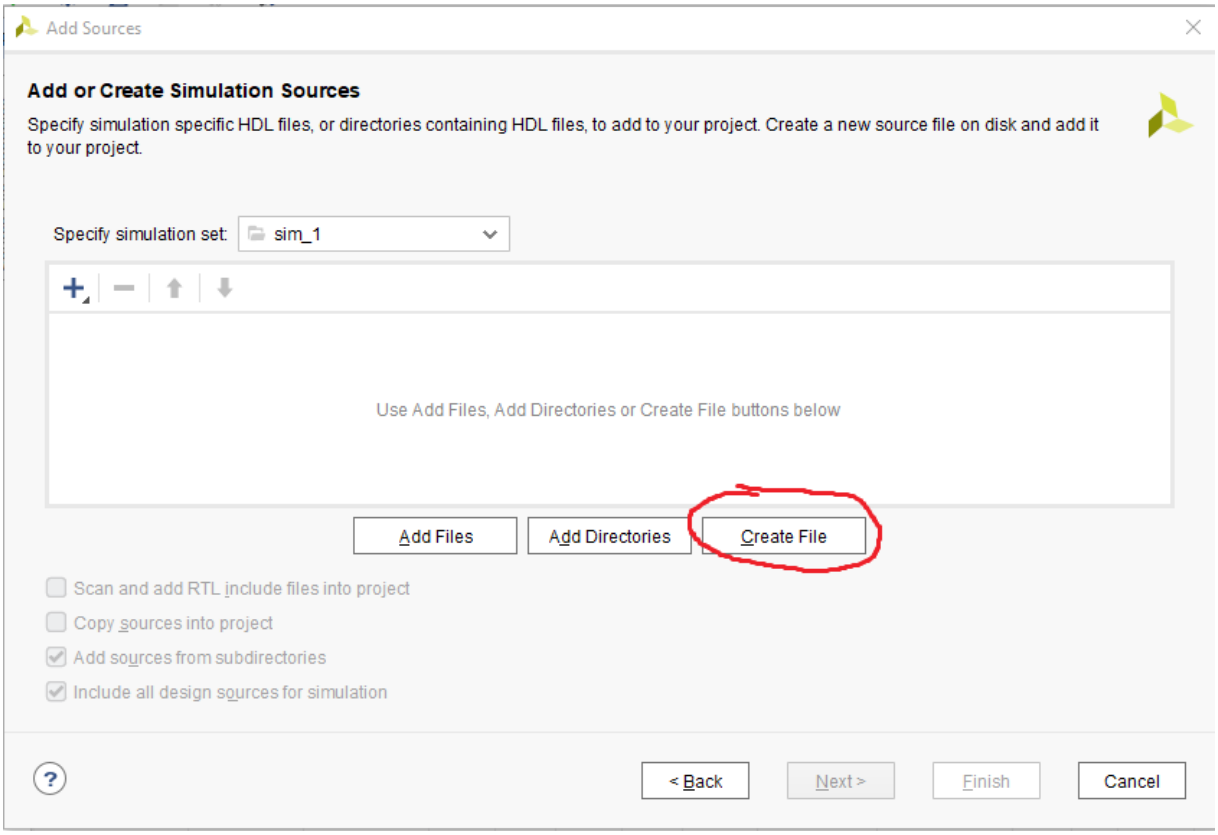


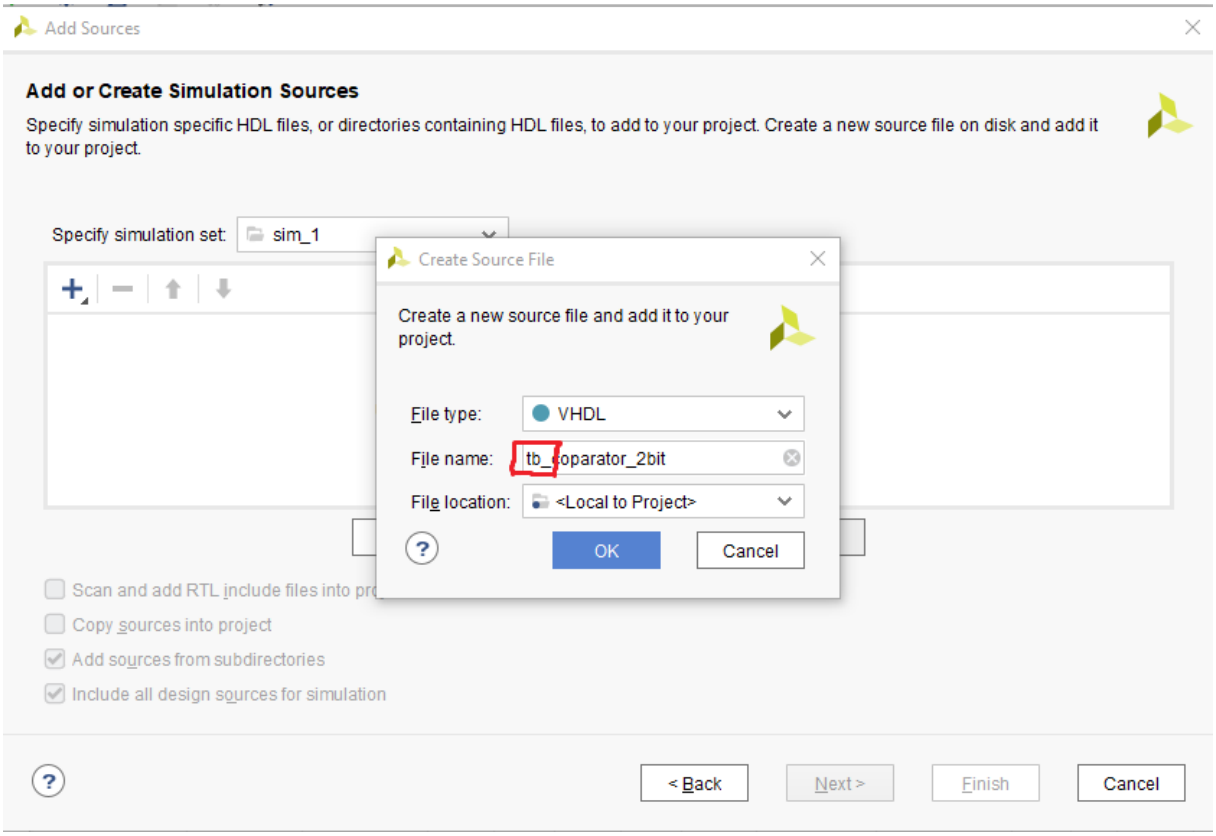


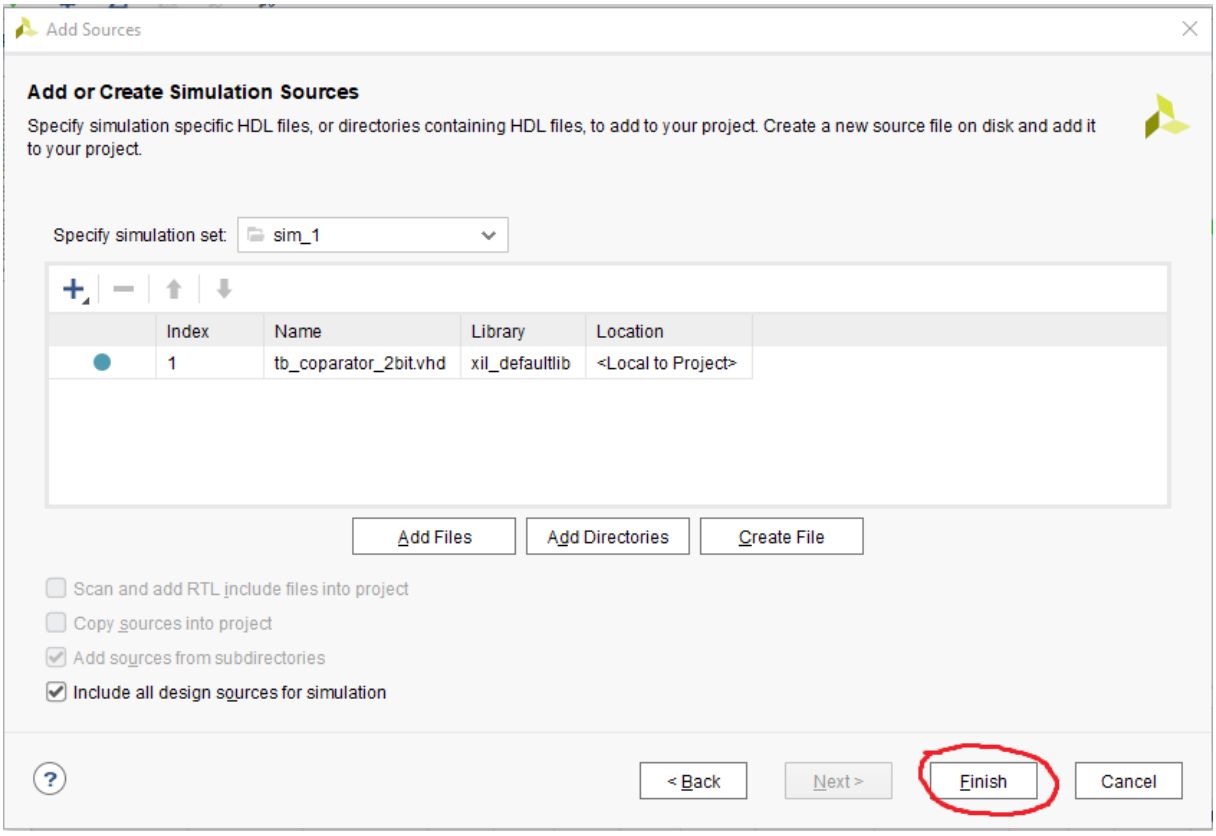
Přidání testbenche:

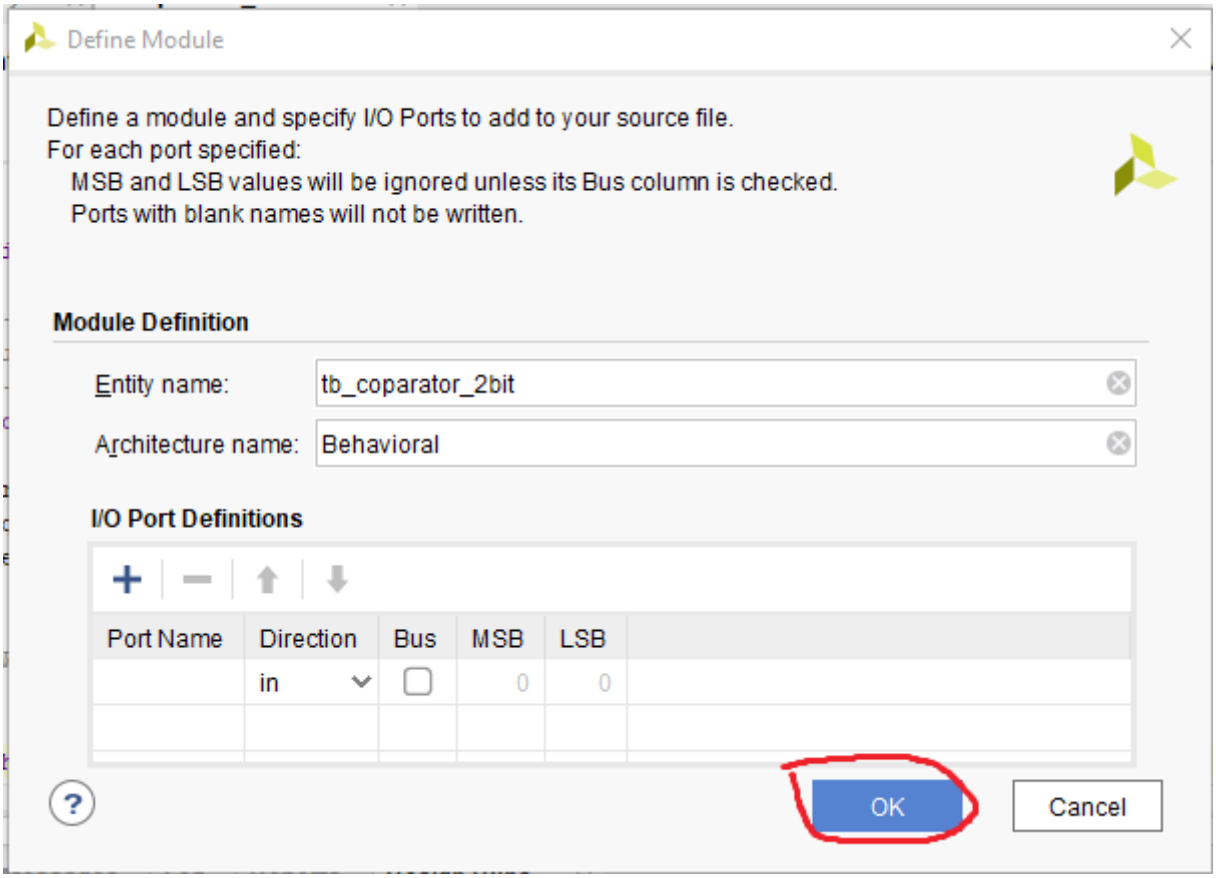


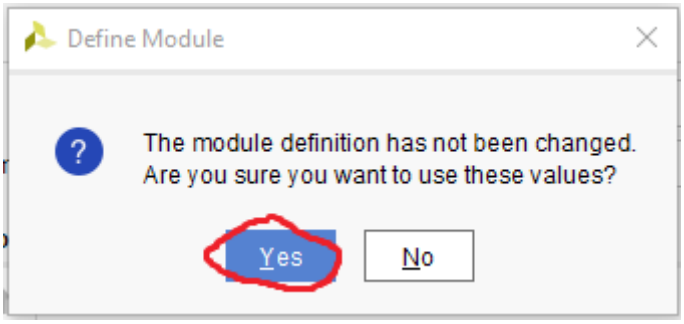

Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel

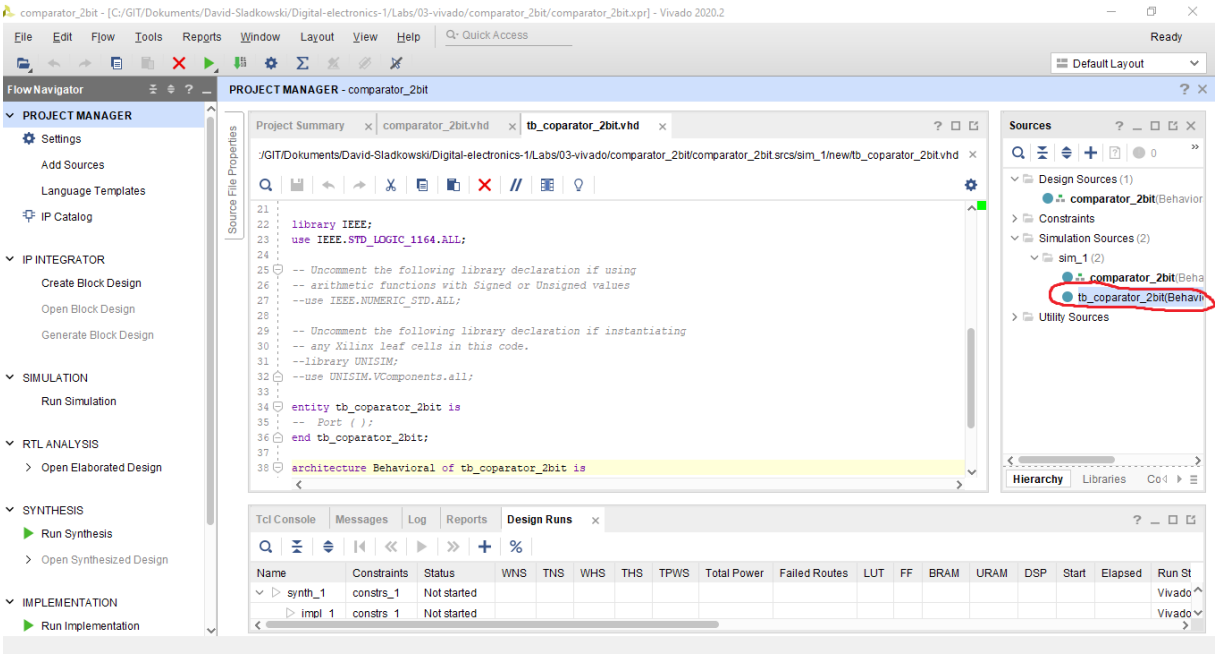

Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
tb_coparator_2bit
File location:
<Local to Project>
OK
Cancel
Scan and add RTL include files into pr
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel

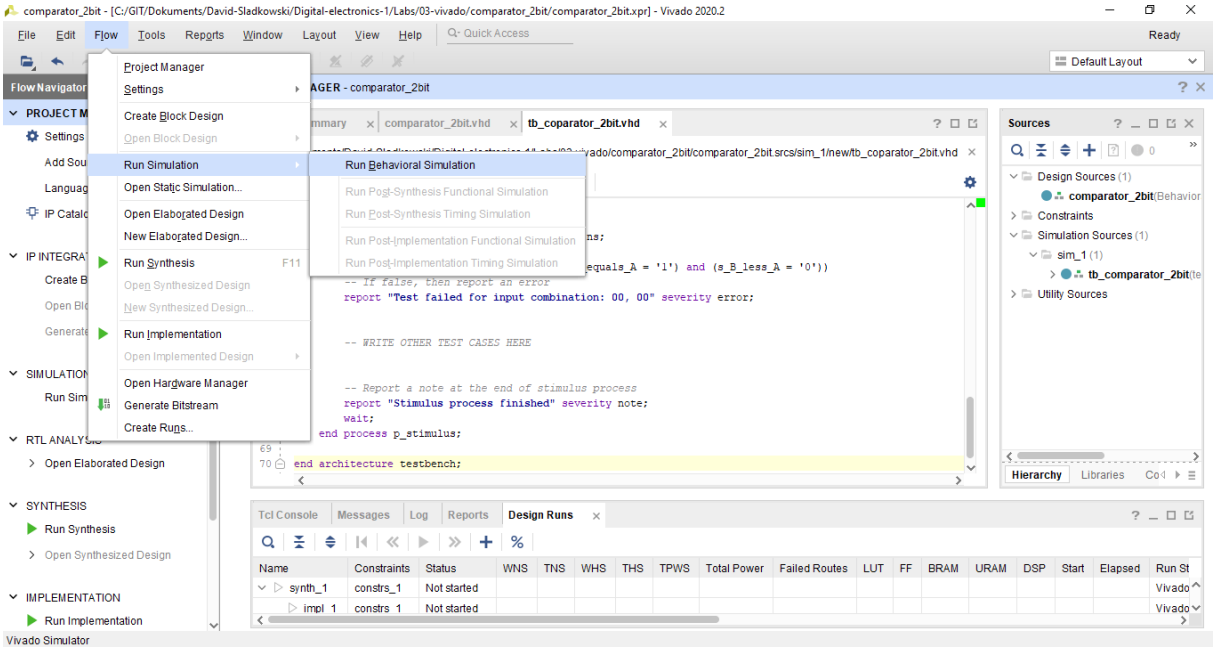

Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Index
Name
Library
Location
1
tb_coparator_2bit.vhd
xil_defaultlib
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name:
tb_coparator_2bit
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
OK
Cancel

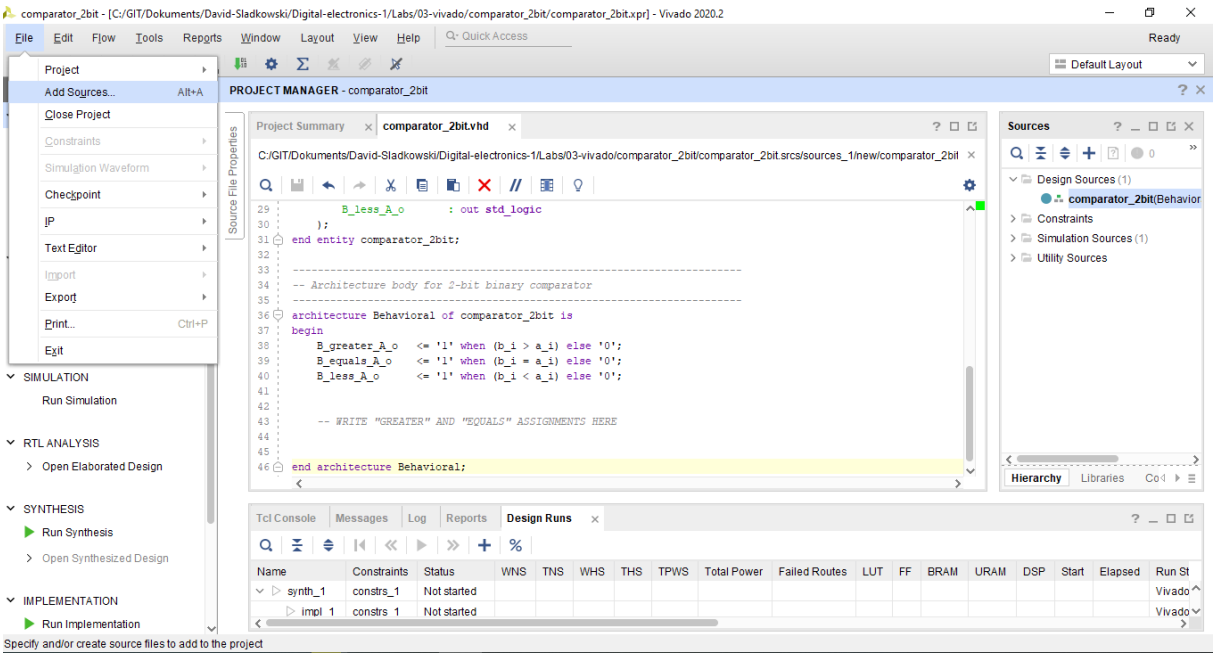

Define Module
The module definition has not been changed.
Are you sure you want to use these values?
Yes
No

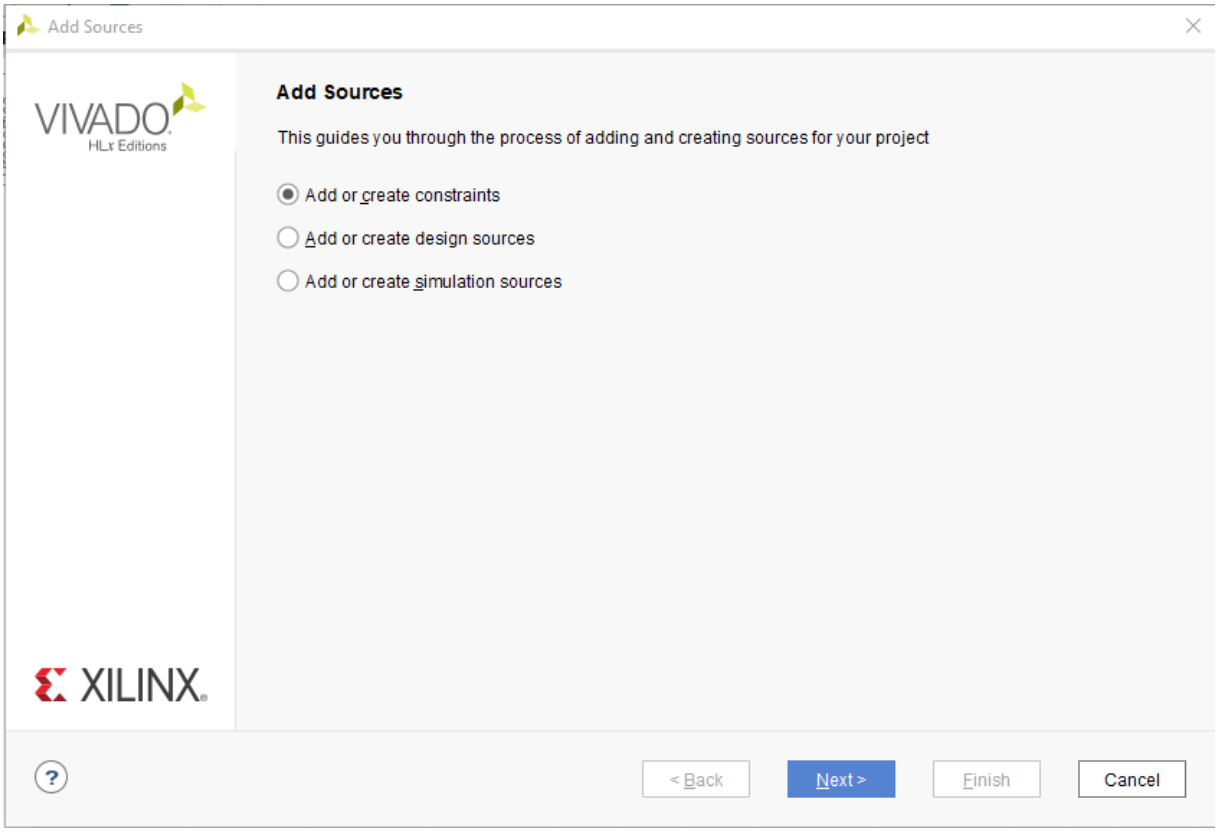


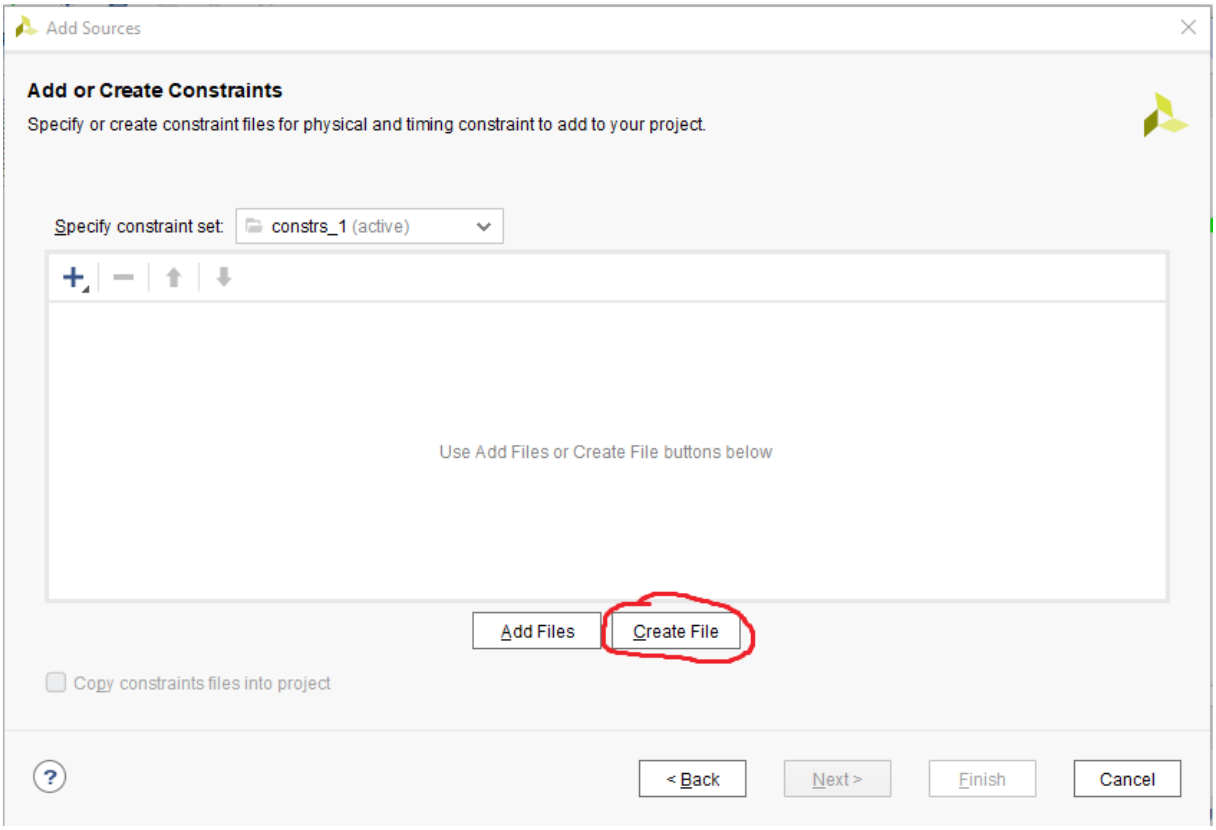
Spuštění simulace:

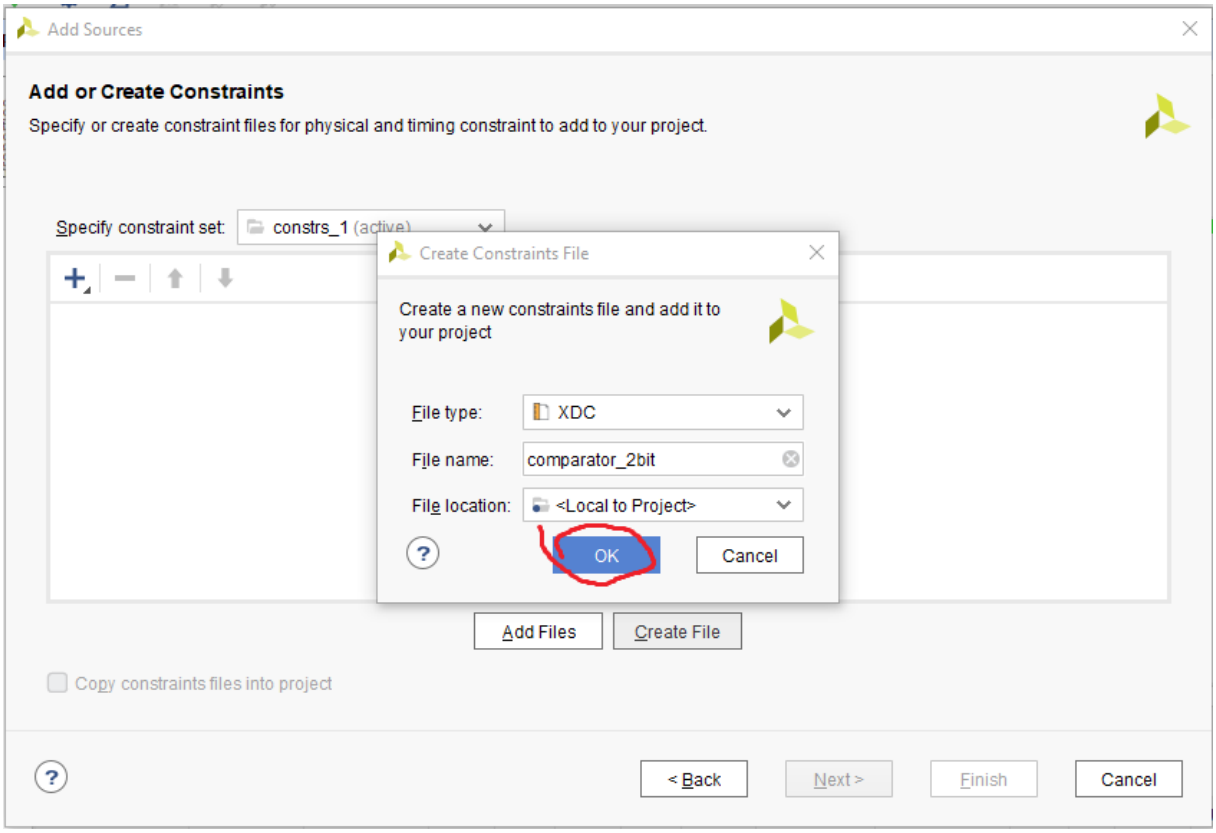


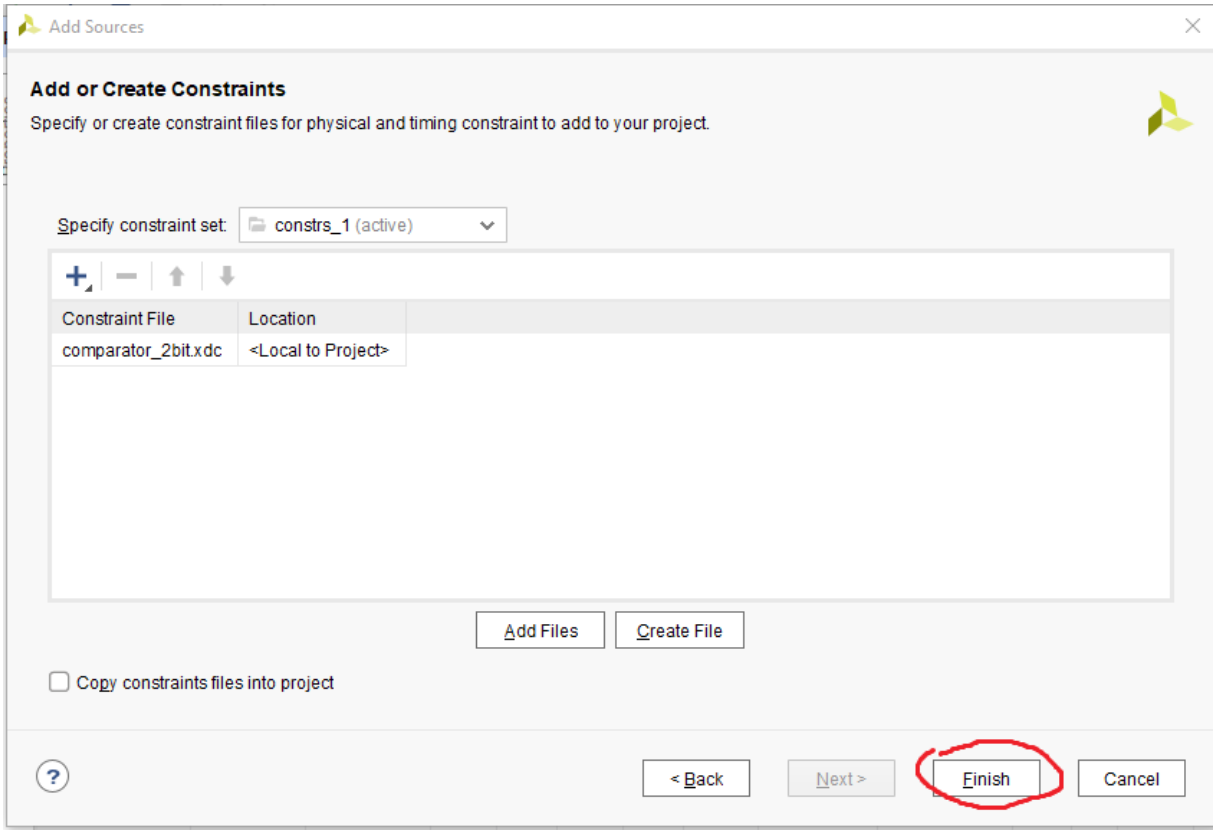
Přidání připojení soubor .XCD

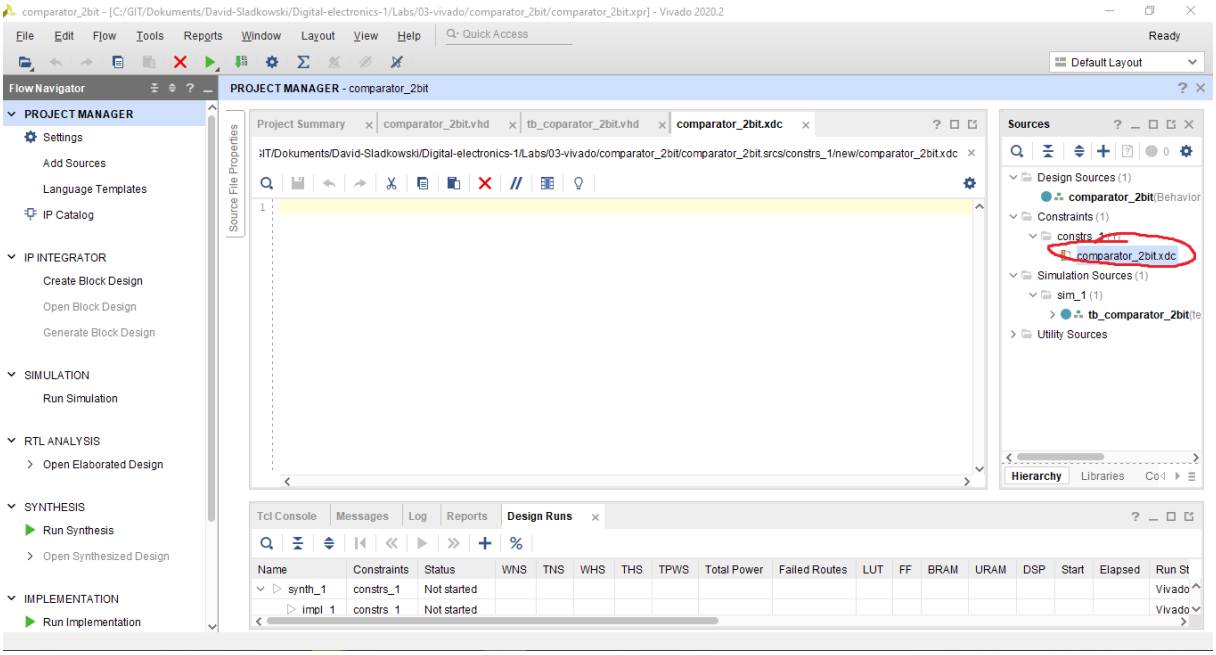





Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Create Constraints File
Create a new constraints file and add it to your project
File type:
XDC
File name:
comparator_2bit
File location:
<Local to Project>
OK
Cancel
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Constraint File
Location
comparator_2bit.xdc
<Local to Project>
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel


File Edit Flow Tools Reports Window Layout View Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
PROJECT MANAGER - comparator_2bit
Project Summary
comparator_2bit.vhd
tb_coparator_2bit.vhd
comparator_2bit.xdc
Sources
Design Sources (1)
Constraints (1)
comparator_2bit.xdc
Simulation Sources (1)
sim_1 (1)
Utility Sources
Hierarchy
Libraries
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started