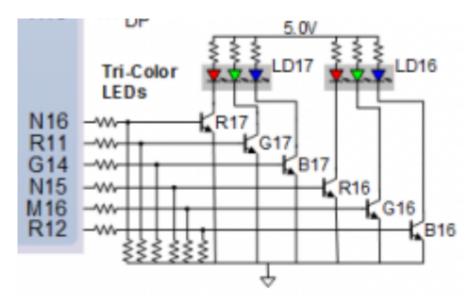


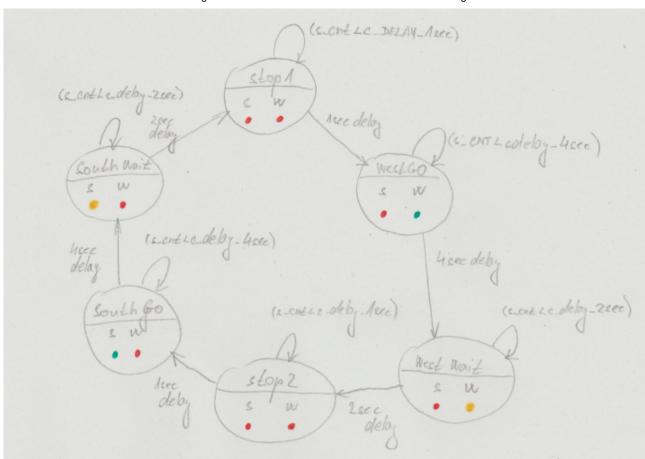
# b) Obrázek s připojením RGB LED na desce Nexys A7 a vyplněnou tabulkou s nastavením barev



RGB LED	Artix-7 pin names	Red	Yellow	Green
LD16	N15, M16, R12	1,0,0	1,1,0	0,1,0
LD17	N16, R11, G14	1,0,0	1,1,0	0,1,0

## 1) Ovladač semaforu

a) Stavový diagram



#### b) Výpis VHDL kódu sekvenčního procesu p\_traffic\_fsm

```
p_traffic_fsm : process(clk)
   begin
        if rising edge(clk) then
            if (reset = '1') then
                                       -- Synchronous reset
                s state <= STOP1;
                                       -- Set initial state
                       <= c_ZERO;
                                       -- Clear all bits
                s_cnt
            elsif (s_en = '1') then
                -- Every 250 ms, CASE checks the value of the s_state
                -- variable and changes to the next state according
                -- to the delay value.
                case s state is
                    -- If the current state is STOP1, then wait 1 sec
                    -- and move to the next GO_WAIT state.
                    when STOP1 =>
                        -- Count up to c DELAY 1SEC
                        if (s_cnt < c_DELAY_1SEC) then</pre>
                            s_cnt <= s_cnt + 1;</pre>
                        else
                            -- Move to the next state
                            s state <= WEST GO;
                            -- Reset local counter value
```

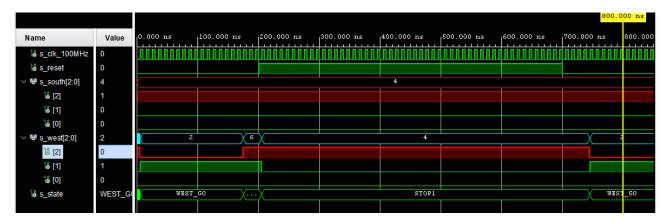
```
s cnt
                   <= c_ZERO;
      end if;
   when WEST GO =>
      -- Count up to c_DELAY_4SEC
      if (s cnt < c DELAY 4SEC) then</pre>
           s_cnt <= s_cnt + 1;</pre>
      else
           -- Move to the next state
           s_state <= WEST_WAIT;</pre>
           -- Reset local counter value
           s_cnt <= c_ZERO;</pre>
      end if;
  when WEST_WAIT =>
      -- Count up to c DELAY 2SEC
      if (s_cnt < c_DELAY_2SEC) then</pre>
           s_cnt \le s_cnt + 1;
      else
           -- Move to the next state
           s state <= STOP2;
           -- Reset local counter value
           s_cnt <= c_ZERO;</pre>
      end if;
 when STOP2 =>
      -- Count up to c_DELAY_1SEC
      if (s_cnt < c_DELAY_1SEC) then</pre>
           s cnt <= s cnt + 1;
      else
           -- Move to the next state
           s_state <= SOUTH_GO;</pre>
           -- Reset local counter value
           s_cnt <= c_ZERO;</pre>
      end if;
when SOUTH_GO =>
      -- Count up to c_DELAY_4SEC
      if (s_cnt < c_DELAY_4SEC) then</pre>
           s_cnt <= s_cnt + 1;
      else
           -- Move to the next state
           s_state <= SOUTH_WAIT;</pre>
           -- Reset local counter value
           s_cnt <= c_ZERO;</pre>
      end if;
when SOUTH WAIT =>
      -- Count up to c_DELAY_2SEC
      if (s_cnt < c_DELAY_2SEC) then</pre>
           s_cnt <= s_cnt + 1;
```

#### c) Výpis VHDL kódu kombinatorického procesu p\_output\_fsm

```
p_output_fsm : process(s_state)
    begin
        case s_state is
            when STOP1 =>
                south_o <= c_RED; -- RED (RGB = 100)
                west o <= c RED; -- RED (RGB = 100)
             when WEST_GO =>
                south o <= c RED; -- RED (RGB = 100)
                west_o <= c_GREEN; -- GREEN (RGB = 010)</pre>
            when WEST WAIT =>
                south_o <= c_RED; -- RED (RGB = 100)
                west_o <= c_YELLOW; -- YELLOW (RGB = 110)</pre>
            when STOP2 =>
                south o <= c RED; -- RED (RGB = 100)
                west_o <= c_RED; -- RED (RGB = 100)
            when SOUTH GO =>
                south_o <= c_GREEN; -- GREEN (RGB = 010)
                west_o <= c_RED; -- RED (RGB = 100)
            when SOUTH WAIT =>
                south_o <= c_YELLOW; -- YELLOW (RGB = 110)</pre>
                west_o <= c_RED; -- RED (RGB = 100)
            when others =>
                south_o <= c_RED; -- RED (RGB = 100)
west_o <= c_RED; -- RED (RGB = 100)
```

```
end case;
end process p_output_fsm;
```

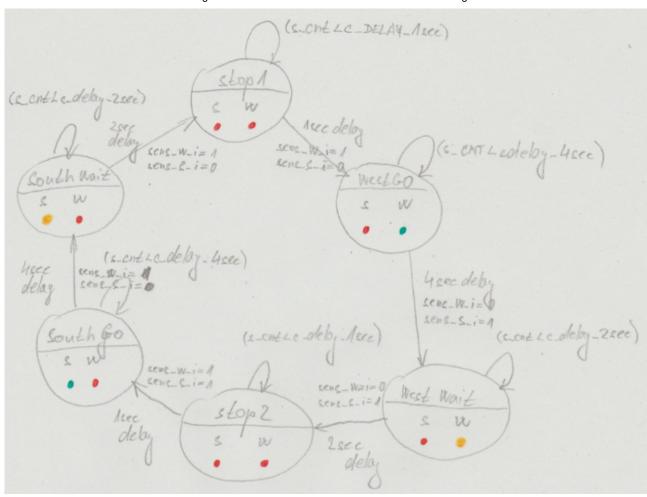
#### d) Screenshoty simulace



# 3) Inteligentní ovladač

a)

### b) Stavový diagram



#### c) Výpis VHDL kódu sekvenčního procesu p\_smart\_traffic\_fsm

```
p_smart_traffic_fsm : process(clk)
    begin
        if rising_edge(clk) then
            if (reset = '1') then
                                        -- Synchronous reset
                 s_state <= STOP1 ;
                                         -- Set initial state
                 s_cnt <= c_ZERO;
                                         -- Clear all bits
             elsif (s_en = '1') then
                  if ((sens_S_i = '0') \text{ and } (sens_W_i = '0')) then
                        s_state <= s_state;</pre>
                  elsif ((sens_S_i = '0') \text{ and } (sens_W_i = '1')) then
                       case s_state is
                              when SOUTH GO =>
                                  if (s_cnt < c_DELAY_4SEC) then</pre>
                                      s_cnt <= s_cnt + 1;</pre>
                                  else
```

```
s_state <= SOUTH_WAIT;</pre>
                        s_cnt <= c_ZERO;</pre>
                   end if;
              when SOUTH_WAIT =>
                   if (s_cnt < c_DELAY_2SEC) then</pre>
                        s_cnt <= s_cnt + 1;</pre>
                   else
                        s_state <= STOP1;</pre>
                        s_cnt <= c_ZERO;</pre>
                   end if;
              when STOP1 =>
                   if (s_cnt < c_DELAY_1SEC) then</pre>
                        s_cnt <= s_cnt + 1;
                   else
                        s_state <= WEST_GO;</pre>
                        s_cnt <= c_ZERO;</pre>
                   end if;
              when others =>
                   s_state <= WEST_GO;</pre>
      end case;
elsif ((sens_S_i = '1') \text{ and } (sens_W_i = '0')) \text{ then}
       case s_state is
           when WEST_GO =>
                   if (s_cnt < c_DELAY_4SEC) then</pre>
                        s_cnt <= s_cnt + 1;
                   else
                        s_state <= WEST_WAIT;</pre>
                        s_cnt <= c_ZERO;</pre>
                   end if;
           when WEST WAIT =>
                   if (s_cnt < c_DELAY_2SEC) then</pre>
                        s_cnt <= s_cnt + 1;</pre>
                   else
                        s_state <= STOP2;</pre>
                        s cnt <= c ZERO;
                   end if;
           when STOP2 =>
                   if (s_cnt < c_DELAY_1SEC) then</pre>
                        s_cnt <= s_cnt + 1;</pre>
```

```
else
                      s_state <= SOUTH_GO;</pre>
                      s_cnt <= c_ZERO;</pre>
                 end if;
          when others =>
                 s_state <= SOUTH_GO;</pre>
     end case;
elsif ((sens_S_i = '1') and (sens_W_i = '1')) then
   case s_state is
        when STOP1 =>
            if (s_cnt < c_DELAY_1SEC) then</pre>
                 s_cnt <= s_cnt + 1;</pre>
             else
                 s_state <= WEST_GO;</pre>
                 s_cnt <= c_ZERO;</pre>
             end if;
        when WEST GO =>
            if (s_cnt < c_DELAY_4SEC) then</pre>
                 s_cnt <= s_cnt + 1;</pre>
             else
                 s_state <= WEST_WAIT;</pre>
                  s cnt <= c ZERO;
             end if;
        when WEST_WAIT =>
            if (s_cnt < c_DELAY_2SEC) then</pre>
                 s_cnt <= s_cnt + 1;
             else
                 s_state <= STOP2;</pre>
                 s_cnt <= c_ZERO;</pre>
             end if;
       when STOP2 =>
             if (s_cnt < c_DELAY_1SEC) then</pre>
                 s_cnt <= s_cnt + 1;</pre>
             else
                 s_state <= SOUTH_GO;</pre>
                 s_cnt <= c_ZERO;</pre>
             end if;
     when SOUTH_GO =>
            if (s_cnt < c_DELAY_4SEC) then</pre>
```

```
s_cnt <= s_cnt + 1;</pre>
                           else
                               s_state <= SOUTH_WAIT;</pre>
                               s_cnt <= c_ZERO;</pre>
                           end if;
                    when SOUTH_WAIT =>
                           if (s_cnt < c_DELAY_2SEC) then</pre>
                               s_cnt <= s_cnt + 1;</pre>
                           else
                               s_state <= STOP1;</pre>
                               s_cnt <= c_ZERO;</pre>
                           end if;
                      -- It is a good programming practice to use the
                      -- OTHERS clause, even if all CASE choices have
                      -- been made.
                      when others =>
                           s_state <= STOP1;</pre>
             end case;
             end if;
         end if; -- Synchronous reset
    end if; -- Rising edge
end process p_smart_traffic_fsm;
```