David Elliott

Evan Yeh

EE125 Homework #2

Problem 1: Multiple Detector

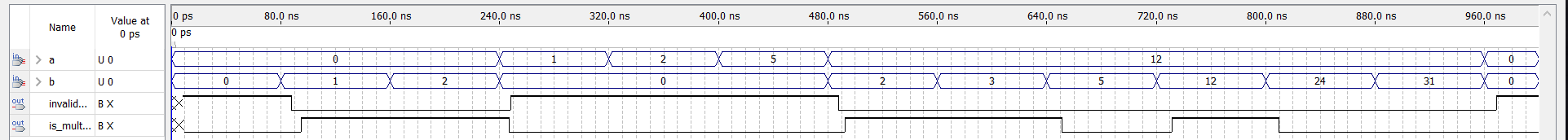
VHDL Code:



Simulation Results:

Tests edge cases:

* 0 is a multiple of all numbers (except 0)
* No number can be a multiple of 0
* a > b
* a < b



Problem 2: Absolute difference calculator

VHDL Code:

absolute\_difference.vhd



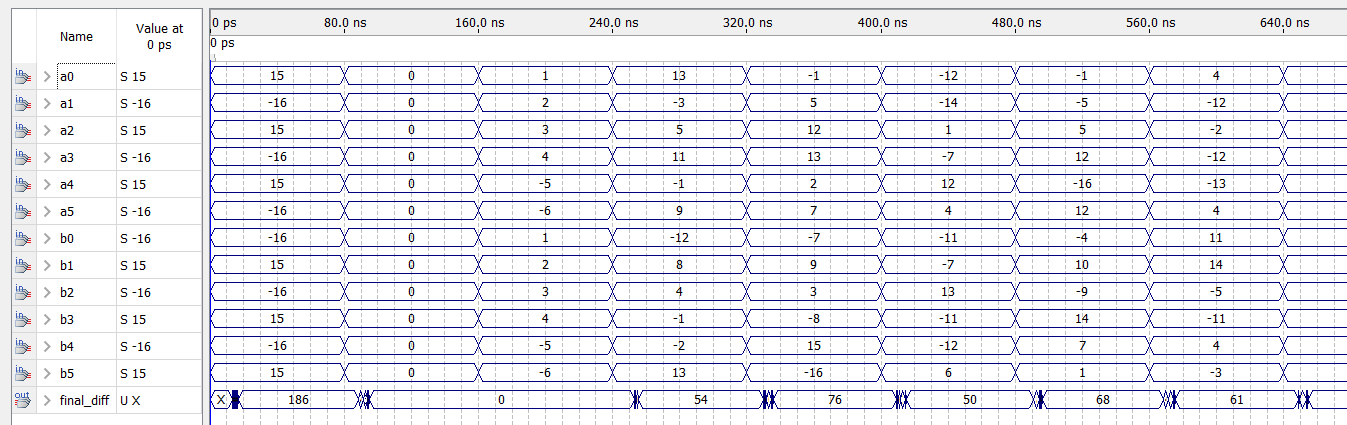
user\_types.vhd



Simulation Results:

Cases:

* maximum absolute difference
* zero input and zero absolute difference
* zero absolute difference
* random test cases



Problem 3: Leading-ones counter

VHDL Code:

Simulation Results:

