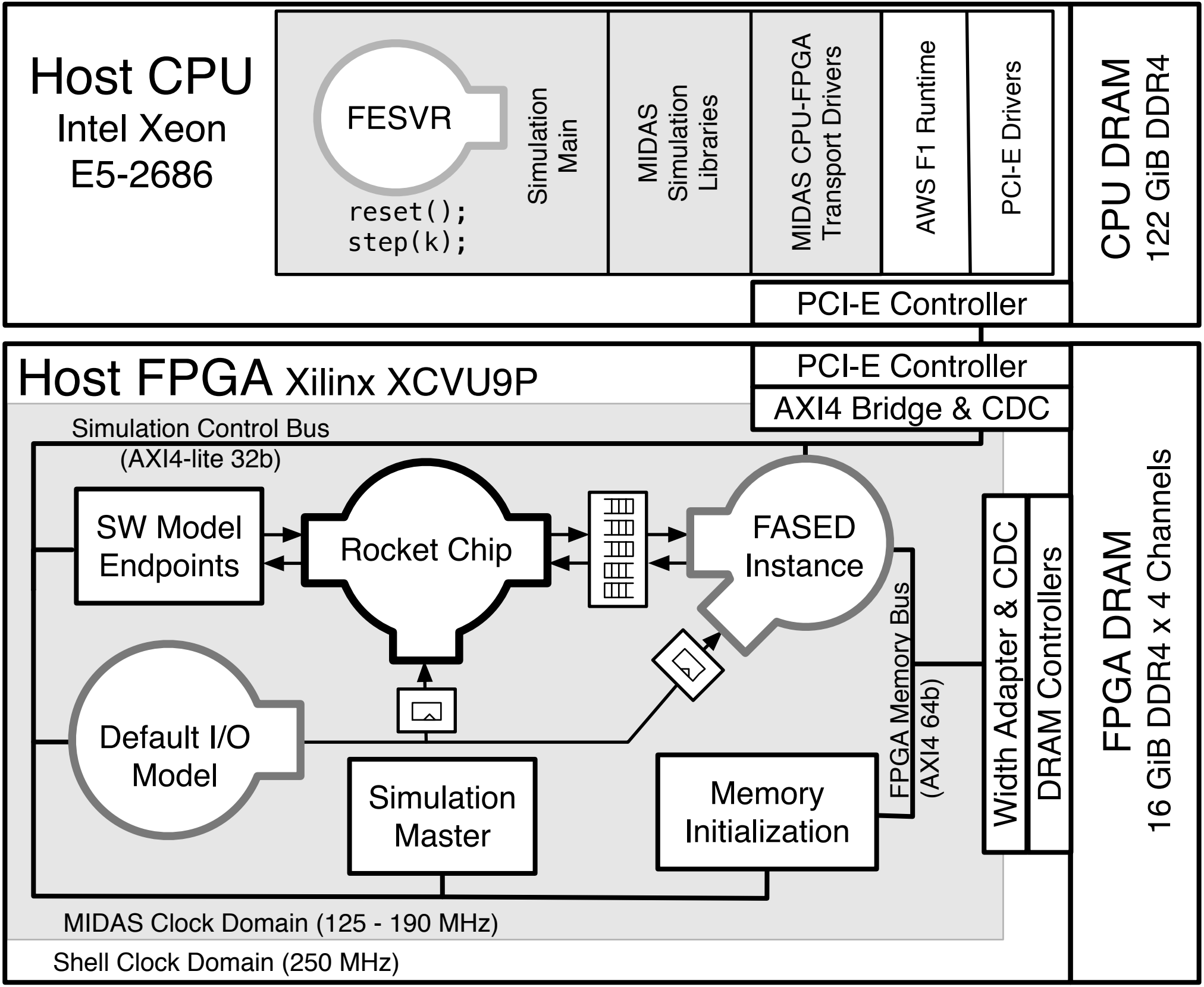
Host CPU
Intel Xeon
E5-2686
FESVR
reset();
step(k);
Simulation Main
MIDAS Simulation Libraries
MIDAS CPU-FPGA Transport Drivers
AWS F1 Runtime
PCI-E Drivers
CPU DRAM
122 GiB DDR4
PCI-E Controller
Host FPGA Xilinx XCVU9P
PCI-E Controller
AXI4 Bridge & CDC
Simulation Control Bus
(AXI4-lite 32b)
SW Model Endpoints
Rocket Chip
FASED Instance
Default I/O Model
Simulation Master
Memory Initialization
FPGA Memory Bus
(AXI4 64b)
Width Adapter & CDC
DRAM Controllers
FPGA DRAM
16 GiB DDR4 x 4 Channels
MIDAS Clock Domain (125 - 190 MHz)
Shell Clock Domain (250 MHz)