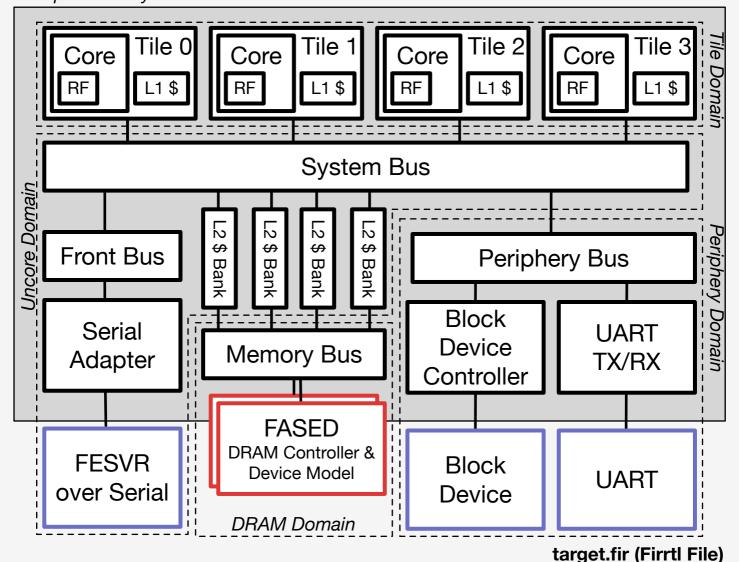
Chip Boundary



```
Optimization Annotations
RAMOptAnnotation(tile0.core.rf),
RAMOptAnnotation(tile1.core.rf),
RAMOptAnnotation(tile2.core.rf),
RAMOptAnnotation(tile3.core.rf),
MultithreadingAnnotation(tile0),
MultithreadingAnnotation(tile0),
MultithreadingAnnotation(tile0),
MultithreadingAnnotation(tile0),
MultithreadingAnnotation(tile0),
Channel Annotations
<Label Bridge Interfaces>
```

```
BridgeAnnotation(
   target = blockdev,
   bridgeClass = BlockDeviceBridge),

BridgeAnnotation(
   target = uart,
   bridgeClass = UARTBridge),

BridgeAnnotation(
   target = serial,
   bridgeClass = SerialBridge),

BridgeAnnotation(
   target = fased0,
   bridgeClass = FASEDMemoryTimingModel),
```

**Bridge Annotations** 

target.anno.json (Annotations File)