PROJECT SCHEDULE TEMPLATE

Logic Circuit Interactive Sim **Manager - David C.**

PROJECT DELIVERABLE

SCOPE STATEMENT

START DATE	END DATE	OVERALL PROGRESS
10/1/2025	12/5/2025	0%

TASK NAME	ASSIGNED TO	DONE BY	STATUS	COMMENTS
Iteration 3 submission	ALL	5-Nov	In progress	requirements on Canvas
Team meeting	ALL	4-Nov	Completed	will work on next steps of project together (meeting ~2pm in Snell)
Additional Info for Logic Gates	Bethany	9-Nov	In progress	
Add logic to sprites	Kyra	9-Nov	In progress	have AND/OR/NAND/etc have 2/3/4 inputs
First draft of GUI, Loading sprites	David	9-Nov	In progress	
WK 6 - Basic program funtions, see tasks	ALL	16-Nov		
research saving methods and handling invalid circuit designs	TBD	11-Nov	Not Started	users can store circuit designs as a JSON or XML file, and Create error messages for invalid circuit designs
Add more advanced gates				suggested: T/D/JK Flip-Flop, S/R Latch, D-Latch
Final Report	ALL	5-Dec	Not Started	