EG21-G

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
1.0	2019-11-19	Lorry XU/ Ethan SHAN	Initial
1.1	2020-04-10	Ward WANG/ Ethan SHAN	1. Updated current consumption and GNSS current consumption (Table 33 and 34). 2. Updated notes (Chapter 6.5). 3. Added the note about the standard that the package warpage level of the module conforms to (Chapter 7.1). 4. Updated module storage information (Chapter 8.1). 5. Updated module manufacturing and soldering information (Chapter 8.2).
1.2	2020-09-21	Ethan SHAN/ Fanny CHEN	1. Updated the description of module form factor (Table 2, Chapter 2.1 and 7.3). 2. Updated the AT command for the operation of ANT_MAIN and ANT_DIV (Chapter 5.1.3). 3. Updated the recommended compatible footprint and the note 3 about the stencil selection when using LCC form factor (Chapter 7.3). 4. Updated the cooling down slope of reflow soldering thermal profile (Chapter 8.2). 5. Updated the module storage information (Chapter 8.1).
1.3	2024-03-19	Soley ZHANG/ Kai YU	1. Added the modulations of LTE features (Table 3). 2. Updated the information on USB serial drivers (Table 3). 3. Added a note on avoiding abnormal RF functions caused by current sink on the module's pins (Chapter 3.2). 4. Updated the power supply limits during burst

	transmission (Figure 8). 5. Updated the capacitance value of C4 in star structure of the power supply (Figure 9). 6. Updated the power-up timing of the module (Figure 13). 7. Added the information on (U)SIM2 interface configured by software (Chapter 3.10). 8. Updated the RF receiving sensitivity (Table 28). 9. Updated the GNSS performance (Table 31). 10. Updated the reference circuit of GNSS antenna (Figure 34). 11. Updated the RF routing guidelines (Chapter 4.3). 12. Updated the power consumption (Table 36). 13. Updated the electrostatic discharge characteristics (Table 38). 14. Added a note on ESD protection (Chapter 7.1). 15. Updated the information on manufacturing and soldering (Chapter 7.2). 16. Updated the packaging specifications (Chapter 7.3).

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1 Introduction

This document defines EG21-G module, and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details as well as other related information of EG21-G module. To facilitate its application in different fields, relevant reference design is also provided for your reference. Associated with application note and user guide, you can use EG21-G module to design and set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

2.1. Frequency Bands and Functions

EG21-G is an LTE/WCDMA/GSM wireless communication module with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, UMTS, EDGE and GPRS networks. It also provides GNSS and voice functionality for your specific applications. The following table shows the supported frequency bands, GNSS and digital audio functions of EG21-G module.

Table 2: Frequency Bands and Functions

Technology	EG21-G
LTE-FDD (with receive diversity)	B1/B2/B3/B4/B5/B7/B8/B12/B13/B18/B19/B20/B25/B26/B28
LTE-TDD (with receive diversity)	B38/B39/B40/B41
WCDMA (with receive diversity)	B1/B2/B4/B5/B6/B8/B19
GSM	GSM850/EGSM900/DCS1800/PCS1900
GNSS (Optional)	GPS, GLONASS, BDS, Galileo, QZSS
Digital Audio (PCM)	Supported

2.2. Key Features

The following table describes the detailed features of EG21-G module.

Table 3: Key Features

Feature	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850 8-PSK ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK ● Class 3 (23 dBm ±2 dB) for WCDMA bands ● Class 3 (23 dBm ±2 dB) for LTE bands
LTE Features	● Support up to non-CA Cat 1 FDD and TDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Modulations: – DL: QPSK, 16QAM and 64QAM – UL: QPSK, 16QAM ● LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL) ● LTE-TDD: Max. 8.96 Mbps (DL), Max. 3.1 Mbps (UL)
UMTS Features	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Support QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL), Max. 384 kbps (UL)
GSM Features	**GPRS:** ● Support GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. 107 kbps (DL), Max. 85.6 kbps (UL) **EDGE:** ● Support EDGE multi-slot class 33 (33 by default) ● Modulations: GMSK and 8-PSK ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 296 kbps (DL), Max. 236.8 kbps (UL)

Internet Protocol Features	● Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/ SMTP/SSL/MQTT/CMUX/SMTPS/FILE/MMS [1] protocols ● Support PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Support (U)SIM card: 1.8 V, 3.0 V
Audio Features	● Support one digital audio interface: PCM interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
PCM Interface	● Used for audio function with external codec ● Support 16-bit linear data format ● Support long frame synchronization and short frame synchronization ● Support master and slave modes, but must be the master in long frame synchronization
USB Interface	● Compliant with USB 2.0 specification (slave only) ● Data transmission rate: up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB ● Support USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–6.7, Android 4.x–13.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: up to 921600 bps, 115200 bps by default ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● Baud rate: 115200 bps
SD Card Interface	Support SD 3.0 protocol
SGMII Interface	● Support 10/100/1000 Mbps Ethernet work mode ● Support max.10 Mbps (DL)/max. 5 Mbps (UL) for 4G network
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS (Optional)	● Protocol: NMEA 0183 ● Data update rate: 1 Hz by default
AT Commands	● Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* ● Quectel enhanced AT commands

[1] The module only supports MMS sending.

Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Size: (29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm ● Package: LGA ● Weight: approx. 4.9 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [2] ● Extended temperature range: -40 °C to +85 °C [3] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

[2] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[3] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module retains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency
- Peripheral interfaces

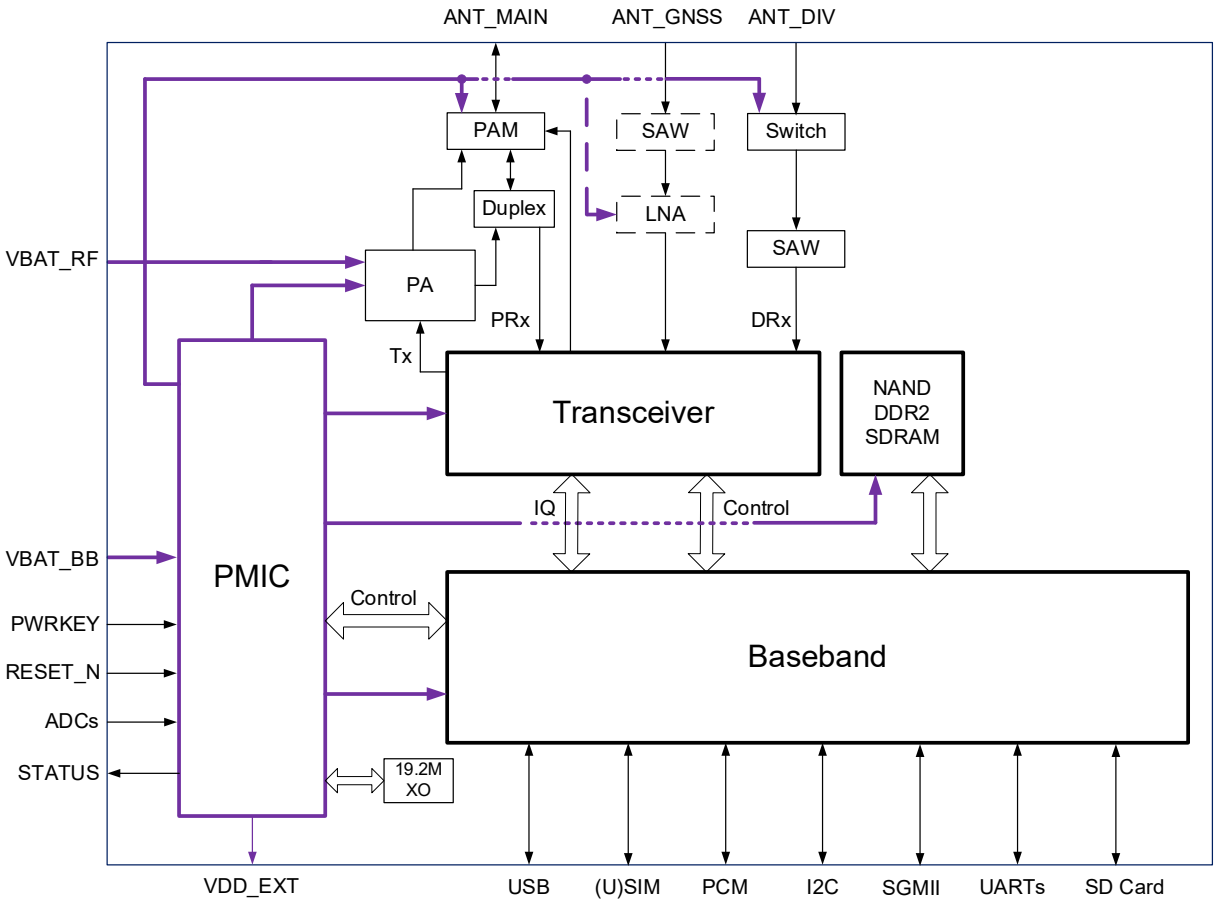


Figure 1: Functional Diagram

2.4. EVB Kit

Quectel supplies an evaluation board (UMTS & LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The module is equipped with 144 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following functions/interfaces.

- Power supply pins
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- ADC interfaces
- SGMII interface
- Indication signals
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

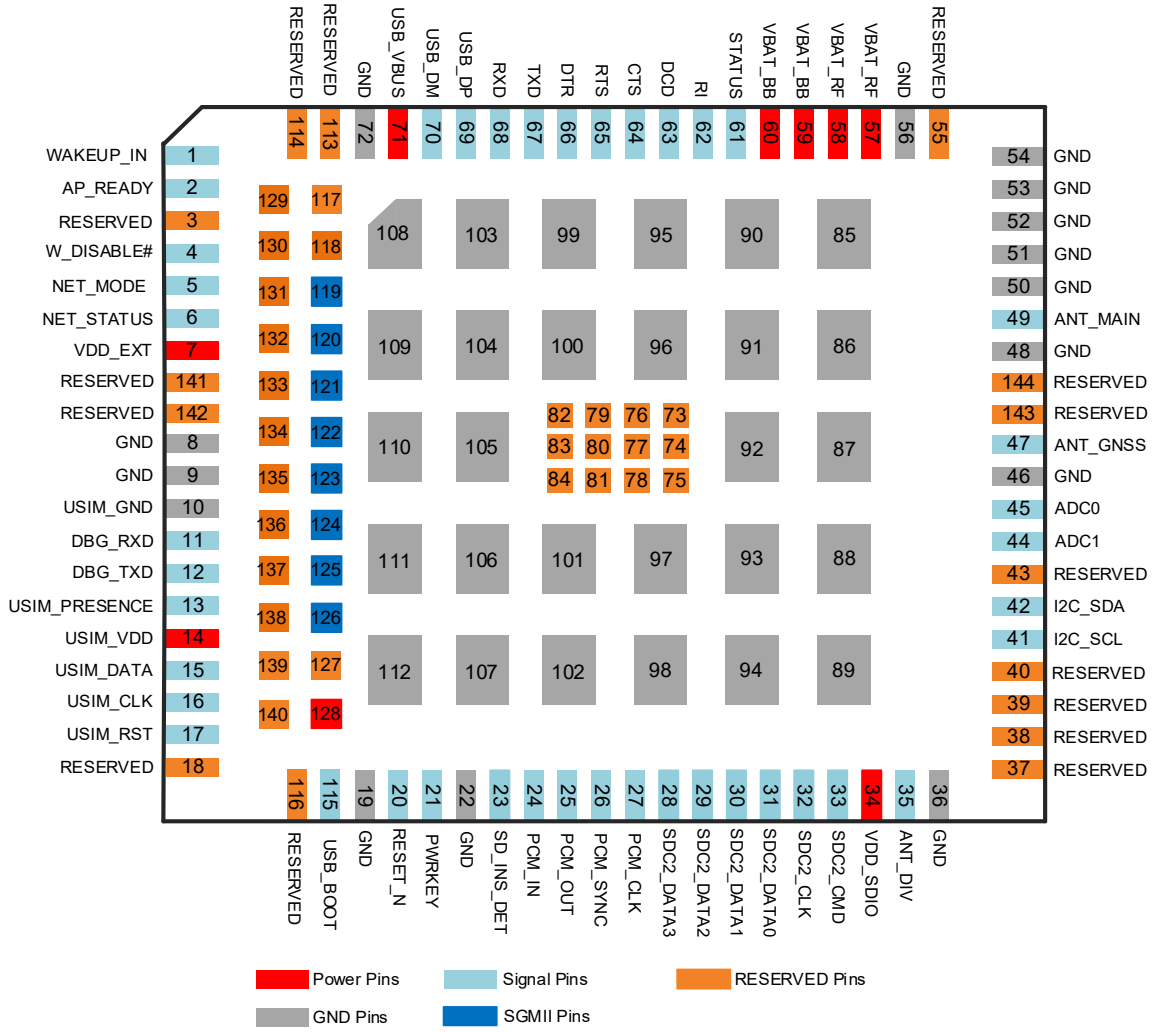


Figure 2: Pin Assignment (Top View)

NOTE

1. BOOT_CONFIG property pins (WAKEUP_IN, NET_MODE and USB_BOOT) cannot be pulled up before startup.
2. PWRKEY output voltage is 0.8 V because of the diode drop in the chipset.
3. Keep all RESERVED pins and unused pins unconnected.
4. GND pins (pins 85–112) should be connected to ground in the design. RESERVED pins (pins 73–84) should not be designed in schematic and PCB decal, and these pins should be served as a keepout area.

5. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.

3.3. Pin Description

The following tables show the pin definition of the module.

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part		It must be provided with sufficient current

					up to 1.8 A in a burst transmission.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the chipset.
RESET_N	20	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	1.8 V power domain. If unused, keep it open.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module's operating status		The drive current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.
NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status		1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	If unused, keep it open.

USB_DP	69	AIO	USB 2.0 differential data (+)		Require differential impedance of 90 Ω. If unused, keep these pins open.
USB_DM	70	AIO	USB 2.0 differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10	-	Specified ground for (U)SIM card		
USIM_VDD	14	PO	(U)SIM card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
USIM_RST	17	DO	(U)SIM card reset	**For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_ PRESENCE	13	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Main UART Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	62	DO	Ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DCD	63	DO	Data carrier detect		
CTS	64	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to the MCU's CTS. 1.8 V power domain. If unused, keep it open.
RTS	65	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep it open.
DTR	66	DI	Data terminal ready, sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. DTR at low level can wake up the module. If unused, keep it open.
TXD	67	DO	Transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep these pins open.
RXD	68	DI	Receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General-purpose ADC interface	Voltage range: 0.3 V to VBAT_BB	If unused, keep these pins open.

ADC1	44	AI	General-purpose ADC interface		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
PCM_OUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	26	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Master mode: output. Slave mode: input. If unused, keep these pins open.
PCM_CLK	27	DIO	PCM clock		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock (for external codec)		Require external pull-up to 1.8 V. If unused, keep these pins open.
I2C_SDA	42	OD	I2C serial data (for external codec)		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_DATA3	28	DIO	SD card data bit 3	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V	SDIO signal level can be selected according to SD card supported level. See SD 3.0 protocol for more details. If unused, keep these pins open.
SDC2_DATA2	29	DIO	SD card data bit 2		
SDC2_DATA1	30	DIO	SD card data bit 1		
SDC2_DATA0	31	DIO	SD card data bit 0		

				V_{IH}max = 3.34 V	
SDC2_CLK	32	DO	SD card clock	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V	
SDC2_CMD	33	DIO	SD card command	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	
SD_INS_DET	23	DI	SD card insertion detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. This pin must be connected if SD card is used, and keep it open if SD card is unused.
VDD_SDIO	34	PO	1.8/2.85 V output power for SD card pull-up circuits	$I_O$max = 50 mA	1.8/2.85 V configurable. Cannot be used for SD card power. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EPHY_RST_N	119	DO	SGMII reset external PHY	**For 1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V	1.8/2.85 V power domain. If unused, keep it open.

				For 2.85 V: V_{OL}max = 0.35 V V_{OH}min = 2.14 V	
EPHY_INT_N	120	DI	SGMII interrupt	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SGMII_MDATA	121	DIO	SGMII management data input/output	**For 1.8 V:** V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **For 2.85 V:** V_{IL}max = 0.71 V V_{IH}min = 1.78 V V_{OL}max = 0.35 V V_{OH}min = 2.14 V	1.8/2.85 V power domain. Requires external pull-up to USIM2_VDD, and the resistor should be 1.5 kΩ. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII management data clock	**For 1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **For 2.85 V:** V_{OL}max = 0.35 V V_{OH}min = 2.14 V	1.8/2.85 V power domain. If unused, keep it open.
SGMII_TX_M	123	AO	SGMII transmit (-)		Add a 0.1 μF capacitor close to the PHY chip. If unused, keep these pins open.
SGMII_TX_P	124	AO	SGMII transmit (+)		
SGMII_RX_P	125	AI	SGMII receive (+)		Add a 0.1 μF capacitor close to the module. If unused, keep these pins open.
SGMII_RX_M	126	AI	SGMII receive (-)		
USIM2_VDD	128	PO	SGMII MDIO pull-up power supply		Configurable power source. 1.8/2.85 V power domain. If unused, keep it open.
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ANT_DIV	35	AI	Diversity antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. This pin at low level can wake up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. This pin at low level can make the module enter airplane mode. If unused, keep it open.
AP_READY	2	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USB_BOOT	115	DI	Force the module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	Active high. 1.8 V power domain. If the forced download mode is not used, the pin cannot be pulled up before startup. It is recommended to reserve a test point.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**

RESERVED	3, 18, 37–40, 43, 55, 73–84, 113, 114, 116–118, 127, 129–144	Keep these pins unconnected.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
	Voice/Data	The module is connected to network. Its power consumption varies with the network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function is invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from the network normally. In this mode, the power consumption is reduced to an ultra-low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

See ***document [2]*** for more details about **AT+CFUN**.

3.5. Power Saving

3.5.1. Sleep Mode

In sleep mode, the module reduces power consumption to an ultra-low level.

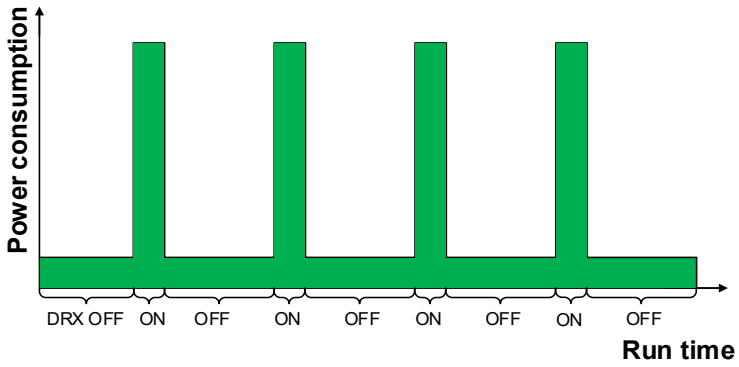


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.5.1.1. UART Application

If the MCU communicates with the module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode. For more details, see ***document [2]***.
- Drive DTR to high level.

The following figure shows the connection between the module and the MCU.

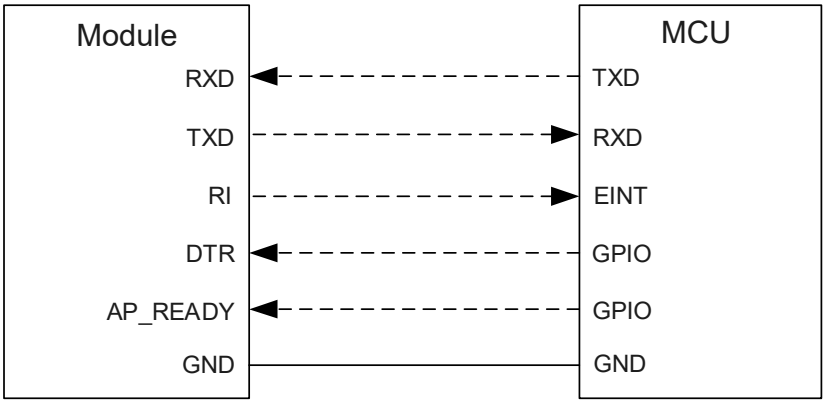


Figure 4: Sleep Mode Application via UART

- Driving the MCU's DTR to low level will wake up the module.
- When the module has a URC to report, RI signal will wake up the MCU. See ***Chapter 3.17.3*** for details about RI behaviors.
- AP_READY will detect the sleep state of the MCU (can be configured to high level or low level detection). See ***document [3]*** for details about **AT+QCFG="apready"**.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

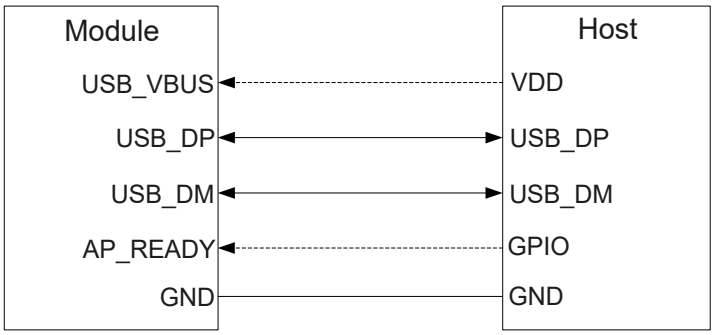


Figure 5: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals via USB bus to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB Suspend and Resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

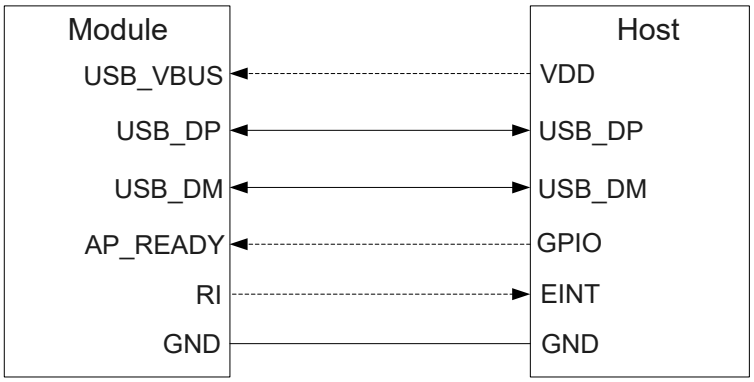


Figure 6: Sleep Mode Application with RI

- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application Without USB Suspend Function

If the host does not support USB Suspend function, USB_VBUS should be disconnected with an external control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

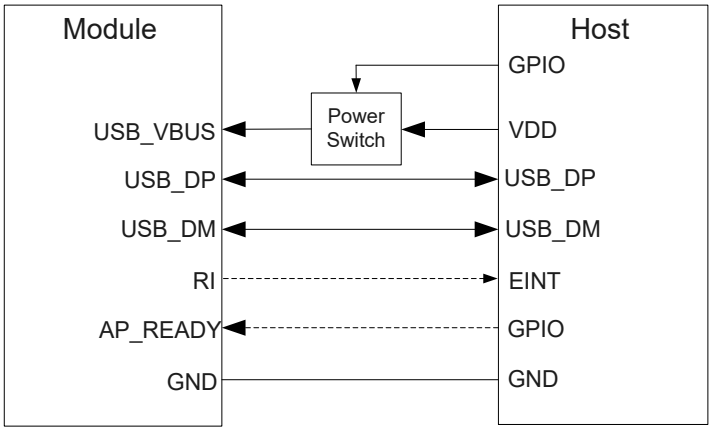


Figure 7: Sleep Mode Application Without Suspend Function

Restoring the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the host.
2. For more details about the module power management application, see ***document [4]***.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter airplane mode.

Software:

AT+CFUN provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4. See ***document [2]*** for more details.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**. See ***document [3]*** for more details.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's BB part

The following table shows the details of VBAT pins and ground pins.

Table 7: Pin Definition of VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's BB part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112					

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

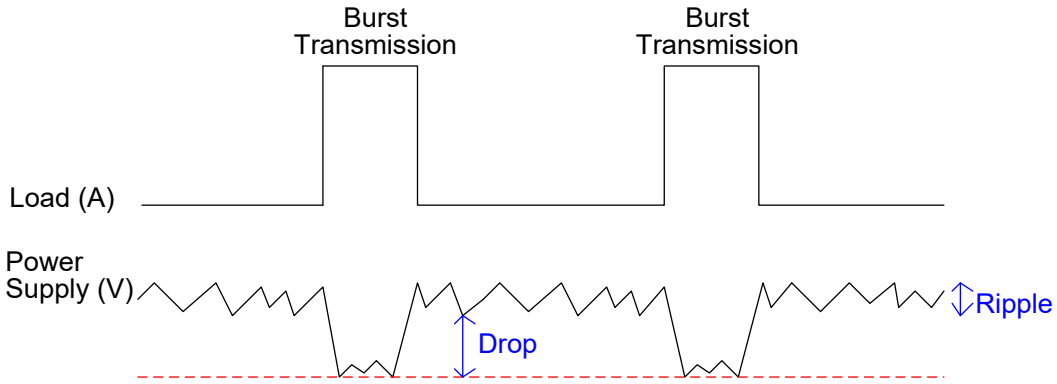


Figure 8: Power Supply Limits During Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, and 100 pF for VBAT_BB, while 100 nF, 33 pF, and 10 pF for VBAT_RF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be at least 1 mm; and the width of VBAT_RF trace should be at least 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to avoid the damage caused by electric surge and electrostatics discharge (ESD), it is suggested that a TVS diode with suggested low reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

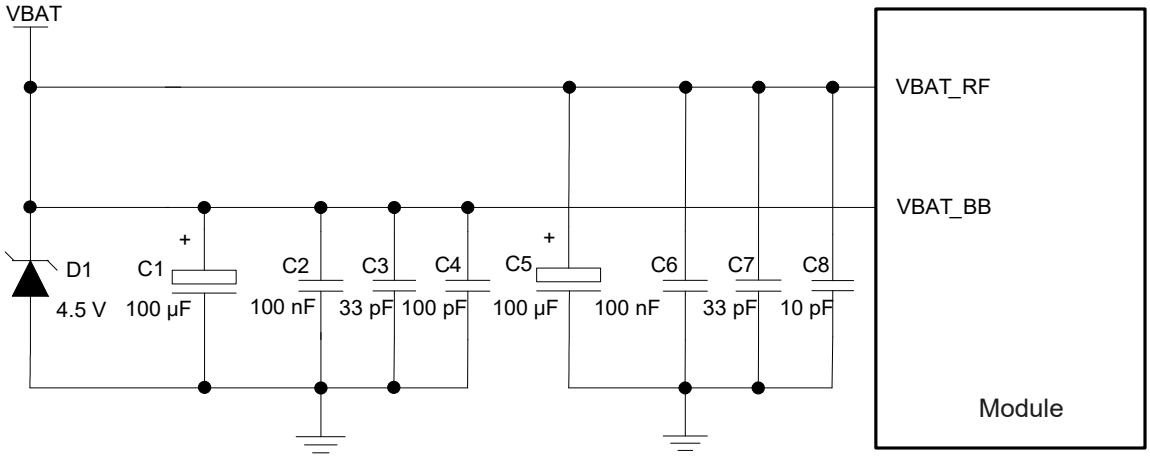


Figure 9: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5.0 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

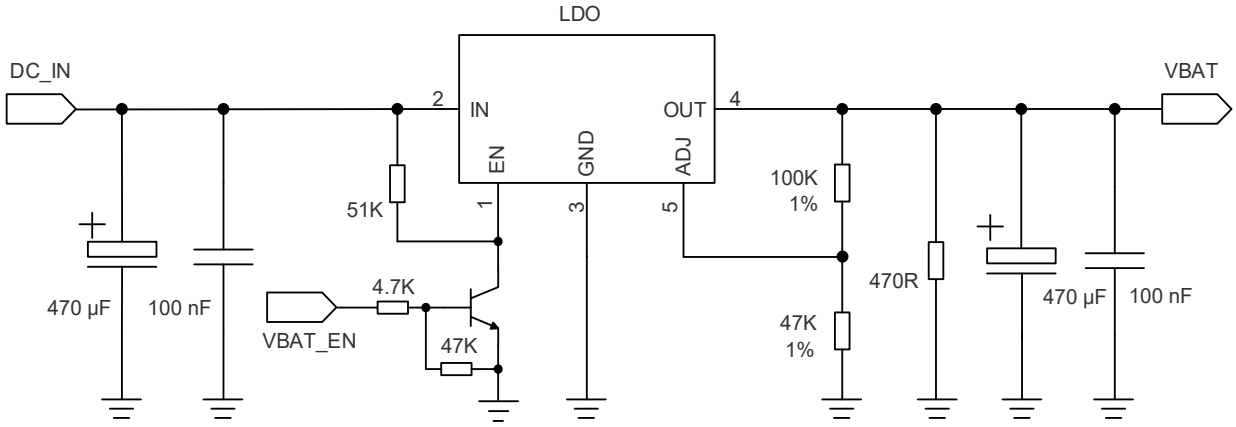


Figure 10: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

3.6.4. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.7. Turn On

3.7.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the chipset.

When the module is in power-down mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY, and release PWRKEY pin after STATUS pin (which requires an external pull-up resistor) outputs a low level. The STATUS pin is used as an indicator to show that the module has turned on normally. A simple reference circuit is illustrated in the following figure.

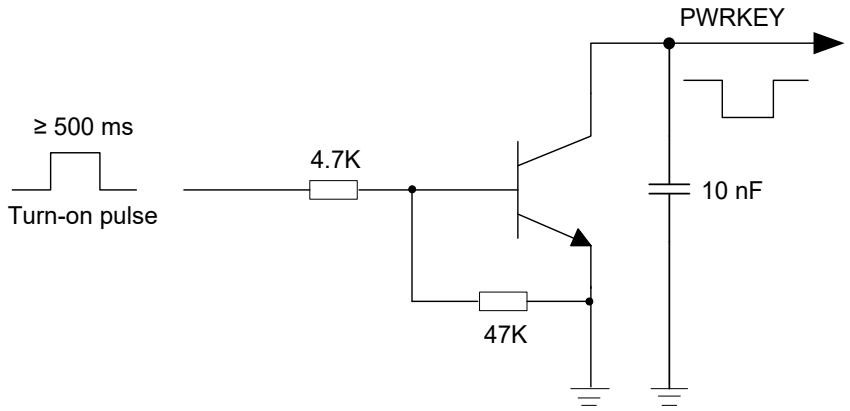


Figure 11: Turn On the Module by Using Driving Circuit

The other way to control the PWRKEY is to use a button. When pressing the button, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

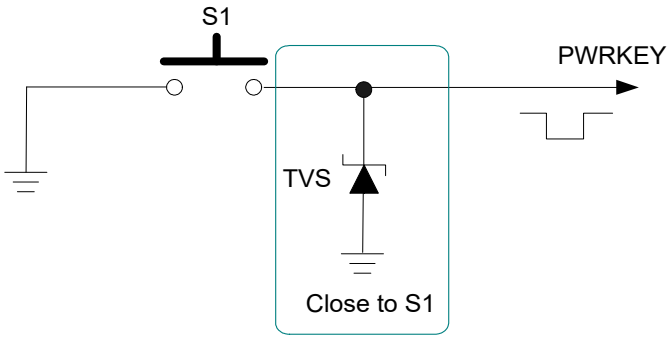


Figure 12: Turn On the Module by Using a Button

The power-up timing is illustrated in the following figure.

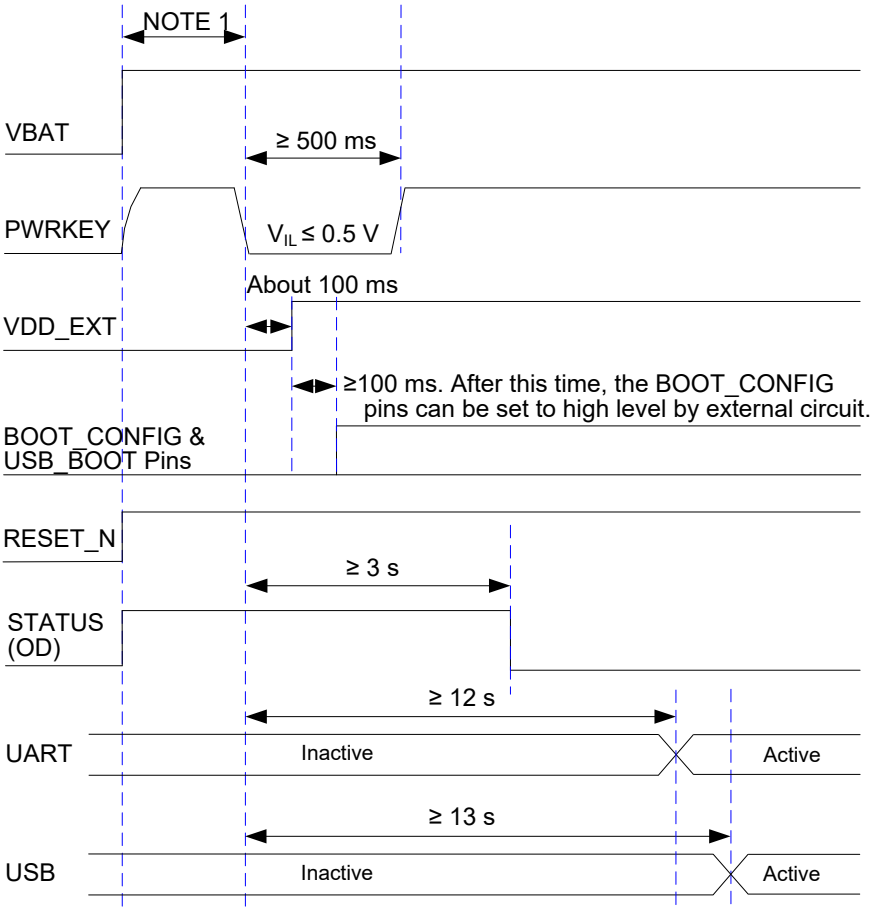


Figure 13: Power-up Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if module needs to be turned on automatically and shutdown is not needed.

3.8. Turn Off

The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD**.

3.8.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 650 ms, the module will execute power-down procedure after the PWRKEY is released. The power-down timing is illustrated in the following figure.

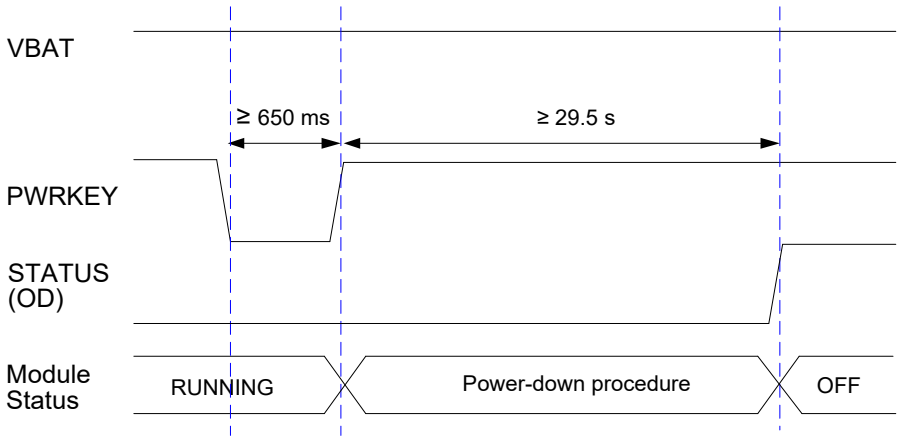


Figure 14: Power-down Timing

3.8.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via PWRKEY pin.

See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after successfully turn-off.

3.9. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N low for 150–460 ms.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

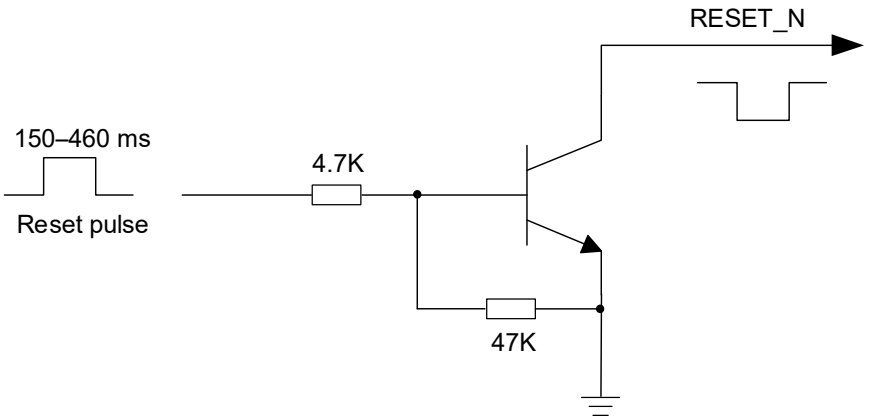


Figure 15: Reference Circuit of RESET_N by Using Driving Circuit

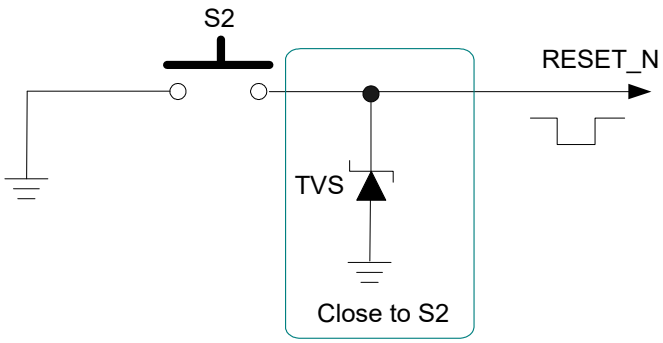


Figure 16: Reference Circuit of RESET_N by Using a Button

The reset timing is illustrated in the following figure.

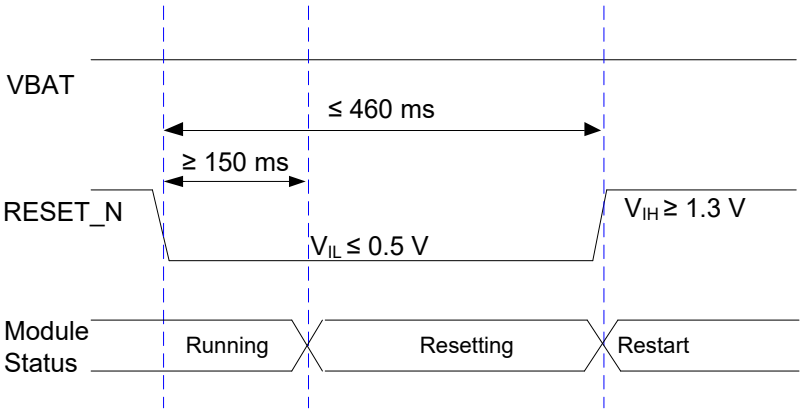


Figure 17: Reset Timing

NOTE

1. Use RESET_N only when failed to turn off the module by **AT+QPOWD** and PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.10. (U)SIM Interface

The module's (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	
USIM_ PRESENCE	13	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_GND	10	-	Specified ground for (U)SIM card	

The module supports the (U)SIM2 interface by configuring pins 119–122 and 128 via **AT+QDSIM=1**. For more details about the AT command, contact Quectel Technical Support.

Table 11: Pin Definition of (U)SIM2 Interface

Pin Name	Pin No.	Configured Function	I/O	Description	Comment
EPHY_RST_N	119	USIM2_RST	DO	(U)SIM2 card reset	
EPHY_INT_N	120	USIM2_DET	DI	(U)SIM2 card hot-plug detect	If unused, keep it open.
SGMII_MDATA	121	USIM2_CLK	DO	(U)SIM2 card clock	
SGMII_MCLK	122	USIM2_DATA	DIO	(U)SIM2 card data	
USIM2_VDD	128	USIM2_VDD	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.

The module supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low-level and high-level detections. By default, it is disabled, and can be configured via **AT+QSIMDET**. See ***document [2]*** for more details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

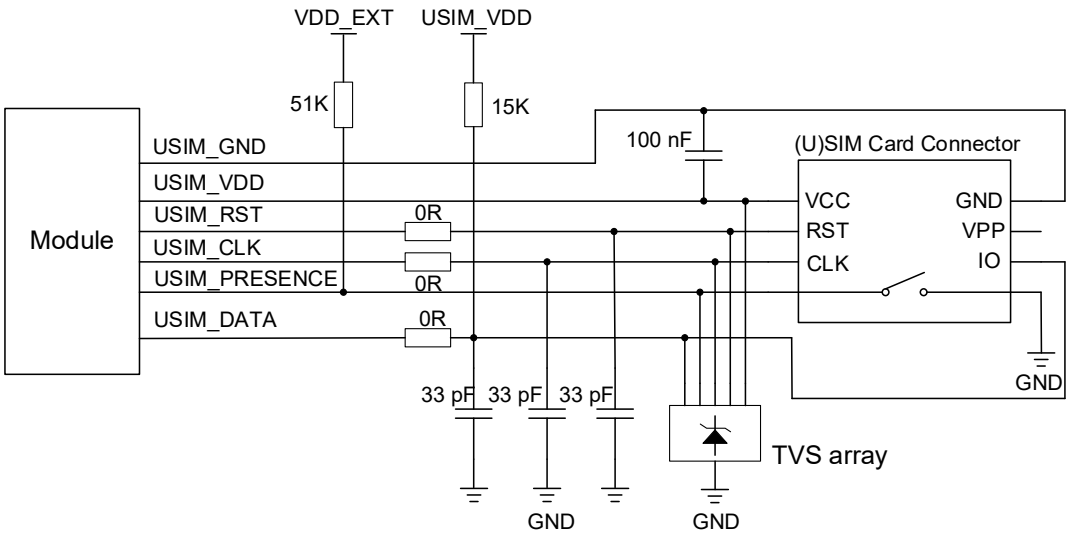


Figure 18: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

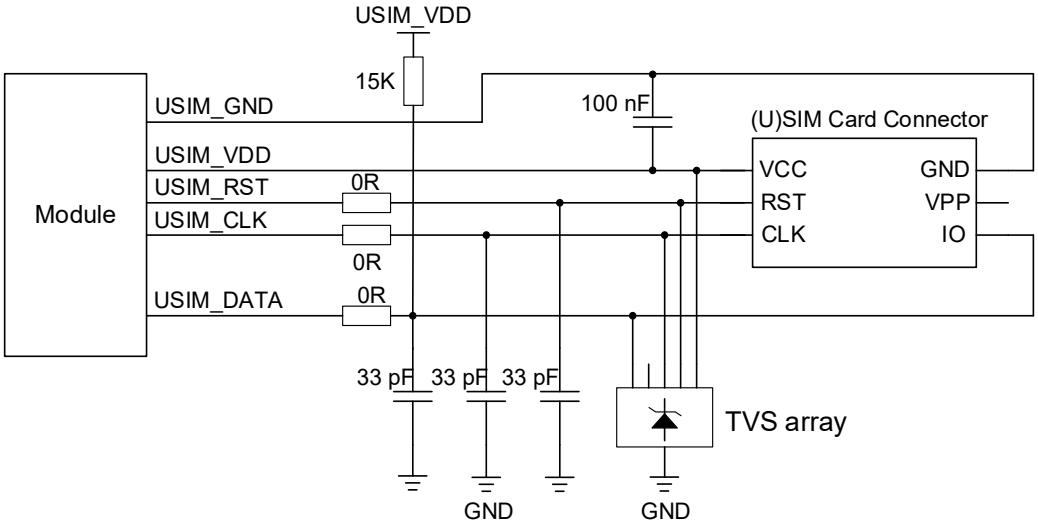


Figure 19: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in your applications, follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM_GND can

be connected to PCB ground directly.

- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, it is recommended to add a TVS array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering out RF interference. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA traces can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.11. USB Interface

The module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. USB interface can only work as a slave device.

USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB.

The following table shows the pin definition of USB interface.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. If unused, keep these pins open.
USB_DM	70	AIO	USB 2.0 differential data (-)	
USB_VBUS	71	AI	USB connection detect	If unused, keep it open.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

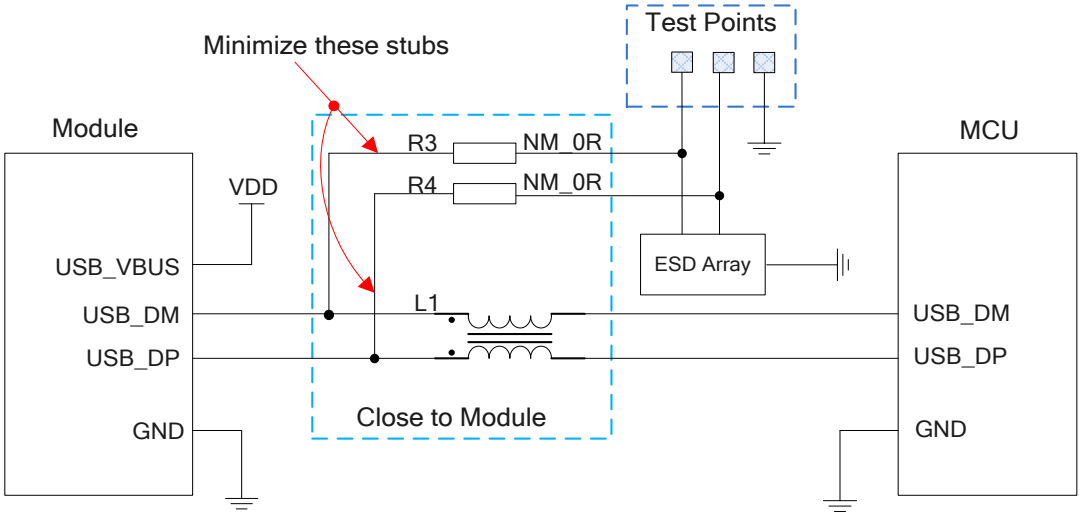


Figure 20: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, the following principles should be complied with when design the USB interface

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so pay attention to the selection of the component. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components as close to the USB connector as possible.

3.12. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and

921600 bps baud rates, and the default is 115200 bps. It also supports RTS and CTS hardware flow control, and can be used for data transmission and AT command communication.

- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Ring indication	1.8 V power domain. If unused, keep them open.
DCD	63	DO	Data carrier detect	
CTS	64	DO	Clear to send signal from the module	Connect to the MCU's CTS. 1.8 V power domain. If unused, keep it open.
RTS	65	DI	Request to send signal to the module	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep it open.
DTR	66	DI	Data terminal ready, sleep mode control	1.8 V power domain. Pulled up by default. DTR at low level can wake up the module. If unused, keep it open.
TXD	67	DO	Transmit	1.8 V power domain. If unused, keep these pins open.
RXD	68	DI	Receive	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Debug UART transmit	1.8 V power domain. If unused, keep them open.
DBG_RXD	11	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. A level-shifting circuit should be used if your application is equipped with a 3.3 V UART interface. A level-shifting chip TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

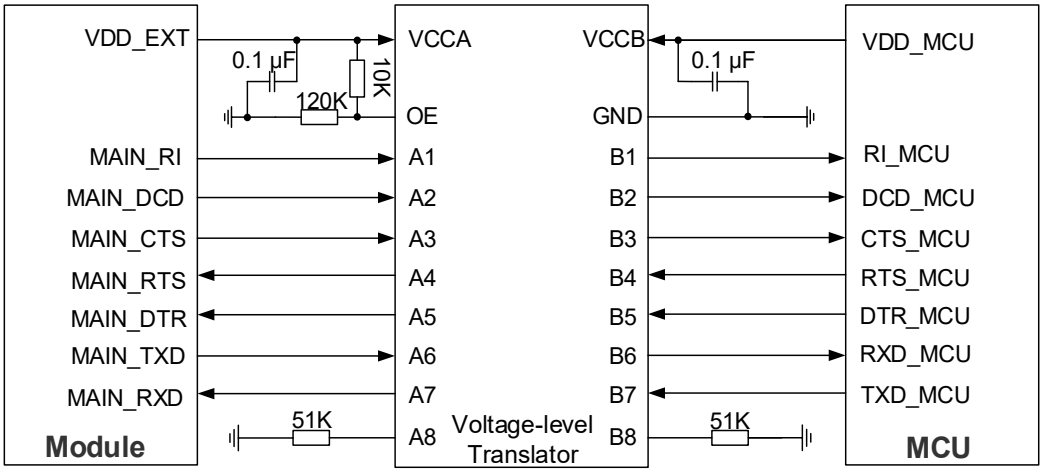


Figure 21: Reference Circuit with Translator Chip (Main UART)

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.

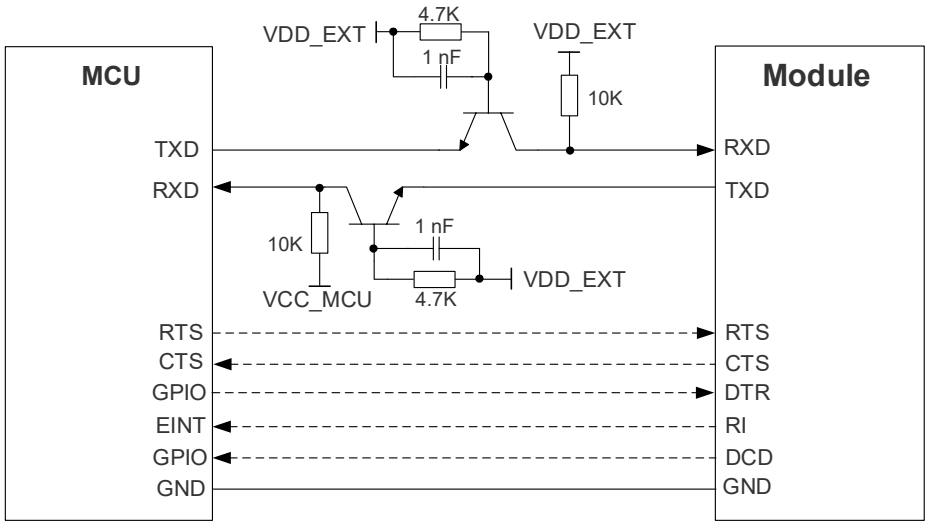


Figure 22: Reference Circuit with Transistor Circuit (Main UART)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. The level-shifting circuits (***Figure 21*** and ***Figure 22***) take the main UART as an example. The circuits of the debug UART are connected in the same way as the main UART.

4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

3.13. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

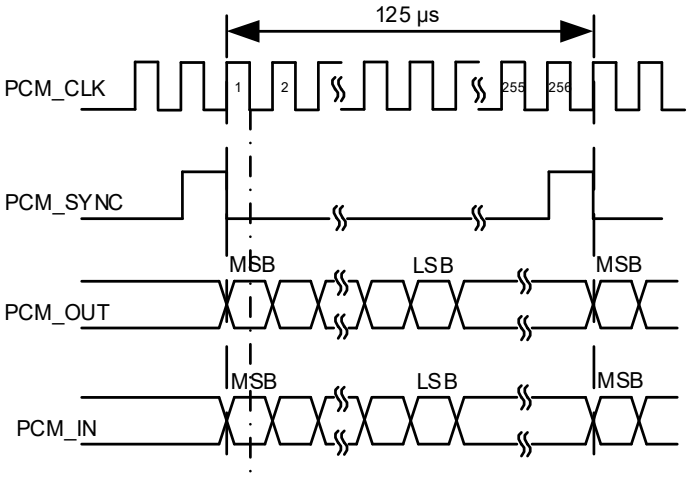


Figure 23: Primary Mode Timing

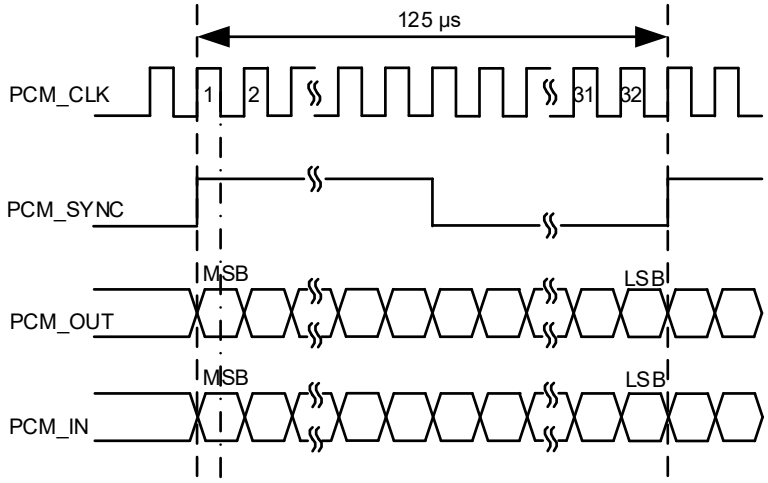


Figure 24: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 15: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8 V power domain. If unused, keep these pins open.
PCM_OUT	25	DO	PCM data output	
PCM_SYNC	26	DIO	PCM data frame sync	1.8 V power domain. Master mode: output. Slave mode: input. If unused, keep these pins open.
PCM_CLK	27	DIO	PCM clock	
I2C_SCL	41	OD	I2C serial clock (for external codec)	Require external pull-up to 1.8 V. If unused, keep these pins open.
I2C_SDA	42	OD	I2C serial data (for external codec)	

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** for more details about **AT+QDAI**.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

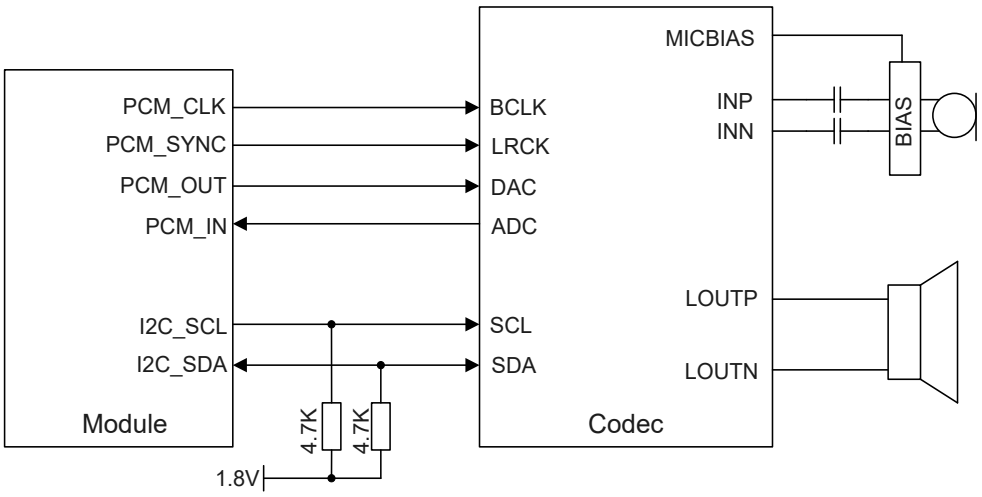


Figure 25: Reference Circuit of PCM and I2C Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuits on the PCM traces, especially for PCM_CLK.
2. The module works as a master device pertaining to I2C interface.

3.14. SD Card Interface

The module supports an SDIO 3.0 interface for SD card. The following table shows the pin definition of SD card interface.

Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	DIO	SD card data bit 3	SDIO signal level can be selected according to SD card supported level. See SD 3.0 protocol for more details. If unused, keep these pins open.
SDC2_DATA2	29	DIO	SD card data bit 2	
SDC2_DATA1	30	DIO	SD card data bit 1	
SDC2_DATA0	31	DIO	SD card data bit 0	
SDC2_CLK	32	DO	SD card clock	
SDC2_CMD	33	DIO	SD card command	

VDD_SDIO	34	PO	1.8/2.85 V output power for SD card pull-up circuits	1.8/2.85 V configurable. Cannot be used for SD card power. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detect	1.8 V power domain. This pin must be connected if SD card is used, and keep it open if SD card is unused.

The following figure shows a reference design of SD card.

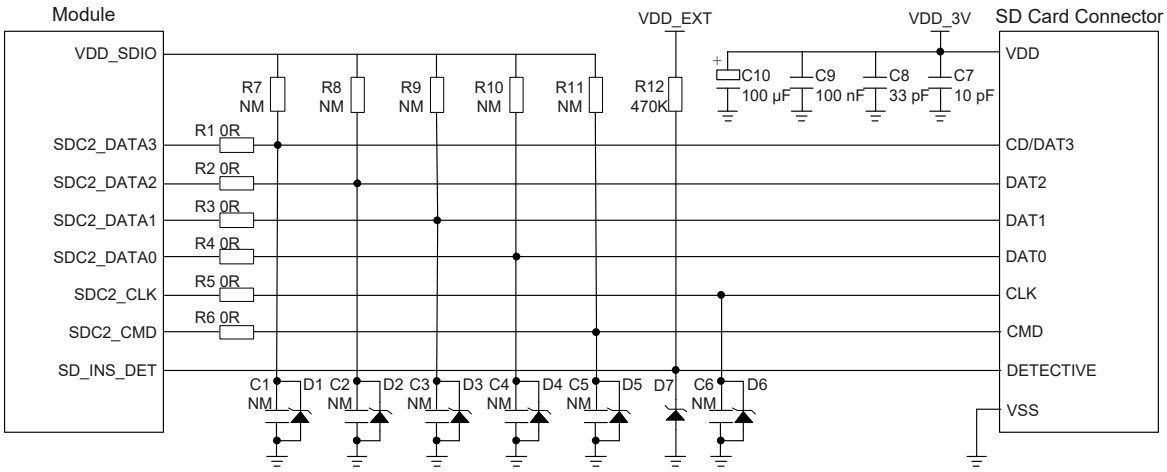


Figure 26: Reference Circuit of SD Card Interface

In SD card interface design, to ensure good communication performance with SD card, the following design principles should be complied with:

- SD_INS_DET must be connected if SD card is used, and keep SD_INS_DET open if SD card is unused.
- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of VDD_SDIO is 50 mA which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to VDD_SDIO. The value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. VDD_SDIO should be used as the pull-up power.
- To adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data

trace is 50 Ω (±10%).
- Make sure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SDC2_CLK and SDC2_DATA[0:3]/SDC2_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 27 mm, so the exterior total trace length should be less than 23 mm.

3.15. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces.

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0.
- **AT+QADC=1**: read the voltage value on ADC1.

For more details about these AT commands, see ***document [2]***.

To improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 17: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	45	AI	General-purpose ADC interface	If unused, keep these pins open.
ADC1	44	AI		

The following table describes the characteristic of ADC function.

Table 18: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC Input Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	15	-	bits

NOTE

1. ADC input voltage must not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT power supply is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.16. SGMII Interface

The module includes an integrated Ethernet MAC with four SGMII data signals, two management signals and two control signals. The key features of the SGMII interface are shown below:

- Compliant with IEEE802.3.
- Support 10/100/1000 Mbps Ethernet work mode.
- Support maximum 10 Mbps (DL)/5 Mbps (UL) for 4G network.
- Support VLAN tagging.
- Support IEEE1588 and Precision Time Protocol (PTP).
- Can be used to connect to external Ethernet PHY, such as AR8033, or to an external switch.
- Management interfaces support dual voltage: 1.8/2.85 V.

The following table shows the pin definition of SGMII interface.

Table 19: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control and Management Signals				
EPHY_RST_N	119	DO	SGMII reset external PHY	1.8/2.85 V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	SGMII interrupt	1.8 V power domain. If unused, keep it open.
SGMII_MDATA	121	DIO	SGMII management data input/output	1.8/2.85 V power domain. Requires external pull-up to USIM2_VDD, and the resistor should be 1.5 kΩ. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII management data clock	1.8/2.85 V power domain. If unused, keep it open.
USIM2_VDD	128	PO	SGMII MDIO pull-up power supply	Configurable power source. 1.8/2.85 V power domain. If unused, keep it open.

SGMII Data Signals				
SGMII_TX_M	123	AO	SGMII transmit (-)	Add a 0.1 μF capacitor close to the PHY chip. If unused, keep these pins open.
SGMII_TX_P	124	AO	SGMII transmit (+)	
SGMII_RX_P	125	AI	SGMII receive (+)	Add a 0.1 μF capacitor close to the module. If unused, keep these pins open.
SGMII_RX_M	126	AI	SGMII receive (-)	

The following figure shows the simplified block diagram for Ethernet application.

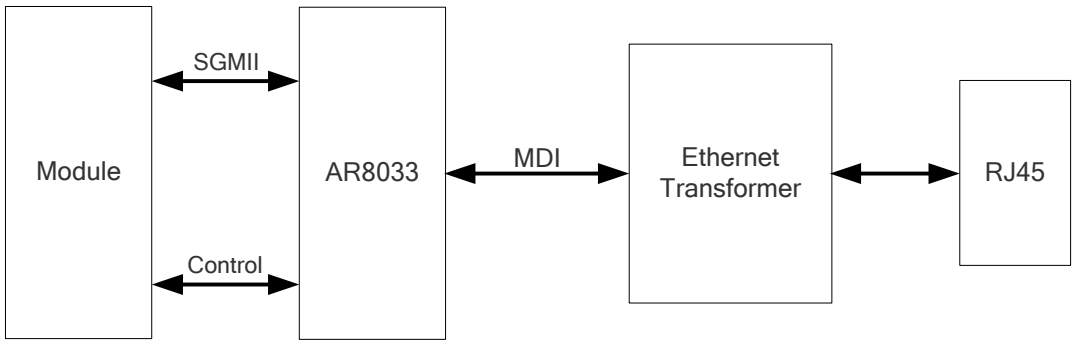


Figure 27: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

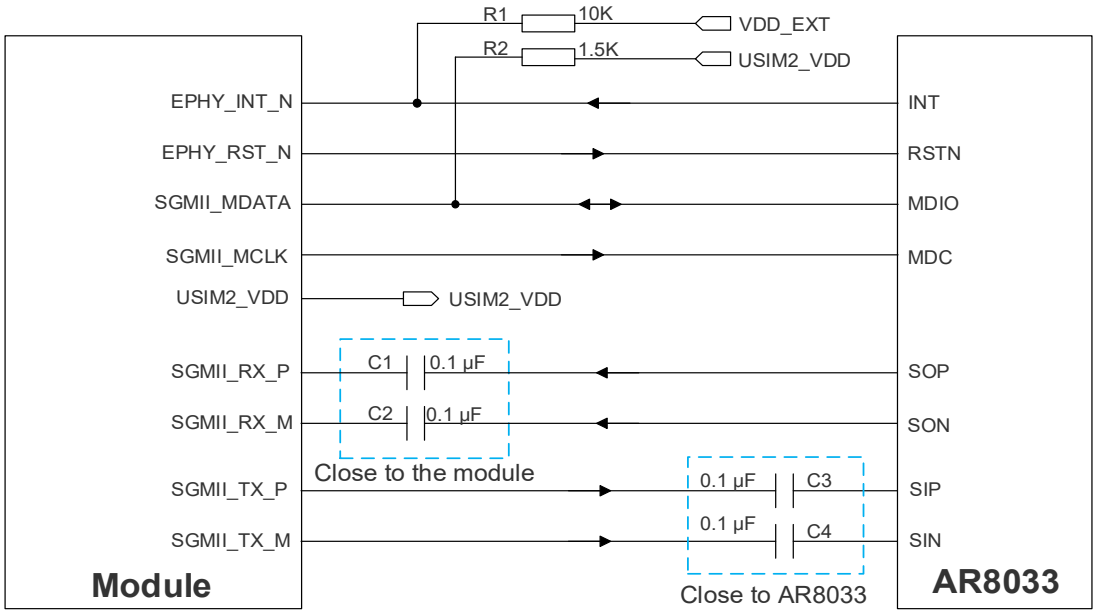


Figure 28: Reference Circuit of SGMII Interface with PHY AR8033 Application

To enhance the reliability and availability in your applications, follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data, control and management signals away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- Keep the maximum trace length less than 10-inch and keep skew on the differential pairs less than 20 mil.
- The differential impedance of SGMII data traces is 100 Ω ±10 % and ensure the integrity of the reference ground.
- Make sure the trace spacing between SGMII_TX_P/M and SGMII_RX_P/M is at least 3 times the trace width, and the same to the adjacent signal traces.

3.17. Indication Signals

3.17.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 20: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep it open.

Table 21: Working State of Network Connection Status/Activity Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle

	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

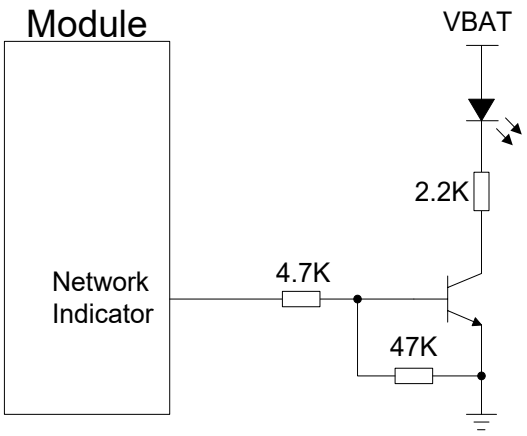


Figure 29: Reference Circuit of the Network Indicator

3.17.2. STATUS

The STATUS pin is an open drain output signal used to indicate the module's operation status. It can be connected to a GPIO of the MCU with a pull-up resistor, or designed according to the LED indicator circuit shown in the figure below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 22: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operating status	The drive current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

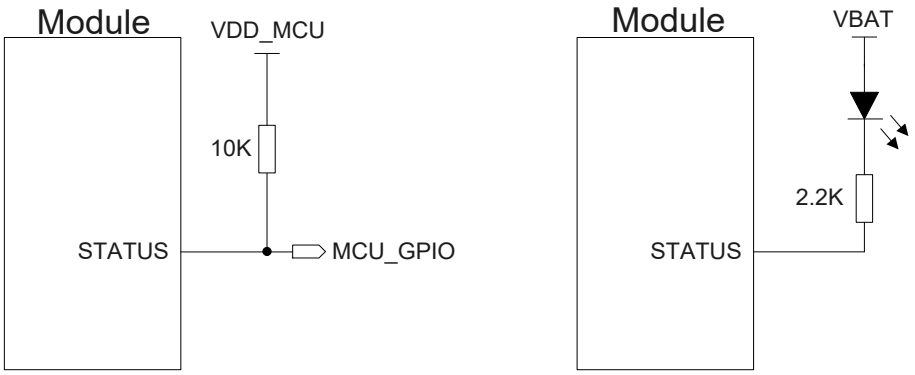


Figure 30: Reference Circuits of STATUS

NOTE

The STATUS pin cannot be used as the shutdown status indication of the module when VBAT power supply is removed.

3.17.3. RI

AT+QCFG="risignaltype","physical" can be used to configure RI behaviors. No matter on which port a URC is presented, the URC will trigger the behaviors of RI pin. For more details about the command, see ***document [3]***.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG**. The default port is USB AT port. See ***document [2]*** for details.

The default behaviors of the RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document [3]*** for details.

Table 23: Behaviors of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120 ms low pulse when a new URC returns

3.18. USB_BOOT Interface

The module provides a USB_BOOT pin. Pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, then the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 24: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to enter download mode	Active high. 1.8 V power domain. If the forced download mode is not used, the pin cannot be pulled up before startup. It is recommended to reserve a test point.

The following figures show the reference circuit of USB_BOOT interface and timing of entering forced download mode.

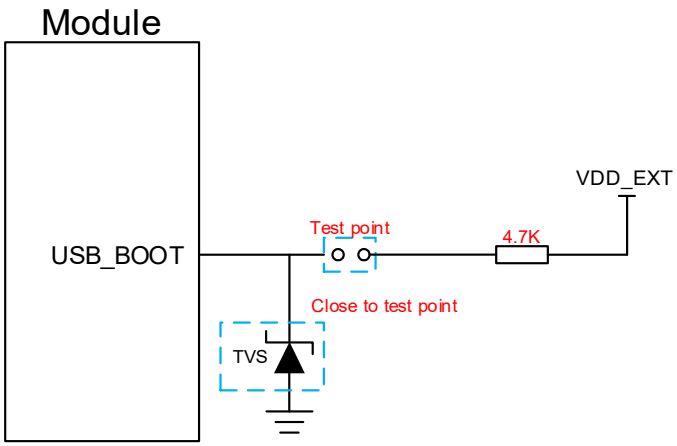


Figure 31: Reference Circuit of USB_BOOT Interface

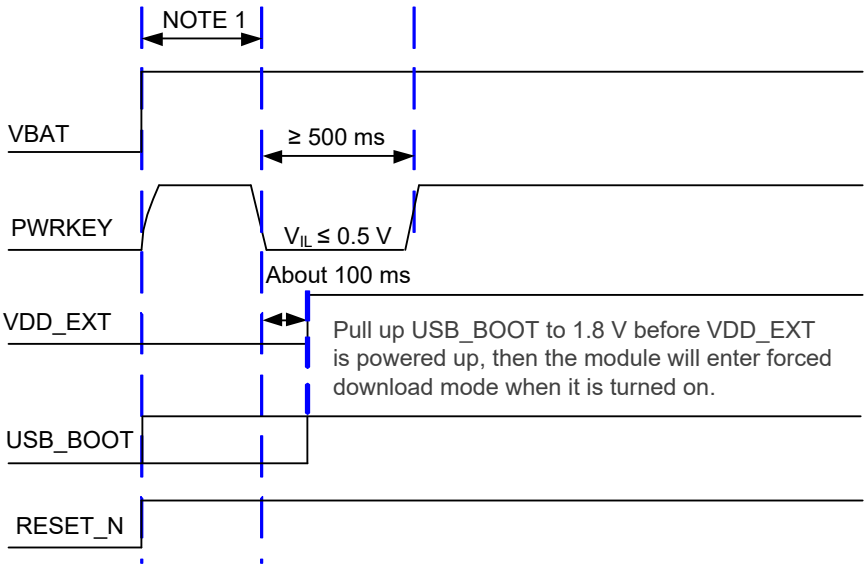


Figure 32: Timing of Entering Forced Download Mode

NOTE

1. Make sure that VBAT is stable before driving PWRKEY low. It is recommended that the time between powering up VBAT and driving PWRKEY low is not less than 30 ms.
2. When using MCU to control the module to enter the forced download mode, follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Connecting the test points as shown in ***Figure 31*** can manually force the module to enter download mode.

4 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The characteristic impedance of the antenna ports is 50 Ω. The antenna interfaces of the module are shown as follow:

- One main antenna interface
- One Rx-diversity antenna interface (which is used to resist the fall of signals caused by high-speed movement and multipath effect)
- One GNSS antenna interface

4.1. Cellular Network

4.1.1. Antenna Interfaces & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 25: Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_DIV	35	AI	Diversity antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 26: Operating Frequency

3GPP Bands	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830–840	875–885	MHz
WCDMA B8	880–915	925–960	MHz
WCDMA B19	830–845	875–890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz

LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

4.1.2. Tx Power

The following table shows the RF output power of the module.

Table 27: Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850/EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800/PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE bands	23 dBm ±2 dB	< -39 dBm

NOTE

1. For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.
2. EG21-G supports LTE B25, and the PA chip in the module does not actually support LTE B25. The chip vendor has confirmed that the SAW integrated in the PA can support LTE B2, but B25 can work at the same frequency as B2. B25 is 5 MHz wider than B2. Therefore, the sensitivity of the RX channels 8630–8689 is poor, and there is a big gap with the 3GPP standard. At a high temperature of 75 °C, the maximum power of channels 26640–26689 will be reduced by about 2.5 dB.

4.1.3. Rx Sensitivity

The following tables show the conducted RF receiving sensitivity of the module.

Table 28: Conducted RF Receiving Sensitivity

Frequency Band	Receiver Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [4]	
EGSM900	-107.6 dBm	-	-	-102 dBm
GSM850	-107.8 dBm	-	-	-102 dBm
DCS1800	-107 dBm	-	-	-102 dBm
PCS1900	-107.8 dBm	-	-	-102 dBm
WCDMA B1	-108.8 dBm	-108.5 dBm	-109.2 dBm	-106.7 dBm
WCDMA B2	-109.5 dBm	-109 dBm	-110.8 dBm	-104.7 dBm
WCDMA B4	-109 dBm	-	-	-106.7 dBm
WCDMA B5	-109.2 dBm	-109.5 dBm	-111 dBm	-104.7 dBm
WCDMA B6	-110 dBm	-109.5 dBm	-111.1 dBm	-106.7 dBm
WCDMA B8	-109.8 dBm	-	-	-103.7 dBm
WCDMA B19	-110.5 dBm	-109.5 dBm	-111.5 dBm	-106.7 dBm
LTE-FDD B1 (10 MHz)	-97 dBm	-98 dBm	-100.4 dBm	-96.3 dBm
LTE-FDD B2 (10 MHz)	-97.7 dBm	-99 dBm	-100.3 dBm	-94.3 dBm
LTE-FDD B3 (10 MHz)	-97 dBm	-97.8 dBm	-99.7 dBm	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97.2 dBm	-97.8 dBm	-100.3 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-98 dBm	-99.3 dBm	-102 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96 dBm	-96.4 dBm	-99.2 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98 dBm	-99 dBm	-101.5 dBm	-93.3 dBm

[4] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

LTE-FDD B12 (10 MHz)	-98 dBm	-99.2 dBm	-101.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-96.8 dBm	-98 dBm	-100 dBm	-93.3 dBm
LTE-FDD B18 (10 MHz)	-98 dBm	-99.4 dBm	-100 dBm	-96.3 dBm
LTE-FDD B19 (10 MHz)	-98 dBm	-99.2 dBm	-101.5 dBm	-96.3 dBm
LTE-FDD B20 (10 MHz)	-98 dBm	-98.8 dBm	-101 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.2 dBm	-98.4 dBm	-100 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-97.8 dBm	-99.5 dBm	-101 dBm	-93.8 dBm
LTE-FDD B28 (10 MHz)	-97.5 dBm	-98.5 dBm	-100.5 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-97.5 dBm	-96.3 dBm	-98 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-97.4 dBm	-98.2 dBm	-100 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.6 dBm	-96.7 dBm	-99.5 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.2 dBm	-95 dBm	-99 dBm	-94.3 dBm

4.1.4. Reference Design

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

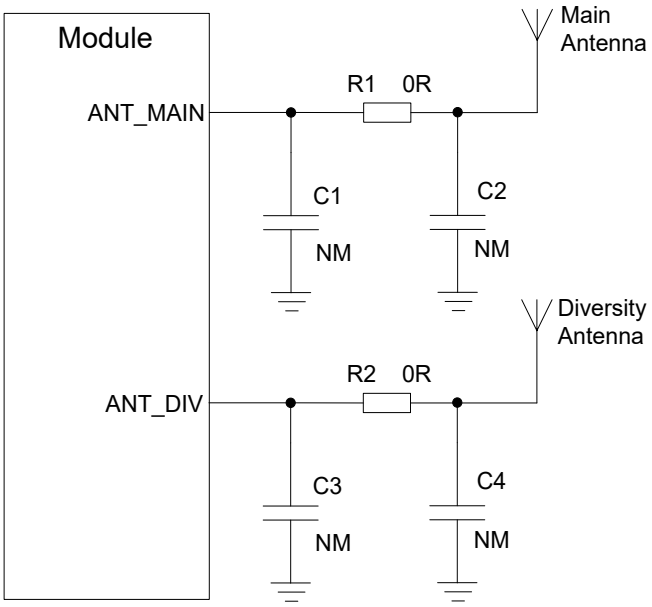


Figure 33: Reference Circuit of Cellular Antenna Interfaces

NOTE

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. For the operation of ANT_MAIN and ANT_DIV, see **AT+QCFG="divctl"** in ***document [3]*** for details.
3. Place the π-type matching components (R1&C1&C2, R2&C3&C4) as close to the antenna as possible.

4.2. GNSS (Optional)

The module includes fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine of the module is turned off by default. It can be turned on by the AT command. For more details about GNSS engine technology and configurations, see ***document [5]***.

4.2.1. Antenna Interface & Frequency Band

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 29: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 30: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz

BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

4.2.2. GNSS Performance

The following table shows the GNSS performance of the module.

Table 31: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF	Cold start @ open sky	Autonomous	33	s
		XTRA start	10	s
	Warm start @ open sky	Autonomous	28	s
		XTRA start	3	s
	Hot start @ open sky	Autonomous	2	s
		XTRA start	1.6	s
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.2.3. Reference Design

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design.

A reference design of GNSS antenna is shown as below.

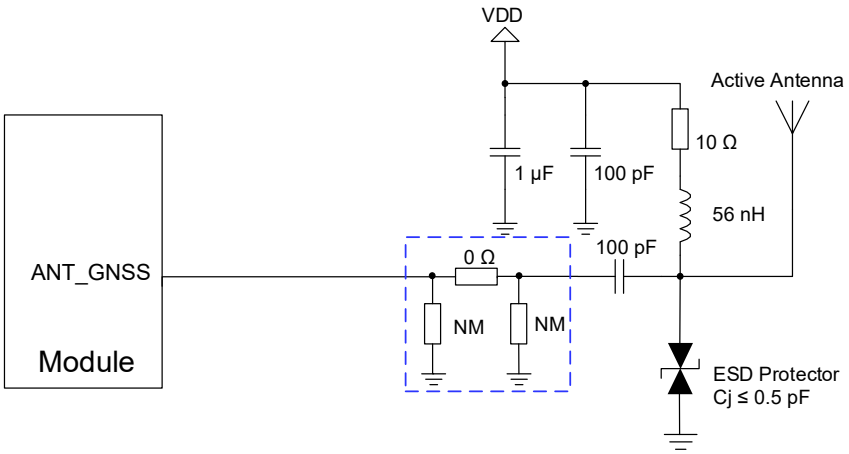


Figure 34: Reference Circuit of GNSS Antenna Interface

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.
3. It is not recommended to add an external LNA when using a passive GNSS antenna.
4. It is recommended to use a passive GNSS antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

4.2.4. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS traces.

4.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

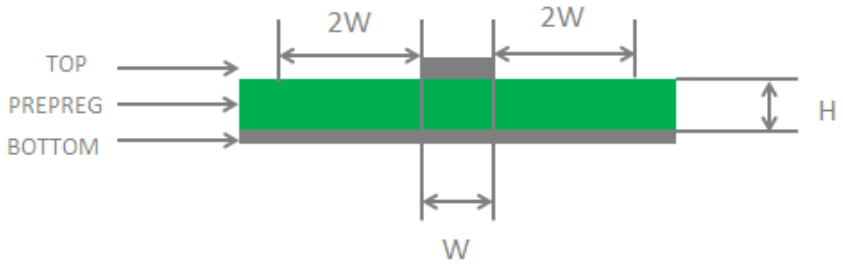


Figure 35: Microstrip Design on a 2-layer PCB

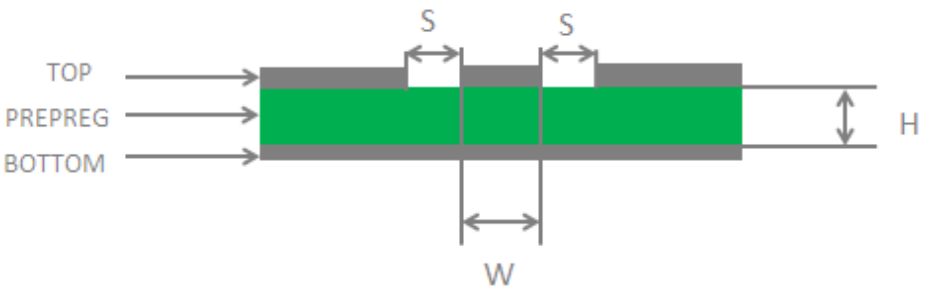


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

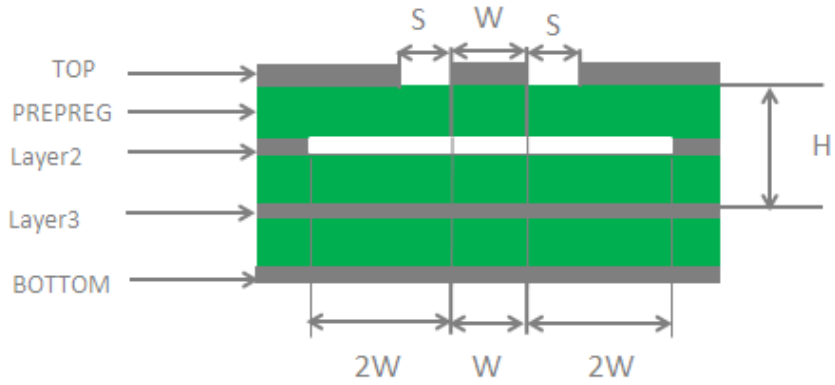


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

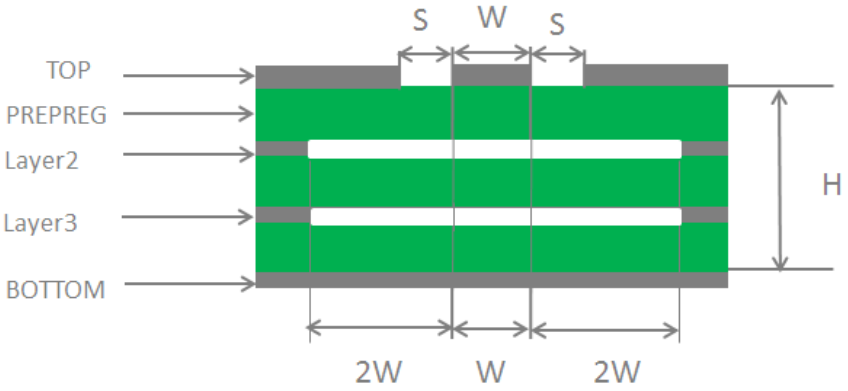


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

4.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 32: Antenna Design Requirements

Type	Requirements
GNSS (Optional)	• Frequency range: 1559–1609 MHz • Polarization: RHCP or linear • VSWR: ≤ 2 (Typ.)
	For passive antenna usage: • Passive antenna gain: > 0 dBi
	For active antenna usage: • Active antenna noise figure: < 1.5 dB • Active antenna embedded LNA gain: < 17 dB
Cellular	• VSWR: ≤ 2 • Efficiency: > 30 % • Max. input power: 50 W • Input impedance: 50 Ω • Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

4.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

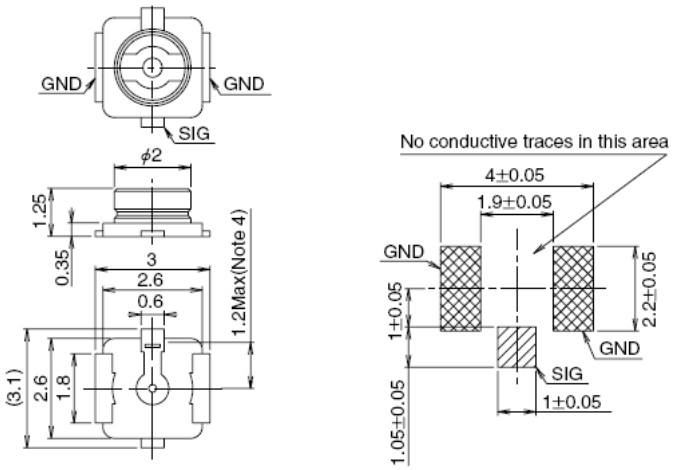


Figure 39: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

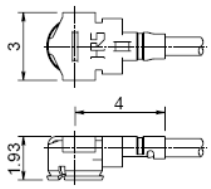
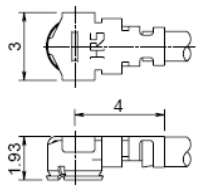
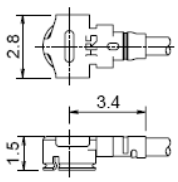
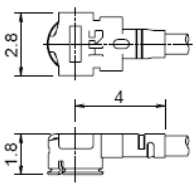
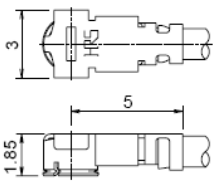
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

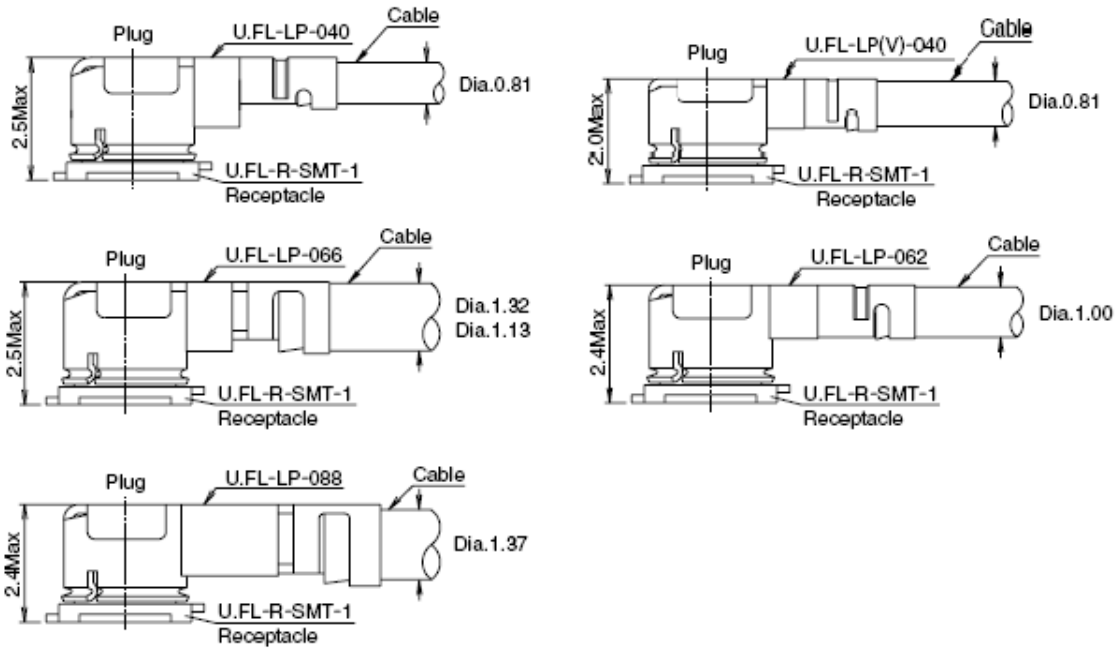


Figure 41: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 33: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC Pins	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 34: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current	Maximum power control level	-	1.8	2.0	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 35: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [5]	-35	+25	+75	ºC
Extended Temperature Range [6]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[5] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[6] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module retains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

5.4. Power Consumption

Table 36: Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.6	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.1	mA
	EGSM900 @ DRX = 5 (USB Suspend)	2.4	mA
	EGSM900 @ DRX = 9 (USB disconnected)	2.0	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.1	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.7	mA
	DCS1800 @ DRX = 5 (USB Suspend)	1.9	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.5	mA
	WCDMA @ PF = 64 (USB disconnected)	1.9	mA
	WCDMA @ PF = 64 (USB Suspend)	2.2	mA
	WCDMA @ PF = 128 (USB disconnected)	1.6	mA
	WCDMA @ PF = 256 (USB disconnected)	1.4	mA
	WCDMA @ PF = 512 (USB disconnected)	1.3	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.4	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.4	mA
	LTE-FDD @ PF = 64 (USB Suspend)	2.6	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.8	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.6	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.6	mA

	LTE-TDD @ PF = 64 (USB disconnected)	2.5	mA
	LTE-TDD @ PF = 64 (USB Suspend)	2.7	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.8	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.6	mA
Idle state	EGSM900 @DRX = 5 (USB disconnected)	16	mA
	EGSM900 @DRX = 5 (USB connected)	25	mA
	WCDMA @ PF = 64 (USB disconnected)	14	mA
	WCDMA @ PF = 64 (USB connected)	25	mA
	LTE-FDD @ PF = 64 (USB disconnected)	16	mA
	LTE-FDD @ PF = 64 (USB connected)	25	mA
	LTE-TDD @ PF = 64 (USB disconnected)	15	mA
	LTE-TDD @ PF = 64 (USB connected)	25	mA
GPRS data transmission (GNSS OFF)	EGSM900 4DL/1UL @ 32.05 dBm	274	mA
	EGSM900 3DL/2UL @ 30.91 dBm	463	mA
	EGSM900 2DL/3UL @ 29.05 dBm	554	mA
	EGSM900 1DL/4UL @ 27.70 dBm	652	mA
	GSM850 4DL/1UL @ 32.16 dBm	303	mA
	GSM850 3DL/2UL @ 29.87 dBm	477	mA
	GSM850 2DL/3UL @ 28.85 dBm	601	mA
	GSM850 1DL/4UL @ 27.51 dBm	707	mA
	DCS1800 4DL/1UL @ 29.34 dBm	150	mA
	DCS1800 3DL/2UL @ 28.60 dBm	245	mA
	DCS1800 2DL/3UL @ 26.62 dBm	303	mA
	DCS1800 1DL/4UL @ 25.73 dBm	359	mA
	PCS1900 4DL/1UL @ 29.37 dBm	165	mA

	PCS1900 3DL/2UL @ 28.08 dBm	270	mA
	PCS1900 2DL/3UL @ 26.41 dBm	332	mA
	PCS1900 1DL/4UL @ 25.47 dBm	391	mA
EDGE data transmission (GNSS OFF)	EGSM900 4DL/1UL @ 26.22 dBm	162	mA
	EGSM900 3DL/2UL @ 25.02 dBm	270	mA
	EGSM900 2DL/3UL @ 23.44 dBm	336	mA
	EGSM900 1DL/4UL @22.47 dBm	402	mA
	GSM850 4DL/1UL @ 25.90 dBm	180	mA
	GSM850 3DL/2UL @ 24.77 dBm	291	mA
	GSM850 2DL/3UL @ 23.03 dBm	363	mA
	GSM850 1DL/4UL @ 21.90 dBm	429	mA
	DCS1800 4DL/1UL @ 25.70 dBm	120	mA
	DCS1800 3DL/2UL @ 25.03 dBm	200	mA
	DCS1800 2DL/3UL @ 23.94 dBm	260	mA
	DCS1800 1DL/4UL @ 22.81 dBm	315	mA
	PCS1900 4DL/1UL @ 25.56 dBm	126	mA
	PCS1900 3DL/2UL @ 24.73 dBm	208	mA
	PCS1900 2DL/3UL @ 23.33 dBm	276	mA
	PCS1900 1DL/4UL @ 22.23 dBm	332	mA
WCDMA data transmission (GNSS OFF)	WCDMA B1 HSDPA @ 22.52 dBm	577	mA
	WCDMA B1 HSUPA @ 21.85 dBm	585	mA
	WCDMA B2 HSDPA @ 22.32 dBm	610	mA
	WCDMA B2 HSUPA @ 21.79 dBm	609	mA
	WCDMA B4 HSDPA @ 22.60 dBm	586	mA
	WCDMA B4 HSUPA @ 22.18 dBm	550	mA

	WCDMA B5 HSDPA @ 22.24 dBm	576	mA
	WCDMA B5 HSUPA @ 21.59 dBm	600	mA
	WCDMA B6 HSDPA @ 22.22 dBm	575	mA
	WCDMA B6 HSUPA @ 21.84 dBm	595	mA
	WCDMA B8 HSDPA @ 22.01 dBm	600	mA
	WCDMA B8 HSUPA @ 21.47 dBm	506	mA
	WCDMA B19 HSDPA @ 22.07 dBm	560	mA
	WCDMA B19 HSUPA @ 22.39 dBm	545	mA
LTE data transmission (GNSS OFF)	LTE-FDD B1 @ 22.99 dBm	700	mA
	LTE-FDD B2 @ 22.93 dBm	750	mA
	LTE-FDD B3 @ 23.30 dBm	730	mA
	LTE-FDD B4 @ 23.55 dBm	785	mA
	LTE-FDD B5 @ 23.06 dBm	712	mA
	LTE-FDD B7 @ 22.76 dBm	700	mA
	LTE-FDD B8 @ 22.93 dBm	831	mA
	LTE-FDD B12 @ 23.19 dBm	660	mA
	LTE-FDD B13 @ 22.79 dBm	685	mA
	LTE-FDD B18 @ 23.18 dBm	690	mA
	LTE-FDD B19 @ 23.04 dBm	634	mA
	LTE-FDD B20 @ 22.95 dBm	750	mA
	LTE-FDD B25 @ 23.50 dBm	763	mA
	LTE-FDD B26 @ 23.20 dBm	761	mA
	LTE-FDD B28 @ 23.40 dBm	720	mA
	LTE-TDD B38 @ 23.32 dBm	400	mA
	LTE-TDD B39 @ 23.06 dBm	353	mA

	LTE-TDD B40 @ 22.70 dBm	366	mA
	LTE-TDD B41 @ 23.37 dBm	395	mA
GSM voice call	EGSM900 PCL = 5 @ 32.2 dBm	295	mA
	EGSM900 PCL = 12 @ 19.2 dBm	124	mA
	EGSM900 PCL = 19 @ 4.1 dBm	100	mA
	GSM850 PCL = 5 @ 32.2 dBm	318	mA
	GSM850 PCL = 12 @ 19.2 dBm	128	mA
	GSM850 PCL = 19 @ 4.1 dBm	94	mA
	DCS1800 PCL = 0 @ 29.3 dBm	161	mA
	DCS1800 PCL = 7 @ 16.1 dBm	108	mA
	DCS1800 PCL = 15 @ 0.7 dBm	85	mA
	PCS1900 PCL = 0 @ 29.4 dBm	173	mA
	PCS1900 PCL = 7 @ 16.1 dBm	106	mA
	PCS1900 PCL = 15 @ 0.3 dBm	79	mA
WCDMA voice call	WCDMA B1 @ 23.5 dBm	640	mA
	WCDMA B2 @ 23.4 dBm	665	mA
	WCDMA B4 @ 23.5 dBm	625	mA
	WCDMA B5 @ 23.3 dBm	620	mA
	WCDMA B6 @ 23.0 dBm	560	mA
	WCDMA B8 @ 23.3 dBm	650	mA
	WCDMA B19 @ 23.2 dBm	576	mA

Table 37: GNSS Power Consumption

Description	Conditions	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Passive antenna	43	mA
	Lost state @ Passive antenna	42	mA
Tracking (**AT+CFUN=0**)	Instrument environment	25	mA
	Open sky @ Passive antenna	43	mA
	Open sky @ Active antenna	43	mA

5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 38: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

5.6. Thermal Dissipation

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On your PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier and power supply.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.

- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to your application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and you can choose one or both of them according to their application structure.

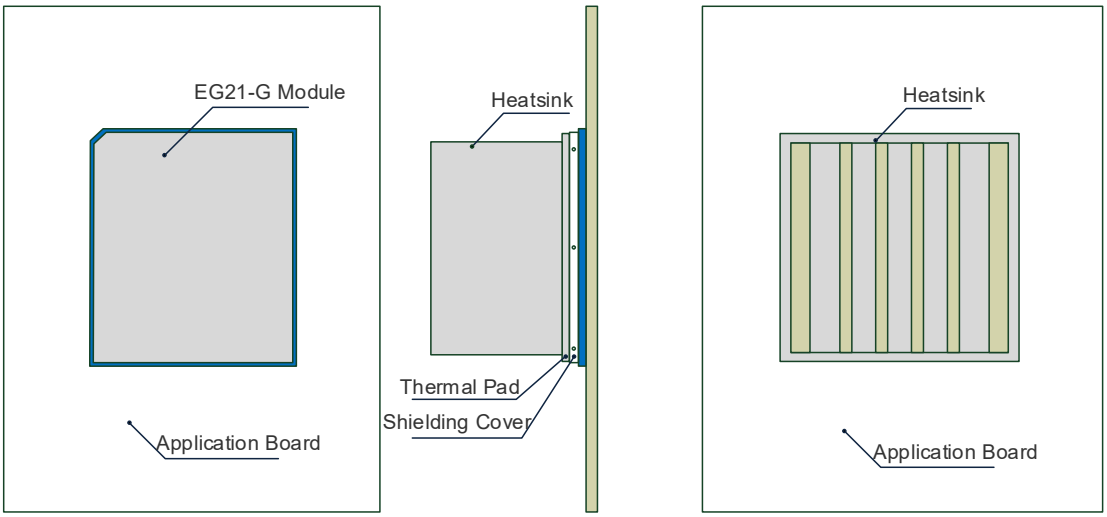


Figure 42: Referenced Heatsink Design (Heatsink at the Top of the Module)

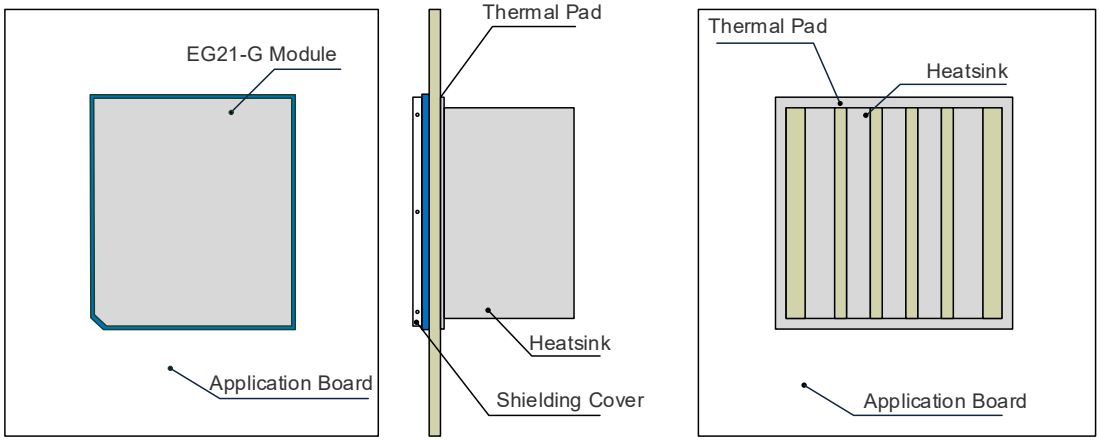


Figure 43: Referenced Heatsink Design (Heatsink at the Backside of Your PCB)

NOTE

The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power and data rate.). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. You can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value. For more details of the command, see ***document [7]***.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

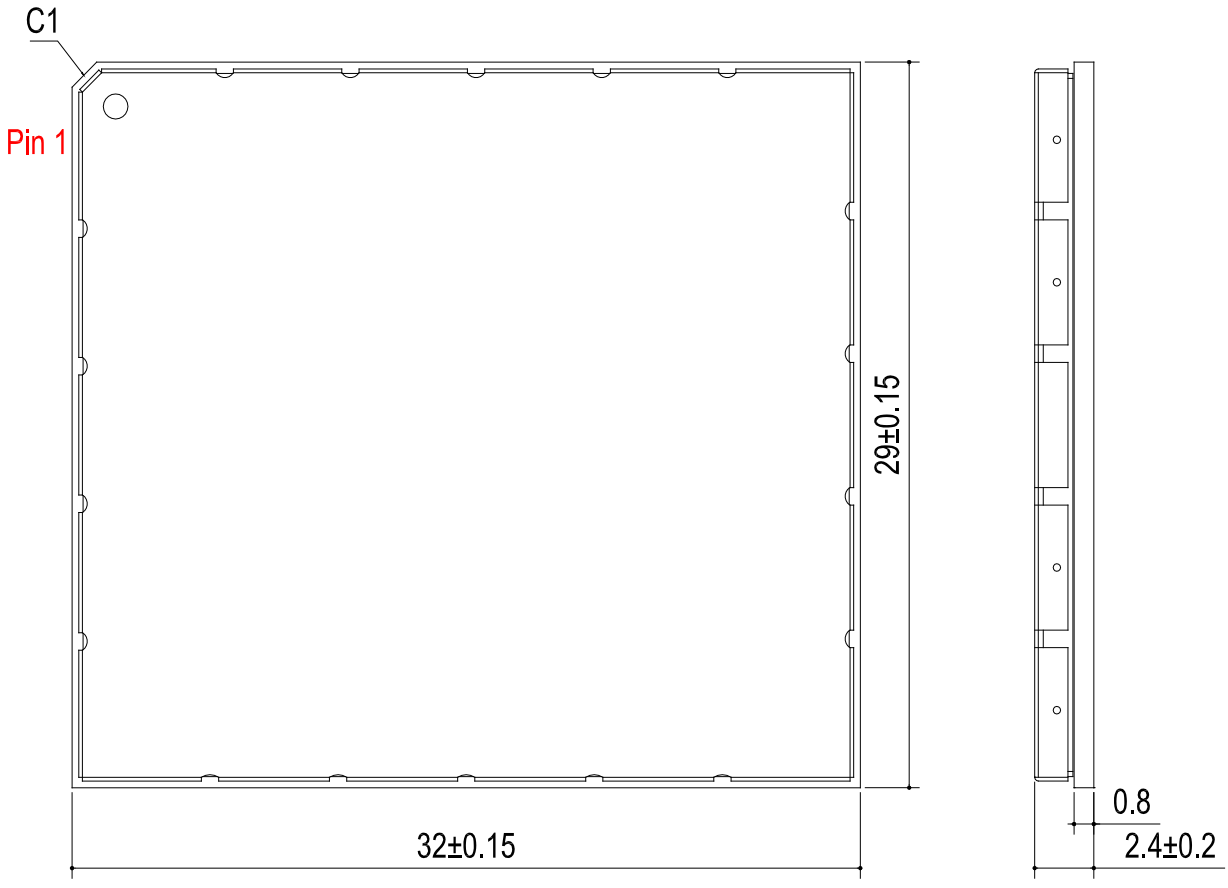


Figure 44: Module Top and Side Dimensions

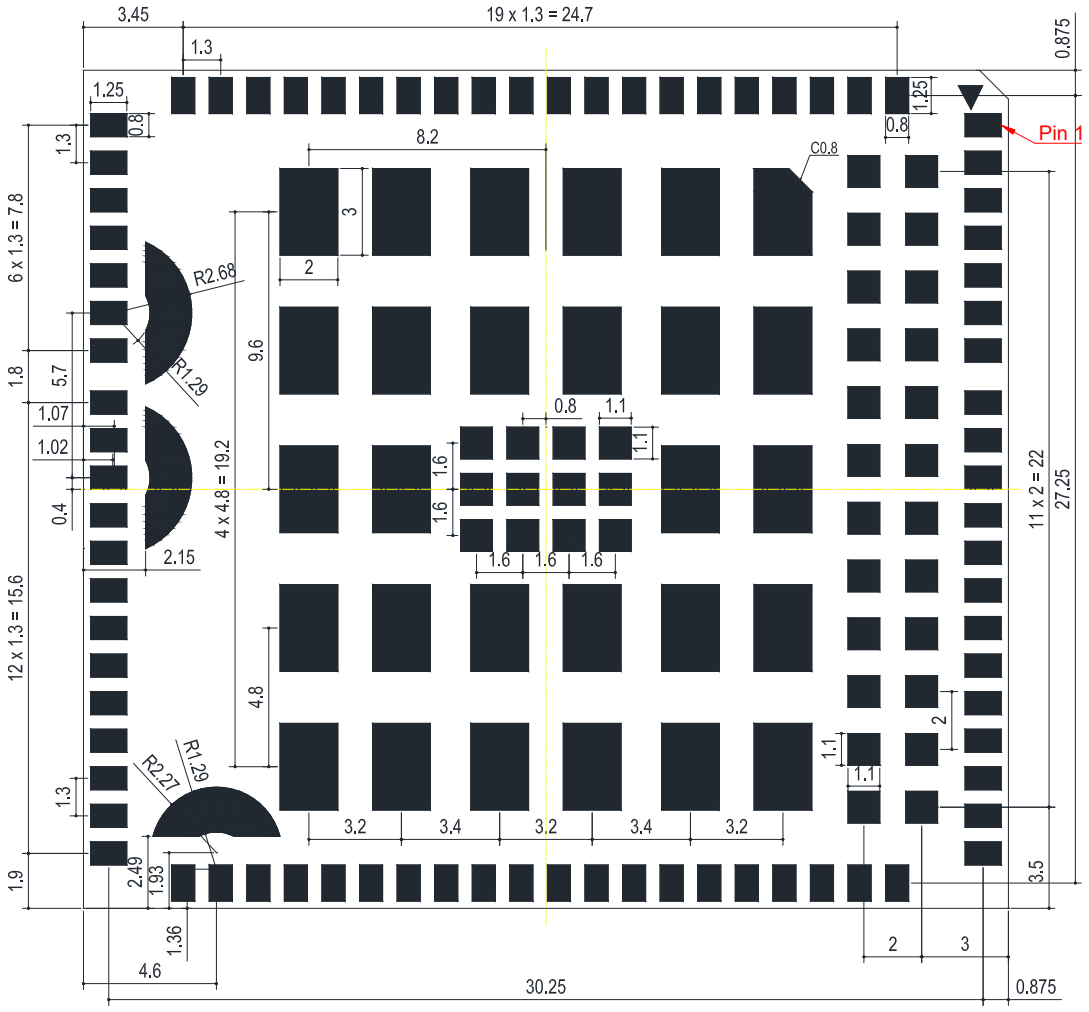


Figure 45: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

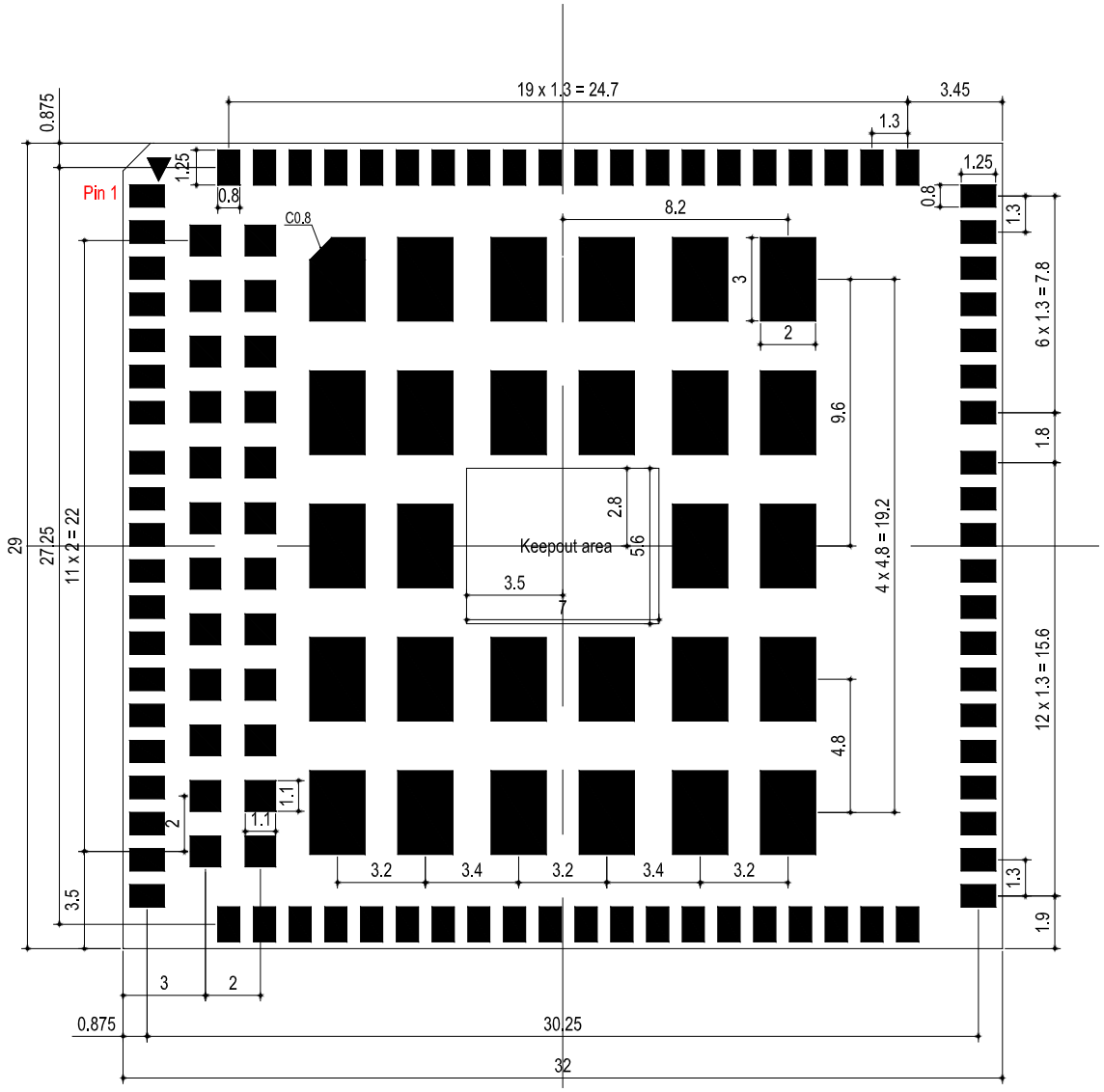


Figure 46: Recommended Footprint

NOTE

1. The keepout area should not be designed.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Recommended Compatible Footprint

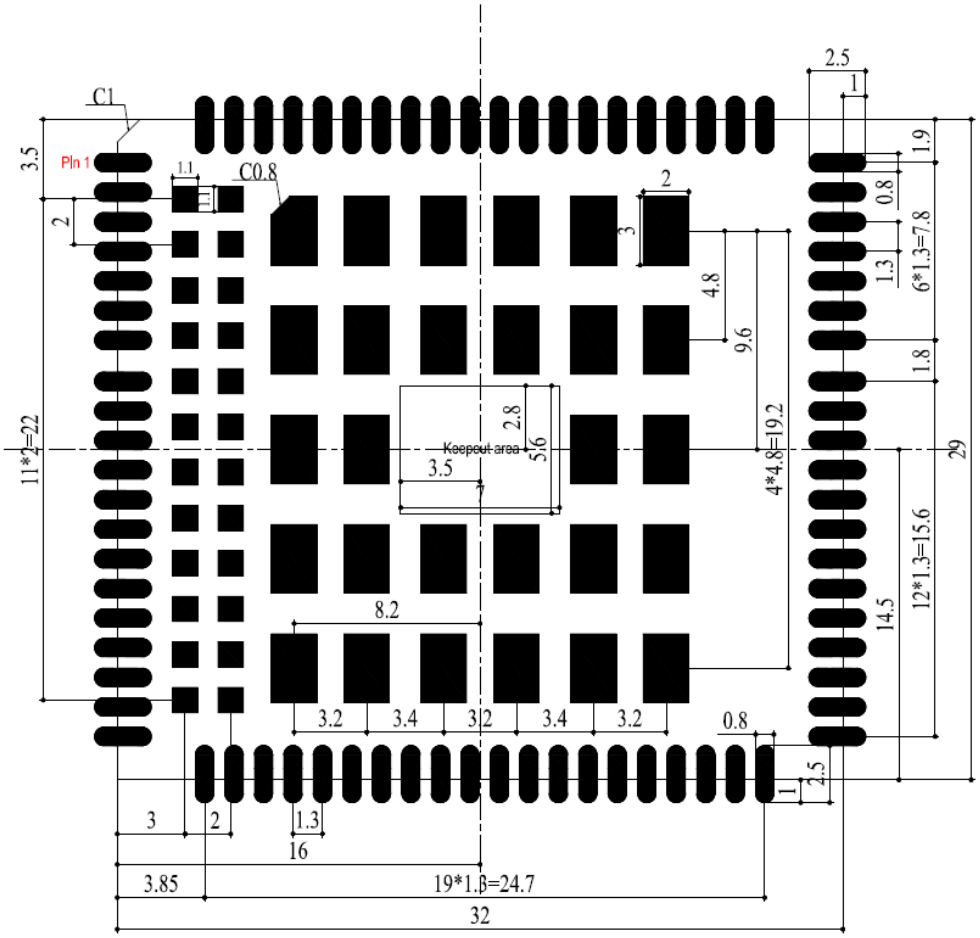


Figure 47: Recommended Compatible Footprint

NOTE

1. The keepout area should not be designed.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
3. LGA form factor is used for EG21-G module, while LCC is recommended only in the compatible design with EC25 series/EC21 series/EC20-CE/EG25-G modules. If you use LCC form factor, you should choose the stencil matched with LGA package instead of that matched with LCC package. For more details, see ***document [8]***.

6.4. Top and Bottom Views

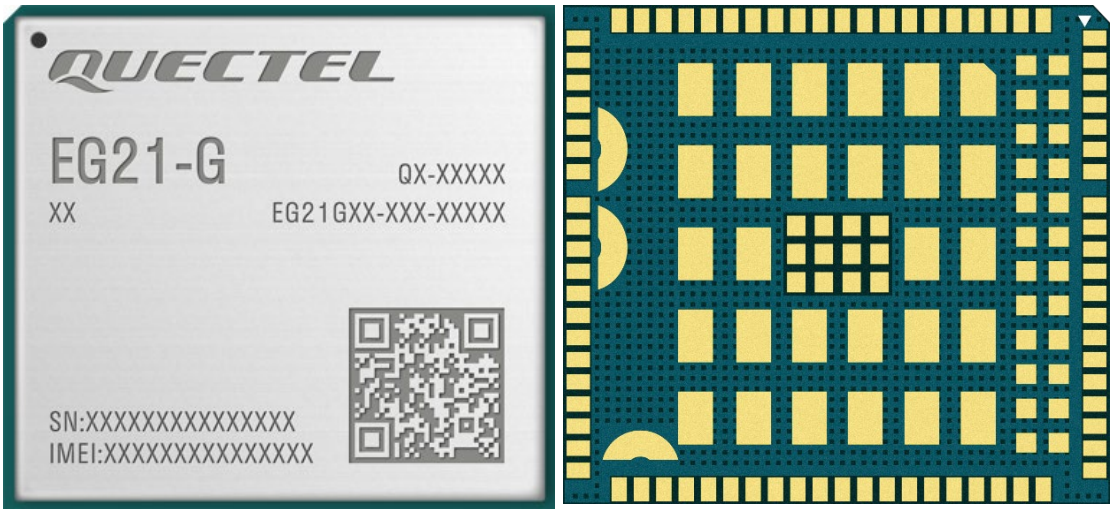


Figure 48: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [9]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

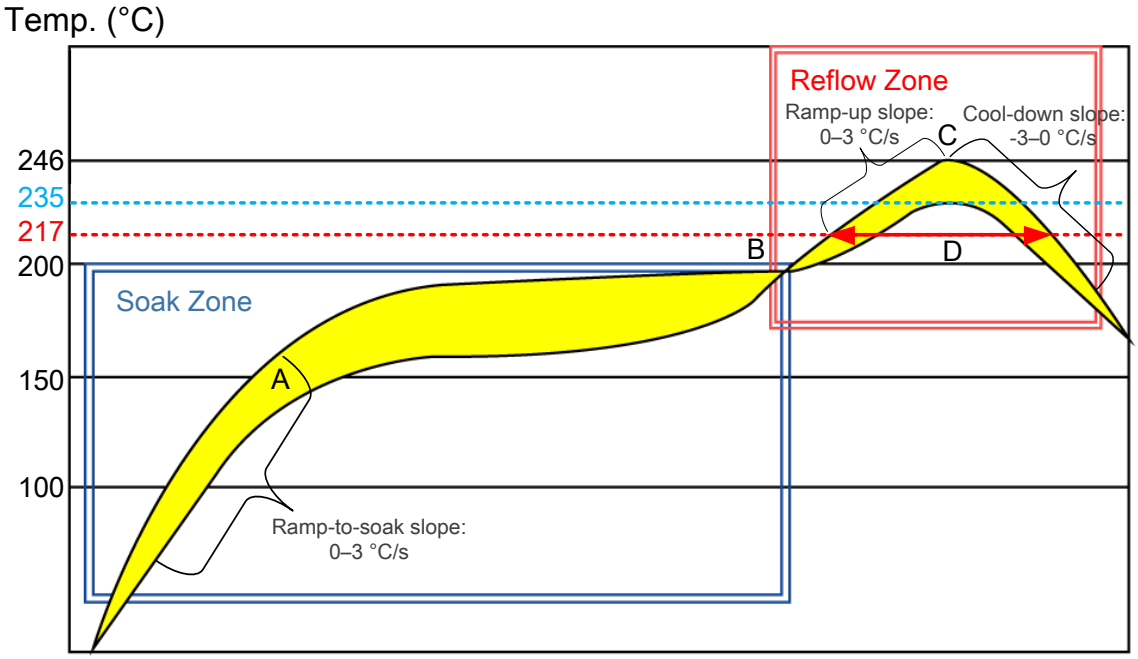


Figure 49: Reflow Soldering Thermal Profile

Table 39: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [8]***.

7.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

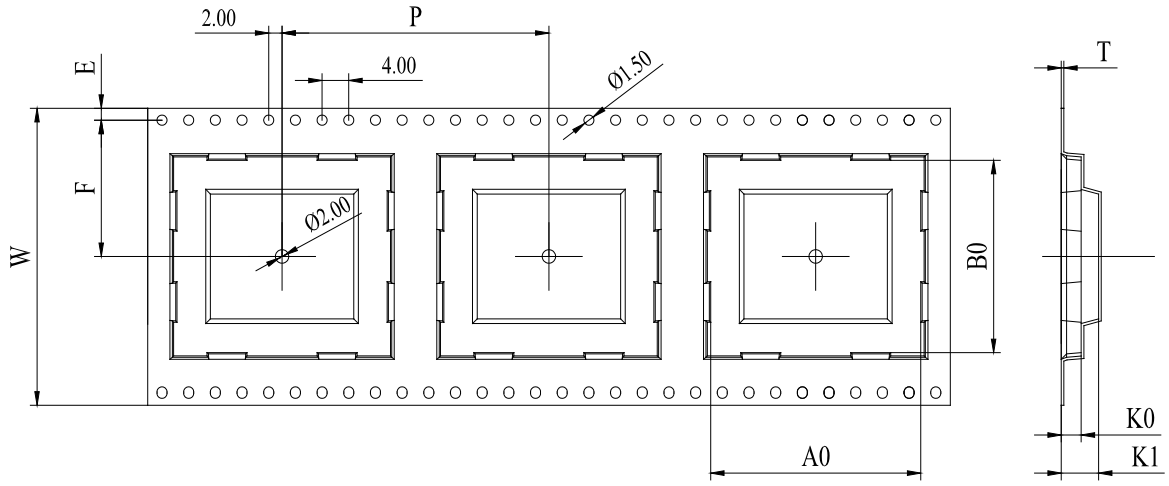


Figure 50: Carrier Tape Dimension Drawing (Unit: mm)

Table 40: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3	3.8	20.2	1.75

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

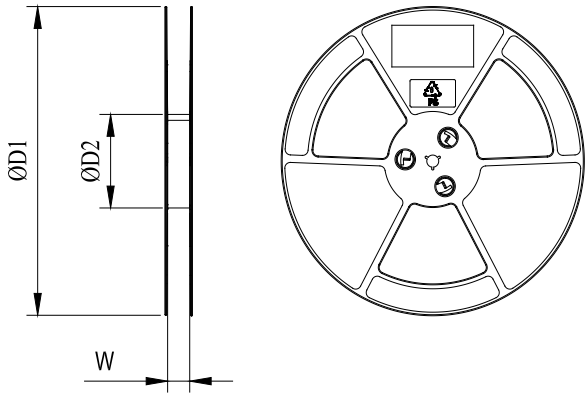


Figure 51: Plastic Reel Dimension Drawing

Table 41: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

7.3.3. Mounting Direction

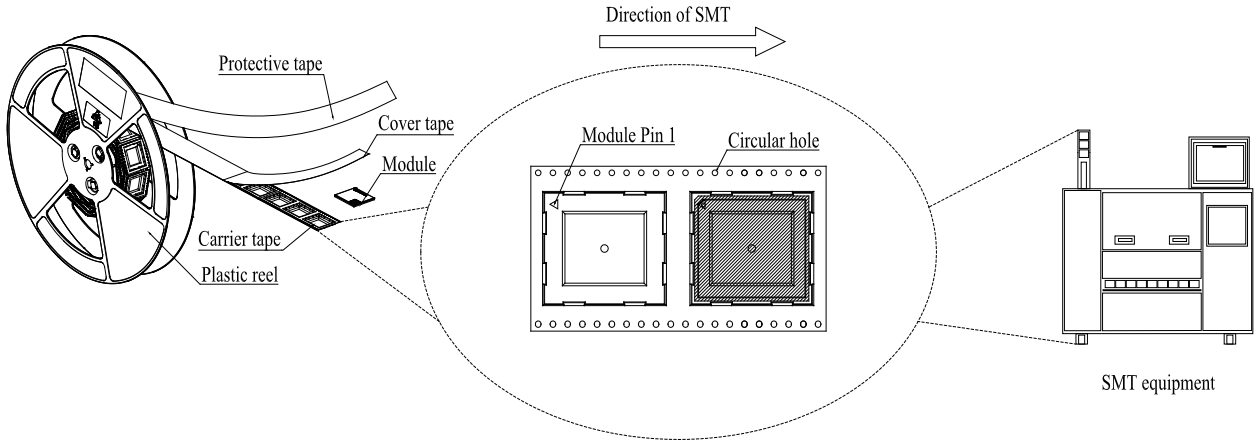
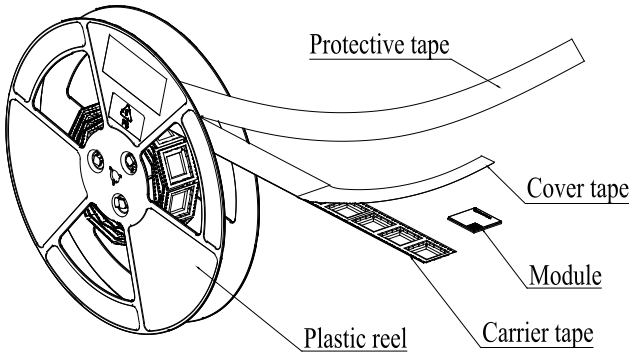


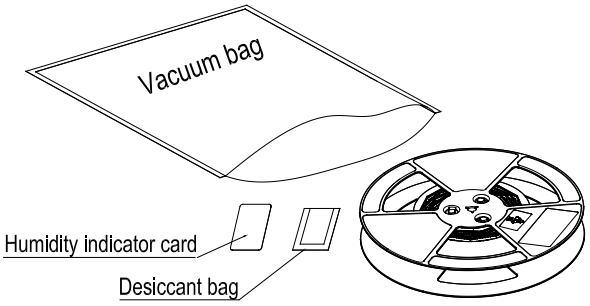
Figure 52: Mounting Direction

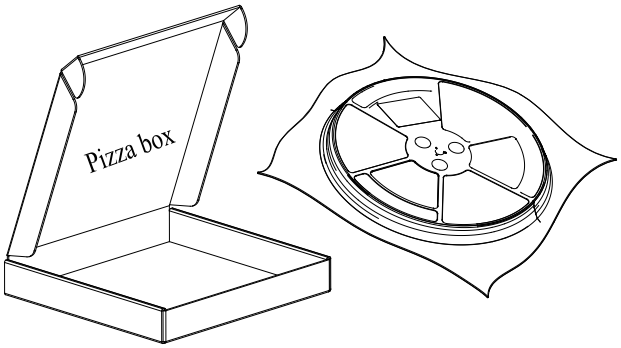
7.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

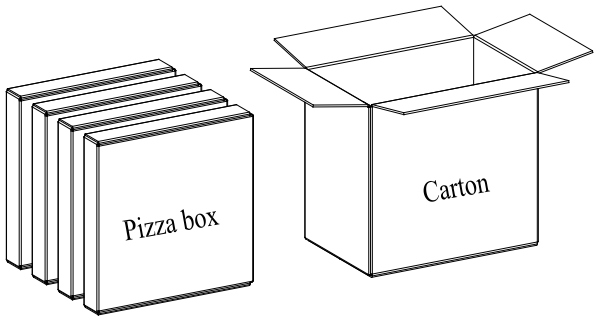


Figure 53: Packaging Process

8 Appendix References

Table 42: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_AT_Commands_Manual
[3] Quectel_EC2x&EG2x&EG9x&EM05_Series_QCFG_AT_Commands_Manual
[4] Quectel_EC2x&EG2x&EG9x&EM05_Series_Low_Power_Mode_Application_Note
[5] Quectel_EC2x&EG2x&EG9x&EM05_Series_GNSS_Application_Note
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_EC2x&EG2x&EG9x&EM05_Series_Software_Thermal_Management_Guide
[8] Quectel_Module_SMT_Application_Note
[9] Quectel_Module_Stencil_Design_Requirements

Table 43: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
Cj	Junction Capacitance
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme

CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MMS	Multimedia Messaging Service
MO	Mobile Originated
MSL	Moisture Sensitivity Level

MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SGMII	Serial Gigabit Media Independent Interface
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VLAN	Virtual Local Area Network
Vmax	Maximum Voltage Value
Vnom	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value

V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access