Project

At KTH University, during the first semester, I took a course regarding Digital Systems Design and Verification using Hardware Description Languages, precisely SystemVerilog. During this course, I was required to work on different designs for different implementations, some of them individually and some in a team. The most complicated and wide project has been implementing a small CPU in a group of three members.

The first step consisted in building the ALU.

The second step consisted in building a register file that would be used to store data in the microprocessor.

The third step consisted in building an FSM that would be used to control the datapath hence fetch and decode instructions. The FSM was supposed to be combined with the ALU and the register file in order to create a microprocessor FSMD.

The last step consisted in designing instruction and data memories and wiring all the pieces up in order to create a complete system.

All of the different steps had to be checked before going to the next one by writing appropriate testbenches that would verify the functionality.

The project put all of my team in front of different challenges. Apart from the ALU and the register file whose design went quite smoothly, the toughest tasks came with the implementation of the FSM as we got different errors in sharing inputs and outputs with the datapath and also in the computation of the next states. Also, the verification of the overall design was quite tedious as we were required to write a proper testbench that would deeply analyse the microprocessor. Nonetheless we managed to finish the design and submit a working and efficient design for our CPU.

For reference on the design and testbench files: https://github.com/davidepanzino/cpu_hdl.git