Cover letter

My name is Davide Finazzi and I studied Electronics Engineering at Politecnico di Milano, Italy, where I got my bachelor's degree in July 2023 with the maximum grade, 110cumLaude. During my bachelor's I had a course about Digital Electronics that introduced me to CMOS digital IC as well as combinational and sequential logic. A great focus was put on learning the language VHDL and in running simulations and generating waveforms by using Xilinx Vivado. During the course we implemented different designs such as PWM modules, FSMs or FIFO buffers. This course was my main motivation for focusing on digital electronics and what led me to choose my current master's program. In Milan I was also enrolled in a module regarding microcontrollers. Here we learnt how to code a microcontroller by the use of its datasheet. We implemented different designs exploiting some peripherals on the board such as timers, ADC and PWM. Right now, I am enrolled at KTH university in Stockholm in the program Embedded Systems on the track of Platforms. The master addresses the problems of designing and assembling an embedded single-/multi-/many-core CPU platform, including VLSI design and embedded software. During the first period I attended a course about digital design and verification using SystemVerilog. The course focused on the HDL and its several features, both for the actual design and the testbench. During the course we were asked to work on different projects, both alone and in team in order to better acquire knowledges. In another course about hardware architectures for deep learning, we also implemented a neuron for a convolutional network to be implemented in hardware and we used the HDL here as well. I am currently following a course about the RTL synthesis, so how to turn the HDL code into a physical chip in a SoC architecture realised as ASIC or FPGA. So far, I have learnt how the Synopsys Design Compiler works and how to compile with both the flat and the bottom-up compiling strategies. We have focused on static time analysis and on optimization strategies. In the following weeks we will focus on the physical design and the Cadence tool.

I do think I would be a great match for this job as I have experience in digital design and verification using HDLs, specifically both SystemVerilog and VHDL.