# Design Project 1: CMOS Image Sensor

TelcomBCN – UPC, DCISE QP09

## 0. Introduction

This exercise addresses the design of a mixed-signal system, including both analog and digital sections. During the first part of the project, the analog part will be developed using design techniques already introduced in previous Exercises. In the second part of the project, the design of the digital part using automatic synthesis will be demonstrated. Finally, the performance of the complete system will be analyzed using mixed-signal simulation.

The design project is based on the circuit explained in detail in the book [Dcise][1], Chap. 7.5. It is **necessary** that you read that section in detail before starting the design of the circuit.

The project Pre-Lab is divided in two parts. The first part addresses the analog section of the system, should be completed before 23rd April, and up-loaded to the Atenea web page. The second part addresses the design of the digital section of the system, should be completed before 10th May, and again uploaded to the Atenea web page. The Lab is done at the laboratory using Cadence tools for schematic capture and simulation. The results of the Lab should be written in a document delivered to the laboratory class professor. The lab section of this exercise should be completed by the end of the semester (1st June).

The evaluation of this final project amounts 2 points of the total qualification of the subject. Note that part of the evaluation of the project will be based on your answers to the Pre-Labs.

For the design of the analog section, technological data for AMS 0.35µm process is required. Such information is found in the Appendix of this document. For the design of the digital section, information of the AMS 0.35µm digital standard cells is required. The information on these cells is found in the datasheets provided by the manufacturer: http://asic.austriamicrosystems.com/databooks/index_c35.html

## 1. System description

The goal of the project is to design a CMOS image sensor for a photographic camera. In order to reduce the circuit size, the sensor will have only 4 pixels (2 rows and 2 columns)[2]. The shutter[3] speed must be selected between 1/8000, 1/4000, 1/2000 and 1/1000[4]. Each pixel in the sensor will include a photodiode which produces a current proportional to the amount of light received. The maximum current provided by the photodiode in conditions of maximum light is 100 nA. Internally, the pixel circuitry converts the current sensed into a voltage. The extreme voltage values will be obtained for the extreme conditions of 0 nA (total darkness), and 100 nA and maximum shutter speed[5]. Optionally, the student may propose techniques to select the ISO sensitivity of the sensor.

The sensor designed will follow the structure of the Active Pixel Sensor (APS) described in the book [Dcise][1], Chap. 7.5. In the first part of the project, you will design the analog part of the sensor, which is essentially described in the book. The control signals (digital) of this analog part will be created with simple `Vpulse` voltage sources. In the second part of the project, the digital circuitry will be added, which will allow generating

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[1] [Dcise] *Diseño de Circuitos y Sistemas Integrados* A. Rubio, J. Altet, X. Aragonés, J.L. González, D. Mateo, F. Moll. Ed. Alfaomega, 2005.

[2] The functionality of a 4 pixels sensor is still representative of a more complex array, which would slow down simulations and make the schematics unnecessarily complex.

[3] Temps d'obturació, tiempo de obturación. Regulates the time during which the sensor is exposed to light. It is measured in seconds (1/500 = 2 ms).

[4] Optionally, the student might add other shutter speeds like 1/500, 1/250, 1/125, 1/60...

[5] This means this is the maximum light level that we want to detect, and will produce the maximum output reading. With this light intensity, slower shutter speeds (or larger diaphragm aperture) will result in the same reading.

the control signals from the inputs of the system (the clock signal, and two bits for the selection of the shutter speed).

The functional sequence of the sensor can be divided in two phases, light acquisition and reading. The acquisition of the light is simultaneously done by all the pixels in the sensor, and is further divided in two phases, pixel reset and light acquisition during the shutter opening time (exposure time). As a result of this phase, each pixel stores a voltage proportional to the amount of light received. Once this acquisition phase is finished, the information stored in each pixel is read sequentially, row after row and, inside each row, column after column. The first row of pixels starts by delivering its stored voltages to the column lines (capacitances), and then these voltages are sequentially read by an analog multiplexer for its A/D conversion. Once all the columns in a row are read, the columns capacitances are initialized (discharged), and the next row of pixels delivers its stored voltages to the column lines. The process is repeated until all the pixels in the sensor are read. The value of the column capacitances in your design is supposed to be $C_{col}$=1 pF.

The following diagram sketches the sequence of actions that take place during the reading of a 4-pixel sensor, including the times specified for each phase, which your design must fulfill:

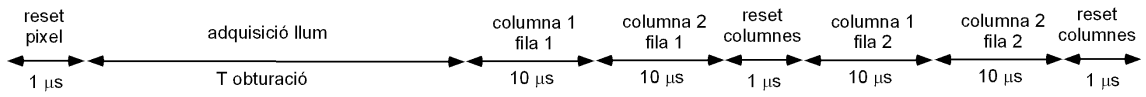


*Fig. 1. Sequence of actions during the reading of a 4-pixel sensor.*

Once this sequence of actions is completed, a new sequence immediately starts. Note that the total time of the sequence is 43 μs+$T_{obturació}$. Also note that the sequence of events in Fig. 1 is not optimized. Some actions in the diagram could be done simultaneously, thus reducing the capture time (increased number of pictures/second). Optionally, the student may propose the optimization of the former sequence, demonstrating the correct functionality of the system.

The final goal of the circuitry is to output a sequence of voltages which have a relationship as linear as possible with the amount of light received by each pixel. The A/D converter will not be included in the circuit to design, and will be just modeled by a 100 fF capacitor connected to the output node.

## 2. Pre-Lab 1

Important note: Neglect the channel-length modulation in all the calculations of this Pre-Lab, λ~0. For the rest of technology parameters, use the tables and expressions that can be found in the Appendix of this document. Always assume that the transistors behave as long-channel (assume that carrier speed saturation is never reached).

1.- Draw the scheme of an active pixel sensor (APS), using the same names for the transistors as those used in the book [Dcise][1]. Identify the variables of the circuit that must be designed. Make a list of inputs and outputs. Draw a symbol for this APS circuit.

2.- Draw the scheme of the complete image sensor (only analog section), where each APS is replaced by its symbol. Also, use a symbol for the analog multiplexer, identifying its inputs and outputs. Identify and list the voltage sources that will be needed to excite all the control inputs of the sensor.

3.- In the APS circuit, transistor M1 has the mission of resetting (precharge) capacitor C. Discuss the voltages that can be reached after this precharge whether a NMOS or a PMOS is used for M1. Include the body effect in your discussion. After your discussion, choose the option that allows the maximum dynamic range (maximum precharge value).

4.- Calculate the minimum voltage allowed in the capacitor, $V_{Fmin}$, in order to guarantee a linear relationship between the voltage in the capacitor ($V_F$) and the voltage in the column line ($V_{col}$). Assume that transistor M5 is biased with a voltage VPN=0.8 V, and $K_3$>>$K_5$. Assume that a transistor working in ohmic region shows a $V_{DS}$ drop of just a few mV.

5.- Calculate the value of capacitor C such that, with the maximum light intensity and maximum shutter speed (1/8000), the APS reaches just its saturation voltage value. Choose as $V_{Fmin}$ the limit value obtained in the former question, plus a safety margin of 200 mV.

6.- Calculate the dimensions of transistor M1 with the following design restrictions:

- Complete precharge of C in less than 1 μs[6]
- Dimensions as small as possible in order to minimize clock-feedthrough[7].
- L=0.35 μm, $W_{min}$=0.4 μm

7.- Calculate the open-circuit voltage of the photodiode, $V_{D\_OC}$, for maximum illumination level.

- Use this model for the photodiode: $I_{PhoDio} = I_S \left( e^{\frac{V_D}{nU_T}} - 1 \right) - I_L$
- $I_S=10^{-15}$; n=0.4; $U_T$ (thermal voltage)=26 mV.

8.- Once the light acquisition phase during $T_{obt}$ has been completed, transistor M2 is switched off. Given that the voltage in the photodiode $V_{D\_OC}$ is not zero, the voltage at the source terminal of M2 will not be zero, but approximately $-V_{D\_OC}$, thus producing a subthreshold current which will discharge the capacitance C during the next phases of the sequence. In this question, you will evaluate the effect of this subthreshold current on the voltage stored in the capacitor.

- Calculate the threshold voltage $V_T$ of an NMOS transistor with the source voltage mentioned above. Use the expressions and technology values that you will find in the Appendix.
- The subthreshold current can be modeled by the expression $I_D = I_{SPEC} e^{\frac{V_{GS}-V_T}{nU_T}}$, where $I_{SPEC} = 2nk' \frac{W}{L} U_T^2$. In these expressions, *n* is a parameter that depends slightly on the technology and that, in subthreshold regime, takes the value 1.45. Calculate the subthreshold current that will flow through M2 in function of its aspect ratio W/L.
- Calculate the variation in the capacitance voltage, $\Delta V_F$, produced by the subthreshold current during a time equal to the reading phase in the sequence of Fig. 1.

9.- Calculate the dimensions of transistor M2 with the following design restrictions:

- Minimize the variation of the capacitance voltage, $\Delta V_F$, produced by the subthreshold current during the reading phase.
- Minimize clock-feedthrough[7]
- L=0.35 μm, $W_{min}$=0.4 μm

10.- Justify the regions of operation of transistors M3 and M4. Calculate the dimensions of transistor M4 with the following criteria:

- Minimize clock-feedthrough[7]
- L=0.35 μm, $W_{min}$=0.4 μm

11.- Calculate the dimensions of transistor M5 with the following design restrictions:

- VPN=0.8 V
- Complete discharge of the column capacitance $C_{col}$ in less than 1 μs [6].
- Minimize the dimensions in order to save area[8].
- L=0.35 μm, $W_{min}$=0.4 μm

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[6] Estimate the charge time as 10τ, where τ is the time constant defined by C and the equivalent resistance Req of the transistor. Estimate Req as the ratio $V_{DS}/I_{DS}$, assuming long-channel behavior, and taking an average value for $V_{DS}$.

[7] Clock feedthrough is a phenomenon of charge injection on $V_F$ when switching M1. This charge injection in undesired because it modifies the voltage $V_F$. Clock feedthrough increases with the parasitic capacitances $C_{GD}$, $C_{GS}$

[8] M3 must be much larger than M5. Dimensions of M5 unnecessarily large may result in an unacceptable area for M3.

12.- Calculate the dimensions of transistor M3 using expression (7.22) from the book [Dcise], such that the term depending on VPN in smaller than $0.1V_T$.

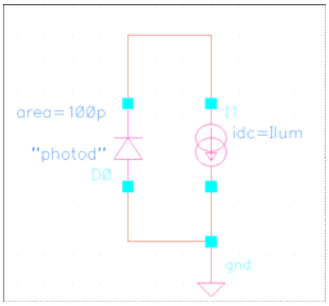
13.- Design the schematic of the analog multiplexer.

14.- Draw a chronogram showing the evolution of the control signals of the 4-pixel analog sensor in order to complete a sequence like that depicted in Fig. 1. (Note that the light levels are not control signals, but input variables of the system).

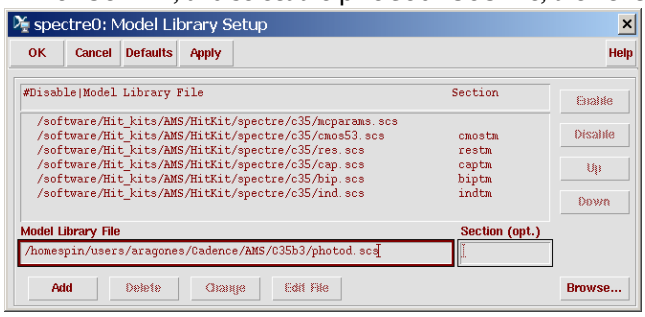
## 3. Lab 1

0.- Instructions to define the photodiode and include its simulation model:

- Copy the files `photod.scs` and `photod.scs.apt` into your working directory.
- In order to emulate the photodiode behavior, you will use a conventional diode in parallel with a DC current source,




- Use the `diode` cell from the `analogLib` library. Model name: `photod`. Device area: `100p`. Junction perimeter factor: `10u`.
- In the `idc` current source, set the DC current value a variable named `Ilum`. You will choose the value of this variable according to the light intensity you want to emulate (100 nA maximum light intensity; 0 nA total darkness).
- Before simulating a circuit that includes this photodiode, you must add the model to the list of model files that are used for the simulation. In the Analog Design Environment window, `Setup` → `Model Libraries...` `Browse...`, and select the `photod.scs` file, then click on `Add` and `OK`.




1.- Obtain the I(V) characteristic curves of the photodiode, for following values of the photogenerated current Ilum: 100 nA; 30 nA; 10 nA; 3 nA; and 1 nA. Measure the open circuit voltage $V_{D\_OC}$ obtained in each case. Verify that the characteristic curves match the expected behavior.

2.- Create the schematic of an Active Pixel Sensor (APS), including at this moment only the photodiode, capacitor C, and transistors M1 and M2. Create a test bench and simulate successive reset and open shutter cycles (two first phases in Fig. 1) and verify the correct functionality. Report the voltage values in the capacitor after each cycle, for different values of `Ilum`, and verify the linearity of the capacitor voltage respect to `Ilum`. Use the cells `cpoly`, `nmos4`, `pmos4` from the `PRIMLIB` library.

3.- Complete now the schematic of the APS with transistors M3 and M4. Generate its symbol. Create a test bench in which the APS output is connected to the column capacitance $C_{col}$ and transistor M5 biased to VPN=0.8 V. Simulate successive cycles of reset, open shutter and row selection, and verify the correct functionality.

4.- Create the schematic of the analog multiplexer, generate its symbol and create a testbench to verify its correct functionality. Remember that the output of the multiplexer must be connected to a capacitance of 100 fF, which emulates the load introduced by the ADC.

5.- Create now the schematic of the complete analog part of the image sensor, including the 4 pixels, 2 column lines, the analog multiplexer and the output load. Create a test bench to verify the correct functionality, setting 4 different Ilum values for the 4 pixels. Verify the correct functionality for different shutter speeds (the same reading should be obtained when doubling the shutter opening time and halving the light value).

6.- Study the linearity of the sensor: Represent graphically $V_F$ (voltage in the pixel capacitance after the time exposure is completed), $V_{col}$ (column voltage) and $V_{out}$ in function of Ilum, at least for the 5 Ilum values specified in question 1. Calculate the sensitivity of the sensor and quantify its linearity (maximum deviation from the average sensitivity).

Optional improvements:

- Improve the linearity by canceling the body effect in M3 (force Bulk=Source).
- Optimize the dynamic range (try lowering VPN).
- Optimize the acquisition sequence (only analog part of the sensor)
- Introduce controllable ISO sensitivity (only analog part of the sensor)
- Increase the number of pixels (only analog part of the sensor)
- Report the power consumption of the analog and digital parts of the sensor.
- Report the power consumption of the digital part if $V_{dd}$ is reduced to half its original value.
- Which modifications should be necessary in the analog part of the sensor if $V_{dd}$ was reduced to half its original value?
- Report the power consumption of the complete circuitry if $V_{dd}$ is reduced to half its original value.
- Include the A/D conversion and show its correct functionality.

# Appendix: Technology data

## *A.1 Transistor data.*

All this data is approximate. It is intended to allow hand calculation with Sah equations. The actual model parameters used by the simulator are not exactly the same since more second order effects need to be considered. However, hand calculations using this data provide a good enough approximation for simulation results, especially in saturation region.

| Parameter | Units | NMOS | PMOS | note |
|---|---|---|---|---|
| $L_{min}$ | µm | 0.35 | 0.35 | |
| $W_{min}$ | µm | 0.35 | 0.35 | |
| $t_{ox}$ | nm | 7.6 | 7.6 | |
| $V_{TH0}$ | V | 0.5 | -0.65 | 1 |
| $\gamma$ | $V^{0.5}$ | 0.58 | -0.40 | 1 |
| NSUB | $10^{15}/cm^3$ | 212 | 101 | 1 |
| K’ | $A/V^2$ | $80\cdot10^{-6}$ | $26\cdot10^{-6}$ | 2 |
| $\lambda$ | $V^{-1}$ | 0.08 | -0.08 | 3 |
| LD | µm | 0.01 | 0.01 | 4 |
| WD | µm | 0.05 | 0.05 | 5 |
| $\mu_o$ | $cm^2/Vs$ | 370 | 126 | 6 |

**Notes:**

1 Body effect: use the following equation:

$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi - V_{BS}} - \sqrt{2\phi}\right)$, where $V_{BS}$ is the bulk-to-substrate voltage and $\phi$ is the substrate potential, calculated using the NSUB parameter (the doping concentration of the substrate):

$\phi = \frac{kT}{q}\ln\left(\frac{NSUB}{n_i}\right)$, with $kT/q$ = 26 mV at 300ºK and $n_i = 1.5\cdot10^{10}$ $cm^{-3}$ at 300ºK for silicon.

2 Gain parameter

This parameter is used in the current expression:

$$I_D = K'\frac{W_{eff}}{L_{eff}}\left(\left(V_{GS} - V_{TH}\right)V_{min} - \frac{V_{min}^2}{2}\right),\ \text{with } V_{min} = \min\left\{\left(V_{GS} - V_{TH}\right), V_{DS}\right\}$$

3 Channel length modulation

The limitations of the simple Sah model makes this parameter value to be not very accurate. The student is warned to take the results obtained using this parameter only as approximate values. It is used to correct the current expression in the saturation region:

$$I_{DSAT} = \frac{K'}{2}\frac{W_{eff}}{L_{eff}}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right)$$

4 The effective channel length is calculated using the following expression:

$$L_{eff} = L - 2\cdot LD$$

5 The effective channel width is calculated using the following expression:

$$W_{eff} = W - 2 \cdot WD$$

6 Carrier's mobility in the channel may be used to obtain a first-hand value for the saturation $V_{DS}$ due to carrier's velocity saturation (short-channel behavior):

$$V_{DSsat} = v_{sat} \frac{L_{eff}}{\mu_o}$$, with $v_{sat} \sim 10^5$ m/s