CHAPTER 13 RESET FUNCTION

When a low pulse is input to the $\overline{\text{RESET}}$ input pin, the system is reset and the hardware devices are placed in the state listed in Table 13-1. When the low-to-high transition of the $\overline{\text{RESET}}$ input is made, the reset state is released and program execution is started. Initialize the register contents within the program as required.

Table 13-1. Hardware States after Reset (1/2)

Hardware (symbol)			Address[Note] (Low-order 12 bits: xx□□□H)	State after reset
Program counter		PC	—	0000H
Program status word		PSW	—	F002H
On-chip RAM	Data memory	—	—	Undefined
	General purpose registers	AW, CW, DW, BW, SP, BP, IX, IY	EFEH-EF0H	Undefined
	Segment registers (bank 7 only)	DS1, SS, DS0	EEEH, EEAH, EE8H	0000H
		PS	EECH	FFFFH
Ports	Port registers	P0, P1, P2	F00H, F08H, F10H	Undefined
		PT	F38H	
	Port mode registers	PM0, PM1, PM2	F01H, F09H, F11H	FFH
		PMT	F3BH	00H
	Port mode control registers	PMC0, PMC1, PMC2	F02H, F0AH, F12H	00H
Timer unit	Timer registers	TM0, TM1	F80H, F88H	Undefined
	Modulo/timer registers	MD0, MD1	F82H, F8AH	Undefined
	Timer control registers	TMC0, TMC1	F90H, F91H	00H
	Interrupt request control registers	TMIC0-TMIC2	F9CH-F9EH	47H
	Macro service control registers	TMMS0-TMMS2	F94H-F96H	Undefined
DMA controller	DMA mode registers	DMAM0, DMAM1	FA1H, FA3H	00H
	DMA control registers	DMAC0, DMAC1	FA0H, FA2H	Undefined
	Interrupt request control registers	DIC0, DIC1	FACH, FADH	47H
Source address pointer		SAR0L, SAR0M, SAR0H, SAR1L, SAR1M, SAR1H,	FC0H, FC1H, FC2H FD0H, FD1H, FD2H,	Undefined
Destination address pointer		DAR0L, DAR0M, DAR0H, DAR1L, DAR1M, DAR1H,	FC4H, FC5H, FC6H, FD4H, FD5H, FD6H,	Undefined
Terminal counter		TC0L, TC0H, TC1L, TC1H,	FC8H, FC9H, FD8H, FD9H,	Undefined

Note xx in the high-order eight bits of an address is a value specified in the IDB register.

Table 13-1. Hardware States after Reset (2/2)

Hardware (symbol)			Address[Note 1] (Low-order 12 bits: xx□□H)	State after reset
Serial interface	Serial mode registers	SCM0, SCM1	F68H, F78H	00H
	Serial control registers	SCC0, SCC1	F69H, F79H	00H
	Baud rate generator	BRG0, BRG1	F6AH, F7AH	00H
	Receive buffer registers	RxB0, RxB1	F60H, F70H	Undefined
	Transmit buffer registers	TxB0, TxB1	F62H, F72H	Undefined
	Serial status registers	SCS0, SCS1	F6BH, F7BH	60H
	Interrupt request control registers	(Error) SEIC0, SEIC1	F6CH, F7CH	47H
		(Reception) SRIC0, SRIC1	F6DH, F7DH	
		(Transmission) STIC0, STIC1	F6EH, F7EH	
	Macro service control registers	(Reception) SRMS0, SRMS1	F65H, F75H	Undefined
		(Transmission) STMS0, STMS1	F66H, F76H	
Timer base interrupt request control register		TBIC	FECH	47H
User flag register		FLAG	FEAH	00H
Internal data area base register		IDB	FFFH	FFH
Processor control register		PRC	FEBH	4EH
Wait control register		WTC	FE8H	FFFFH
Refresh mode register		RFM	FE1H	FCH
Standby control register		STBC	FE0H	Retention[Note 2]
External interrupt	External interrupt mode register	INTM	F40H	00H
	Interrupt request control registers	EXIC0-EXIC2	F4CH-F4EH	47H
	Macro service control register	EMS0-EMS2	F44H-F46H	Undefined
Interrupt source register		IRQS	FEFH	Undefined
Interrupt priority register		ISPR	FFCH	00H

Notes 1. xx in the high-order eight bits of an address is a value specified in the IDB register.

    2. After power on reset: 00H