CHAPTER 5 BUS CONTROL

The µPD70325 and 70335 have the bus control pins listed in parts (a) and (b) of Table 5-1.

When using the functions of the shared pins, the desired function must be selected by setting the port mode control register (PMCn).

Table 5-1. Bus Control Pin Functions

(a) µPD70325

Pin name	I/O	Function	Remark
A0-A19	O	Address bus	
D0-D7	I/O	Data bus	
R/$\overline{\text{W}}$	O	Read/write identification	
$\overline{\text{MREQ}}$	O	Indicates memory cycle	
$\overline{\text{MSTB}}$	O	Memory read/memory write strobe signal	
$\overline{\text{IOSTB}}$	O	I/O cycle strobe signal	
$\overline{\text{REFRQ}}$	O	Indicates memory refresh cycle	
HLDRQ	I	Bus hold request signal	Also used for P27
$\overline{\text{HLDAK}}$	O	Bus hold acknowledge signal	Also used for P26
DMARQ0	I	DMA request signal	Also used for P20
DMARQ1	I	DMA request signal	Also used for P23
$\overline{\text{DMAAK0}}$	O	Indicates DMA acknowledge cycle	Also used for P21
$\overline{\text{DMAAK1}}$	O	Indicates DMA acknowledge cycle	Also used for P24
READY	I	Wait insertion in bus cycle from external source	Also used for P17
$\overline{\text{INTAK}}$	O	Indicates interrupt acknowledge cycle	Also used for P13 and $\overline{\text{INTP2}}$

The µPD70325's $\overline{\text{MSTB}}$ signal becomes active 1/2 clock cycles behind the $\overline{\text{MREQ}}$ signal and becomes inactive simultaneously with the $\overline{\text{MREQ}}$ signal. When generating a memory access signal, using the $\overline{\text{MREQ}}$ signal instead of the $\overline{\text{MSTB}}$ signal enables the memory access signal to become active 1/2 clock cycles faster.
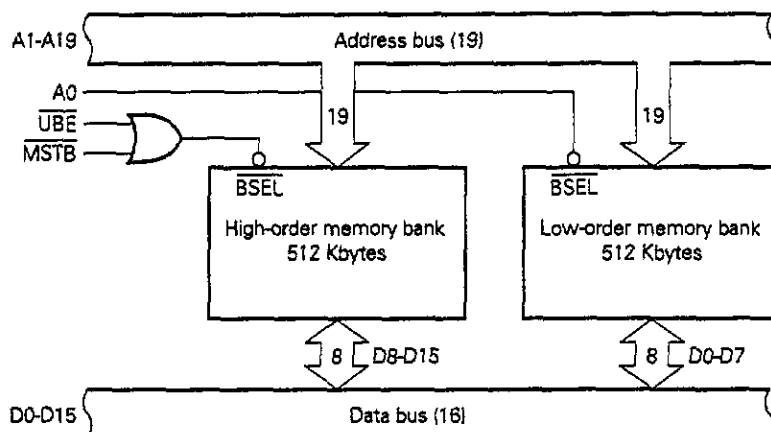
(b) μPD70335

Pin name	I/O	Function	Remark
A0	O	Used for address LSB output and low-order memory bank selection	
A9/A1-A16/A8, A17/A18,A19	O	19-bit address output by multiplexing	
A18/ŪBE	O	Address bit 18 output and high-order memory bank selection signal output by multiplexing	
D0-D15	I/O	Data bus	
R/W̄	O	Read/write identification	
M̄R̄ĒQ̄	O	Indicates that a bus cycle has started. High-order address strobe signal	
M̄S̄T̄B̄	O	Memory read/memory write strobe signal. Low-order address strobe signal	
ĪŌS̄T̄B̄	O	I/O cycle strobe signal. Low-order address strobe signal	
R̄ĒFRQ	O	Indicates memory refresh cycle	
HLDRQ	I	Bus hold request signal	Also used for P27
H̄L̄D̄ĀK̄	O	Bus hold acknowledge signal	Also used for P26
DMARQ0	I	DMA request signal	Also used for P20
DMARQ1	I	DMA request signal	Also used for P23
D̄M̄ĀĀK̄0	O	Indicates DMA acknowledge cycle	Also used for P21
D̄M̄ĀĀK̄1	O	Indicates DMA acknowledge cycle	Also used for P24
READY	I	Wait insertion in bus cycle from external source	Also used for P17
ĪN̄T̄ĀK̄	O	Indicates interrupt acknowledge cycle	Also used for P13 and ĪN̄T̄P̄2

Because the μPD70335 manages the memory addresses for each byte and has a 16-bit external data bus, memory is separated into high-order and low-order banks for connection. Figure 5-1 shows an outline of the memory bank structure.

The high-order 19 bits (all except A0) of physical addresses are input to the memory address pins of each of the high-order and low-order banks. The A0 signal is used to select the low-order memory banks, and the A18/ŪBE signal is used to select the high-order memory bank.

Figure 5-1. Memory Bank Structure

The μPD70335's memory cycle consists of three states—T1, T2, and T3 (see section **5.5 Bus Timings**).

In the T1 state, the first address (high-order address) of a 20-bit address is output onto the external address bus. In the T2 state, the second address (low-order address) of a 20-bit address is output onto the external address bus. In the T3 state, data is read and written.

Wait state TW is inserted between the T2 and T3 states of a read cycle. It is inserted between the T1 and T2 states of a write cycle.

From the T1 state to the T3 state, the least significant bit of a physical address is output from the A0 pin. From the A18/$\overline{UBE}$ pin, the 18th bit of a physical address is output in the T1 state, and the $\overline{UBE}$ signal is output in the state following the T1 state.

Table 5-2 describes the relationship between the A0 and $\overline{UBE}$ signals.

Table 5-2. μPD70335 Data Access

Access	$\overline{UBE}$	A0	Number of bus cycles
Word at even address	0	0	1
Word at odd address	0	1	2
	1	0	
Byte at even address	1	0	1
Byte at odd address	0	1	1

The I/O read/write cycle timing is the same as the memory read/write cycle timing except that $\overline{IOSTB}$ rather than $\overline{MSTB}$ is activated.

In a memory refresh cycle, the $\overline{MREQ}$ and $\overline{MSTB}$ signals are inactive.

To access the external memory or I/O, the μPD70335 outputs a 20-bit physical address from a total of 12 pins (11 address pins and the A18/$\overline{UBE}$ pin) in time-division multiplexing, as listed in Table 5-3.

Table 5-3. Address Time-Division Multiplexing Output

Pin name	Memory cycle		I/O cycle		Refresh cycle
	First	Second	First	Second	
A0	A0	A0	A0	A0	"0"
A9/A1	A9	A1	A9	A1	A0
A10/A2	A10	A2	A10	A2	A1
A11/A3	A11	A3	A11	A3	A2
A12/A4	A12	A4	A12	A4	A3
A13/A5	A13	A5	A13	A5	A4
A14/A6	A14	A6	A14	A6	A5
A15/A7	A15	A7	A15	A7	A6
A16/A8	A16	A8	"0"	A8	A7
A17/A18	A17	A18	"0"	"0"	A8
A19	A19	A19	"0"	"0"	"0"
A18/$\overline{\text{UBE}}$	A18	$\overline{\text{UBE}}$	"0"	$\overline{\text{UBE}}$	"0"
$\overline{\text{REFRQ}}$	"1"	"1"	"1"	"1"	"0"

5.1 Programmable Wait Function

For the μPD70325 and 70335, wait state insertion in a bus cycle (except a memory refresh cycle) can be specified by software. It is specified for each of the eight 128-Kbyte blocks of the 1-Mbyte memory space and the I/O space by setting the wait control register (WTC) as shown in Figure 5-2. However, the same value is set for memory space block 6 (C0000H to DFFFFH) and block 7 (E0000H to FFFFFH).

Wait state specification can be selected among four types listed in Table 5-4 as desired for each block. When READY pin control is used, port 1 mode control register (PCM1) bit 7 must be set to 1 because the READY pin is also used for P17. When PMC1 bit 7 is set to 0, the READY state is always set; that is, two wait states are specified. When READY pin control is selected, two wait states of TAW are inserted regardless of the READY pin state. The READY pin is sensed by its level. Wait states are inserted when the pin is low.

Access to the internal data area is not affected by the programmable wait function. These settings are applied to all external area access except for memory refresh.

When $\overline{\text{RESET}}$ is input, the WTC register contents are initialized to FFFFH.
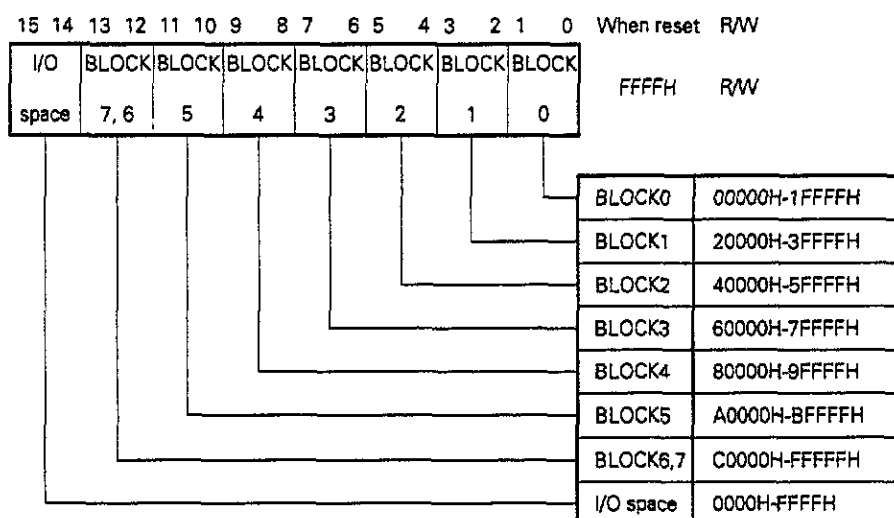
Figure 5-2. WTC

Table 5-4. Wait State Settings

BLOCKn, I/O space	Wait state
00	0 states
01	1 state
10	2 states
11	2 states + inserted state(s) depending on READY pin

When wait control with the READY pin is selected in the wait control register (WTC), the CPU in the μPD70325 or 70335 automatically inserts two wait states (TAWs), as described below. Figure 5-3 shows the wait for the READY pin in the μPD70325 and Figure 5-4 shows the wait for the READY pin in the μPD70335.

μPD70325: between T1 and T2 states
μPD70335: between T2 and T3 states

The μPD70325 and 70335 sample the READY pin state in the first TAW. At that time, wait state (TW) insertion is enabled or disabled depending on the READY pin's state.

(1) When READY pin is high

This disables wait state (TW) insertion after the automatically inserted TAW. Only set the READY pin high when disabling wait state insertion; otherwise, set it low.

(2) When READY pin is low

This adds wait states (TW) after the automatically inserted TAW. TW is inserted as many times as the READY pin is sampled when low. If the READY pin is high during the first TAW, a READY wait state (TW) will not be inserted afterward even if the next TAW is low.

The μPD70325 and μPD70335 differ in their output timing of control signals $\overline{MREQ}$, $\overline{MSTB}$, and $\overline{IOSTB}$. The READY signal timing in these products is defined as follows.

μPD70325: During the memory read/write cycle, it is defined by the $\overline{MREQ}$ signal.
         During the I/O read/write cycle, it is defined by the $\overline{IOSTB}$ signal.
μPD70335: During the memory read/write cycle[Note], it is defined by the $\overline{MREQ}$ signal.
         During the I/O read/write cycle, it is defined by the $\overline{MREQ}$ and $\overline{IOSTB}$ signals.

Note In the μPD70335, the memory read cycle and memory write cycle use different $\overline{MSTB}$ output timing.

Caution **No refresh cycle is inserted in the wait state. Accordingly, when the DRAM is refreshed using the refresh function, if the wait state is prolonged, refresh is not executed at that time and the DRAM contents may not be retained.**

Figure 5-3.   Wait via READY Pin (μPD70325) (1/8)

(a)   No addition of wait state to memory read cycle
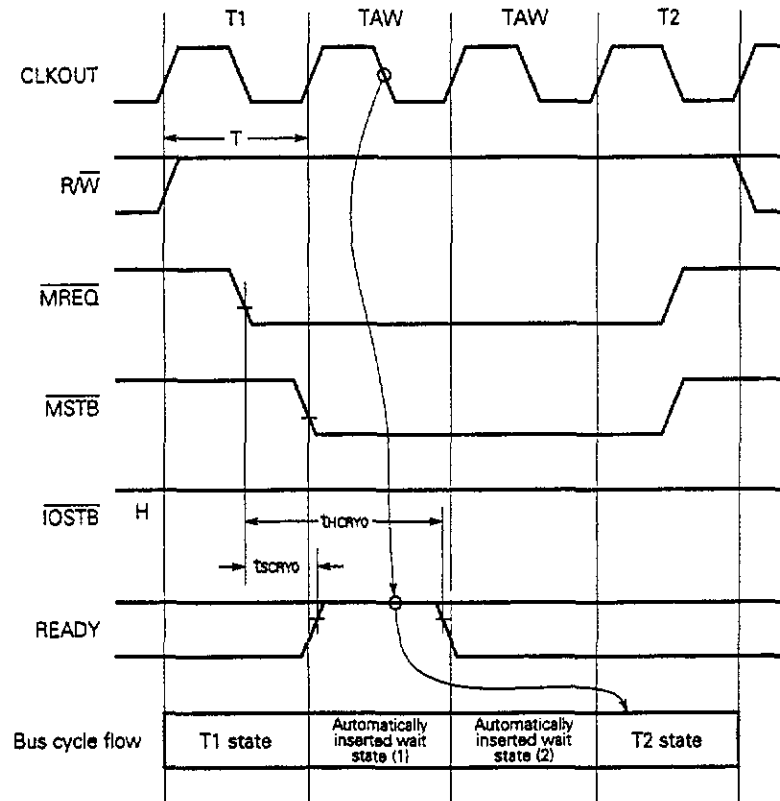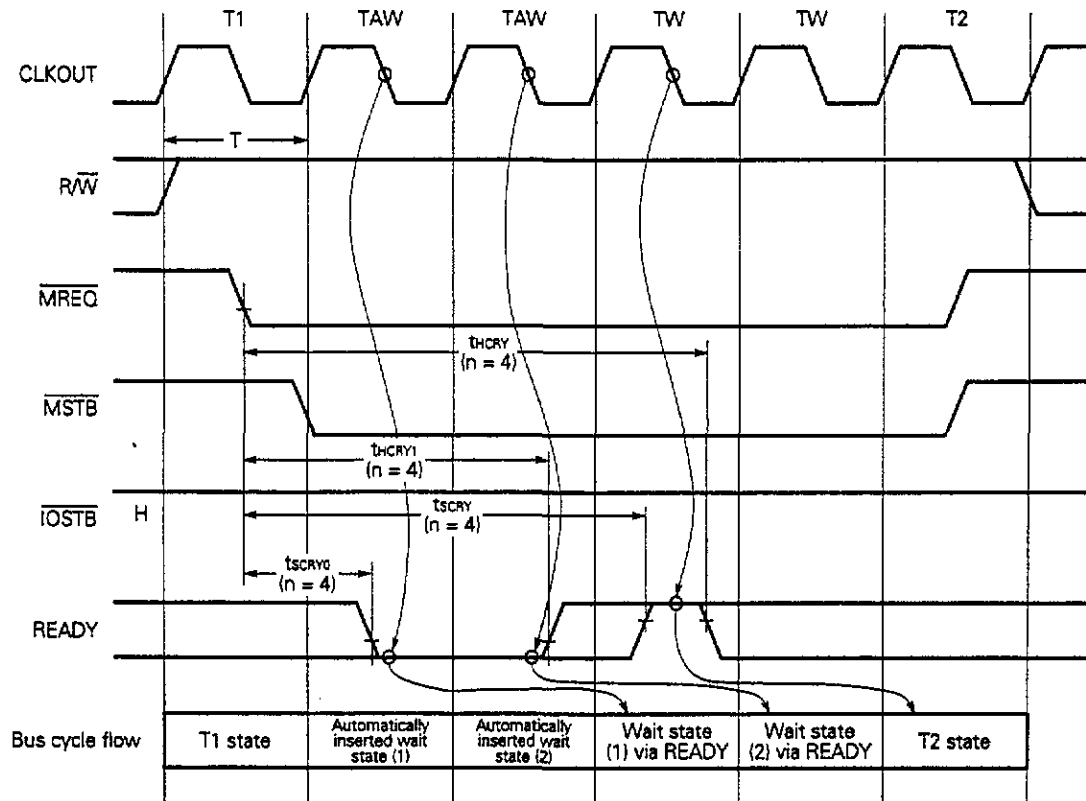

When operation frequency is 10 MHz

T=100 ns

$t_{SCRYO}=T - 80(Max.)=20$ ns

$t_{HCRYO}=T(Min.)=100$ ns

Figure 5-3. Wait via READY Pin (μPD70325) (2/8)

(b) Addition of two wait states to memory read cycle

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

t_{SCRY0}=T – 80(Max.)=20 ns

t_{HCRY1}= (n – 2)T(Min.)=200 ns

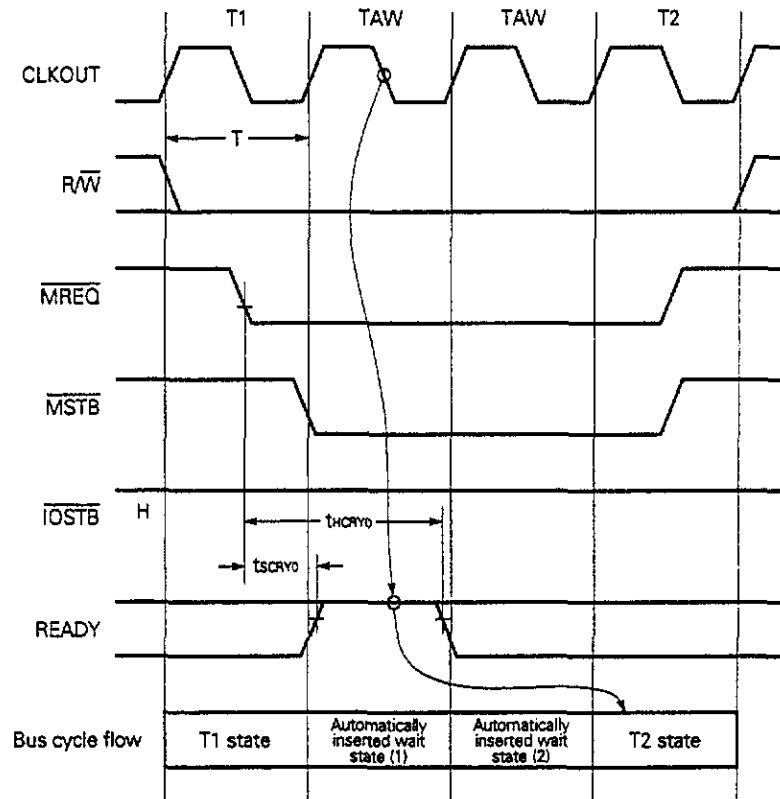t_{SCRY}=(n – 1)T – 80(Max.)=220 ns

t_{HCRY}=(n – 1)T(Min.)=300 ns

Figure 5-3. Wait via READY Pin (μPD70325) (3/8)

(c) No addition of wait state to memory write cycle

Bus cycle flow	T1 state	Automatically inserted wait state (1)	Automatically inserted wait state (2)	T2 state

When operation frequency is 10 MHz

T=100 ns

$t_{SCRYO}=T - 80(Max.)=20$ ns

$t_{HCRYO}=T(Min.)=100$ ns

Figure 5-3. Wait via READY Pin (μPD70325) (4/8)

(d) Addition of two wait states to memory write cycle
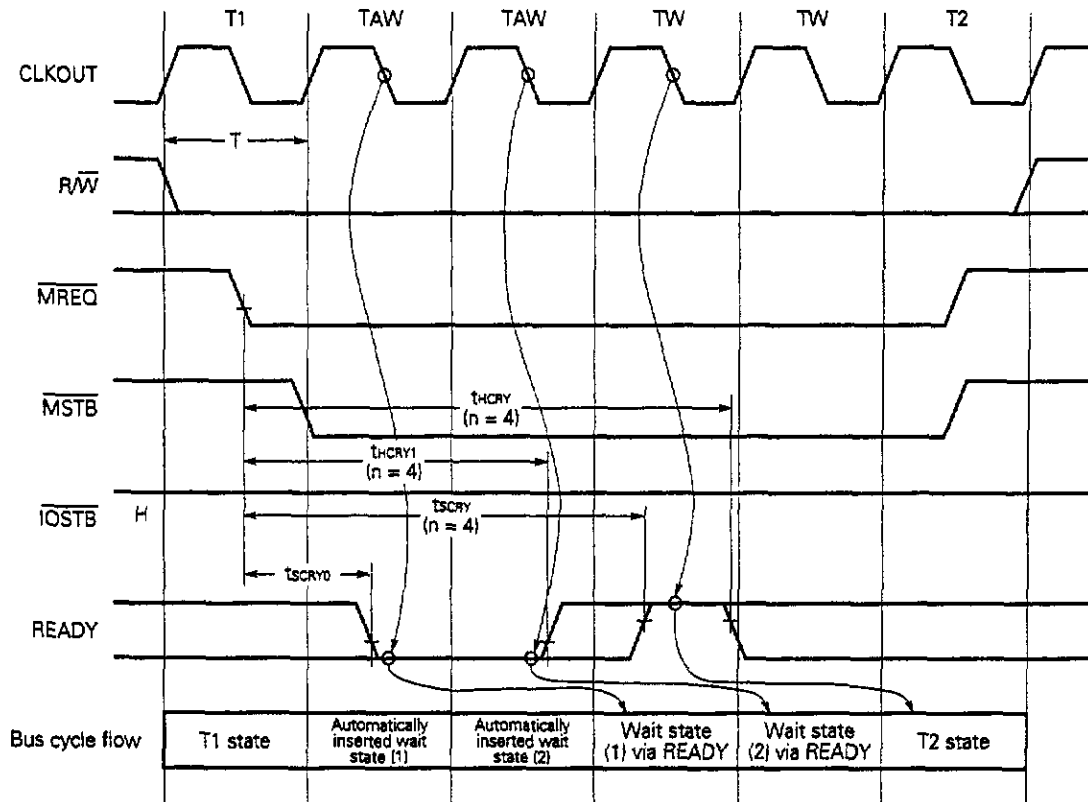

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

t_{SCRY0}=T − 80(Max.)=20 ns
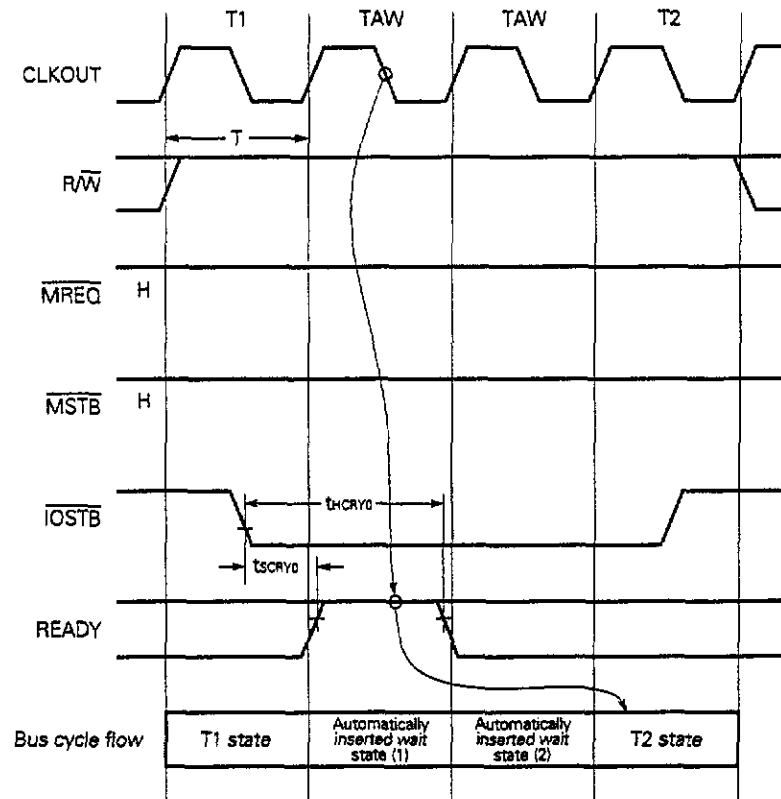
t_{HCRY1}=(n − 2)T(Min.)=200 ns

t_{SCRY}=(n − 1)T − 80(Max.)=220 ns

t_{HCRY}=(n − 1)T(Min.)=300 ns

Figure 5-3. Wait via READY Pin (μPD70325) (5/8)

(e) No addition of wait state to I/O read cycle

When operation frequency is 10 MHz

T=100 ns

t_{SCRYO}=T – 80(Max.)=20 ns

t_{HCRYO}=T(Min.)=100 ns

Figure 5-3. Wait via READY Pin (μPD70325) (6/8)

(f) Addition of two wait states to I/O read cycle
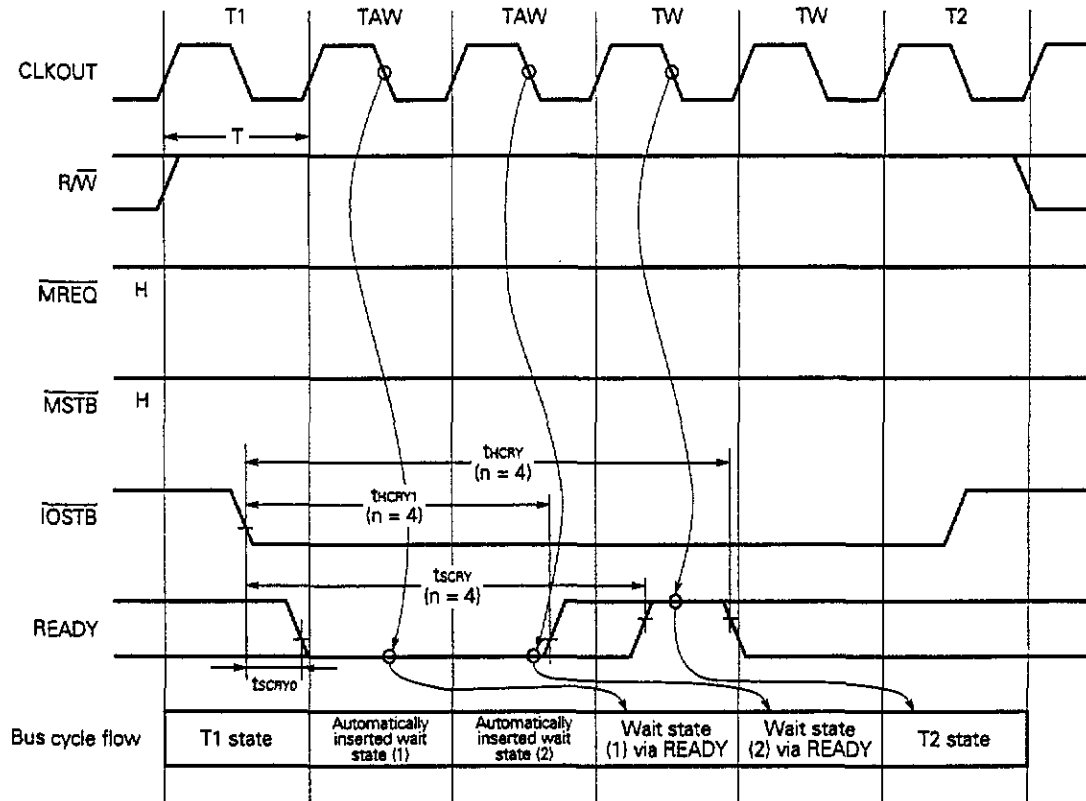

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

t_{SCRY0}=T − 80(Max.)=20 ns

t_{HCRY1}=(n − 2)T(Min.)=200 ns

t_{SCRY}=(n − 1)T − 80(Max.)=220 ns

t_{HCRY}=(n − 1)T(Min.)=300 ns

Figure 5-3. Wait via READY Pin (μPD70325) (7/8)

(g) No addition of wait state to I/O write cycle

When operation frequency is 10 MHz

T=100 ns

$t_{SCRYO}=T - 80(Max.)=20$ ns

$t_{HCRYO}=T(Min.)=120$ ns

Figure 5-3. Wait via READY Pin (μPD70325) (8/8)

(h) Addition of two wait states to I/O write cycle

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

$t_{SCRY0}=T - 80(Max.)=20$ ns

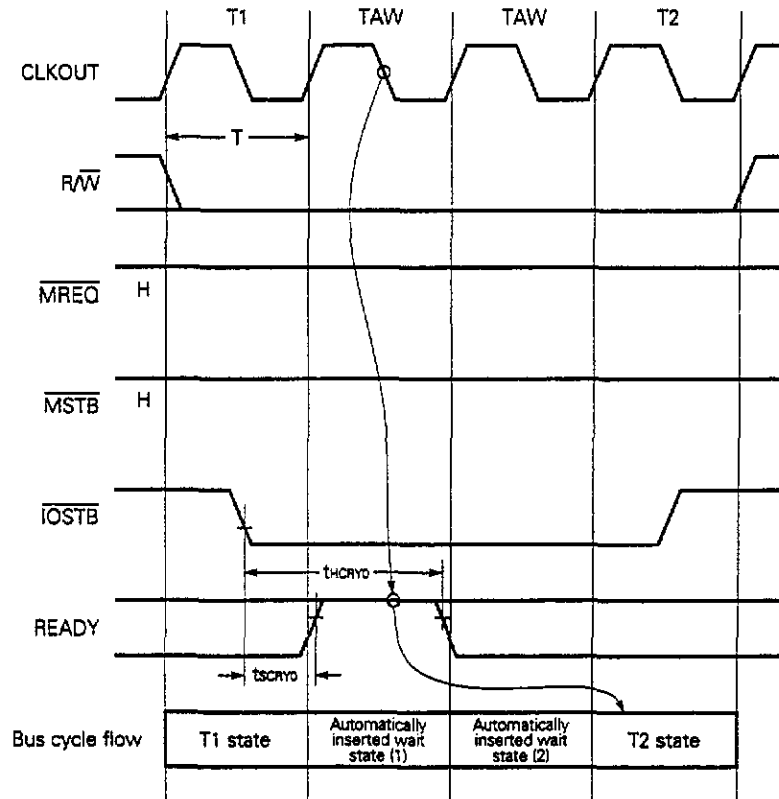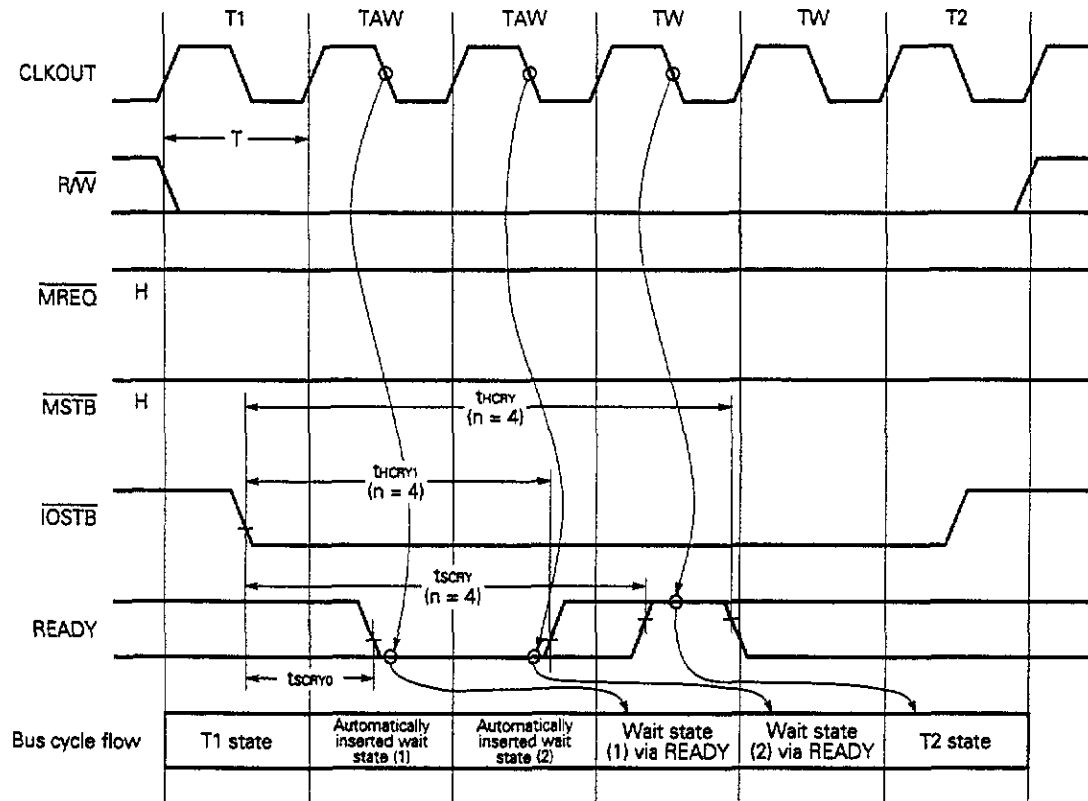$t_{HCRY1}=(n - 2)T(Min.)=200$ ns

$t_{SCRY}=(n - 1)T - 80(Max.)=220$ ns

$t_{HCRY}=(n - 1)T(Min.)=300$ ns

Figure 5-4. Wait via READY Pin (μPD70335) (1/8)

(a) No addition of wait state to memory read cycle

When operation frequency is 10 MHz
T=100 ns
tscRYo=2T – 80(Max.)=120 ns
tHCRYo=2T(Min.)=200 ns

Figure 5-4. Wait via READY Pin (μPD70335) (2/8)

(b) Addition of two wait states to memory read cycle

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

$t_{SCRY0}=2T - 80(Max.)=120$ ns
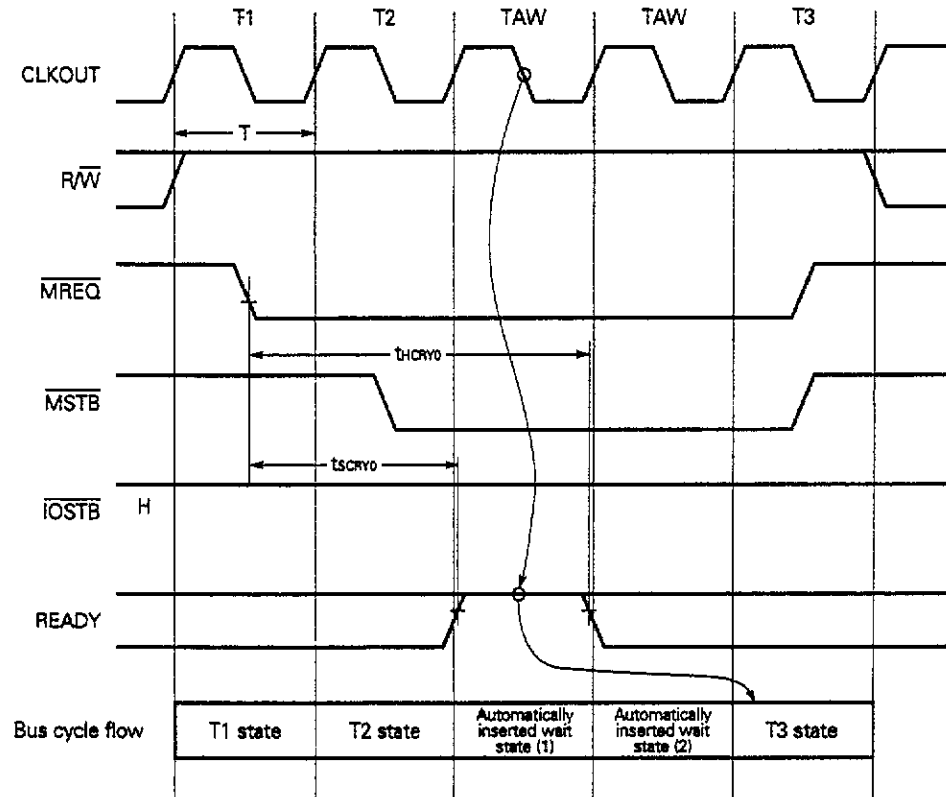
$t_{HCRY1}=(n - 1)T(Min.)=300$ ns

$t_{SCRY}=nT - 80(Max.)=320$ ns

$t_{HCRY}=nT(Min.)=400$ ns

Figure 5-4. Wait via READY Pin (μPD70335) (3/8)

(c) No addition of wait state to memory write cycle
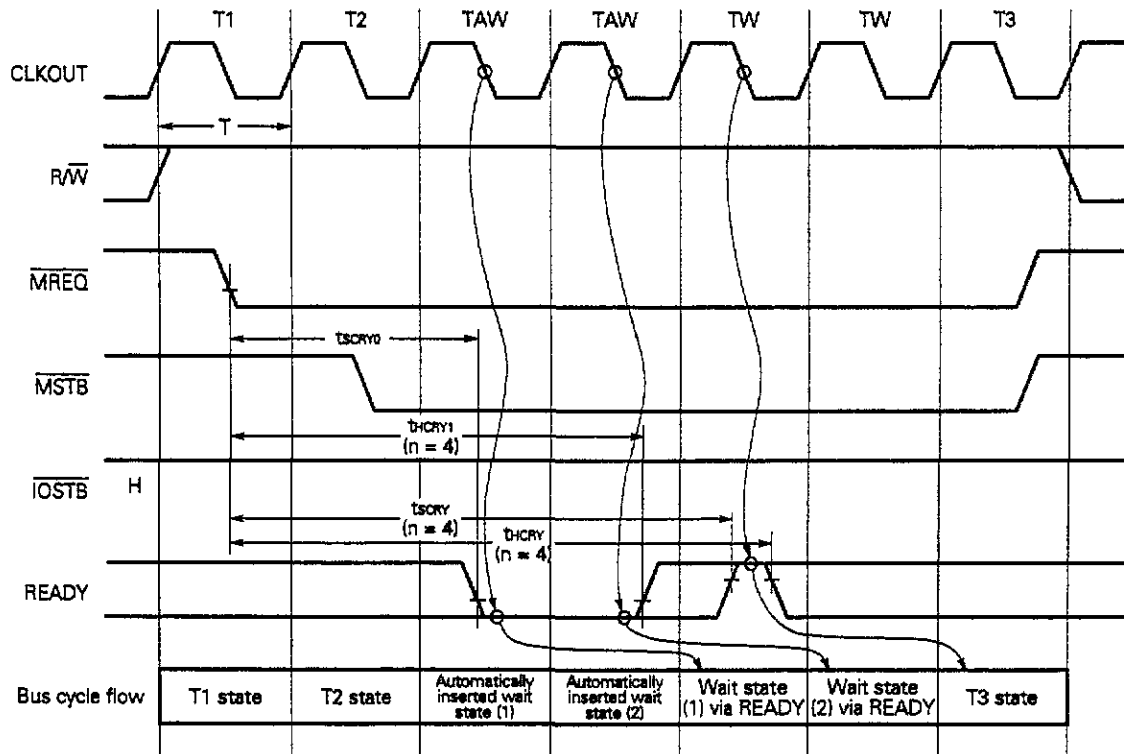

When operation frequency is 10 MHz

T=100 ns

t_{SCRY0}=2T − 80(Max.)=120 ns

t_{HCRY0}=2T(Min.)=200 ns

Figure 5-4. Wait via READY Pin (μPD70335) (4/8)

(d) Addition of two wait states to memory write cycle

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

$t_{SCRY0} = 2T - 80(\text{Max.}) = 120$ ns
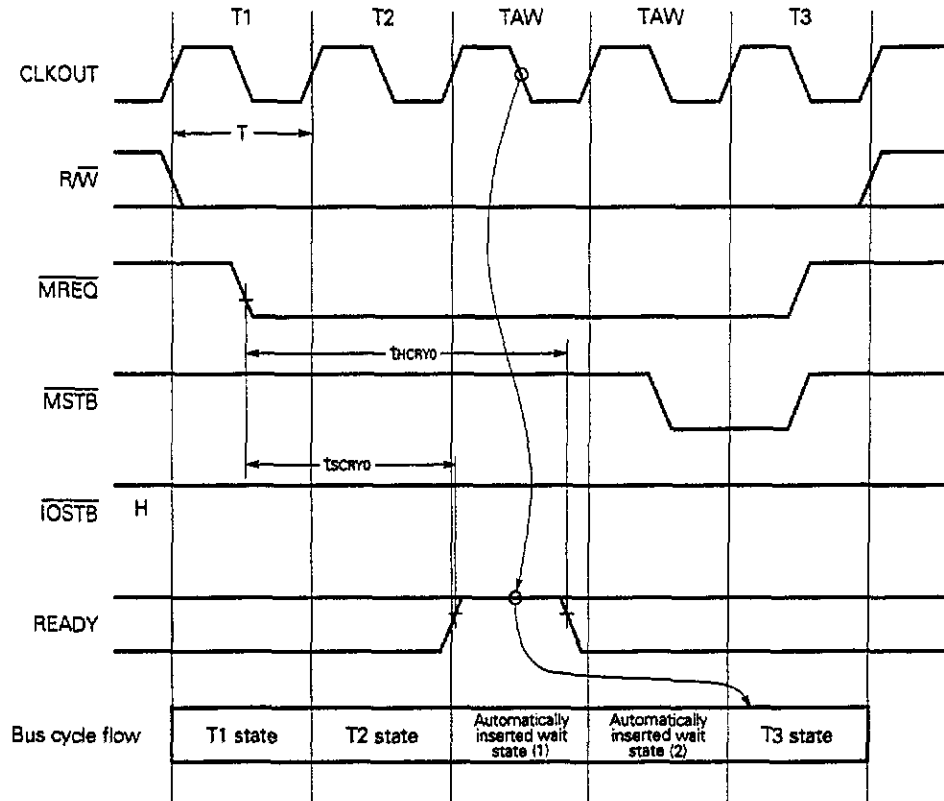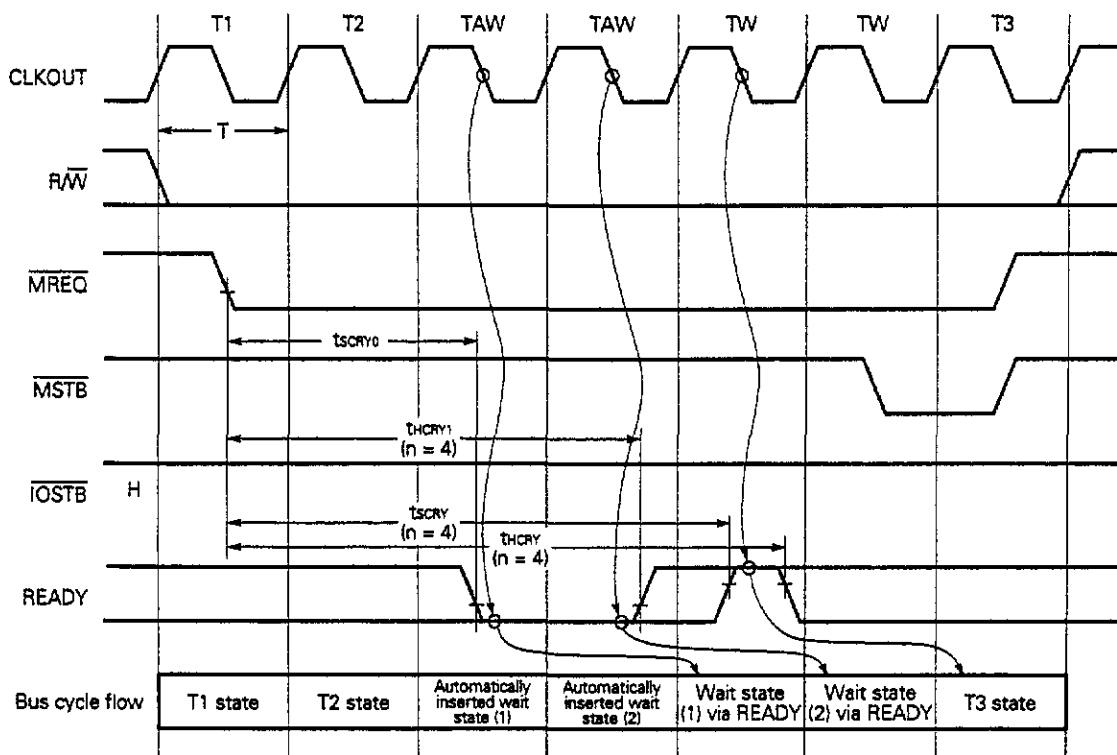
$t_{HCRY1} = (n - 1)T(\text{Min.}) = 300$ ns

$t_{SCRY} = nT - 80(\text{Max.}) = 320$ ns

$t_{HCRY} = nT(\text{Min.}) = 400$ ns

Figure 5-4. Wait via READY Pin (μPD70335) (5/8)

(e) No addition of wait state to I/O read cycle

When operation frequency is 10 MHz

$T = 100$ ns

$t_{SCRYO} = 2T - 80(Max.) = 120$ ns

$t_{HCRYO} = 2T(Min.) = 200$ ns

$t_{SSRYO} = T - 80(Max.) = 20$ ns

$t_{HSRYO} = T(Min.) = 100$ ns

Figure 5-4. Wait via READY Pin (μPD70335) (6/8)

(f) Addition of two wait states to I/O read cycle

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

$t_{SCRY0}=2T - 80(Max.)=120$ ns

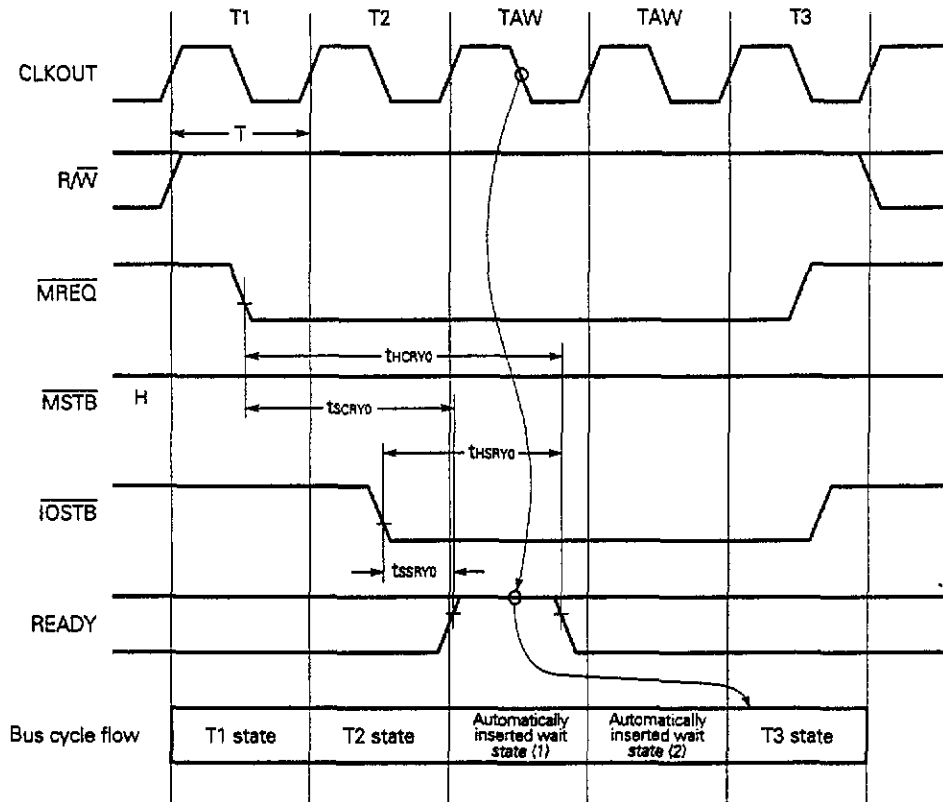$t_{HCRY1}=(n - 1)T(Min.)=300$ ns

$t_{SCRY}=nT - 80(Max.)=320$ ns

$t_{HCRY}=nT(Min.)=400$ ns

$t_{SSRY0}=T - 80(Max.)=20$ ns

$t_{HSRY1}=(n - 2)T(Min.)=200$ ns

$t_{SSRY}=(n - 1)T - 80(Max.)=220$ ns

$t_{HSRY}=(n - 1)T(Min.)=300$ ns

Figure 5-4. Wait via READY Pin (μPD70335) (7/8)

(g) No addition of wait state to I/O write cycle
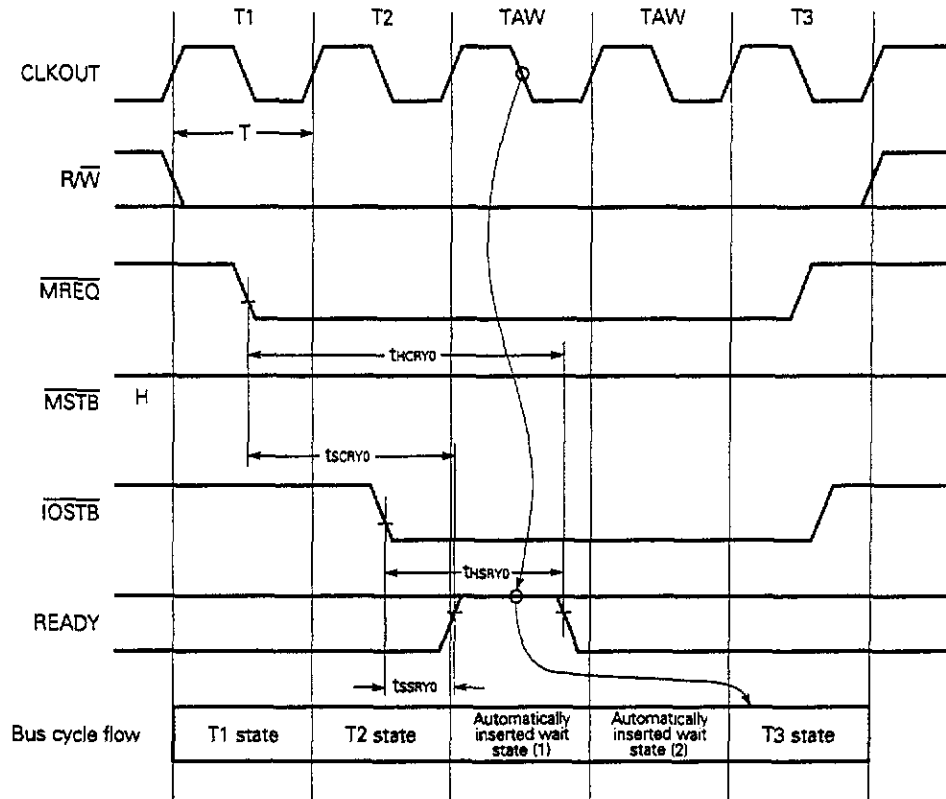
When operation frequency is 10 MHz
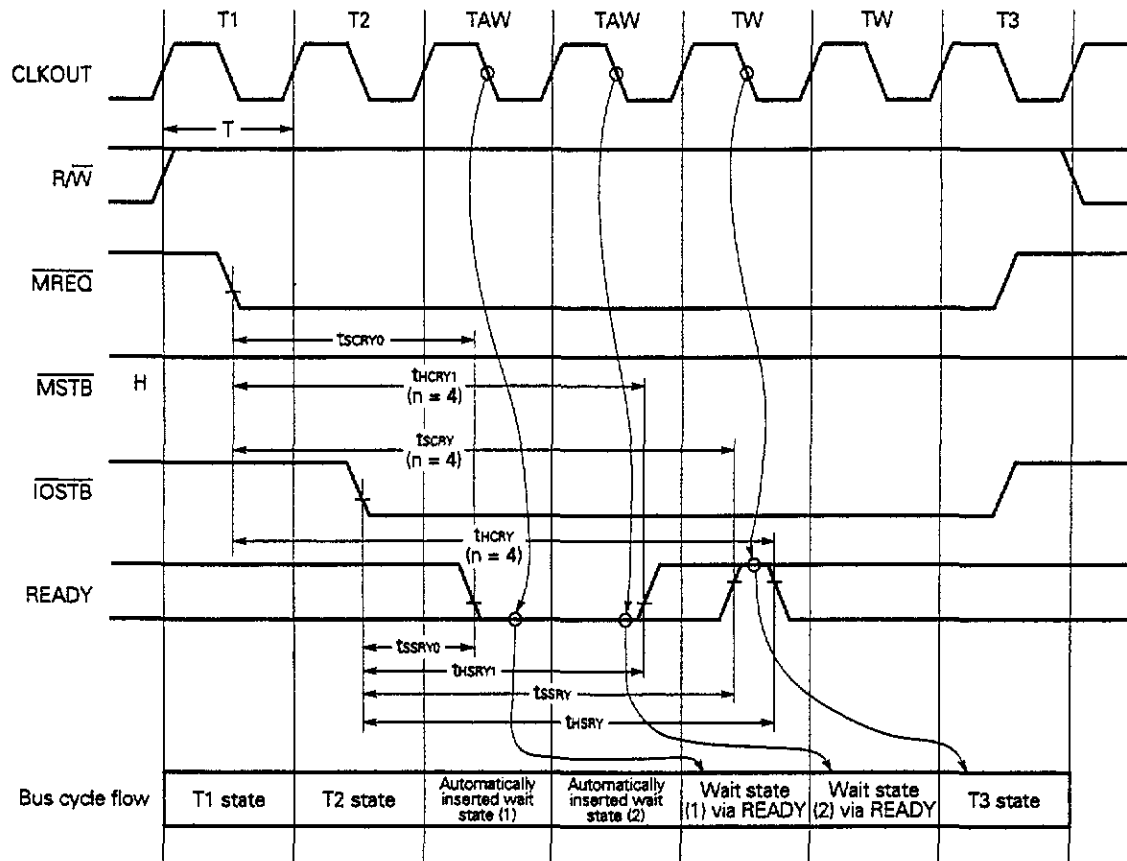
$T=100$ ns

$t_{SCRYO}=2T - 80(Max.)=120$ ns

$t_{HCRYO}=2T(Min.)=200$ ns

$t_{SSRYO}=T - 80(Max.)=20$ ns

$t_{HSRYO}=T(Min.)=100$ ns

Figure 5-4. Wait via READY Pin (μPD70335) (8/8)

(h) Addition of two wait states to I/O write cycle

When operation frequency is 10 MHz

T=100 ns

Assign 4 to n because the total number of wait states is four.

$t_{SCRY0}=2T - 80(\text{Max.})=120$ ns

$t_{HCRY1}=(n - 1)T(\text{Min.})=300$ ns

$t_{SCRY}=nT - 80(\text{Max.})=320$ ns

$t_{HCRY}=nT(\text{Min.})=400$ ns

$t_{SSRY0}=T - 80(\text{Max.})=20$ ns
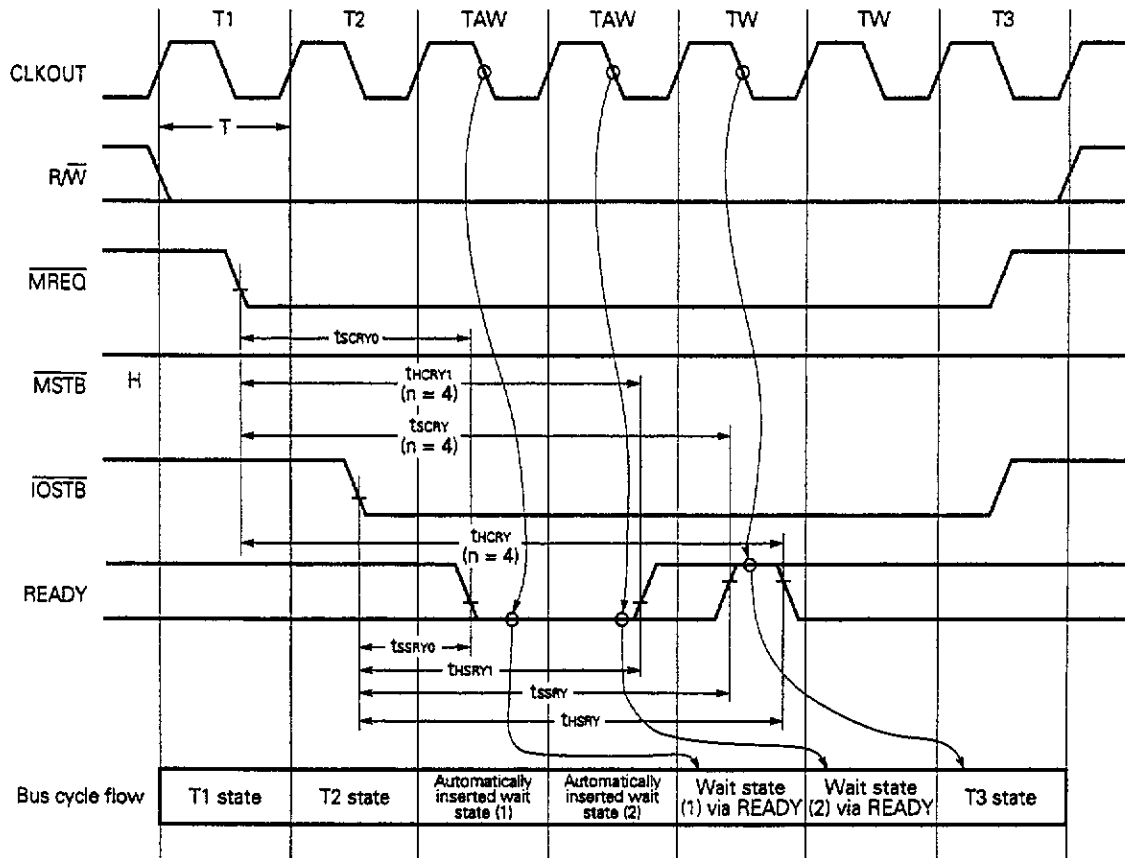
$t_{HSRY1}=(n - 2)T(\text{Min.})=200$ ns

$t_{SSRY}=(n - 1)T - 80(\text{Max.})=220$ ns

$t_{HSRY}=(n - 1)T(\text{Min.})=300$ ns

5.2 Bus Hold Function

The μPD70325 and 70335 each have a bus hold function. High pulse input from an external device to the HLDRQ pin indicates that an external device has used the bus. When detecting that the HLDRQ pin is high, the μPD70325 or 70335 sets high-impedance output from A0 to A19, D0 to D7 (D0 to D15), $\overline{\text{REFRQ}}$, $\overline{\text{MREQ}}$, $\overline{\text{MSTB}}$, $\overline{\text{IOSTB}}$, and R/$\overline{\text{W}}$ and sets the $\overline{\text{HLDAK}}$ pin low to inform the external device that the buses are released. Then the V25 or V35 enters the hold mode. During the hold mode, operations such as instruction execution and prefetch interrupt acknowledgment are stopped and only the on-chip peripheral hardware which does not use the buses is operated. During the hold mode, the V25 or V35 checks the $\overline{\text{HLDRQ}}$ pin and sets the sets the HLDAK signal high when HLDRQ is detected as low to inform the external device that the buses are not released. After one clock, the V25 or V35 restarts execution of instructions.

A bus hold request can also be acknowledged during the HALT mode (see section **12.2**). When the hold mode is released (if the HLDRQ signal is low), a return is made to the HALT mode.

During execution of a block transfer instruction that has a repeat prefix added, a bus hold request can be acknowledged after each bus cycle.

Bus hold requests are not acknowledged when one instruction following BUSLOCK **Note** prefix is being executed or when an interrupt acknowledgment operation is being performed.

In the hold mode, the μPD70325 or 70335 can insert a memory refresh cycle by setting refresh mode (RFM) register HLDRF (bit 6). At every refresh timing, the V25 or V35 forcibly sets the $\overline{\text{HLDAK}}$ signal high and checks that HLDRQ goes low, then executes a refresh cycle. After this, if the HLDRQ signal goes high, the V25 or V35 again enters the hold mode. If the HLDRQ signal remains low, the hold mode is released and the V25 or V35 restarts execution of instructions.

The HLDRQ pin is also used for P27, and the $\overline{\text{HLDAK}}$ pin is also used for P26. To use the bus hold function, set port 2 mode control register (PMC2) bits 6 and 7 to 1.

Note BUSLOCK
REP
MOVBK
No bus hold requests are acknowledged during block servicing instruction execution in such a program.

5.2.1 Response time from HLDRQ to $\overline{\text{HLDAK}}$ (unit: clock cycles)

The response time from HLDRQ to $\overline{\text{HLDAK}}$ is shown below. However, the following cases are exceptions to this.
- When an interrupt acknowledge cycle is generated by an external interrupt controller
- When a BUSLOCK instruction is executed
- When in STOP mode

	MIN.	MAX.
μPD70325	3	7+2W
μPD70335	3	6+W

W: Number of wait states

5.3 Refresh Functions

The μPD70325 and 70335 each have functions for refreshing DRAM and pseudo SRAM. These functions include:
- Periodical refresh cycle insertion function in a series of bus cycles
- Refresh address and refresh pulse output function to refresh DRAM and pseudo SRAM
- Pseudo SRAM power-down self-refresh mode support function
- Refresh cycle generation function during hold mode or HALT mode
- Wait state insertion function in a refresh cycle

5.3.1 Refresh mode register (RFM)

The refresh mode register (RFM) is an 8-bit register that controls the refresh function. The register can be written or read by making an 8-bit or 1-bit memory access.

When RESET is asserted, the RFM register contents are initialized to FCH.

The RFM register format is shown below. The bit functions are described as follows.

7	6	5	4	3	2	1	0
RFLV	HLDRF	HLTRF	RFEN	RFW1	RFW0	RFT1	RFT0

RFT0 and RFT1 : Refresh cycle specification bits

Refresh cycle can be selected out of output taps 3 to 6 of the time base counter (see **CHAPTER 10**). A refresh cycle is generated at intervals listed in Table 5-5.

Table 5-5. Refresh Cycles

When f_{CLK} = 8 MHz

RFT 1	RFT 0	Refresh cycles
0	0	$2^4/f_{CLK}$ (2.0 μs)
0	1	$2^5/f_{CLK}$ (4.0 μs)
1	0	$2^6/f_{CLK}$ (8.0 μs)
1	1	$2^7/f_{CLK}$ (16.0 μs)

RFW0 and RFW1 : Bits specifying the number of wait states to be inserted in a refresh cycle

The number of wait states inserted in a refresh cycle is specified by setting RFW0 and RFW1 as shown in Table 5-6 rather than the programmable wait function described in section **5.1** above.

Table 5-6. Number of Wait States Inserted in Refresh Cycle

RFW 1	RFW 0	Wait states
0	0	0 states
0	1	1 state
1	0	2 states
1	1	2 states

RFEN : Bit to enable automatic refresh cycle insertion

When this bit is set to 1, automatic refresh cycle insertion is enabled. When set to 0, automatic refresh cycle insertion is disabled. REFRQ pin output is controlled by the RFLV bit contents (for details, see the **RFLV bit description** below).

HLTRF : Bit to enable automatic refresh cycle insertion during the HALT mode

When this bit is set to 1, automatic refresh cycle insertion during HALT mode is enabled. When set to 0, it is disabled. However, when the RFEN bit is set to 0, the automatic refresh cycle insertion is disabled regardless of the HLTRF bit contents.

HLDRF : Bit to enable automatic refresh cycle insertion during the hold mode

When this bit set is to 1, automatic refresh cycle insertion during hold mode is enabled. When set to 0, it is disabled.

When it is enabled, HLDAK output is forcibly set high at every refresh timing and a refresh cycle is automatically inserted.

RFLV : REFRQ signal output level specification bit

Figure 5-5 shows the control circuit that depends upon the RFLV bit contents. Output is determined according to the logic listed in Table 5-7. When the RFLV bit is read, it becomes the master RFLV output. When this bit is written, it is written into slave RFLV. Master RFLV is written into when the refresh timing is generated. The pseudo SRAM power-down self-refresh mode can be supported by using the RFLV bit.

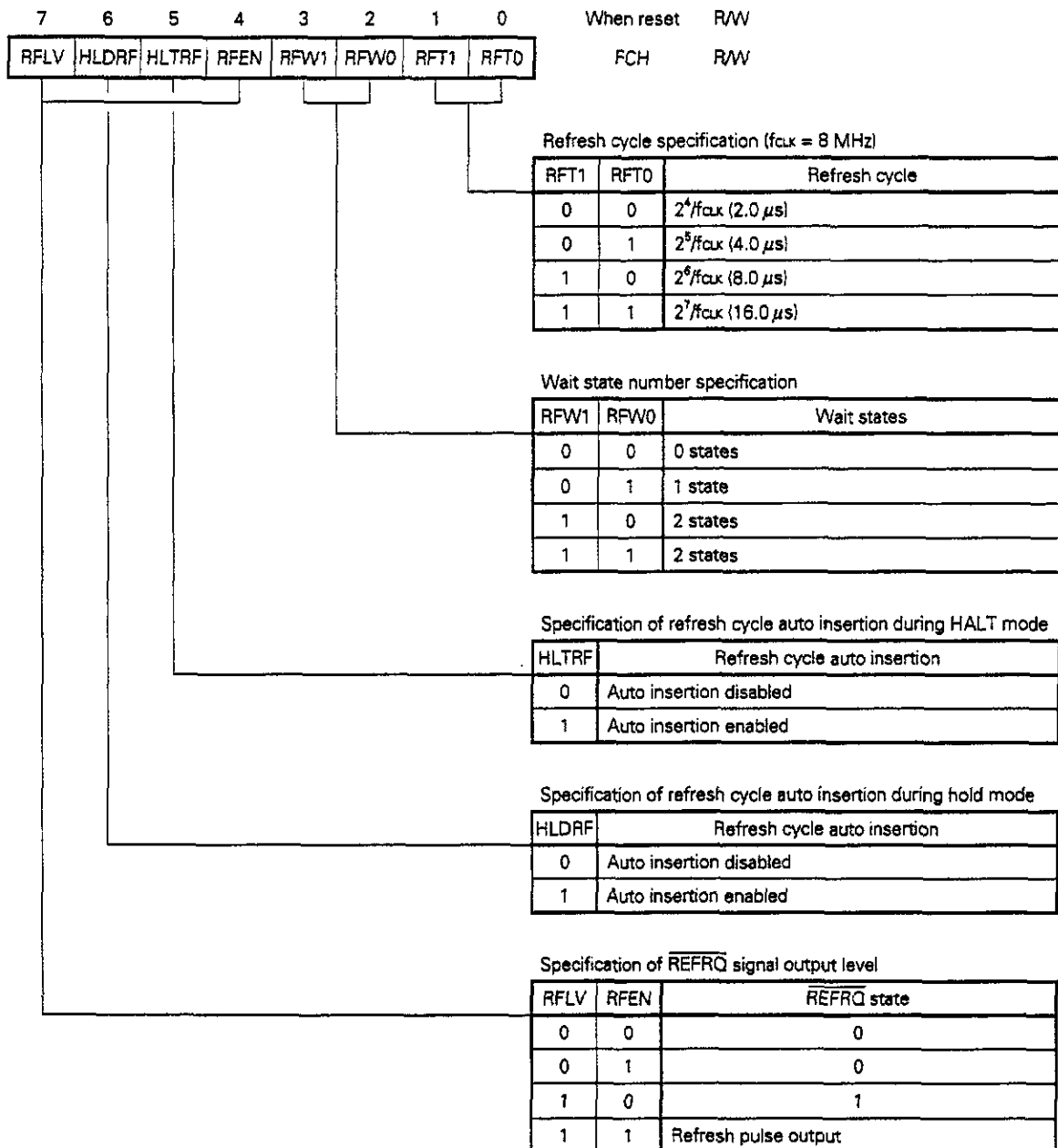**Figure 5-5. Control Circuit Depending on the RFLV Bit Contents**
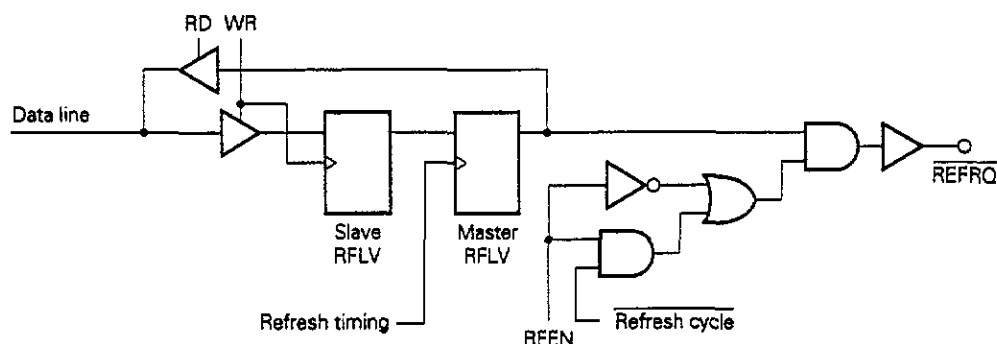
Table 5-7. $\overline{\text{REFRQ}}$ Signal Output Levels

RFLV	RFEN	$\overline{\text{REFRQ}}$ state
0	0	0
0	1	0
1	0	1
1	1	Refresh pulse output

A refresh cycle is inserted at the refresh timing when the RFEN bit is set to 1. At that time, $\overline{\text{MREQ}}$, $\overline{\text{MSTB}}$, and $\overline{\text{IOSTB}}$ go high, a refresh address is output to A0 to A8, low level is output to A9 to A18 (for the μPD70325; see **Table 5-3** for the μPD70335), and a refresh pulse is output from the $\overline{\text{REFRQ}}$ pin.

Even if the RFLV bit is written, it does not become read data until the next refresh timing.

Figure 5-6. RFM

7	6	5	4	3	2	1	0
RFLV	HLDRF	HLTRF	RFEN	RFW1	RFW0	RFT1	RFT0

When reset   R/W

FCH   R/W

Refresh cycle specification (fc$_{LK}$ = 8 MHz)

RFT1	RFT0	Refresh cycle
0	0	2^4/fc$_{LK}$ (2.0 μs)
0	1	2^5/fc$_{LK}$ (4.0 μs)
1	0	2^6/fc$_{LK}$ (8.0 μs)
1	1	2^7/fc$_{LK}$ (16.0 μs)

Wait state number specification

RFW1	RFW0	Wait states
0	0	0 states
0	1	1 state
1	0	2 states
1	1	2 states

Specification of refresh cycle auto insertion during HALT mode

HLTRF	Refresh cycle auto insertion
0	Auto insertion disabled
1	Auto insertion enabled

Specification of refresh cycle auto insertion during hold mode

HLDRF	Refresh cycle auto insertion
0	Auto insertion disabled
1	Auto insertion enabled

Specification of $\overline{REFRQ}$ signal output level

RFLV	RFEN	$\overline{REFRQ}$ state
0	0	0
0	1	0
1	0	1
1	1	Refresh pulse output

5.3.2 Connection to pseudo SRAM

Figure 5-7 shows a circuit example connecting pseudo SRAM equivalent to the μPD42832.

Figure 5-7. μPD42832 Connection Circuit Example
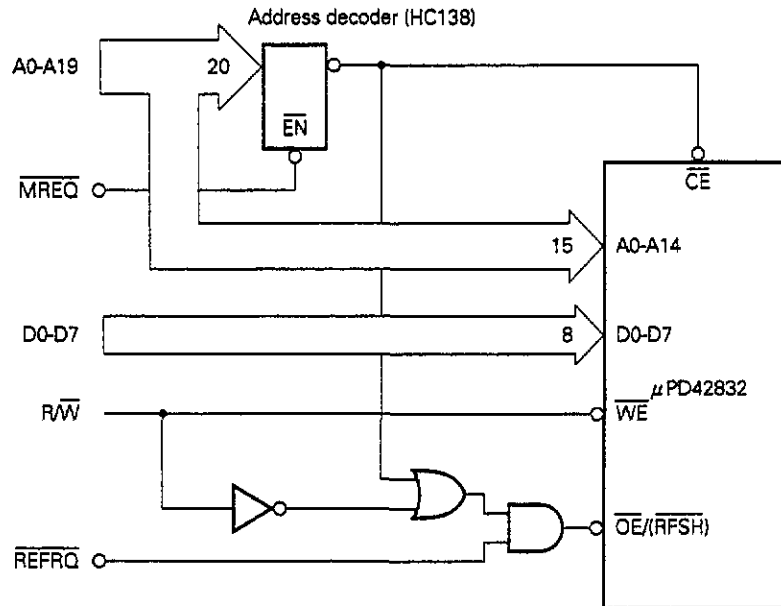
In this connection example, two modes can be used: pulse refresh mode and power-down self-refresh mode. In the pulse refresh mode, pulses are given to the $\overline{OE}/(\overline{RFSH})$ pin from the $\overline{REFRQ}$ pin when the $\overline{CE}$ pin is high. In the power-down self-refresh mode, the $\overline{REFRQ}$ pin is set low by software which resets bit 7 (RFLV) to 0 in the refresh mode register (RFM).

The power-down self-refresh mode is used when the CPU is in the standby (STOP) mode and cannot perform pulse refresh operations. Thus, the RFLV bit is reset to 0 just before the CPU enters the standby mode. When the CPU is restored from the standby mode, the RFLV bit is set to 1 so that pulse refresh operations can be performed.

Caution When reset ($\overline{RESET}$ pin = 0), the $\overline{REFRQ}$ pin goes to high-impedance.

5.3.3 Connection to DRAM

Figure 5-8 shows a circuit examples connecting the μPD41256 (256 Kbytes × 1-bit structure).

Figure 5-8. μPD41256 Connection Circuit Example
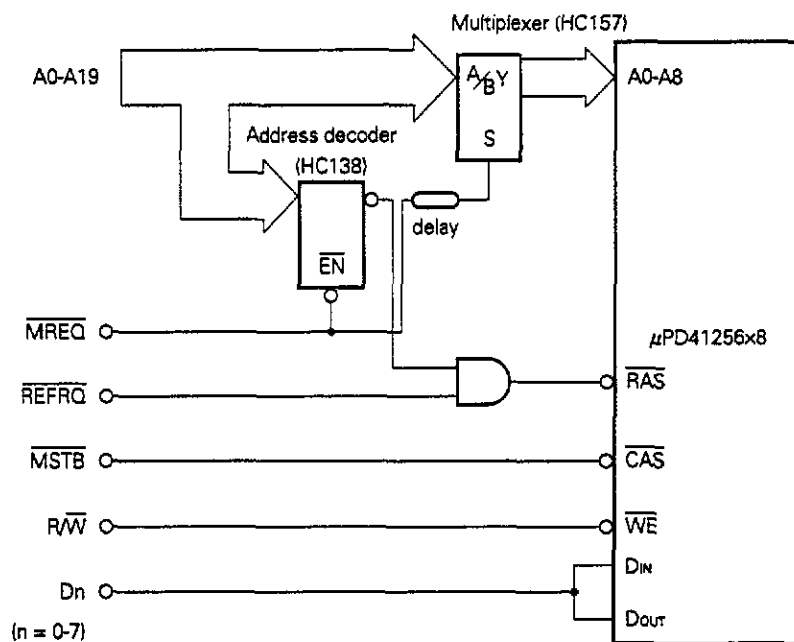
In this connection example, refresh operations are performed by $\overline{RAS}$ only refresh using the 9-bit refresh address output to the address bus in synchronization with a pulse output from the $\overline{REFRQ}$ pin.

5.4 Bus Mastership

The bus mastership priority levels for the μPD70325 and 70335 follow the order shown below.

(1) Refresh cycle (see section 5.3)

Whenever refresh cycle insertion is enabled, a refresh cycle is generated. However, during the hold mode, the $\overline{\text{HLDAK}}$ signal is forcibly set high and a wait is made for the HLDRQ signal to go low before a refresh cycle is executed.

No refresh cycle is started while wait cycles are inserted by the READY pin.

(2) Hold mode (see section 5.2)

The transition to the hold mode is made except during execution of one instruction following a BUSLOCK prefix or interrupt acknowledge cycle.

(3) DMA cycle (see Chapter 6)

(4) Other bus cycles

However, when an $\overline{\text{INTAK}}$ cycle is being executed, refresh cycles, hold modes, and DMA cycles are temporarily held pending. DMA cycles are also held pending during operations of interrupt acknowledgment for internal interrupts. See section **4.17 Hardware Interrupt Response Time** for description of time required for interrupt acknowledgment.

In the STOP mode, the buses do not operate. (See **Table 12-2** for the bus state).

Data transfer (block transfer, DMA transfer, macro service, etc.) can be used at the same time with the same program, but simultaneous execution is not possible because the data transfer uses a single bus.

5.5 Bus Timings

Figures 5-9 to 5-30 show the main bus timings (except for DMA).

When no bus access is made, the control pins are deactivated and both data bus output and address bus output are undefined.

5.5.1 Bus timing of μPD70325

Figure 5-9. Memory Read Cycle   **Figure 5-10. Memory Write Cycle**   **Figure 5-11. I/O Read Cycle**
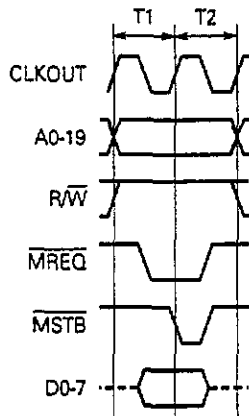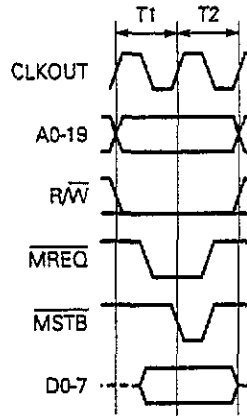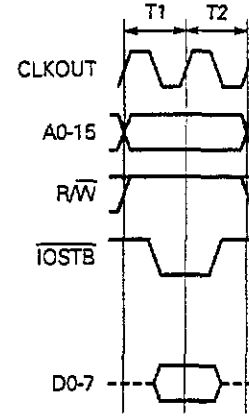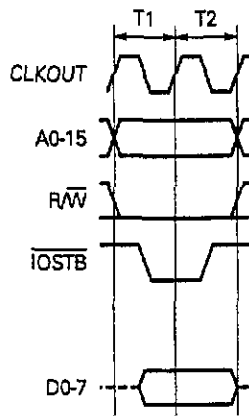
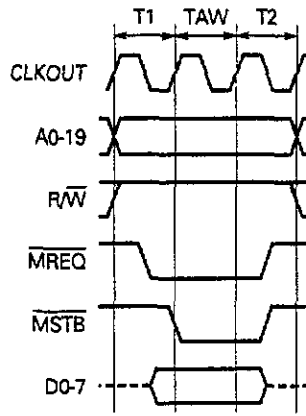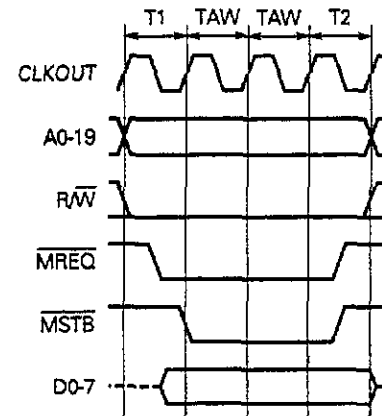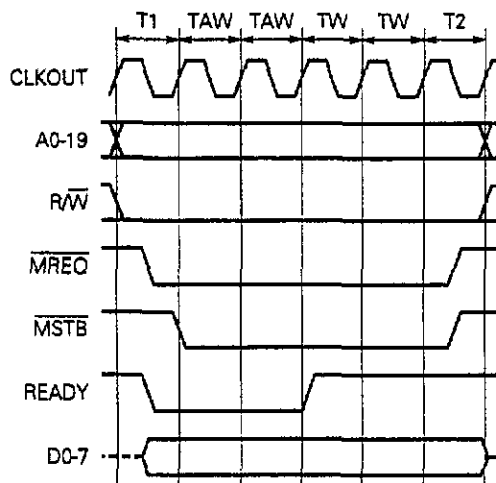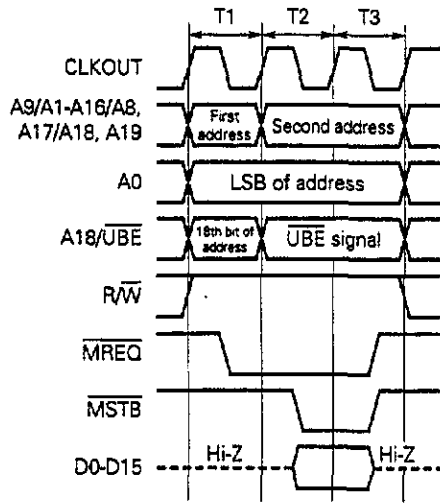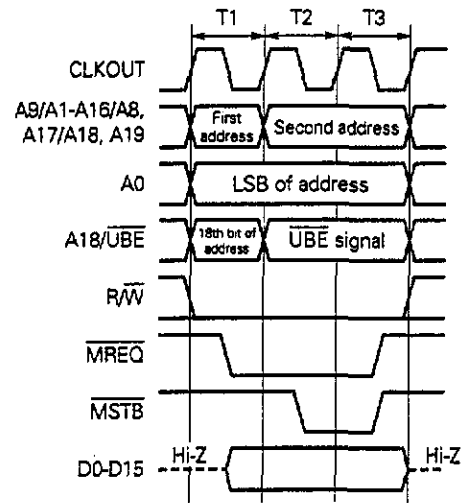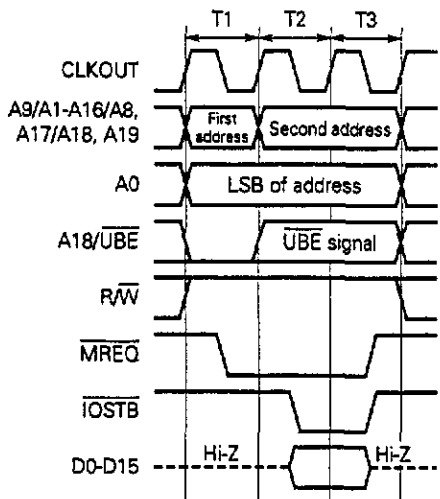**Figure 5-12. I/O Write Cycle**   **Figure 5-13. Memory Read Cycle (when one wait state is inserted)**   **Figure 5-14. Memory Write Cycle (when two wait states are inserted)**

Remark The broken line indicates high-impedance.

Figure 5-15. Memory Write Cycle (during READY pin operation)

Remark The broken line indicates high-impedance.

Figure 5-16. Refresh Cycle (when one wait state is inserted)
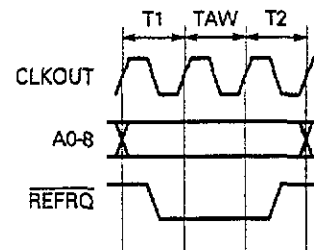
Figure 5-17. Bus Hold Acknowledgment Release Timing
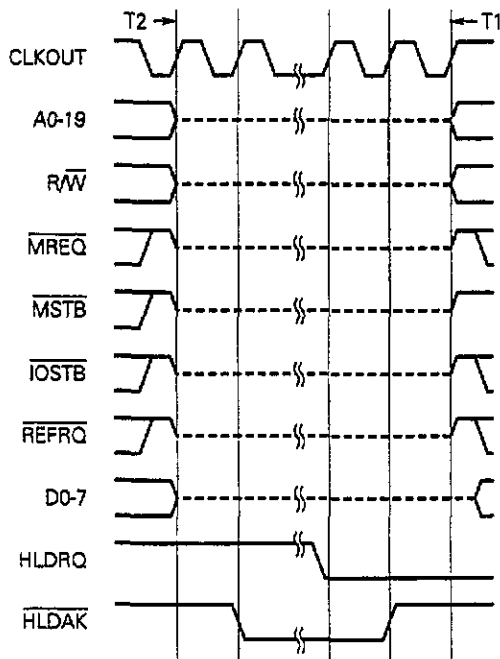
Remark *The broken line indicates high-impedance.*

Figure 5-18. Refresh Cycle in Hold Mode (0 wait state)
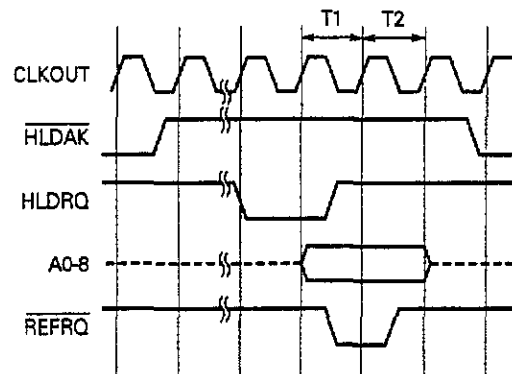
Remark The broken line indicates high-impedance.

Figure 5-19. Bus Hold Acknowledgment Release Timing during HALT Mode
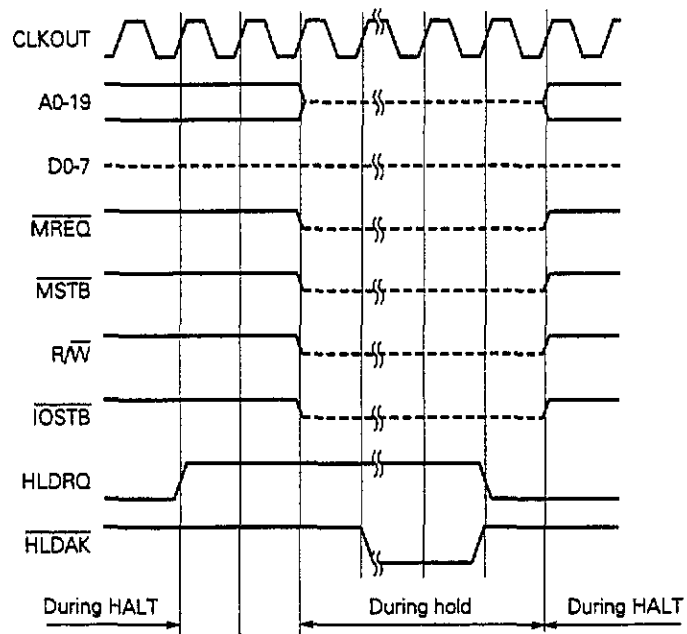
Remark   The broken line indicates high-impedance.

5.5.2 Bus timing of μPD70335

Figure 5-20. Memory Read Cycle

Figure 5-21. Memory Write Cycle

Figure 5-22. I/O Read Cycle
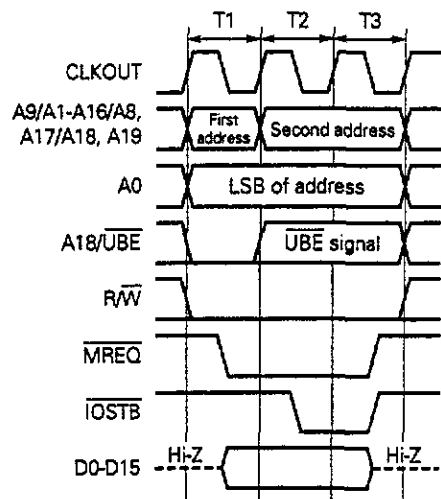

Figure 5-23. I/O Write Cycle

Figure 5-24. Memory Read Cycle (when one wait state is inserted)

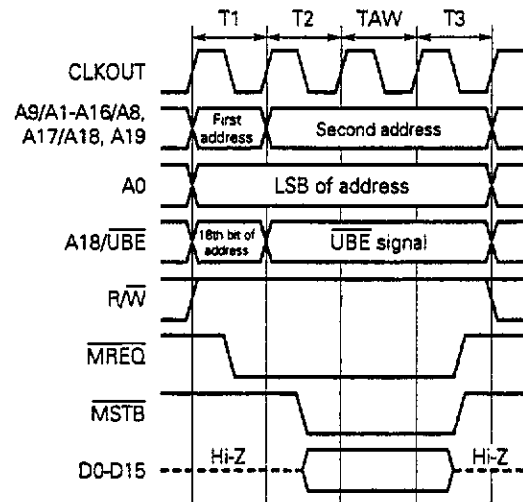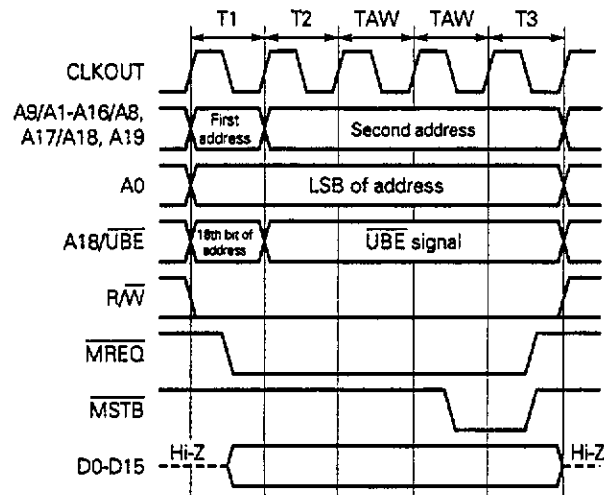Figure 5-25. Memory Write Cycle (when two wait states are inserted)

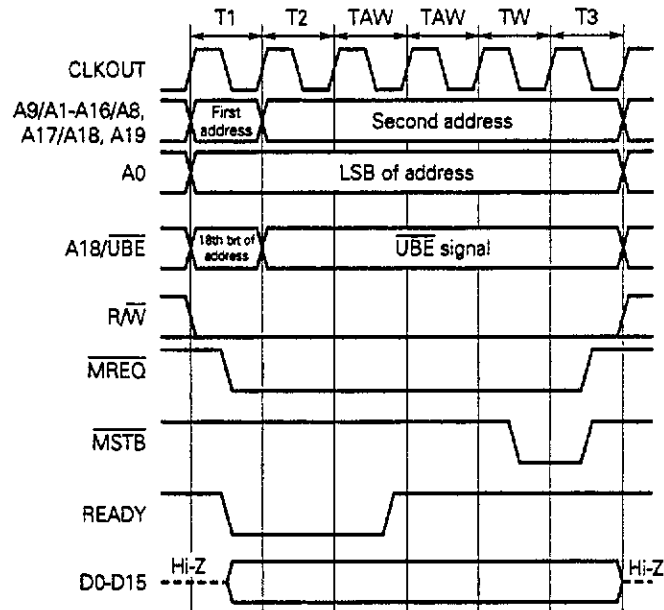**Figure 5-26. Memory Write Cycle (during READY pin operation)**

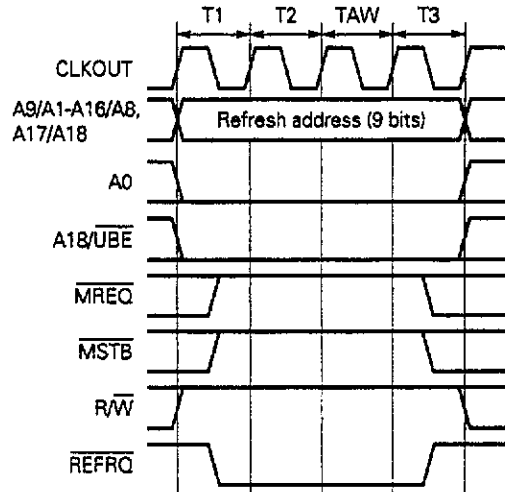**Figure 5-27. Refresh Cycle (when one wait state is inserted)**

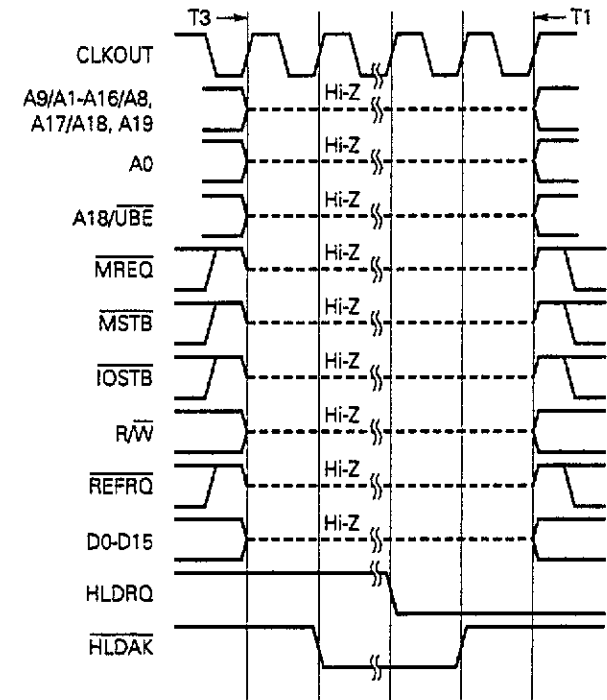**Figure 5-28. Bus Hold Acknowledgment Release Timing**
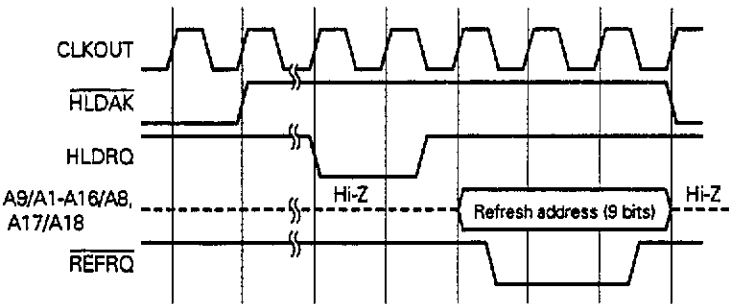

Figure 5-29. Refresh Cycle in Hold Mode

Figure 5-30. Bus Hold Acknowledgment Release Timing during HALT Mode