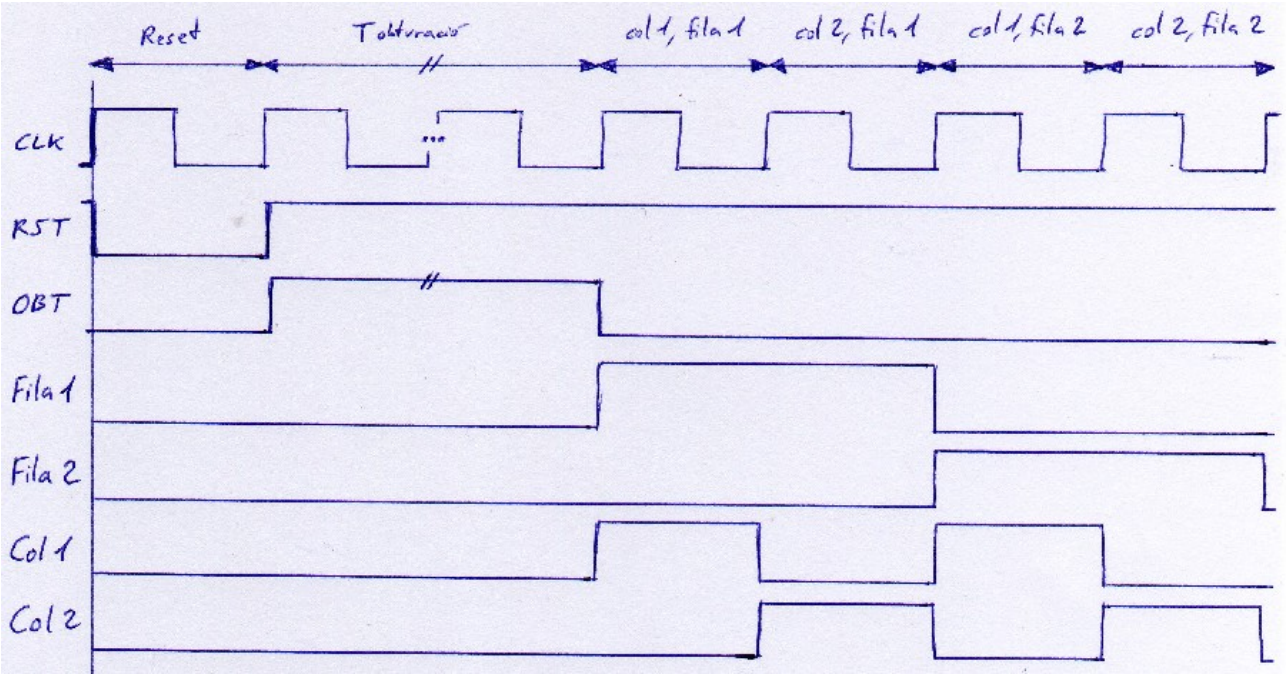
Prelab 2

15.- Draw the chronogram of the control inputs of the analog section according to this new sequence. Detail the duration of each pulse (in numbers of clock periods, not μs), including the shutter opening time for the different values of SelObt.

Cronograma de las entradas:

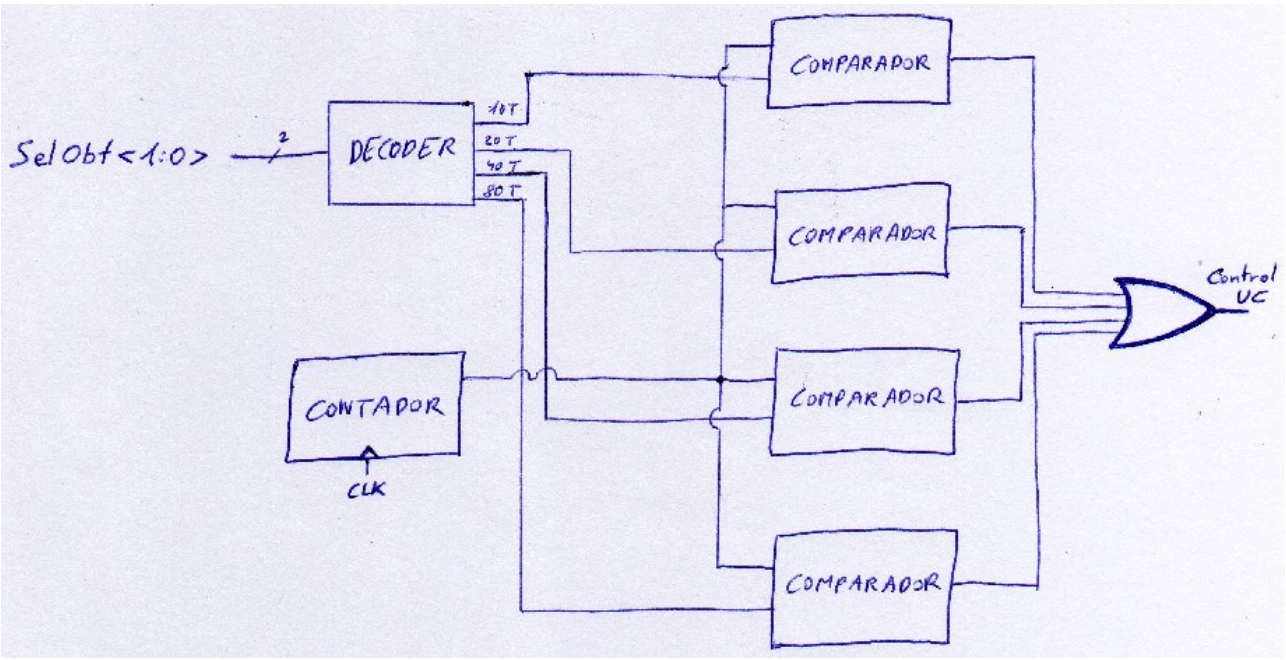


Teniendo en cuenta las duraciones de Tobt según la velocidad del obturador, estas seran las duraciones, en periodos de reloj:

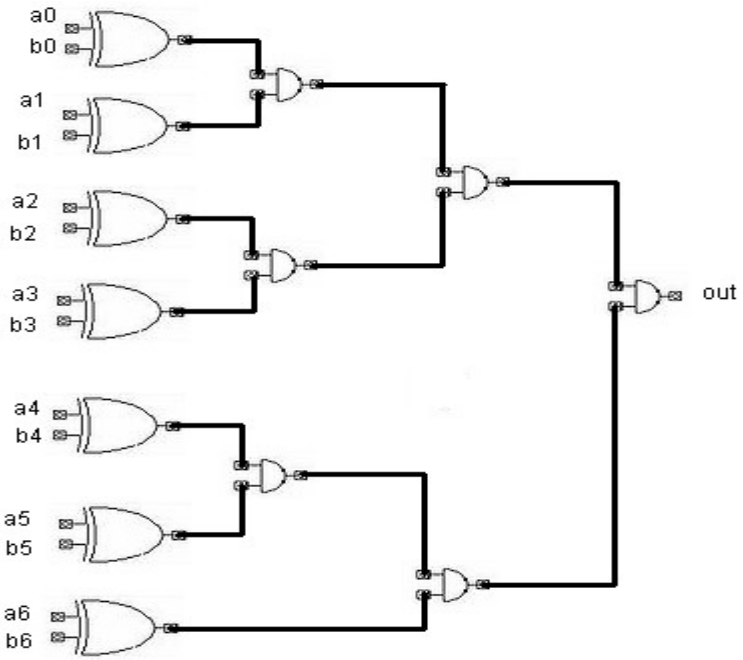
SelObt<1>	SelObt<0>	Shutter Speed	Shutter Time	Duración T_{obt}
0	0	1/8000	125μs	$10 \cdot T_{CLK}$
0	1	1/4000	250μs	$20 \cdot T_{CLK}$
1	0	1/2000	500μs	$40 \cdot T_{CLK}$
1	1	1/1000	1ms	$80 \cdot T_{CLK}$

16.- Design the schematic of the Process Unit, using the following basic elements:

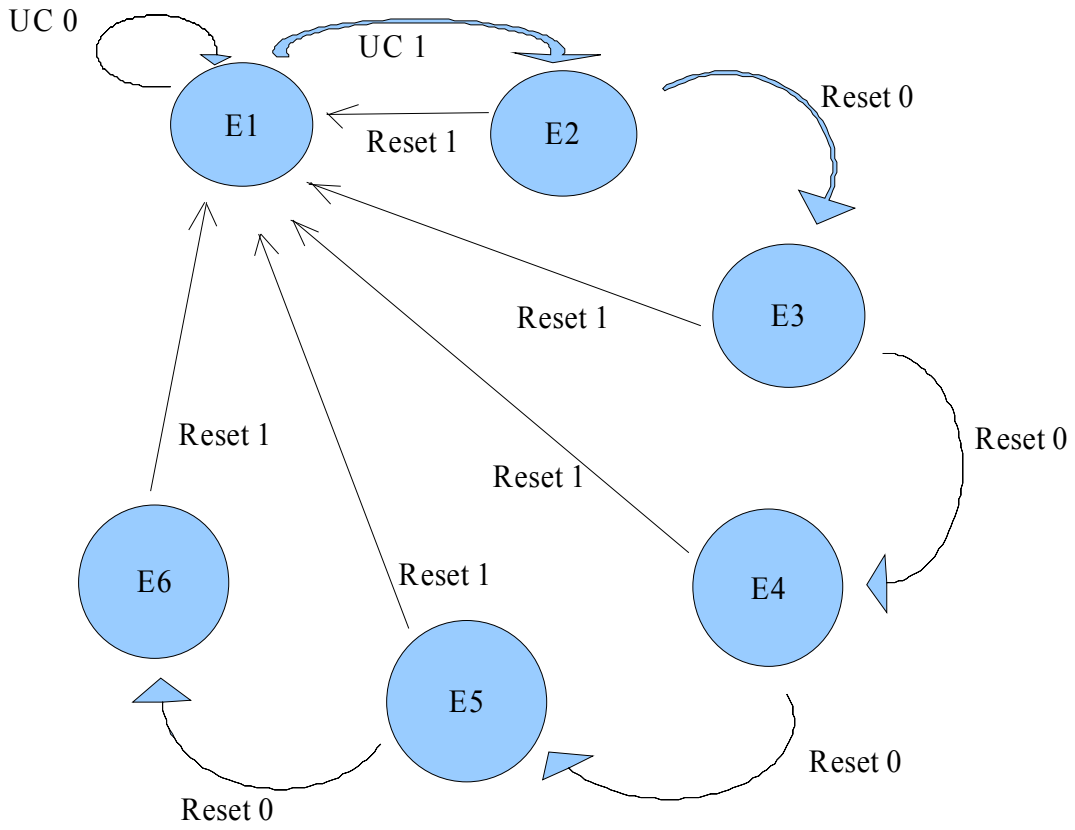
- **Basic logic gates (AND, OR, NOT...)**
- **TFEC1 from the CORELIB library: toggle flip-flop with active low asynchronous reset.**
- **Comparator: combinational circuit that outputs '1' when both input buses have the same value, '0' otherwise.**
- **Decoder: combinational circuit that implements a look-up table with input SelObt<1:0> and outputs the shutter opening time, expressed in number of clock periods.**



17.- Design a 7-bit comparator, which delivers a '1' output when both inputs have the same value, and '0' otherwise. Use simple gates like AND, OR, NAND, NOR, INV, XOR, NXOR as basic elements.



18.- Draw the states diagram of the finite state machine that, from the clock signal and the pulse output by the Process Unit, generates the control signals of the analog part and the Process Unit. Specify clearly the conditions of the transitions between the different states, and the states in which the outputs are active '1'.



	OBT	SELCOL1	SELCOL2	SELROW1	SELROW2
E1	1	0	0	0	0
E2	0	1	0	1	0
E3	0	0	1	1	0
E4	0	1	0	0	1
E5	0	0	1	0	1
E6	0	0	0	0	0