CHAPTER 9 TIMER UNIT

The timer unit in the μPD70325 and 70335 can be used as an interval timer, a one-shot timer, or a square wave output.

9.1 Timer Unit Structure and Operation

The timer unit consists of two 16-bit timer registers, two 16-bit modulo/timer registers, and one 8-bit timer control register. The structure and operation of each operation mode are explained below.

(1) Interval timer mode

When the timer unit is set to the interval timer mode, timers 0 and 1 can be used as shown in Figure 9-1.

**Figure 9-1. Timer Unit Structure during Interval Timer Mode**
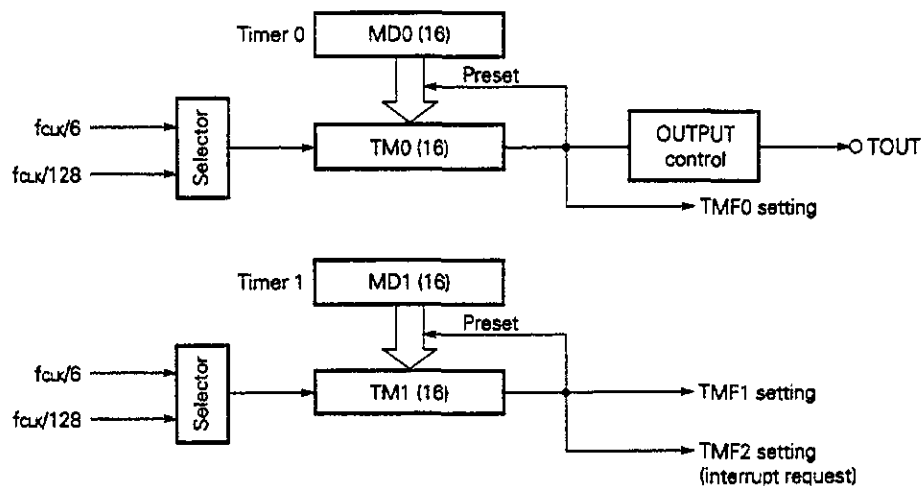
When the interval timer mode is specified in the timer control register (TMC0) and the TS0 bit is set to 1, the MD0 register value is set in the TM0 register and the clock specified in the TCLK0 bit is counted down. If the timer value is set to 0 during the countdown, the MD0 register value is again set in the TM0 register and the clock is counted down. (Count value = setting value + 1)

A similar count operation is also performed for the timer 1 registers.

(2) One-shot timer mode

When the timer unit is set to the one-shot timer mode, timer 0 is used as shown in Figure 9-2. However, timer 1 can also be operated as an interval timer at the same time.

Figure 9-2. Timer Unit Structure during One-shot Timer Mode
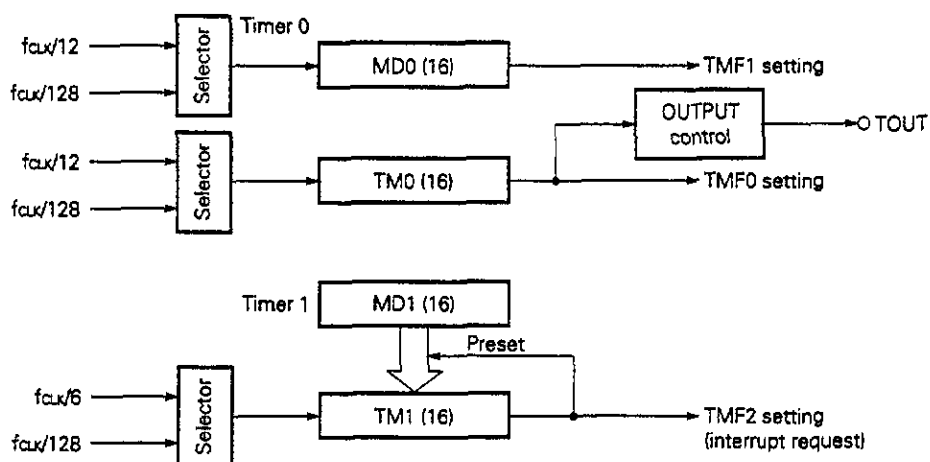
When the one-shot timer mode is specified in the timer control register (TMC0) and the TS0/MS0 bit is set to 1, the clock specified in the TCLK0/MCLK0 bit is counted down in the TM0/MD0 register. When the timer value is set to 0 during the countdown, the count operation stops. At that time, 0000H is retained in the TM0/MD0 register.

9.2 Timer Control Registers (TMC0 and TMC1)

The TMC0 register is an 8-bit register that controls TM0 and MD0 register operations. The TMC1 register is an 8-bit register that controls TM1 and MD1 register operations.

The registers can be written/read by making an 8-bit or 1-bit memory access, in which case up to six wait states are inserted.

When $\overline{\text{RESET}}$ is input, the contents of each register are initialized to 00H. The TMC0 and TMC1 registers differ in format as shown below.

(Interval timer mode, one-shot timer mode)

	7	6	5	4	3	2	1	0
TMC0	TS0	TCLK0	MS0	MCLK0	ENT0	ALV	MOD1	MOD0

(Interval timer mode)

	7	6	5	4	3	2	1	0
TMC1	TS1	TCLK1	0	0	0	0	0	0

The operation mode of timer 0 consisting of TM0 and MD0 (or timer 1 consisting of TM1 and MD1) is specified by setting TMC0 (or TMC1) register bits 0 and 1 (MOD0 and MOD1).

MOD0 and MOD1 : Timer 0 (or timer 1) operation mode specification bits

Set both MOD0 and MOD1 to 0 to select interval timer operation mode. Set MOD0 to 1 and MOD1 to 0 to select one-shot timer operation mode. In the interval timer operation mode, TM0 (or TM1) serves as a timer register for counting down the setup value and MD0 (or MD1) serves as a modulo register for retaining the interval setup value. In the one-shot timer operation mode, both TM0 and MD0 serve as timer registers for counting down the setup value. TMC1 bits 0 and 1 are fixed to 0 and timer 1 operates only as an interval timer.

Therefore, timer 0 consisting of TM0 and MD0 operates as a 16-bit interval timer or 16-bit one-shot timer. Timer 1 consisting of TM1 and MD1 operates as a 16-bit interval timer.

Timer 0 can also output a square wave to the TOUT pin. Square wave output to the TOUT pin is controlled by setting the TMC0 register. However, because the TOUT pin is also used for P15, set port 1 mode control register bit 5 (PMC15) to 1 to set the pin to the control mode before outputting a square wave to the TOUT pin. At this time, square wave output to the TOUT pin depends on the CPU's internal timing and does not depend on CLKOUT output.

ALV : Active level specification bit of TOUT pin output

When the ENTO bit is reset to 0, the TOUT pin output becomes active-low when the ALV bit is reset to 0 and active-high when the ALV bit is set to 1.

ENTO : Bit specifying operation of square wave output to TOUT pin

When the ENTO bit is reset to 0, the TOUT pin level becomes inactive as specified in the ALV bit when in interval timer mode.

During one-shot timer mode, the following changes occur according to the setup value in the ALV bit.

ALV	Timing of change	TOUT pin
0	TS0 = 1	1
	TMF0 = 1	0
1	TS0 = 1	0
	TMF0 = 1	1

When the ENTO bit is set to 1, the TOUT pin level is inverted according to the timing whereby the timer unit interrupt request flag (TMF0) is set to 1.

Figure 9-3. Output State of TOUT Pin (during One-shot Timer Mode)

① : ALV = 1, ENTO = 0

② : ALV = 0, ENTO = 1
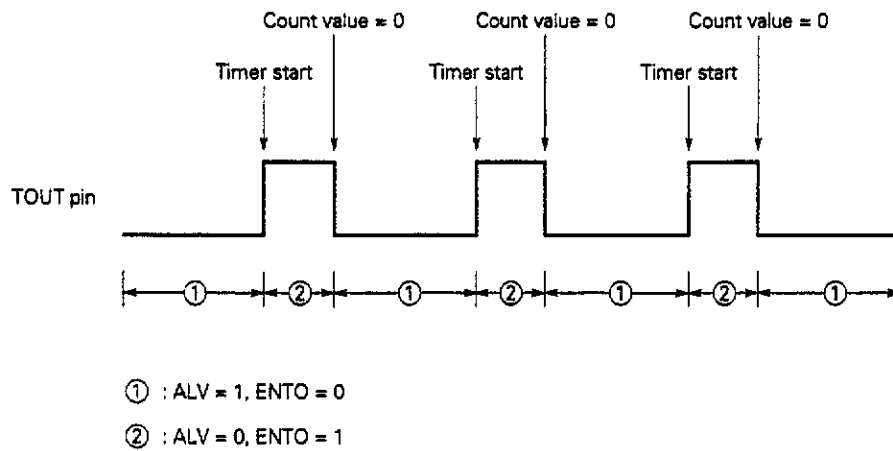
When the timer counter is started,② is set.
After completion of the countdown (after inversion of TOUT output), set as shown for ①.

Other bits in the TMC0 and TMC1 registers are explained below for each operation mode.

(1) Interval timer mode (MOD0 = 0, MOD1 = 0): Timers 0 and 1

$\boxed{\text{TCLK0}}$ and $\boxed{\text{TCLK1}}$: Count clock specification bits in TM0 and TM1 registers

Table 9-1 lists the reference values when the system clock frequency (f_{CLK}) is 8 MHz.

$\boxed{\text{TS0}}$ and $\boxed{\text{TS1}}$: Operation control bits for timers 0 and 1

When the TS0 (or TS1) bit is set to 1, the MD0 (MD1) register value is set in the TM0 (TM1) register and the TM0 (TM1) register starts counting down. When the TS0 (TS1) bit is reset to 0, the TM0 (TM1) register retains the contents of the TM0 (TM1) and MD0 (MD1) registers and stops counting down.

If the timer value is set to 0 or if the TS0 (or TS1) bit is again set to 1 during the countdown, the MD0 (MD1) register value is again set in the TM0 (TM1) register and the TM0 (TM1) register again starts counting down.

Table 9-1. TMn Count Time in Interval Timer Mode (n = 0 or 1)

When f_{CLK} = 8 MHz

TCLKn	Count clock	Resolution	Full count
0	$f_{CLK}/6$	0.75 μs	49.1 ms
1	$f_{CLK}/128$	16 μs	1.04 s

(2) One-shot timer mode (MOD0 = 1, MOD1 = 0): Timer 0 only

$\boxed{\text{TCLK0}}$: TM0 register count clock specification bit

Table 9-2 lists the reference values when the system clock frequency (f_{CLK}) is 8 MHz.

$\boxed{\text{TS0}}$: TM0 register operation control bit

When the TS0 bit is set to 1, the countdown is started from the retained TM0 register contents. When the timer value is set to 0, the TS0 bit is reset to 0 and count operation is stopped. When the TS0 bit is reset to 0, the TM0 register retains the current value and stops counting.

$\boxed{\text{MCLK0}}$: MD0 register count clock specification bit

Table 9-2 lists the reference values when the system clock frequency (f_{CLK}) is 8 MHz. When the interval timer mode is set, the MCLK0 bit does not affect the count operation.

MS0 : MD0 register count operation control bit

When the MS0 bit is set to 1, the countdown is started from the retained MD0 register contents. When the timer value is set to 0, the MS0 bit is reset to 0 and the count operation is stopped. When the MS0 bit is reset to 0, the MD0 register retains the current value and stops counting.

When the interval timer mode is set, the MS0 bit does not affect the count operation.

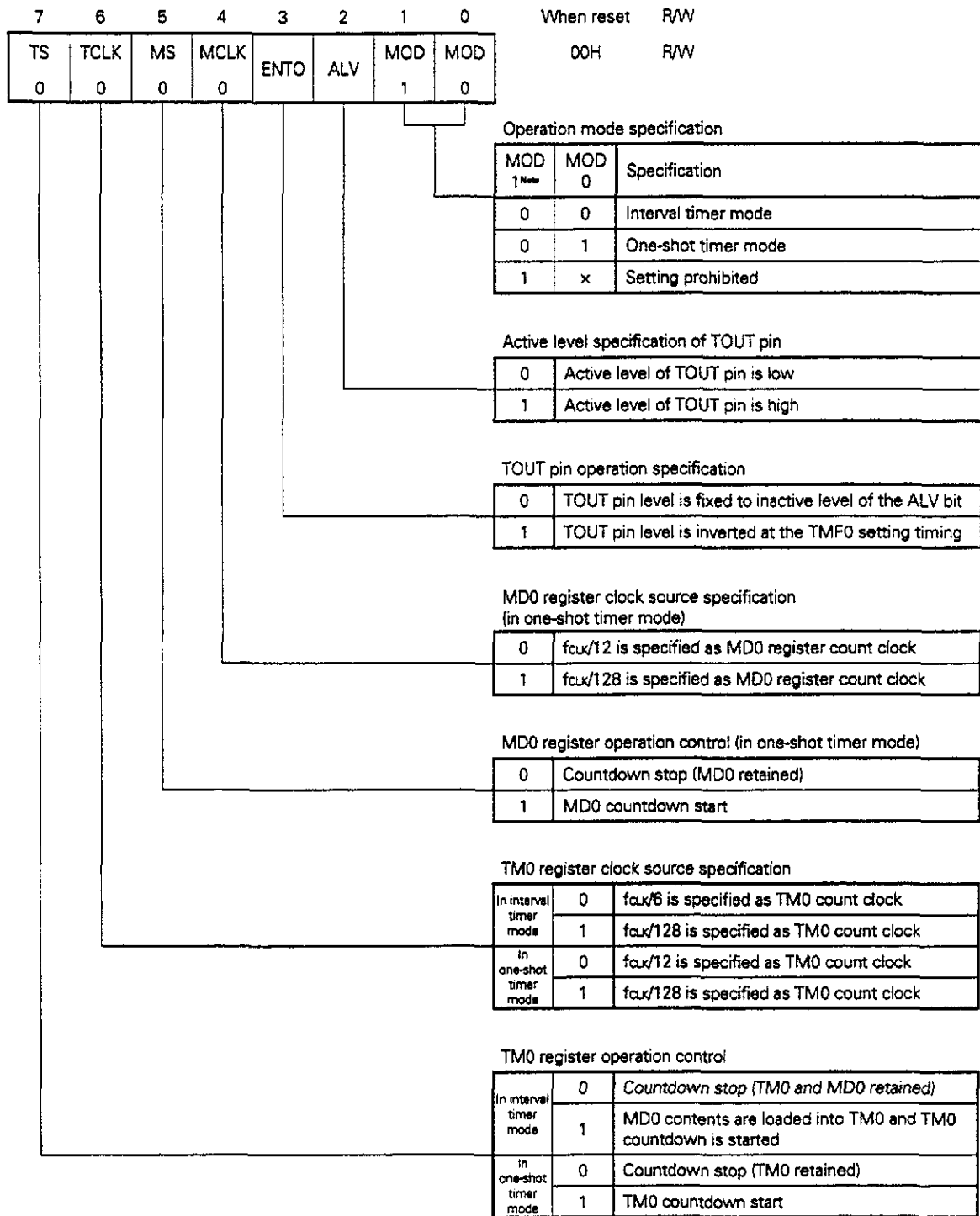**Table 9-2. TM0 and MD0 Count Time in One-shot Timer Mode**

When f_{CLK} = 8 MHz

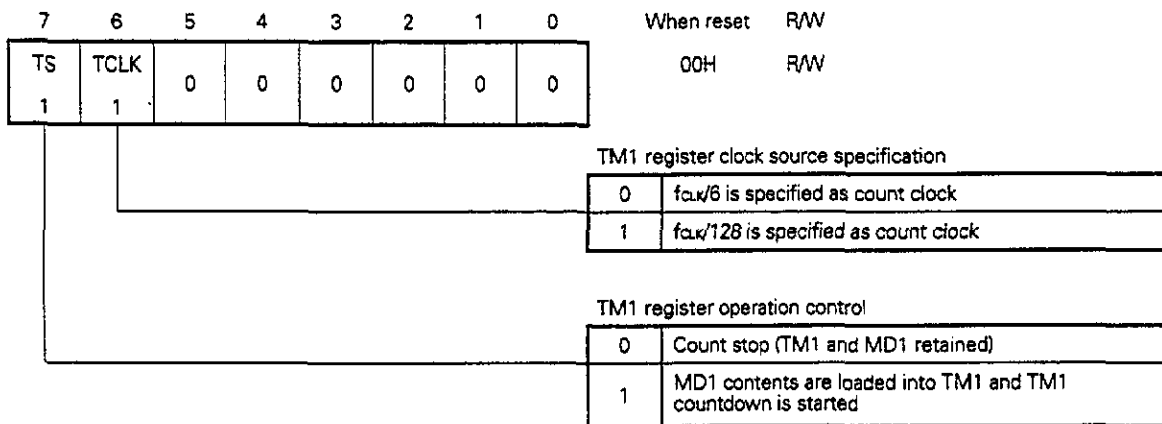| TCLK0/ MCLK0	Count clock	Resolution	Full count
0	f_{CLK}/12	1.5 μs	98.3 ms
1	f_{CLK}/128	16 μs	1.04 s

Caution **The TM0 register count clock when the interval timer mode is set differs from that when the one-shot timer mode is set.**

Figure 9-4. TMC0

7	6	5	4	3	2	1	0
TS	TCLK	MS	MCLK	ENTO	ALV	MOD	MOD
0	0	0	0			1	0

When reset   R/W
00H   R/W

Operation mode specification

MOD 1[Note]	MOD 0	Specification
0	0	Interval timer mode
0	1	One-shot timer mode
1	×	Setting prohibited

Active level specification of TOUT pin

0	Active level of TOUT pin is low
1	Active level of TOUT pin is high

TOUT pin operation specification

0	TOUT pin level is fixed to inactive level of the ALV bit
1	TOUT pin level is inverted at the TMF0 setting timing

MD0 register clock source specification
(in one-shot timer mode)

0	$f_{clk}/12$ is specified as MD0 register count clock
1	$f_{clk}/128$ is specified as MD0 register count clock

MD0 register operation control (in one-shot timer mode)

0	Countdown stop (MD0 retained)
1	MD0 countdown start

TM0 register clock source specification

In interval timer mode	0	$f_{clk}/6$ is specified as TM0 count clock
	1	$f_{clk}/128$ is specified as TM0 count clock
In one-shot timer mode	0	$f_{clk}/12$ is specified as TM0 count clock
	1	$f_{clk}/128$ is specified as TM0 count clock

TM0 register operation control

In interval timer mode	0	Countdown stop (TM0 and MD0 retained)
	1	MD0 contents are loaded into TM0 and TM0 countdown is started
In one-shot timer mode	0	Countdown stop (TM0 retained)
	1	TM0 countdown start

Note Be sure to write "0" into MOD1.

Figure 9-5. TMC1

7	6	5	4	3	2	1	0	When reset	R/W
TS 1	TCLK 1	0	0	0	0	0	0	00H	R/W

TM1 register clock source specification

0	f$_{CLK}$/6 is specified as count clock
1	f$_{CLK}$/128 is specified as count clock

TM1 register operation control

0	Count stop (TM1 and MD1 retained)
1	MD1 contents are loaded into TM1 and TM1 countdown is started

9.3 Timer Unit Interrupt Requests

Three interrupt requests (TMF0 to TMF2) occur from the timer unit. Their occurrence conditions vary depending on the timer operation mode specification.

When the interval timer mode is set, TMF0 is set to 1 when the TM0 register value is set to 0 by counting down, and TMF1 and TMF2 are set to 1 when the TM1 register value is set to 0 by counting down. (See **Figure 9-6 (a)**.)

When the TM0 and MD0 registers are set to the one-shot timer mode, TMF0 is set to 1 when the TM0 register value is set to 0 by counting down, and TMF1 is set to 1 when the MD0 register value is set to 0 by counting down. In this case, TMF2 is set to 1 when the value of the TM1 register operating as interval timer changes to 0 by counting down.

Figure 9-6. Interrupt Requests Occurring from Timer Unit

(a) When TM0 and MD0 are set to interval timer mode
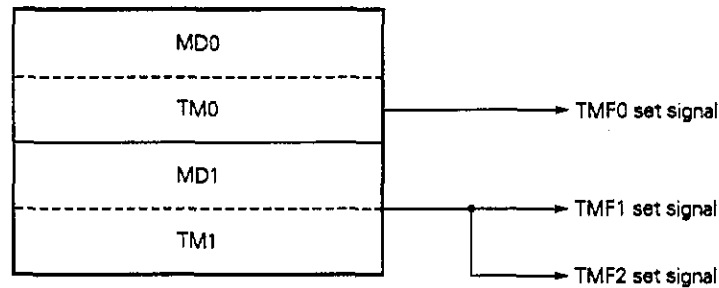
(b) When TM0 and MD0 are set to one-shot timer mode
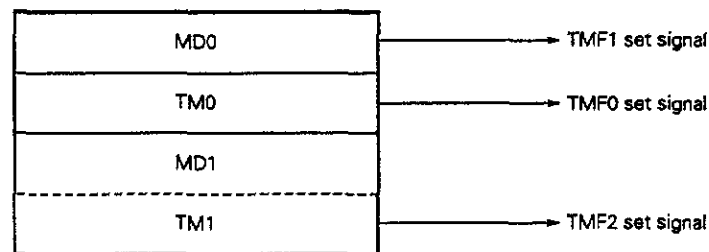
TMF0 to TMF2: Timer unit interrupt request flags 0 to 2

9.3.1 Timer unit interrupt request control registers (TMIC0, TMIC1, and TMIC2)

The TMICn register (n = 0 to 2) is an 8-bit register that controls the corresponding three interrupt requests that occur from the timer unit. These three interrupt requests make up one group and the priority level is programmable as a timer unit interrupt request group. The priority levels in the group are fixed as follows.

TMF0>TMF1>TMF2

Figure 9-7. TMIC0, TMIC1, and TMIC2

	7	6	5	4	3	2	1	0
TMIC0	TMF0	TMMK0	MS/$\overline{INT}$	ENCS	0	PR2	PR1	PR0
TMIC1	TMF1	TMMK1	MS/$\overline{INT}$	ENCS	0	1	1	1
TMIC2	TMF2	TMMK2	MS/$\overline{INT}$	ENCS	0	1	1	1

Caution **Bits 2 to 0 of TMIC1 and TMIC2 are fixed to 1. The TMIC1 and TMIC2 interrupt request priority levels conform to the TMIC0 PR2 to PR0 settings.**

For details of the TMICn register bits, see section **4.8 Interrupt Request Control Register**.

The registers can be written/read by making an 8-bit or 1-bit memory access, in which case one wait state is inserted.

When $\overline{RESET}$ is input, the TMICn register contents are initialized to 47H.

9.3.2 Timer unit macro service control registers (TMMS0, TMMS1, and TMMS2)

The TMMS0 to TMMS2 registers are 8-bit registers that control macro service which is started when three types of interrupt requests occur from the timer unit.

The TMMS0 register is used to control the macro service that is started when the TMF0 flag is set.

The TMMS1 register is used to control the macro service that is started when the TMF1 flag is set, and the TMMS2 register is used to control the macro service started when the TMF2 flag is set.

The registers can be written/read by making an 8-bit or 1-bit memory access, in which case one wait state is inserted.

Figure 9-8. TMMS0, TMMS1, and TMMS2

7	6	5	4	3	2	1	0
MSM 2	MSM 1	MSM 0	DIR	0	CH 2	CH 1	CH 0

For details of the TMMSn register bits, see section **4.5.4 Macro service control register**.