CHAPTER 12 STANDBY FUNCTION

The µPD70325 and 70335 each contain the following two operation clock control modes for the standby function intended for low power consumption.

- HALT mode ....Stops CPU operation clock only. The CPU status and the data contents and internal RAM contents are all retained. Peripheral hardware operation is continued.
  Total system power consumption can be lowered by intermittent operation using the HALT mode in combination with the normal operation mode.

- STOP mode ....Stops the oscillator and the entire internal circuitry.
  The internal RAM contents and output data on ports are retained by consuming very low power.

The HALT or STOP mode is set by executing the HALT or STOP instruction.

12.1 Standby Control Register (STBC)

The standby control register (STBC) is an 8-bit register which contains a standby flag (SBF). The high-order seven bits are fixed to 0.

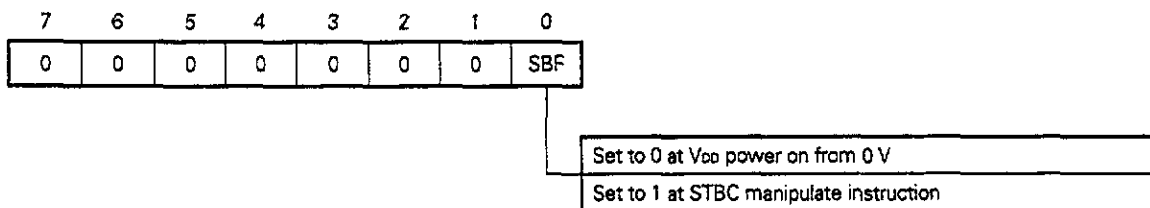The SBF flag is used to decide a return from the STOP mode.

The SBF flag is set to 1 only by executing an instruction. The flag is cleared (to 0) only when the supply voltage (Vdd) rises from 0 V; it is not cleared by executing any instruction.

Therefore, the SBF flag can be tested to determine a reset start when the power is turned on (SBF = 0) or a return from the STOP mode (SBF = 1[Note]).

The STBC register is not initialized when the $\overline{\text{RESET}}$ signal is input.

Note Preset the SBF flag to 1 before entering the STOP mode.

Figure 12-1. STBC

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SBF

Set to 0 at Vdd power on from 0 V
Set to 1 at STBC manipulate instruction

12.2 HALT Mode

The HALT mode stops the CPU operation clock.

The entire system's power consumption can be reduced by setting the HALT mode at the CPU idle time. The HALT mode is set by executing the HALT instruction.

In the HALT mode, the CPU clock stops and program execution is stopped, but the contents of all registers and on-chip RAM just before the HALT mode is entered are retained. Table 12-2 lists the hardware states.

12.2.1 HALT mode release

The HALT mode is released when a nonmaskable interrupt (NMI) or an unmasked maskable interrupt request occurs or when $\overline{\text{RESET}}$ is input. (See **Figure 12-2.**)

If an unmasked interrupt request, macro service request, or DMA request occurs just after the transition to the HALT state is made by executing the HALT instruction, the instruction that immediately follows the HALT instruction is executed. Therefore, place one or more NOP instructions immediately after the HALT instruction.

When a macro service request or DMA request occurs, the HALT mode is released and macro service or DMA processing is started (see **Figure 12-3.**) When the macro service or DMA processing terminates, a return is again made to the HALT mode. However, the HALT mode is released when the condition described in Table 12-1 arises during the macro service or DMA processing.

(1) HALT mode release when an interrupt occurs

(a) When interrupt service routine sets HALT mode

The HALT mode is released when a nonmaskable interrupt request or an unmasked maskable interrupt request having a higher priority level than the interrupt being serviced occurs.
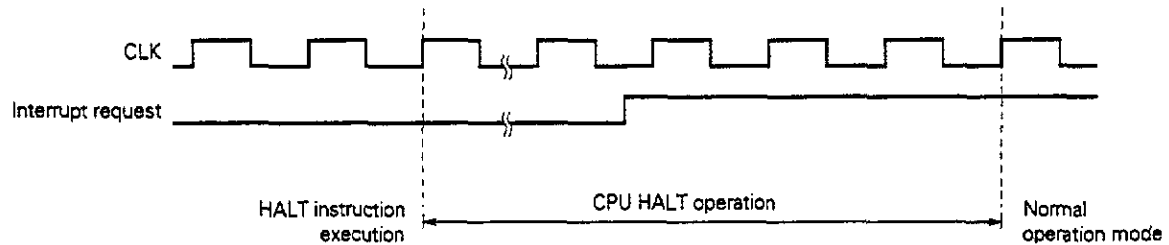
(b) Other than (a)

The HALT mode is released when a nonmaskable interrupt request or an unmasked maskable interrupt request occurs regardless of the priority level.
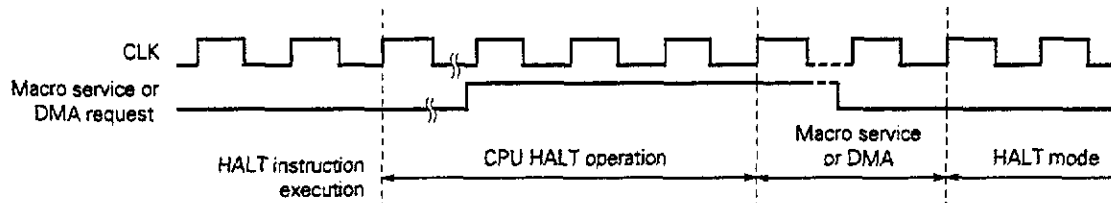
(2) HALT mode release when $\overline{\text{RESET}}$ is input

Same as the normal reset operation.

Figure 12-2. HALT Mode Release when Interrupt Request Occurs

Figure 12-3. Macro Service or DMA Start during HALT Mode

Table 12-1. Operation after HALT Mode is Released when Interrupt Request Occurs

Release source	EI state	DI state
Nonmaskable interrupt request	A branch is taken to the vector address after the HALT mode is released.	A branch is taken to the vector address after the HALT mode is released.
Maskable interrupt request	A branch is taken to the vector address after the HALT mode is released.	The next instruction is executed after the HALT mode is released.
Macro service request	If the macro service is started and the macro service counter is set to 0H or a transfer data match is found in the character search mode, a branch is taken to the vector address. If the macro service counter is not set to 0H or a transfer data match is not found in the character search mode, the HALT mode is entered again.	If the macro service is started and the macro service counter is set to 0H or a transfer data match is found in the character search mode, the HALT mode is released and the next instruction is executed.
DMA request	If DMA is started and the terminal counter is set to FFFFH, a branch is taken to the vector address. If the terminal counter is not set to FFFFH, the HALT mode is entered again.	If DMA is started and the terminal counter is set to FFFFH, the HALT mode is released and the next instruction is executed.

12.3 STOP Mode

The STOP mode stops the oscillator.

The STOP mode is useful when the entire application system stops. This mode enables very low power consumption. The STOP mode is set by executing the STOP instruction. In the STOP mode, all clocks stop. Although program execution is stopped, the contents of all registers and on-chip RAM just before the STOP mode is set are retained. Table 12-2 lists the hardware states.

Caution **In the STOP mode, the X1 and X2 pin levels are fixed. Therefore, do not use the STOP mode when using an external clock. Use a crystal or ceramic resonator when using the STOP mode.**

12.3.1 STOP mode release
The STOP mode is released when an NMI request occurs or when $\overline{\text{RESET}}$ is input.

(1) STOP mode release when NMI request occurs (Figure 12-4)
When a valid edge is input to the NMI pin, the oscillator restarts oscillation. The time base counter (TBC) also starts operation. After the STOP mode is released, the clock is not immediately supplied. Instead, clock supply is started after the oscillation stabilization time is counted by the TBC. To count the oscillation stabilization time, the TBC uses a half of the interval time specified in the processor control register (PRC) bits 2 and 3 (TB0 and TB1). (However, any interrupt request occurring from the TBC at the time is disabled.) Set half of the interval time as 30 ms or more.

(2) STOP mode release when $\overline{\text{RESET}}$ is input ·
Same as normal reset operation.
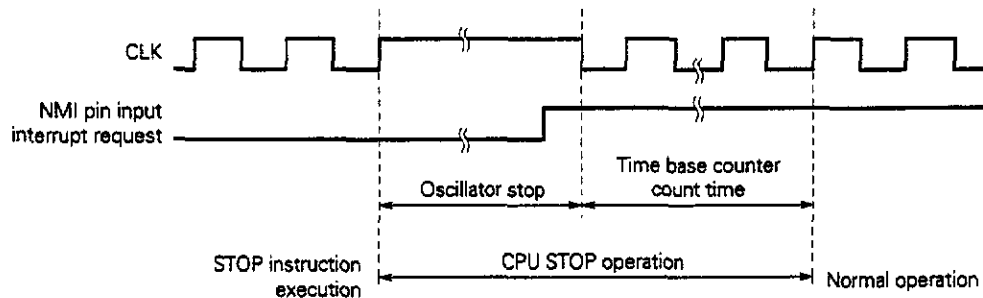
Figure 12-4. STOP Mode Release by Input to NMI Pin

Table 12-2. HALT Mode and STOP Mode

Item		HALT mode	STOP mode
Oscillator		Operation	Stop
Internal system clock		Stop	
16-bit timer		Operation	Stop
Time base counter			
HOLD circuit			
Serial interface			
Interrupt request controller			
DMA controller			
I/O line		Retention	Retention
Bus line	A0-A19	Retention	Retention
	D0-D15	High impedance	High impedance
R/W̄ output		High	High
Refresh operation		Operation or stop	Stop
Data retention		All internal data, such as CPU status and RAM contents, is retained.	All internal data, such as CPU status and RAM contents, is retained.
Release method		• Nonmaskable interrupt request • Maskable interrupt request • R̄ĒS̄ĒT̄ input • Macro service request[Note] • DMA[Note]	• Nonmaskable interrupt request • R̄ĒS̄ĒT̄ input

Note After the macro service or DMA processing terminates, a return is again made to the HALT mode.

[MEMO]