Exercise 1: Static behavior of the MOS transistor

TelcomBCN – UPC, DCISE QT10

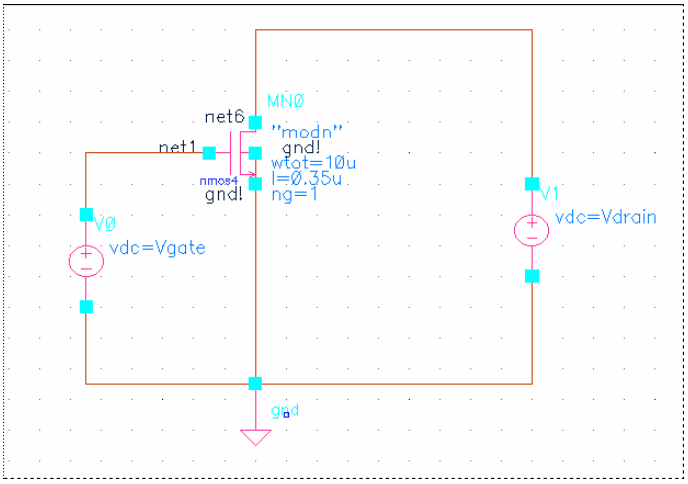
0. Introduction

This exercise addresses the analysis of the static behavior of the MOS transistor. Book equations modeling results for long and short channel behavior will be compared against the transistor model simulation results obtained from professional integrated circuit design environments. There is a first part (Pre-Lab) that you should complete before 1st October and up-load it to the Atenea web page. The second part (Lab) is done at the laboratory using Cadence tools for schematic capture and simulation. The results of the Lab should be written in a report and up-load it to the Atenea web page before 15th October. Criteria for the evaluation of this report are also available in Atenea. The lab section of this exercise should be completed in one session.

In this exercise the technological data for AMS 0.35µm process is required. Such information is found in the Appendix of this document.

1. Pre-Lab

Consider a NMOS transistor with W=10 µm and L=0.35 µm, connected as shown in the figure and implemented in a 0.35µm CMOS process with technology data shown in the appendix:



Long-channel equations:

a) Assuming a long-channel behavior, plot the $I_D(V_{DS})$ curves obtained from analytical calculations, for V_{DS} ranging from 0 to 3.3 V and for Vgate from 0 to 3.5 V, with 0.5 V increments (8 curves in the same graph).

Describe the analysis (type, variable to sweep, range, step, parameter analysis, etc.) necessary to obtain these curves with the Cadence environment.

b) Identify the regions of operations (choices are: cut-off, ohmic, saturation) of the transistor and write the numerical I_{DS} values (in mA) in the following tables:

Region of operation;

	Vdrain=0.5	Vdrain=2	Vdrain=3.5
Vgate=1			
Vgate=2			
Vgate=3,5			

I_{DS} current (in mA):

	Vdrain=0.5	Vdrain=2	Vdrain=3.5
Vgate=1			
Vgate=2			
Vgate=3.5			

c) Plot $I_D(V_{GS})$, for a fixed Vdrain=3.5 V. Compare this curve with the increase of I_D observed in the curves obtained in a). Which is the mathematical function that describes $I_D(V_{GS})$ in saturation[1]?

Describe the analysis (type, variable to sweep, range, step, parameter analysis, etc.) necessary to obtain these curves with the Cadence environment.

d) Imagine now that both W and L of the transistor are multiplied by a factor of 20 (ignore the effect of LD, WD). Would the curves obtained before change? Why?

Short-channel equations:

e) Calculate the V_{DS} saturation voltage due to carrier's velocity saturation (limit for short-channel behavior), from the technology values listed in the Appendix.

f) Repeat the $I_D(V_{DS})$ plot of question a), but now considering that the transistor may enter saturation due to carrier's velocity saturation (short-channel behavior). Do you think that the curves obtained are realistic?

h) Complete the tables related to the regions of operation (choices are now: cut-off, ohmic, Vgs-saturation, carrier-saturation) and I_{DS}:

Region of operation;

	Vdrain=0.5	Vdrain=2	Vdrain=3.5
Vgate=1			
Vgate=2			
Vgate=3.5			

I_{DS} current (in mA):

	Vdrain=0.5	Vdrain=2	Vdrain=3.5
Vgate=1			
Vgate=2			
Vgate=3.5			

i) Plot $I_D(V_{GS})$, for a fixed Vdrain=3.5 V. Compare this curve with the increase of I_D observed in the curves obtained in f), and what was obtained in question c). Comment the difference of the behavior observed using the long channel and the short channel equations.

j) Imagine now that both W and L of the transistor are multiplied by a factor of 20 (ignore the effect of LD, WD). Would the curves obtained before change? Why?

Design using load curves:

k) Read carefully the corresponding section "Design using load curves" of the Lab. Describe the procedure (steps to follow) and the analysis (type, variable to sweep, range, step, parameter analysis, etc.) necessary to determine the requested width value.

[1] There is no need to give a mathematical expression. Just identify the type of function.

PMOS transistor case:

l) Calculate the V_{DS} saturation voltage due to carrier's velocity saturation (limit for short-channel behavior) for a PMOS transistor with W=10 μm and L=0.35 μm, from the technology values listed in the Appendix.

m) Complete the tables related to the regions of operation of the PMOS transistor (choices are: cut-off, ohmic, Vgs-saturation, carrier-saturation) and I_{DS}. Assume Vsource=3.5 V

Region of operation;

	Vdrain=3	Vdrain=1,5	Vdrain=0
Vgate=2,5			
Vgate=1,5			
Vgate=0			

I_{DS} current (in mA):

	Vdrain=3	Vdrain=1,5	Vdrain=0
Vgate=2,5			
Vgate=1,5			
Vgate=0			

n) Draw the schematic and describe the type of analysis necessary to obtain $I_D(V_{DS})$ curves (for different values of Vgate, i.e. equivalent to the curves in a)) of a PMOS transistor with the Cadence environment.

2. Lab

In the lab sessions we will make extensive use of the DC analysis to check the real behavior of two MOS transistors with the same aspect ratio (10/0.35) in a 0.35 µm technology, one with L=0,35 µm (W=10 µm) and the other with L=7 µm, and acquire experience using Cadence capabilities.

The results of the Lab should be written in a written report and up-loaded to the Atenea web page before 15th October.

This report will be evaluated according to the following criteria:

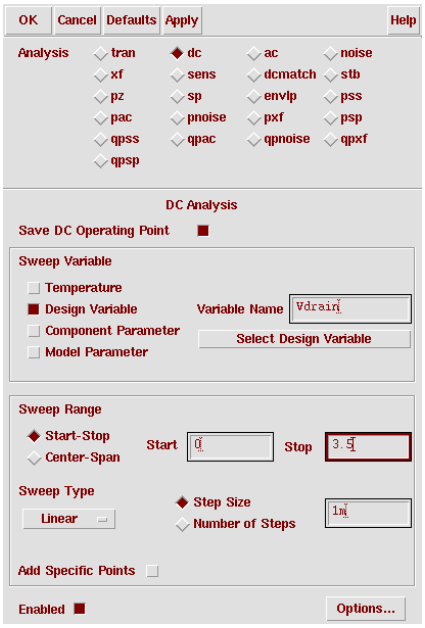
40% according % of work completed (number of questions answered)
20% according formal aspects (organization of the document; clear format; information provided in a direct, readable, concise and complete way)
40% according to the accuracy of results and the answers to questions 1 - 14.

The criteria used to evaluate each of these aspects are explained in the corresponding document found in the section of the Atenea web page corresponding to this exercise

Curves and regions of operation

Create a library called *Exercici1*. In this library, create a cell called *NMOS_test1*, view *schematic*. Create a schematic for testing a NMOS transistor, like that shown in the first page. Take the nmos4 cell from the PRIMLIB library, set *width*=10 um and *length*=0.35 um. Take the vdc sources from the analogLib library, specifying *Vdrain* and *Vgate* as DC voltages, respectively. There is no need to create a symbol for this schematic, since this will not be a hierarchical design.

Call the Analog Design Environment and set the required options in the Setup menu. Copy the variables from the schematic cellview and set the values *Vgate*=2.5 V and *Vdrain*=3.3 V. Set the drain current as an output to be plot. Specify a DC analysis for *Vdrain* ranging from 0 to 3.3 V. Make sure to switch the "Save DC Operating Point" option ON. Save the simulation state.



Obtain a set of curves as those of questions a) or f) of the Pre-Lab (with the same set of *Vgate* values).

1. For each of the curves generated, identify the points at which $Vdrain=Vgate-V_{THO}$.
2. Report the curves obtained from simulation and compare them against those obtained in questions a) and f) of the Pre-lab.

Obtain now the $I_D(Vgate)$ curves, with *Vdrain* parameterized from 0.5 to 3.5 V with 1 V linear steps.

3. Report the curves obtained from simulation and compare them against those obtained in the pre-lab, questions c) and h).
4. Why does the curve for *Vdrain*=0.5 show a behavior different than the rest?

5. Evaluate whether the transistor is more likely to behave as short-channel or long-channel according to the following criteria. Which is your conclusion?
   - → Current values
   - → Spacing between curves in the $I_D(V_{drain})$ plots
   - → V_{drain} at which saturation starts
   - → Function described by the $I_D(V_{gate})$ curves (V_{drain} > 2 V)

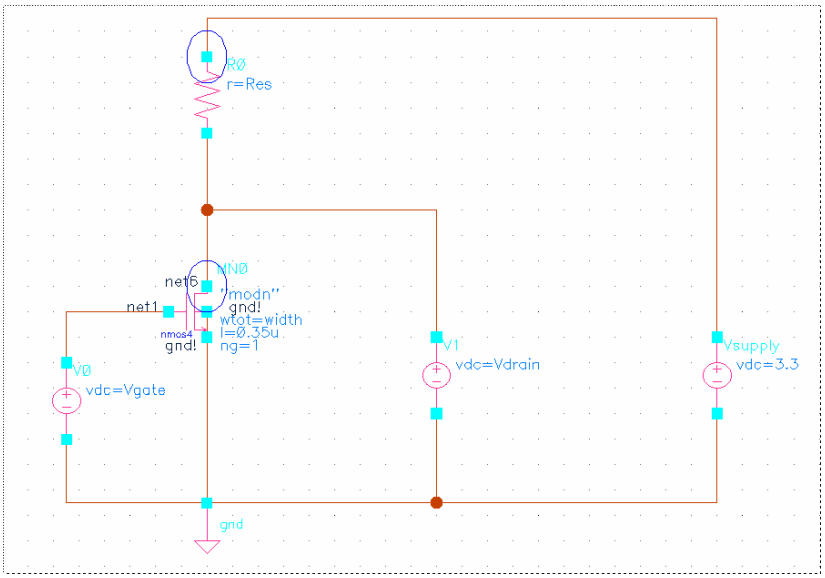
Copy now the former schematic into a new cellview called *NMOS_test2*. Edit the transistor in the schematic and modify the *width* and *length* values so that *length*=7 um while the 10/0.35 aspect ratio is preserved. Perform the same steps and simulations you did in the previous section until get the DC characteristic curves (you can load the simulation state of the *NMOS_test1* cell).

6. Report the $I_D(Vdrain)$ curves obtained from simulation and compare them against those obtained in the pre-lab, questions a) and f).
7. Report the $I_D(Vgate)$ curves obtained from simulation and compare them against those obtained in the pre-lab, questions c) and h).

8. Evaluate whether the transistor is more likely to behave as short-channel or long-channel according to the following criteria. Which is your conclusion?
   - → Current values
   - → Spacing between curves in the $I_D(V_{drain})$ plots
   - → V_{drain} at which saturation starts
   - → Function described by the $I_D(V_{gate})$ curves (V_{drain} > 2 V)

<u>Design using load curves.</u>

Open now the *NMOS_test1* and connect an ideal resistor (res symbol from the analogLib library) between the NMOS drain and a voltage source (named *Vsupply*) with a 3.3 DC voltage value. Set the value of the resistor to be 1K. Edit the transistor and set its width to a new variable called *width*.



We want to use the characteristic curves $I_D(V_{drain})$ of the NMOS transistor and the load curve of the resistor $I_{RES}(V_{drain})$ to graphically determine the transistor width that allows a 1.5 mA current when loaded with 1 KΩ resistor and its gate voltage is set to 2.5 V [2]. In the Analog Design Environment, make sure that *Vgate*=2.5 V.

Perform the analysis necessary to obtain graphically the desired width value with a 0.05 μm resolution.

9. Describe the analysis performed and report the plots obtained.
10. Which is the width value that you have obtained? Which is the aspect ratio W/L? Which is the drain voltage for a 1.5 mA current?
11. The former graphical method is equivalent to analytically solving a set of equations. Write this set of equations.
12. What would happen to I_D and V_{drain} if the transistor was replaced by another with the same aspect ratio, but L= 7 μm (justify your answer, don't make a new simulation)

PMOS transistor

Create a new schematic to obtain the $I_D(Vdrain)$ voltages for a PMOS transistor with *width*=10 um and *length*=0.35 um. Take the pmos4 cell from the PRIMLIB library. Make sure to connect the bulk to the source node. Fix a supply voltage of V_{DD}=3.5 V and create a parametric analysis sweeping *Vgate* from 0 to 3.5 V with 0.5 V increments.

13. Report the schematic created.
14. Report the curves obtained. Compare to the values obtained in the pre-lab, question m).

[2] Graphic design using characteristic curves used to be a common method. Now CAD tools allow faster methods. For example, you could edit the schematic to delete the voltage source connected to the drain, run a simple DC analysis sweeping the *width* variable, and find the value that gives you the desired current.

Appendix: Technology data

A.1 Transistor data.

All this data is approximate. It is intended to allow hand calculation with Sah equations. The actual model parameters used by the simulator are not exactly the same since more second order effects need to be considered. However, hand calculations using this data provide a good enough approximation for simulation results, especially in saturation region.

Parameter	Units	NMOS	PMOS	note
L_{min}	µm	0.35	0.35	
W_{min}	µm	0.35	0.35	
t_{ox}	nm	7.6	7.6	
V_{TH0}	V	0.5	-0.65	1
γ	$V^{0.5}$	0.58	-0.40	1
NSUB	$10^{15}/cm^3$	212	101	1
K’	A/V^2	$80 \cdot 10^{-6}$	$26 \cdot 10^{-6}$	2
λ	V^{-1}	0.08	-0.08	3
LD	µm	0.01	0.01	4
WD	µm	0.05	0.05	5
μ_o	cm^2/Vs	370	126	6

Notes:

1 Body effect: use the following equation:

$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi - V_{BS}} - \sqrt{2\phi}\right)$, where V_{BS} is the bulk-to-substrate voltage and ϕ is the substrate potential, calculated using the NSUB parameter (the doping concentration of the substrate):

$\phi = \frac{kT}{q}\ln\left(\frac{NSUB}{n_i}\right)$, with kT/q = 26 mV at 300ºK and $n_i = 1.5 \cdot 10^{10}$ cm^{-3} at 300ºK for silicon.

2 Gain parameter

This parameter is used in the current expression:

$$I_D = K'\frac{W_{eff}}{L_{eff}}\left(\left(V_{GS} - V_{TH}\right)V_{min} - \frac{V_{min}^2}{2}\right), \text{ with } V_{min} = \min\left\{\left(V_{GS} - V_{TH}\right), V_{DS}\right\}$$

3 Channel length modulation

The limitations of the simple Sah model makes this parameter value to be not very accurate. The student is warned to take the results obtained using this parameter only as approximate values. It is used to correct the current expression in the saturation region:

$$I_{DSAT} = \frac{K'}{2}\frac{W_{eff}}{L_{eff}}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right)$$

4 The effective channel length is calculated using the following expression:

$$L_{eff} = L - 2 \cdot LD$$

5 The effective channel width is calculated using the following expression:

$$W_{eff} = W - 2 \cdot WD$$

6 Carrier's mobility in the channel may be used to obtain a first-hand value for the saturation V_{DS} due to carrier's velocity saturation (short-channel behavior):

$$V_{DSsat} = v_{sat} \frac{L_{eff}}{\mu_o}$$, with $v_{sat} \sim 10^5$ m/s