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Grup 21

Simulation of the circuit: DC analysis

Simulation results analysis in WaveScan:

Q1: Measure the inverter threshold voltage ($V_{threshold}=V_{in}=V_{out}$).
Vth= 1'5V

Q2: Measure the input voltage for which the ouput is 90% of its maximum value.
90%Vdd = Vo = 2'97V → Vin= 1'2V

Q3: Measure the input voltage for which the ouput is 10% of its maximum value.
10%Vdd = Vo = 330mV → Vin= 1'69V

Q4: Which are (approximately) the threshold voltages of the NMOS and PMOS transistors?
Vtn ~ 0'5 V (quan la gràfica I(Vds) comença a baixar)
Vtp ~ -(Vdd – 2'6855 V) = -0'6145 V (quan la gràfica I(Vds) arriba pràcticament a 0).

Q5: Why are the currents negative?
Tal com hem definit els nodes en l'schematic ens surt d'aquesta manera.

Q6: Which is the current at the threshold voltage?
Ith = -1'13mA (mínim de la gràfica)

Q7: Which is the maximum current (absolute value)? At which V_{in} is this maximum current produced?
El corrent màxim el trobem a Vth = 1'13mA
El corrent mínim és pràcticament igual i nul durant els intervals [0,Vtn] volts i a [VDD+Vtp,VDD] volts.

Q8: Which is (approximately) the current at cutoff? (note that you will need to zoom)
Pràcticament nul. Fent zoom veiem que per a :
· NMOS: Icutoff ~ 1'7uA
· PMOS: Icutoff ~ 1'9uA

Results analysis using the calculator:

Q10. Which is the maximum value of dV_{out}/dV_{in} (absolute value)? At which V_{in} is this maximum produced?
Per a Vin=Vth=1'5V tenim un valor absolut $|dV_{out}/dV_{in}| = 17{,}43$.

Q11. Can you give now a better estimation of the threshold voltages of the NMOS and PMOS transistors?
Mesurant aquests valors desde la funció dV_{out}/dV_{in} obtenim uns valors de:
Vtn ~ 0'5 V
Vtp ~ 0'645 V

Time domain (TRAN) simulation

Simulation of the circuit: TRAN analysis

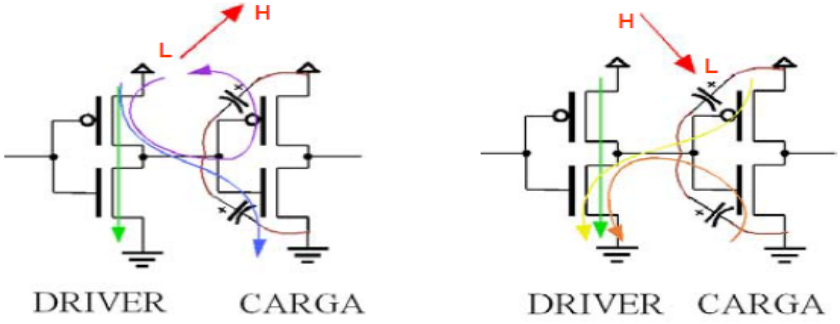
Q12. In which transitions of Vout do we have the highest current consumption?
En les transicions de Vout LH es consumeix aproximadament 5mA mentre que a les HL gairebé no passa d'1mA.
(veure la figura següent per entendre el sentit dels corrents al passar transicions LH o HL).

Q13. Use the cursors and zoom tools to measure the delay between input and output when a rise edge at
Vout occurs (measure it a $V_{DD}/2$)
TpLH ~ 0'5ns

Q14. Use the cursors and zoom tools to measure the delay between input and output when a fall

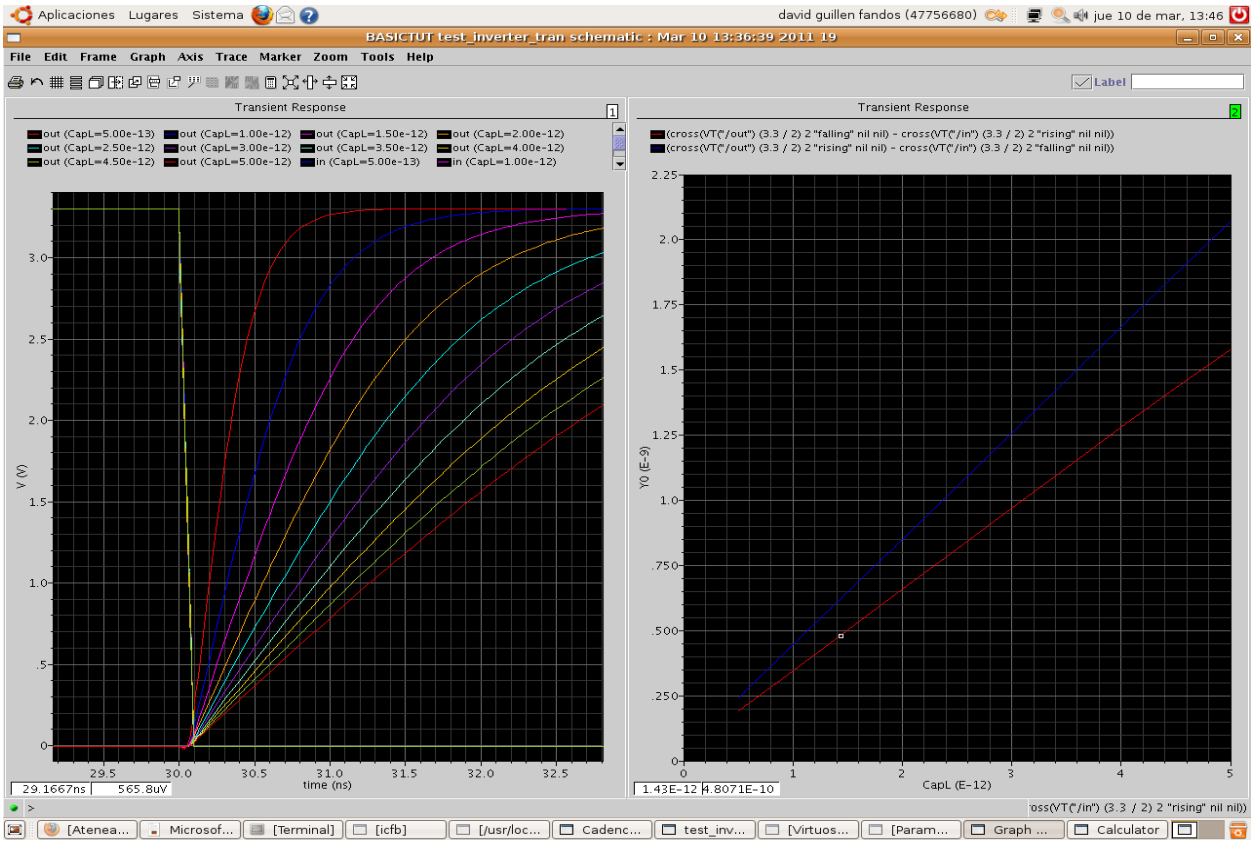
edge at
Vout occurs (measure it a $V_{DD}/2$)
TpHL ~ 0'4ns

Q15. Which delay is faster? Why?
TpLH > TpHL en les transicions de Vout. Degut a què Id pmos < Id nmos (els transistors tenen dimensions diferents, les constants kn' i kp' també etc.).
TpLH intervé el transistor PMOS: Id ↓ → Ron_eq_LH ↑ → TpLH ↑ (veure la figura següent)



Simulation of the circuit: Parametric analysis

Q16. Measure the delay between input and output for the rise edge at Vout for all the CapL values.
Q17. Represent graphically the delay dependence with the load capacitance.



Q18. Why the slope of tp_H_L and tp_L_H is different?
Com ja s'ha comentat a la Q15, per a valors constants del condensador CapL a la sortida de l'inversor, donades les característiques diferents del PMOS i NMOS, el temps de propagació de pujada (rising) de Vout TpLH és més gran que el de baixada (falling) TpHL.