# HN62318B Series
# HN62328B Series

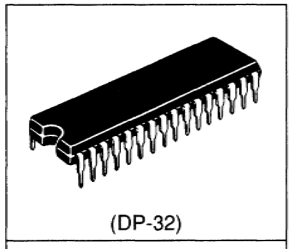
## 8M (1M x 8-bit) Mask ROM

### ■ DESCRIPTION

The Hitachi HN62318B/HN62328B Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 8-bit.

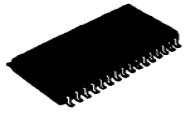
The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62318B/HN62328B is offered with JEDEC-standard pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages.



(DP-32)

(FP-32D)



(TTP-32D)

### ■ FEATURES

- Single Power Supply:
  $V_{CC}$ = 5 V ± 10%
- Fast Access Time:
  150 ns/200 ns (Max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

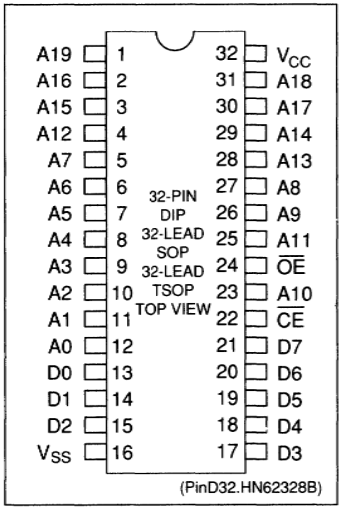
### ■ ORDERING INFORMATION

| Type No. | Access Time | Package |
|---|---|---|
| HN62318BP | 150 ns/200 ns | 32-pin Plastic DIP |
| HN62328BP | 150 ns/200 ns | (DP-32) |
| HN62318BF | 150 ns/200 ns | 32-lead Plastic SOP |
| HN62328BF | 150 ns/200 ns | (FP-32D) |
| HN62318BTT | 150 ns/200 ns | 32-lead Plastic TSOP |
| HN62328BTT | 150 ns/200 ns | (TTP-32D) |

### ■ PIN DESCRIPTION

| Pin Name | Function |
|---|---|
| $A_0$ - $A_{19}$ | Address |
| $D_0$ - $D_7$ | Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |
| NC | No Connection |

### ■ PIN ARRANGEMENT

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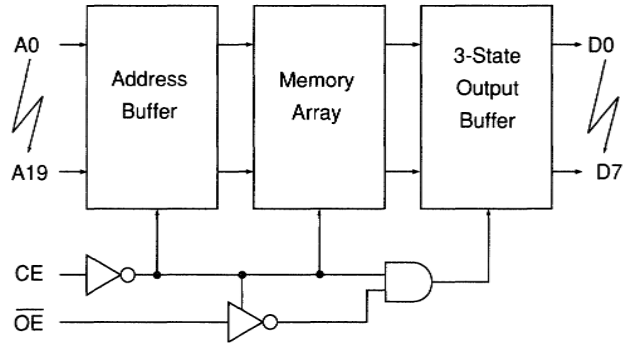
## ■ BLOCK DIAGRAM




(BD.HN62328B)

## ■ ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage [1] | $V_{CC}$ | -0.3 to +7.0 | V |
| Terminal Voltage [1] | $V_T$ | -0.3 to $V_{CC}$ + 0.3 | V |
| Operating Temperature Range | $T_{OPR}$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 to +125 | °C |
| Temperature Under Bias | $T_{BIAS}$ | -20 to +85 | °C |

Notes: 1. With respect to $V_{SS}$.

## ■ CAPACITANCE

($V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V, $T_a$ = 25°C, $V_{IN}$ = 0 V, f = 1MHz)

| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance [1] | $C_{IN}$ | - | 15 | pF |
| Output Capacitance [1] | $C_{OUT}$ | - | 15 | pF |

Notes: 1. This parameter is sampled and not 100% tested.

## ■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0 V, $T_a$ = 0 to 70°C)

| Item | Symbol | Min. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | - | 10 | µA | $V_{IN}$ = 0 to $V_{CC}$ |
| Output Leakage Current | $I_{LO}$ | - | 10 | µA | $\overline{CE}$ = 2.2 V, $V_{OUT}$ = 0 to $V_{CC}$ |
| Operating $V_{CC}$ Current | $I_{CC}$ | - | 50 | mA | $V_{CC}$ = 5.5 V, $I_{DOUT}$ = 0 mA, $t_{RC}$ = Min. |
| Standby $V_{CC}$ Current | $I_{SB}$ | - | 30 | µA | $V_{CC}$ = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V |
| Input Voltage | $V_{IH}$ | 2.2 | $V_{CC}$+0.3 | V | |
| | $V_{IL}$ | -0.3 | 0.8 | V | |
| Output Voltage | $V_{OH}$ | 2.4 | - | V | $I_{OH}$ = -205 µA |
| | $V_{OL}$ | - | 0.4 | V | $I_{OL}$ = 1.6 mA |

## ■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0 V, $T_a$ = 0 to 70°C)

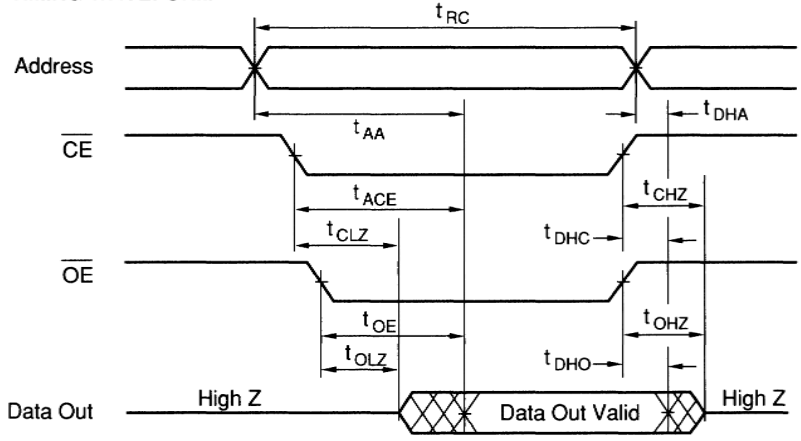
**Test Conditions**

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

| Item | Symbol | HN62318B | | HN62328B | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle Time | $t_{RC}$ | 150 | - | 200 | - | ns |
| Address Access Time | $t_{AA}$ | - | 150 | - | 200 | ns |
| $\overline{CE}$ Access Time | $t_{ACE}$ | - | 150 | - | 200 | ns |
| $\overline{OE}$ Access Time | $t_{OE}$ | - | 70 | - | 100 | ns |
| Output Hold Time from Address Change | $t_{DHA}$ | 0 | - | 0 | - | ns |
| Output Hold Time from $\overline{CE}$ | $t_{DHC}$ | 0 | - | 0 | - | ns |
| Output Hold Time from $\overline{OE}$ | $t_{DHO}$ | 0 | - | 0 | - | ns |
| $\overline{CE}$ to Output in High Z | $t_{CHZ}$ [1] | - | 70 | - | 70 | ns |
| $\overline{OE}$ to Output in High Z | $t_{OHZ}$ [1] | - | 70 | - | 70 | ns |
| $\overline{CE}$ to Output in Low Z | $t_{CLZ}$ | 10 | - | 10 | - | ns |
| $\overline{OE}$ to Output in Low Z | $t_{OLZ}$ | 10 | - | 10 | - | ns |

Note: 1. $t_{CHZ}$, and $t_{OHZ}$ define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

## ■ READ TIMING WAVEFORM




(TD.R.HN62328B)

Note: 1. $t_{DHA}$, $t_{DHC}$, $t_{DHO}$ are determined by the faster time.
2. $t_{AA}$, $t_{ACE}$, $t_{OE}$ are determined by the slower time.
3. $t_{CLZ}$, $t_{OLZ}$ are determined by the slower time.

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