Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

We learned the basics of how to use Vivado. We used verilog to make our board's leds light up when they met certain logic gate conditions.
We both worked on all parts of the lab together.
David Hedge
Jordan Clifton

Lab Questions

1 - Describe the stages of building a Verilog project in Vivado.

1. Create a project
2. Add files
3. Simulate the circuit
4. Fix any issues discovered during simulation
5. Compile the code
6. Program the device

2 - What is the value in looking at the elaborated design schematic?

An elaborated design schematic takes the code that has been written, and given it works, accurately displays the function in an easy to read visual format. It shows the outputs and inputs as well as what gates are implemented.

3 - Why should we simulate our designs frequently? What does the simulation do?

We should make sure to simulate our designs frequently because it results in a shorter feedback loop in what is a very lengthy build process. This helps us find and fix mistakes earlier on. The simulation.

Simulating creates a software-based simulation of our circuit. It allows us to narrow down problems in our designs that might otherwise be impossible to find.

Code Submission

Has also been submitted at the submission link.

https://github.com/davidhedge26/ECEL