Algorithm Final Project

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Problem

2016 D. Static Timing Analysis

Definition

Static Timing Analysis (STA) is a method that can find true paths. It then use critical paths to validate the timing performance of a design. Circuit designer use this method check whether a circuit meet certain timing requirement.

True Path is a path that can be responsible for the delay of a circuit.

False Path is a path that doesn't matter for the timing analysis.

Problem Description

Design a parallel STA program for combinational logic circuit under multicore environment. Need to handle floating-mode.

Input

- Verilog gate-level netlist.

Output

- List of true paths (critical paths).

Team

Group 24

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Schedule

Date	Item
5/3	Apply for contest.
5/4	Contest application deadline.
5/5	Start implementing it.
5/13	Finish basic function.
5/14	Start progress report.
5/17	Finish progress report.
5/18	Start optimization (parallelize it).
6/8	Alpha test.
6/10	Finish optimization.
6/11	Start documentation and presentation.
6/13	Finish documentation and presentation.
6/14	Project deadline.

Some Ideas

Use a directed graph to represent the circuit. Vertices represent gates, primary inputs and primary outputs. Edges represent wires. Edges has weights, represent delays.

Bibliography

- ICCAD 2016 Contest Problem D. Static Timing Analysis Description, by Chung-Ming Huang and Wei-Chang Tsai
- Fundamental Algorithms for System Modeling, Analysis, and Optimization, by Edward, Jaijeet, Sanjit and Stavros