Analog Lab project
(EE254)

Design a D-flip flop using transistors.

Group -15

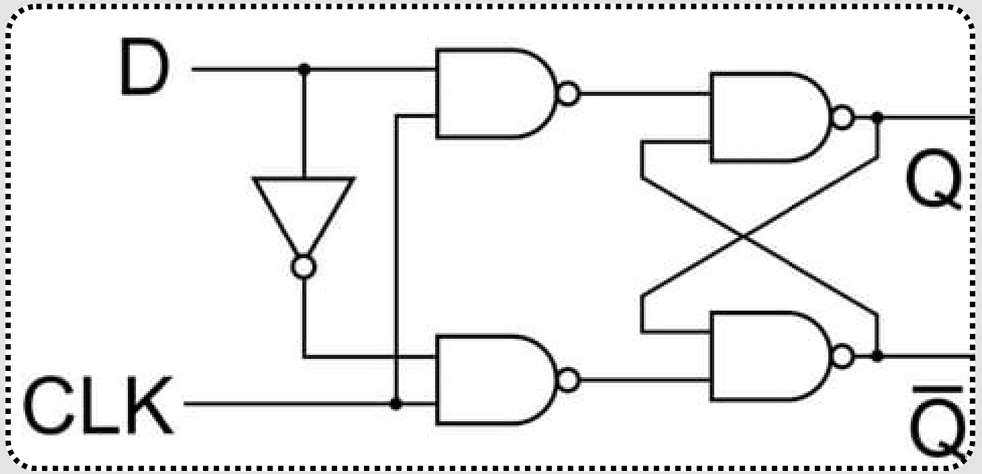
Members

Advait Varma	230002006
Himanshu	230002029
Praneet Masiya	230002055
David Kumar	230002022
Yash Shrivastava	230002067

Introduction

What is a D flip flop

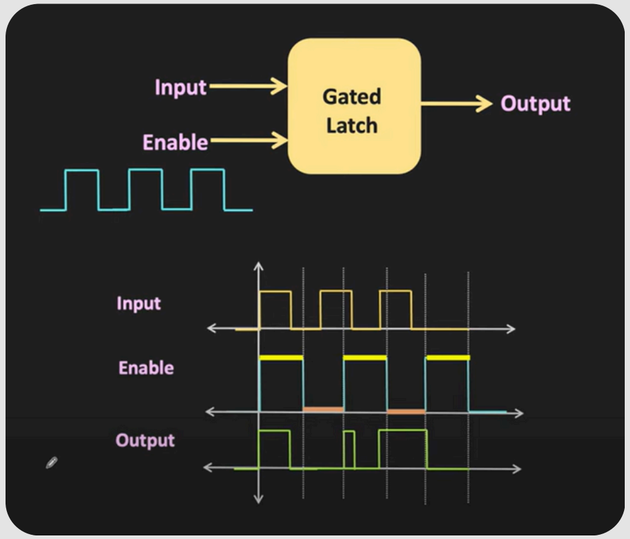
A D flip-flop, also known as a D-type or data flip-flop, is a digital storage element utilized in sequential logic circuits. It captures the value of the D (data) input at a specific part of the clock cycle, typically on the rising or falling edge of the clock signal, and holds this value until the next clock event. Hence, they are also known as Delay Flip Flop

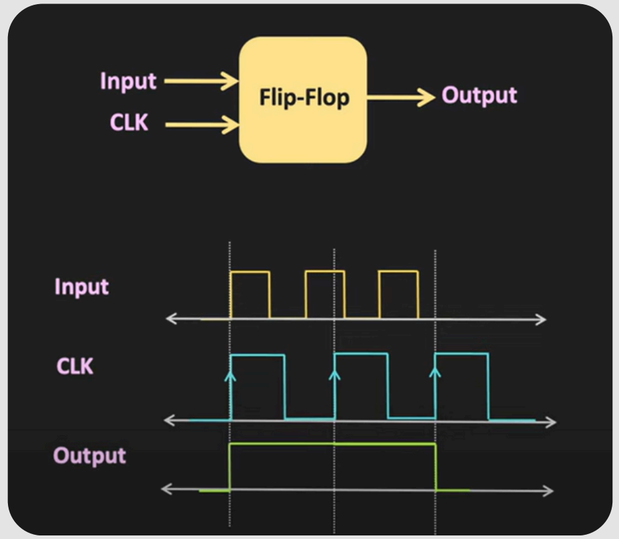


Context

Difference between A latch and a Flip Flop

The key difference between a latch and a flip-flop lies in their triggering mechanism: latches are level-triggered, responding to the continuous presence of input signals, while flip-flops are edge-triggered, responding only to changes (edges) of a clock signal.





Process

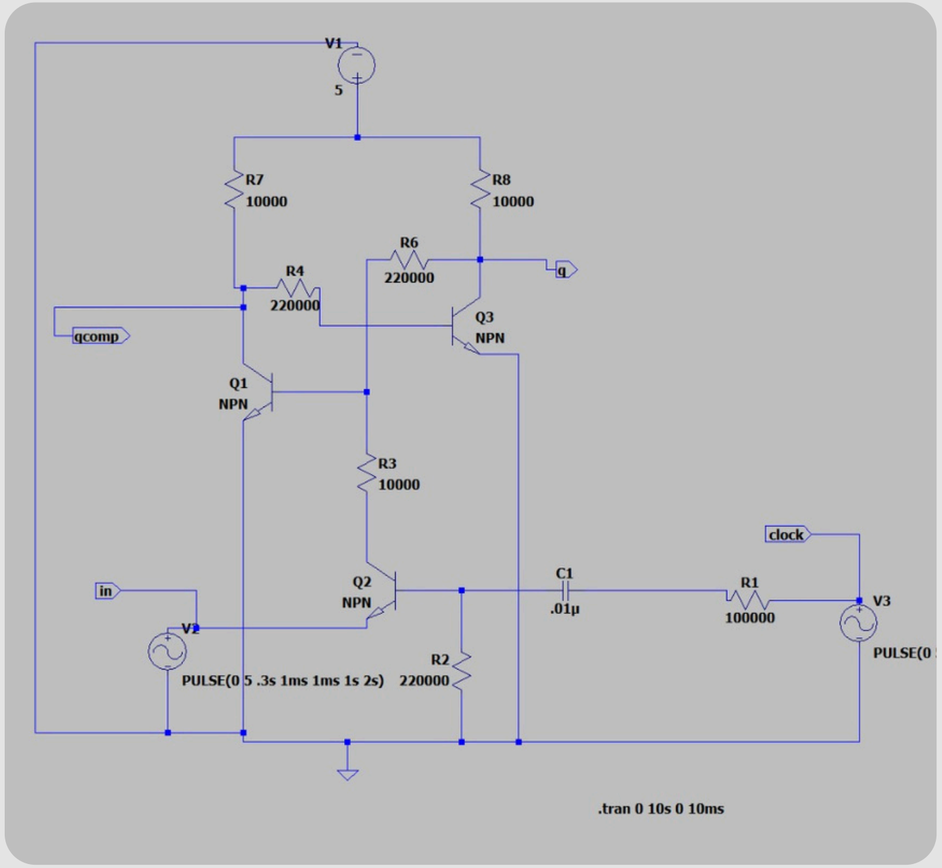
First We Made The Ideation That we Need to Make The logic gates First
The use of Components was too heavy And we Didnt wanted To rely on that Around 9-10 BJTs was required.

So we looked For a more optimized Approach , we considered creating the Flip flop using only Few BJTs, By Creating A basic SR latch.

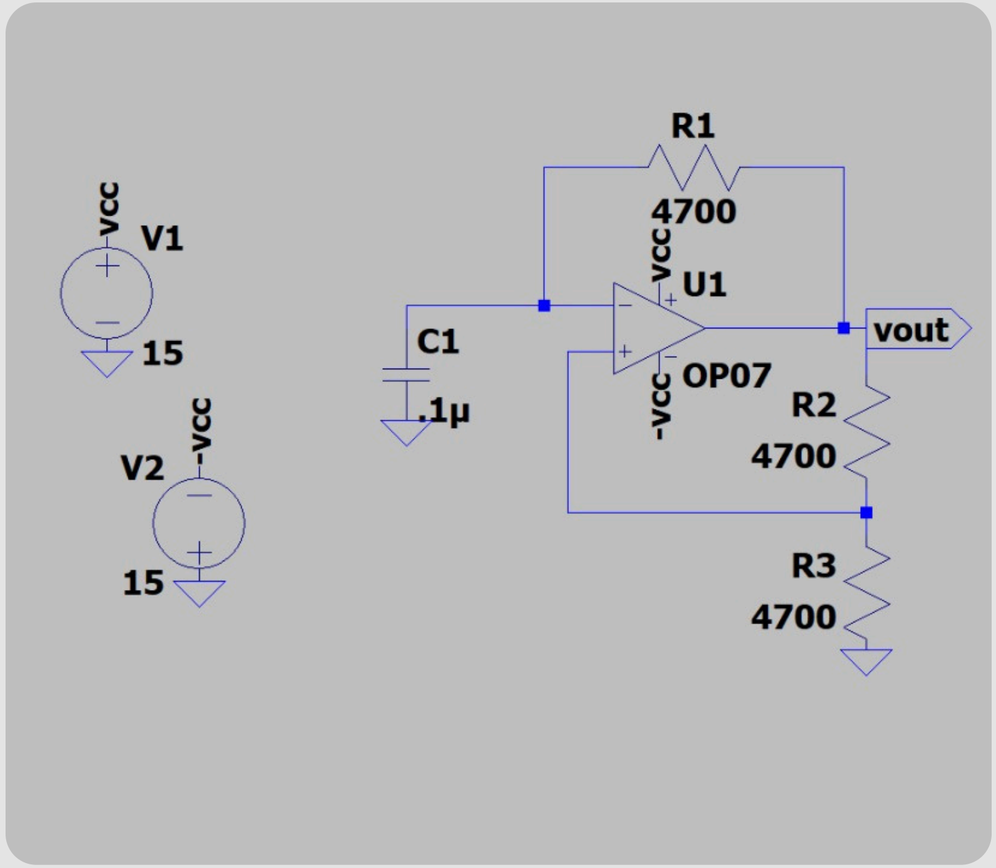
Then We Divided The Project into 2 parts

- Making D FlipFlop
- Making Astable Multivibrator using OP-AMP

Phases Of our Project



D flip Flop



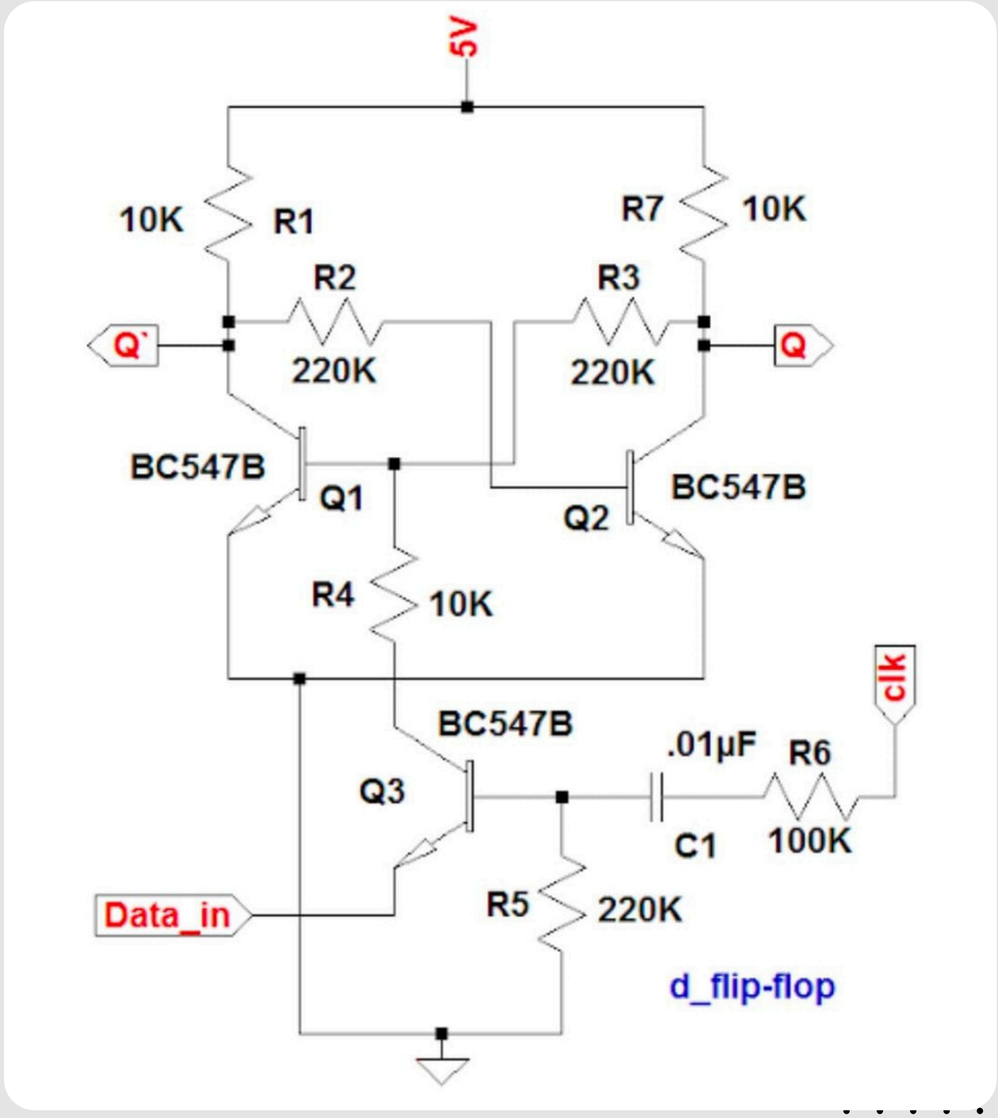
Astable MultiVibrator

D flip Flop

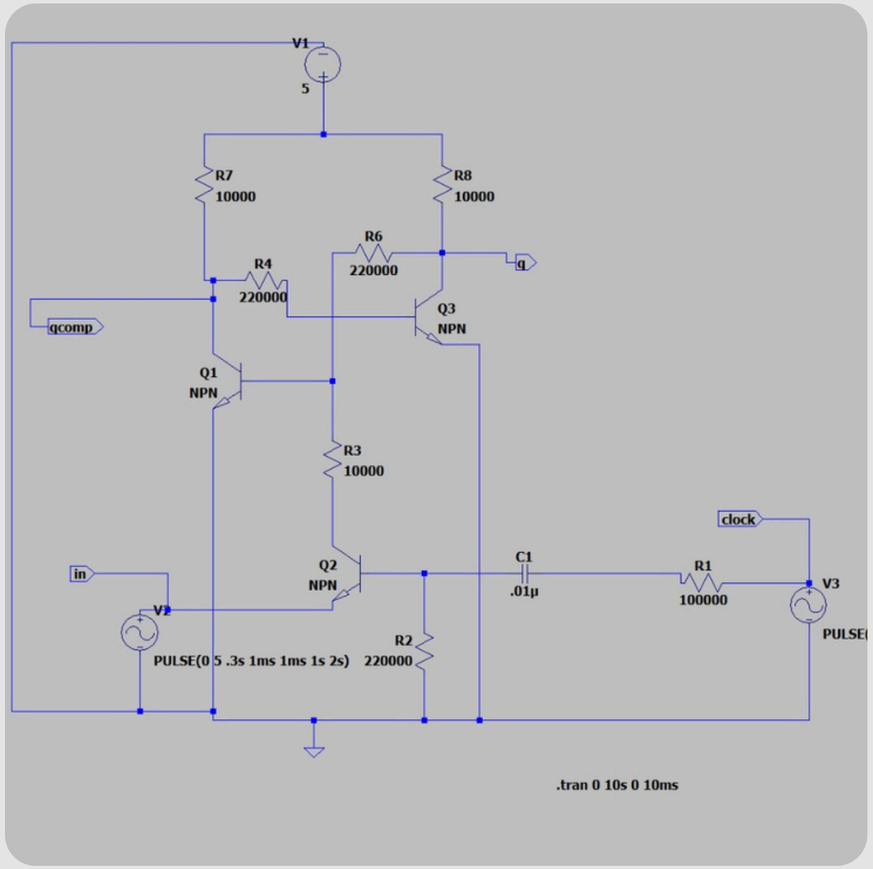
Here Instead of making Logic gates One by one and then Implementing the gates , We designed The flip Flop Only by using 3 BJTs (NPN). It operates By using the BJT in saturation Reigon

I.e Gates Were Not Neccessary

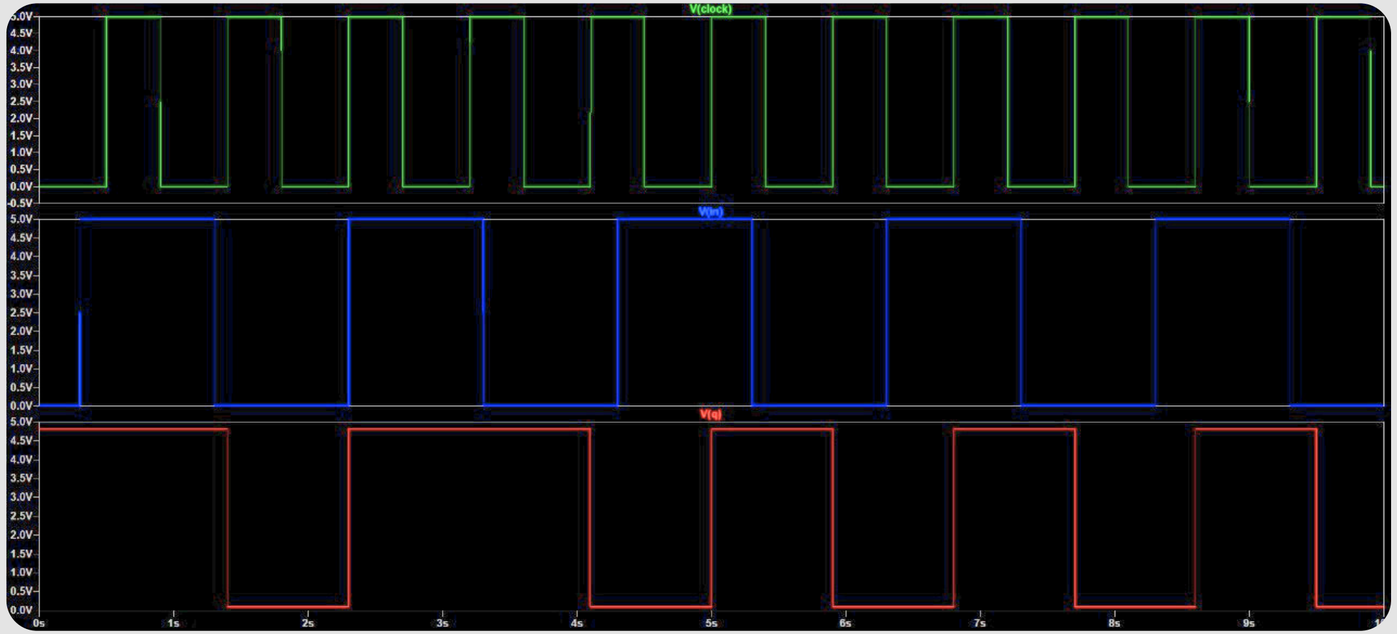
D	CLK	Q	Q`
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



D flip Flop



Schematic



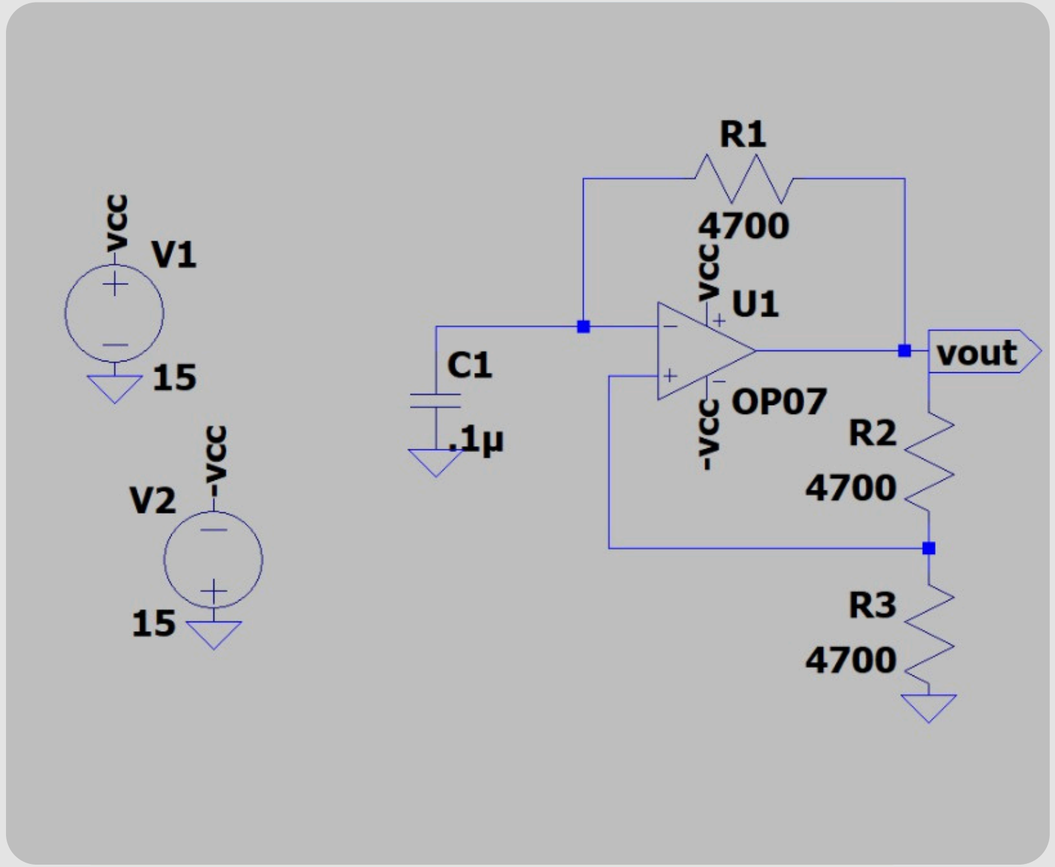
Output

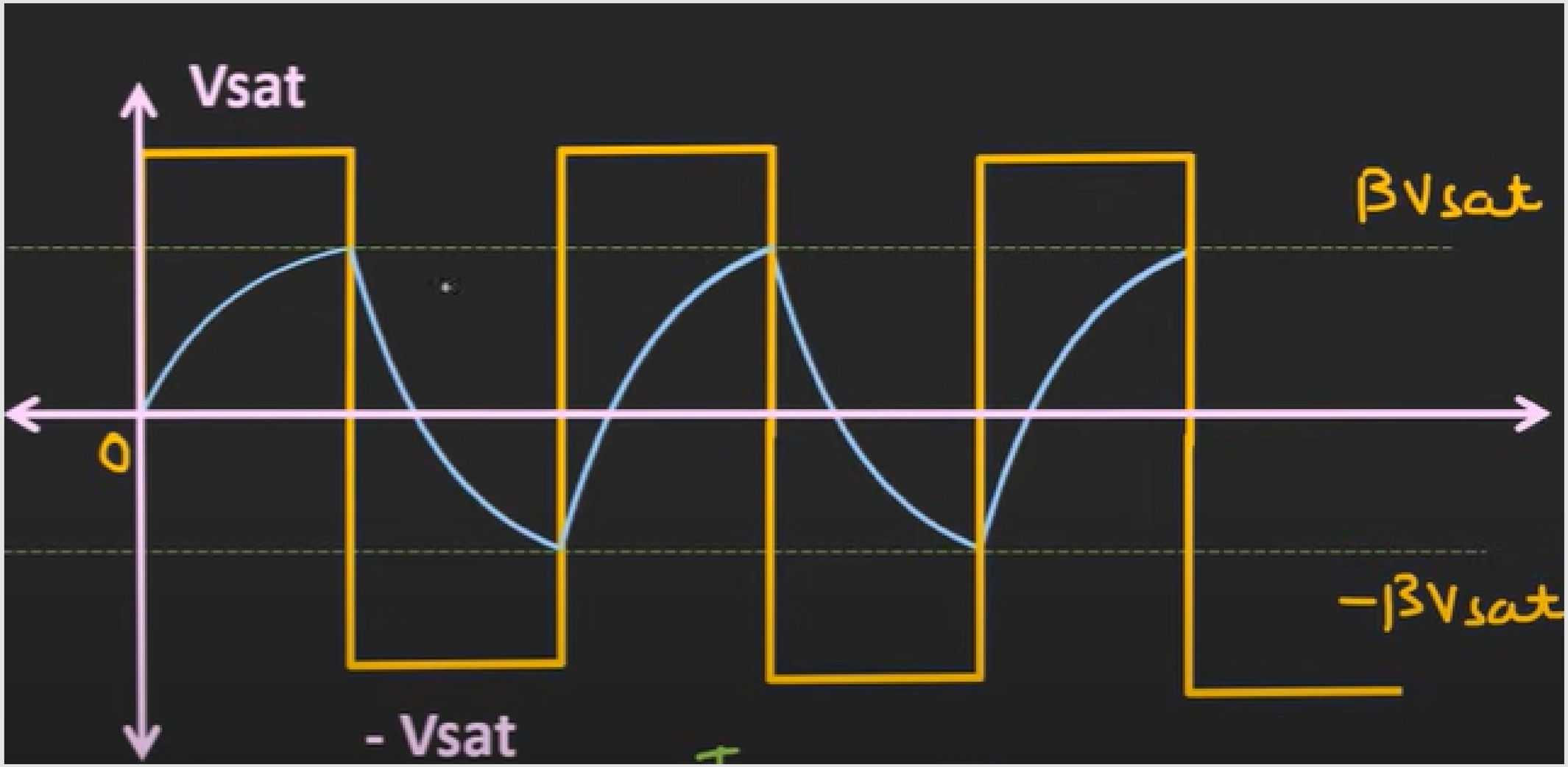
Green : clk
Blue : Vin
Red : Vout

Astable Multivibrator

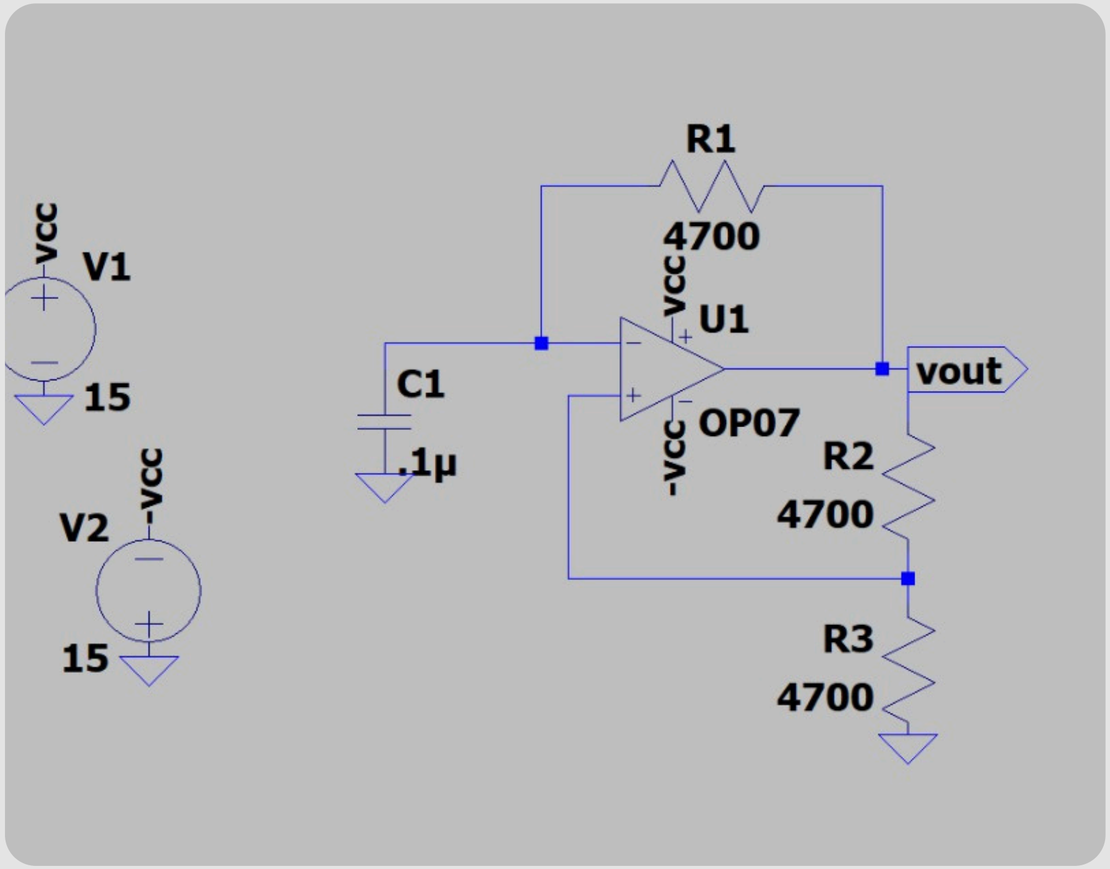
An astable multivibrator, also called a free-running multivibrator, is a circuit that continuously produces square waves or pulses without the use of an external trigger. The term “astable” refers to the absence of a stable state in this particular type of multivibrator.

$$T = 2\tau \ln \frac{1+\beta}{1-\beta}$$

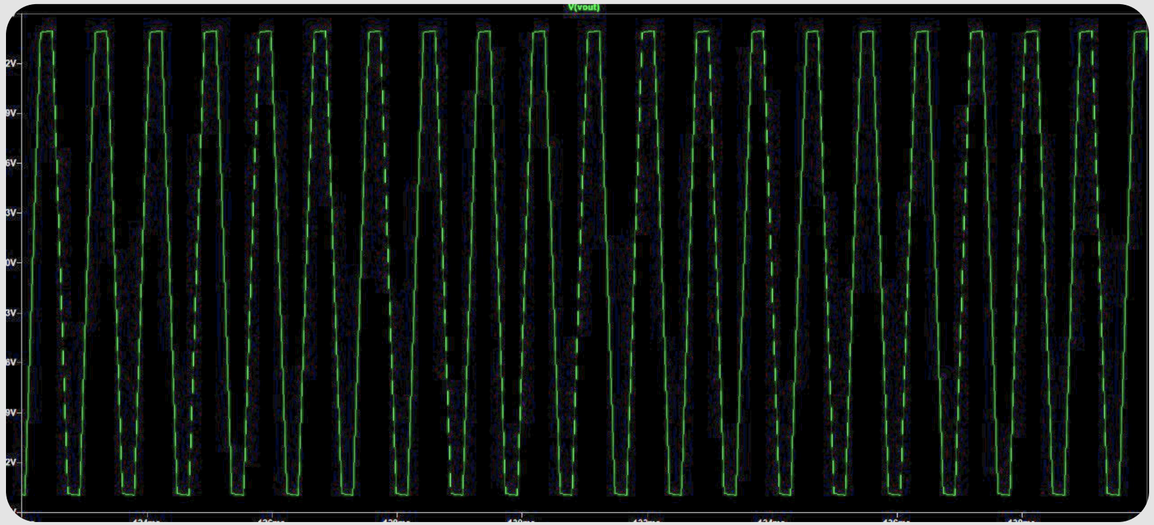



Vsat
βVsat
0
−βVsat
- Vsat

Astable Multivibrator

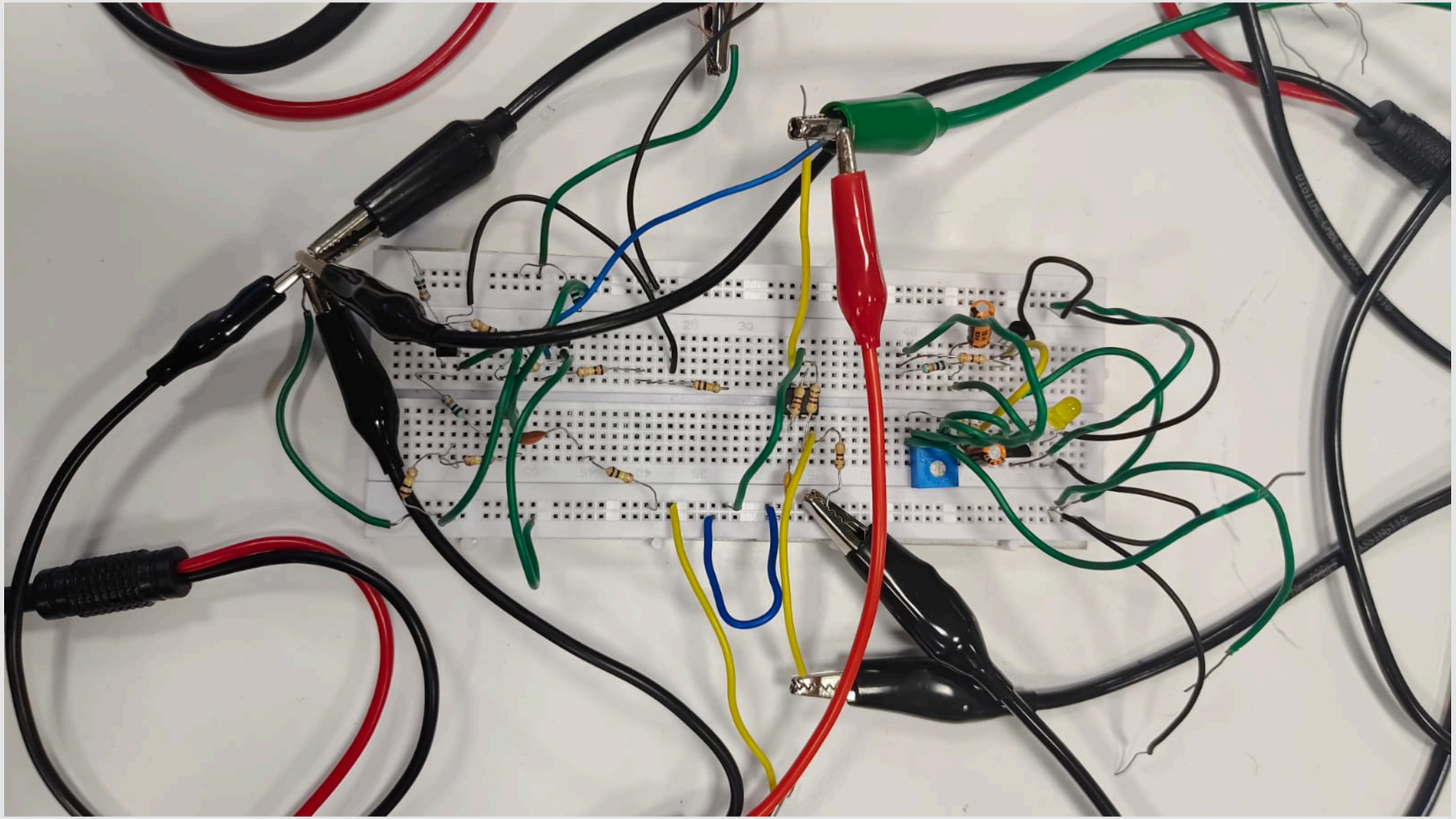


Schematic



Output

Final Circuit

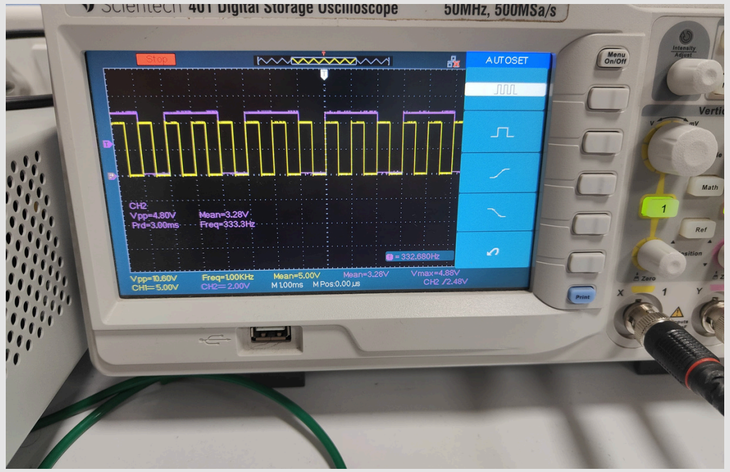


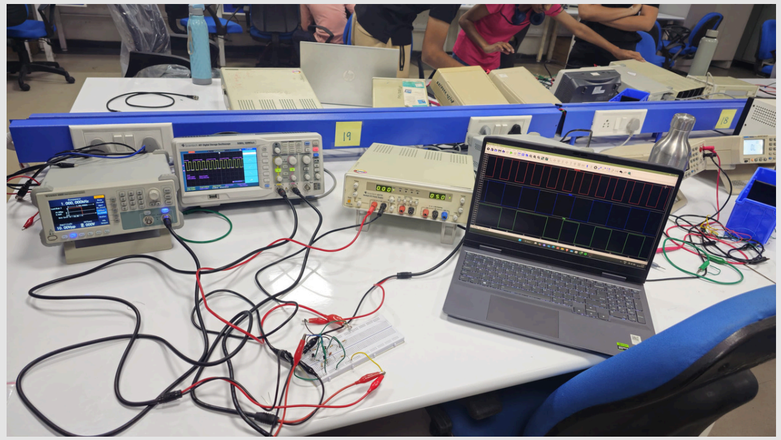
PROBLEMS FACED

WHEN IMPLEMENTING USING 4 GATES
WE NEEDED 11 BJTS WHICH OPENED A LOT OF SPACE FOR ERRORS
ALSO IT WAS NOT EFFICIENT AND FAST

WE FIRST USED ASTABLE MULTIVIBRATOR USING BJT FOR CLOCK SIGNAL , BUT WE GOT LOWER AMPLITUDE , SAME FOR FREQUENCY . THIS OCCURED DUE TO VALUE OF R&C

Results





The following circuit uses an astable multivibrator to generate the clock signal needed to drive the D flip-flop and produce the desired output. Initially, we built the astable multivibrator using BJTs (Bipolar Junction Transistors). However, during testing, we found that the output amplitude was low, and the frequency was also not stable.

To solve these issues, we replaced the BJT-based multivibrator with an Op-Amp-based multivibrator. Using the Op-Amp improved both the amplitude and the frequency stability of the clock signal, thereby enhancing the performance of the D flip-flop circuit.

Thank You