

The image contains two circuit diagrams for the Audio_Amps module, labeled 'Audio_Amps_Left' and 'Audio_Amps_Right'.

Audio_Amps_Left Diagram:

- Inputs:** L_LINE (red), L_FEEDBACK (green), L_BIAS (blue).
- Outputs:** TP29 L_AUDIO (red), TP30 L_BIASED (blue).
- Power:** +28V (red) and GND (green).
- File:** Audio_Amps.schematic

Audio_Amps_Right Diagram:

- Inputs:** R_LINE (red), R_FEEDBACK (green), R_BIAS (blue).
- Outputs:** TP32 R_AUDIO (red), TP33 R_BIASED (blue).
- Power:** +28V (red) and GND (green).
- File:** Audio_Amps.schematic

These terminals can be connected to the outputs to test the accuracy of the current outputs and test long-term reliability

High Voltage 28V Bus is boosted from 5V line using the Puleis U3V50AHV boost converter.

The line is then regulated using the TPS7A701 LDO.

Pin 3 of pot RV1 intentionally not connected

Optional Resistor to solder in if current draw is too low to regulate

5V UR

TP23 28V UR

U16

U13

TP24 28V

RV1

R24

R25

R26

C32

C33

C34

C35

C36

200K 1% Resistor 3360-1-200K

28V UR PRE

Optional Resistor to solder in if current draw is too low to regulate

Current Output Circuit CH1

CH1_CURSET
CH1_CURS
CH1_ENA
CH1_ENA_OUT
CH1_ENA_IN
CH1_ENA_OUT

CH1_OUT_A_PRE
CH1_OUT_B_PRE

File: current_circuit_sch

Current Output Circuit CH2

CH2_CURSET
CH2_CURS
CH2_ENA
CH2_ENA_OUT
CH2_ENA_IN
CH2_ENA_OUT

CH2_OUT_A_PRE
CH2_OUT_B_PRE

File: current_circuit_sch

This button must be pressed for current to flow out of either channel. This acts as an "e-stop," or "deadman's switch".

To send a signal to the MCU about the state of the button, we also switch the 28V divider. We have no more free pins on the MCU, so we will compare the signal of the 9V and 28V divider. If 28V /IN is high and the MCU reads 0 from the 9V/DIV, we know that the button is not pressed.

We accept that we will not have information on the 9V/DIV while not running the device

The diagram shows a green rectangular component labeled '53 TLA2010A'. It has several pins on its left and right sides. On the left, there are pins for '28V_DIV', '28V_DIV_PRES', and 'GND'. On the right, there are pins for 'NC_2,1', 'COM_2,1', 'NC_2,2', 'COM_2,2', 'NC_1,1', 'COM_1,1', 'NC_1,2', 'COM_1,2', 'NC_1,3', 'COM_1,3', and 'NC_1,4'. On the far right, there are pins for 'CH2_OUT_A_PRES', 'CH2_OUT_A', 'CH2_OUT_A_PRES', 'CH2_OUT_A', and 'CH2_OUT_A'. The circuit is connected to a 28V supply and a 9V supply. The 28V supply is connected to the '28V_DIV' pin. The 9V supply is connected to the '9V/DIV' pin. The button is connected to the '28V_DIV_PRES' pin. The button is also connected to the '9V/DIV' pin. The button is labeled '53 TLA2010A'.

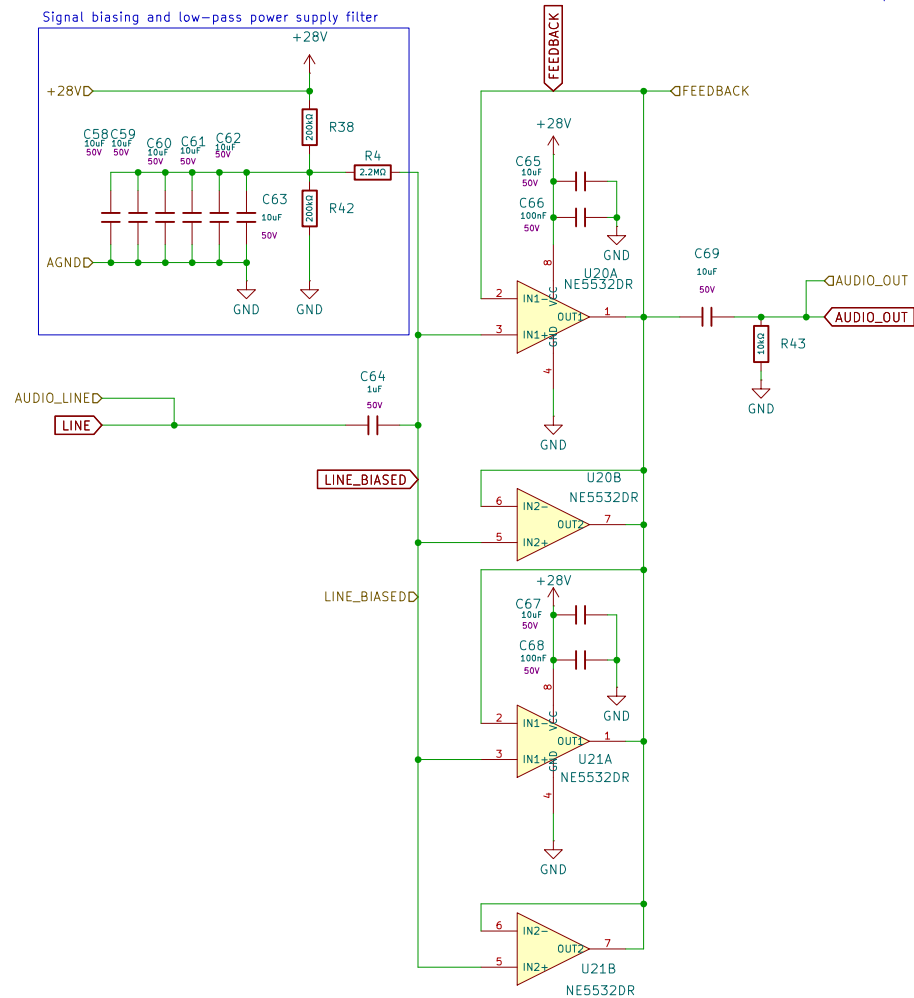
Putting holes for 0-ohm resistor in case SCK (MCT) needs to be bonded to GND

ESP-32-S3 Circuit Design courtesy of <https://www.instructables.com/Build-a-custom-ESP32-Boards-from-the-Scratch-the-Complete/>

ESP32-S3-MINI-1 Pin Functions:

Pin	Function
1	U0TXD/GPIO43/CLK_OUT1
2	U0RXD/GPIO44/CLK_OUT2
3	GPIO18/U0CTS/ADC2_CH5/XTAL_32K_P
4	GPIO20/U1CTS/ADC2_CH9/CLK_OUT1/USB_D+
5	GPIO19/U1RTS/ADC2_CH8/CLK_OUT2/USB_D-
6	GPIO17/TOUCH18/ADCL_CH7/SUBSPICLK
7	GPIO12/TOUCH12/ADCL_CH2/FSPIQ/FSPI0T/SUBSPICLK
8	GPIO13/TOUCH13/ADCL_CH3/FSPIQ/FSPI0T/SUBSPICLK
9	GPIO14/TOUCH14/ADCL_CH4/FSPIQ/FSPI0T/SUBSPICLK
10	GPIO15/TOUCH15/ADCL_CH5/FSPIQ/FSPI0T/SUBSPICLK
11	GPIO16/TOUCH16/ADCL_CH6/FSPIQ/FSPI0T/SUBSPICLK
12	GPIO17/TOUCH17/ADCL_CH7/FSPIQ/FSPI0T/SUBSPICLK
13	GPIO18/TOUCH18/ADCL_CH8/FSPIQ/FSPI0T/SUBSPICLK
14	GPIO19/TOUCH19/ADCL_CH9/FSPIQ/FSPI0T/SUBSPICLK
15	GPIO20/TOUCH20/ADCL_CH10/FSPIQ/FSPI0T/SUBSPICLK
16	GPIO21/TOUCH21/ADCL_CH11/FSPIQ/FSPI0T/SUBSPICLK
17	GPIO22/TOUCH22/ADCL_CH12/FSPIQ/FSPI0T/SUBSPICLK
18	GPIO23/TOUCH23/ADCL_CH13/FSPIQ/FSPI0T/SUBSPICLK
19	GPIO24/TOUCH24/ADCL_CH14/FSPIQ/FSPI0T/SUBSPICLK
20	GPIO25/TOUCH25/ADCL_CH15/FSPIQ/FSPI0T/SUBSPICLK
21	GPIO26/TOUCH26/ADCL_CH16/FSPIQ/FSPI0T/SUBSPICLK
22	GPIO27/TOUCH27/ADCL_CH17/FSPIQ/FSPI0T/SUBSPICLK
23	GPIO28/TOUCH28/ADCL_CH18/FSPIQ/FSPI0T/SUBSPICLK
24	GPIO29/TOUCH29/ADCL_CH19/FSPIQ/FSPI0T/SUBSPICLK
25	GPIO30/TOUCH30/ADCL_CH20/FSPIQ/FSPI0T/SUBSPICLK
26	GPIO31/TOUCH31/ADCL_CH21/FSPIQ/FSPI0T/SUBSPICLK
27	GPIO32/TOUCH32/ADCL_CH22/FSPIQ/FSPI0T/SUBSPICLK
28	GPIO33/TOUCH33/ADCL_CH23/FSPIQ/FSPI0T/SUBSPICLK
29	GPIO34/TOUCH34/ADCL_CH24/FSPIQ/FSPI0T/SUBSPICLK
30	GPIO35/TOUCH35/ADCL_CH25/FSPIQ/FSPI0T/SUBSPICLK
31	GPIO36/TOUCH36/ADCL_CH26/FSPIQ/FSPI0T/SUBSPICLK
32	GPIO37/TOUCH37/ADCL_CH27/FSPIQ/FSPI0T/SUBSPICLK
33	GPIO38/TOUCH38/ADCL_CH28/FSPIQ/FSPI0T/SUBSPICLK
34	GPIO39/TOUCH39/ADCL_CH29/FSPIQ/FSPI0T/SUBSPICLK
35	GPIO40/TOUCH40/ADCL_CH30/FSPIQ/FSPI0T/SUBSPICLK
36	GPIO41/TOUCH41/ADCL_CH31/FSPIQ/FSPI0T/SUBSPICLK
37	GPIO42/TOUCH42/ADCL_CH32/FSPIQ/FSPI0T/SUBSPICLK
38	GPIO43/TOUCH43/ADCL_CH33/FSPIQ/FSPI0T/SUBSPICLK
39	GPIO44/TOUCH44/ADCL_CH34/FSPIQ/FSPI0T/SUBSPICLK
40	GPIO45/TOUCH45/ADCL_CH35/FSPIQ/FSPI0T/SUBSPICLK
41	GPIO46/TOUCH46/ADCL_CH36/FSPIQ/FSPI0T/SUBSPICLK
42	GPIO47/TOUCH47/ADCL_CH37/FSPIQ/FSPI0T/SUBSPICLK
43	GPIO48/TOUCH48/ADCL_CH38/FSPIQ/FSPI0T/SUBSPICLK
44	GPIO49/TOUCH49/ADCL_CH39/FSPIQ/FSPI0T/SUBSPICLK
45	GPIO50/TOUCH50/ADCL_CH40/FSPIQ/FSPI0T/SUBSPICLK
46	GPIO51/TOUCH51/ADCL_CH41/FSPIQ/FSPI0T/SUBSPICLK
47	GPIO52/TOUCH52/ADCL_CH42/FSPIQ/FSPI0T/SUBSPICLK
48	GPIO53/TOUCH53/ADCL_CH43/FSPIQ/FSPI0T/SUBSPICLK
49	GPIO54/TOUCH54/ADCL_CH44/FSPIQ/FSPI0T/SUBSPICLK
50	GPIO55/TOUCH55/ADCL_CH45/FSPIQ/FSPI0T/SUBSPICLK
51	GPIO56/TOUCH56/ADCL_CH46/FSPIQ/FSPI0T/SUBSPICLK
52	GPIO57/TOUCH57/ADCL_CH47/FSPIQ/FSPI0T/SUBSPICLK
53	GPIO58/TOUCH58/ADCL_CH48/FSPIQ/FSPI0T/SUBSPICLK
54	GPIO59/TOUCH59/ADCL_CH49/FSPIQ/FSPI0T/SUBSPICLK
55	GPIO60/TOUCH60/ADCL_CH50/FSPIQ/FSPI0T/SUBSPICLK
56	GPIO61/TOUCH61/ADCL_CH51/FSPIQ/FSPI0T/SUBSPICLK
57	GPIO62/TOUCH62/ADCL_CH52/FSPIQ/FSPI0T/SUBSPICLK
58	GPIO63/TOUCH63/ADCL_CH53/FSPIQ/FSPI0T/SUBSPICLK
59	GPIO64/TOUCH64/ADCL_CH54/FSPIQ/FSPI0T/SUBSPICLK
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61	GPIO66/TOUCH66/ADCL_CH56/FSPIQ/FSPI0T/SUBSPICLK
62	GPIO67/TOUCH67/ADCL_CH57/FSPIQ/FSPI0T/SUBSPICLK
63	GPIO68/TOUCH68/ADCL_CH58/FSPIQ/FSPI0T/SUBSPICLK
64	GPIO69/TOUCH69/ADCL_CH59/FSPIQ/FSPI0T/SUBSPICLK
65	GPIO70/TOUCH70/ADCL_CH60/FSPIQ/FSPI0T/SUBSPICLK
66	GPIO71/TOUCH71/ADCL_CH61/FSPIQ/FSPI0T/SUBSPICLK
67	GPIO72/TOUCH72/ADCL_CH62/FSPIQ/FSPI0T/SUBSPICLK
68	GPIO73/TOUCH73/ADCL_CH63/FSPIQ/FSPI0T/SUBSPICLK
69	GPIO74/TOUCH74/ADCL_CH64/FSPIQ/FSPI0T/SUBSPICLK
70	GPIO75/TOUCH75/ADCL_CH65/FSPIQ/FSPI0T/SUBSPICLK
71	GPIO76/TOUCH76/ADCL_CH66/FSPIQ/FSPI0T/SUBSPICLK
72	GPIO77/TOUCH77/ADCL_CH67/FSPIQ/FSPI0T/SUBSPICLK
73	GPIO78/TOUCH78/ADCL_CH68/FSPIQ/FSPI0T/SUBSPICLK
74	GPIO79/TOUCH79/ADCL_CH69/FSPIQ/FSPI0T/SUBSPICLK
75	GPIO80/TOUCH80/ADCL_CH70/FSPIQ/FSPI0T/SUBSPICLK
76	GPIO81/TOUCH81/ADCL_CH71/FSPIQ/FSPI0T/SUBSPICLK
77	GPIO82/TOUCH82/ADCL_CH72/FSPIQ/FSPI0T/SUBSPICLK
78	GPIO83/TOUCH83/ADCL_CH73/FSPIQ/FSPI0T/SUBSPICLK
79	GPIO84/TOUCH84/ADCL_CH74/FSPIQ/FSPI0T/SUBSPICLK
80	GPIO85/TOUCH85/ADCL_CH75/FSPIQ/FSPI0T/SUBSPICLK
81	GPIO86/TOUCH86/ADCL_CH76/FSPIQ/FSPI0T/SUBSPICLK
82	GPIO87/TOUCH87/ADCL_CH77/FSPIQ/FSPI0T/SUBSPICLK
83	GPIO88/TOUCH88/ADCL_CH78/FSPIQ/FSPI0T/SUBSPICLK
84	GPIO89/TOUCH89/ADCL_CH79/FSPIQ/FSPI0T/SUBSPICLK
85	GPIO90/TOUCH90/ADCL_CH80/FSPIQ/FSPI0T/SUBSPICLK
86	GPIO91/TOUCH91/ADCL_CH81/FSPIQ/FSPI0T/SUBSPICLK
87	GPIO92/TOUCH92/ADCL_CH82/FSPIQ/FSPI0T/SUBSPICLK
88	GPIO9

Audio Amplification Circuit



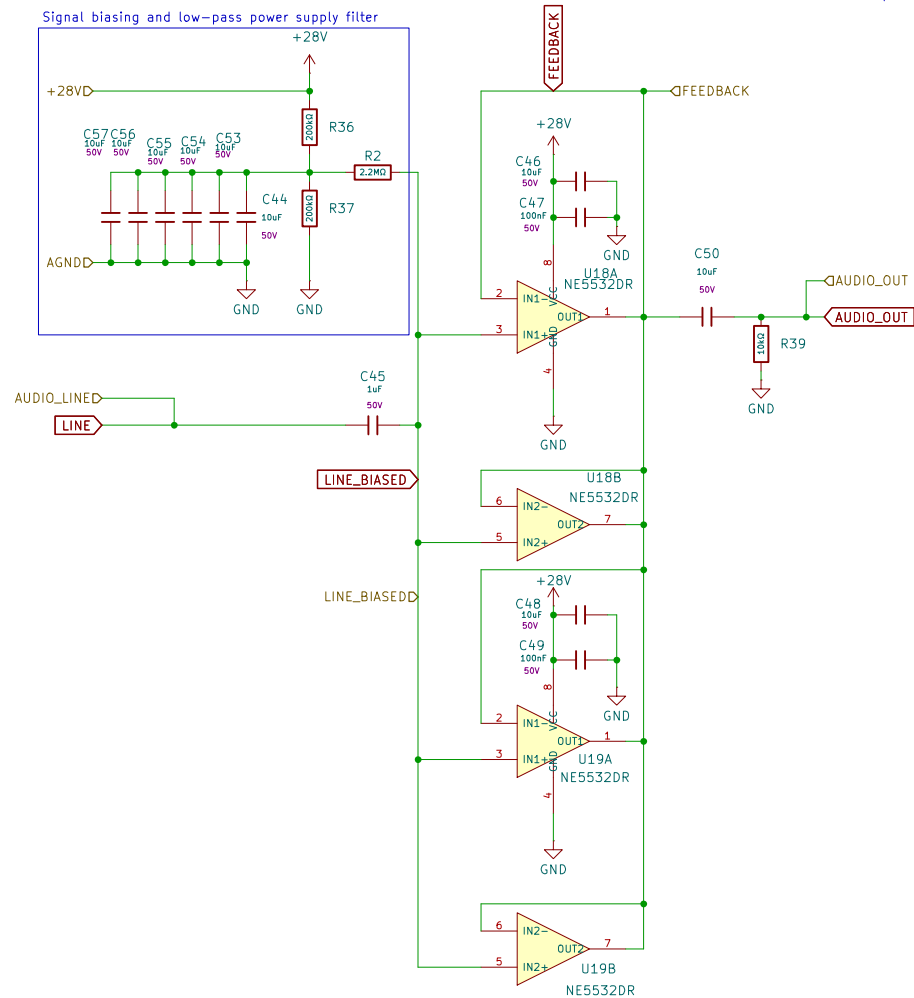
This circuit is used to boost the current output of the PCM5102a DAC so that it can drive 16-ohm headphones or in-ear monitors. Each channel has 4 NE5532's (2x dual packages) paralleled as unity-gain buffers to the PCM5102a's output.

The incoming signal passed through a capacitor to remove DC bias, then the signal is biased to half of the 28V high voltage supply, passed through the op-amps, then passed through another capacitor to again remove the DC bias.

The 28V power supply may be set lower, 28V is just the nominal value

OP Amp circuit design inspired by:
<https://www.youtube.com/watch?v=Ut-m8dl7INA&t=1s>

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This circuit provides a current-regulated bi-phasic AC output waveform.

First, a current-set voltage between 0 and 3.3V is set by the ESP32 using PWM at 100 kHz.

Then, this output voltage is reduced using a potentiometer as a voltage divider (RV6).

This potentiometer controls 2 circuits – the first reduces the current-set-PWM-voltage as mentioned;

and the second sends a 0–3.3V analog signal to the MCU to allow the MCU to determine the current position of the pot.

From here, the voltage-divider-reduced current-set-PWM signal is filtered using a low pass RC filter. (R_FILT and C_FILT)

The filtered voltage-divider-reduced current-set-PWM signal is used as a reference voltage to set the current using the Howland current pump as described in the Analog Devices technical note referenced below. The main difference between this circuit and the technical note is that the technical note's ADA4870 output buffer has been replaced with the lower-current (and cheaper) BUF634a.

The regulated output current "CURR_OUT" (with voltage up to 28V) is then fed into the SN754410NE H-Bridge Driver, controlled by pins on the ESP32 (driven by the RMT peripheral in software to ensure precise signal timing)

The op-amp circuit is fed by –2.5V on the negative PS terminal so that there is enough op-amp headroom to accommodate an output current setpoint of 0.

Circuit heavily based on: <https://www.analog.com/en/resources/analog-dialogue/articles/a-large-current-source-with-high-accuracy-and-fast-setting.html>

Current output is approximately equal to $V_{SET} / (k * R16)$.

Where $k = R40 / R32$.

Generally, R40 should not be increased, and there should be a preference for a larger k value and a smaller R40 value to reduce measurement error.

Current Regulation + BiPhasic Output Circuit

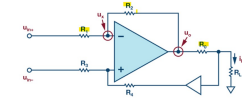


Figure 2. Enhanced Howland current source circuit.

While a large k will reduce the speed and precision of the circuit, inserting a buffer into the feedback route to form an enhanced Howland current source will eliminate this, as shown in Figure 2. All the current flows through R_3 is through R_3 . The output current is calculated with Equation 2.

$$I_L R_0 \left[1 + \frac{R_1}{R_2} + R_L \left(1 - \frac{R_1}{R_2} \times \frac{R_4}{R_5} \right) \right] =$$

$$V_{in} \left(\frac{R_4}{R_5} + 1 \right) - V_{in} \left(\frac{R_4}{R_5} + \frac{R_1}{R_2} \times \frac{R_4}{R_5} \right)$$

NOTE: Discrepancy: the equation is changed to Equation 3. The output current is independent of the load and only controlled by the input voltage, it's an ideal VCCS.

$$I_L = \frac{V_{in+1} - V_{in-}}{R R_0}$$

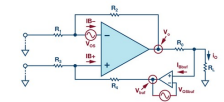


Figure 3. Offset voltage calculation.

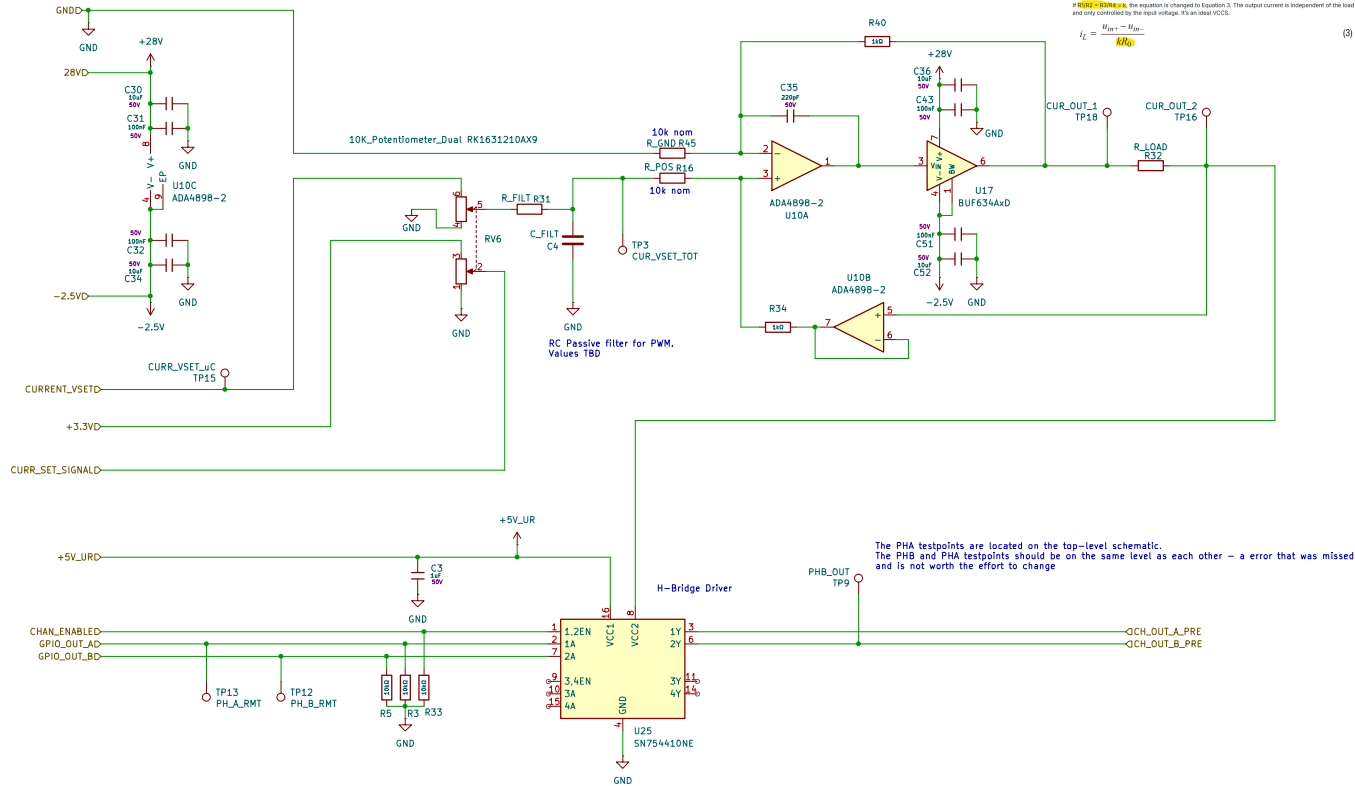
Ignore the mismatch from the gain resistors, and consider $R_1/R_2 = R_3/R_4 = k$, $R_1/R_2 = R_3/R_4$. The output offset current depends on the amplifier's offset and bias current, as shown in Equation 5.

$$I_D = \left(\frac{1}{k} + 1 \right) \times \frac{1}{R_0} \times I_{os} + \left(\frac{1}{k} + 1 \right) \times \frac{1}{R_0} \times \frac{R_1 R_2}{R_1 + R_2} \times$$

$$I_{os} + \frac{1}{R_0} \times V_{OS(off)} - I_{B(off)}$$

Taking the mismatch of R_1/R_2 and R_3/R_4 into consideration, R_0 will influence the output offset current. The worst relative error is shown in Equation 6. The error depends on R_1/R_2 and k . A smaller load resistor and higher k will increase the offset error.

$$\text{Max Relative Error of } I_D = \frac{R_1}{R_0} \times \frac{2A_k}{k(k+1)}$$



This circuit provides a current-regulated bi-phasic AC output waveform.

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Then, this output voltage is reduced using a potentiometer as a voltage divider (RV6).

This potentiometer controls 2 circuits – the first reduces the current-set-PWM-voltage as mentioned;

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Current output is approximately equal to $V_{SET} / (k * R16)$.

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Current Regulation + BiPhasic Output Circuit

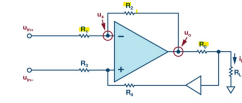


Figure 2. Enhanced Howland current source circuit.

While a large $R2$ will reduce the speed and precision of the circuit, inserting a buffer into the feedback route to form an enhanced Howland current source will eliminate this, as shown in Figure 2. All the current flows through $R4$ is through $R4$. The output current is calculated with Equation 2.

$$I_L R_0 \left[1 + \frac{R_1}{R_2} + R_L \left(1 - \frac{R_1}{R_2} \times \frac{R_4}{R_5} \right) \right] = V_{SET} \quad (2)$$

NOTE: Discrepancy: the equation is changed to Equation 3. The output current is independent of the load and only controlled by the input voltage, it's an ideal VCCS.

$$I_L = \frac{V_{SET} - V_{offset}}{R R_0} \quad (3)$$

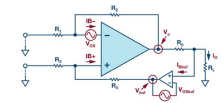


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Ignore the mismatch from the gain resistors, and consider $R_1/R_2 = R_3/R_4 = k$, $R_3/R_4 = R_1/R_2$. The output offset current depends on the amplifier's offset and bias current, as shown in Equation 5.

$$I_{D-} = \left(\frac{1}{k} + 1 \right) \times \frac{1}{R_0} \times I_{os} + \left(\frac{1}{k} + 1 \right) \times \frac{1}{R_0} \times \frac{R_1 R_2}{R_1 + R_2} \times I_{os} + \frac{1}{R_0} \times V_{OSoffset} - I_{Boffset} \quad (5)$$

Taking the mismatch of R_1/R_2 and R_3/R_4 into consideration, R_0 will influence the output offset current. The worst relative error is shown in Equation 6. The error depends on R_1/R_2 and k . A smaller load resistor and higher k will increase the offset error.

$$\text{Max Relative Error of } I_{D-} = \frac{R_1}{R_0} \times \frac{2A_2}{k(k+1)} \quad (6)$$

