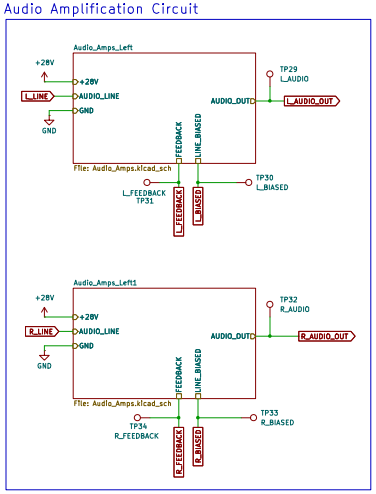
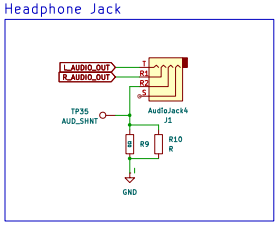
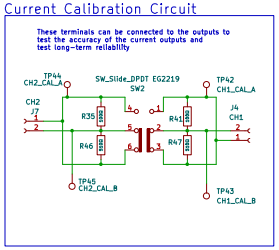
Audio Amplification Circuit



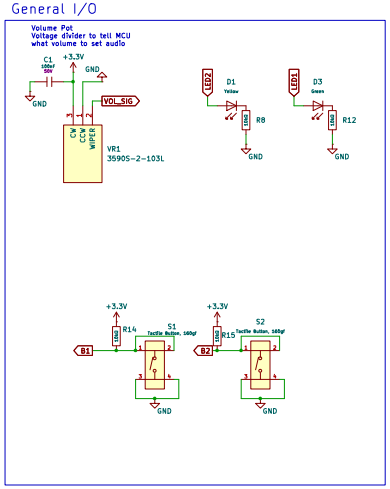
Headphone Jack



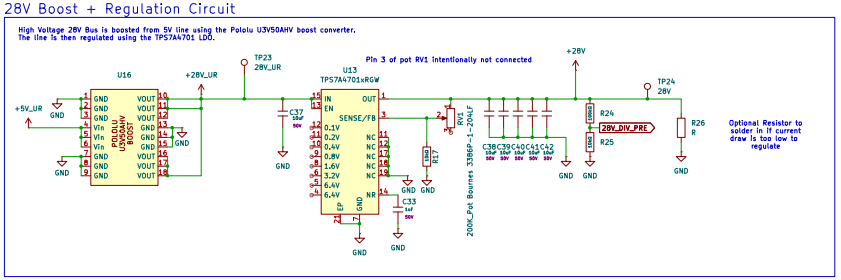
Current Calibration Circuit



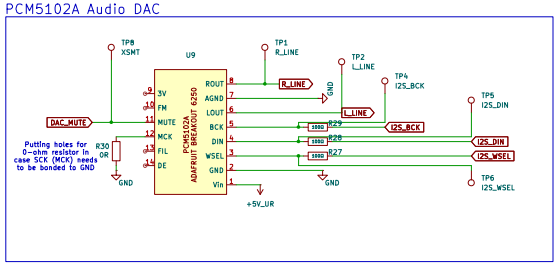
General I/O



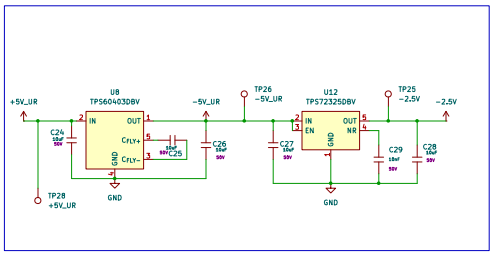
28V Boost + Regulation Circuit



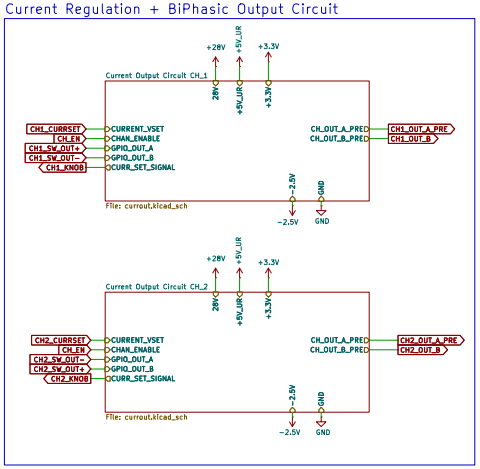
PCM5102A Audio DAC



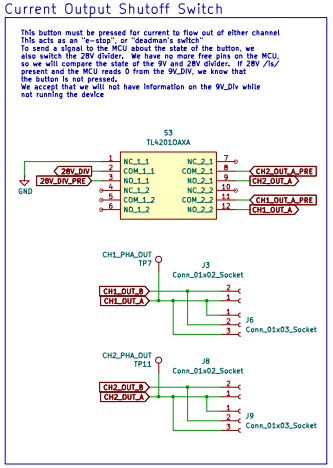
−2.5V Rail Circuit



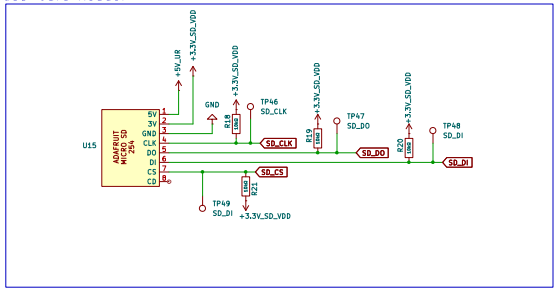
Current Regulation + BiPhasic Output Circuit



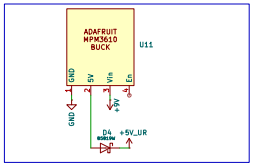
Current Output Shutoff Switch



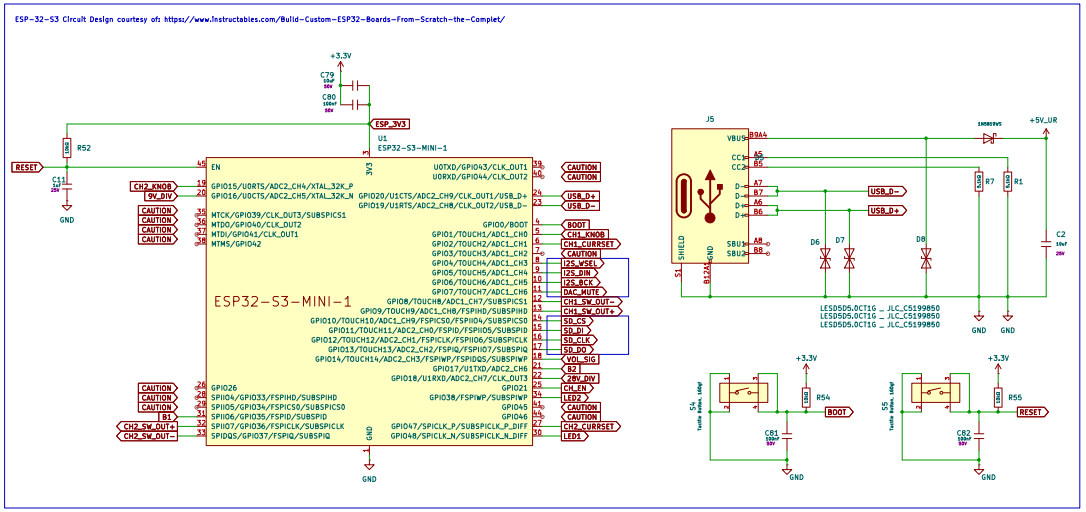
uSD Card Reader



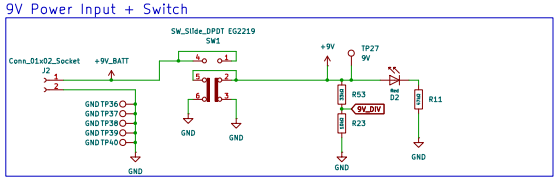
5V Rail Circuit



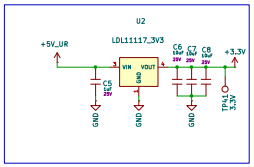
ESP32-S3-MINI



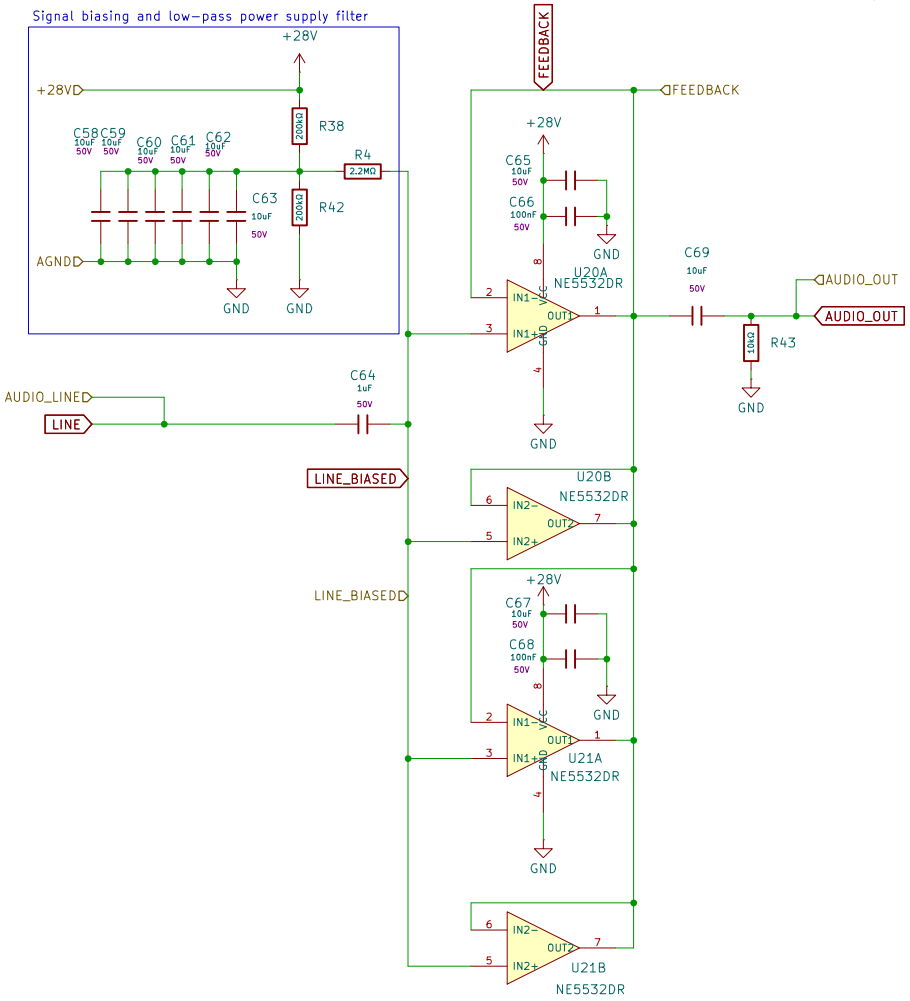
9V Power Input + Switch



3.3V Rail Circuit



Audio Amplification Circuit



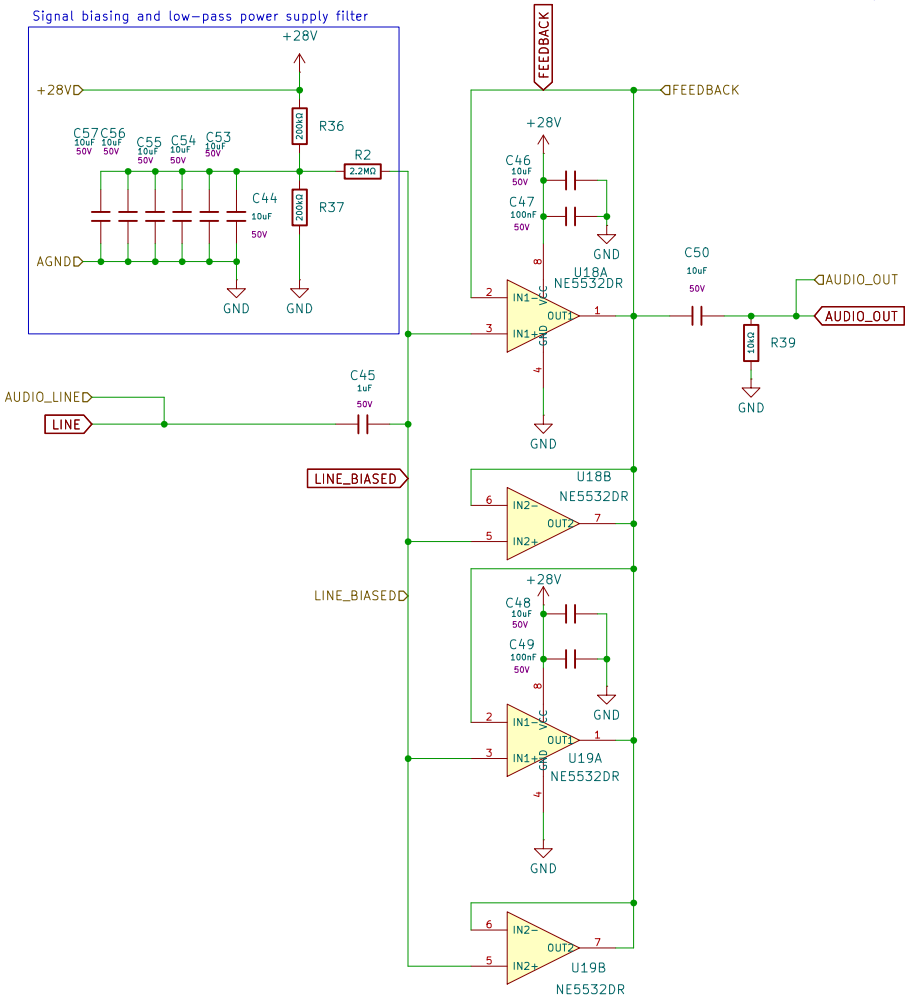
This circuit is used to boost the current output of the PCM5102a DAC so that it can drive 16-ohm headphones or in-ear monitors. Each channel has 4 NE5532's (2x dual packages) paralleled as unity-gain buffers to the PCM5102a's output.

The incoming signal passed through a capacitor to remove DC bias, then the signal is biased to half of the 28V high voltage supply, passed through the op-amps, then passed through another capacitor to again remove the DC bias.

The 28V power supply may be set lower, 28V is just the nominal value

OP Amp circuit design inspired by:
https://www.youtube.com/watch?v=Ut-m8dl7INA&t=1s

Audio Amplification Circuit



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Current Regulation + BiPhasic Output Circuit

This circuit provides a current-regulated bi-phasic AC output waveform.

First, a current-set voltage between 0 and 3.3V is set by the ESP32 using PWM at 100 kHz.

Then, this output voltage is reduced using a potentiometer as a voltage divider (RV6).

This potentiometer controls 2 circuits – the first reduces the current-set-PWM-voltage as mentioned;
and the second sends a 0-3.3V analog signal to the MCU to allow the MCU to determine the current position of the pot.

From here, the voltage-divider-reduced current-set-PWM signal is filtered using a low pass RC filter. (R_FILT and C_FILT)

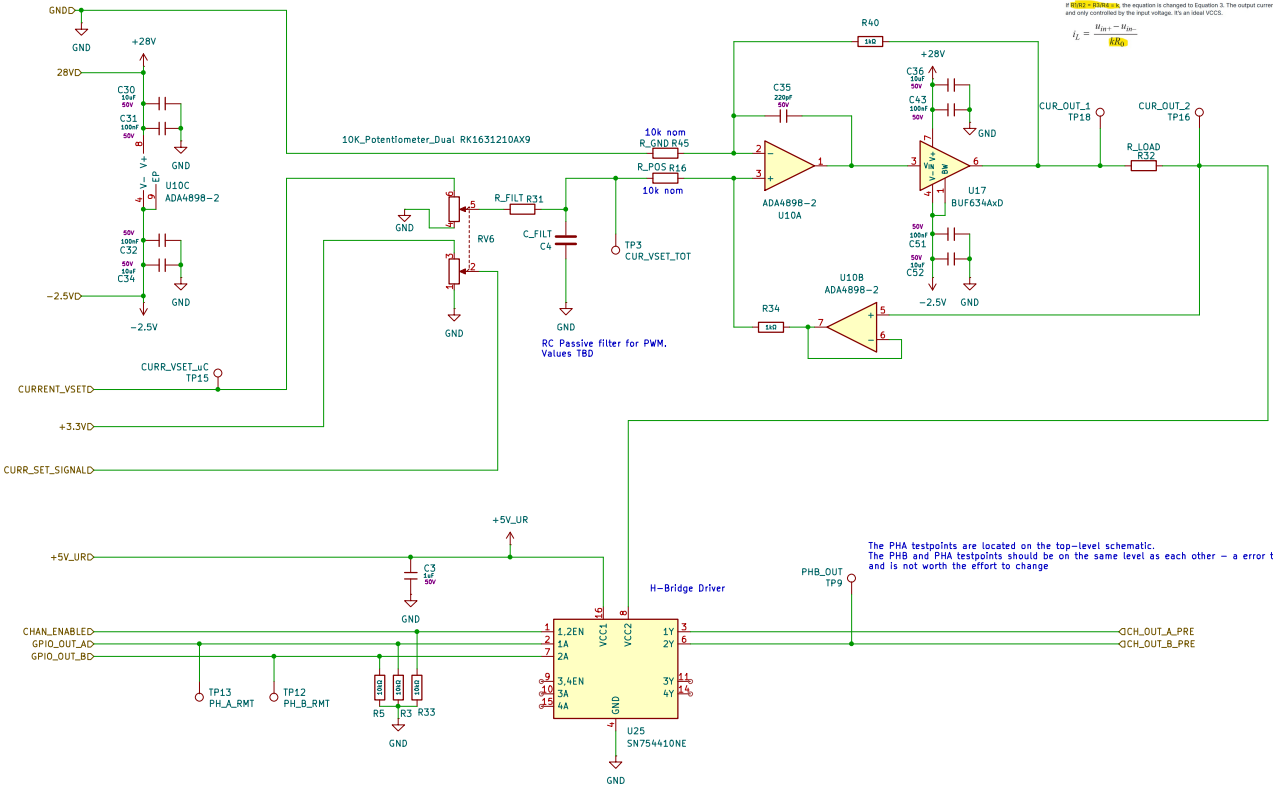
The filtered voltage-divider-reduced current-set-PWM signal is used as a reference voltage to set the current using the Howland current pump
as described in the Analog Devices technical note referenced below. The main difference between this circuit and the technical note
is that the technical note's ADA4870 output buffer has been replaced with the lower-current (and cheaper) Buf634a.

The regulated output current "CURR_OUT" (with voltage up to 28V) is then fed into the SN754410NE H-Bridge Driver, controlled by
pins on the ESP32 (driven by the RMT peripheral in software to ensure precise signal timing)

The op-amp circuit is fed by -2.5V on the negative PS terminal so that there is enough op-amp headroom to accommodate an output current setpoint of 0.

Circuit heavily based on: https://www.analog.com/en/resources/analog-dialogue/articles/a-large-current-source-with-high-accuracy-and-fast-settling.html

Current output is approximately equal to V_SET / (k * R16).
Where k = R40 / R32.
Generally, R40 should not be increased, and there should be a preference for a larger k value and a smaller R40 value
to reduce measurement error.



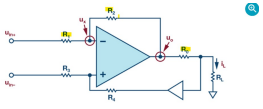


Figure 2. Enhanced Howland current source circuit.

While a large R2 will reduce the speed and precision of the circuit, inserting a buffer into the feedback route to form an enhanced Howland current source will eliminate this, as shown in Figure 2. All the current flows through R_0 is through into R_L. The output current is calculated with Equation 2.

$$i_L R_0 \left[1 + \frac{R_1}{R_2} + R_L\left(1 - \frac{R_1}{R_2} \times \frac{R_4}{R_3}\right)\right] = u_{in+}\left(\frac{R_4}{R_3} + 1\right) - u_{in-}\left(\frac{R_4}{R_3} + \frac{R_1}{R_2} \times \frac{R_4}{R_3}\right) \quad (2)$$

If $R1/R2 = R3/R4 = k$, the equation is changed to Equation 3. The output current is independent of the load and only controlled by the input voltage. It's an ideal VCCS.

$$i_L = \frac{u_{in+} - u_{in-}}{kR_0} \quad (3)$$

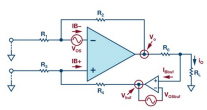


Figure 3. Offset voltage calculation.

Ignore the mismatch from the gain resistors, and consider $R_1/R_2 = R_3/R_4 = k$, $R_1//R_2 = R_3//R_4$. The output offset current depends on the amplifiers' offset and bias current, as shown in Equation 5.

$$I_O = \left(\frac{1}{k} + 1\right) \times \frac{1}{R_0} \times V_{os} + \left(\frac{1}{k} + 1\right) \times \frac{1}{R_0} \times \frac{R_1 R_2}{R_1 + R_2} \times I_{os} + \frac{1}{R_0} \times V_{OSbuf} - I_{Bbuf} \quad (5)$$

Taking the mismatch of R_1/R_2 and R_3/R_4 into consideration, R_L will influence the output offset current. The worst relative error is shown in Equation 6. The error depends on R_L/R_0 and k. A smaller load resistor and higher k will decrease the offset error.

$$Max\ Relative\ Error\ of\ I_O = \frac{R_L}{R_0} \times \frac{2\Delta_2}{k(k+1)} \quad (6)$$

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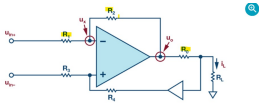

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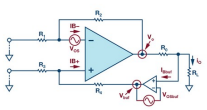

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