

Team09 Lab3 Report

B06204039 財金五 林有安 B07501003 電機四 盧彥安 B07502022 電機四 梁皓瑋

層級架構

module DE2_115

|__ pll

|__ Debounce * 3

|__ SevenHexDecoder * 3

|__ Top

|__ I2cInitializer

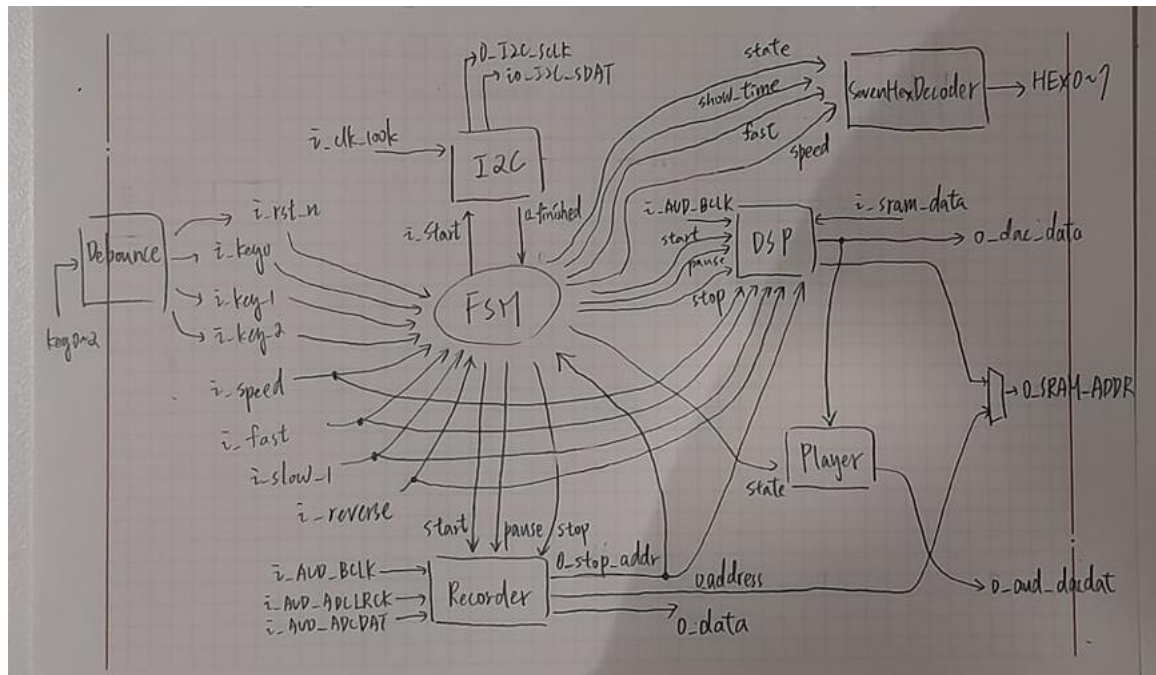
|__ AudDSP

|__ AudPlayer

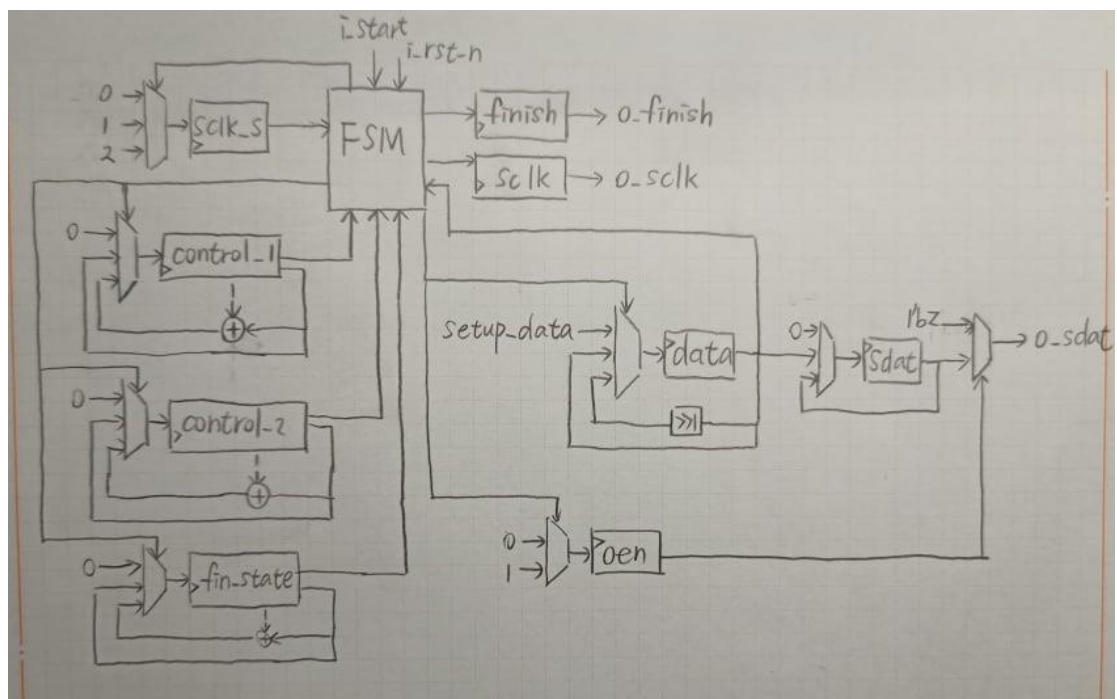
|__ AudRecorder

Block Diagram

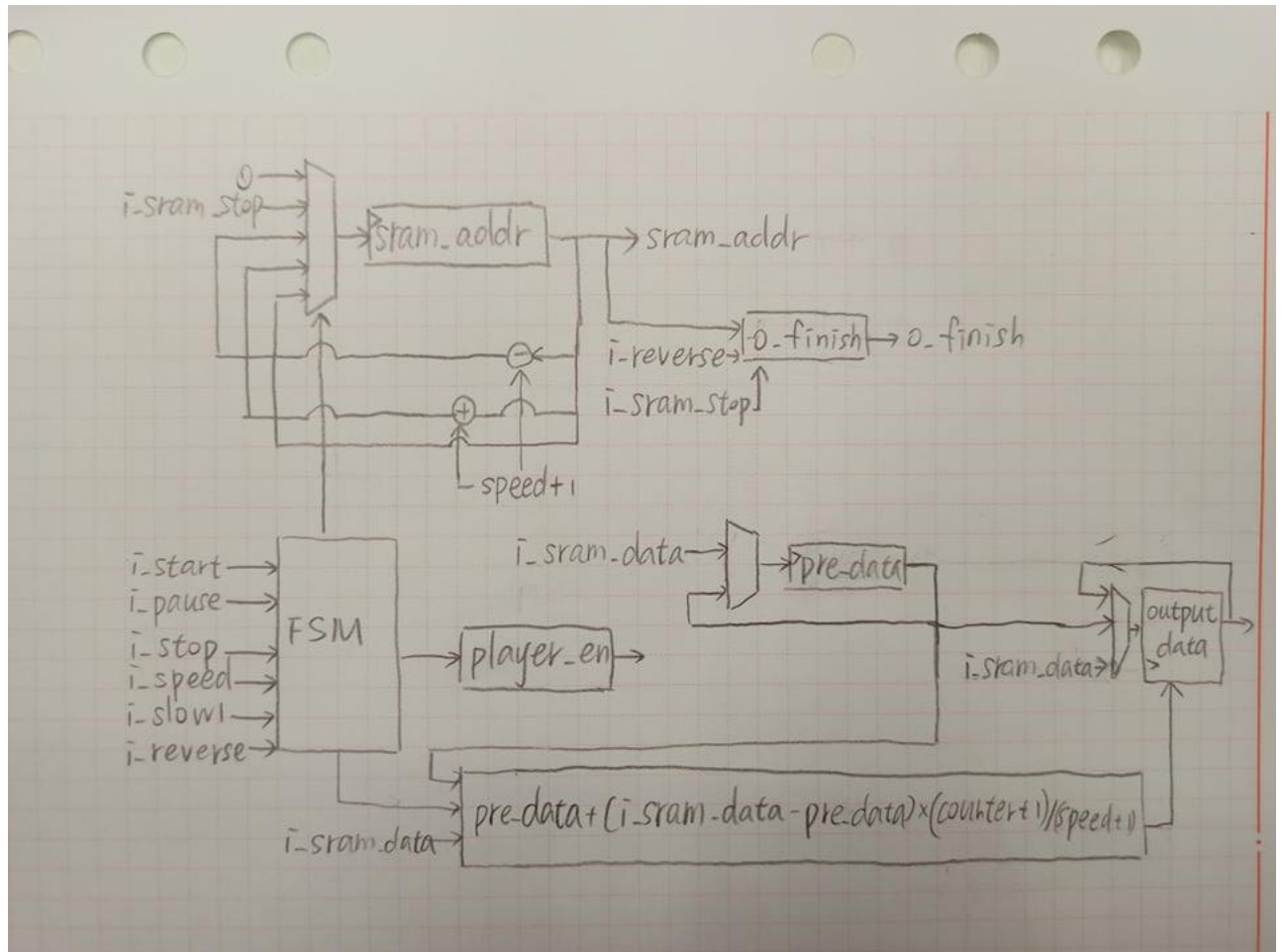
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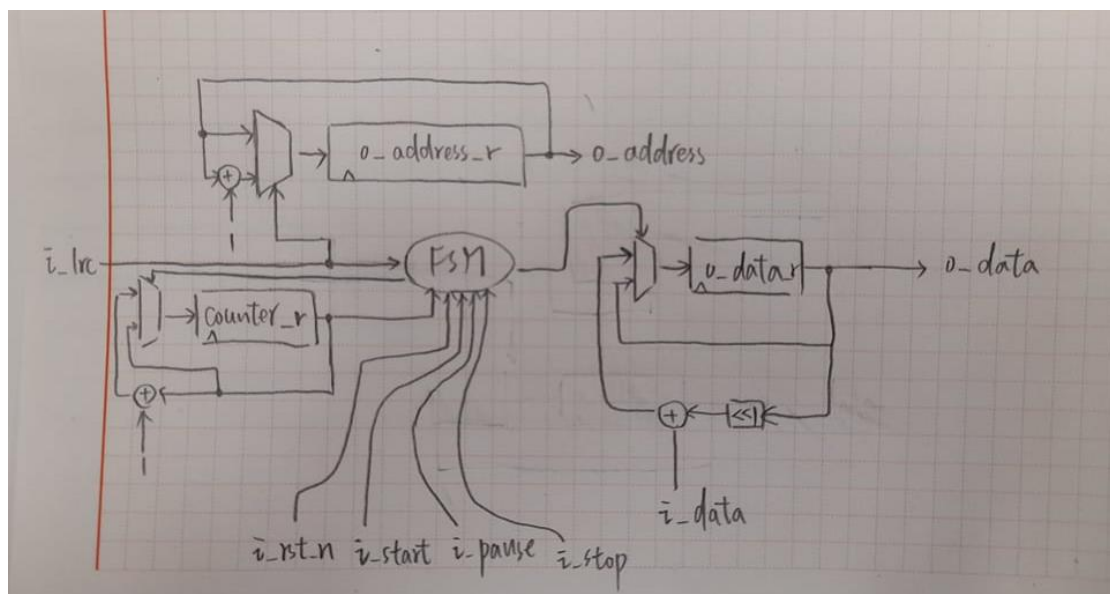
I2cInitializer



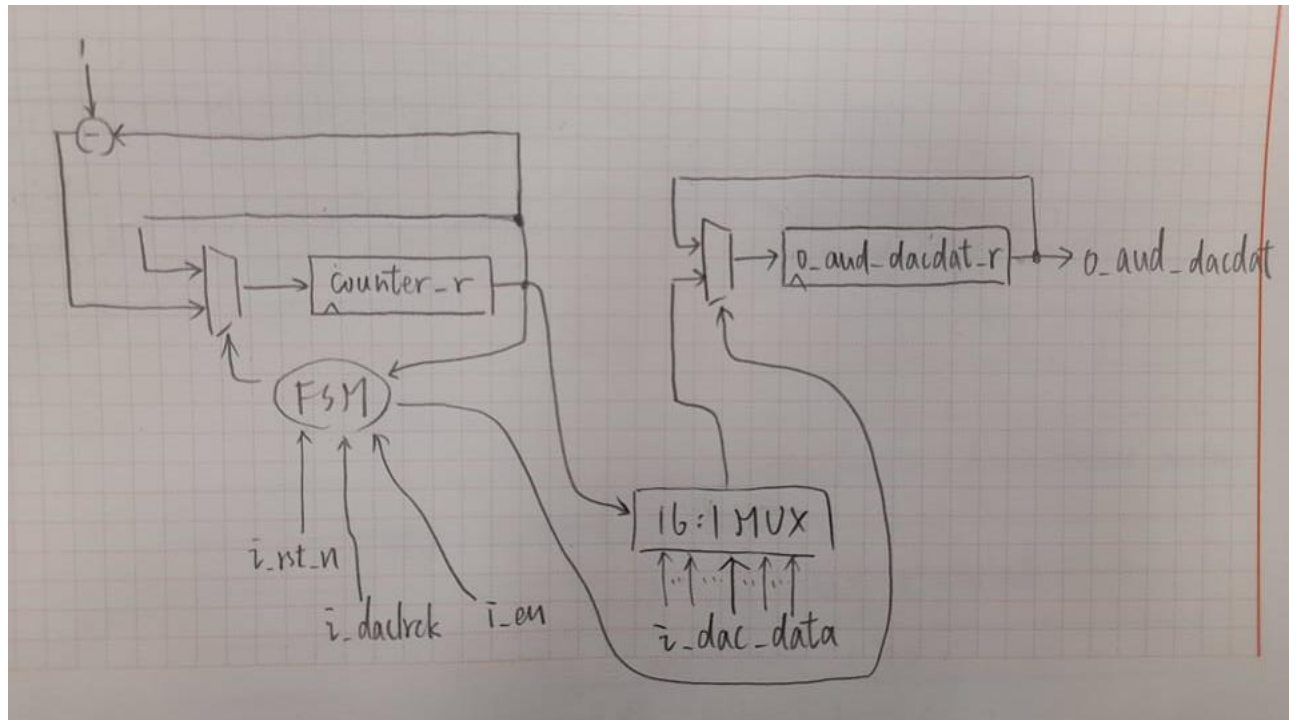
AudDSP



AudRecorder

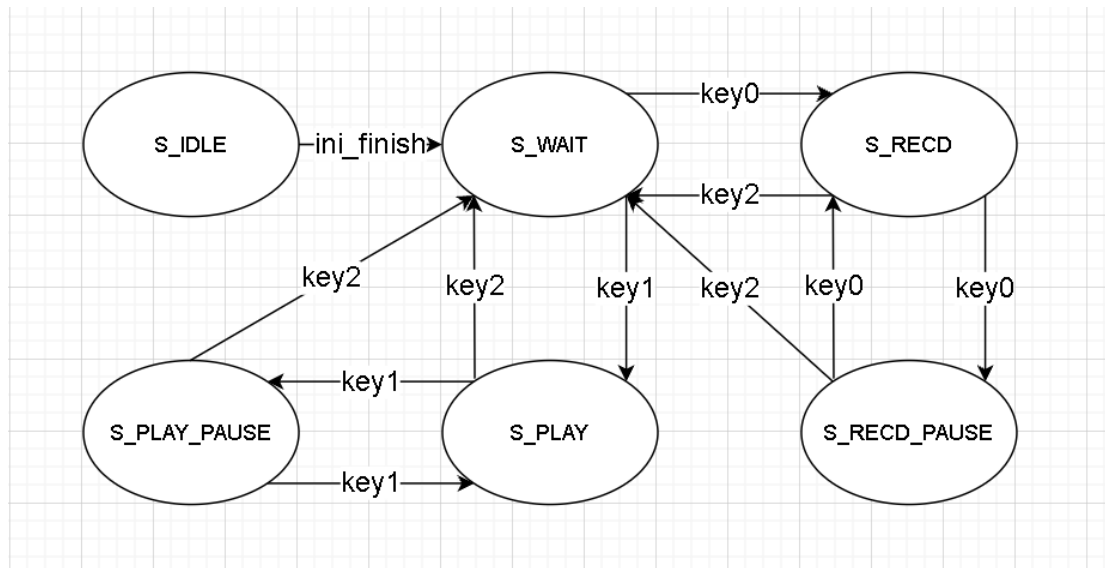


AudPlayer

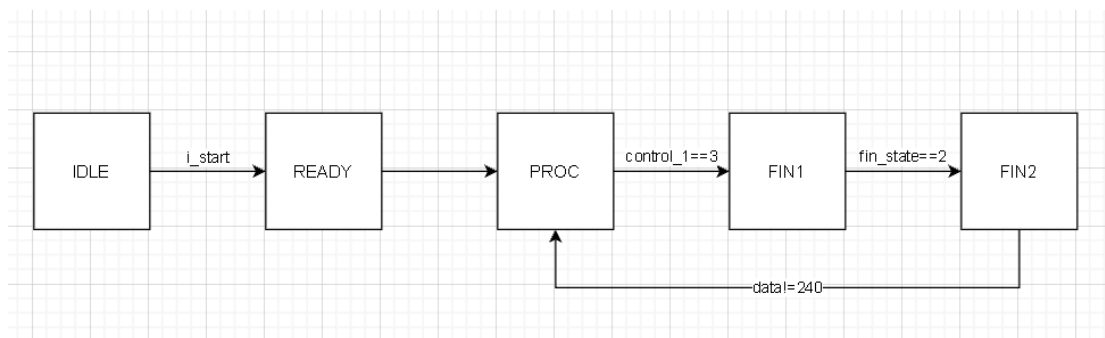


FSM or Scheduling

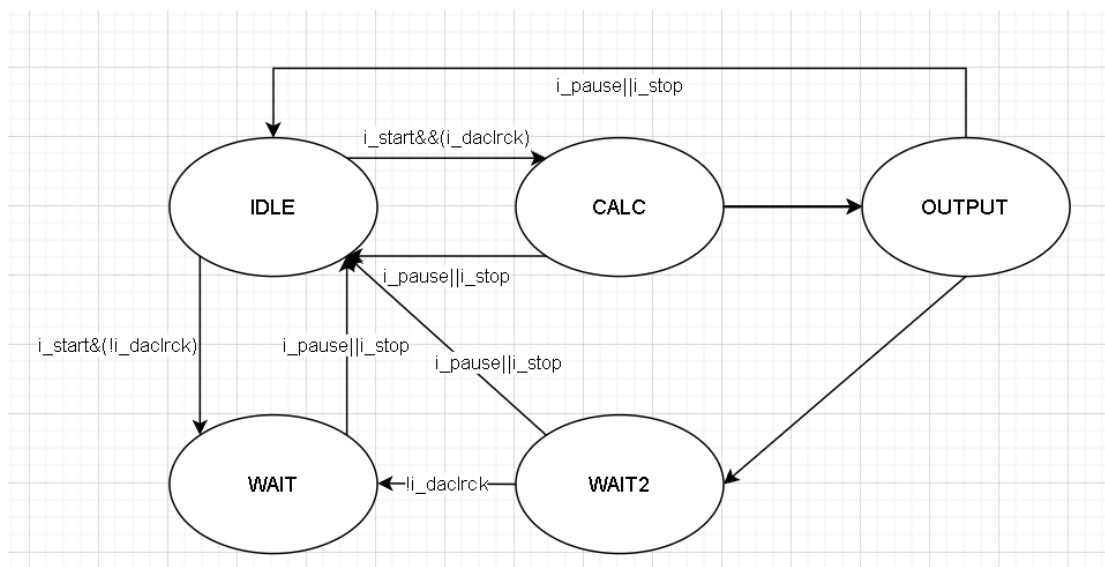
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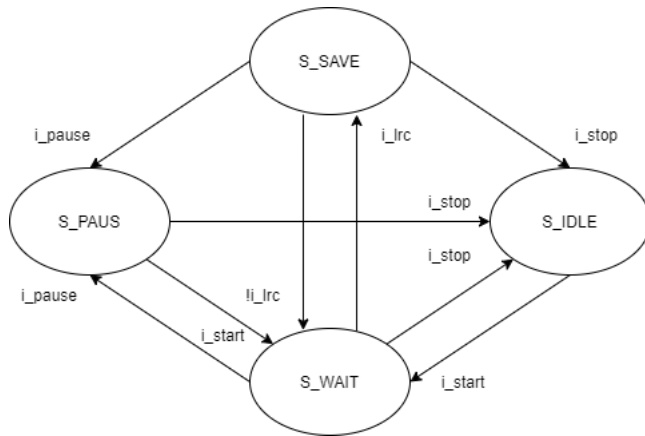
I2cInitializer



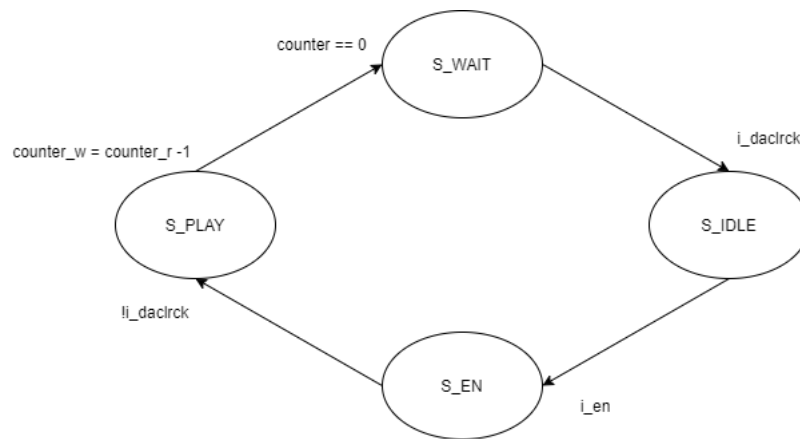
AudDSP



AudRecorder



AudPlayer



Fitter Summary 截圖

The screenshot shows the Quartus II Fitter Summary window for a project named DE2_115. The summary indicates a successful fit on a Cyclone IV E device (EP4CE10K10F23C7).

Resource	Used	Available	Usage (%)
Total logic elements	1,229	114,480	1%
Total combinational functions	1,219	114,480	1%
Dedicated logic registers	447	114,480	< 1%
Total registers	518	529	98%
Total pins	0	0	0%
Total virtual pins	0	0	0%
Total memory bits	4 / 3,881,312	3,881,312	< 1%
Embedded Multiplier 9-bit elements	4 / 532	532	< 1%
Total PLLs	1 / 4	4	25%

The bottom section of the window shows the compilation progress and messages. The compilation was successful, with 0 errors and 576 warnings. The TimeQuest Timing Analyzer was also successful.

Timing Analyzer 截圖

Flow Summary

Flow Settings

Flow Non-Default Global Settings

Flow Elapsed Time

Flow OS Summary

Flow Log

Analysis & Synthesis

Fitter

Flow Messages

Flow Suppressed Messages

Assembler

TimeQuest Timing Analyzer

Summary

Parallel Compilation

SDC File List

Clocks

Slow 1200mV 85C Model

Fmax Summary

Timing Closure Recommendations

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'pll0|altpll_1|sd1|pll7|clk[1]'

Setup: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'CLOCK_50'

Hold: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_1|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK2_50'

Summary [\[hide details\]](#)

This design contains failing setup paths with a worst-case slack of -2.736 ns. Run [Report Timing Closure Recommendations](#) for recommendations on how to close setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [\[hide details\]](#)

Slack	From	To	Recommendations
1 -2.736	Debounce:deb2 neg_r	Top:top0 state_r S_WAIT	Report recommendations for this path
2 -2.716	Debounce:deb0 neg_r	Top:top0 state_r S_REC0_PAUSE	Report recommendations for this path
3 -2.665	Debounce:deb1 neg_r	Top:top0 state_r S_PLAY	Report recommendations for this path
4 -2.615	Top:top0 state_r S_PLAY	Top:top0 time_counter_r[27]	Report recommendations for this path
5 -2.615	Top:top0 state_r S_PLAY	Top:top0 time_counter_r[15]	Report recommendations for this path

Table of Contents

Flow Summary

Flow Settings

Flow Non-Default Global Settings

Flow Elapsed Time

Flow OS Summary

Flow Log

Analysis & Synthesis

Fitter

Flow Messages

Flow Suppressed Messages

Assembler

TimeQuest Timing Analyzer

Summary

Parallel Compilation

SDC File List

Clocks

Slow 1200mV 85C Model

Fmax Summary

Timing Closure Recommendations

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'pll0|altpll_1|sd1|pll7|clk[1]'

Setup: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'CLOCK_50'

Hold: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_1|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK2_50'

Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-2.736	-14.852
2	CLOCK_50	-2.615	-103.384
3	pll0 altpll_1 sd1 pll7 clk[1]	80.591	0.000
4	pll0 altpll_1 sd1 pll7 clk[0]	9989.058	0.000

Slow 1200mV 85C Model Setup Summary			
	Clock	Slack	End Point TNS
1	p10 altpl_0 sd1 pl7 ck[0]	-10.123	-433.455
2	AUD_BCLK	-5.455	-424.052

Slow 1200mV 85C Model Setup: 'AUD_BCLK'									
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data	
1	-2.736	Debounce:deb2 neg_r	Top:top0 state_r_s_WAIT	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.339	5.984	
2	-2.716	Debounce:deb0 neg_r	Top:top0 state_r_s_REC'D_PAUSE	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.976	
3	-2.665	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.925	
4	-2.592	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY_PAUSE	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.852	
5	-2.585	Debounce:deb1 neg_r	Top:top0 state_r_s_WAIT	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.339	5.833	
6	-2.373	Debounce:deb0 neg_r	Top:top0 state_r_s_REC'D	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.206	5.488	
7	-2.251	Debounce:deb0 neg_r	Top:top0 state_r_s_PLAY	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.511	
8	-2.249	Debounce:deb0 neg_r	Top:top0 state_r_s_WAIT	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.339	5.497	
9	-2.215	Debounce:deb2 neg_r	Top:top0 state_r_s_REC'D_PAUSE	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.475	
10	-2.187	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY_PAUSE	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.447	
11	-2.150	Debounce:deb2 neg_r	Top:top0 state_r_s_REC'D	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.206	5.265	
12	-2.115	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY	p10 altpl_1 sd1 pl7 ck[1]	AUD_BCLK	0.001	3.351	5.375	
13	-1.770	Top:top0 12cdn realizer into finish	Top:top0 state_r_s_IDLE	p10 altpl_1 sd1 pl7 ck[0]	AUD_BCLK	1.000	3.350	6.028	
14	-1.668	Top:top0 12cdn realizer into finish	Top:top0 state_r_s_WAIT	p10 altpl_1 sd1 pl7 ck[0]	AUD_BCLK	1.000	3.350	5.926	
15	2.380	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.554	
16	2.589	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.345	
17	2.662	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.272	
18	2.703	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.231	
19	2.782	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[13]	AUD_BCLK	AUD_BCLK	83.000	-0.052	80.184	
20	2.806	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[9]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.128	
21	2.834	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[10]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.100	
22	2.913	Top:top0 AudDSP:dsd0 pre_data[0]	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.844	
23	2.928	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[7]	AUD_BCLK	AUD_BCLK	83.000	-0.084	80.006	
24	2.969	Top:top0 AudDSP:dsd0 pre_data[1]	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.788	
25	3.045	Top:top0 AudDSP:dsd0 pre_data[2]	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.712	
26	3.082	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[5]	AUD_BCLK	AUD_BCLK	83.000	-0.052	79.884	
27	3.122	Top:top0 AudDSP:dsd0 pre_data[0]	Top:top0 AudDSP:dsd0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.635	
28	3.176	Top:top0 AudDSP:dsd0 pre_data[4]	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.581	
29	3.178	Top:top0 AudDSP:dsd0 pre_data[1]	Top:top0 AudDSP:dsd0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.579	
30	3.191	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[6]	AUD_BCLK	AUD_BCLK	83.000	-0.052	79.775	
31	3.195	Top:top0 AudDSP:dsd0 pre_data[0]	Top:top0 AudDSP:dsd0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.562	
32	3.236	Top:top0 AudDSP:dsd0 pre_data[0]	Top:top0 AudDSP:dsd0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.521	
33	3.249	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[4]	AUD_BCLK	AUD_BCLK	83.000	-0.052	79.717	
34	3.250	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsd0 output_data[8]	AUD_BCLK	AUD_BCLK	83.000	-0.052	79.716	
35	3.251	Top:top0 AudDSP:dsd0 pre_data[1]	Top:top0 AudDSP:dsd0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.506	
36	3.254	Top:top0 AudDSP:dsd0 pre_data[2]	Top:top0 AudDSP:dsd0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.503	
37	3.261	Top:top0 AudDSP:dsd0 pre_data[3]	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.496	
38	3.292	Top:top0 AudDSP:dsd0 pre_data[1]	Top:top0 AudDSP:dsd0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.465	
39	3.311	Top:top0 AudDSP:dsd0 pre_data[6]	Top:top0 AudDSP:dsd0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.446	
40	3.315	Top:top0 AudDSP:dsd0 pre_data[0]	Top:top0 AudDSP:dsd0 output_data[13]	AUD_BCLK	AUD_BCLK	83.000	-0.229	79.474	
41	3.327	Top:top0 AudDSP:dsd0 pre_data[2]	Top:top0 AudDSP:dsd0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.261	79.430	

Flow Summary	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
Flow Settings	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[27]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Flow Non-Default Global Settings	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Flow Elapsed Time	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Flow OS Summary	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Flow Log	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Analysis & Synthesis	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Fitter	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Flow Messages	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Flow Suppressed Messages	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Assembler	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
TimeQuest Timing Analyzer	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Summary	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[26]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Parallel Compilation	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[29]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
SDC File List	-2.615	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[28]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Clocks	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[30]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.775
Slow 1200mV 85C Model	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Fmax Summary	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Timing Closure Recommendations	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Setup Summary	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Hold Summary	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Recovery Summary	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Removal Summary	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Minimum Pulse Width Summary	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Worst-Case Timing Paths	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Setup: 'AUD_BCLK'	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Setup: 'CLOCK_50'	-2.557	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.717
Setup: 'p0 altpl_1 sd1 p17 clk[1]'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Setup: 'p0 altpl_1 sd1 p17 clk[0]'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Hold: 'CLOCK_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Hold: 'p0 altpl_1 sd1 p17 clk[0]'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Hold: 'p0 altpl_1 sd1 p17 clk[1]'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Hold: 'AUD_BCLK'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK2_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK3_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK4_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK5_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK6_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Minimum Pulse Width: 'CLOCK7_50'	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599

Table of Contents	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
Flow Summary	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Flow Settings	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Flow Non-Default Global Settings	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Flow Elapsed Time	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Flow OS Summary	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[26]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Flow Log	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[29]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Analysis & Synthesis	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[28]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Fitter	-2.427	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[30]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.599
Flow Messages	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Flow Suppressed Messages	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Assembler	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
TimeQuest Timing Analyzer	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Summary	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Parallel Compilation	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
SDC File List	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Clocks	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Slow 1200mV 85C Model	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Fmax Summary	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Timing Closure Recommendations	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Setup Summary	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Hold Summary	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Recovery Summary	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Removal Summary	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
Minimum Pulse Width Summary	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Worst-Case Timing Paths	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Setup: 'AUD_BCLK'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Setup: 'CLOCK_50'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Setup: 'p0 altpl_1 sd1 p17 clk[1]'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Setup: 'p0 altpl_1 sd1 p17 clk[0]'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Hold: 'CLOCK_50'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Hold: 'p0 altpl_1 sd1 p17 clk[0]'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Hold: 'p0 altpl_1 sd1 p17 clk[1]'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Hold: 'AUD_BCLK'	-2.363	Top:top0 state_r_s_REC_PAUSE	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
Minimum Pulse Width: 'CLOCK_50'	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
Minimum Pulse Width: 'CLOCK2_50'	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
Minimum Pulse Width: 'CLOCK3_50'	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
Minimum Pulse Width: 'CLOCK4_50'	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
60	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
61	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
62	-2.376	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.816	2.548
63	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
64	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
65	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
66	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
67	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
68	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
69	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
70	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
71	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
72	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
73	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
74	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
75	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
76	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
77	-2.363	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.523
78	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
79	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
80	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
81	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
82	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
83	-2.326	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.417	2.897
84	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
85	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
86	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
87	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
88	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
89	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
90	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
91	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
92	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
93	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
94	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
95	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
96	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
97	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
98	-2.249	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.828	2.409
99	-2.247	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.267	2.968
100	-2.247	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.267	2.968

Table of Contents

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'pll0|altpll_1|sd1|pll7|clk[1]'

Setup: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'CLOCK_50'

Hold: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_1|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_1|sd1|pll7|clk[1]'

Minimum Pulse Width: 'pll0|altpll_1|sd1|pll7|clk[0]'

Datasheet Report

Metastability Summary

Slow 1200mV 0C Model

Fmax Summary

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'pll0|altpll_1|sd1|pll7|clk[1]'

Setup: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'CLOCK_50'

Hold: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_1|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Slow 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-2.602	-14.091
2	CLOCK_50	-2.402	-94.872
3	pll0 altpll_1 sd1 pll7 clk[1]	80.804	0.000
4	pll0 altpll_1 sd1 pll7 clk[0]	9989.947	0.000

Recovery Summary	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data
Close	-2.602	Debounce:deb2 neg_r	Top:top0 state_r_s_WAIT	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.041	5.553
Removal Summary	-3.562	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	5.524
Minimum Pulse Width Summary	-2.534	Debounce:deb0 neg_r	Top:top0 state_r_s_REC'D_PAUSE	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	5.496
Worst-Case Timing Paths	-2.488	Debounce:deb1 neg_r	Top:top0 state_r_s_WAIT	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.041	5.439
Setup: 'AUD_BCLK'	-2.464	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY_PAUSE	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	5.426
Setup: 'CLOCK_50'	-2.298	Debounce:deb0 neg_r	Top:top0 state_r_s_REC'D	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	2.916	5.124
Setup: 'p0 altp0_1 sd1 p07 ck[1]'	-2.115	Debounce:deb0 neg_r	Top:top0 state_r_s_PLAY	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	5.077
Setup: 'p0 altp0_1 sd1 p07 ck[0]'	-2.108	Debounce:deb0 neg_r	Top:top0 state_r_s_WAIT	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.041	5.059
Hold: 'CLOCK_50'	-2.067	Debounce:deb2 neg_r	Top:top0 state_r_s_REC'D_PAUSE	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	5.029
Hold: 'p0 altp0_1 sd1 p07 ck[0]'	-2.057	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY_PAUSE	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	5.019
Hold: 'p0 altp0_1 sd1 p07 ck[1]'	-2.010	Debounce:deb2 neg_r	Top:top0 state_r_s_REC'D	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	2.916	4.836
Hold: 'AUD_BCLK'	-1.992	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY	p0 altp0_1 sd1 p07 ck[1]	AUD_BCLK	0.001	3.052	4.954
Minimum Pulse Width: 'CLOCK_50'	-1.631	Top:top0 I2cInitiaizer int0 finish	Top:top0 state_r_s_IDLE	p0 altp0_1 sd1 p07 ck[0]	AUD_BCLK	1.000	3.052	5.592
Minimum Pulse Width: 'CLOCK2_50'	-1.563	Top:top0 I2cInitiaizer int0 finish	Top:top0 state_r_s_WAIT	p0 altp0_1 sd1 p07 ck[0]	AUD_BCLK	1.000	3.052	5.524
Minimum Pulse Width: 'CLOCK3_50'	10.287	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.657
Minimum Pulse Width: 'AUD_BCLK'	10.471	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.473
Minimum Pulse Width: 'AUD_BCLK'	10.533	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.411
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[1]'	10.570	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.374
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[1]'	10.650	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[13]	AUD_BCLK	AUD_BCLK	83.000	-0.050	72.319
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[0]'	10.656	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[9]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.288
Datasheet Report	10.685	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[10]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.259
Metastability Summary	10.763	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[7]	AUD_BCLK	AUD_BCLK	83.000	-0.075	72.181
Slow 1200mV OC Model	10.802	Top:top0 AudDSP:dsp0 pre_data[0]	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.982
Fmax Summary	10.854	Top:top0 AudDSP:dsp0 pre_data[1]	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.930
Setup Summary	10.897	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[5]	AUD_BCLK	AUD_BCLK	83.000	-0.050	72.072
Hold Summary	10.917	Top:top0 AudDSP:dsp0 pre_data[2]	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.867
Recovery Summary	10.986	Top:top0 AudDSP:dsp0 pre_data[0]	Top:top0 AudDSP:dsp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.798
Removal Summary	10.996	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[5]	AUD_BCLK	AUD_BCLK	83.000	-0.050	71.973
Minimum Pulse Width Summary	11.033	Top:top0 AudDSP:dsp0 pre_data[4]	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.751
Minimum Pulse Width Summary	11.038	Top:top0 AudDSP:dsp0 pre_data[1]	Top:top0 AudDSP:dsp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.746
Minimum Pulse Width Summary	11.047	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[4]	AUD_BCLK	AUD_BCLK	83.000	-0.050	71.922
Minimum Pulse Width Summary	11.048	Top:top0 AudDSP:dsp0 pre_data[0]	Top:top0 AudDSP:dsp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.736
Minimum Pulse Width Summary	11.084	Top:top0 state_r_s_REC'D	Top:top0 AudDSP:dsp0 output_data[8]	AUD_BCLK	AUD_BCLK	83.000	-0.050	71.885
Minimum Pulse Width Summary	11.085	Top:top0 AudDSP:dsp0 pre_data[0]	Top:top0 AudDSP:dsp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.699
Minimum Pulse Width Summary	11.100	Top:top0 AudDSP:dsp0 pre_data[1]	Top:top0 AudDSP:dsp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.684
Minimum Pulse Width Summary	11.101	Top:top0 AudDSP:dsp0 pre_data[2]	Top:top0 AudDSP:dsp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.683
Minimum Pulse Width Summary	11.106	Top:top0 AudDSP:dsp0 pre_data[3]	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.678
Minimum Pulse Width Summary	11.137	Top:top0 AudDSP:dsp0 pre_data[1]	Top:top0 AudDSP:dsp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.647
Minimum Pulse Width Summary	11.152	Top:top0 AudDSP:dsp0 pre_data[6]	Top:top0 AudDSP:dsp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.632
Minimum Pulse Width Summary	11.163	Top:top0 AudDSP:dsp0 pre_data[2]	Top:top0 AudDSP:dsp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.235	71.621
Minimum Pulse Width Summary	11.165	Top:top0 AudDSP:dsp0 pre_data[0]	Top:top0 AudDSP:dsp0 output_data[13]	AUD_BCLK	AUD_BCLK	83.000	-0.210	71.644

Recovery Summary	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
Removal Summary	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[27]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width Summary	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Worst-Case Timing Paths	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Setup: 'AUD_BCLK'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Setup: 'CLOCK_50'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Setup: 'p0 altp0_1 sd1 p07 ck[1]'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Setup: 'p0 altp0_1 sd1 p07 ck[0]'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Hold: 'CLOCK_50'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Hold: 'AUD_BCLK'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'CLOCK_50'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'CLOCK2_50'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'CLOCK3_50'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[25]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'AUD_BCLK'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[26]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[1]'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[29]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[0]'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[28]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'AUD_BCLK'	-2.402	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[30]	AUD_BCLK	CLOCK_50	1.000	-0.861	2.530
Minimum Pulse Width: 'CLOCK_50'	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width: 'AUD_BCLK'	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[1]'	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width: 'p0 altp0_1 sd1 p07 ck[0]'	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Datasheet Report	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Metastability Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Slow 1200mV OC Model	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Fmax Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Setup Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Hold Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Recovery Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Removal Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width Summary	-2.349	Top:top0 state_r_s_PLAY	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.859	2.479
Minimum Pulse Width Summary	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[27]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Setup: 'AUD_BCLK'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[15]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Setup: 'CLOCK_50'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[16]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Setup: 'p0 altp0_1 sd1 p07 ck[1]'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[17]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Setup: 'p0 altp0_1 sd1 p07 ck[0]'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[18]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Hold: 'CLOCK_50'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[19]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Hold: 'AUD_BCLK'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[20]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Minimum Pulse Width: 'CLOCK_50'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[21]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Minimum Pulse Width: 'CLOCK2_50'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[22]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Minimum Pulse Width: 'CLOCK3_50'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[23]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373
Minimum Pulse Width: 'AUD_BCLK'	-2.234	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[24]	AUD_BCLK	CLOCK_50	1.000	-0.850	2.373

Table of Contents

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_1|sd1|pll7|clk[1]'

Minimum Pulse Width: 'pll0|altpll_1|sd1|pll7|clk[0]'

Datasheet Report

Metastability Summary

Fast 1200mV 0C Model

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'pll0|altpll_1|sd1|pll7|clk[1]'

Setup: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'CLOCK_50'

Hold: 'pll0|altpll_1|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_1|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_1|sd1|pll7|clk[1]'

Minimum Pulse Width: 'pll0|altpll_1|sd1|pll7|clk[0]'

Datasheet Report

Metastability Summary

Multicorner Timing Analysis Summary

Multicorner Datasheet Report Summary

Advanced I/O Timing

Clock Transfers

Report TCCS

Report RSKM

Unconstrained Paths

Fast 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-1.651	-8.216
2	CLOCK_50	-0.643	-23.688
3	pll0 altpll_1 sd1 pll7 clk[1]	82.035	0.000
4	pll0 altpll_1 sd1 pll7 clk[0]	9994.433	0.000

Table of Contents		Fast 1200mV 0C Model Setup: 'AUD_BCLK'									
		Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data		
Minimum Pulse Width: 'pll0 altpl_1 sd1 pll7 clk[1]'		-1.651	Debounce:deb2 neg_r	Top:top0 state_r_s_WAIT	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.710	3.259		
	Minimum Pulse Width: 'pll0 altpl_1 sd1 pll7 clk[0]'	-1.556	Debounce:deb1 neg_r	Top:top0 state_r_s_WAIT	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.710	3.164		
Datasheet Report		-1.543	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY_PAUSE	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	3.153		
Metastability Summary		-1.542	Debounce:deb0 neg_r	Top:top0 state_r_s_REC0_PAUSE	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	3.152		
Fast 1200mV 0C Model		-1.433	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	3.043		
	Setup Summary	-1.386	Debounce:deb0 neg_r	Top:top0 state_r_s_REC0	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.622	2.906		
Hold Summary		-1.231	Debounce:deb0 neg_r	Top:top0 state_r_s_WAIT	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.710	2.839		
Recovery Summary		-1.189	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY_PAUSE	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	2.799		
Removal Summary		-1.185	Debounce:deb2 neg_r	Top:top0 state_r_s_REC0_PAUSE	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	2.795		
Minimum Pulse Width Summary		-1.128	Debounce:deb0 neg_r	Top:top0 state_r_s_PLAY	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	2.738		
Worst-Case Timing Paths		-1.115	Debounce:deb2 neg_r	Top:top0 state_r_s_REC0	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.622	2.635		
	Setup: 'AUD_BCLK'	-1.006	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY	pll0 altpl_1 sd1 pll7 clk[1]	AUD_BCLK	0.001	1.712	2.616		
Setup: 'CLOCK_50'		-0.661	Top:top0 I2cInitializer init0 finish	Top:top0 state_r_s_IDLE	pll0 altpl_1 sd1 pll7 clk[0]	AUD_BCLK	1.000	1.719	3.277		
Setup: 'pll0 altpl_1 sd1 pll7 clk[1]'		-0.624	Top:top0 I2cInitializer init0 finish	Top:top0 state_r_s_WAIT	pll0 altpl_1 sd1 pll7 clk[0]	AUD_BCLK	1.000	1.719	3.240		
Hold: 'CLOCK_50'		44.127	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.849		
Hold: 'pll0 altpl_1 sd1 pll7 clk[1]'		44.196	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.780		
Hold: 'pll0 altpl_1 sd1 pll7 clk[0]'		44.257	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.719		
Hold: 'AUD_BCLK'		44.272	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.704		
Minimum Pulse Width: 'CLOCK2_50'		44.322	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[13]	AUD_BCLK	AUD_BCLK	83.000	-0.021	38.664		
Minimum Pulse Width: 'CLOCK3_50'		44.324	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[10]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.652		
Minimum Pulse Width: 'AUD_BCLK'		44.338	Top:top0 AudDSP:dsdp0 pre_data[0]	Top:top0 AudDSP:dsdp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.554		
Minimum Pulse Width: 'pll0 altpl_1 sd1 pll7 clk[1]'		44.350	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[9]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.626		
Minimum Pulse Width: 'pll0 altpl_1 sd1 pll7 clk[0]'		44.368	Top:top0 AudDSP:dsdp0 pre_data[1]	Top:top0 AudDSP:dsdp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.524		
Minimum Pulse Width: 'CLOCK_50'		44.405	Top:top0 AudDSP:dsdp0 pre_data[2]	Top:top0 AudDSP:dsdp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.487		
Minimum Pulse Width: 'AUD_BCLK'		44.407	Top:top0 AudDSP:dsdp0 pre_data[1]	Top:top0 AudDSP:dsdp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.485		
Minimum Pulse Width: 'pll0 altpl_1 sd1 pll7 clk[1]'		44.408	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[7]	AUD_BCLK	AUD_BCLK	83.000	-0.031	38.568		
Minimum Pulse Width: 'pll0 altpl_1 sd1 pll7 clk[0]'		44.437	Top:top0 AudDSP:dsdp0 pre_data[1]	Top:top0 AudDSP:dsdp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.455		
Datasheet Report		44.468	Top:top0 AudDSP:dsdp0 pre_data[0]	Top:top0 AudDSP:dsdp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.424		
Metastability Summary		44.473	Top:top0 AudDSP:dsdp0 pre_data[4]	Top:top0 AudDSP:dsdp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.419		
Multicorner Timing Analysis Summary		44.474	Top:top0 AudDSP:dsdp0 pre_data[2]	Top:top0 AudDSP:dsdp0 output_data[14]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.418		
Multicorner Datasheet Report Summary		44.483	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[5]	AUD_BCLK	AUD_BCLK	83.000	-0.021	38.503		
Advanced I/O Timing		44.483	Top:top0 AudDSP:dsdp0 pre_data[0]	Top:top0 AudDSP:dsdp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.409		
Clock Transfers		44.498	Top:top0 AudDSP:dsdp0 pre_data[1]	Top:top0 AudDSP:dsdp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.394		
Report TCCS		44.500	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[6]	AUD_BCLK	AUD_BCLK	83.000	-0.021	38.486		
Report RSKM		44.513	Top:top0 AudDSP:dsdp0 pre_data[1]	Top:top0 AudDSP:dsdp0 output_data[11]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.379		
Unconstrained Paths		44.522	Top:top0 AudDSP:dsdp0 pre_data[3]	Top:top0 AudDSP:dsdp0 output_data[15]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.370		
Messages		44.533	Top:top0 AudDSP:dsdp0 pre_data[0]	Top:top0 AudDSP:dsdp0 output_data[13]	AUD_BCLK	AUD_BCLK	83.000	-0.105	38.369		
		44.534	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[4]	AUD_BCLK	AUD_BCLK	83.000	-0.021	38.452		
		44.535	Top:top0 state_r_s_REC0	Top:top0 AudDSP:dsdp0 output_data[8]	AUD_BCLK	AUD_BCLK	83.000	-0.021	38.451		
		44.535	Top:top0 AudDSP:dsdp0 pre_data[0]	Top:top0 AudDSP:dsdp0 output_data[10]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.357		
		44.535	Top:top0 AudDSP:dsdp0 pre_data[2]	Top:top0 AudDSP:dsdp0 output_data[12]	AUD_BCLK	AUD_BCLK	83.000	-0.115	38.357		

Minimum Pulse Width: 'p0[alpb1_1sd1p1k7]ck[1]'

Minimum Pulse Width: 'p0[alpb1_1sd1p1k7]ck[0]'

Datasetheet Report

Metasheet Summary

Fast 1200mV OC Model

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'p0[alpb1_1sd1p1k7]ck[1]'

Setup: 'p0[alpb1_1sd1p1k7]ck[0]'

Hold: 'CLOCK_50'

Hold: 'p0[alpb1_1sd1p1k7]ck[0]'

Hold: 'p0[alpb1_1sd1p1k7]ck[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'p0[alpb1_1sd1p1k7]ck[1]'

Minimum Pulse Width: 'p0[alpb1_1sd1p1k7]ck[0]'

Datasetheet Report

Metasheet Summary

Multicore Timing Analysis Summary

Multicore Datasetheet Report Summary

Advanced I/O Timing

Clock Transfers

Report TCCS

Report RSQM

Unconstrained Paths

Messages

Close

Minimum Pulse Width: 'p0|altpl_1|sd1|p87|ck[1]'

Minimum Pulse Width: 'p0|altpl_1|sd1|p87|ck[0]'

Datasheet Report

Metastability Summary

Fast 1200MHz OC Mode

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'CLOCK_50'

Setup: 'p0|altpl_1|sd1|p87|ck[1]'

Setup: 'p0|altpl_1|sd1|p87|ck[0]'

Hold: 'CLOCK_50'

Hold: 'p0|altpl_1|sd1|p87|ck[0]'

Hold: 'p0|altpl_1|sd1|p87|ck[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'p0|altpl_1|sd1|p87|ck[1]'

Minimum Pulse Width: 'p0|altpl_1|sd1|p87|ck[0]'

Datasheet Report

Metastability Summary

Multicorner Timing Analysis Summary

Multicorner Datasheet Report Summary

Advanced I/O Timing

Clock Transfers

Report TCCS

Report RSKM

Unconstrained Paths

Messages

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay	
60	-0.543	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.303	1.217
61	-0.543	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.303	1.217
62	-0.543	Top:top0 state_r_s_WAIT	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.303	1.217
63	-0.526	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.115	1.388
64	-0.526	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.115	1.388
65	-0.526	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.115	1.388
66	-0.526	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.115	1.388
67	-0.526	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.115	1.388
68	-0.526	Top:top0 state_r_s_PLAY	Top:top0 showtime_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.115	1.388
69	-0.523	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.022	1.478
70	-0.523	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.022	1.478
71	-0.523	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.022	1.478
72	-0.523	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.022	1.478
73	-0.523	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.022	1.478
74	-0.523	Top:top0 state_r_s_REC'D	Top:top0 showtime_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.022	1.478
75	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
76	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
77	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
78	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
79	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
80	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
81	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
82	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
83	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
84	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
85	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
86	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[11]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
87	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[12]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
88	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[13]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
89	-0.507	Top:top0 state_r_s_REC'D_PAUSE	Top:top0 time_counter_r[14]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.179
90	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[0]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
91	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[1]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
92	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[2]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
93	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[3]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
94	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[4]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
95	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[5]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
96	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[6]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
97	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[7]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
98	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[8]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
99	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[9]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125
100	-0.453	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 time_counter_r[10]	AUD_BCLK	CLOCK_50	1.000	-0.305	1.125

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-2.736	0.175	N/A	N/A	9.244
1	AUD_BCLK	-2.736	0.201	N/A	N/A	40.585
2	CLOCK2_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
4	CLOCK_50	-2.615	0.175	N/A	N/A	9.244
5	p[0] atp[1] sd1 pl[7] ck[0]	9989.058	0.181	N/A	N/A	4999.708
6	p[0] atp[1] sd1 pl[7] ck[1]	80.591	0.182	N/A	N/A	41.373
2	Design-wide TNS	-118.236	0.0	0.0	0.0	0.0
1	AUD_BCLK	-14.852	0.000	N/A	N/A	0.000
2	CLOCK2_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
4	CLOCK_50	-103.384	0.000	N/A	N/A	0.000
5	p[0] atp[1] sd1 pl[7] ck[0]	0.000	0.000	N/A	N/A	0.000
6	p[0] atp[1] sd1 pl[7] ck[1]	0.000	0.000	N/A	N/A	0.000

		Property	Setup
			Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	29	29
4	Unconstrained Input Port Paths	1048	1048
5	Unconstrained Output Ports	80	80
6	Unconstrained Output Port Paths	299	299

遇到的問題與解決辦法

I2C 的規範很多，一開始沒有全部顧及到，沒辦法錄音及播放，後來查資料還有和同學討論，再加上用 SevenHexDecoder 顯示目前 Top 所在的 state 在板子上才終於修正並確定了 I2C 有合理運作。

一開始錄音播放時雖然有聲音，但會有許多雜訊，似乎是一個給 SRAM data 的 register 值的問題，應該是我們在原本以為沒差的地方把他的值從鎖住變成歸回到 0 就解決了。

Bonus 設計

用七段顯示器顯示目前 Top 工作狀態在閒置，錄音，錄音暫停，播放或播放暫

停。

用七段顯示器顯示目前的錄音時間和目前播放到多少秒的錄音。

用七段顯示器顯示目前的播放是快速還是慢速，是 $2(1/2)$ 倍還是 $3(1/3)$ 倍...，且
可在播放過程中隨意調整速度。

能夠倒著播放錄好的音訊。