Avnet Zynq Mini-ITX Motherboard
Board Definition File Installation and Tutorial
(Vivado 2015.3)

Version 1.0
May 2015

AVNET electronics marketing

1 Installing the Avnet Board Definition Files

Please unzip the **zynq_mini_itx_board_files_v2015_3.zip** file to the following folder of the Vivado 2015.3 install directory.

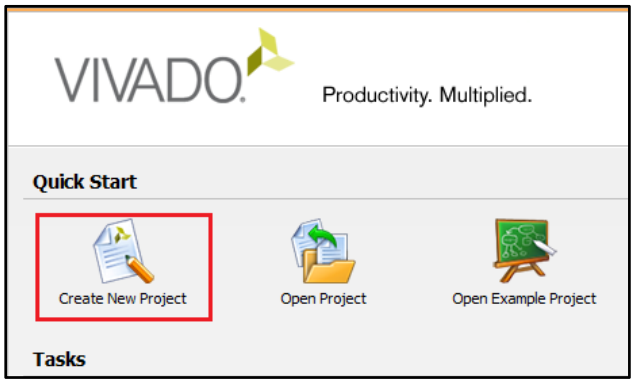
<install_location>\Vivado\2015.3\data\boards\board_files

2 Using the Avnet Board Definition Files in Vivado 2015.3

Once the Avnet board definition files are installed, they can be used to generate a Zynq based design. Please follow the steps shown below to generate an example design using the Avnet board files in Vivado 2015.3 tool.

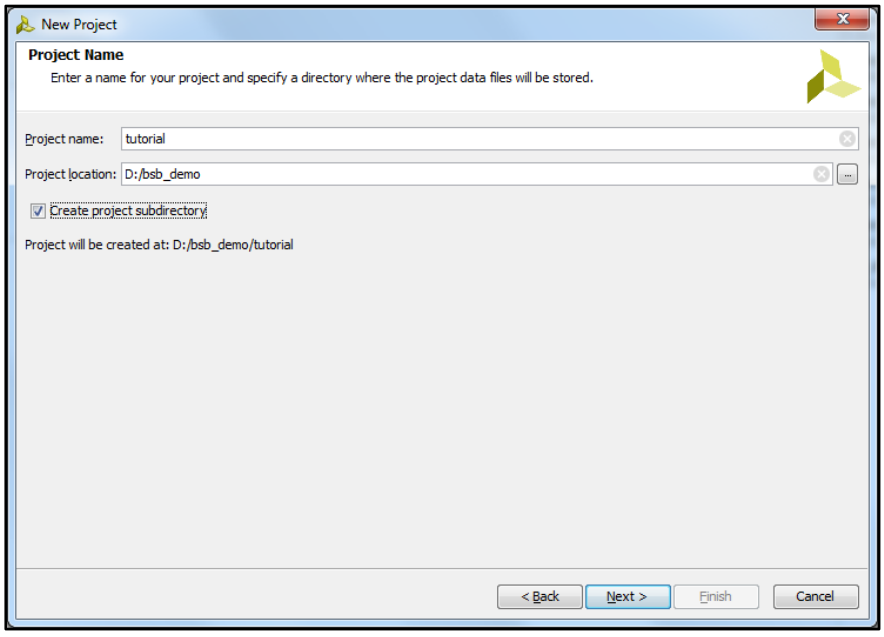
- Start the Vivado tool via **Start > All Programs > Xilinx Design Tools > Vivado 2015.3 > Vivado 2015.3**

- Select **Create New Project**.

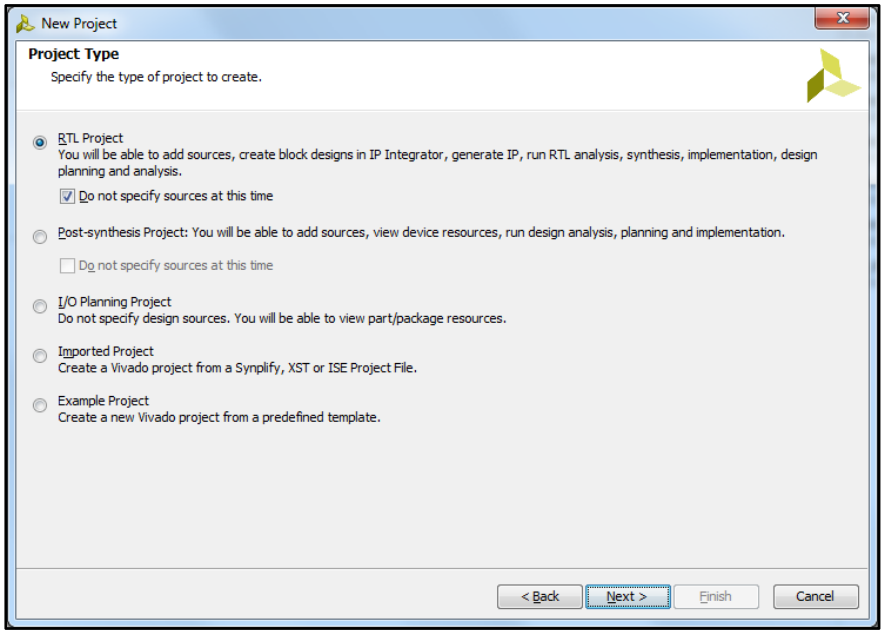


- Click **Next** to continue.

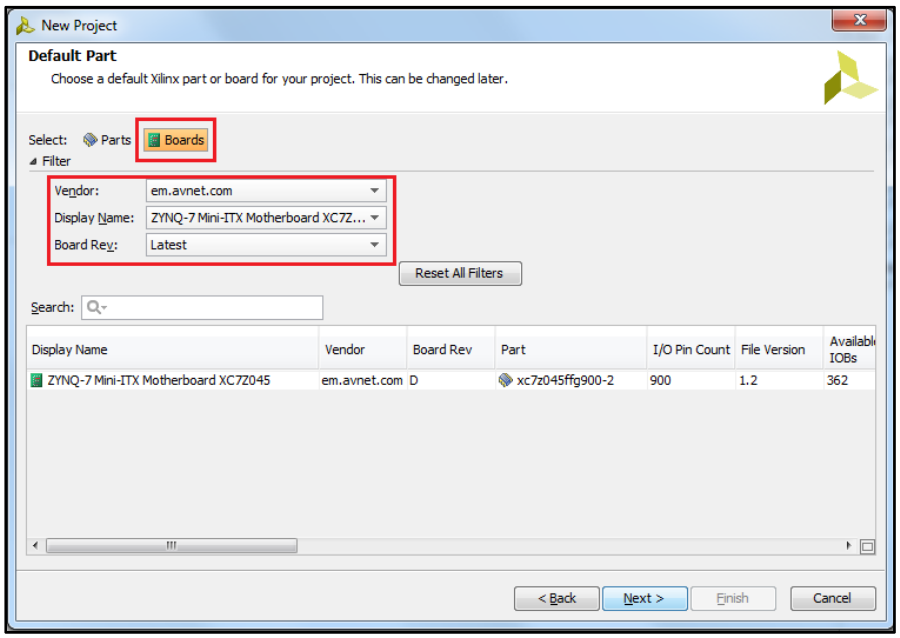
- Set the project name and location and click **Next** to continue. In this case, the project location is set to **D:/bsb_demo** and the project name is set to **tutorial**. Make sure the **Create project subdirectory** box is checked as shown in the following figure.



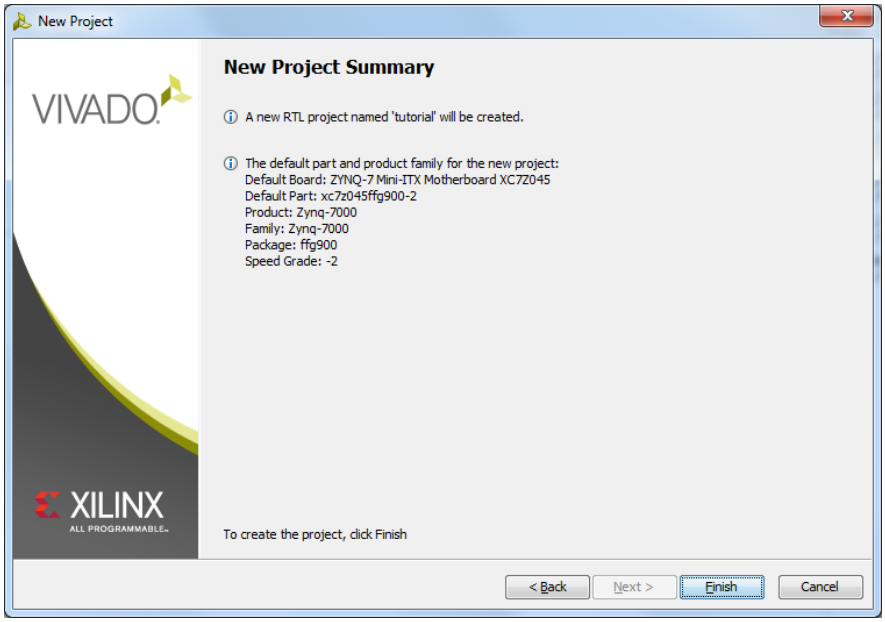
- Select the **RTL Project** type and make sure the **Do not specify sources at this time** box is checked as shown in the following figure. Click **Next** to continue.



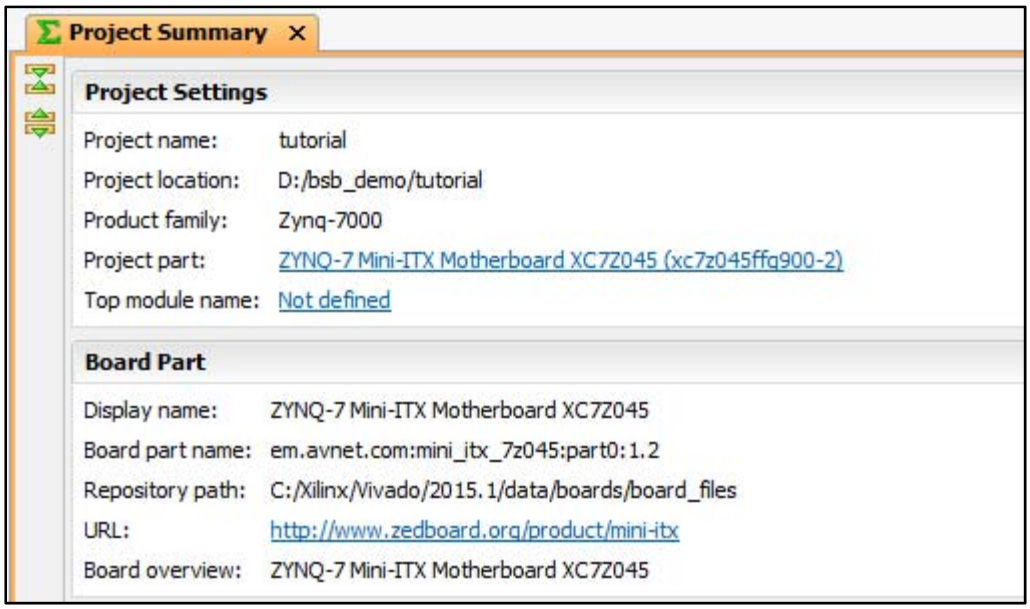
- In the **Default Part** dialog box
  a. Click on **Boards** next to **Select** type as shown below.
  b. Set the **Vendor** to **em.avnet.com**.
  c. Set the **Display Name** to **ZYNQ-7 Mini-ITX Motherboard XC7Z045** (Alternatively, you can set the board to **ZYNQ-7 Mini-ITX Motherboard XC7Z100).**
  d. Set the **Board Rev** to **Latest**.
  e. Click **Next** to continue.



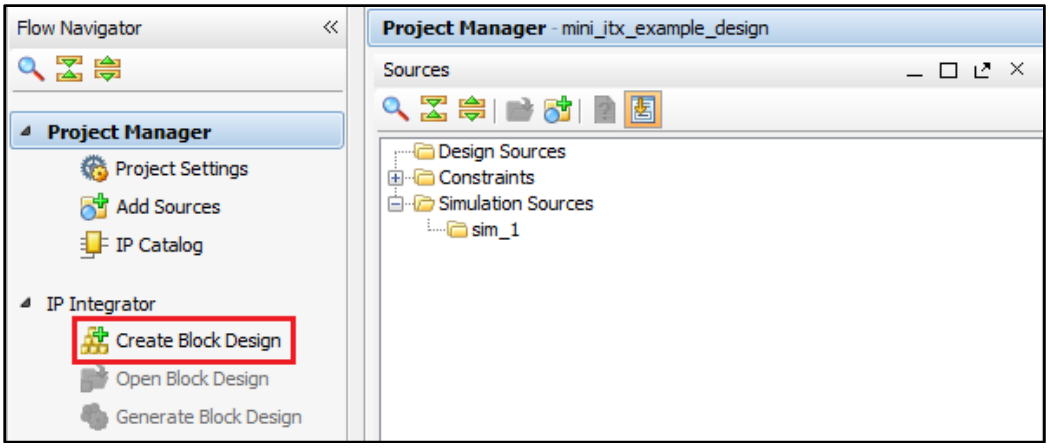
- Click **Finish** to continue.



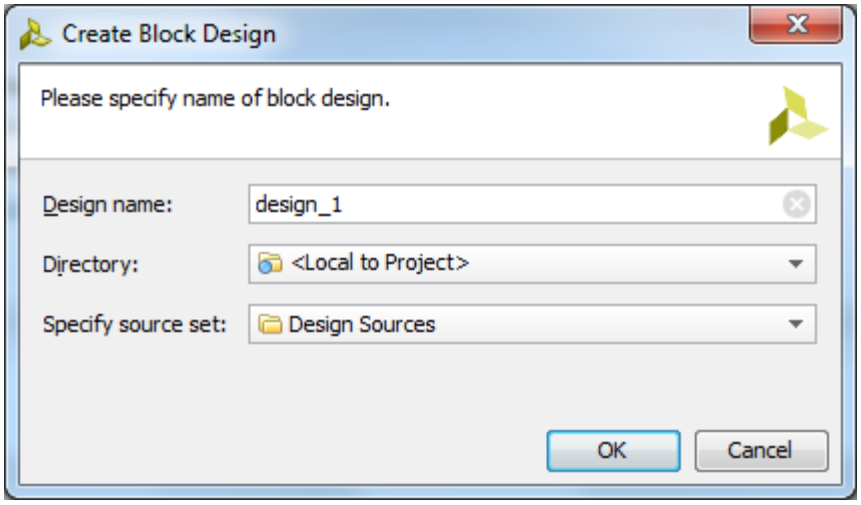
The Vivado Project Summary should look as shown in the following figure (the screenshot will be different when using the **ZYNQ-7 Mini-ITX Motherboard XC7Z100** board).



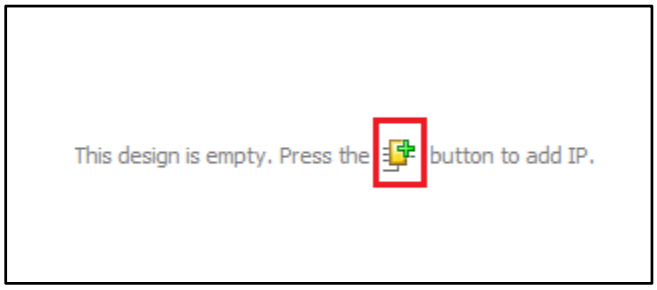
- Click on the **Create Block Design** as shown in the following figure.



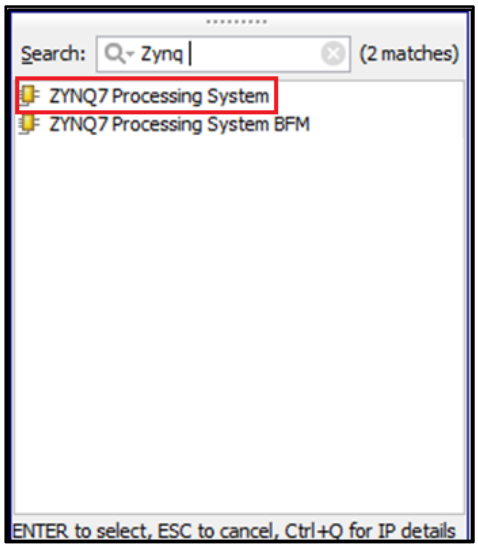
- When the following dialog box appears, click **OK** to continue.



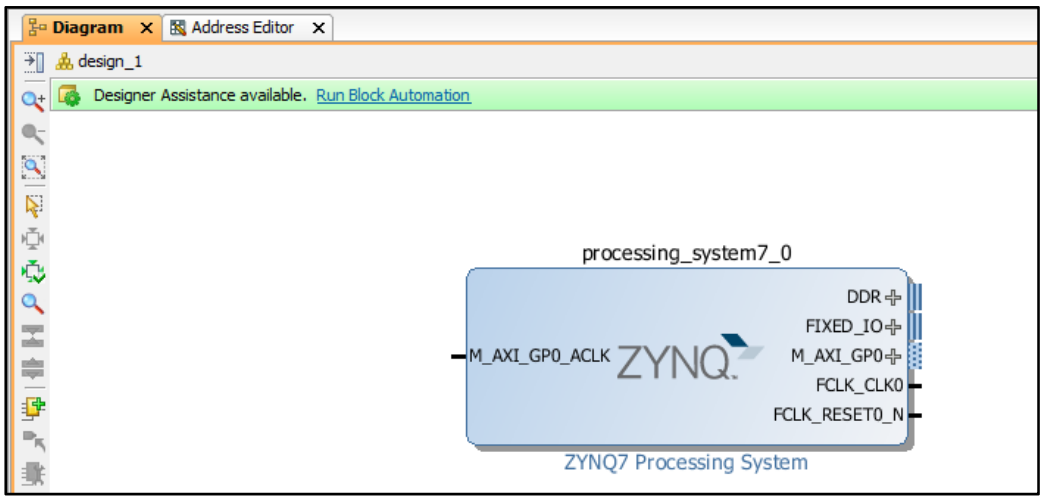
- Click on the **Add IP** icon in the white canvas area as shown in the following figure.



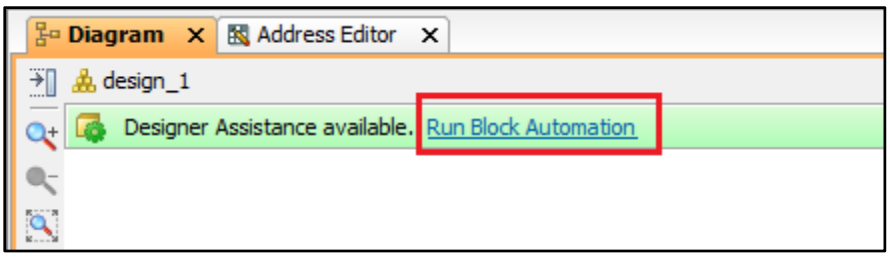
- Type **Zynq** in the **Search** box and then double-click on the **ZYNQ7 Processing System** IP as shown in the following figure.



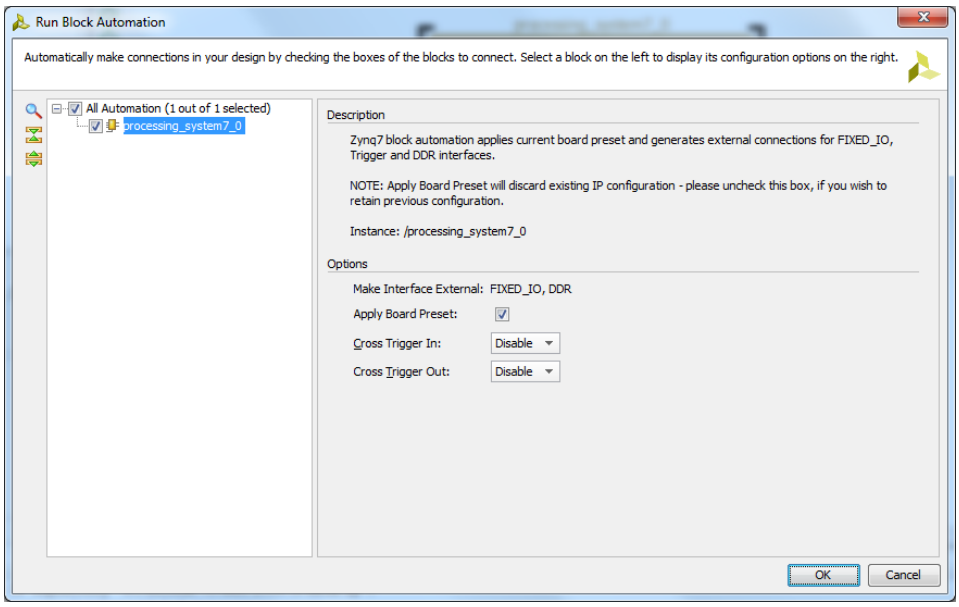
The Zynq IP will be added to the design as shown in the following figure.



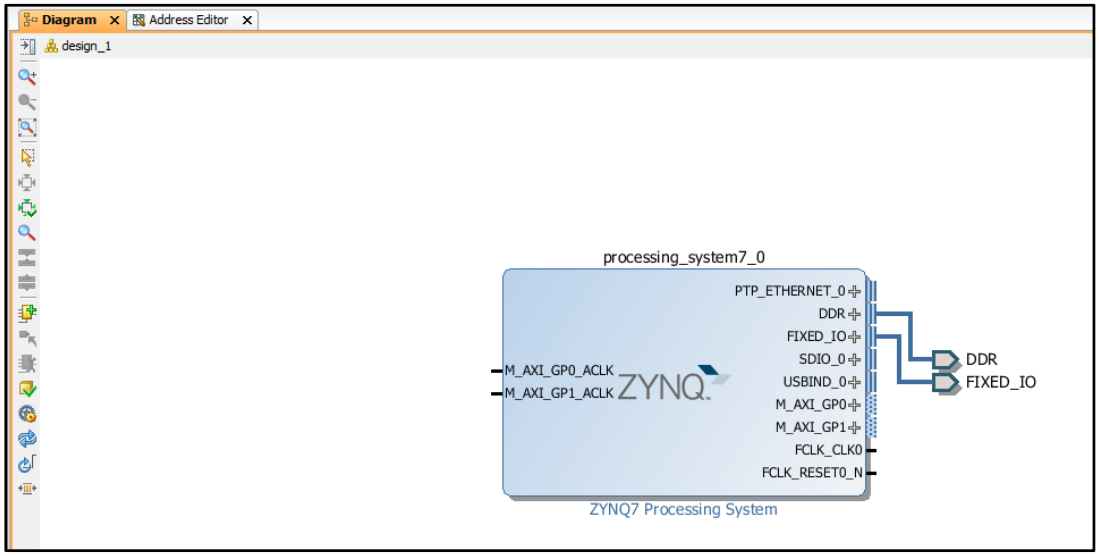
- The Zynq device has not yet been configured for the Avnet Mini-ITX board. Click on the **Run Block Automation** to configure the Zynq device with the Mini-ITX board settings.



- When the following dialog box appears, click **OK** to continue.

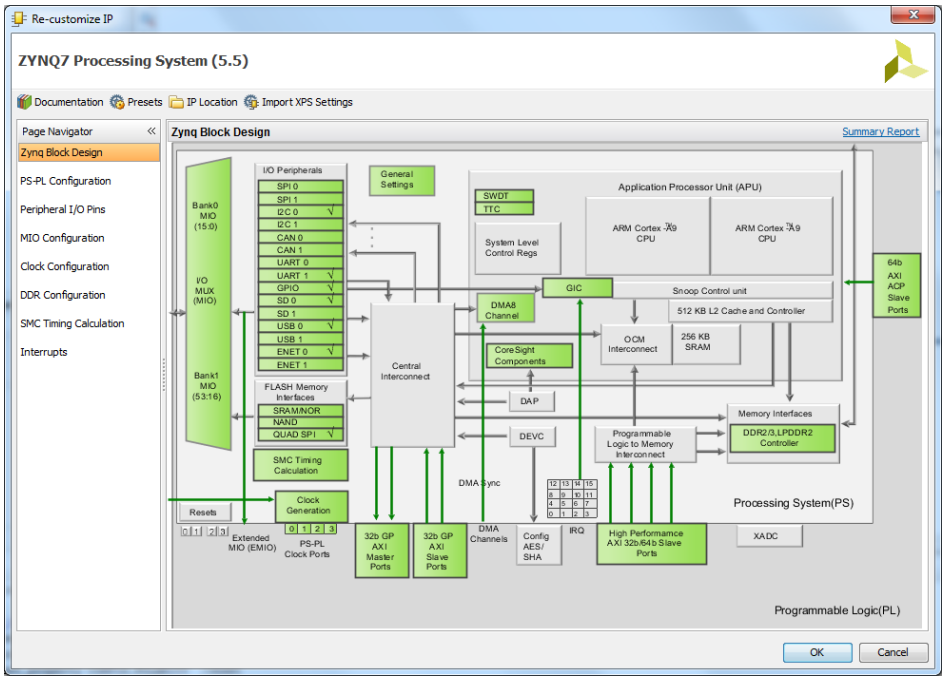


- The Zynq device will be configures as shown in the following figure. The Zynq device is now configured with the Zynq Mini-ITX board level settings such as PS DDR3, PS peripheral selections, clocking, etc.

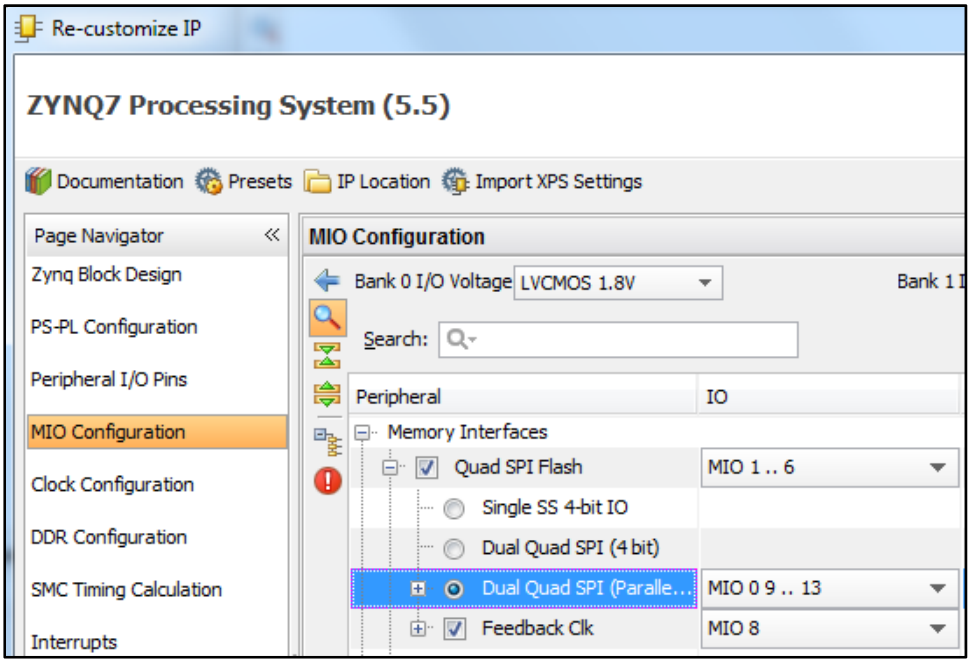


- The Avnet Mini-ITX board uses two QSPI x4 devices to boot and configure the Zynq device. However, in Vivado 2015.3 designs using the board definition files, only one QSPI device gets enabled. So, after configuring the Zynq device with the Mini-ITX board setting, the second QSPI device must be enabled manually.

  Double-Click on the Zynq IP in the Vivado block design to open the Zynq **Re-customize IP** dialog box as shown in the following figure.

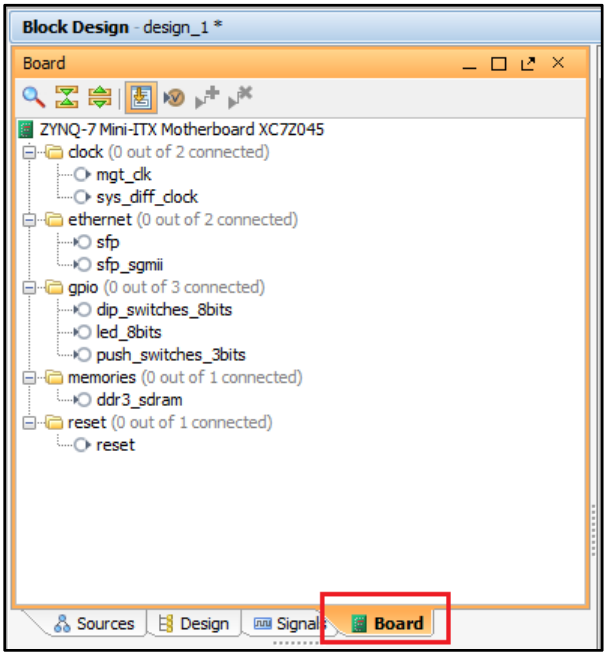


- In the **Re-customize IP** dialog box:
    a. Click on the **MIO Configuration** under the **Page Navigator**.
    b. Expand the **Memory Interfaces**.
    c. Expand the **Quad SPI Flash**.
    d. Select the **Dual Quad SPI** option as shown below.
    e. Click OK to continue.

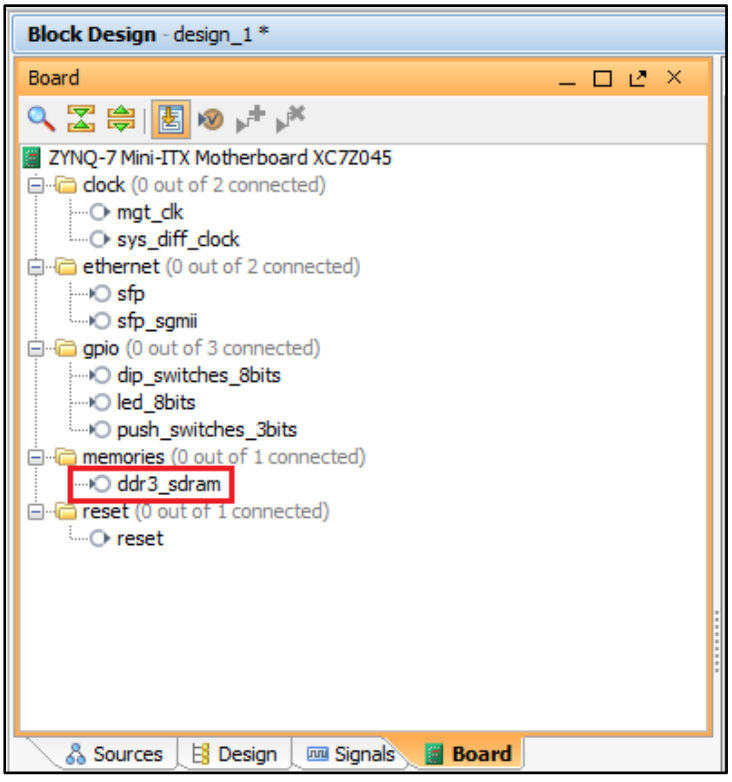


You are now ready to add memory and peripherals to the design that are connected to the Zynq PL on the Mini-ITX board such as PL DDR3, LEDs, DIP switches, and Push switches.

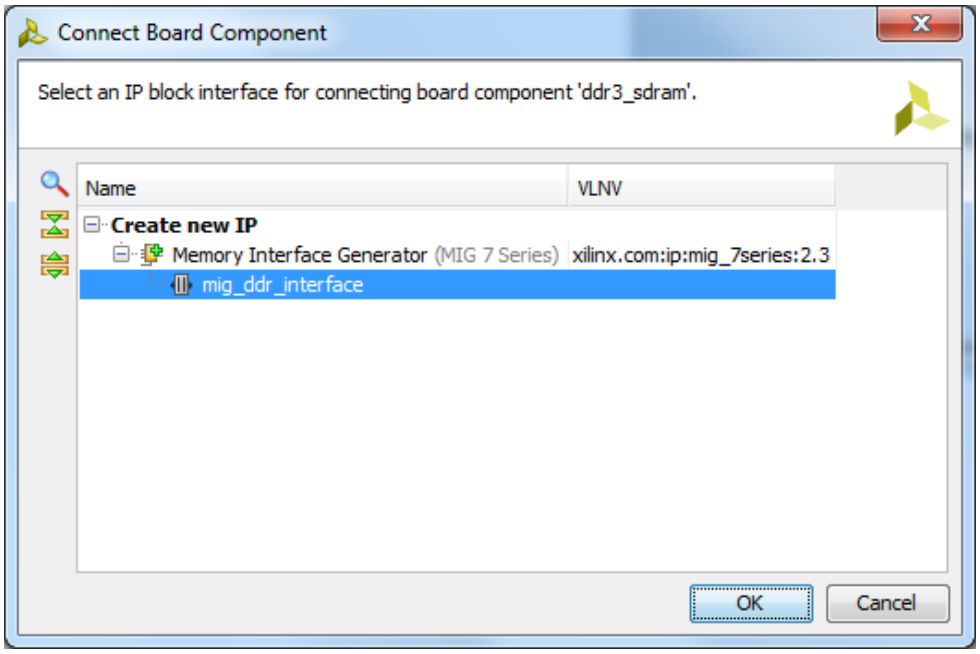
- Under **Block Design** window in Vivado, click on the **Board** tab as shown in the following figure. You will see a set of memory and peripherals that can be connected to the Zynq PL on the Mini-ITX board.



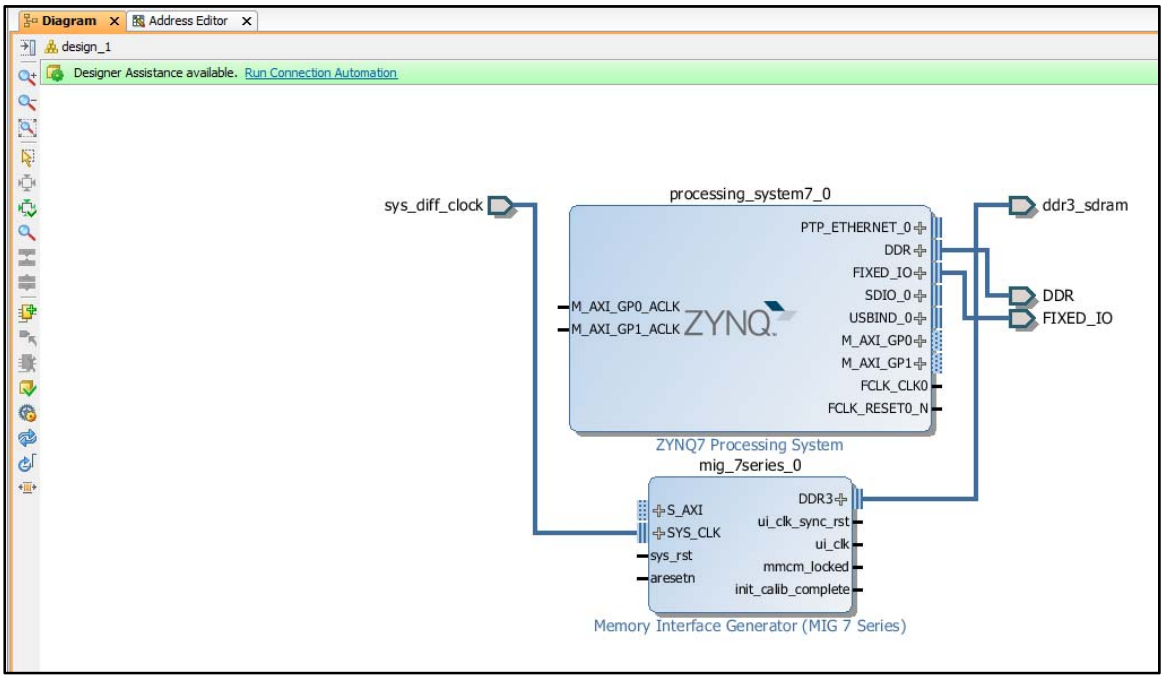
- Double click on the **ddr3_sdram** as shown in the following figure to add the PL DDR3 interface to the design.



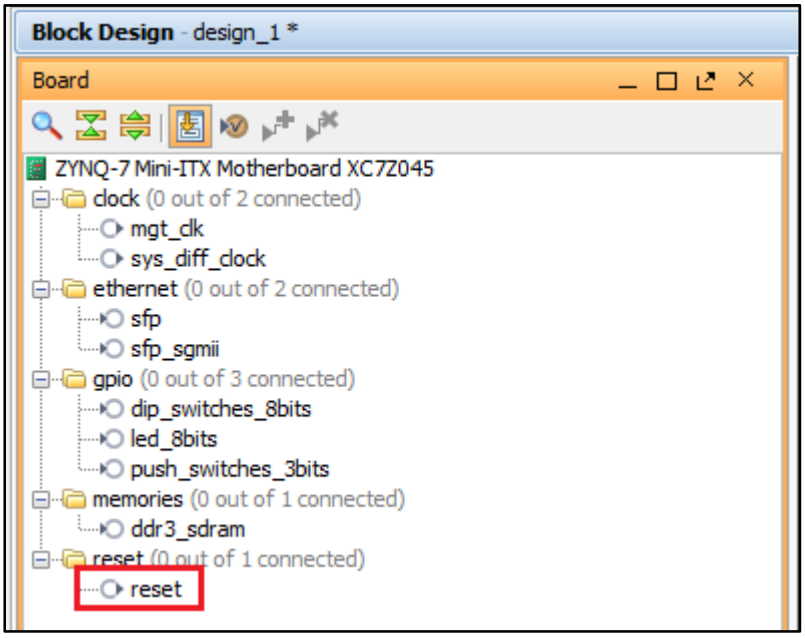
- When the following dialog box appears, click **OK** to continue. This will add the PL DDR3 interface to the design.



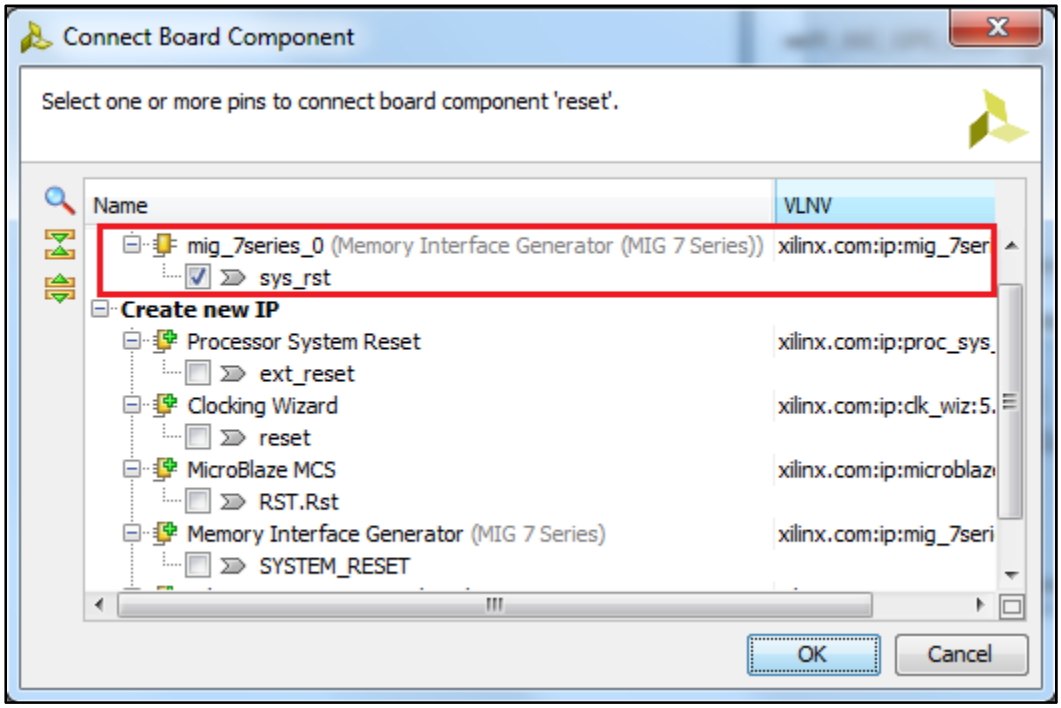
The block design will look as shown in the following figure with the PL DDR3 MIG controller instantiated in the design and the PL DDR3 signals as well as the system clock assigned to the device pins.



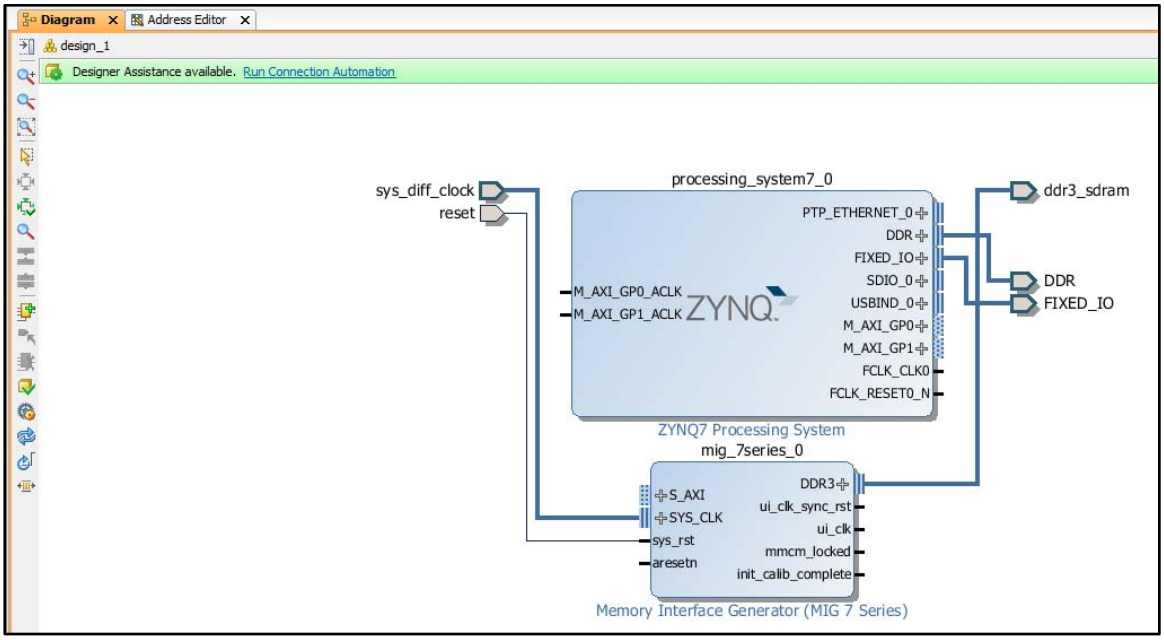
- Double click on the **reset** as shown in the following figure to add the eternal PL reset signal to the PL DDR3 MIG controller.



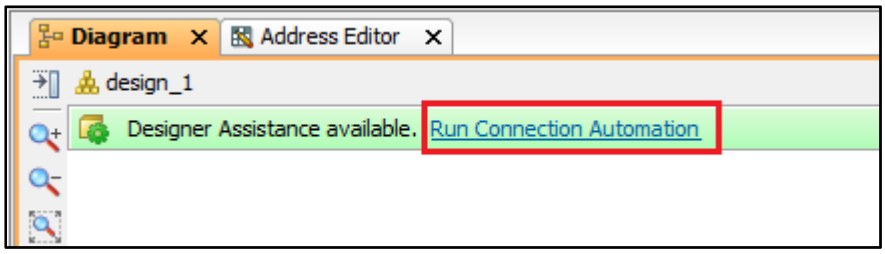
- When the following dialog box appears, click **OK** to continue. This will connect the PL external **reset** signal to the PL DDR3 MIG controller **sys_rst** signal.



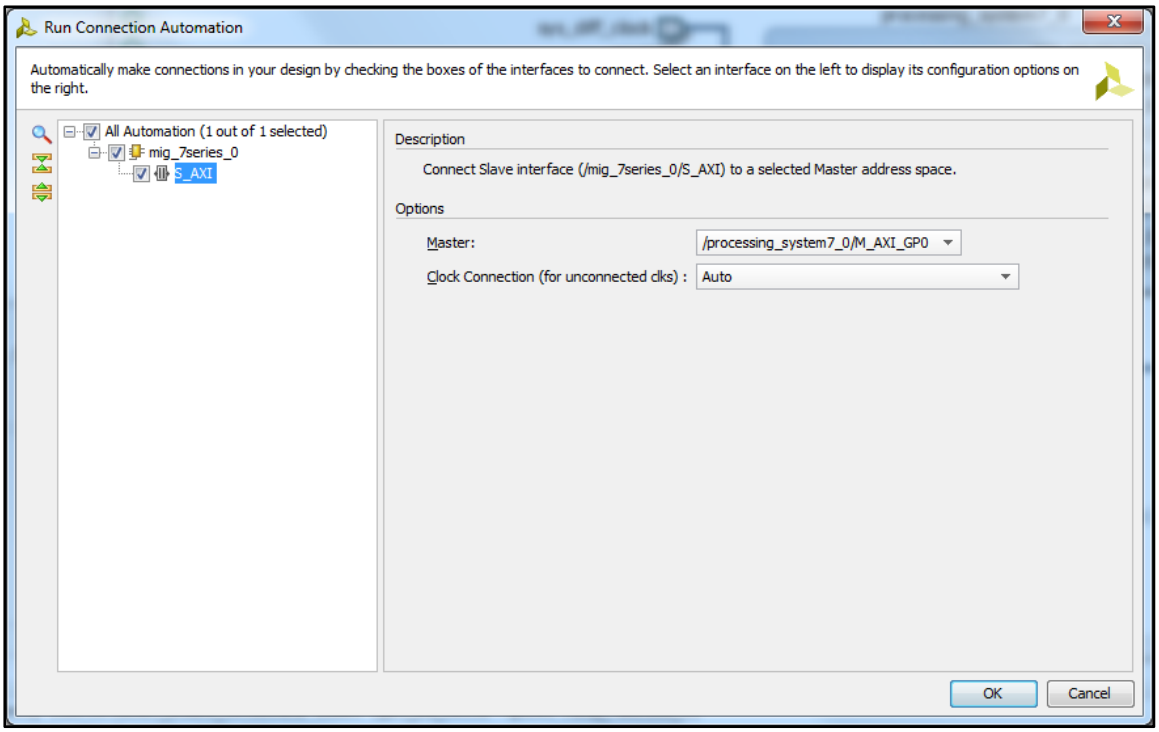
The block design will look as shown in the following figure.



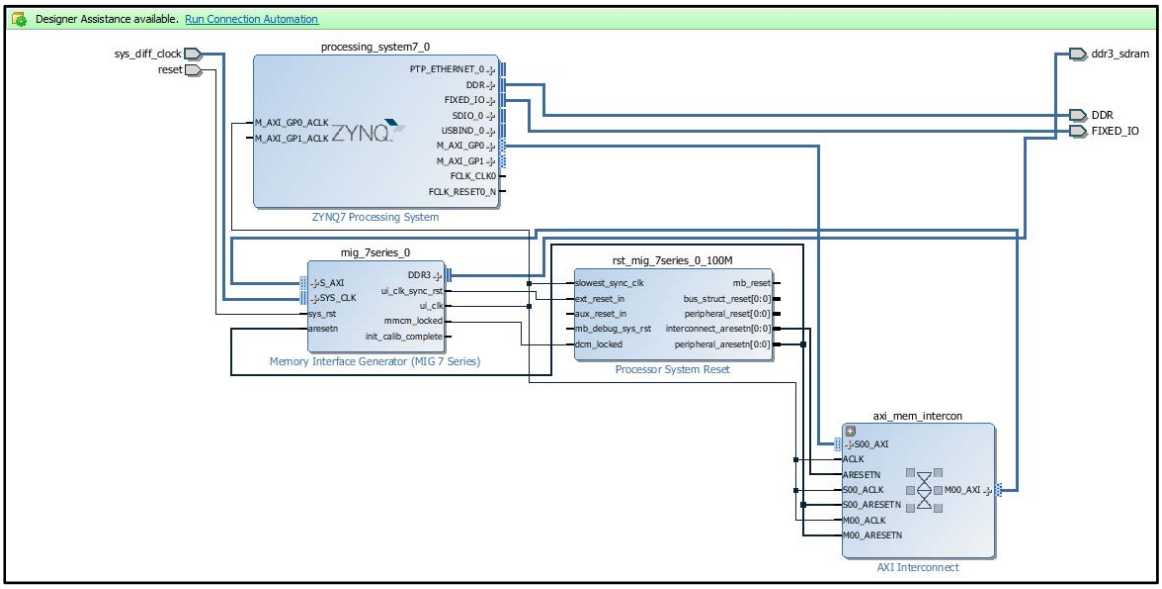
- Click on the **Run Connection Automation** to connect the PL DDR3 MIG controller to the Zynq PS as shown in the following figure.



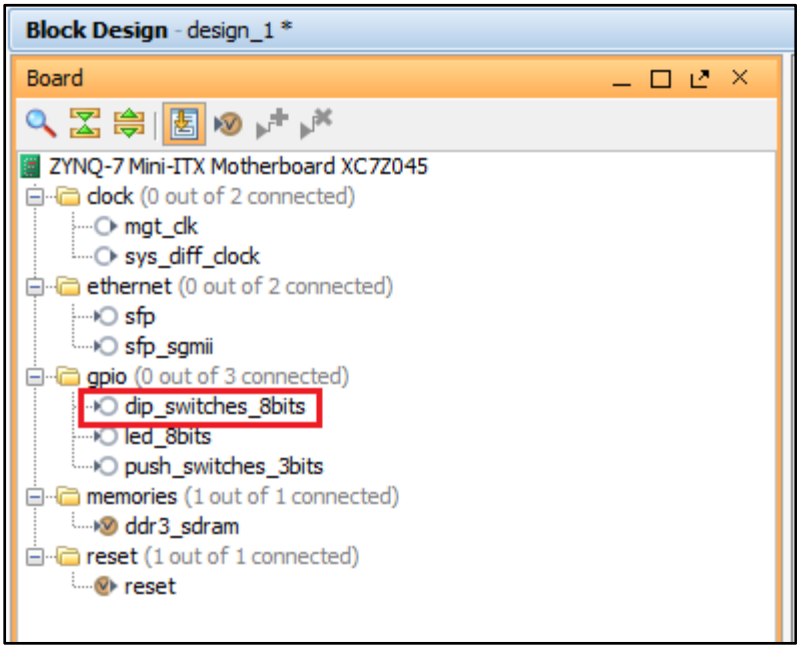
- When the following dialog box appears, click **OK** to continue. The PL DDR3 will be connected to the PS General-Purpose GP0 interface. The Zynq architecture allocates 1GB of address space to the GP0 interface. The entire GP0 1GB address space will occupied by the PL DDR3 interface. Hence, no other PL peripherals can be connected to the GP0 interface.



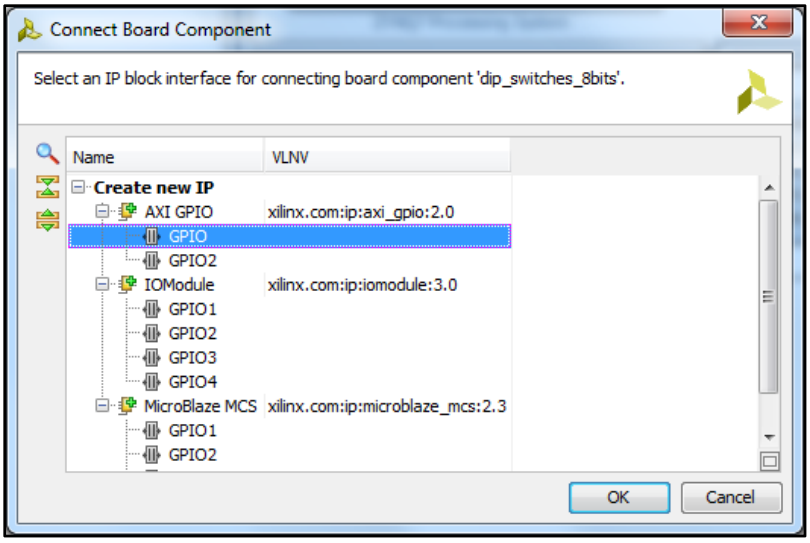
The block design will look as shown in the following figure.



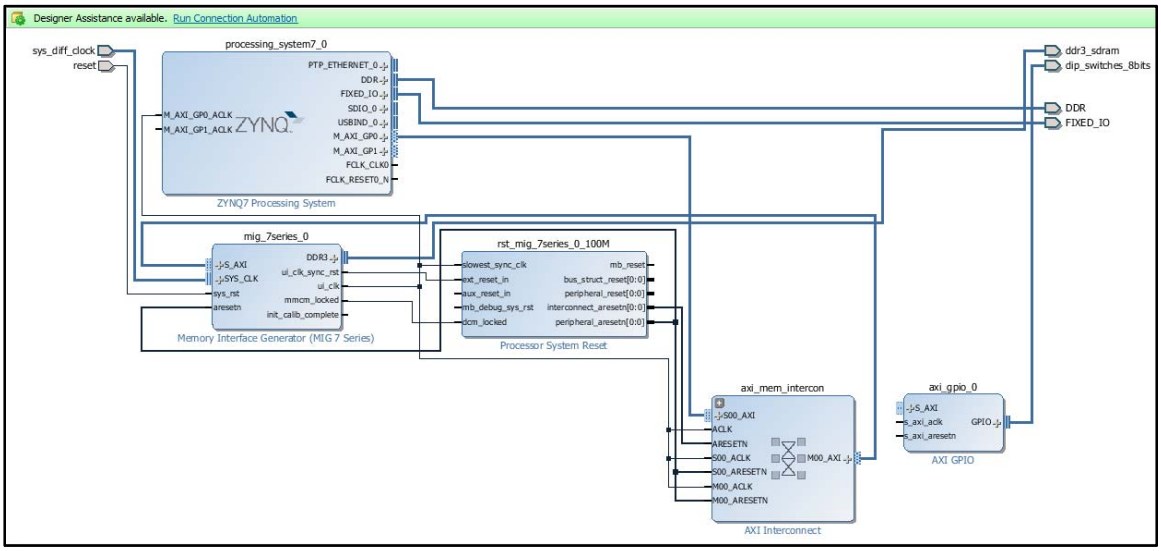
- Double click on the **dip_switches_8bits** as shown in the following figure to add the eternal PL 8-position DIP switches to the design. This will add a PL GPIO core to the design so that the DIP switches can be read via the Zynq PS.



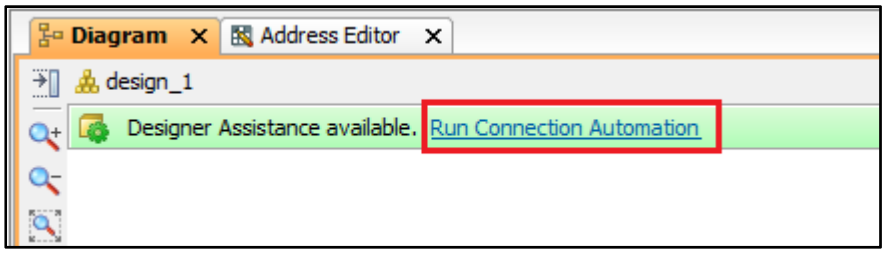
- When the following dialog box appears, make sure the **GPIO** is selected as shown and click **OK** to continue.



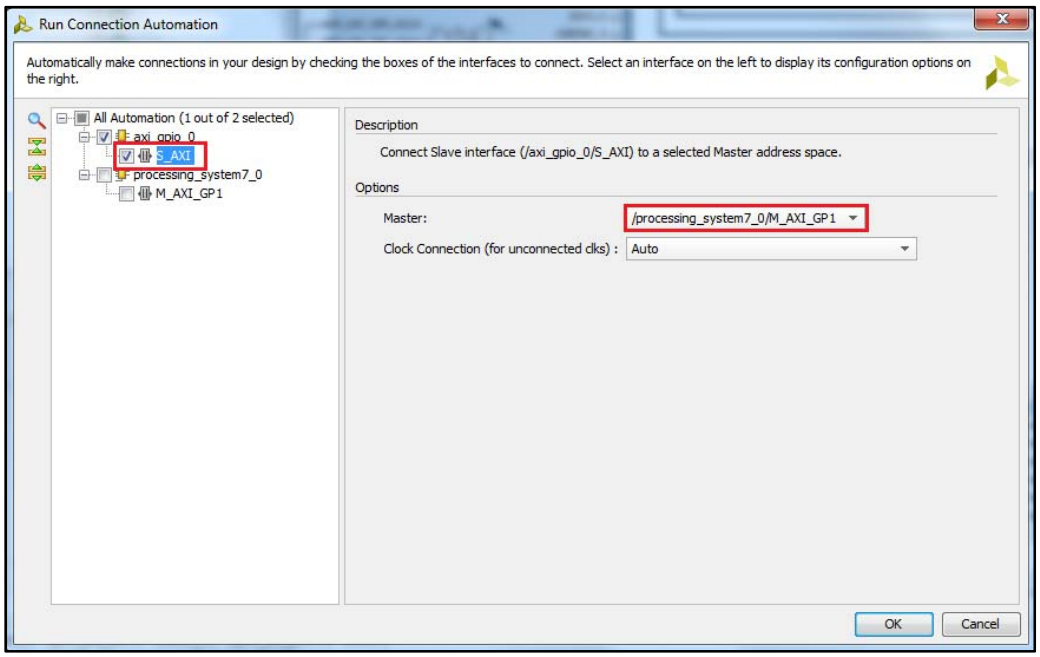
The **axi_gpio_0** IP will be added to the design and the block design will look as shown in the following figure.



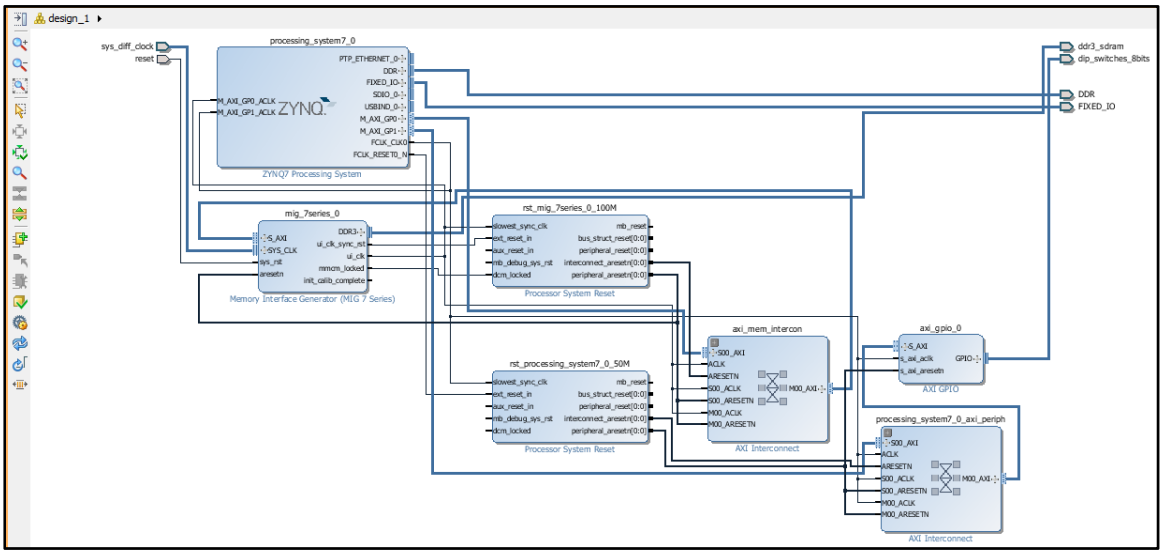
- Click on the **Run Connection Automation** to connect the **axi_gpio_0** IP to the Zynq PS as shown in the following figure.



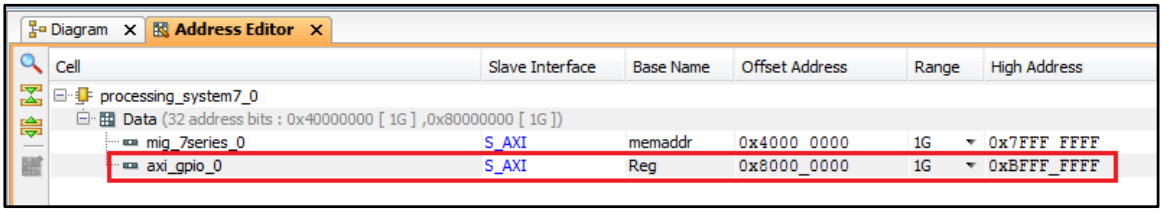
- When the following dialog box appears:
    a. Check the box next to the **S_AXI** as shown in the following figure.
    b. Under the **Options**, set the **Master** to **/processing_system7_0/M_AXI_GP1** as shown. Recall, since **/processing_system7_0/M_AXI_GP0** is connected to the PL DDR3 interface, other PL peripherals or memories cannot be connected to GP0 as the entire GP0 1GB address space is occupied by the PL DDR3.
    c. Click **OK** to continue.



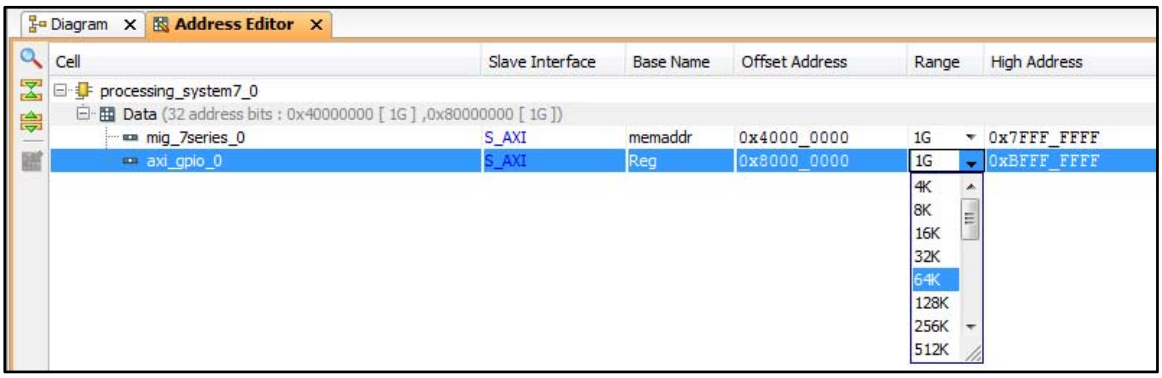
The **axi_gpio_0** IP will be connected to the PS via the **GP1** interface and the block design will look as shown in the following figure.



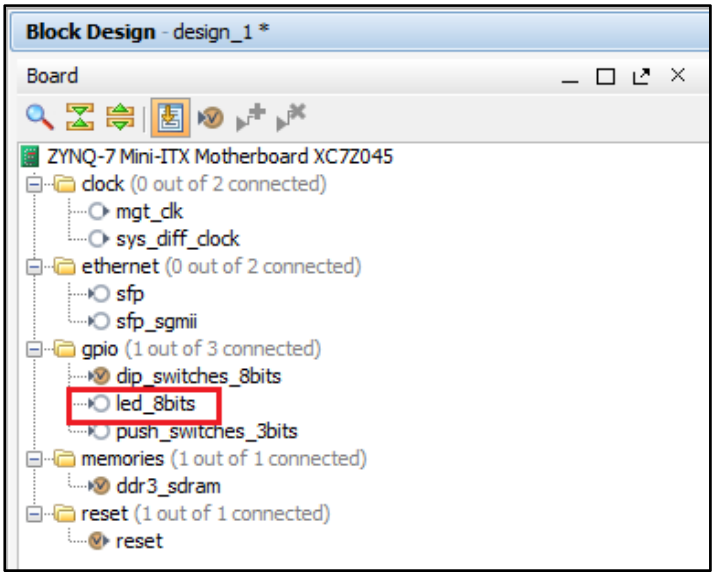
- Click on the **Address Editor** tab as shown in the following figure. You will notice Vivado has assigned 1GB of address space to the **axi_gpio_0** IP which was added to the design in the previous steps.



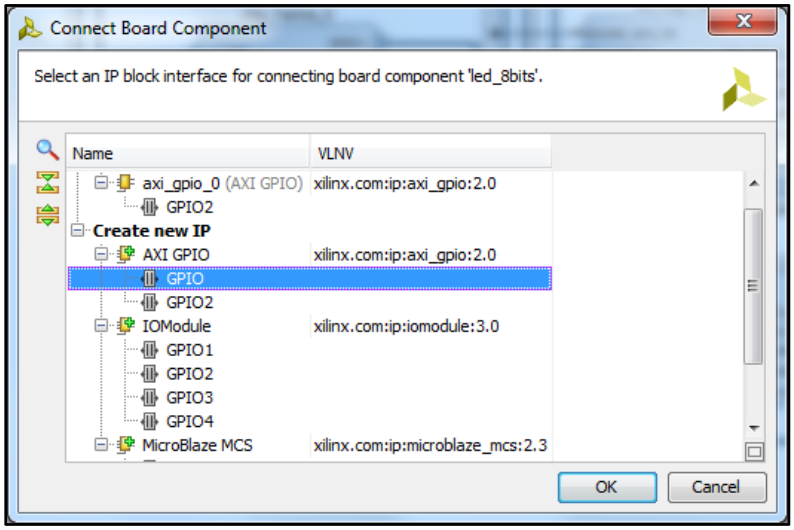
- There is no need for 1GB of address space for the **axi_gpio_0** IP. Also, if 1GB of address space is assigned to the **axi_gpio_0** IP, there won't be any address space left for other peripherals as only 1GB of address space is allocate to GP1. Change the **axi_gpio_0** IP address space to 64KB as shown in the following figure.



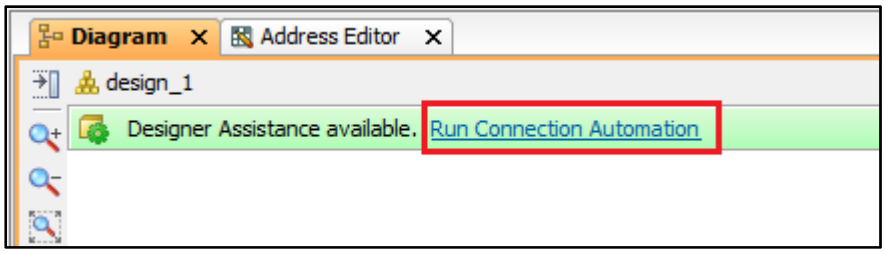
- Double click on the **led_8bits** as shown in the following figure to add the eternal PL LEDs to the design. This will add a PL GPIO core to the design so that the LEDs can be written to via the Zynq PS.



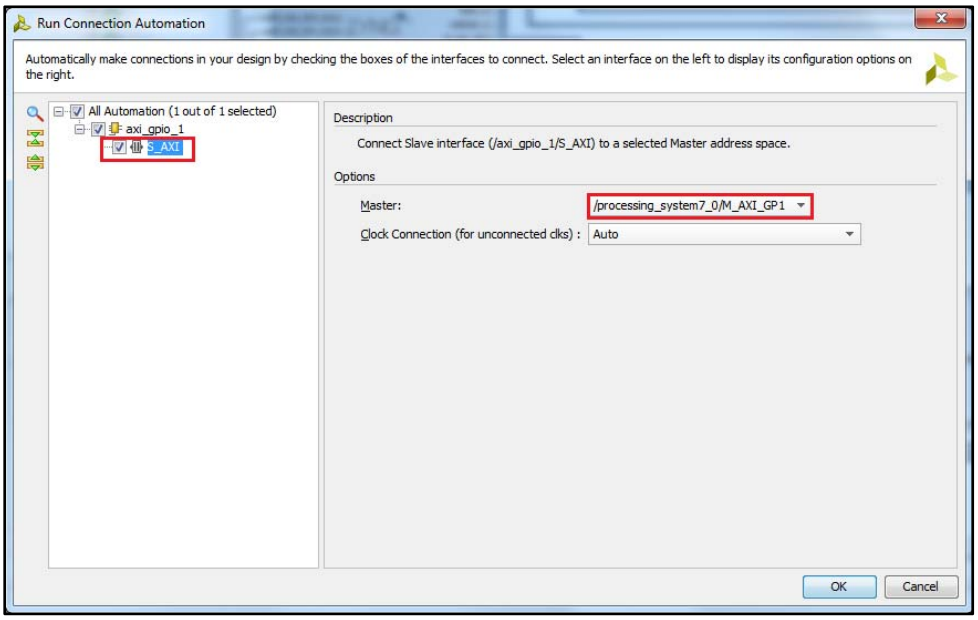
- When the following dialog box appears, select the **GPIO** under the **Create new IP** as shown and then click OK.



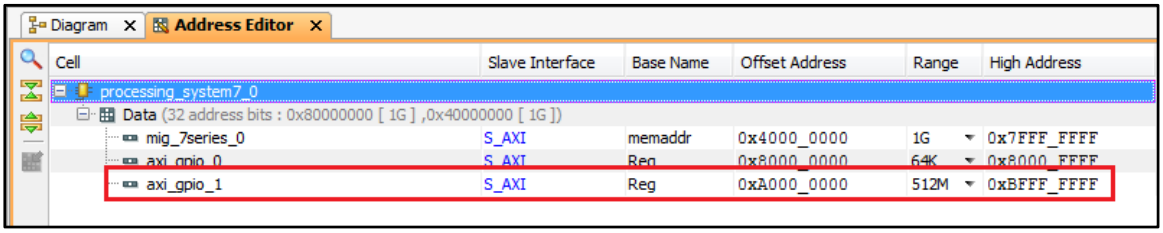
- Click on the **Run Connection Automation** to connect the **axi_gpio_1** IP (the new GPIO just added to the design) to the Zynq PS as shown in the following figure.



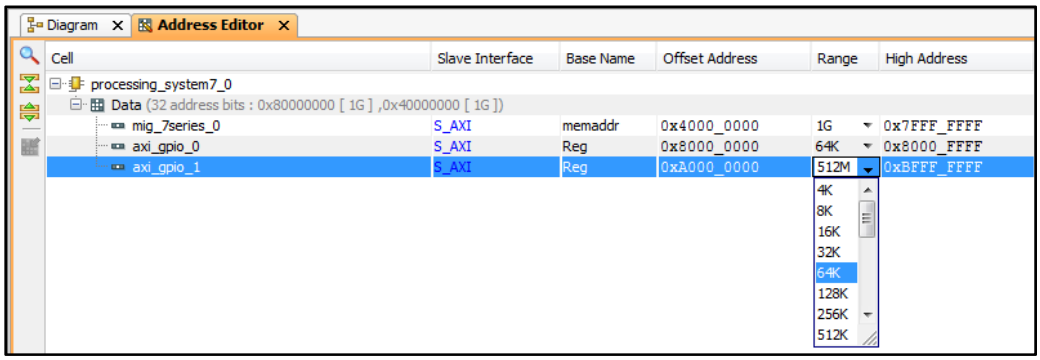
- When the following dialog box appears:
    a. Check the box next to the **S_AXI** as shown in the following figure.
    b. Under the **Options**, set the **Master** to **/processing_system7_0/M_AXI_GP1** as shown.
    c. Click **OK** to continue.



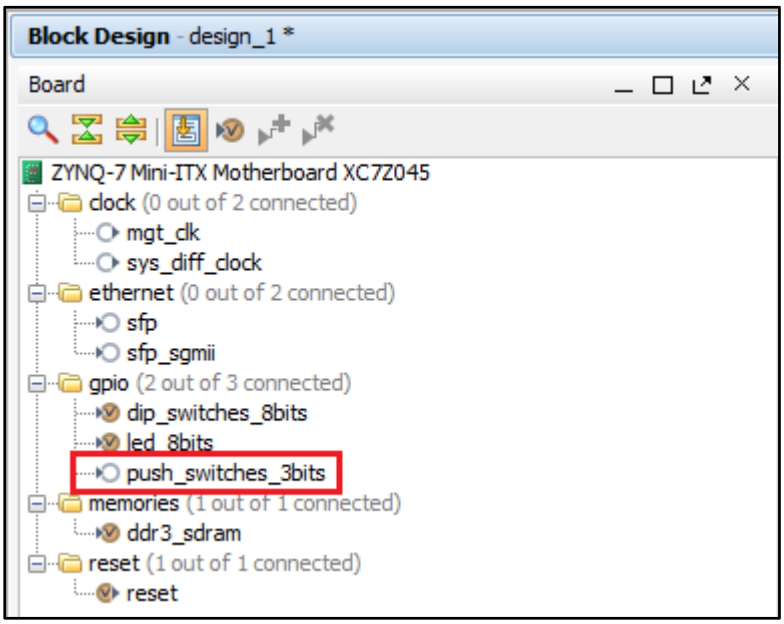
- Click on the **Address Editor** tab as shown in the following figure. You will notice Vivado has assigned 512MB of address space to the **axi_gpio_1** IP.



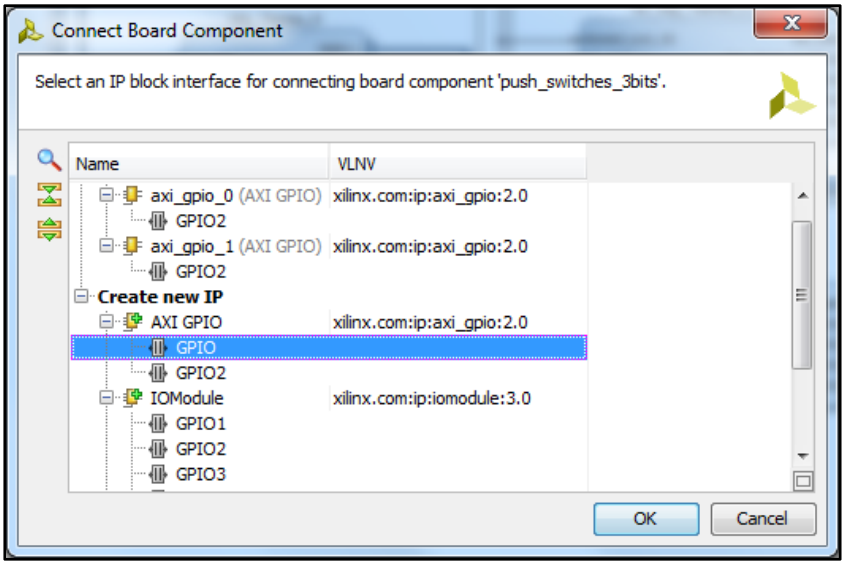
- Change the **axi_gpio_1** IP address space to 64KB as shown in the following figure.



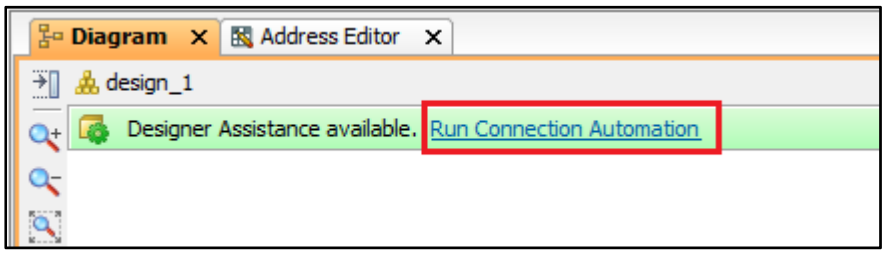
- Double click on the **push_switches_3bits** as shown in the following figure to add the eternal PL Push switches to the design. This will add a PL GPIO core to the design so that the Push switches can be read via the Zynq PS.



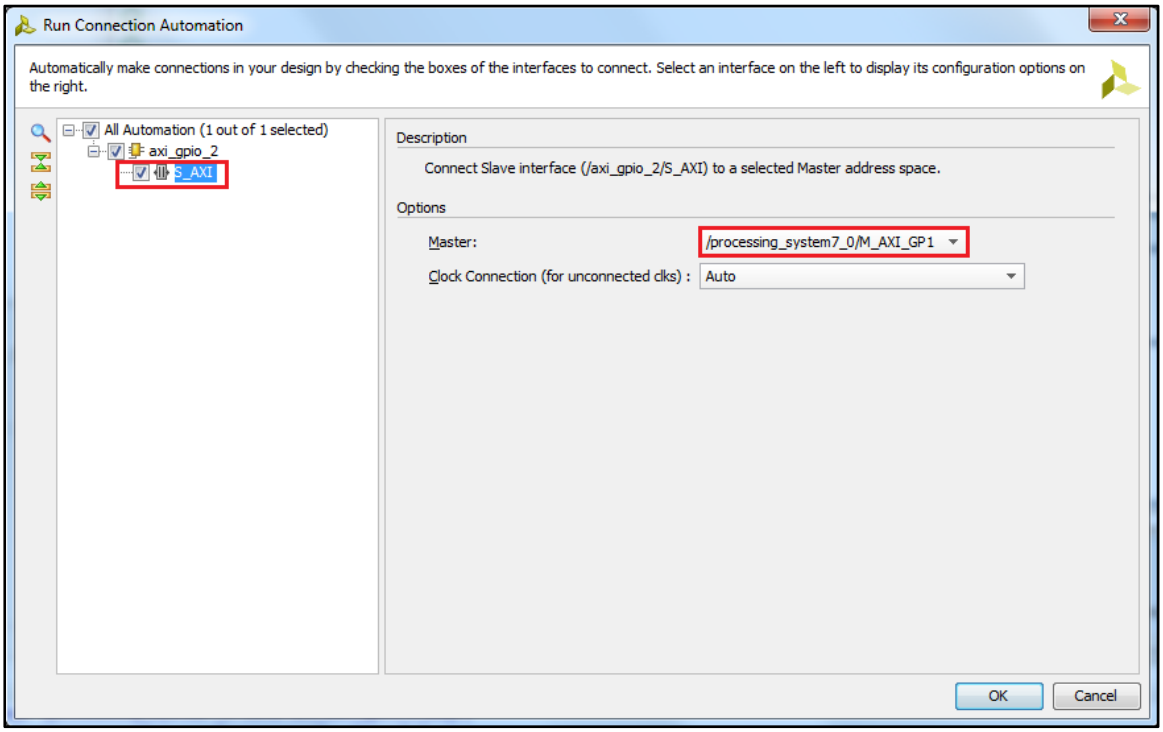
- When the following dialog box appears, select the **GPIO** under the **Create new IP** as shown and then click OK.



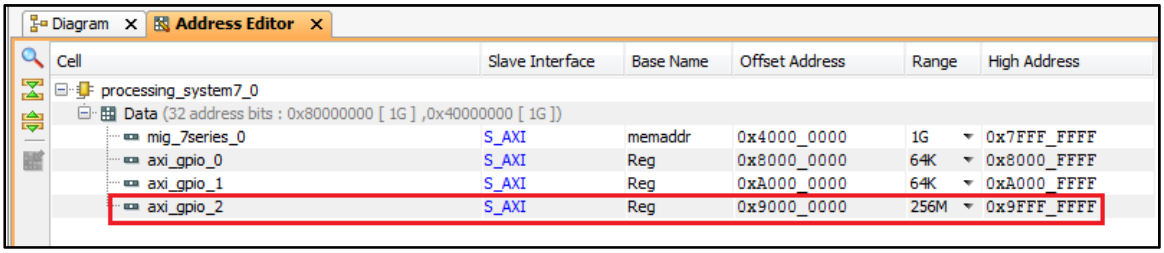
- Click on the **Run Connection Automation** to connect the **axi_gpio_2** IP (the new GPIO just added to the design) to the Zynq PS as shown in the following figure.



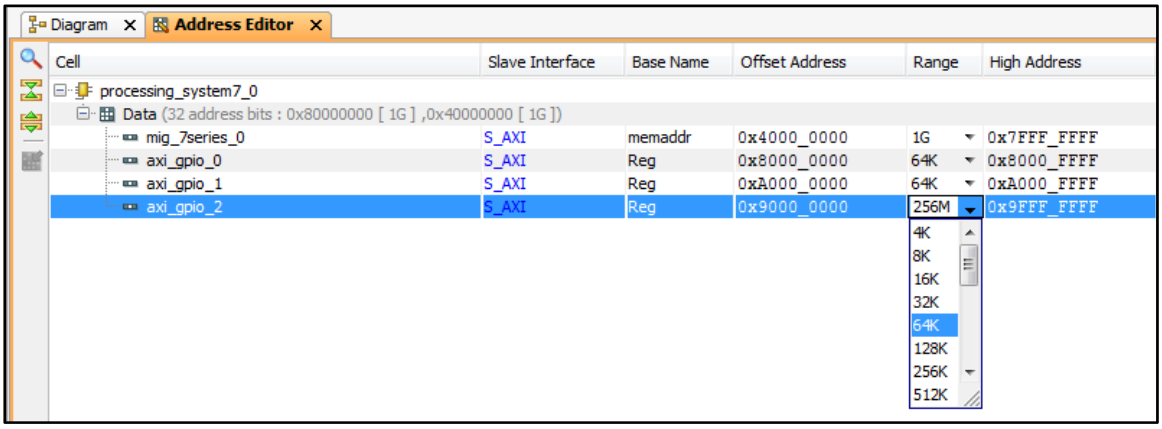
- When the following dialog box appears:
  a. Check the box next to the **S_AXI** as shown in the following figure.
  b. Under the **Options**, set the **Master** to **/processing_system7_0/M_AXI_GP1** as shown.
  c. Click **OK** to continue.



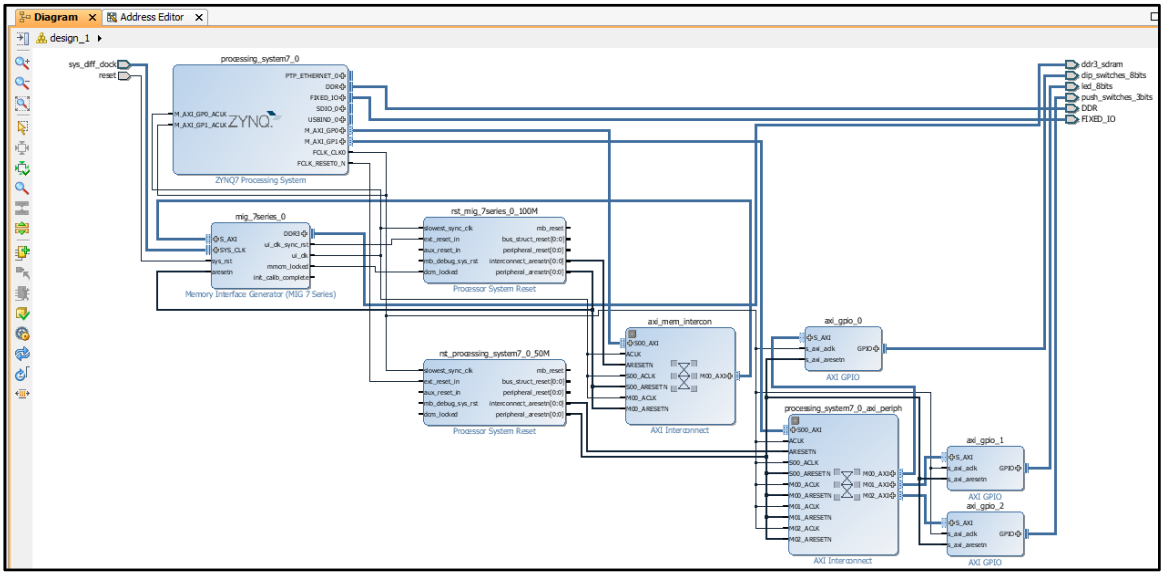
- Click on the **Address Editor** tab as shown in the following figure. You will notice Vivado has assigned 256MB of address space to the **axi_gpio_2** IP.



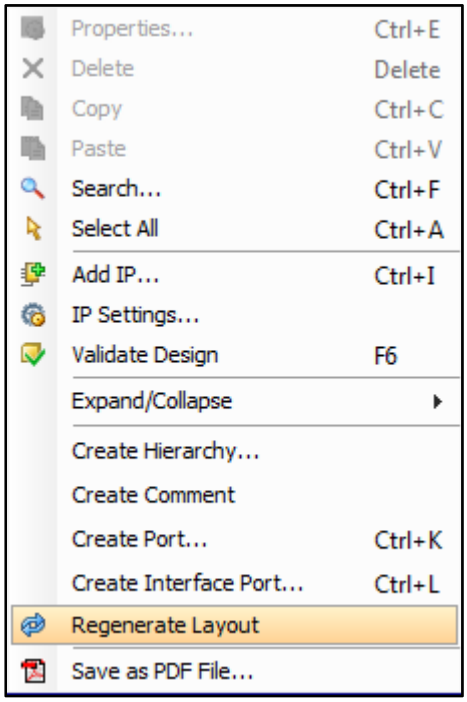
- Change the **axi_gpio_2** IP address space to 64KB as shown in the following figure.



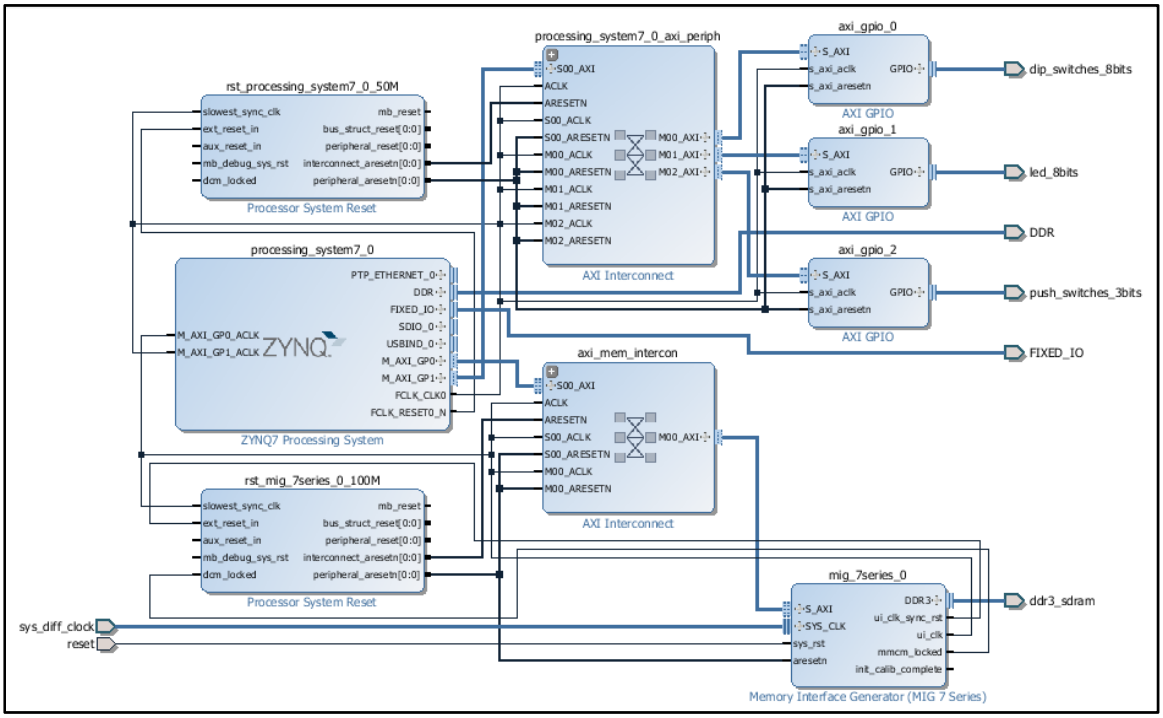
The block design will look as shown in the following figure.



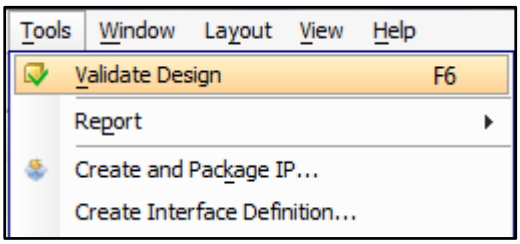
- Right-click in the white space of the block design diagram and select **Regenerate Layout** as shown in the following figure.



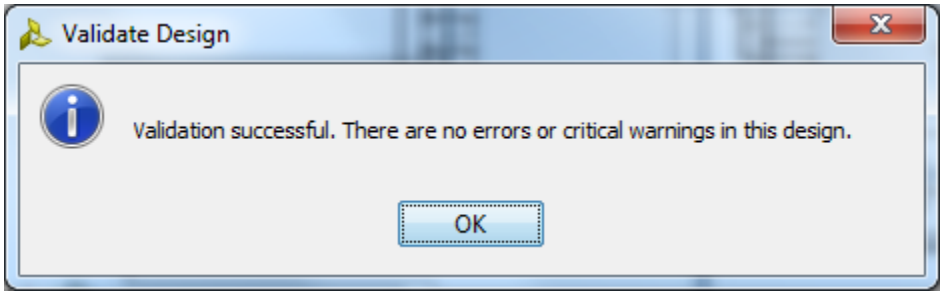
This will clean up the block design drawing and places all PL memory and peripheral interfaces (MIG DDR3 controller and the 3 GPIO ports) to the right of the block design as shown in the following figure.



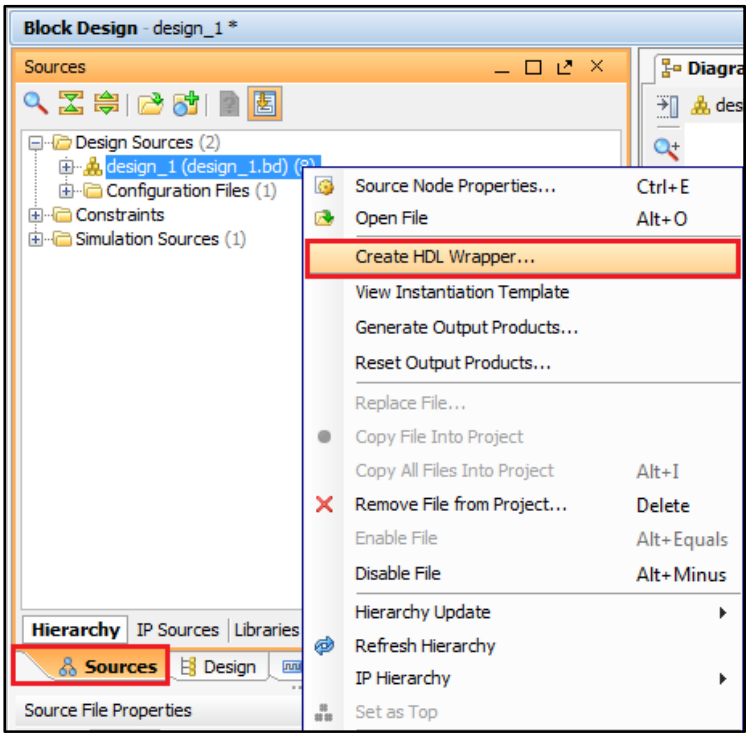
- Select **Tools > Validate Design** from the Vivado toolbar as shown in the following figure. This will validate the design to make sure all block design connections are valid.



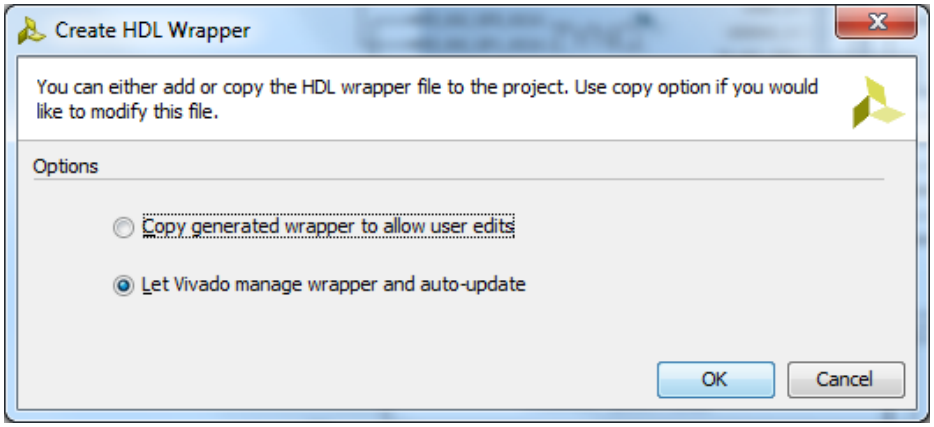
- When the following dialog box appears, click **OK** to continue.



- Click on the **Sources** tab as shown in the following figure. Then right-click on the **design_1 (design_1.bd) (8)** and select **Create HDL Wrapper**. This will create a top-level HDL wrapper file for the design.



- When the following dialog box appears, click OK to continue.



The generation of the hardware platform using the Mini-ITX Board Definition Files is now completed. You can now build the design, generate a bit file, export the hardware platform to the SDK, and begin running test software and applications on the hardware platform.