ECE 322L
Electronics 2

04/14/20 - Lecture 21

Intro to power amplifiers

Power transistors

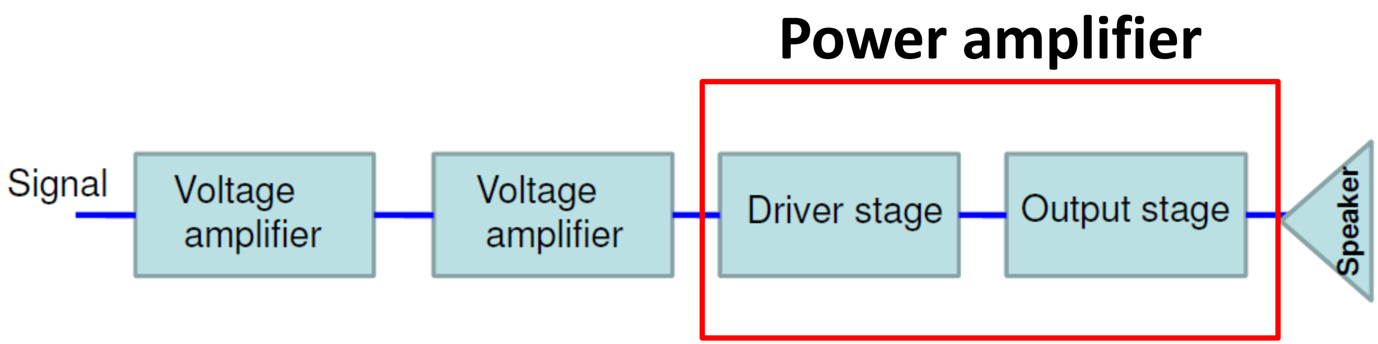
Overview

- Introduction to power amplifiers
- Power considerations
- Power transistors-BJT
- Originfof current, voltage, and power rating for a transistor.
- Safe operating area (SOA)
- Heat transfer models from the device to the ambient.

(Neamen 6.10, 8.1, 8.2.1, 8.2.4-S&S, 6th edition, 11.7)

Power Amplifiers

- ➢ **Large-signal amplifiers**
- ➢ **Generally the last stage of a multistage amplifier.**
- ➢ **The function of a practical power amplifier is to deliver high power to an output device, such as a loud speaker.**
- ➢ **Typical output power rating of a power amplifier will be 1W or higher. The schematic diagram of a multi-stage amplifier utilizing a power amplifier is shown below**



Desired functionalities of a power amplifier

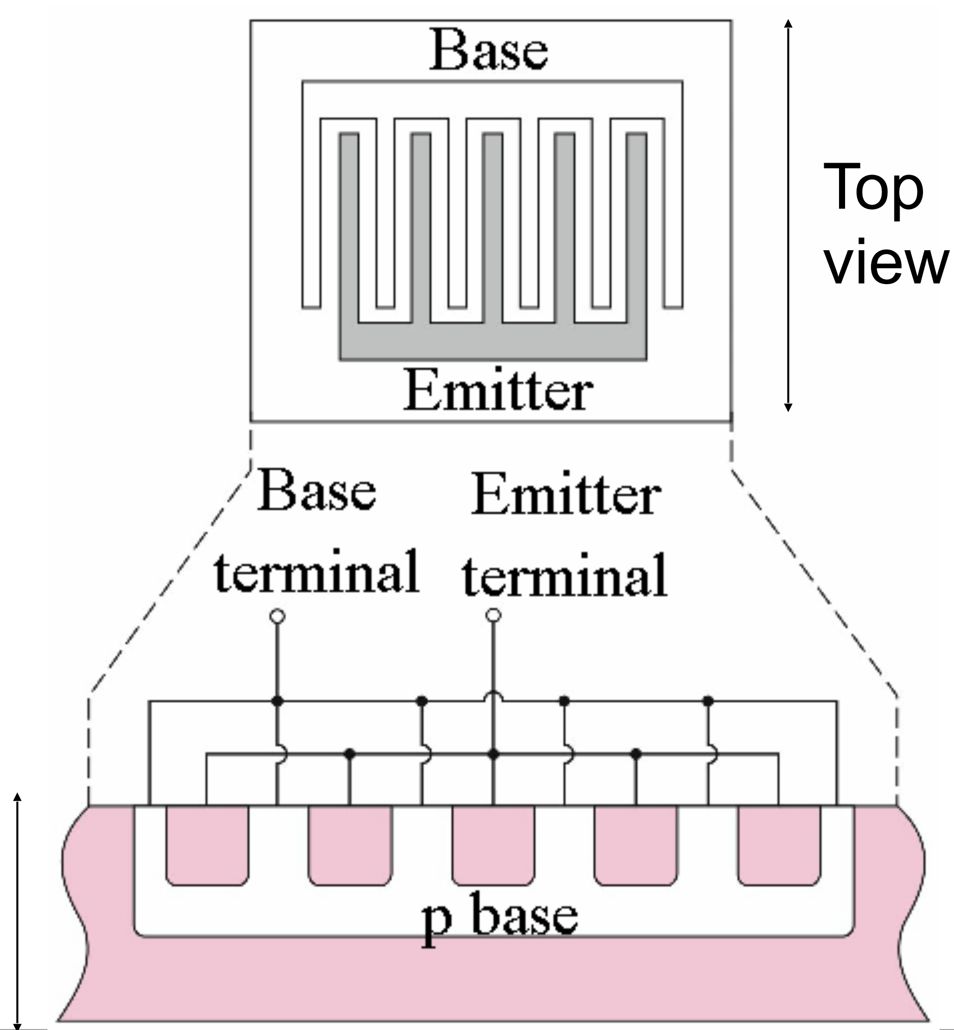
- Capability to deliver a high level of power to the load without loss of gain and maintaining a linear transfer function.
- Limit power dissipation, i.e., efficiently deliver power to the load.
- Capability to handle large voltage and current.

Power transistor-BJT

Power transistors are used to sustain the high output voltage and current.

Physical structure;

- Large emitter area to handle large current densities
- Narrow emitter width to minimize parasitic base resistance



Cross-sectional view

Power transistor-BJT

Large-area devices – the geometry and doping concentration are different from those of small-signal transistors

Examples of BJT rating:

Parameter	**Small-signal BJT (2N2222A)**	**Power BJT (2N3055)**	**Power BJT (2N6078)**
V_{CE} (max) (V)	40	60	250
I_C (max) (A)	0.8	15	7
P_D (max) (W)	1.2	115	45
β	35 – 100	5 – 20	12 – 70
f_T (MHz)	300	0.8	1

Transistor rating

Power transistors need to withstand high levels of voltage, current, and power. Hence, it is important to understand what determines transistors ratings.

A transistor is characterized by three limitations

- Maximum rated current
- Maximum rated voltage
- Maximum rated power.

These three limitations define a safe operating area (SOA) for a transistor

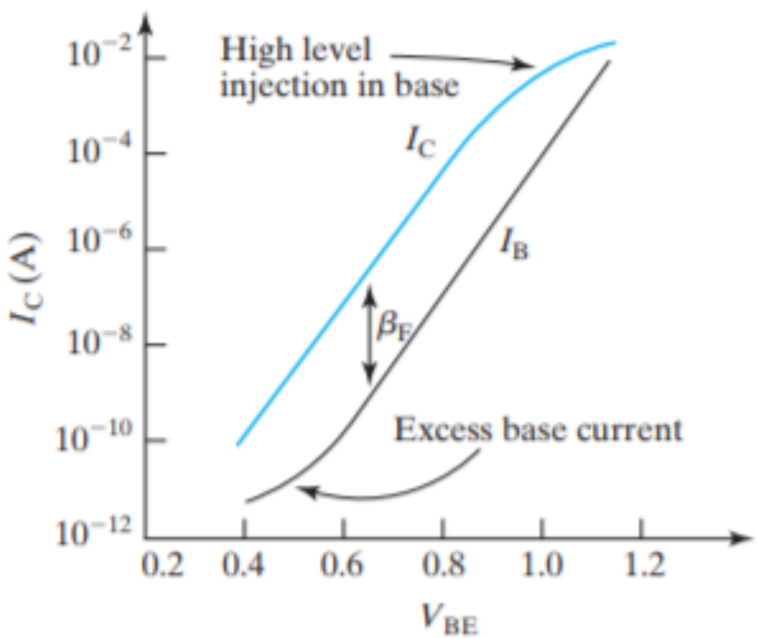
Current rating

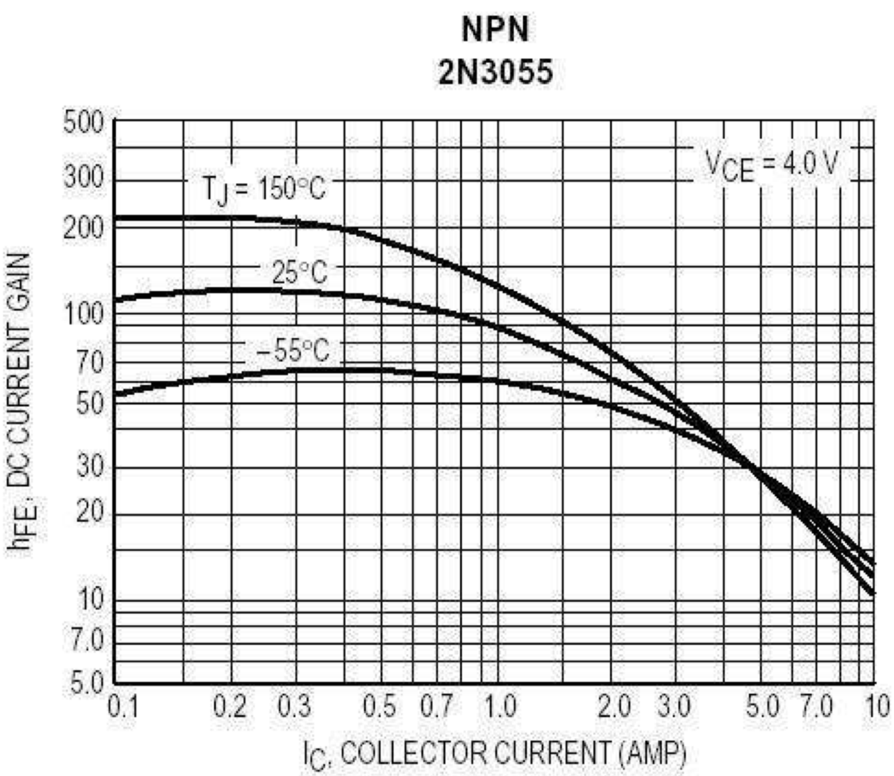
The maximum rated collector current, $I_{C(\mathrm{rated})}$ may be related to the following:

- maximum current that the wires connecting the semiconductor to the external terminals can handle
- current which leads to maximum power dissipation when the transistor is in active mode.
- the collector current at which the gain falls below a minimum specified value

Current rating

Current gain vs I_c





Voltage rating

- The maximum (output) voltage limitation is determined by the onset of breakdown.
- Breakdown is a deleterious effect that occurs in the presence of high electric field.
- Causes high resistance elements to allow flow of high current.
- Typically an irreversible effect permanently damaging the element.

Avalanche Breakdown

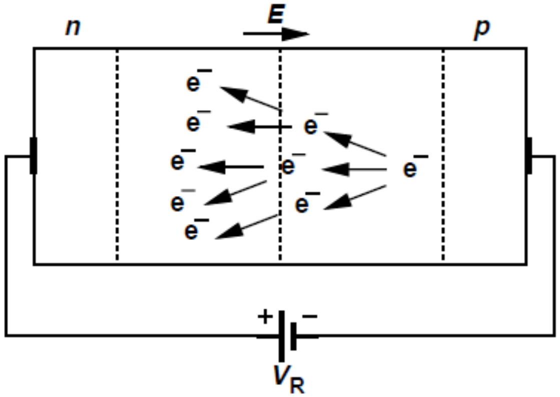
Two types of breakdown occur in BJTs

•Avalanche breakdown in the reverse-biased base-collector junction (involves gain and breakdown at the p-n junction)

•Second breakdown – non-uniformities in current density which increase temperature in localized regions of the semiconductor.

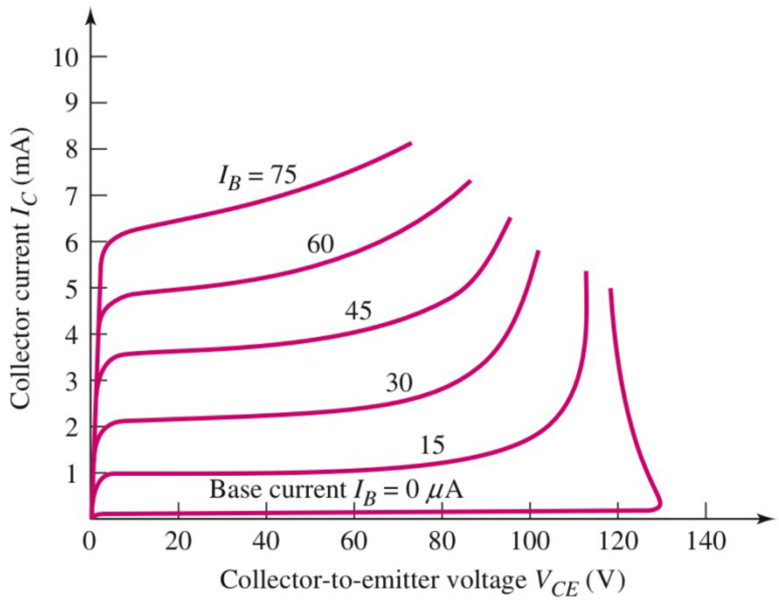
Avalanche Breakdown

- In <u>reverse biased junctions</u> a <u>wide</u> *depletion region* causes <u>high</u> <u>electric field</u> and <u>tremendous</u> *acceleration.*
- Very few electrons make it through depletion region with high velocity.
- These electrons collide with atoms in the depletion region and free more electrons (Process called *<u>Multiplication</u>*).
- <u>Results</u> in higher and higher current flow which cause permanent damage to the device.



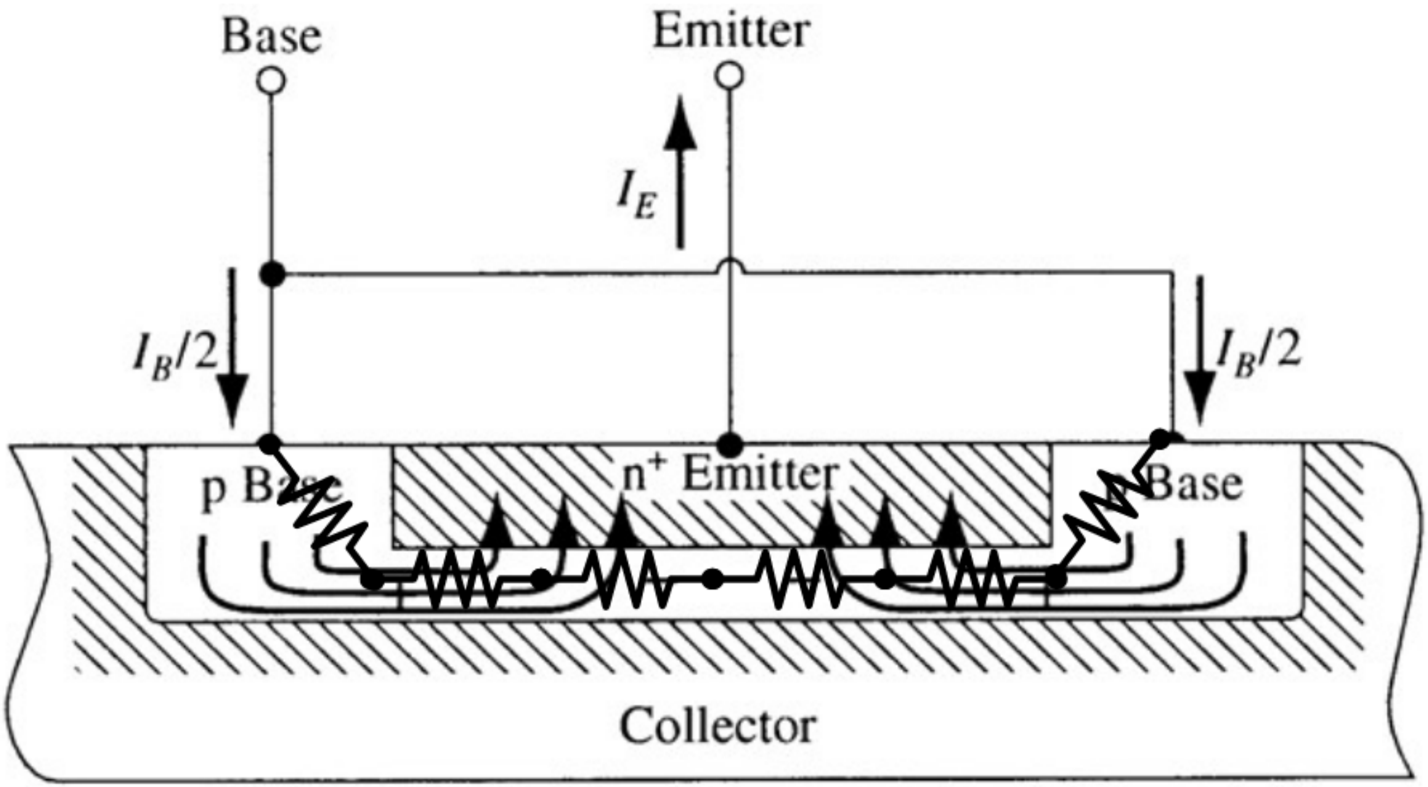
Avalanche (Primary) Breakdown

- In a BJT in forward active mode the B-C junction is reverse biased. In an npn, as the VCE increases, the voltage on the collector becomes significantly higher than the voltage on the base.
- A point is reached where avalanche occurs at the B-C junction.
- Thus the collector current dramatically increases.



- ✓ The breakdown voltage when the base terminal is open-circuited (I_B=0) is V_{CEO}, approx. 130V
- ✓ All the curves tend to merge to the same collector-emitter voltage, denoted as $V_{CE(sus)}$ once breakdown has occurred.
- ✓ $V_{CE(sus)}$ is the voltage necessary to sustain the transistor in breakdown.

Second-breakdown



Second-Breakdown occurs because current flow across the emitter–base junction is not uniform. Rather, the current density is greatest near the periphery of the junction (**current crowding**).

Second-Breakdown

- Locally dissipated power and hence temperature rise (at locations called **hot spots**).
- Since a temperature rise causes an increase in current, a localized form of **thermal runaway** can occur, leading to junction destruction.
- <u>Thermal Runaway</u>: Increase in temperature leads to higher current and power dissipation, which in turn increases the temperature further until the device is destroyed.

Dissipate power in a BJT

The average power dissipated in a BJT must be kept below a specified maximum value to ensure that the temperature of the device does not exceed the maximum allowable value.

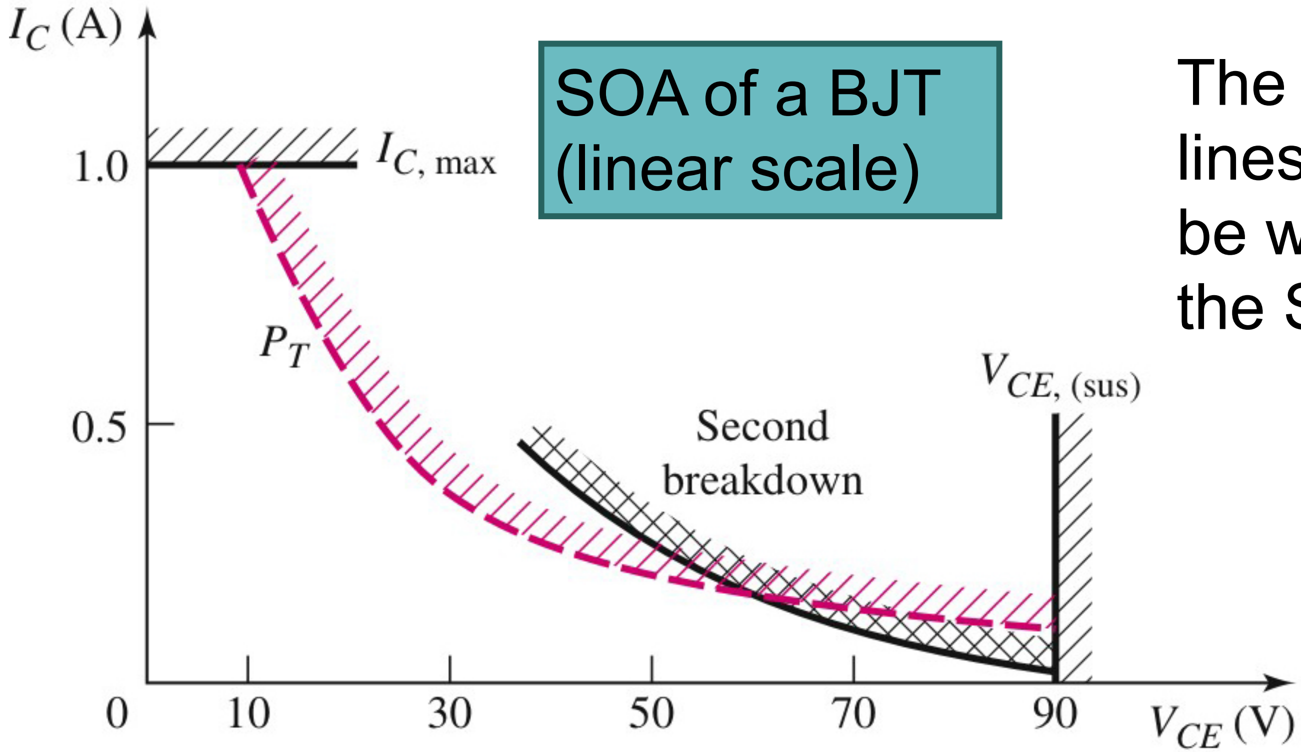
The maximum rated power, P_T

$$P_T = V_{CE} I_C$$

The power handling ability of a BJT is limited by two factors, i.e. the maximum junction temperature, T_{Jmax} that the BJT can be operated at and second-breakdown.

Safe operating area (SOA)

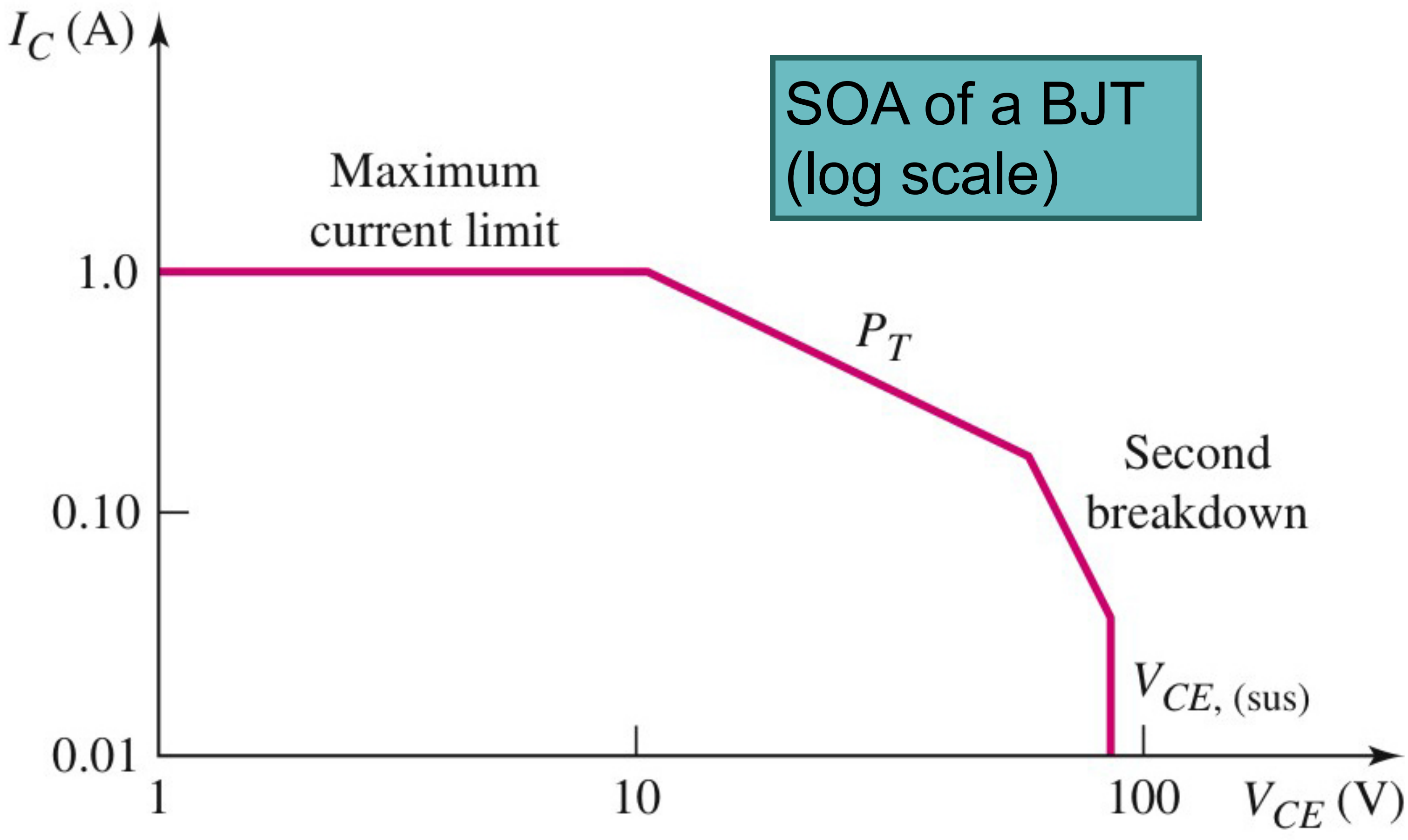
The safe operating area (SOA) is bounded by $I_{C(\max)}$; $V_{CE(sus)}$ and maximum rated power curve, P_T and the transistor's second breakdown characteristics curve.



SOA of a BJT (linear scale)

The load lines must be within the SOA

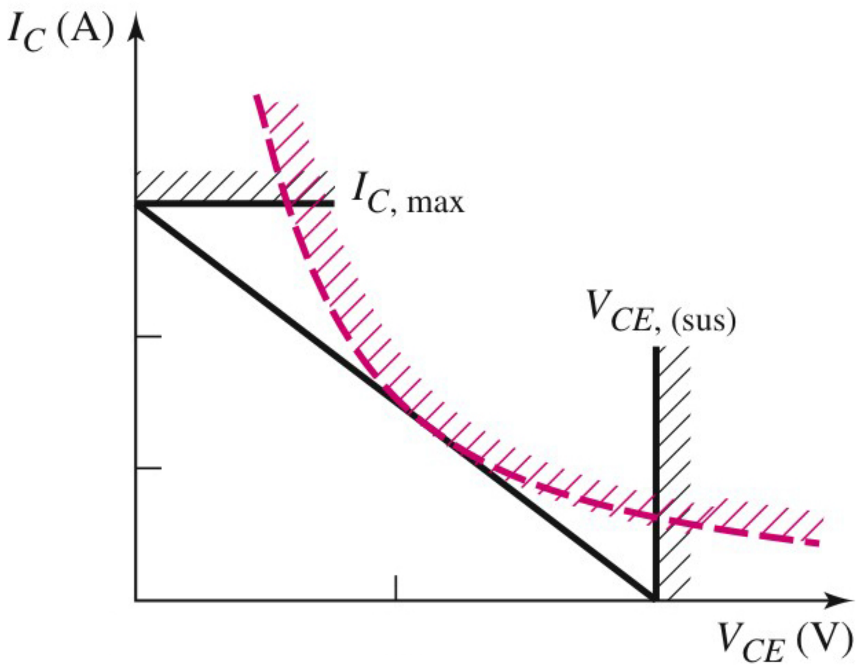
Safe operating area (SOA)

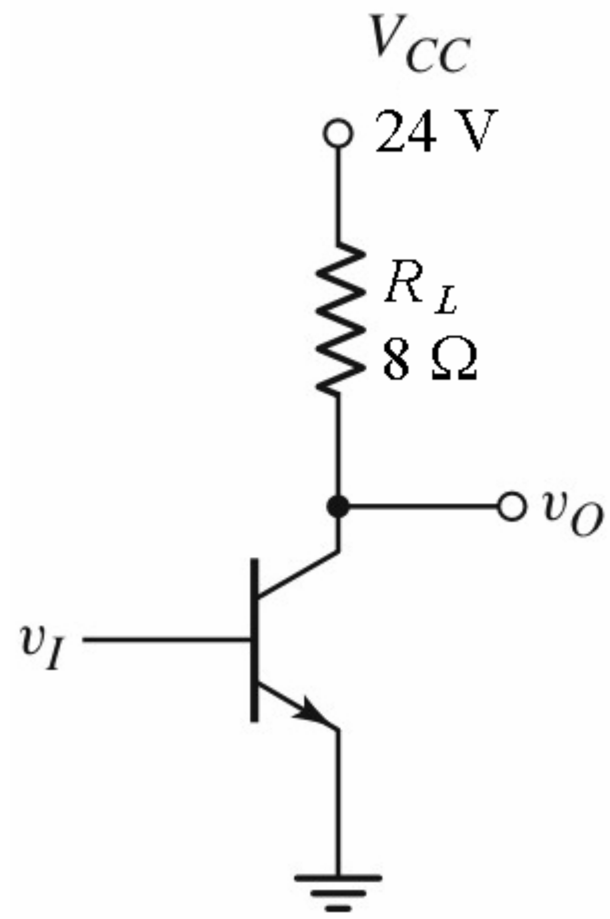


SOA of a BJT
(log scale)

In-class problem 1

Determine the required DC ratings (current, voltage and power) of the BJT.





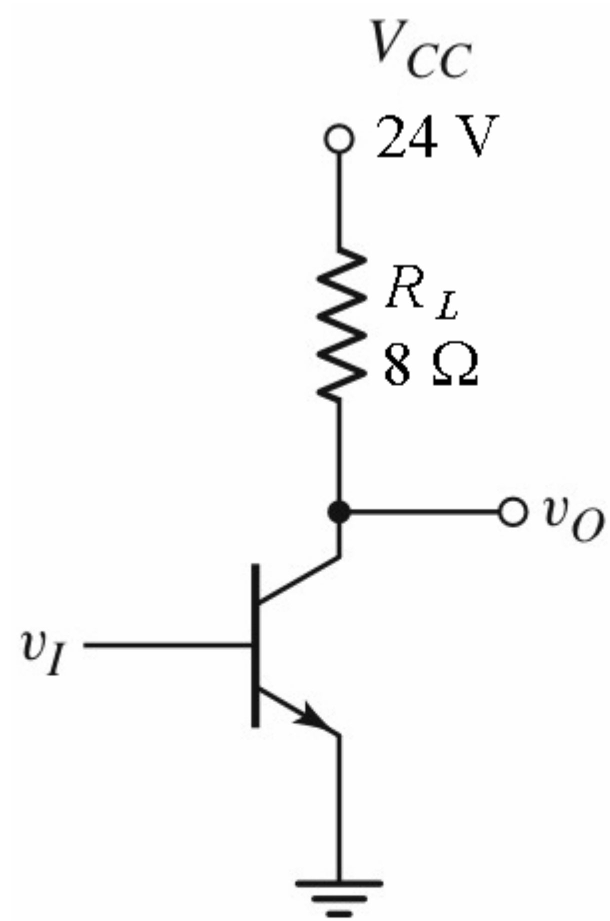
In-class problem 1, solution

For $V_{CE} \cong 0$ the maximum collector current;

$$I_{C(\max)} = \frac{V_{CC}}{R_L} = \frac{24}{8} = 3\ \text{A}$$

For $I_C = 0$ the maximum collector-emitter voltage;

$$V_{CE(\max)} = V_{CC} = 24\ \text{V}$$



In-class problem 1, solution

$$P_T = V_{CE} I_C = (V_{CC} - I_C R_L) I_C = V_{CC} I_C - I_C^2 R_L$$

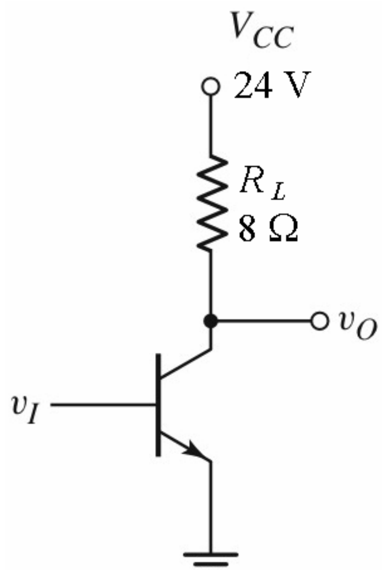
The maximum power occurs when $\dfrac{dP_T}{dI_C} = 0$

i.e. when $V_{CC} - 2I_C R_L = 0$ Differentiating

or when $I_C = 1.5\ \text{A}$

At this point; $V_{CE} = V_{CC} - I_C R_L = 12\ \text{V}$

and; $P_T = V_{CE} I_C = 18\ \text{W}$



In-class problem 1, solution

Thus the transistor ratings are;

$$I_{C(\max)} = 3\text{ A}$$

$$V_{CE(\max)} = 24\text{ V}$$

$$P_T = 18\text{ W}$$

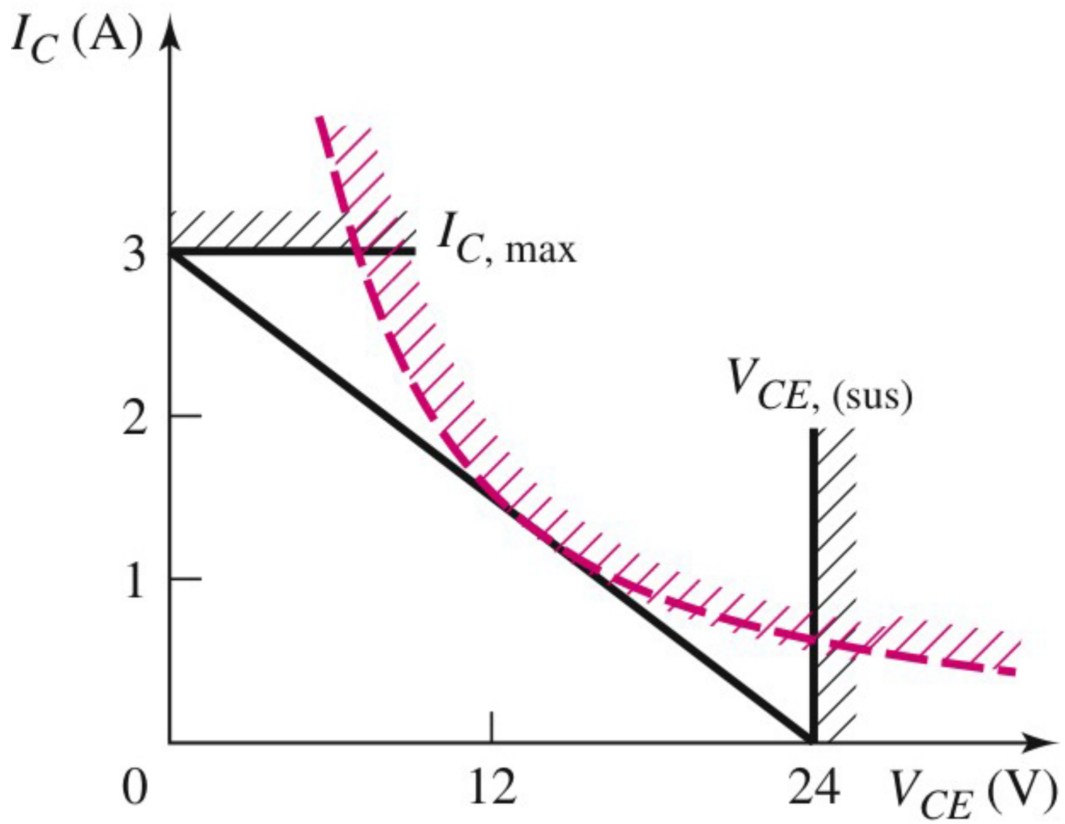
In practice, to find a suitable transistor for a given application, safety factors are normally used. A transistor with $I_{C(\max)} > 3\text{ A},\ V_{CE(\max)} > 24\text{ V},\ P_T > 18\text{ W}$ will be required.

In-class problem 1, solution

The load line equation is;

$$V_{CE} = V_{CC} - I_C R_L$$

The load line must be within the SOA



Take-home problem 1

The common-emitter circuit in Figure P8.2 is biased at $V_{CC} = 24$ V. The maximum transistor power is rated at $P_{Q,\max} = 25$ W. The other parameters of the transistor are $\beta = 60$ and $V_{BE}(\text{on}) = 0.7$ V. (a) Determine R_L and R_B such that the transistor is biased at the maximum power point. (b) For $V_p = 12$ mV, determine the average power dissipated in the transistor.

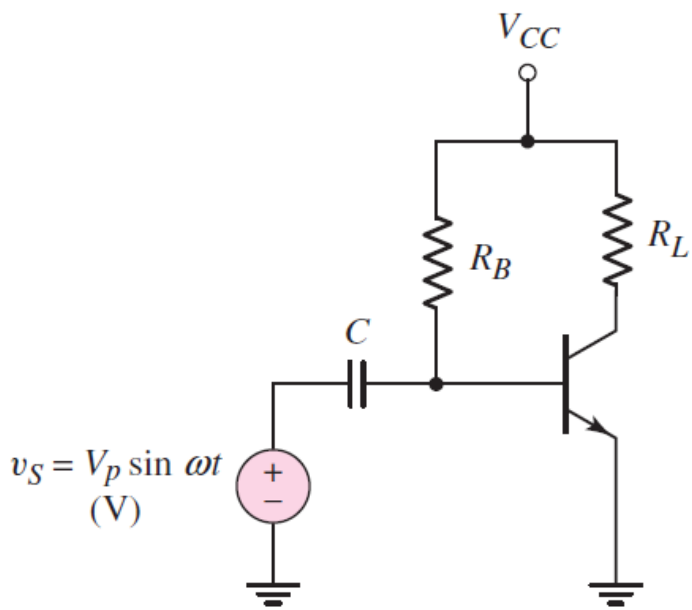


Figure P8.2

Take-home problem 1, solution

8.2

(a) $P_{Q,\max} = V_{CEQ} \cdot I_{CQ}$

$$25 = \left(\frac{24}{2}\right) \cdot I_{CQ} \Rightarrow I_{CQ} = 2.083 \text{ A}$$

$$R_L = \frac{24-12}{2.083} = 5.76\,\Omega$$

$$I_{BQ} = \frac{2.083}{60} = 0.03472 \text{ A}$$

$$R_B = \frac{24-0.7}{0.03472} = 671\,\Omega$$

(b) $r_\pi = \dfrac{\beta V_T}{I_{CQ}} = \dfrac{(60)(0.026)}{2.083} = 0.7489\,\Omega$

$$I_b = \frac{V_p}{r_\pi} = \frac{12\,mV}{0.7489} = 16.02 \text{ mA}$$

$$I_c = \beta I_b = (60)(0.01602) = 0.9614 \text{ A}$$

$$\overline{P}_{avg} = \frac{1}{2} I_c^2 R_C = \frac{1}{2}(0.9614)^2(5.76) = 2.66 \text{ W}$$

For the transistor,

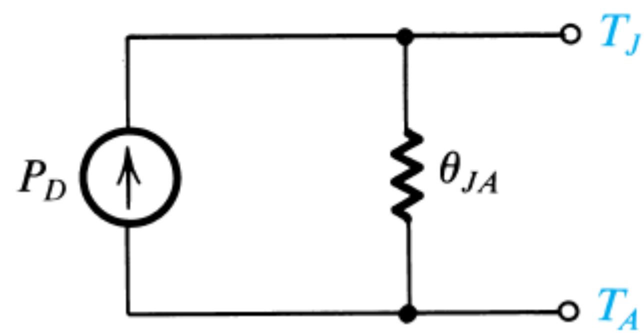
$$P_Q = 25 - 2.66 = 22.34 \text{ W}$$

Heat Flow From Device to Ambient

Power transistors dissipate large amounts of power.
The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature T_J must not be allowed to exceed a specified maximum, $T_{J\max}$; otherwise the transistor could suffer permanent damage.

In a steady state in which the transistor is dissipating P_D watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

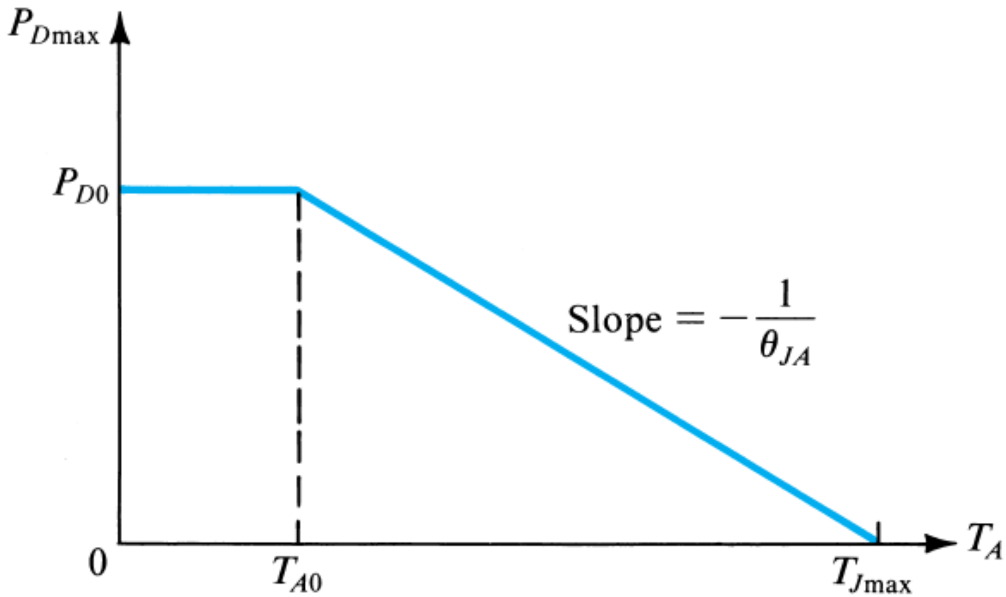
$$T_J - T_A = \theta_{JA} P_D$$



θ_{jA}: Thermal resistance between the junction and the ambient.

Power Derating Curve

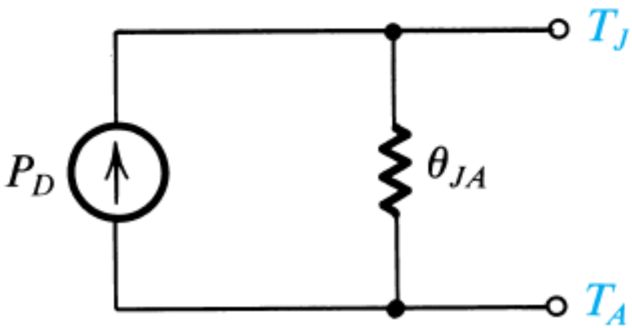
Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a "power-derating" curve.



$$P_{D,\max} = \frac{T_{j,\max} - T_A}{\theta_{jA}}$$

$$T_J - T_A = \theta_{JA} P_D$$

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}}$$



A low thermal resistance is desired to efficiently remove heat from the junction, thereby increasing the power rating of the transistor

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$
$$T_J - T_A = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

θ_{jA}: Thermal resistance between the junction and the ambient.
θ_{jC} :Thermal resistance between the junction and the case.
θ_{CS} : Thermal resistance between the case and the heat sink.
θ_{SA} : Thermal resistance between the heat sink and the ambient.

Heat Sinks

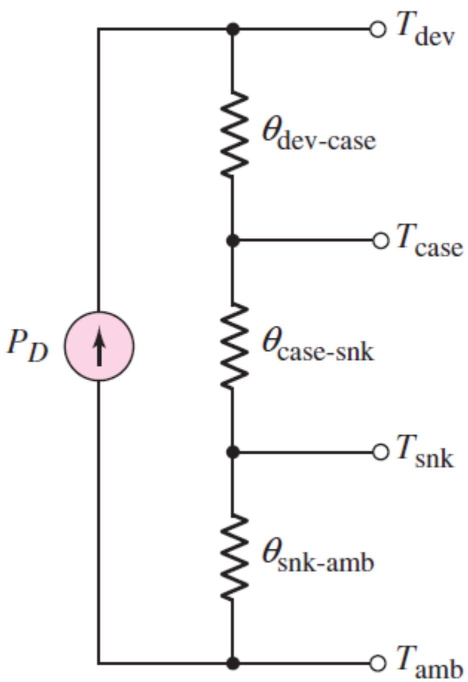


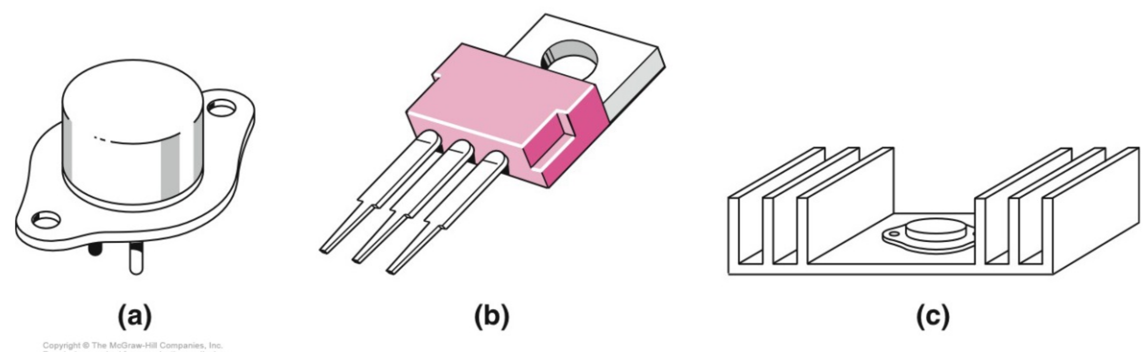
Figure 8.11 Electrical equivalent circuit for heat flow from the device to the ambient

Without heat sink

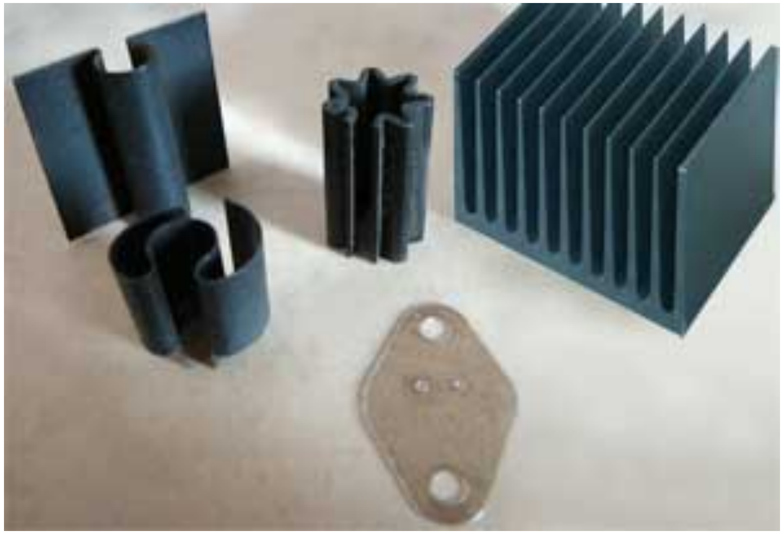
$$T_{\text{dev}} - T_{\text{amb}} = P_D(\theta_{\text{dev-case}} + \theta_{\text{case-amb}})$$

With heat sink

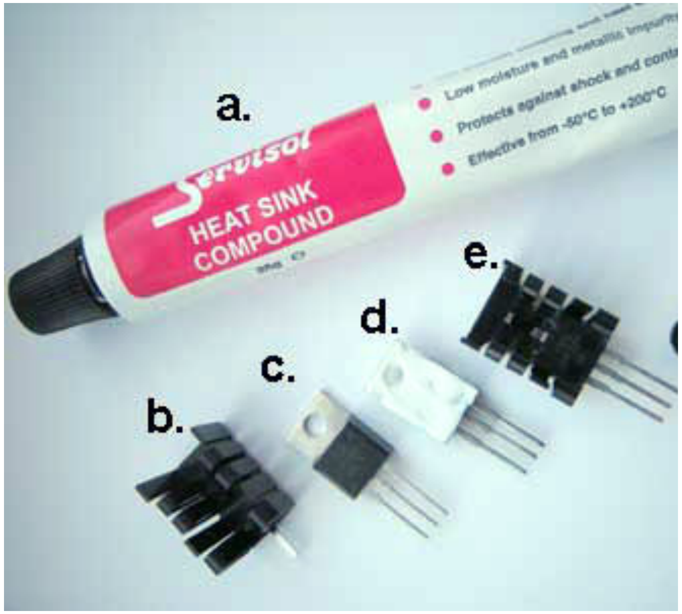
$$T_{\text{dev}} - T_{\text{amb}} = P_D(\theta_{\text{dev-case}} + \theta_{\text{case-snk}} + \theta_{\text{snk-amb}})$$



Heat Sinks



Examples of heat sinks



(a) Tube of heat-sink compound.
(b) Heat-sink.
(c) TIP31 transistor.
(d) shows the transistor smeared with heat-sink compound.
(e) shows the transistor fitted to the heat-sink.

In-class problem 2

A BJT is specified to have $T_{J\max} = 150°C$ and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_C = 25°C$$
$$2 \text{ W at } T_A = 25°C$$

Above 25°C, the maximum power dissipation is to be derated linearly with $\theta_{JC} = 3.12°C/W$ and $\theta_{JA} = 62.5°C/W$. Find the following:

(a) The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A = 50°C$.
(b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which $\theta_{CS} = 0.5°C/W$ and $\theta_{SA} = 4°C/W$. Find the temperature of the case and of the heat sink.
(c) The maximum power that can be dissipated safely if an *infinite heat sink* is used and $T_A = 50°C$.

In-class problem 2, solution

(a)

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

(b) With a heat sink, θ_{JA} becomes

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$
$$= 3.12 + 0.5 + 4 = 7.62°\text{C/W}$$

Thus,

$$P_{D\max} = \frac{150 - 50}{7.62} = 13.1 \text{ W}$$

Figure 11.28 shows the thermal equivalent circuit with the various temperatures indicated.

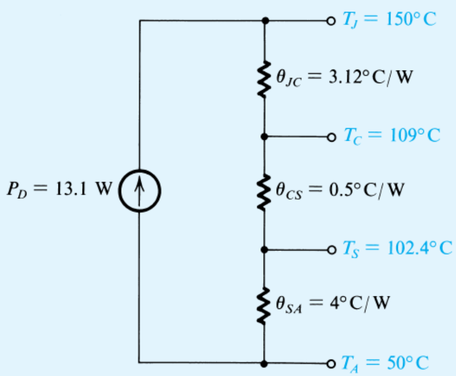


Figure 11.28 Thermal equivalent circuit for Example 11.8.

(c) An infinite heat sink, if it existed, would cause the case temperature T_C to equal the ambient temperature T_A. The infinite heat sink has $\theta_{CA} = 0$. Obviously, one cannot buy an infinite heat sink; nevertheless, this terminology is used by some manufacturers to describe the power-derating curve of Fig. 11.27. The abscissa is then labeled T_A and the curve is called "power dissipation versus ambient temperature with an infinite heat sink." For our example, with infinite heat sink,

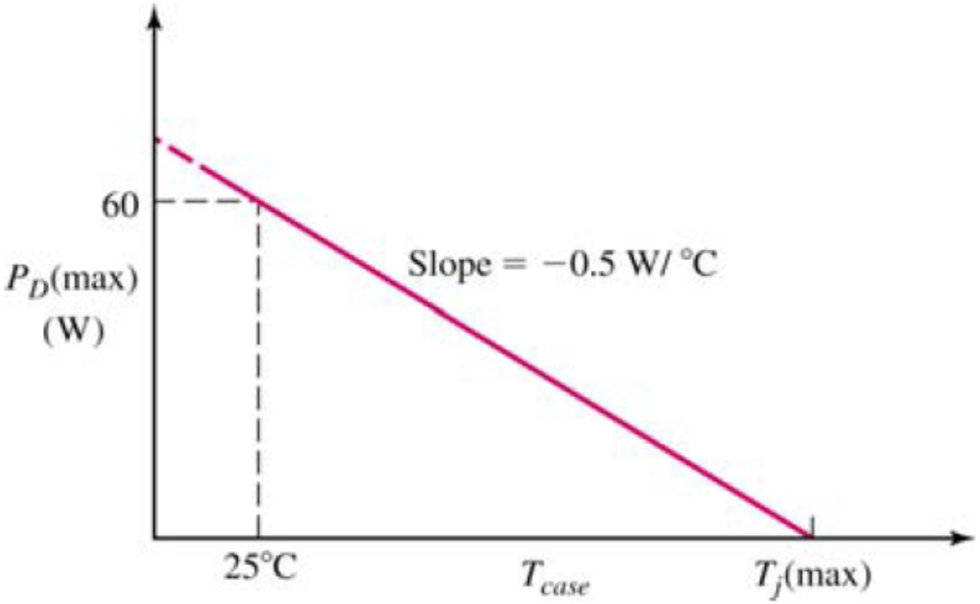
$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC}} = \frac{150 - 50}{3.12} = 32 \text{ W}$$

Take-home problem 2

A particular transistor is rated for a maximum power dissipation of 60 W if the case temperature is at 25 °C. Above 25 °C, the allowed power dissipation is reduced by 0.5W/°C. (a) Sketch the power derating curve. (b) What is the maximum allowed junction temperature? (c) What is the value of $\theta_{dev-case}$?

Take-home problem 2, solution

(a)



(b) $$P_D = P_{D,\max} - (Slope)(T_j - 25)$$

$$\text{At } P_D = 0,\ T_{j,\max} = \frac{60}{0.5} + 25 \Rightarrow \underline{T_{j,\max} = 145°C}$$

(c) $$P_{D,\max} = \frac{T_{j,\max} - T_{case}}{\theta_{dev-amb}} \quad \text{or} \quad \theta_{dev-amb} = \frac{145-25}{60} \Rightarrow \underline{\theta_{dev-amb} = 2°C/W}$$