ECE 322L
Electronics 2

02/13/20 - Lecture 8

IC MOSFET Amplifiers

Updates and Overview

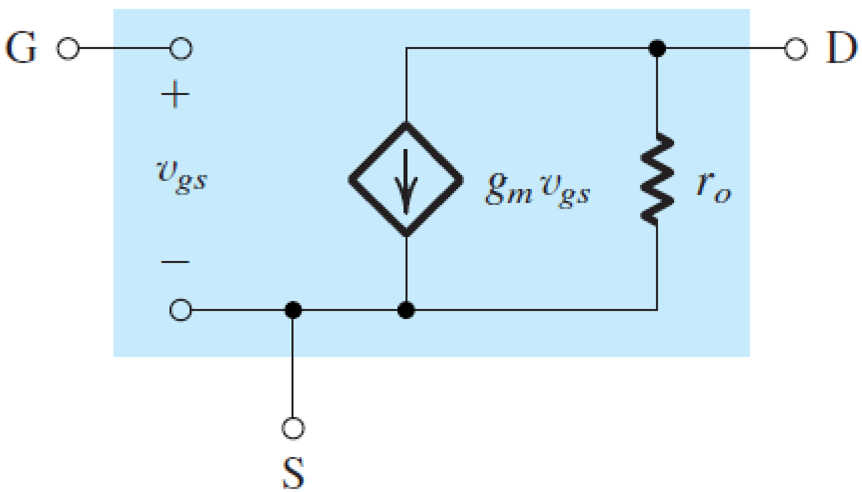
- Midterm 1 on Tue, Feb 18^{th}
- Homework 3 and Lab 4 are online
- Comparison of the three basic amplifier configurations (Neamen 4.6, S&S 5.6.7)
- Single-stage IC MOSFET amplifiers

  Amplifiers with enhancement load

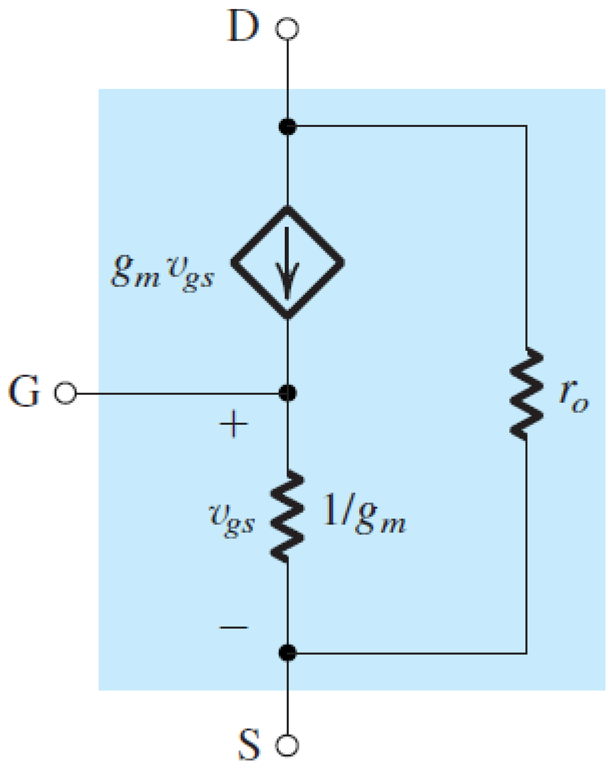
  (Neamen 4.7.1-4.7.2)

Small-signal equivalent circuits

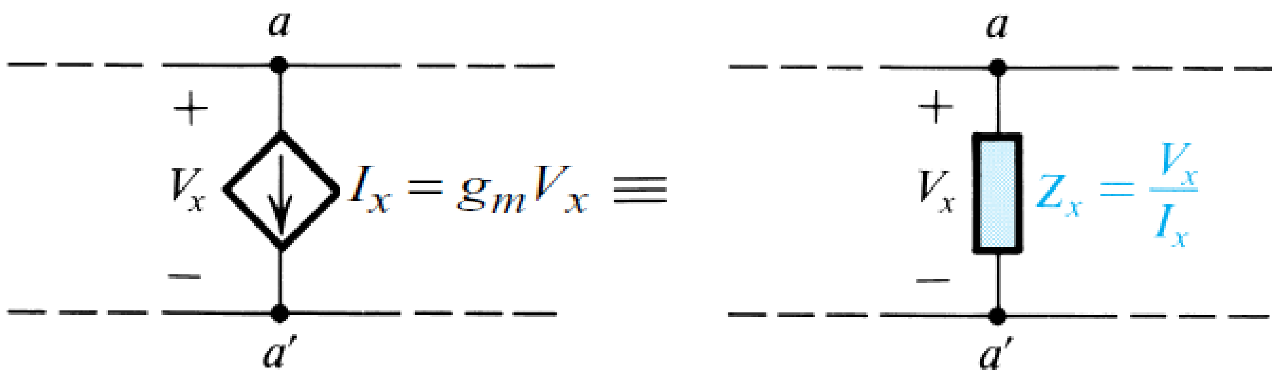
Π model



T model



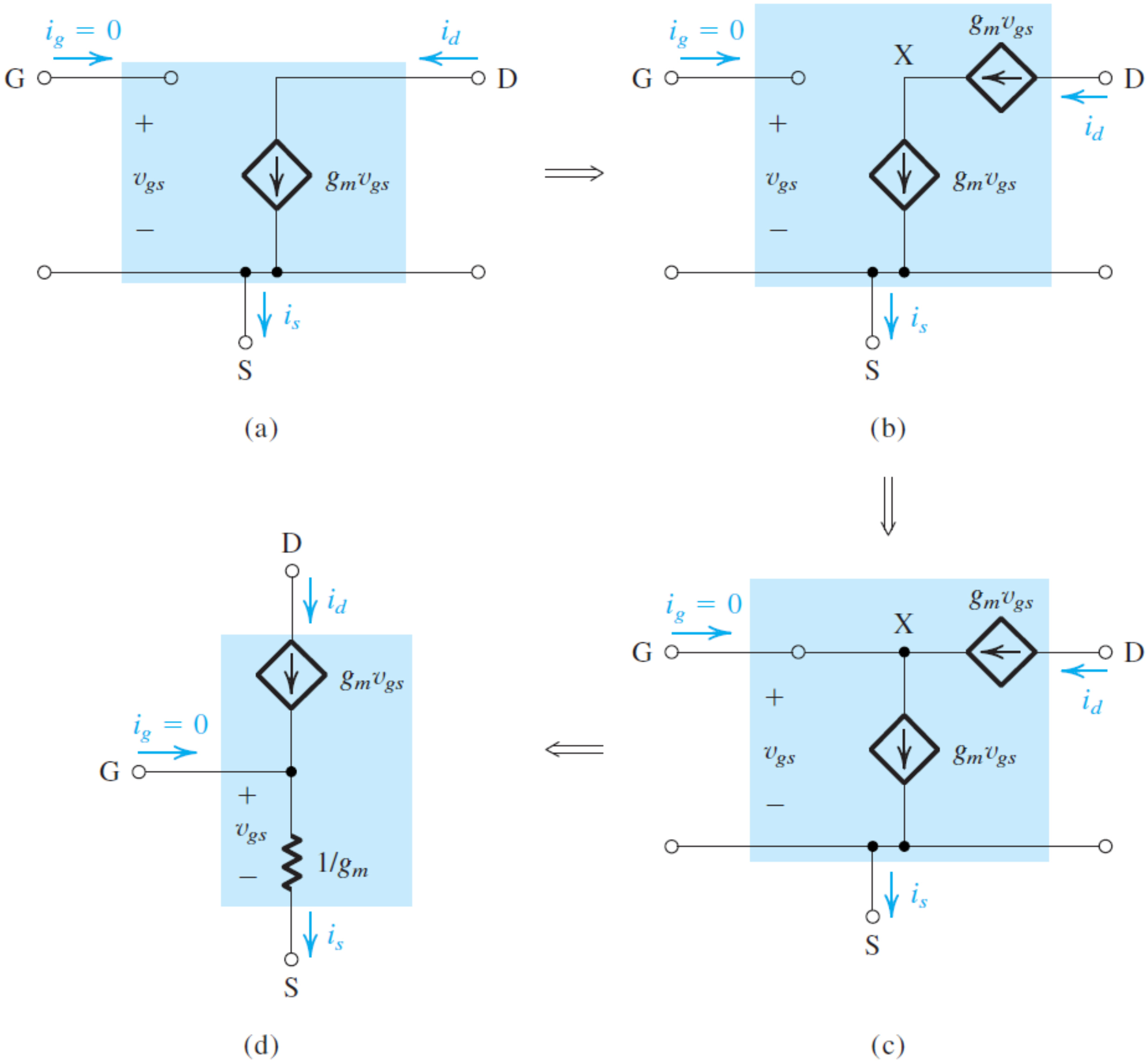
Source-absorption theorem



The current **source-absorption theorem** establishes that if, in one branch of the circuit with a voltage Vx, there is a dependent current **source** controlled by Vx, the **source** can be replaced by a simple impedance with value equal to the 1/**source controlling factor**.

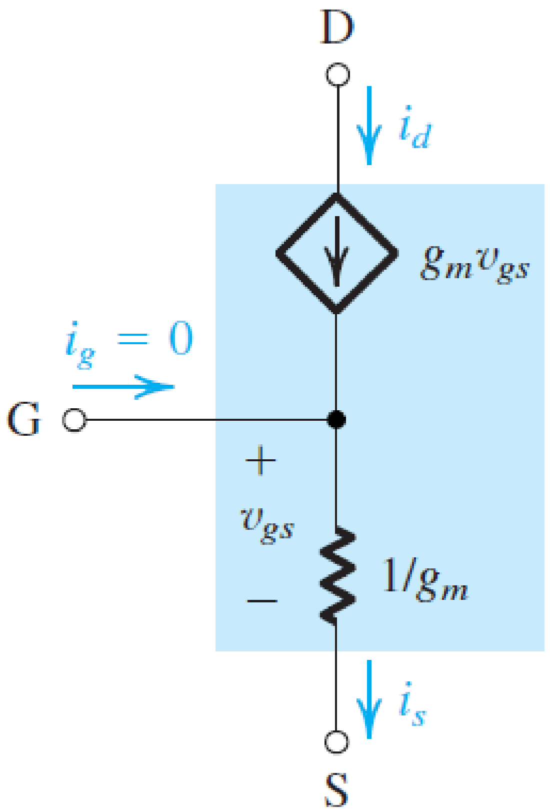
(S&S Appendix D)

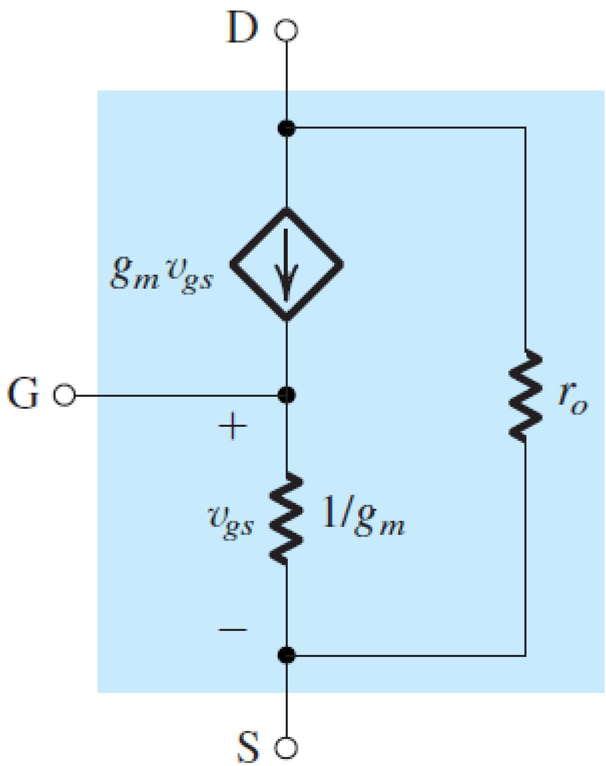
Conversion from a Π to a T model



λ=0

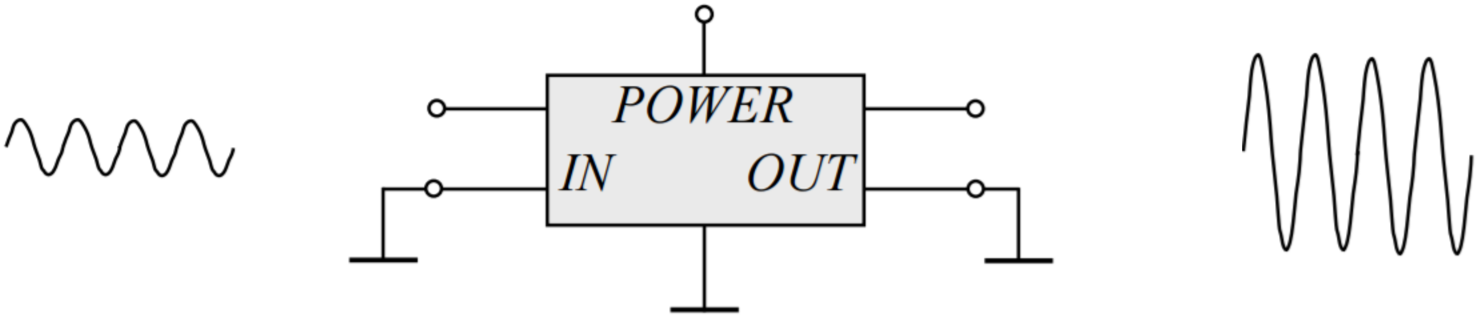
T model

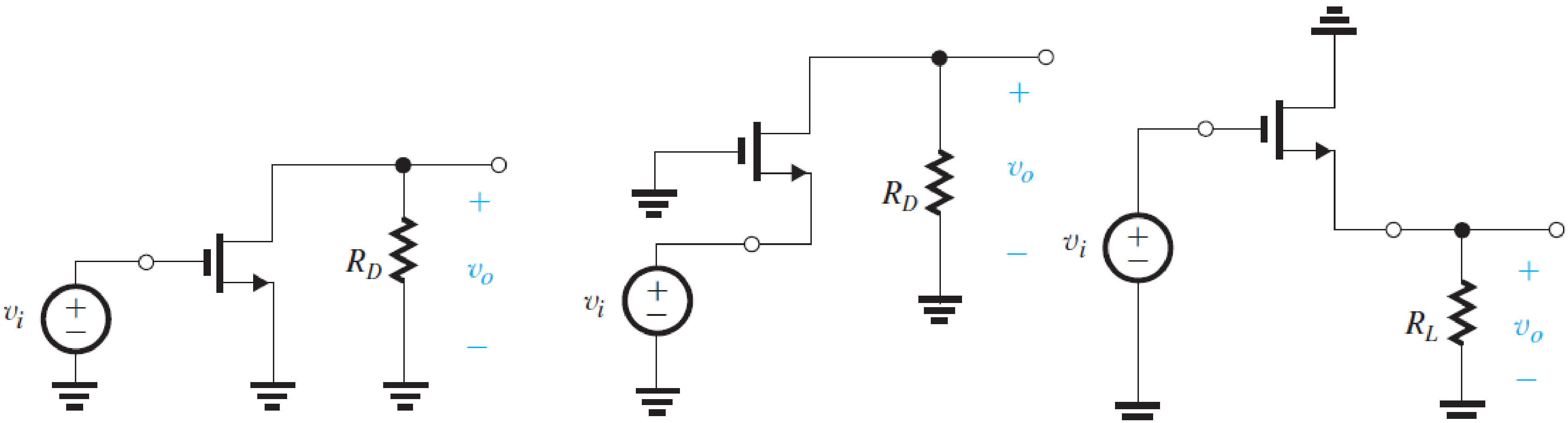




$\lambda=0$ $\lambda\neq0$

Basic Configurations for FET Amplifiers





(a) Common Source (CS) (b) Common Gate (CG) (c) Common Drain (CD)

There are three basic configurations for connecting the MOSFET as an amplifier. Each of these configurations is obtained by connecting one of the three MOSFET terminals to ground, thus creating a two-port network with the grounded terminal being *common* to the input and output ports.

Comparison of Amplifier Topologies

Common Source

- **Large $A_v < 0$**
  - degraded by R_S
- **Large R_{in}**
  - determined by biasing circuitry
- **$R_o \cong R_D$ (Moderate)**
- **r_o decreases A_v & R_o**
  but impedance seen looking into the drain can be "boosted" by source degeneration

Common Gate

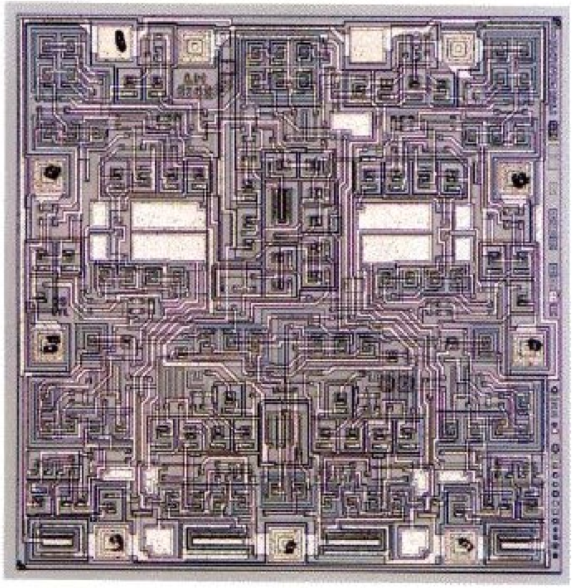
- **Large $A_v > 0$**
  -degraded by R_S
- **$0 < A_i \leq 1$**
- **Small R_{in}**
  - 1/gm
- **$R_o \cong R_D$ (Moderate)**
- **r_o decreases A_v & R_o**
  but the impedance seen looking into the drain can be "boosted" by source degeneration

Common Drain*

- **$0 < A_v \leq 1$**
- **Large R_{in}**
  - determined by biasing circuitry
- **R_o=1/gm**
  - decreased by R_S
- **r_o decreases A_v & R_o**

*** Also known as source follower**

MOSFET Amplifiers as Integrated Circuits

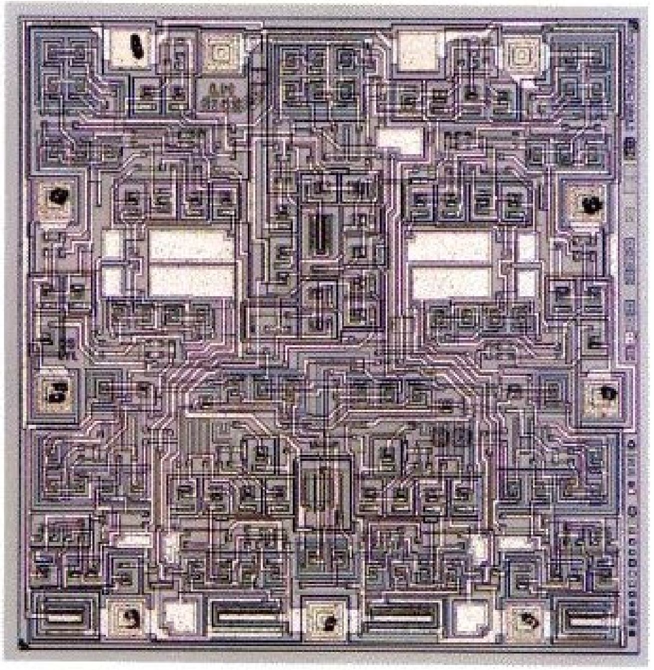


Benefit-The amplifier circuit can be quite **complex**, yet still **small and inexpensive**.

Challenge-**Bias** solutions are **more complex** for two reasons:

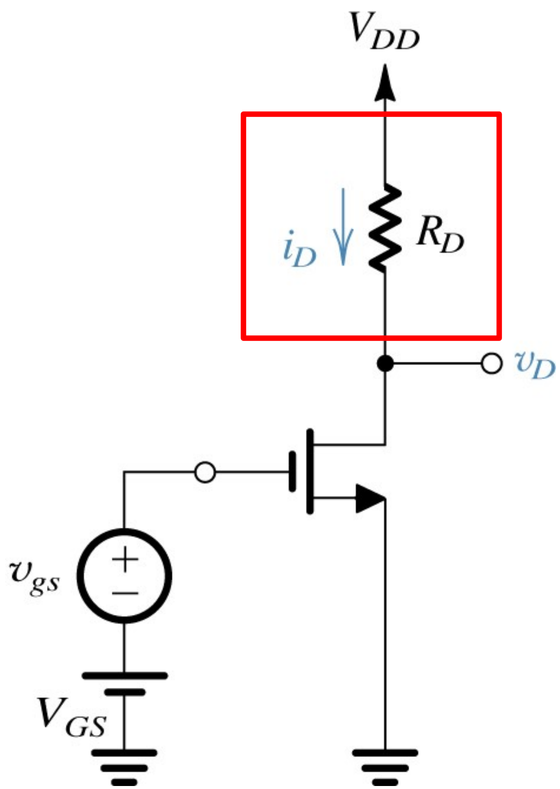
- DC blocking capacitors are not used in IC as **large capacitors (C>50-100 pF)** take **too much space.**
- Simple resistor biasing cannot be implemented in IC **as large resistors (R>1-10kΩ)** would take **too much space**. In addition there is a poor control on absolute values of the resistance **(~20% tolerance).**

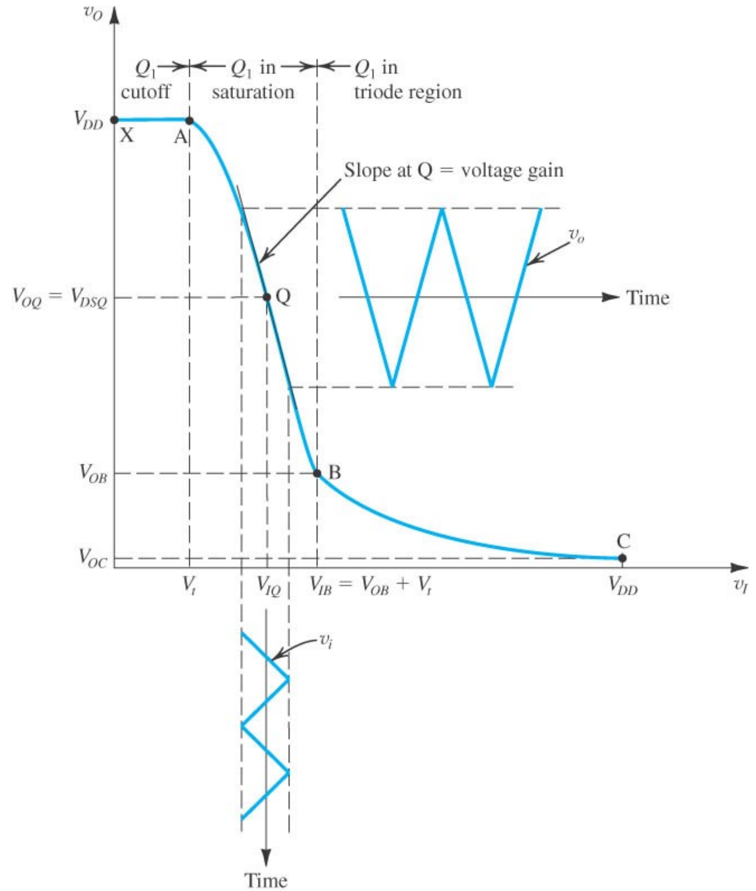
MOSFET Amplifiers as Integrated Circuits



When possible, every component that we saw in a discrete amplifier needs to be transposed into the IC version of it, i.e., something that takes up little space, can be fabricated with relatively low tolerance and follows similar processing steps than a transistor.

Discrete MOSFET Amplifier





(c)

Resistors take up far too much **space** on integrated circuit substrates.

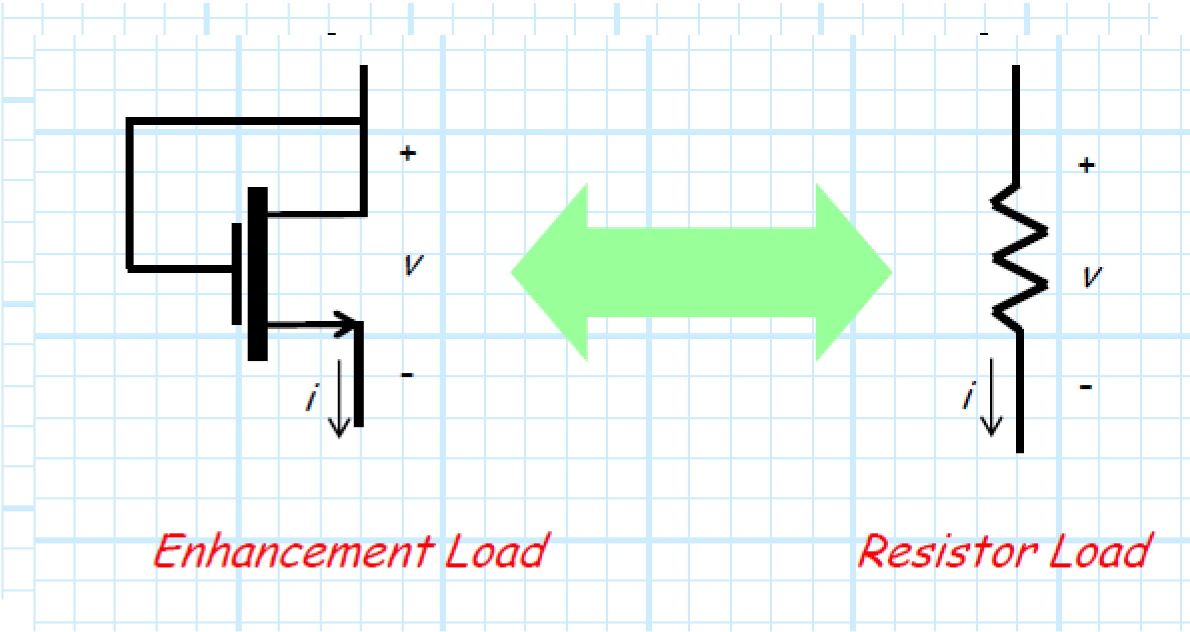
Q: How do we solve this problem??

A: We make a **resistor** out of a **transistor**!

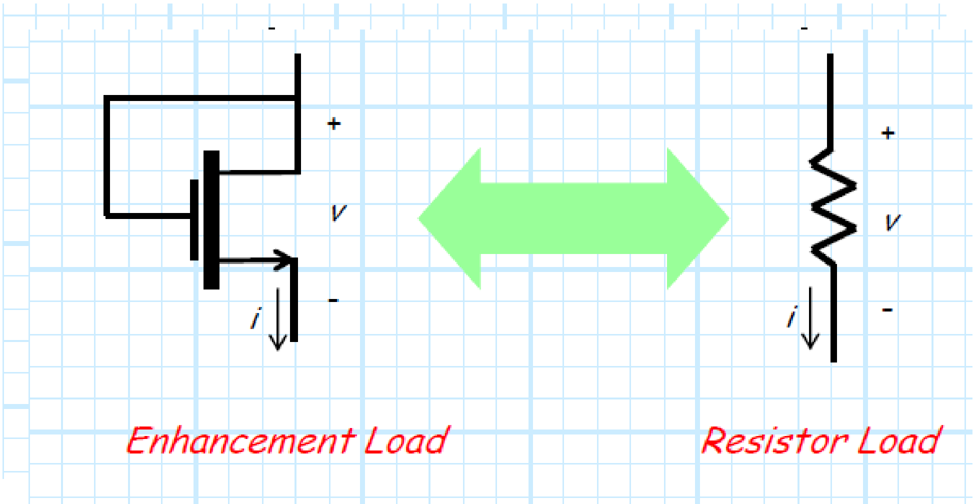
The Concept of Enhancement Load

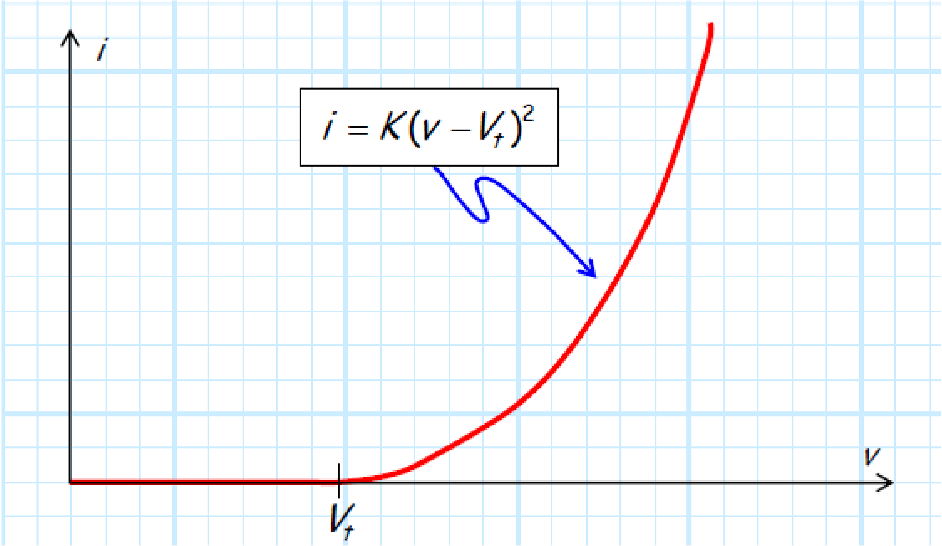
Resistors take up far too much **space** on integrated circuit substrates.
Q: How do we solve this problem??
A: We make a **resistor** out of a **transistor**!

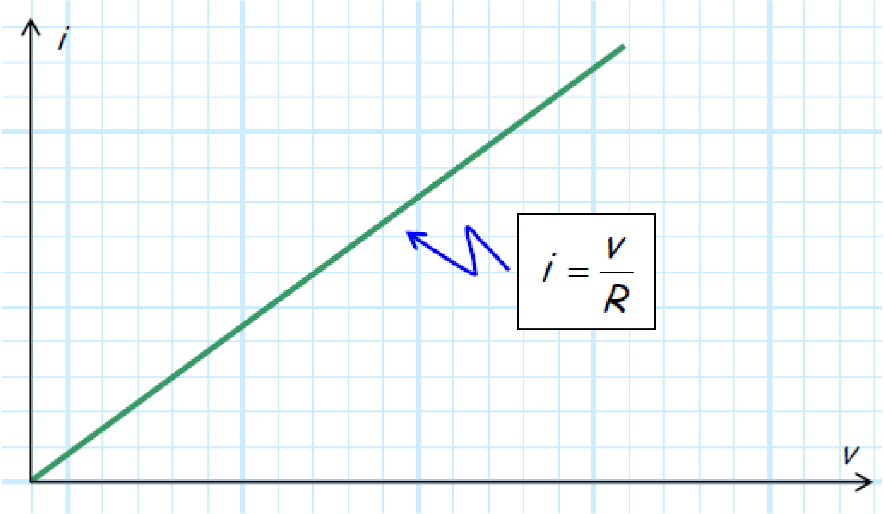
Q:How can we do that!? A resistor is a **two-**terminals device, whereas a transistor is a **three-**terminals device.
A: We can make a two-terminal device from a MOSFET by **connecting** the gate and the drain!



Enhancement Load and Resistor



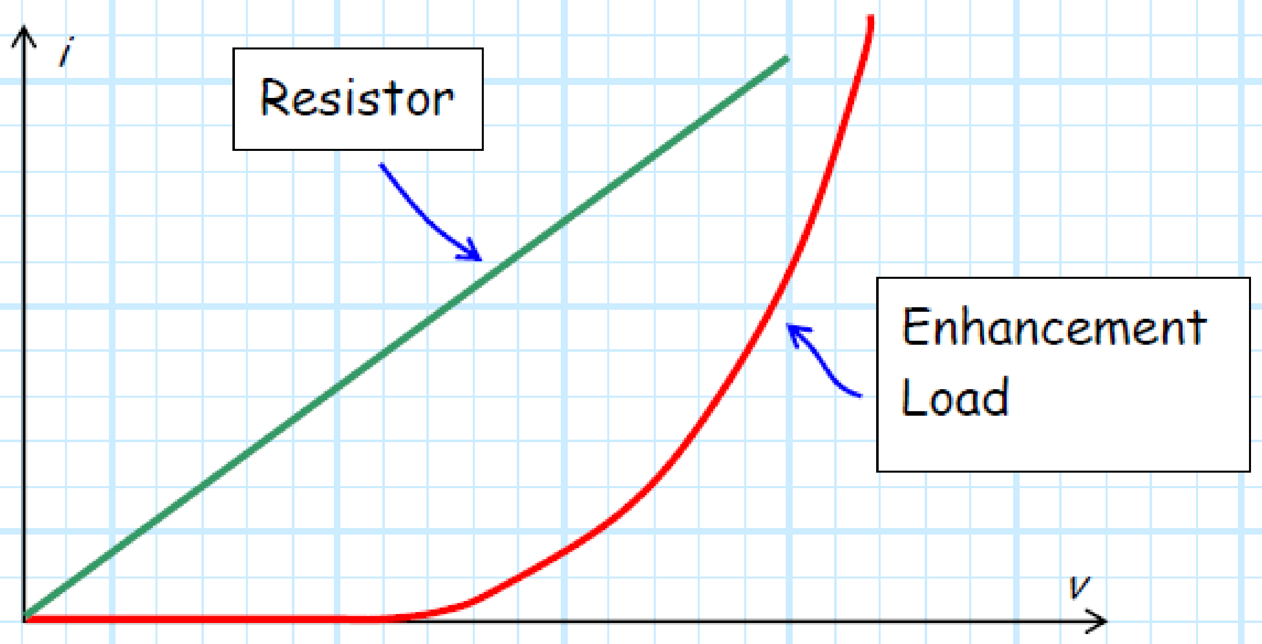




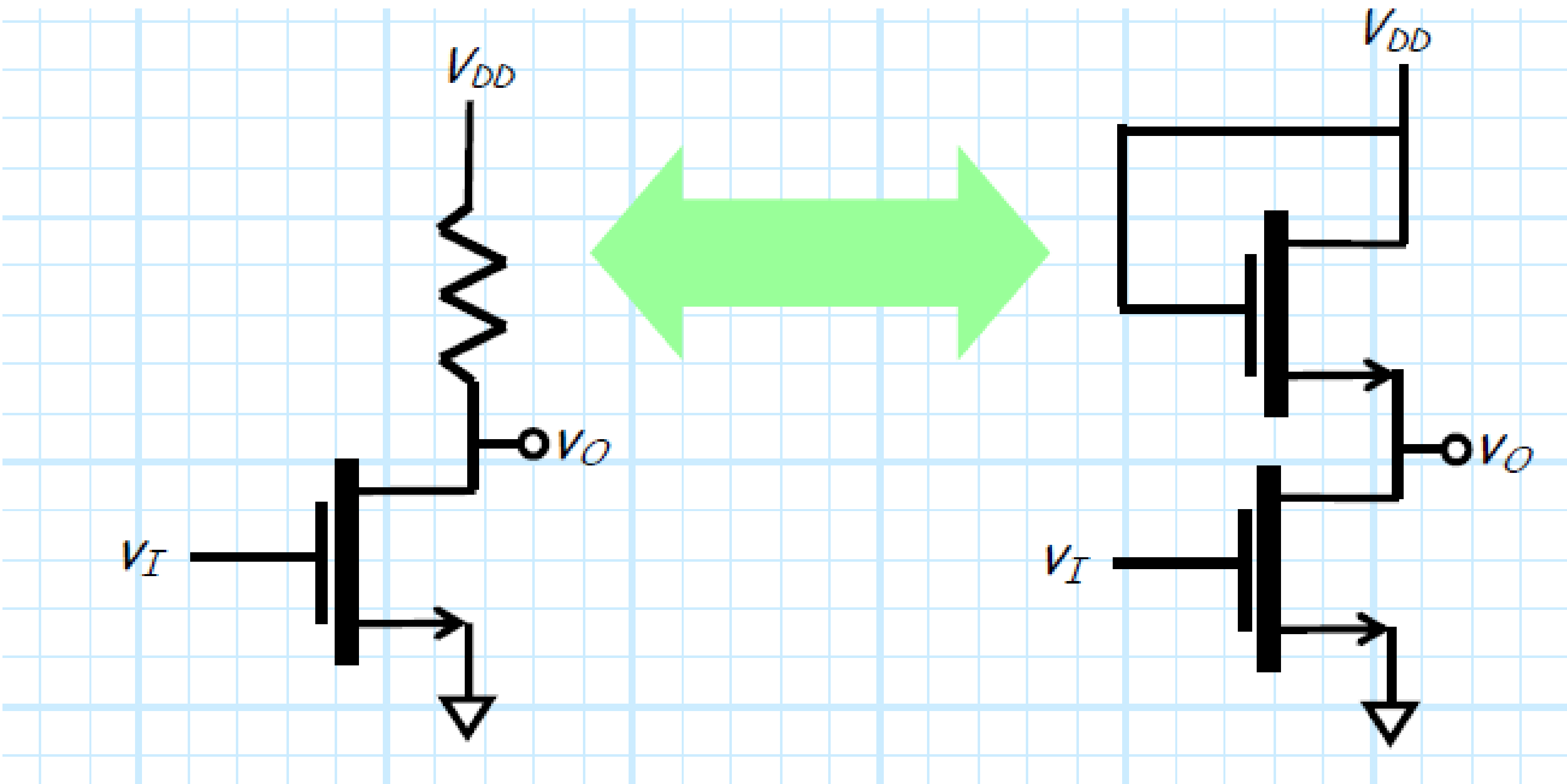
Enhancement Load and Resistor

1) They **both** have $i = 0$ when $v = 0$.

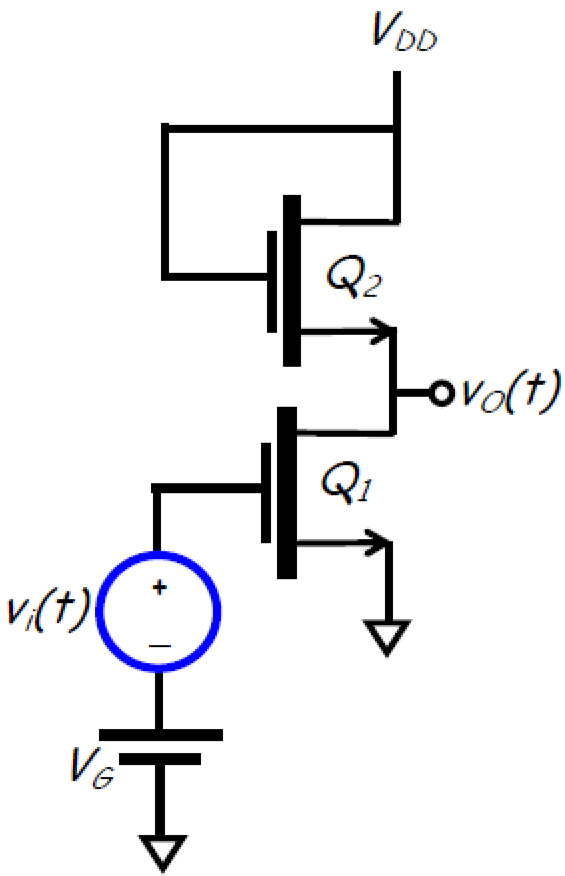
2) They **both** have increasing current i with increasing voltage v.



MOSFET Amplifier with Enhancement Load

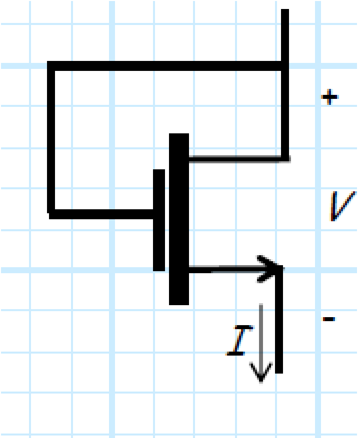


NMOS Amplifier with Enhancement Load



- We need to perform DC analysis (Determine the Q point)
- We need to perform small-signal analysis (Determine input resistance, output resistance, and gain)

DC model of an Enhancement Load



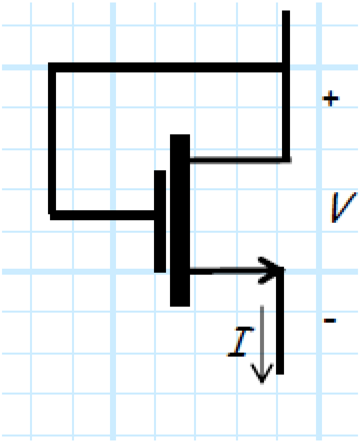
Since the gate is tied to the drain, we find $v_G = v_D$, and thus $v_{GS} = v_{DS}$. As a result, we find that $v_{DS} > v_{GS} - V_t$ **always**.

Therefore, we find that if $v_{GS} > V_t$, the MOSFET will be in **saturation** ($i_D = K(v_{GS} - V_t)^2$), whereas if $v_{GS} < V_t$, the MOSFET is in **cutoff** ($i_D = 0$).

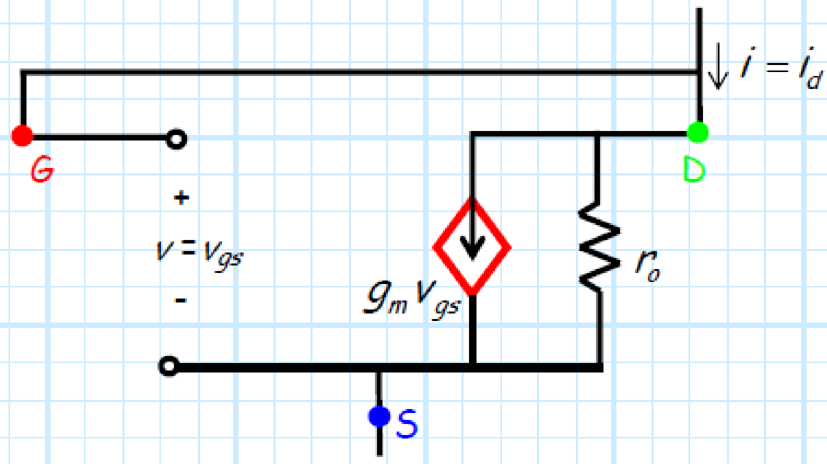
Since for enhancement load $i = i_D$ and $v = v_{GS}$, we can describe the enhancement load as:

$$i = \begin{cases} 0 & \text{for } v < V_t \\ K(v - V_t)^2 & \text{for } v > V_t \end{cases}$$

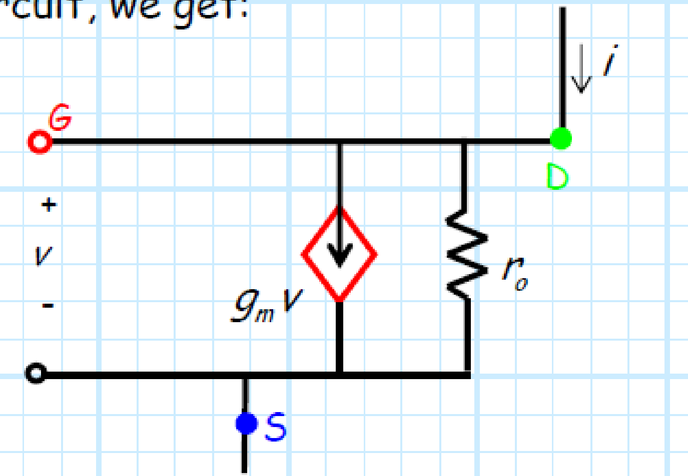
Small-signal Model of an Enhancement Load



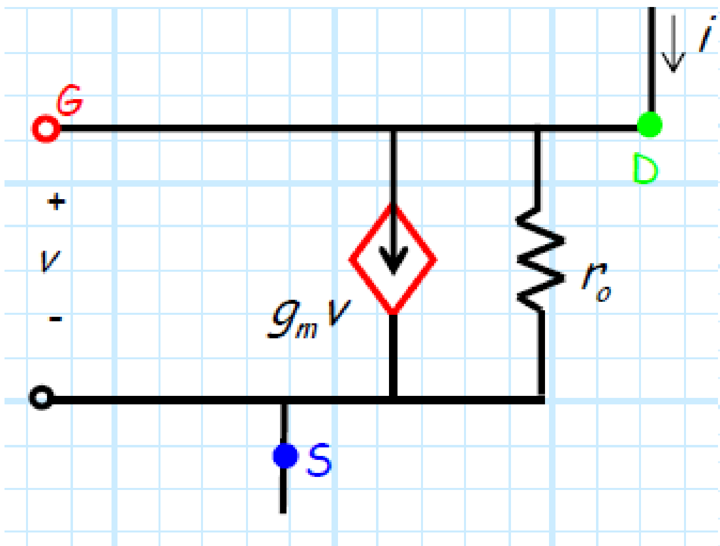
Inserting the MOSFET **small-signal model**, we get:



Redrawing this circuit, we get:



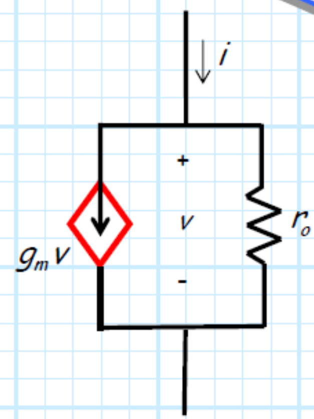
Small-signal Model of an Enhancement Load



Or, simplifying further, we have the small-signal equivalent circuit for an enhancement load:

*It is imperative that **you** understand that the circuit to my right is the **small-signal equivalent circuit** for an enhancement load.*

*Please replace all **enhancement loads** with this small-signal model whenever you are attempting to find the **small-signal circuit** of any MOSFET amplifier.*

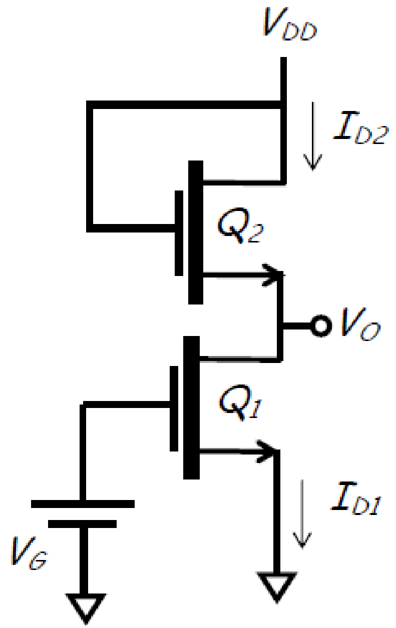


Enhancement Load
Small-Signal Model

DC analysis

Step 1 - *DC Analysis*

The DC circuit of this amplifier is:



Note that we are neglecting any channel modulation effect in the DC analysis.

Note that:

$$I_{D1} = I_{D2} \doteq I_D$$

and that:

$$V_{GS1} = V_G - 0 = V_G$$

and also that:

$$V_{DS2} = V_{GS2}$$

and finally that:

$$V_{DS1} = V_{DD} - V_{DS2}$$

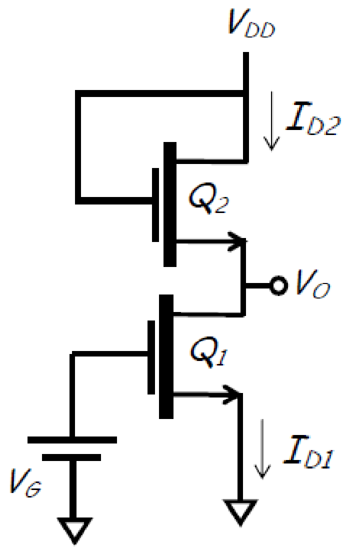
Let's of course **ASSUME** that both Q_1 and Q_2 are in saturation. Therefore we **ENFORCE**:

$$\begin{aligned} I_{D1} &= K_1 (V_{GS1} - V_{t1})^2 \\ &= K_1 (V_G - V_{t1})^2 \end{aligned}$$

Note that there are no unknowns in the previous equation. The drain current is explicitly determined from K_1 , V_G, and V_{t1}!

Continuing with the **ANALYSIS**, we can find the drain current through the enhancement load (I_{D2}), since it is equal to the current through Q_1:

DC analysis



$$I_{D2} = I_{D1} = K_1 (V_G - V_{t1})^2$$

Yet we also know that V_{GS2} must be related to this drain current as:

$$I_{D2} = K_2 (V_{GS2} - V_{t2})^2$$

and therefore combining the above equations:

$$I_{D1} = I_{D2}$$
$$K_1 (V_G - V_{t1})^2 = K_2 (V_{GS2} - V_{t2})^2$$

Note this last equation has only one unknown (V_{GS2})!
Rearranging, we find that:

$$V_{GS2} = \sqrt{\frac{K_1}{K_2}} (V_G - V_{t1}) + V_{t2}$$

Since $V_{DS2} = V_{GS2}$ and $V_{DS1} = V_{DD} - V_{DS2}$, we can likewise state that:

$$V_{DS2} = \sqrt{\frac{K_1}{K_2}} (V_G - V_{t1}) + V_{t2}$$

and:

$$V_{DS1} = V_{DD} - V_{t2} - \sqrt{\frac{K_1}{K_2}} (V_G - V_{t1})$$

Now, we must **CHECK** to see if our assumption is correct.

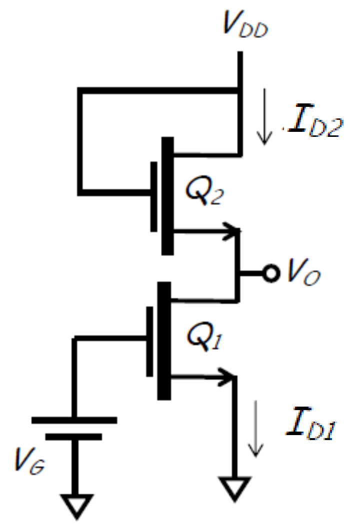
The saturation assumption will be correct if:

$$V_{DS1} > V_{GS1} - V_{t1}$$
$$> V_G - V_{t1}$$

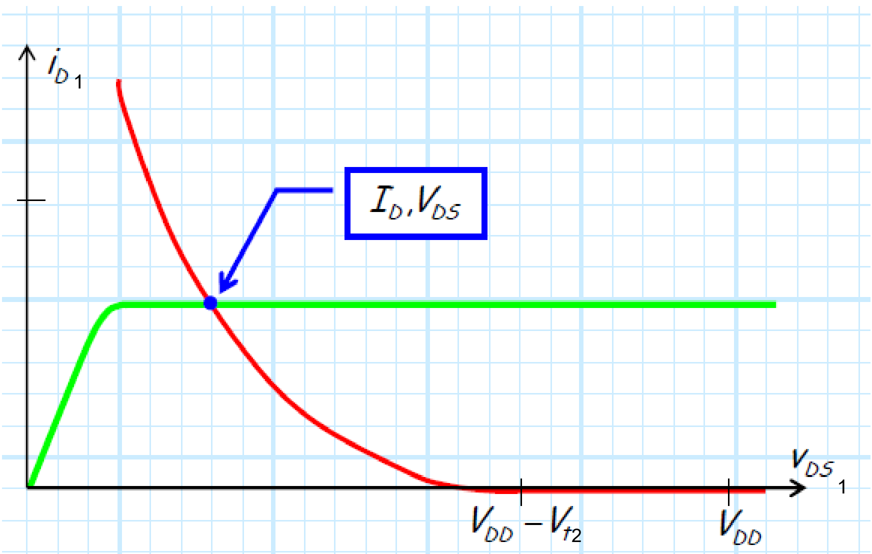
and:

$$V_{GS1} > V_{t1} \quad \therefore \quad \text{if} \quad V_G > V_{t1}$$

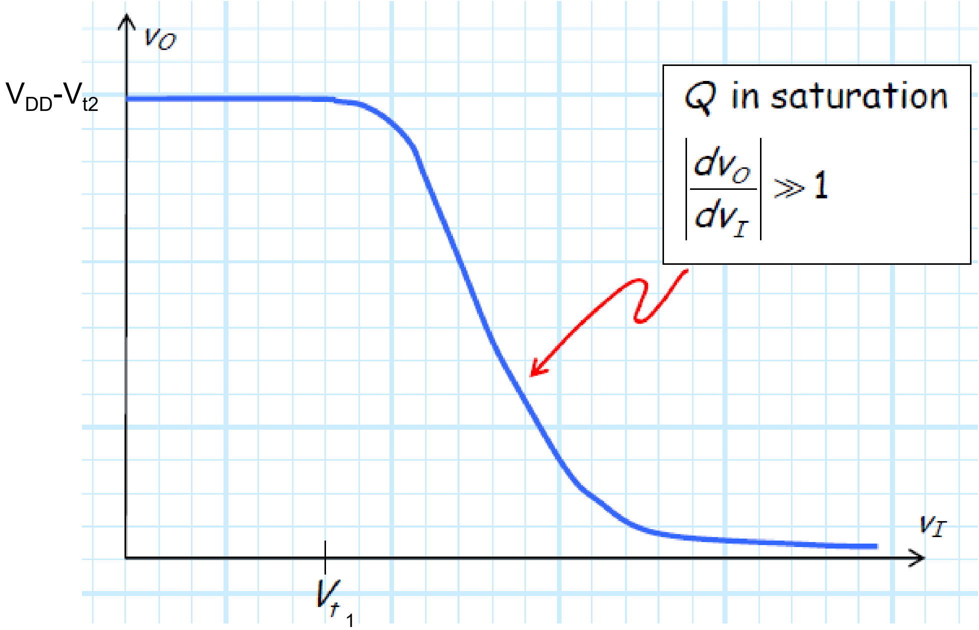
DC analysis



V_{DD}
I_{D2}
Q_2
V_O
Q_1
I_{D1}
V_G



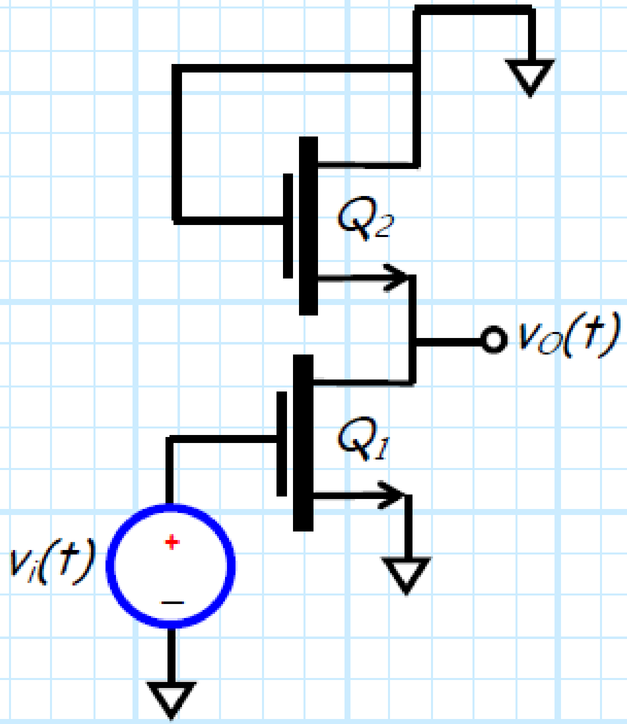
$i_{D\,1}$
I_D, V_{DS}
$v_{DS\,1}$
$V_{DD} - V_{t2}$
V_{DD}



v_O
V_{DD}-V_{t2}
Q in saturation
$\left|\frac{dv_O}{dv_I}\right| \gg 1$
v_I
$V_{t\,1}$

Small-signal analysis

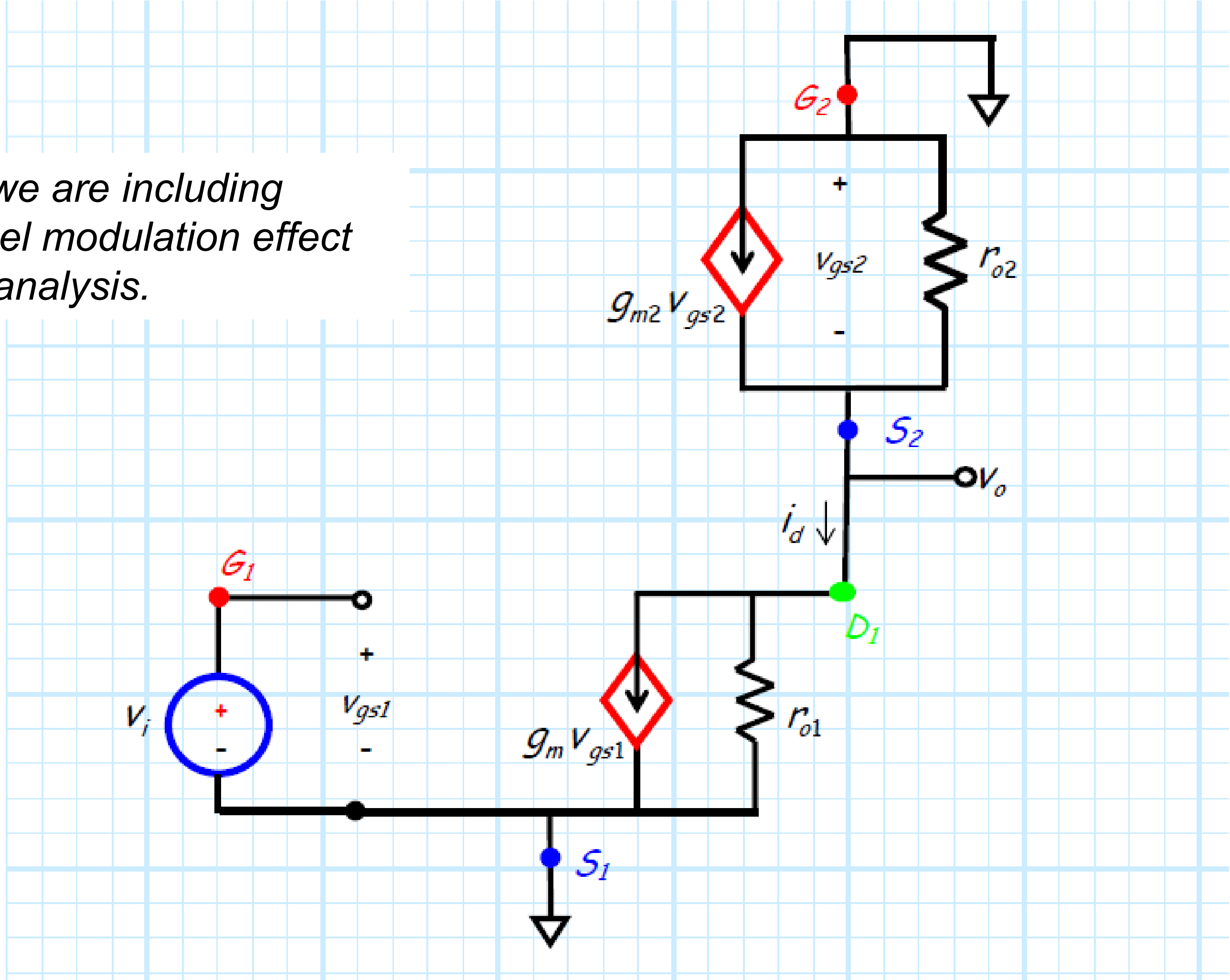
First, let's turn off the DC sources:



We now replace **MOSFET** Q_1 with its equivalent small-signal model, **and** replace the **enhancement load** with its equivalent small-signal model.

Small-signal analysis

Note that we are including any channel modulation effect in the DC analysis.



Note S_1 and G_2 are at **small-signal ground**!

Small-signal analysis

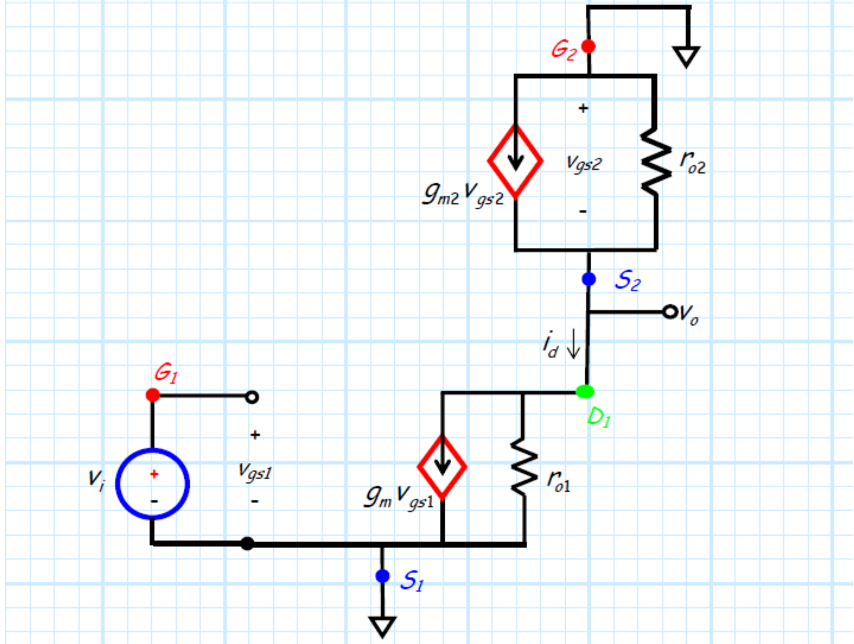
We require the small-signal parameters for each of the transistors Q_1 and Q_2. Therefore:

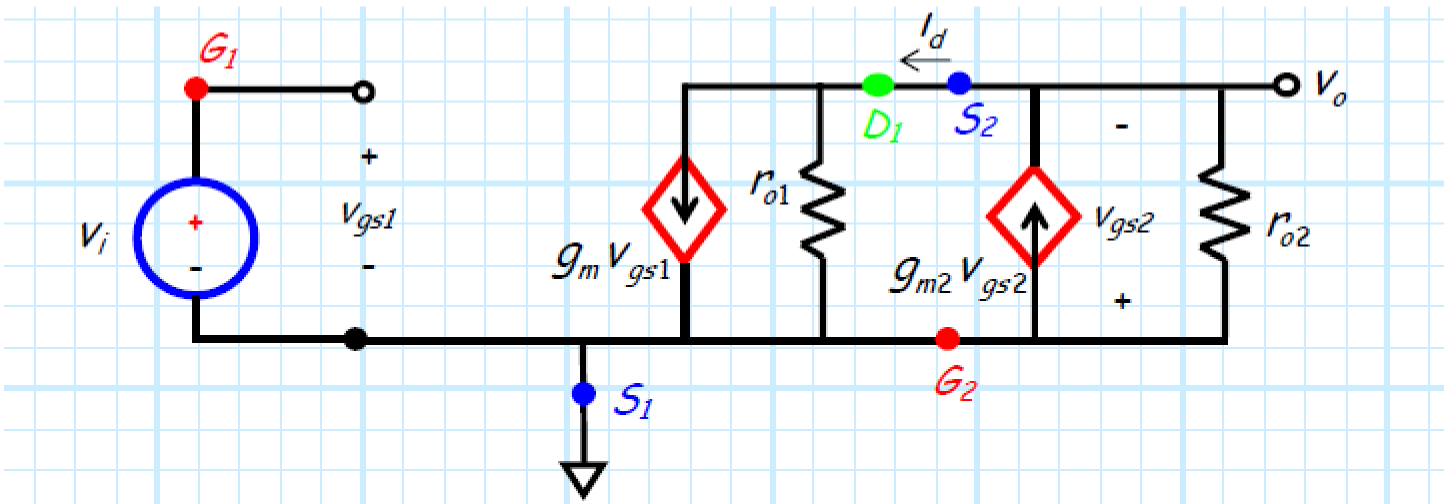
$$g_{m1} = 2K_1 (V_G - V_{t1}) \quad \text{and} \quad g_{m2} = 2K_1 (V_{GS2} - V_{t2})$$

and:

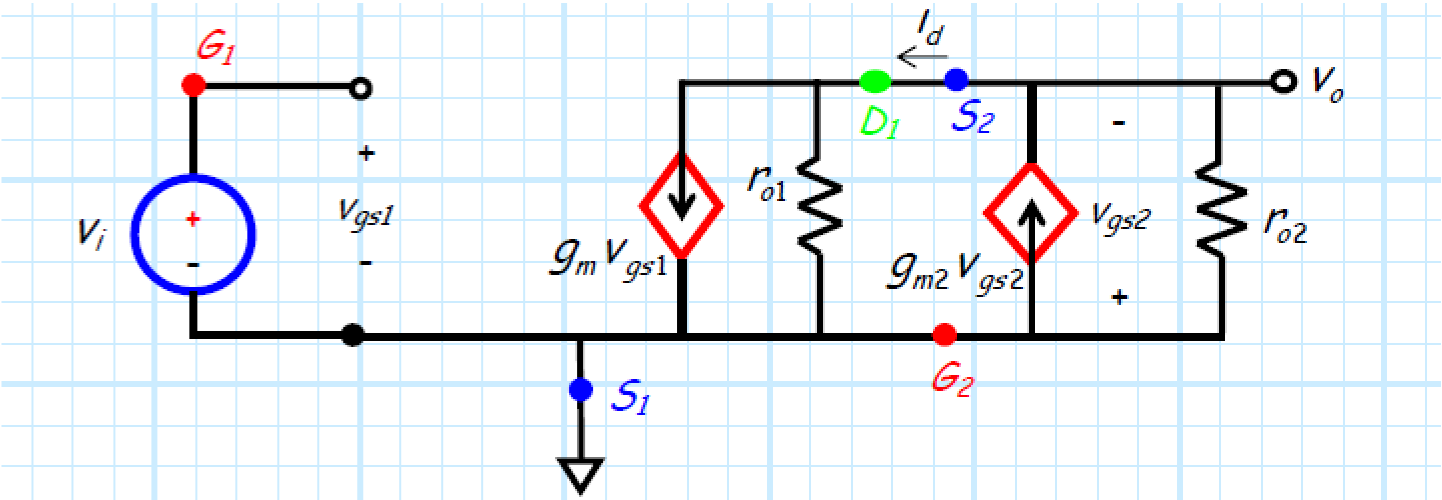
$$r_{o1} = \frac{1}{\lambda_1 I_D} \quad \text{and} \quad r_{o2} = \frac{1}{\lambda_2 I_D}$$

Small-signal analysis

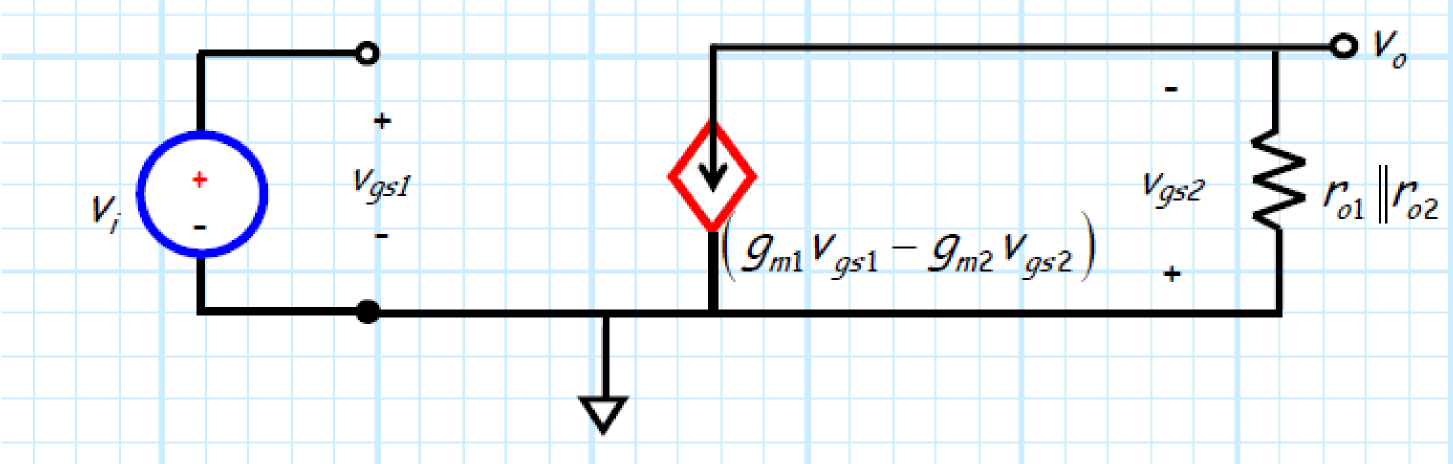




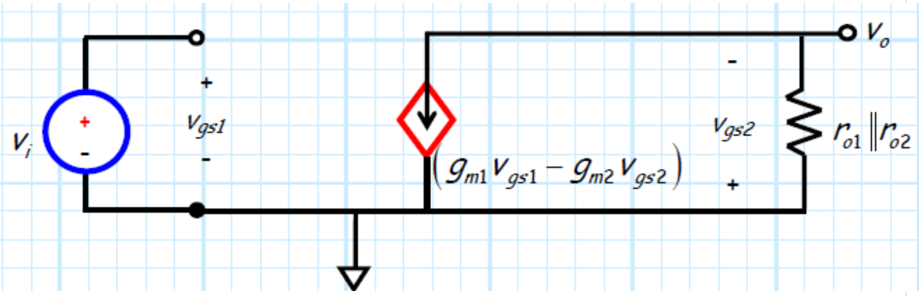
Small-signal analysis



Simplifying further, we find:



Small-signal analysis



Therefore, we find that:

$$v_{gs1} = v_i$$

and that:

$$v_{gs2} = -v_o$$

as well as that:

$$\begin{aligned} v_o &= -\left(g_{m1} v_{gs1} - g_{m2} v_{gs2}\right)\left(r_{o1} \| r_{o2}\right) \\ &= -\left(g_{m1} v_i + g_{m2} v_o\right)\left(r_{o1} \| r_{o2}\right) \end{aligned}$$

Rearranging, we find:

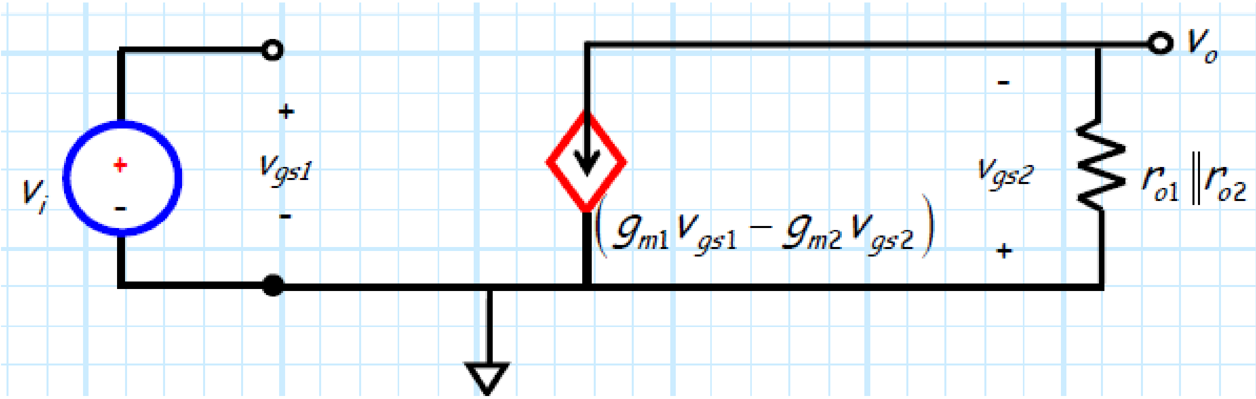
$$A_{vo} = \frac{v_o}{v_i} = \frac{-\left(r_{o1} \| r_{o2}\right) g_{m1}}{1 + \left(r_{o1} \| r_{o2}\right) g_{m2}} \approx \frac{-g_{m1}}{g_{m2}}$$

But recall that:

$$\begin{aligned} g_m &= 2K\left(V_{GS} - V_t\right) \\ &= 2\sqrt{K}\sqrt{I_D} \end{aligned}$$

where we have used the fact that $I_D = K\left(V_{GS} - V_t\right)^2$ to determine that $\left(V_{GS} - V_t\right) = \sqrt{I_D / K}$.

Small-signal analysis



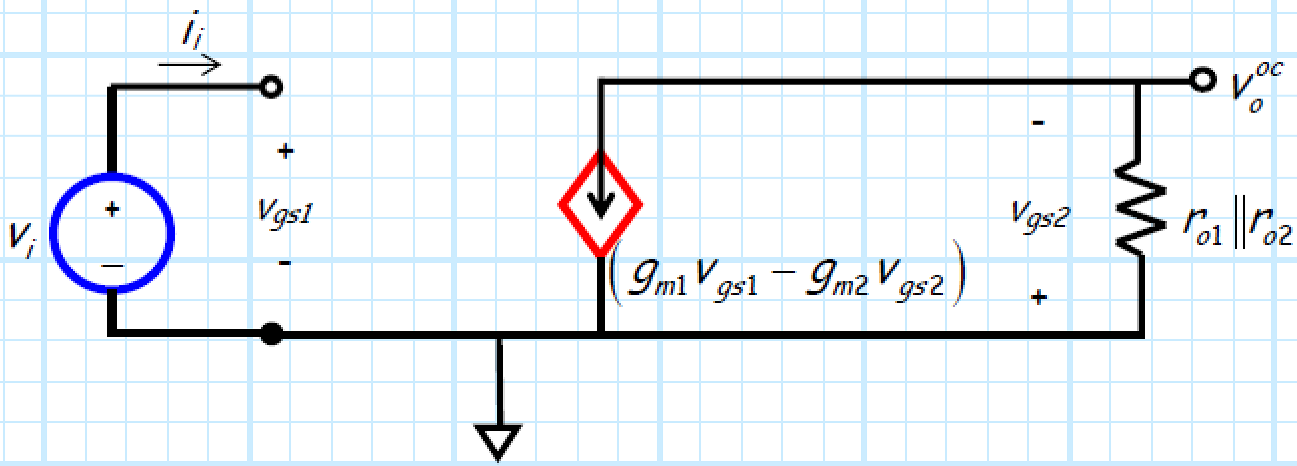
Therefore:

$$\left|A_{vo}\right| = \frac{g_{m1}}{g_{m2}} = \frac{2\sqrt{K_1}\sqrt{I_D}}{2\sqrt{K_2}\sqrt{I_D}} = \sqrt{\frac{K_1}{K_2}} = \frac{\sqrt{\left(W/L\right)_1}}{\sqrt{\left(W/L\right)_2}}$$

In other words, we adjust the MOSFET channel geometry to set the small-signal gain of this amplifier!

Small-signal analysis

Now let's determine the small-signal input and output resistances of this amplifier!



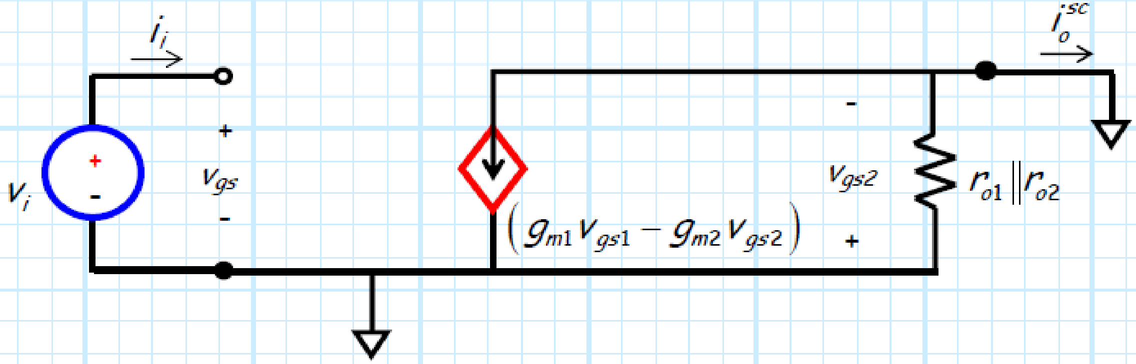
It is evident that since $i_i = i_g = 0$:

$$R_i = \frac{v_i}{i_i} = \infty \qquad \text{(Great!!!)}$$

Small-signal analysis

Now for the output resistance, we know that the open-circuit output voltage is:

$$v_o^{oc} = -\left(g_{m1} v_{gs1} - g_{m2} v_{gs2}\right)\left(r_{o1} \| r_{o2}\right)$$



Likewise, the short-circuit output current i_o^{sc} is:

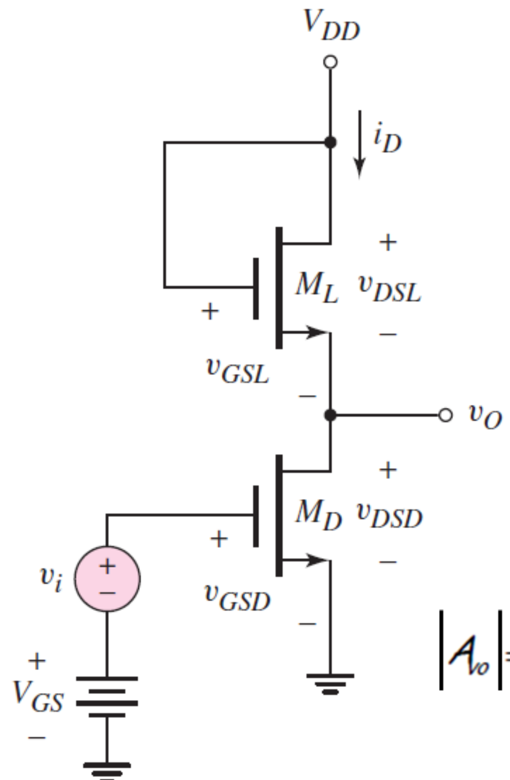
$$i_{os} = -\left(g_{m1} v_{gs1} - g_{m2} v_{gs2}\right)$$

Thus, the small-signal output resistance of this amplifier is equal to:

$$R_o = \frac{v_o^{oc}}{i_o^{sc}} = \frac{-\left(g_{m1} v_{gs1} - g_{m2} v_{gs2}\right)\left(r_{o1} \| r_{o2}\right)}{-\left(g_{m1} v_{gs1} - g_{m2} v_{gs2}\right)} = \left(r_{o1} \| r_{o2}\right)$$

In class problem

Ex 4.11: The bias voltage for the enhancement-load amplifier shown in Figure 4.39(a) is $V_{DD} = 3.3$ V. The transistor parameters are $V_{TND} = V_{TNL} = 0.4$ V, $k_n' = 100\,\mu\text{A/V}^2$, $(W/L)_L = 1.2$, and $\lambda = 0$. (a) Design the circuit such that the small-signal voltage gain is $|A_v| = 8$. (b) Determine V_{GSDQ} such that the Q-point is in the center of the saturation region. (Ans. (a) $(W/L)_D = 76.8$, (b) $V_{GSDQ} = 0.561$ V).



$$|A_{vo}| = \frac{-g_{m1}}{g_{m2}} = \frac{2\sqrt{K_1}\sqrt{I_D}}{2\sqrt{K_2}\sqrt{I_D}} = \sqrt{\frac{K_1}{K_2}} = \frac{\sqrt{\left(W/L\right)_1}}{\sqrt{\left(W/L\right)_2}}$$

In class problem, Solution

(a) $|A_v| = 8 = \sqrt{\dfrac{(W/L)_D}{(W/L)_L}} = \sqrt{\dfrac{(W/L)_D}{1.2}} \Rightarrow \left(\dfrac{W}{L}\right)_D = 76.8$

(b)

$$V_{GSDQ} = \left|\frac{V_{GSDt} - V_{GSDC}}{2}\right| + V_{GSDC}$$

$$V_{DSDQ} = \left|\frac{V_{DSDt} - V_{DSDC}}{2}\right| + V_{DSDt}$$

$V_{GSDC} = V_{TN} = 0.4V \qquad V_{DSDC} = V_{DD} - V_{TNL} = 3.3 - 0.4 = 2.9V$

$V_{DSDt} = V_{DSD(SAT)} = V_{GSDt} - V_{TND}$

$I_{DD} = K_{nD}(V_{GSD} - V_{TND})^2 = I_{DL} = K_{nL}(V_{GSL} - V_{TNL})^2$

$V_{GSL} = V_{DD} - V_{DSD}$

$K_{nD}(V_{GSD} - V_{TND})^2 = K_{nL}(V_{DD} - V_{DSD} - V_{TNL})^2$

$V_{DSD_t} = (V_{DD} - V_{TNL}) - \sqrt{\dfrac{K_{nD}}{K_{nL}}}\,(V_{GSD} - V_{TND})$

$V_{GSD} - V_{TND} = (V_{DD} - V_{TNL}) - \sqrt{\dfrac{K_{nD}}{K_{nL}}}\,(V_{GSD} - V_{TND})$

$$V_{GSDt} = \frac{(V_{DD} - V_{TNL}) + V_{TND}\left(1 + \sqrt{K_{nD}/K_{nL}}\right)}{1 + \sqrt{\dfrac{K_{nD}}{K_{nL}}}}$$

$\sqrt{\dfrac{K_{nD}}{K_{nL}}} = \sqrt{\dfrac{(W/L)_D}{(W/L)_L}} = 8$

$$V_{GSDt} = \frac{(3.3 - 0.4) + 0.4(1+8)}{1+8} = 0.7222V$$

$$V_{GSDQ} = \frac{0.7222 - 0.4}{2} + 0.4 = 0.561V$$

$V_{DSDt} = 0.561 - 0.4 = 0.161V$

$$V_{DSDQ} = \frac{2.9 - 0.161}{2} + 0.161 = 1.53V$$

Overview of lecture 9

Single-stage IC MOSFET amplifiers-Amplifiers with active loads (Neamen 4.7.4)

Multi-stage MOSFET amplifiers (Neamen 4.8.1)