ECE 322L
Electronics 2

01/30/20 - Lecture 4

Biasing configurations 2

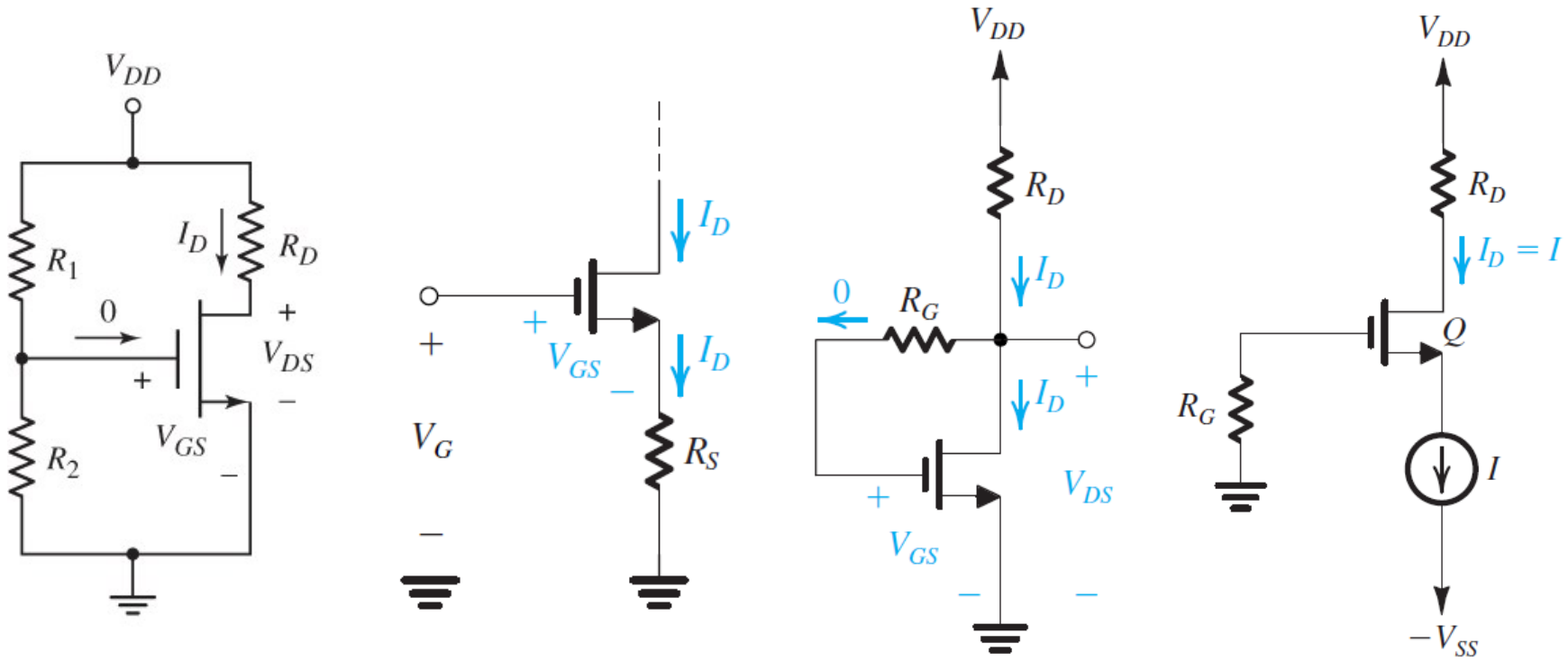
Updates and overview

- Homework 1 is online (Both soft and hard copies will be accepted). The TA will create a link for you to upload the homework.
- Lab 2 will be online tomorrow
- More examples of biasing circuits

(Neamen 3.2,3.4, S&S 5.3, 5.4, 5.7)

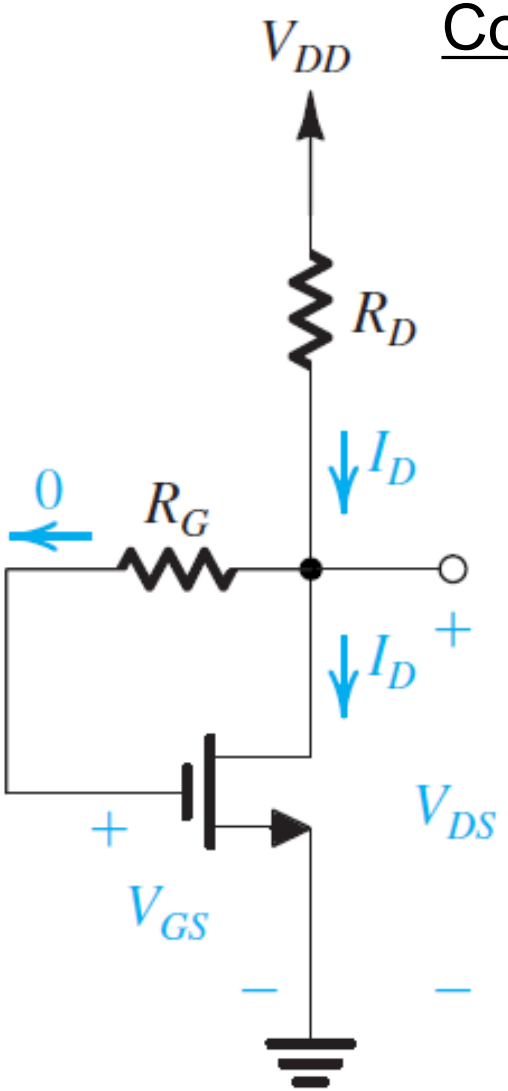
Biasing circuits

A well-designed biasing circuit for an amplifier should force a stable and predictable V_{GS}, I_D, and V_{DS} that ensure operation in the saturation region for all expected input signal levels.



Four possible biasing circuits or configurations

Biasing by a drain-to-gate feedback resistor



Condition: very large R_G (MΩ)

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \Rightarrow I_D = \frac{V_{DD} - V_{GS}}{R_D}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

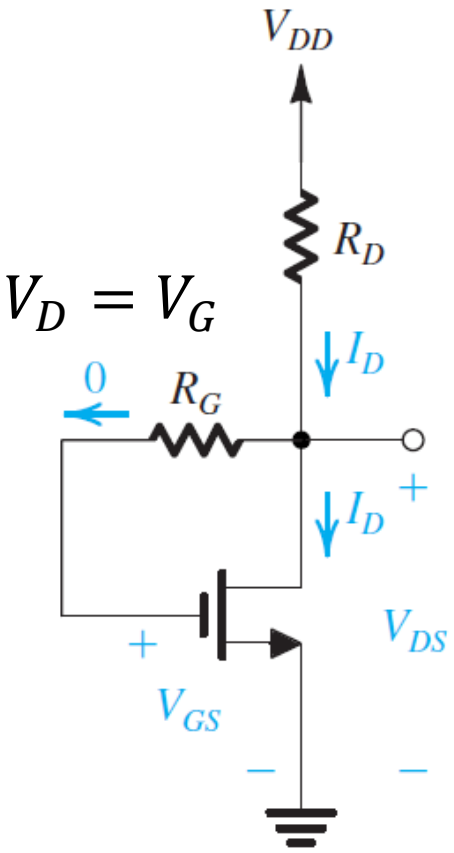
$$\frac{V_{DD} - V_{GS}}{R_D} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$V_{GS} = V_{DS} = f(V_{DD}, R_D)$$

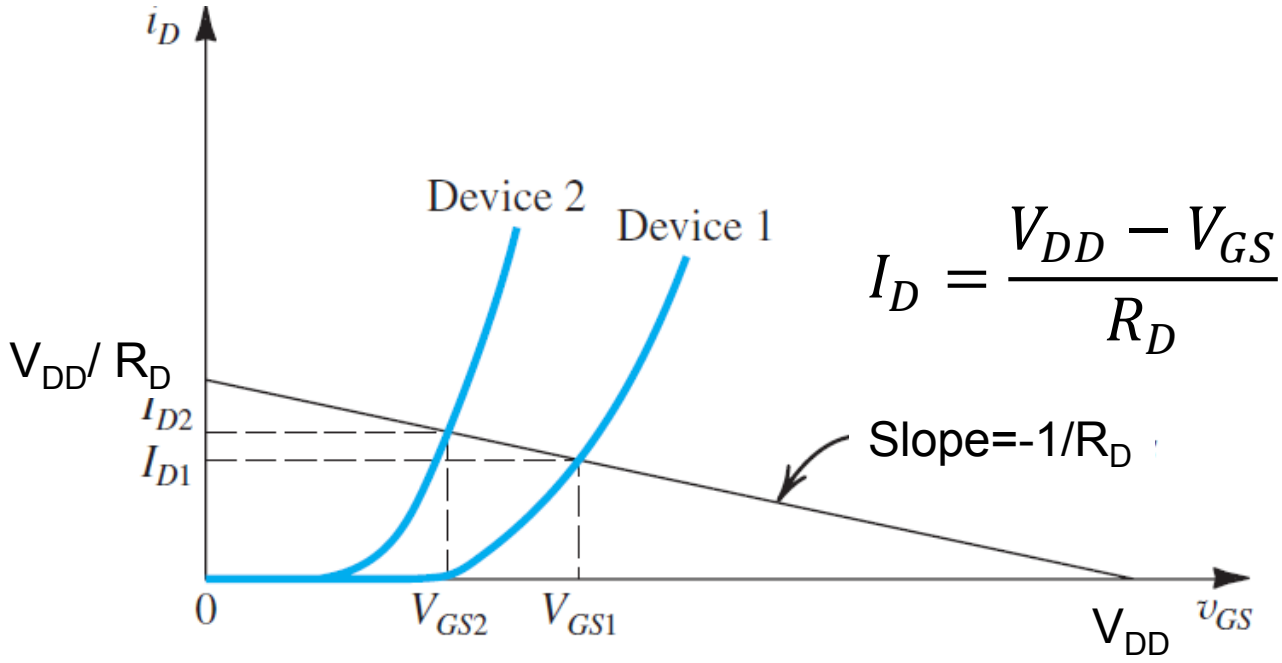
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Biasing by a drain-to-gate feedback resistor

R_D implements a feedback loop which keeps I_D relatively stable



$$V_{DD} = V_{GS} + R_D I_D \qquad I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$



$$I_D = \frac{V_{DD} - V_{GS}}{R_D}$$

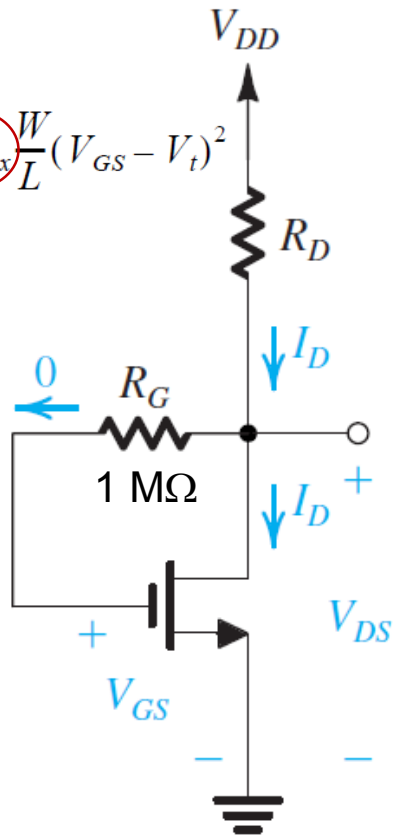
A high R_D is preferable to ensure stability

Trade off: High R_D will reduce V_{DS} and move the Q point towards triode

In class problem 1

D5.35 Design the circuit in Fig. 5.54 to operate at a dc drain current of 0.5 mA. Assume $V_{DD} = +5$ V, $k_n'W/L = 1$ mA/V^2, $V_t = 1$ V, and $\lambda = 0$. Use a standard 5% resistance value for R_D, and give the actual values obtained for I_D and V_D.

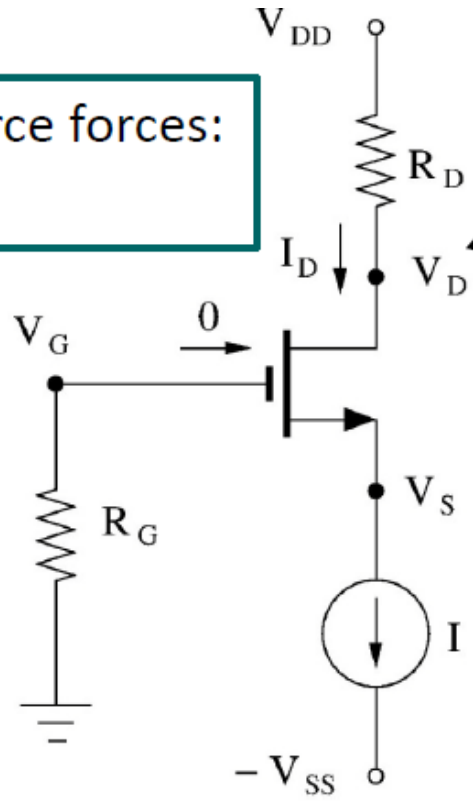
$$I_D = \frac{1}{2}\underbrace{\mu_n C_{ox}}_{k_n'}\frac{W}{L}(V_{GS} - V_t)^2$$



Standard Resistor Values (±5%)						
1.0	10	100	1.0K	10K	100K	1.0M
1.1	11	110	1.1K	11K	110K	1.1M
1.2	12	120	1.2K	12K	120K	1.2M
1.3	13	130	1.3K	13K	130K	1.3M
1.5	15	150	1.5K	15K	150K	1.5M
1.6	16	160	1.6K	16K	160K	1.6M
1.8	18	180	1.8K	18K	180K	1.8M
2.0	20	200	2.0K	20K	200K	2.0M
2.2	22	220	2.2K	22K	220K	2.2M
2.4	24	240	2.4K	24K	240K	2.4M
2.7	27	270	2.7K	27K	270K	2.7M
3.0	30	300	3.0K	30K	300K	3.0M
3.3	33	330	3.3K	33K	330K	3.3M
3.6	36	360	3.6K	36K	360K	3.6M
3.9	39	390	3.9K	39K	390K	3.9M
4.3	43	430	4.3K	43K	430K	4.3M
4.7	47	470	4.7K	47K	470K	4.7M
5.1	51	510	5.1K	51K	510K	5.1M
5.6	56	560	5.6K	56K	560K	5.6M
6.2	62	620	6.2K	62K	620K	6.2M
6.8	68	680	6.8K	68K	680K	6.8M
7.5	75	750	7.5K	75K	750K	7.5M
8.2	82	820	8.2K	82K	820K	8.2M
9.1	91	910	9.1K	91K	910K	9.1M

Figure 5.54 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

Biasing by a Current Source



1) Current source forces:
$I_D = I$

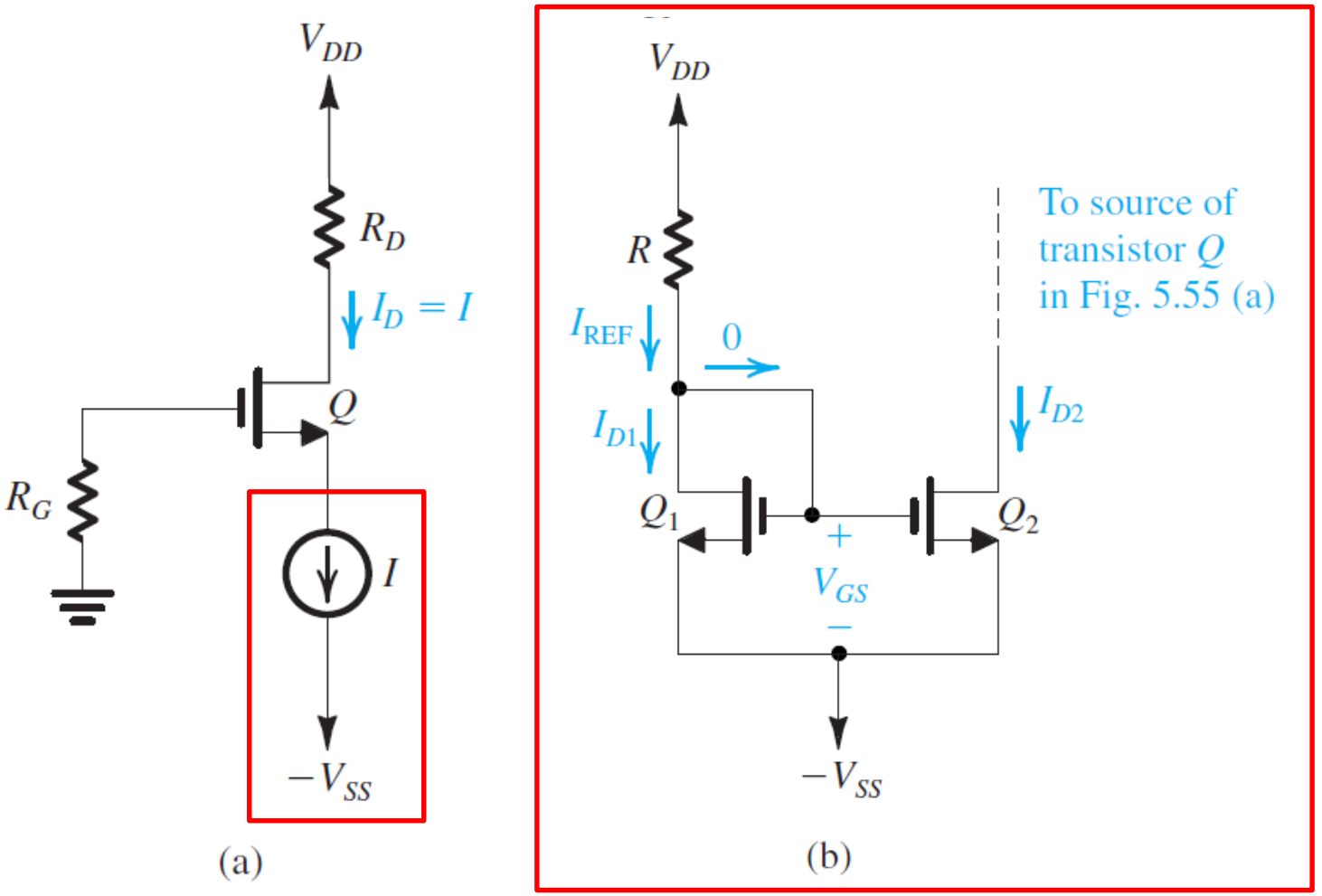
2) $V_D = V_{DD} - R_D I_D$

3) V_{GS} is set by
$I_D = 0.5\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$

4) $V_S = V_G - V_{GS} = -V_{GS}$

5) $V_{DS} = V_D - V_S$

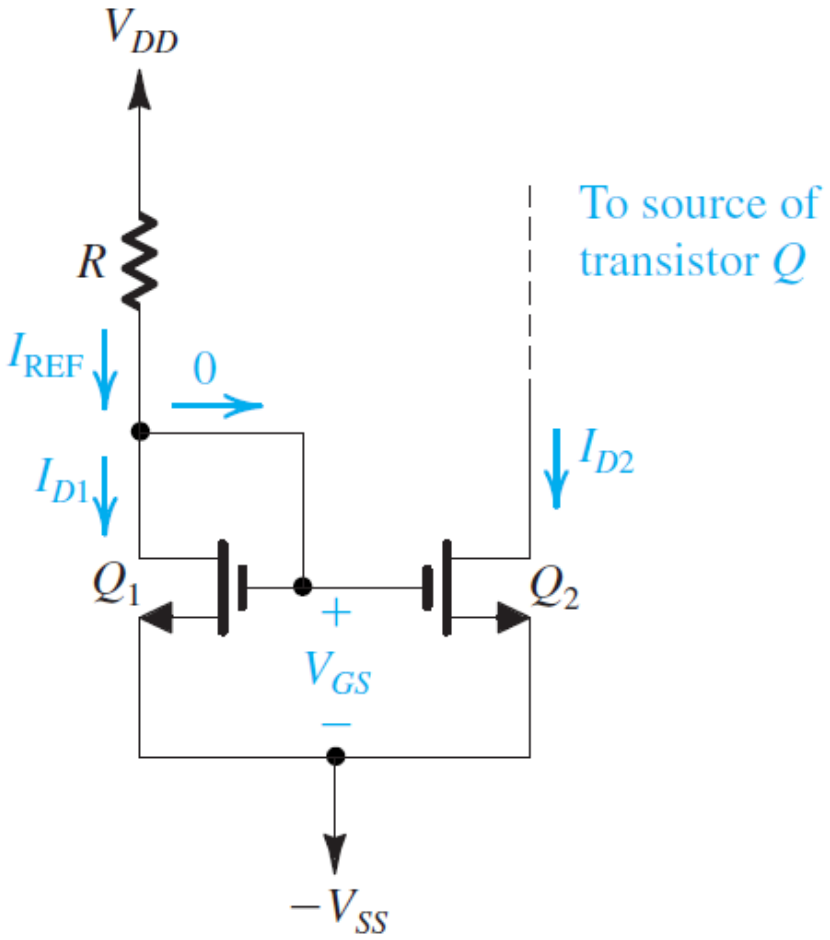
Biasing by a Current Source (IC)



Current mirror

Current Mirror

Assumptions: k_n' and V_t are the same for Q_1 and Q_2



$$I = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2(V_{GS} - V_t)^2$$

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1(V_{GS} - V_t)^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R}$$

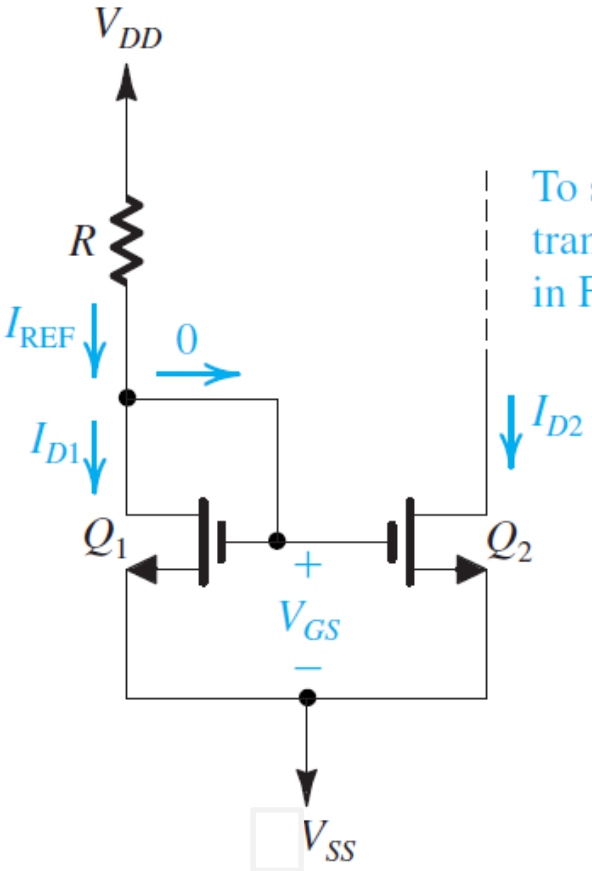
$$I = I_{REF}\frac{(W/L)_2}{(W/L)_1}$$

Q2 needs to be in saturation for mirroring to occur

Q1 is in saturation because $V_{DS} = V_{GS}$

In class problem 2

D5.36 Using two transistors Q_1 and Q_2 having equal lengths but widths related by $W_2/W_1 = 5$, design the circuit of Fig. 5.55(b) to obtain $I = 0.5$ mA. Let $V_{DD} = -V_{SS} = 5$ V, $k_n'(W/L)_1 = 0.8$ mA/V^2, $V_t = 1$ V, and $\lambda = 0$. Find the required value for R. What is the voltage at the gates of Q_1 and Q_2? What is the lowest voltage allowed at the drain of Q_2 while Q_2 remains in the saturation region?



To source of transistor Q in Fig. 5.55 (a)

$$I_D = \frac{1}{2}\underbrace{\mu_n C_{ox}}_{k_n'}\frac{W}{L}(V_{GS} - V_t)^2$$

$$I = I_{REF}\frac{(W/L)_2}{(W/L)_1}$$

Overview of lecture 5

- More on current mirrors
- (Neamen 3.2,3.4, S&S 5.3, 5.4, 5.7)
- FETs as amplifiers; total components and small signal analysis

  (Neamen 4.1.1, 4.1.2- S&S from 5.5.1 to 5.5.6)