ECE 371
Materials and Devices

11/26/19 - Lecture 24

Ch. 10 – MOS Capacitor

General Information

- Homework 8 assigned, due on Thursday 12/5
- Final Exam (Tuesday 12/10, 12:30pm-2:30pm, cumulative but focused on ch. 7,8,10)
- Reading for next time: 10.1, 10.3

p-Type with Positive Bias

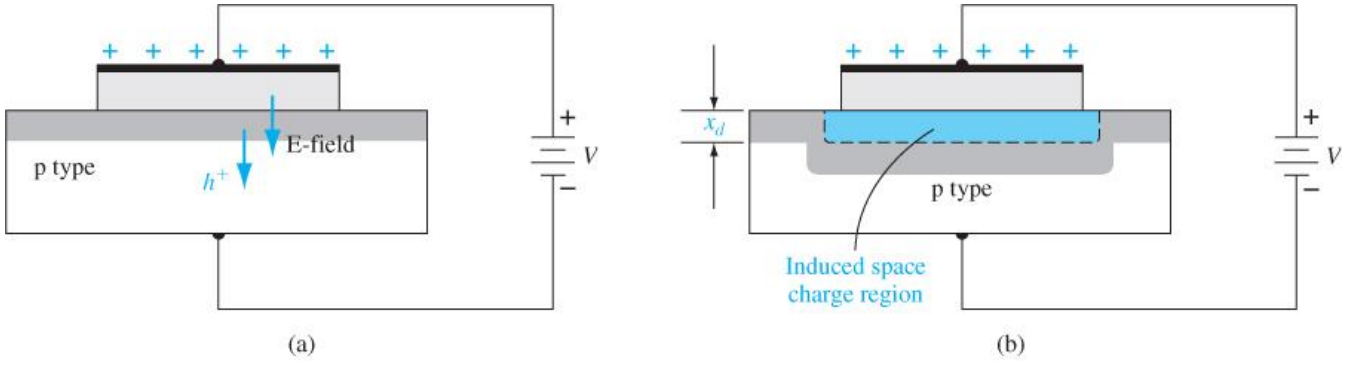


Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

- Top metal gate is at a positive voltage with respect to the substrate
- Electric field forces holes away from the oxide-semiconductor interface
- Negative space-charge region forms near the interface (depletion of holes)

MOS Capacitor: p-type Band Diagrams

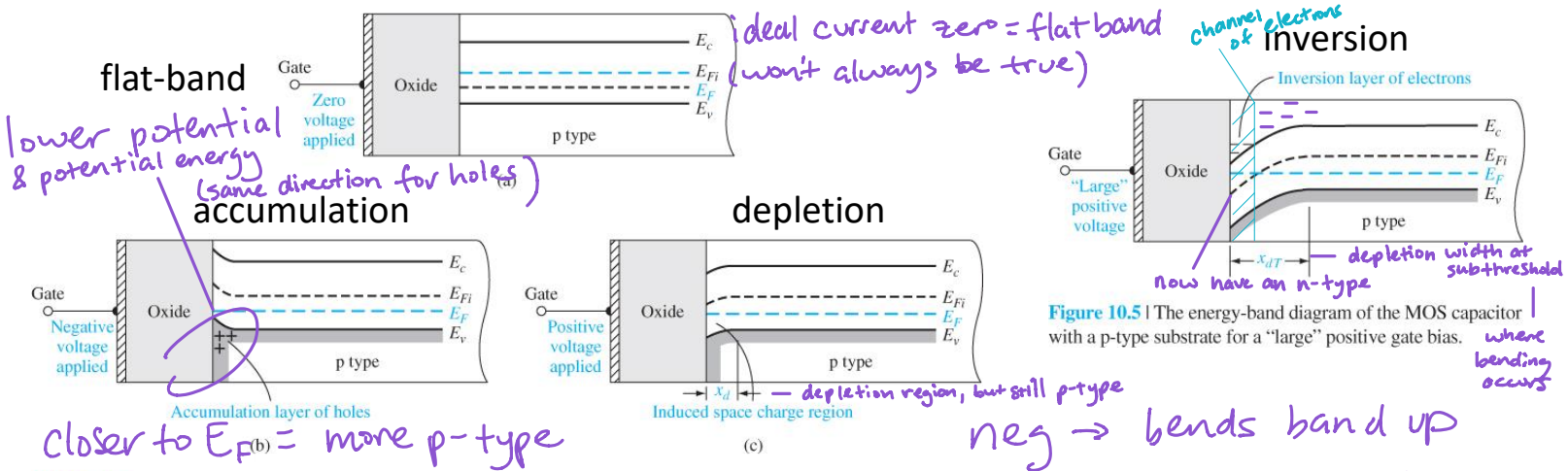


Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case, (b) a negative gate bias, and (c) a moderate positive gate bias.

Figure 10.5 | The energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.

- Zero bias is the "flat band" condition
- Negative bias causes ***accumulation*** of holes near the surface since E_v-E_F is smaller near the surface. Surface appears more "p-type."
- Positive bias causes ***depletion*** of holes near the surface. A space-charge region forms where holes are depleted and ionized acceptors remain. E_v-E_F is larger near the surface.
- Larger positive bias causes a higher E-field, more band bending, and a larger depletion width. E_F-E_{Fi} > 0 near the surface, which means surface is "n-type." An ***inversion*** layer of electrons forms.
- Devices are in thermal equilibrium (e.g. - $\frac{dE_F}{dx} = 0$) since no current can flow

Fermi level flat

MOS Capacitor: n-Type Substrate

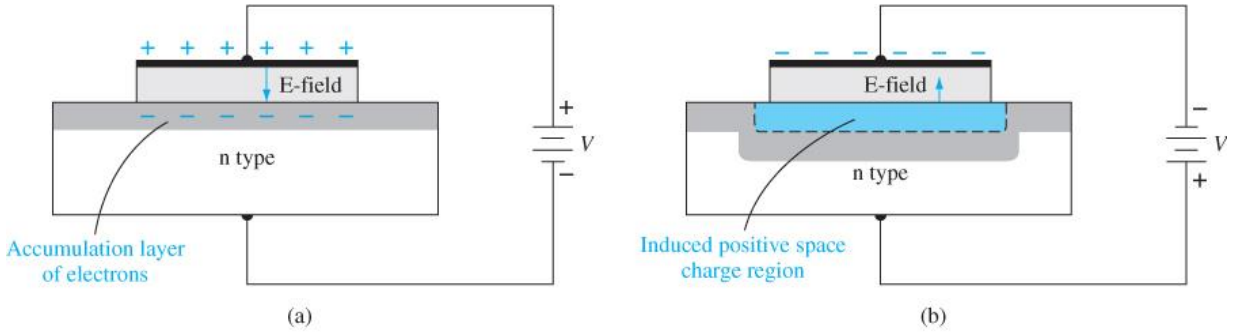
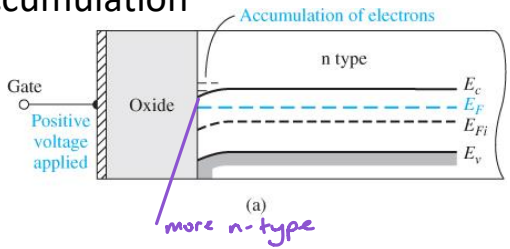


Figure 10.6 | The MOS capacitor with an n-type substrate for (a) a positive gate bias and (b) a moderate negative gate bias.

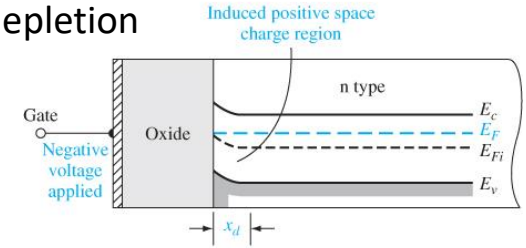
- Positive voltage causes accumulation of electrons near the surface
- Negative voltage causes depletion of electrons near the surface

MOS Capacitor: n-Type Band Diagrams

accumulation



depletion



inversion

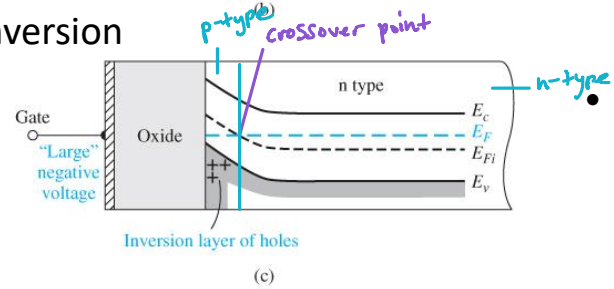


Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias, (b) a moderate negative bias, and (c) a "large" negative gate bias.

- Positive bias causes ***accumulation*** of electrons near the surface since E_c-E_F is smaller near the surface. Surface appears more "n-type."
- Negative bias causes ***depletion*** of electrons near the surface. A space-charge region forms where electrons are depleted and ionized donors remain. E_c-E_F is larger near the surface.
- Larger negative bias causes a higher E-field, more band bending, and a larger depletion width. E_{Fi}-E_F > 0 near the surface, which means surface is "p-type." An ***inversion*** layer of holes forms.

Depletion Layer Thickness

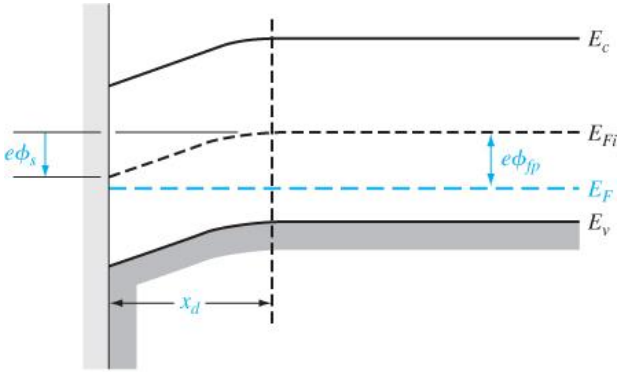


Figure 10.8 | The energy-band diagram in the p-type semiconductor, indicating surface potential.

p-type

$$\phi_{Fp} = \frac{kT}{e} ln\left(\frac{N_a}{n_i}\right)$$

$$x_d = \left(\frac{2\varepsilon_s \phi_s}{eN_a}\right)^{\frac{1}{2}}$$

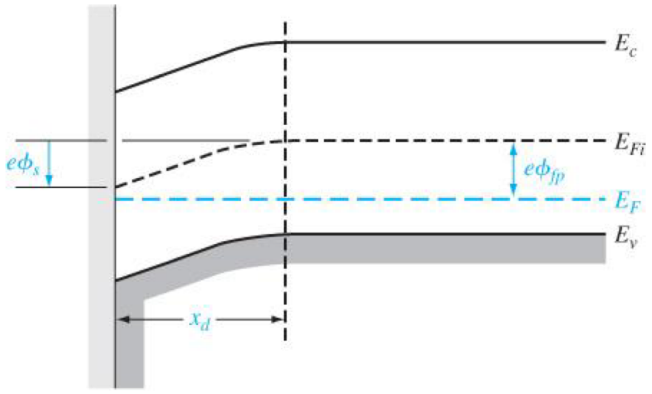
n-type

$$\phi_{Fn} = \frac{kT}{e} ln\left(\frac{N_d}{n_i}\right)$$

$$x_d = \left(\frac{2\varepsilon_s \phi_s}{eN_d}\right)^{\frac{1}{2}}$$

- What is the width of the space-charge region near the surface?
- ϕ_s is the surface potential (i.e., the potential across the space-charge region)
- ϕ_s can be found with a similar procedure to that used for V_{bi} of a pn-junction. Try it!
- Looks like a one-sided (asymmetric) pn-junction

Depletion Layer Thickness



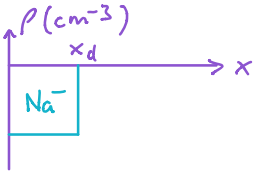
$E_{Fi} > E_F \rightarrow$ p-type

$e\phi_s$ (surface potential)

$= E_{Fi\,bulk} - E_{Fi\,surface}$

(amount of band bending)

① calculate from E-field



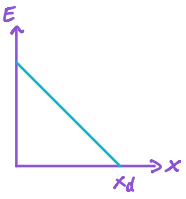
$Na^- \rightarrow$ fixed acceptors

from this we can find E-field

$$E(x) = \int \frac{-eN_a}{\epsilon_s}\,dx = \frac{-eN_a}{\epsilon_s}\,x$$

$$E(x_d) = 0 = \frac{-eN_a}{\epsilon_s} + C_1 = 0$$

$$\boxed{E(x) = \frac{-eN_a}{\epsilon_s}(x - x_d)}$$



② $\phi(x) = -\int \frac{-eN_a}{\epsilon_s}(x - x_d)\,dx$

$$= \frac{eN_a}{\epsilon_s}\left(\frac{x^2}{2} - x_d x\right) + C_2$$

$\phi(x_d) = 0 \rightarrow C_2 = \frac{eN_a x_d^2}{2\epsilon_s}$

$$\phi(x) = \frac{eN_a}{2\epsilon_s}\left(x^2 - 2x_d x + x_d^2\right)$$

$$\boxed{\phi(x) = \frac{eN_a}{2\epsilon_s}(x - x_d)^2}$$

At $x = 0$, $\phi(0) = \phi_s$

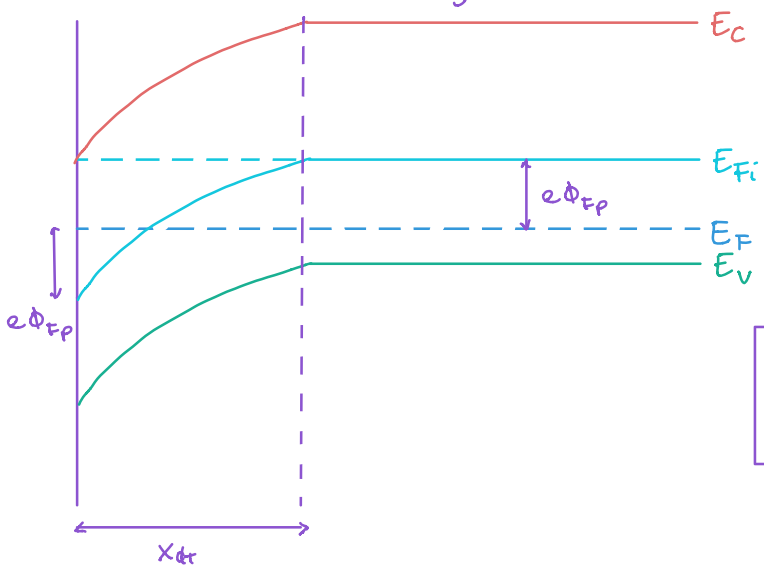
$$\phi_s = \frac{eN_a x_d^2}{2\epsilon_s} \rightarrow x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a}\right)^{1/2}$$

(depletion width for p-type* substrate)

* for n-type, just replace Na with Nd

For special case $\phi_s = 2\phi_{Fp}$

E_{Fi} comes all the way down

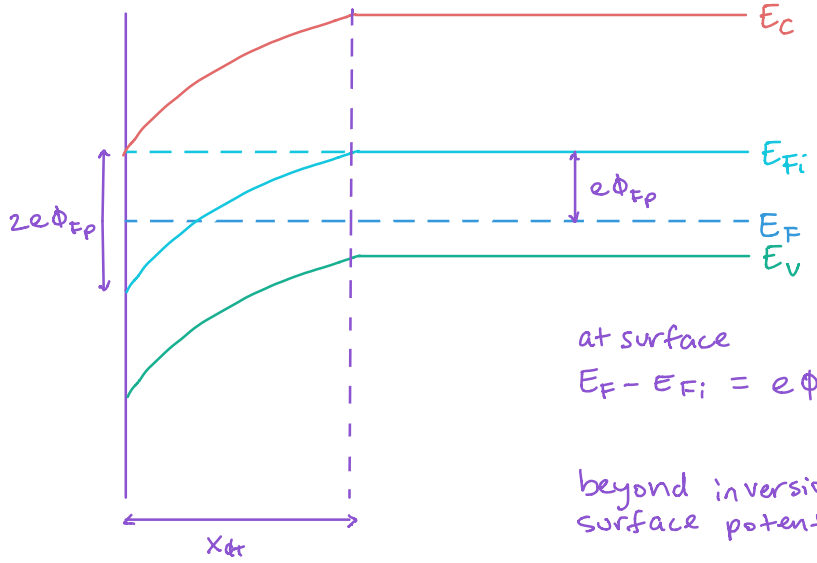


$$e\phi_s = 2e\phi_{Fp}$$
(threshold voltage)

then

$$x_d \rightarrow x_{dT} = \left(\frac{4\epsilon_s \phi_{Fp}}{e N_a}\right)^{1/2}$$

Surface Charge Density



at surface

$E_F - E_{Fi} = e\phi_{Fp}$ at inversion

beyond inversion increase surface potential $\Delta\phi_s$

$E_F - E_{Fi} = e\phi_{Fp} + e\Delta\phi_s$

recall: $n = n_i \exp\left[\frac{E_F - E_{Fi}}{kT}\right]$

$V_t = \frac{kT}{e}$

$n_s = n_i \exp\left[\frac{e\phi_{Fp} + e\phi_s}{kT}\right]$

$= n_i \exp\left(\frac{\phi_{Fp}}{V_t}\right) \exp\left(\frac{\Delta\phi_s}{V_t}\right)$

$$n_s = n_{st} \exp\left(\frac{\Delta\phi_s}{V_t}\right)$$

n_{st} (inverted surface charge density at threshold)

Threshold Inversion Point

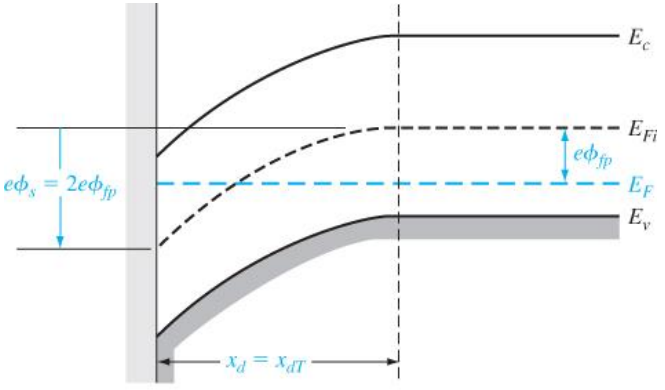


Figure 10.9 | The energy-band diagram in the p-type semiconductor at the threshold inversion point.

Maximum Depletion Widths

p-type

$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{Fp}}{eN_a}\right)^{\frac{1}{2}}$$

n-type

$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{Fn}}{eN_d}\right)^{\frac{1}{2}}$$

- Threshold Inversion Point: when the electron concentration at the surface is the same as the hole concentration in the bulk (p-type substrate)
- Occurs when $e\phi_s = 2e\phi_{Fp}$
- The depletion region width practically reaches a maximum at the threshold inversion point since the electron inversion layer "screens" any additional voltage applied to the gate from adding electric field to the semiconductor

Threshold Inversion Point

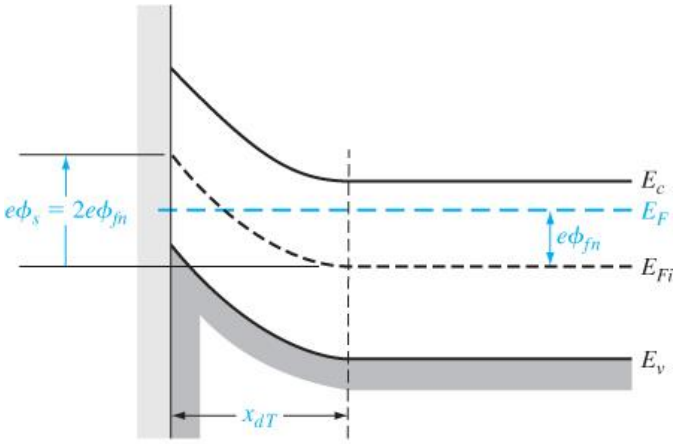


Figure 10.10 | The energy-band diagram in the n-type semiconductor at the threshold inversion point.

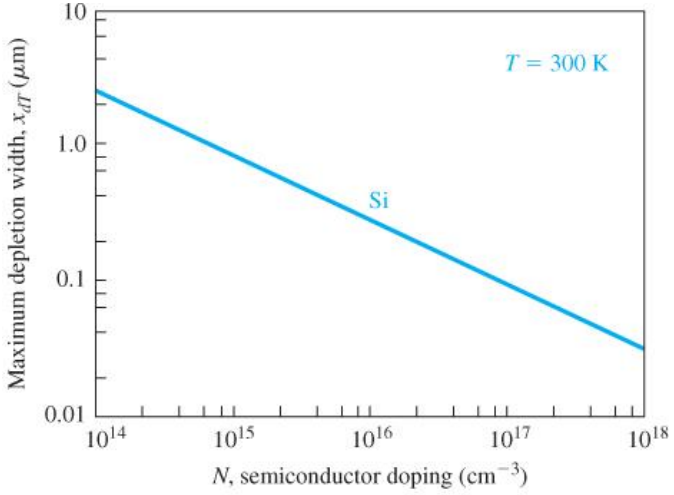


Figure 10.11 | Maximum induced space charge region width versus semiconductor doping.

- Similar condition exists for n-type substrates ($e\phi_s = 2e\phi_{Fn}$) when the hole concentration at the surface becomes equal to the electron concentration in the bulk
- The depletion width is inversely proportional to the square root of the doping concentration

Surface Charge Density

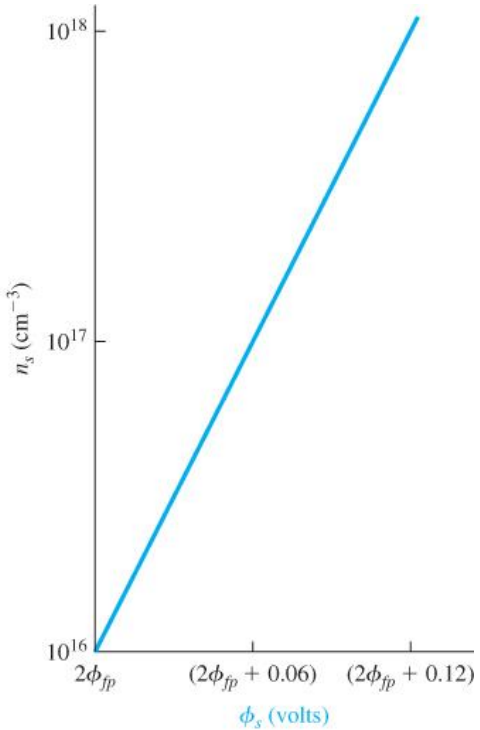


Figure 10.12 | Electron inversion charge density as a function of surface potential.

- How does the surface charge density (n_s) change as a function of change in surface potential ($\Delta\phi_s$)?

$$n_s = n_{st} exp\left(\frac{\Delta\phi_s}{V_t}\right)$$

surface charge density

- $\Delta\phi_s$ is the change in surface potential beyond the threshold inversion point
- n_{st} is the surface electron density at the threshold inversion point
- Inversion charge density increases very rapidly with a small increase in surface potential
- Screens gate charge → depletion width constant beyond inversion

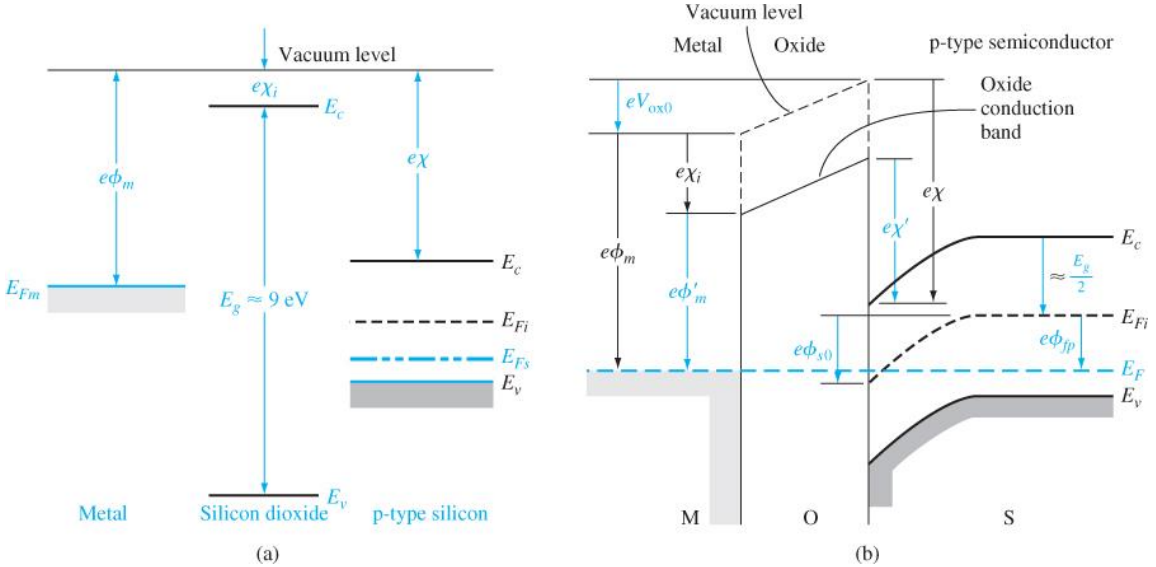
Terminology

- Vacuum Level: the minimum energy an electron must posses to completely free itself from the material
- Work Function (ϕ): energy difference between the vacuum level and the Fermi energy
  - For metals ϕ_m is an invariant material constant
  - For semiconductors, ϕ_{semi} depends upon doping
- Electron Affinity (χ): the difference between the vacuum level and the conduction band energy
- Modified Metal Work Function (ϕ_m'): the potential required to inject an electron from the metal into the conduction band of the oxide
- Modified Electron Affinity (χ'): the difference between the conduction band energy at the semiconductor surface and the conduction band energy at the oxide surface
- V_{ox0}: the potential difference across the oxide at zero bias. Not necessarily zero.
- ϕ_{s0}: potential at the surface at zero bias

Non-Ideal MOS

- In the previous band diagram drawings for accumulation, inversion, and depletion, we assumed the MOS structure was "ideal," meaning:
  1. The work functions in the metal and semiconductor were the same
  2. There was no charge within or at the surface of the oxide
- As a result, the energy bands in the semiconductor were flat under zero gate bias (see Figures 10.4 and 10.7, for example)
- In reality under non-ideal conditions, the work functions may be different and charges may exist within the oxide
- Under non-ideal conditions there will be band bending within the semiconductor near the oxide surface even under zero bias
- The shape of the band bending depends upon the sign of $\phi_m - \phi_{semi}$
- This band bending is important in determining the sign of the voltage that must be applied to reach flat band

Work Function Difference



$$\phi_{s0} = -(V_{ox0} + \phi_{ms})$$

Figure 10.13 | (a) Energy levels in a MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

- Under non-ideal conditions there is surface band bending even at zero gate bias
- Fermi levels must align between metal, oxide, and semiconductor
- Since $\phi_m - \phi_{semi}$ are constants, the vacuum level energy must change
- The band bending at the surface depends upon the oxide charge and the metal-semiconductor work function difference ($\phi_{ms} = \phi_m - \phi_{semi}$)

Work Function Difference

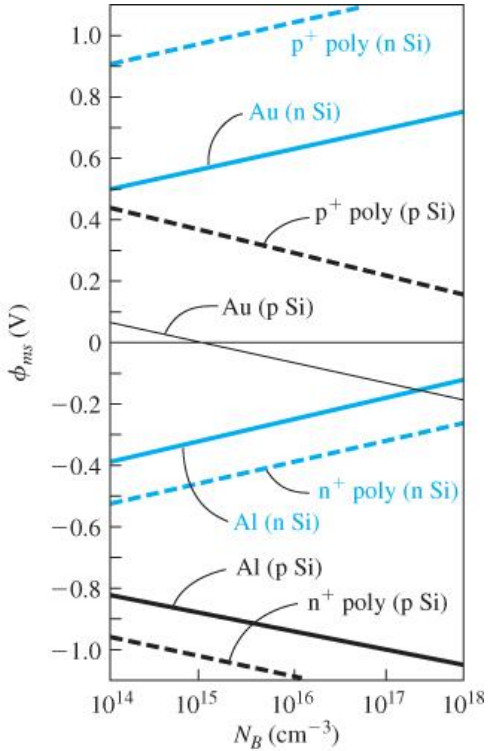


Figure 10.16 | Metal–semiconductor work function difference versus doping for aluminum, gold, and n⁻ and p⁻ polysilicon gates.
(*From Sze [17] and Werner [20].*)

- The direction of the band bending depends upon the sign of ϕ_{ms}
- The sign depends upon the gate and semiconductor materials and the semiconductor doping type and concentration

p-type

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2} + \phi_{Fp}\right)$$

n-type

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2} - \phi_{Fn}\right)$$

Flat-Band Voltage

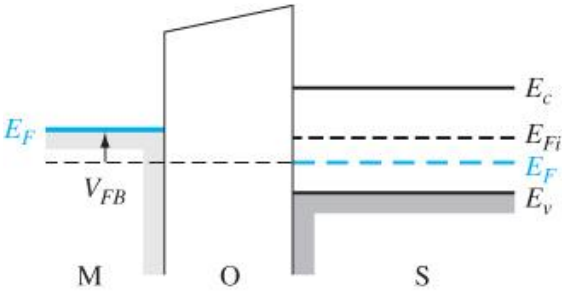


Figure 10.17 | Energy-band diagram of a MOS capacitor at flat band.

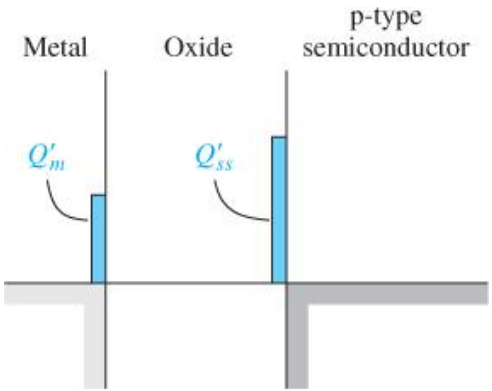


Figure 10.18 | Charge distribution in a MOS capacitor at flat band.

- Flat-Band Voltage: applied bias required such that there is no band bending in the semiconductor
- Bias needed to counteract $V_{ox0} + \phi_{ms}$
- If the oxide has some fixed charge (Q_{ss}') at the oxide-semiconductor interface, the flat-band voltage is given by

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}'}{C_{ox}}$$

- C_{ox} is the capacitance per unit area in the oxide
- With no charge in the oxide, the flat-band voltage is equal to the difference in work functions between the metal and semiconductor