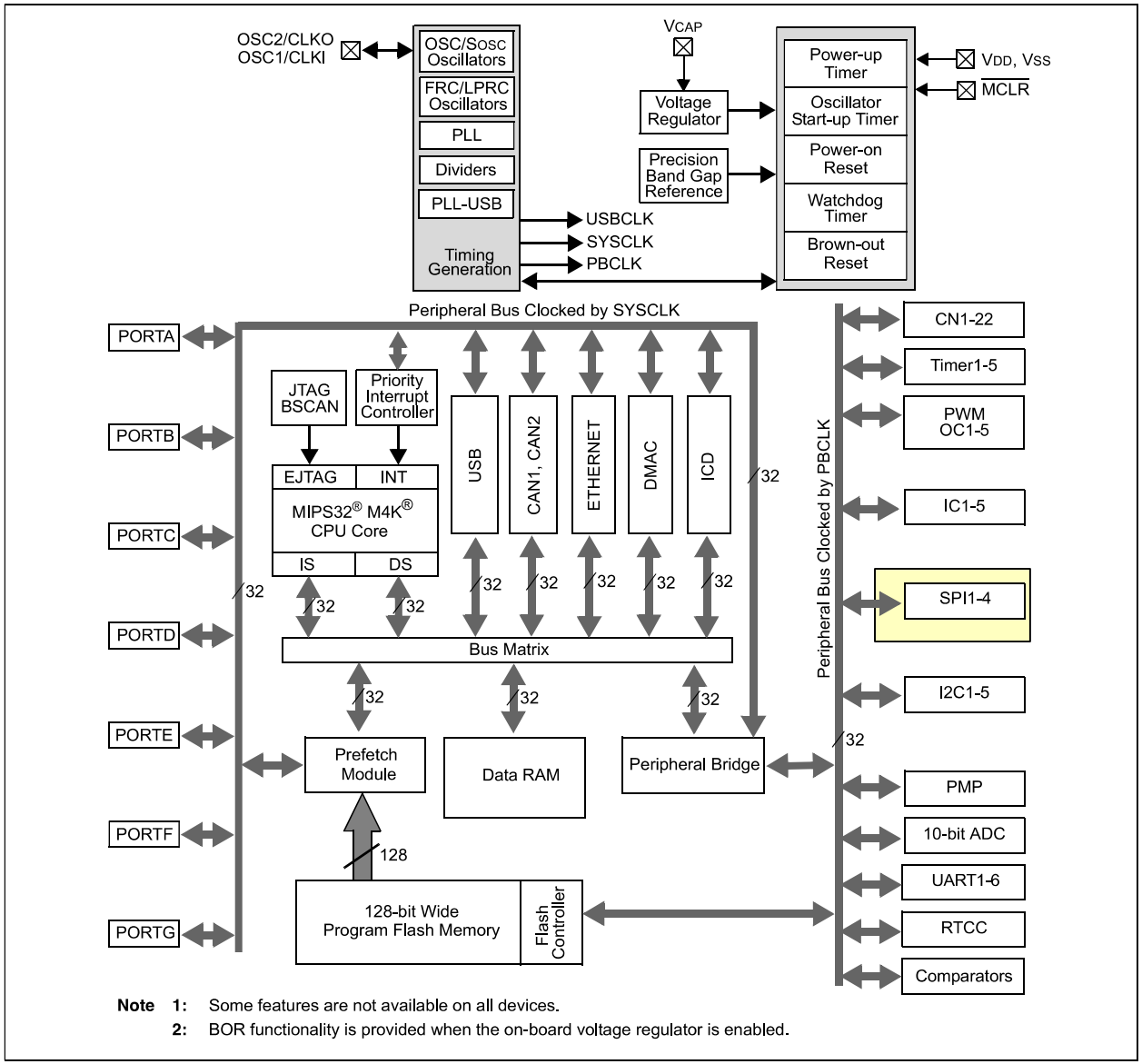
Serial Peripheral Interface (SPI)

Dr. Edward Nava
ejnava@unm.edu

PIC Architecture

FIGURE 1-1: BLOCK DIAGRAM(1,2)



Note 1: Some features are not available on all devices.

2: BOR functionality is provided when the on-board voltage regulator is enabled.

SPI Interface

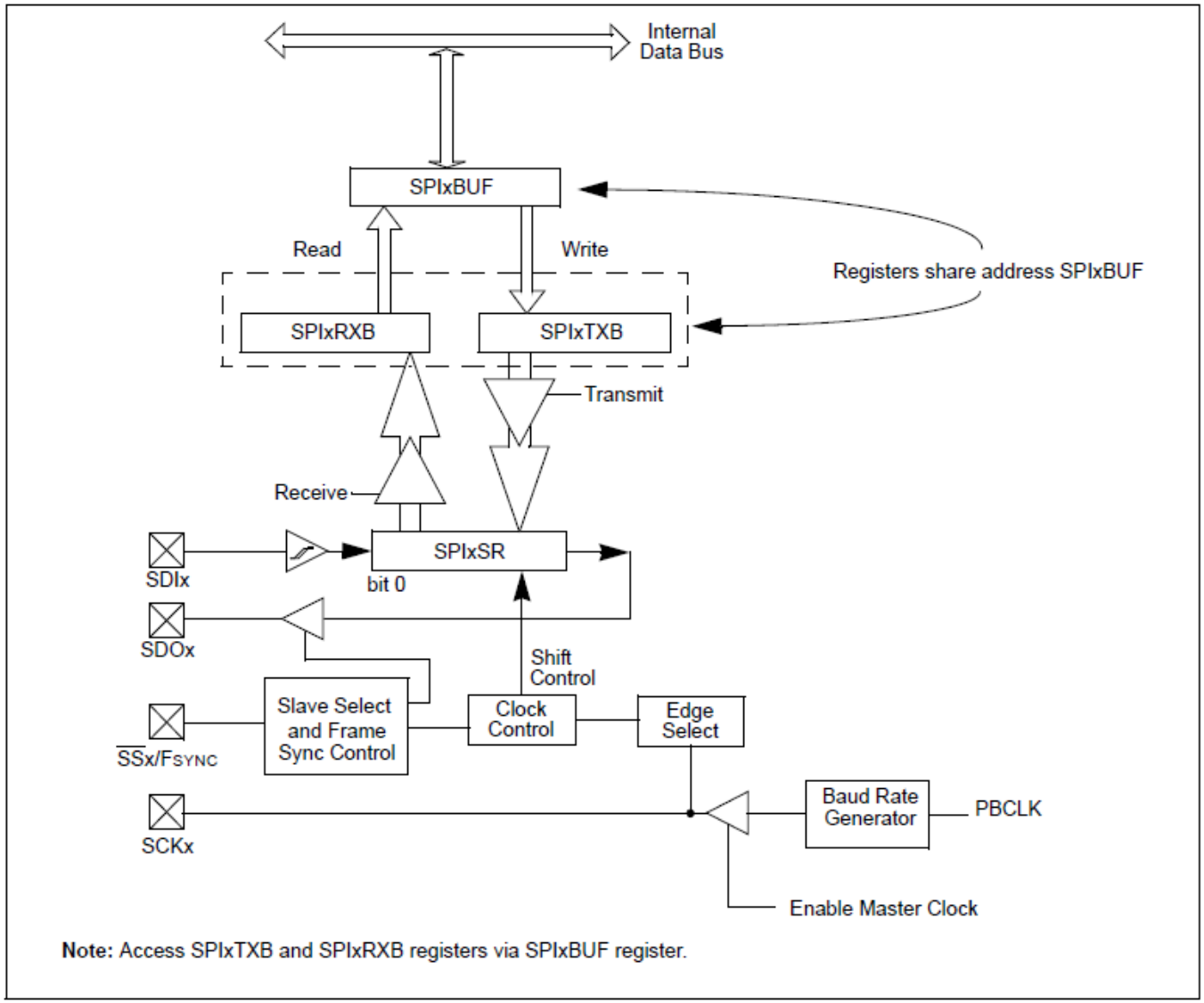
- **Characteristics**
  - It is the simplest serial Interface, but the PIC 32 version has many options.
  - Synchronous
  - Full Duplex communication
  - Uses a minimum of three signal wires, SDO, SDI and SCK
  - Can use a Slave Select (SSx) or Frame Sync signal
  - Is compatible with Motorola® SPI and SIOP interfaces.

SPI Interface

- **Features**
  - Can operate in either Master or Slave mode
  - Multiple clock formats
  - Supports framed SPI protocol
  - Has standard and enhanced buffering modes
  - User configurable data width of 8, 16, or 32 bits
  - Receive & Transmit FIFO buffers
  - Programmable interrupt modes

SPI Block Diagram

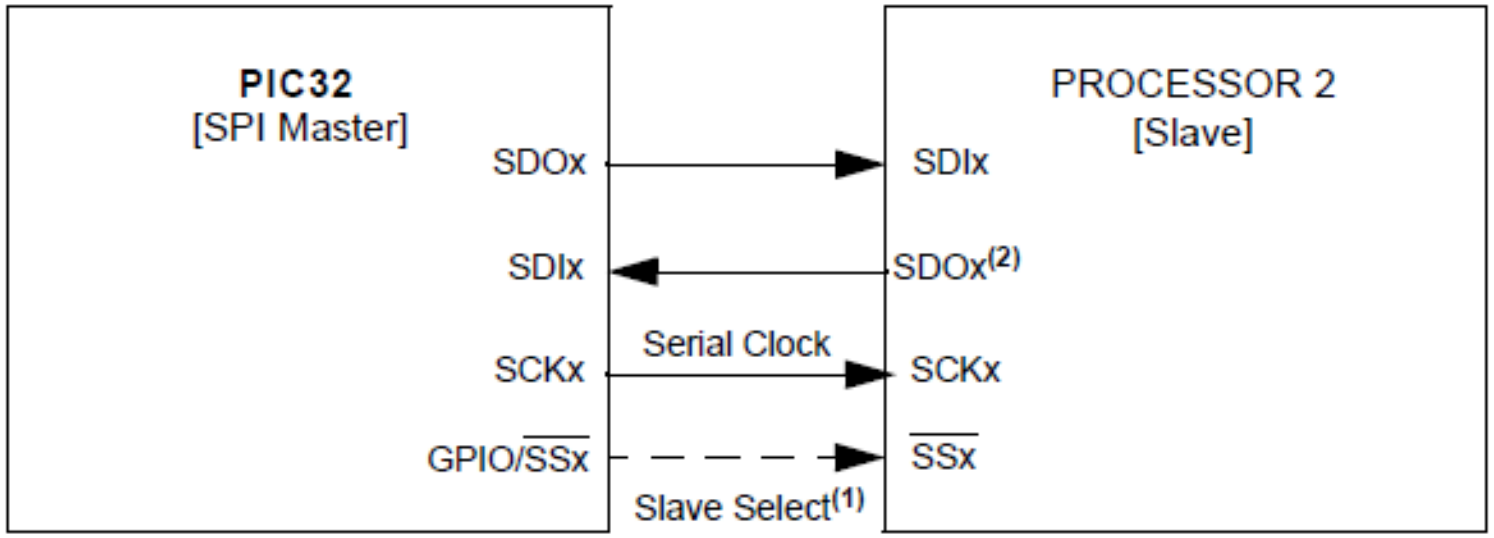
FIGURE 17-1: SPI MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB registers via SPIxBUF register.

SPI Link Configuration

Figure 23-2: Typical SPI Master-to-Slave Device Connection Diagram



Note 1: In Normal mode, the usage of the Slave Select pin ($\overline{SSx}$) is optional.
2: Control of the SDOx pin can be disabled for Receive-Only modes.

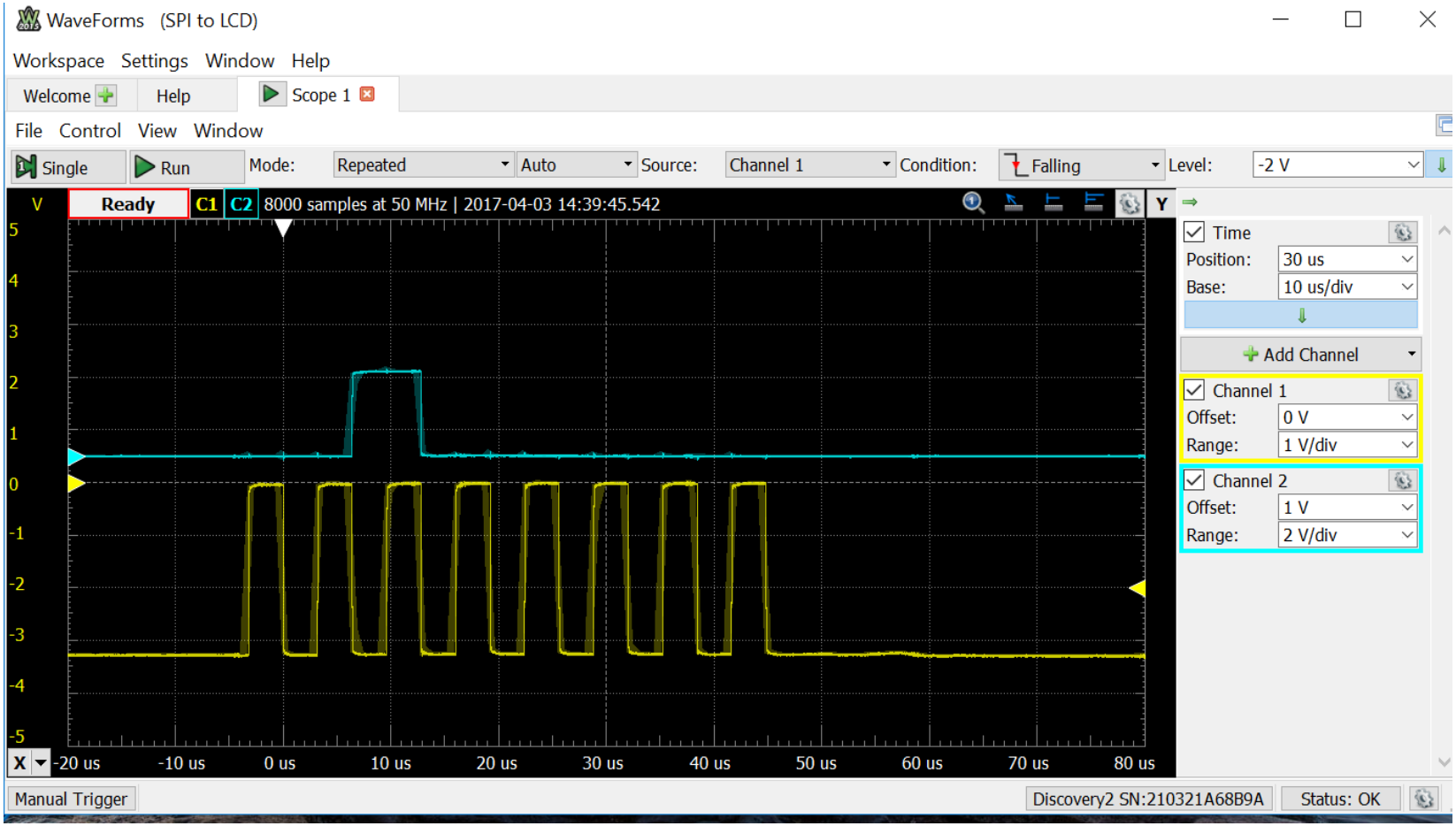
Using the SPI Interface

- For communication with the SPI Interface, data are written to and read from a single SPI*x*BUF register.
- The SPI*x*RXB (Receive) and SBI*x*TXB (Transmit) buffers are both accessed via the SPI*x*BUF register.
- The interface is basically a shift register, with bits simultaneously shifted in on the SDI*x* pin and out on the SDO*x* pin, in sync with clock on the SCK*x* pin.
- If configured as bus master, the transmitted clock is derived from the PBCLK.

SPI Communication Protocol

- When a slave device is enabled by a SS signal, the master device clocks data bits out of its shift register and into the shift register of the slave device.
- If data is being transmitted in both directions, the same clock is used by the slave device to shift data bits out of its shift register and into the shift register on the master device.
- For bidirectional data flow, a bit is shifted out of one end of a devices shift register at the same time a bit is shifted into the other end of the same shift register.
- As the master device controls all data transfers using the transmitted clock, no start or stop bits are necessary.

SPI Communication Protocol



Top signal is SDO and the bottom signal is SCK

PIC32 SPI Interfaces on MX7

- The PIC32 microcontroller has four SPI interfaces
- Three SPI interfaces are accessible on the MX-7 development board, SPI1, SPI3, & SPI4
- SPI1 signals are accessible via connector JD

SPI SFRs

TABLE 4-12: SPI1-2 REGISTERS MAP(1,2)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5810	SPI1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0008
5820	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5830	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0008
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5A10	SPI2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: SPI2 Module is not present on PIC32MX420FXXXX/440FXXXX devices.

SPI Baud Rate

- **From Table 32-28 of the PIC data sheet, we see that the minimum period for SCK is 40nS, which corresponds to a clock of 25Mhz.**
- **In our system, PBCLK is 10MHz, which is acceptable.**
- **The baud rate we select will be constrained by the timing requirements of the external devices connected to the SPI interface.**
- **For our applications, we will configure SCK to 156.25 KHz.**
- **The Baud rate values are found in Section 23 of the PIC Reference manual in table 23.4. This is in the section 23.3.7 - SPI Master Mode Clock Frequency.**