Inter-Integrated Circuit Interface (I2C or I^2C)

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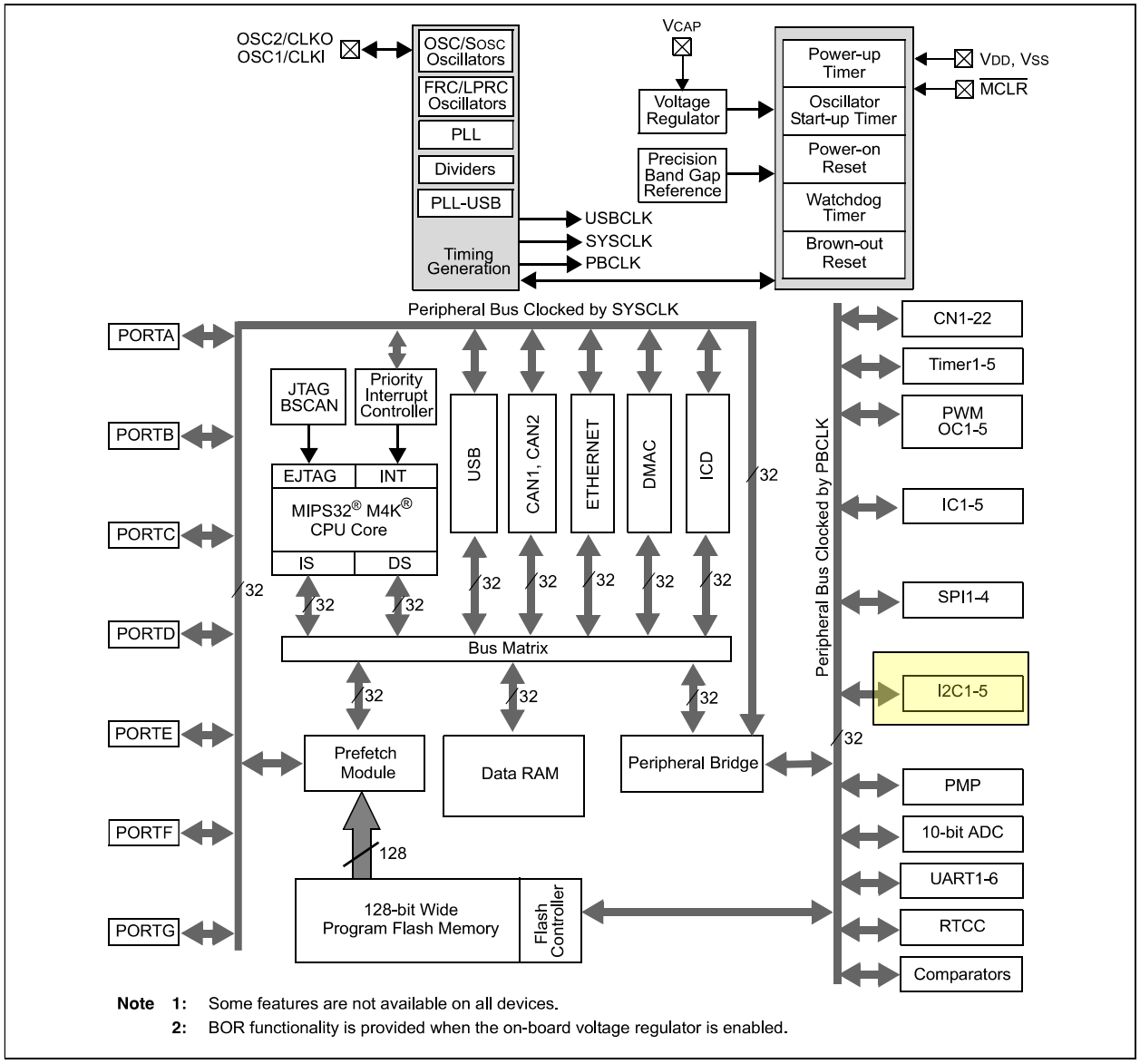
PIC Architecture

FIGURE 1-1: BLOCK DIAGRAM(1,2)



Note 1: Some features are not available on all devices.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

I^2C Interface

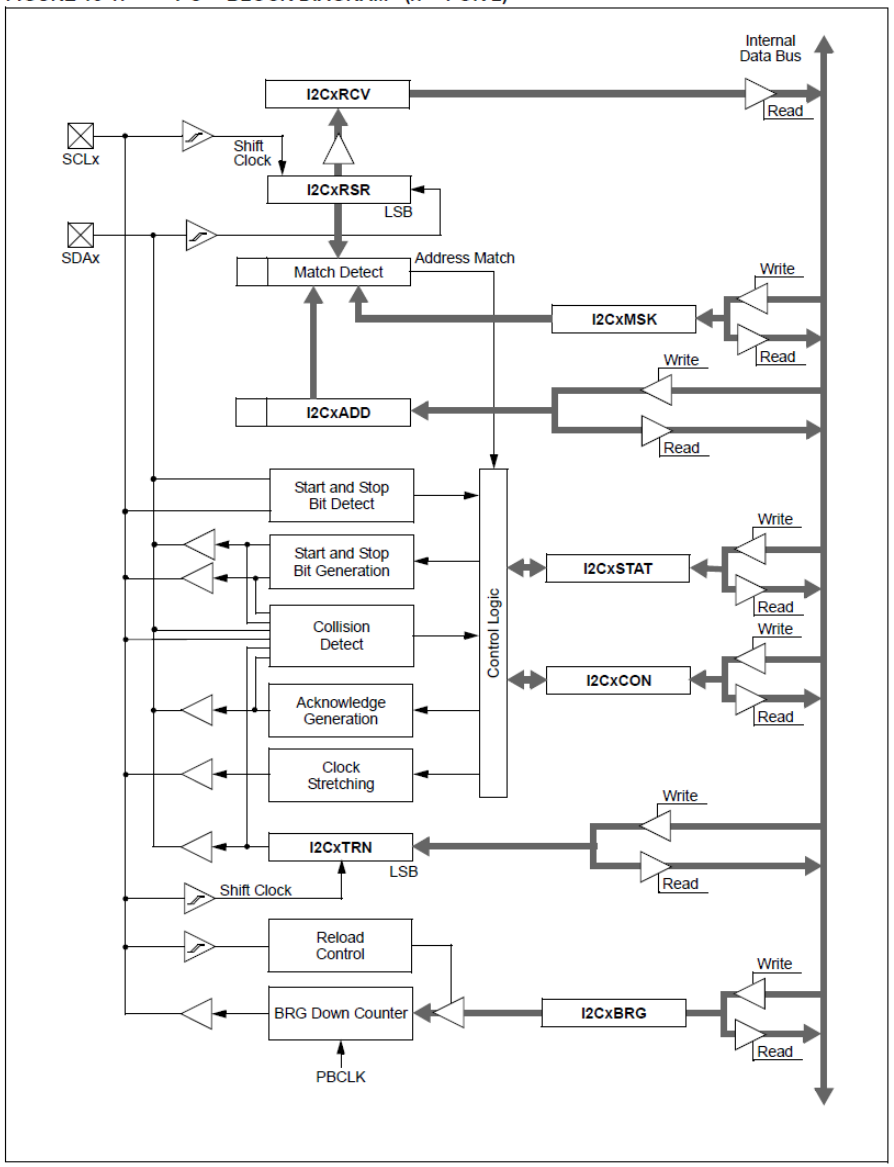
- **Characteristics**
  - Synchronous
  - Half Duplex communication
  - Uses a minimum of two signal wires, SDA and SCL
  - Serial Transmission

I^2C Interface

- **Features**
  - Can operate in either Master or Slave mode
  - Supports 7 or 10 bit addresses in both Master and Slave modes
  - Allows for bidirectional data transfers
  - Can suspend and resume serial transfers using serial clock synchronization
  - Supports multi-master operation – detects bus collisions and arbitrates accordingly
  - Provides support for address bit masking

I²C Block Diagram

FIGURE 18-1: I²C™ BLOCK DIAGRAM (x = 1 OR 2)



I^2C Communication

- With an I^2C communication link, multiple devices can assert a signal on the shared data line, so coordination of the transmissions is required.
- Unlike SPI, which uses a hardware signal to select which slave device should receive and/or transmit a message, I^2C requires that the address of the slave is transmitted on the data line as the first part of the communication.

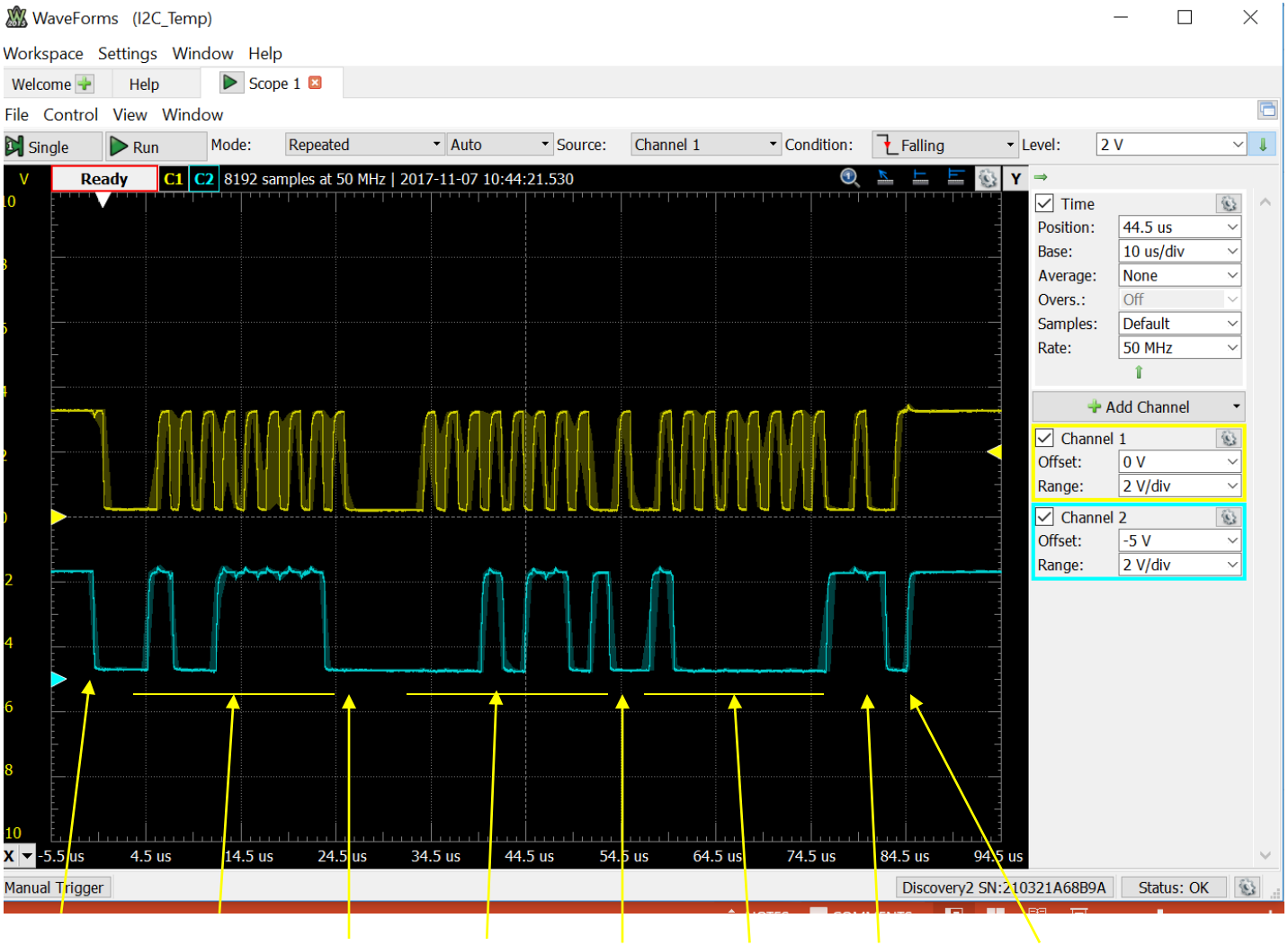
I^2C Communication Protocol

- The I^2C bus must not be busy before any data can be sent over the bus.
- Both the SCL and SDA lines are high when the bus is not busy.
- A start bit is identified by a high to low transition of the SDA line while SCL is high.
- One bit of data is transferred during each clock pulse:
  - Data on the bus must be stable while the clock line is high.
  - Data can change while the clock line is low.
- Each transmission of 8 data bits is followed by an acknowledgement cycle.
- The ACK signal is identified by a device lowering the SDA line during the ACK clock pulse.

I²C Communication Protocol

- A master receiver must signal the end of the data to the transmitter by not lowering the SDA line during the ACK clock high pulse (*A Negative Acknowledgement* – NACK). Then the transmitter leaves the SCL line high so that the master can generate the Stop bit.
- The Stop bit is identified by a low to high transition of the SDA line while the SCL line is high.

I2C Waveform



Start data Slave ACK data Master ACK data Master NACK Stop

PIC32 I2C Interfaces on MX7

- The PIC32 microcontroller has five I2C interfaces
- Four SPI interfaces are accessible on the MX-7 development board. I2C1 and I2C2 are accessible via daisy-chain connectors J7 and J8, respectively.
- On the MX-7 board, a serial EEPROM is connected to I2C2.
- To minimize conflicts, we will use I2C1.
- I2C3 and I2C4 signals are acessible via PMOD connectors JE and JF.

SPI SFRs

TABLE 19-1: I2C1THROUGH I2C5 REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5230	I2C5MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5240	I2C5BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5250	I2C5TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5260	I2C5RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
5300	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5310	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5320	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5330	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5340	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5350	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5360	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
5400	I2C2CON(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5410	I2C2STAT(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5420	I2C2ADD(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5430	I2C2MSK(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5440	I2C2BRG(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5450	I2C2TRN(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
5460	I2C2RCV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: This register is not available on 64-pin devices.

Usage Details

- When the master transmits a 7-bit address to a slave device, the seven address bits are shifted to the left one position. Then, the least significant bit is set to either 0 or 1 to indicate that data will be written to the slave or read from the slave, respectively.