ECE 322L Electronics 2

01/21/20 - Lecture 1
Course Introduction

General Information

ECE 322 L – Electronics 2

- Semester: Spring 2020
- Class Time: T-R 11:00 am 12:15 pm
- Class Location: CENT 1026
- Class Website: https://learn.unm.edu
 - Syllabus
 - Rubric
 - Announcements
 - Lecture slides
 - Homework
 - Homework and exam solutions
 - Lab assignments & design project
 - Additional materials

About me





TECHNISCHE UNIVERSITÄT CHEMNITZ

MS in Electrical Engineering 2004

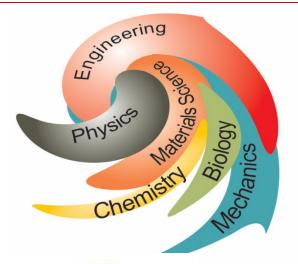
PhD in Electrical Engineering and Information Technology 2009



Courses: ECE 213, 371, 322L, 570, independent studies

A convergent research program

We engineer materials' attributes and device characteristics to implement novel or improved functionality in condensed matter.



- Thrust 1
 Synthesis of inorganic sheets
- Thrust 2
 Assembly of inorganic sheets
- Thrust 3
 Engineering heterogeneous materials





Office of Science

Additional personnel

Teaching assistant

Rahul Jaiswal (<u>rahulj@unm.edu</u>)

Lab manager

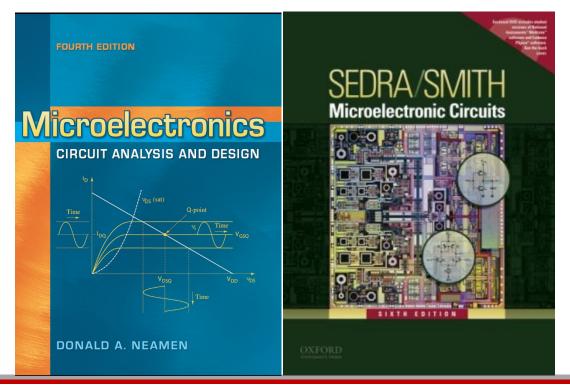
David Modisette (<u>dmodiset@unm.edu</u>)

Additional personnel

- Your name
- Your stage within the undergraduate program
- What are you hoping to learn in this course.

Textbook and Reference Material

- Microelectronics circuit analysis and design by Donald A. Neamen, 4th Edition, McGraw Hill (*TEXTBOOK*).
- Microelectronics circuits by Sedra and Smith, 6th Edition,
 Oxford Series in Electrical & Computer Engineering
- Class notes and handouts.



Assessment

Homework Policy

Homework will be posted on UNM Learn every Thursday and it will be due a week later (the following Thursday) by 11 am. Late submissions will MOT be accepted. The class TA will ensure that you get your homework back by the following Tuesday. Homework solutions will be posted on

UNM Learn.

Grading:

Homework: 15%

2 Mid-Term Examinations: 20%

Lab reports 15%

Design Problem: 30%

Final Examination: 20%

There will be no curving of the grades.

Class participation will count as extra-credit I will grade class participation between 0 and 60.

- The extra-credit score will be multiplied by the following factor:

- (100-Final grade w/o extra-credit)/100.
- -The result will then be added to your final grade

A-:	88-91.99
B+:	84-87.99
B:	80-83.99
B-:	76-79.99
C+:	72-75.99
C:	68-71.99
C-:	64-67.99
D:	60-63.99

A:

96-100

92-95.99

00 04 00

Below 60

Important Dates

Important Dates:

- Mid Term I: Tuesday, Feb 18th, 2020 (11:00 AM-12:15PM-Place: CENT 1026)
- Mid Term II: <u>Tuesday, March 31st, 2020</u> (11:00 AM-12:15PM-Place: CENT 1026)
- All lab reports are due: Friday, April 3rd, 2020 at 5 PM (Please, e-mail a copy to the TA)
- Final Examination: <u>Tuesday, May 12th, 2020</u> (12:30PM-2:30PM-CENT 1026)

Top Six Ways to Avoid an A grade

- ➤ Skip lectures
- Being passive during lectures
- Don't ask questions in class/exams/lab sessions/office hours
- Don't attend labs
- Don't review slides, reading material, HW solutions, sample problems and solutions
- > Work on the design project at the last minute.

Educational Objectives of This Class

Bloom's Taxonomy of Educational Objectives

Creating

Evaluating

Analyzing

Applying

Understanding

Remembering

designing, constructing, inventing, devising...

hypothesizing, judging, checking, critiquing...

organizing, structuring, outlining, integrating...

using, implementing...

summarizing, inferring, interpreting, comparing...

recognizing, listing, naming, identifying...

Higher Order Skills

Educational Objectives (Bloom)

1. Remembering (Knowledge)

Recalling material you have learned. Remembering facts, principles, steps in a sequence, etc.

2. Understanding (Comprehension)

Understanding the material. At this stage you should be able to explain what you know, translate to new forms & symbols and extrapolate.

3. Applying (Application)

At this stage you should be able to use the material in new situations, that is apply concepts, principles, rules, theories and laws to find solutions to new problems - problems you haven't seen before.

4. Analyzing (Analysis)

At this level you should be able to break things apart so that relationships are understood. For example, you might analyze an amplifier circuit using what you learn about transistors.

5. Evaluating (Evaluation)

Here you should be able to use what you know about a subject area to make critical judgments, rate ideas or objects and to accept or reflect materials based on standards. The key skill is the ability to make judgments.

6. Creating (Synthesis)

You should be able to put together parts to form a new whole. Engineers do this when they write proposals, design new products, etc.

Problem Based Learning



"I think it's an exaggeration, but that there's a lot of truth in saying that when you go to school, the trauma is that you must stop learning and you must now accept being taught."

- Seymour Papert

- You will be expected to read the book and review slides before the lectures.
- Lectures will mostly consist of problem solving exercises, which is best to undertake as a part of a team.
- Sit together with your team members in the class

Make the Informal Group Structured Problems Drive Lectures Active Activities Team Activities the Course

> Instructor Centered

Active Learning

Collaborative Learning Student Centered

Cooperative Problem Based Learning Learning

Labs

No lab this week. However, I am requesting you all to meet with the TA on Wed at 3:30 pm in ECE311. The purpose of the meeting is to make arrangements for future lab sessions.

Lab: Rm ECE 311

- Mondays, 15:30-18:00 (Sect 001);
- Wednesdays 15:30-18:00 (Sect 003).

These times may change upon tomorrow's meeting. One intro lab (Next week), 7 labs to familiarize yourself with FET and BJT operation and to build complex circuits, 5 open labs to finalize your design project.

Design Project

- It will be on UNM Learn starting next week
- Involving Spice modeling and building an audio amplifier
- Due at the end of the semester
- Team project
- The roles of each team member should be rotated during the course of the project.

Team Contract: All the teams are required to develop a 1-2-page team contract that clearly states, among other things, the roles and responsibilities of each member, conflict resolution techniques, by which mean the team members will exchange information, a data storage plan, etc. The team contract, duly signed by all team members, will be due on 03/26/2020-11 am.

This course focuses on analog signals





- More accurate

 More affected by noise

- Continuous
- Infinite range of values

Digital signals



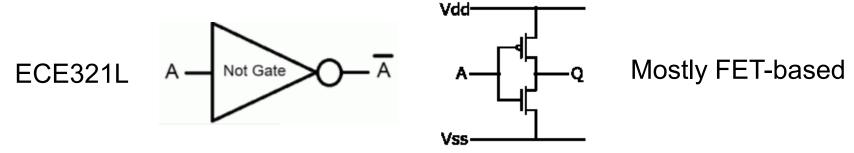
- Less accurate
- Less affected by noise
- Allows storing more info in a smaller space
- More secure

- Discrete
- Finite range of values (Typically 2)

Both type of signals can be generated, transmitted and processed using the same bunch of electronic components

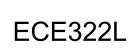
Digital electronic circuits process discrete signals

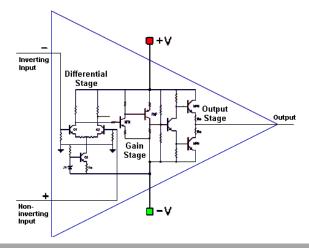
Main function of digital electronic circuit is to implement boolean algebra through logic gates (NOT, AND, XOR,...)



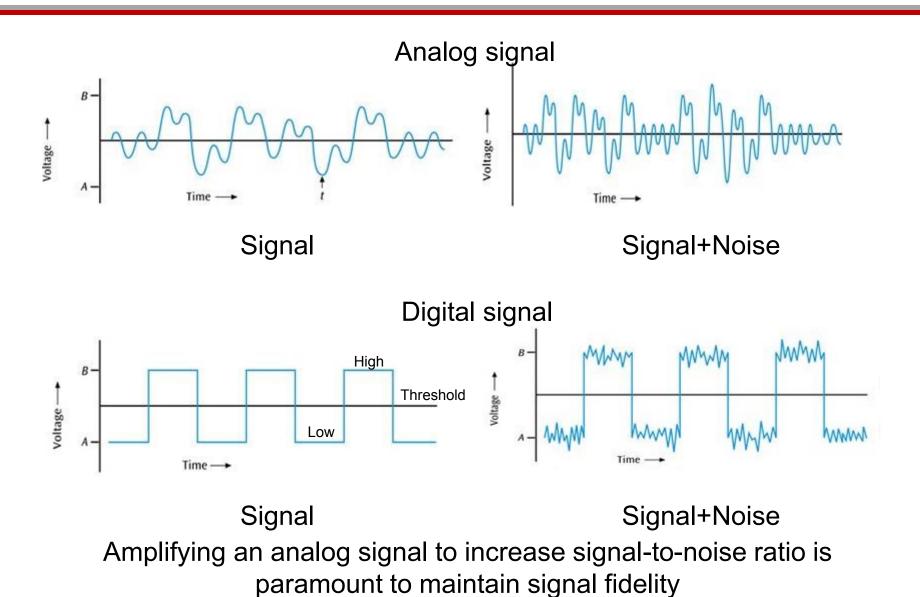
Analog electronic circuits process continuous signals

Main function of analog electronic circuits is signal amplification and filtering





Mostly BJT-based



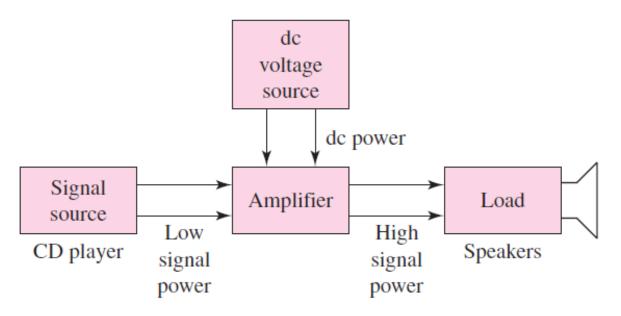
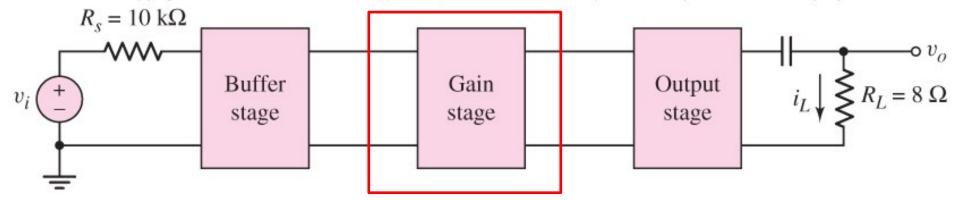
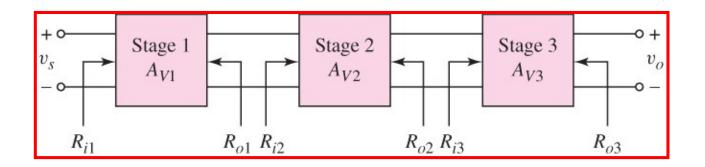


Figure PR1.1 Schematic of an electronic circuit with two input signals: the dc power supply input, and the signal input

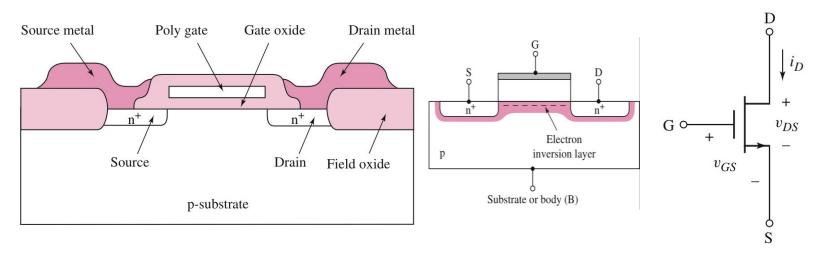
Block diagram of an amplifier (Ch. 6)

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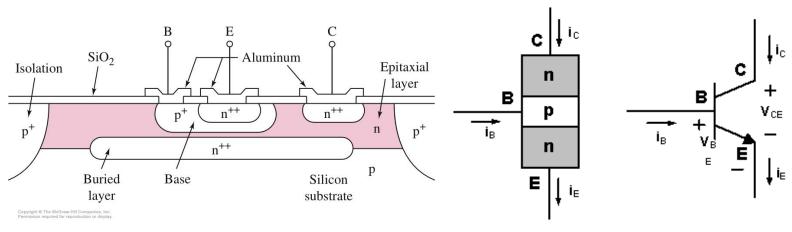




Field effect transistors (FETs, Ch 3 and 4)



Bipolar Junction Transistors (BJTs, Ch 5 and 6)



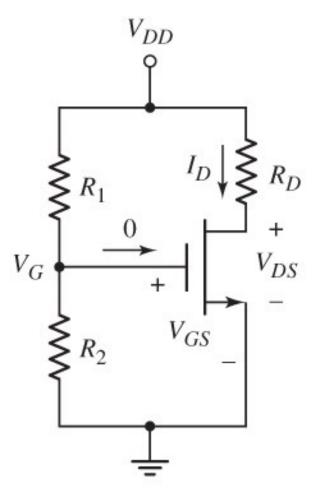
- Module 0: Course Overview and Key Concepts (Learning Objectives, Key concepts from the four modules, Lab preparation and expectations, design project overview) (Lecture Notes)
- ➤ Module 1: Field Effect Transistors and Amplifiers: Operation of a MOSFET, NMOS, PMOS, CMOS, DC/AC Analysis, JFETs, Applications, MOSFET Amplifier, DC/AC Load Line Analysis, AC Equivalent Circuit, CS, CD, CG Amplifiers (Chapters 3 and 4)
- ➤ Module 2: Bipolar Junction Transistors and Amplifiers: Operation of a BJT, DC/AC Analysis, Transistor Biasing, Linear Amplifier, DC/AC Load Line Analysis, AC Equivalent Circuit, CE, CC, CB Amplifiers (Chapters 5 and 6)
- ➤ Module 3: Frequency Response: Amplifier Frequency Response, Transfer Functions, Bode Plot, Frequency Response of BJT and FETs, Miller Effect, Transistor Circuits (Chapter 7)
- Module 4: Power Transistors: Power amplifiers, BJT and MOSFET Power transistors, Classes of Amplifiers, Circuit configurations (Chapter 8)

Learning Outcomes of the Course

At the end the course, you should be able to:

- Analyze the operation of FETs and determine the DC/AC response of the FET
- Design and analyze the response of various MOSFET functional circuits such as amplifiers (CS, CG, CD, etc), using AC/DC load line analysis.
- Analyze the operation of a BJT and determine the DC/AC response of the BJT.
- Design and analyze the response of various BJT functional circuits such as amplifiers (CE, CC, CB, cascade, cascode, Darlington pair, etc), using AC/DC load line analysis.
- Construct Bode plots of the gain magnitude and phase of various amplifier circuits taking into account circuit capacitors and time constants and determine their frequency response.
- Determine the short circuit gain versus frequency of a BJT and the unity gain bandwidth of an FET and determine their Miller capacitances using the expanded hybrid-p model
- Analyze and design various circuit configurations of power transistors and amplifiers.
- Work together in a team and evaluate/assess your individual performance and the performance of your teammates.

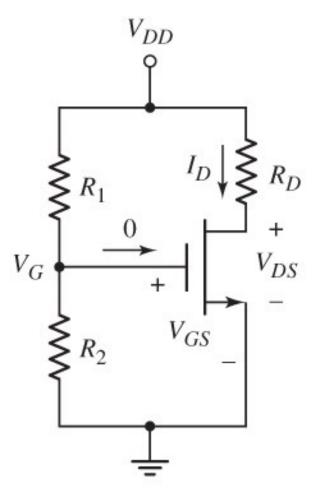
In-class question 1



Consider the circuit shown in this page. When $V_{GS}=0$, the transistor is in

- (A) Cut-off
- (B) Saturation
- (C) Non-saturation
- (D) Breakdown

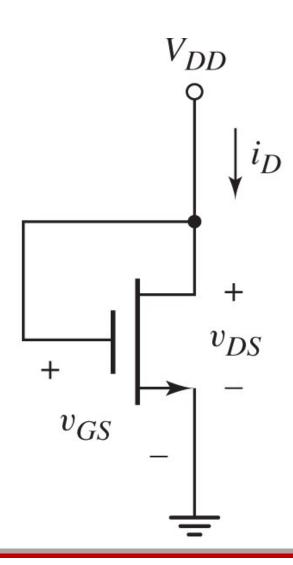
In-class question 1, Soln.



Consider the circuit shown in this page. When $V_{GS}=0$, the transistor is in

- (A) Cut-off
- (B) Saturation
- (C) Non-saturation
- (D) Breakdown

In-class question 2

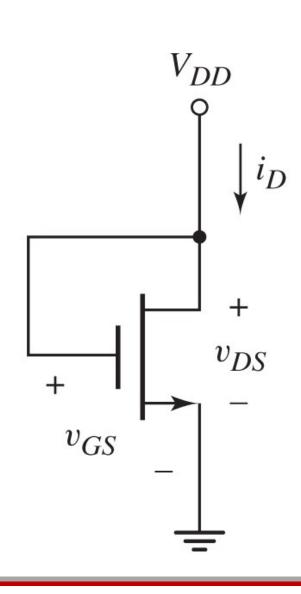


Consider the transistor shown in this figure. Is this transistor in

- (A) Cut-off
- (B) Non-saturation
- (C) Saturation
- (D) Depends on the value of V_{DD}

$$V_{DD}>V_{TN}$$

In-class question 2, Soln.



Consider the transistor shown in this figure. Is this transistor in

- (A) Cut-off
- (B) Non-saturation
- (C) Saturation
- (D) It depends on the value of $V_{\rm DD}$

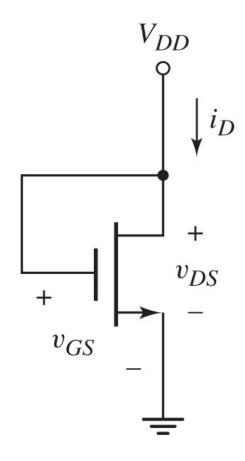
Because
$$V_{DS}=V_{GS}>V_{GS}-V_{TN}=V_{DS}(Sat)$$

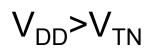
 $V_{DS}>V_{TN}$

$$V_{DD}>V_{TN}$$

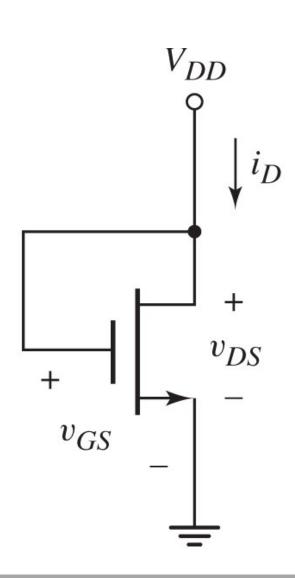
In-class question 3

Consider the transistor shown in this figure. Sketch the $\sqrt{i_D} \ vs. \ v_{GS}$ characteristic for the transistor below.





In class question 3, Soln.



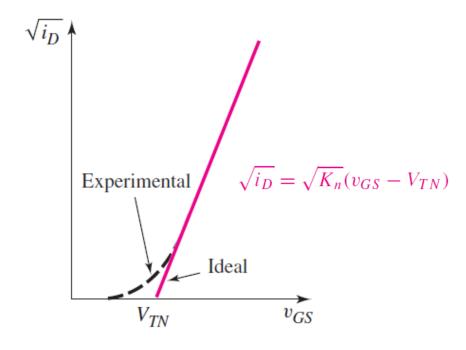
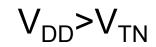
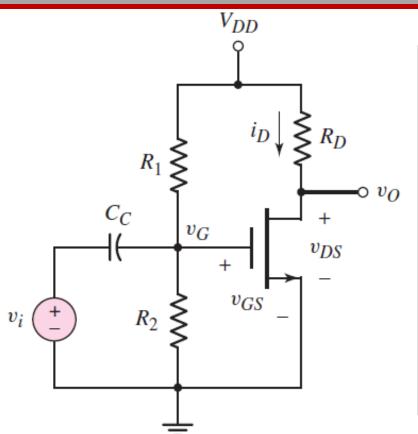


Figure 3.23 Plot of $\sqrt{i_D}$ versus v_{GS} for a MOSFET biased in the saturation region showing subthreshold conduction. Experimentally, a subthreshold current exists even for $v_{GS} < V_{TN}$.



In-class question 4

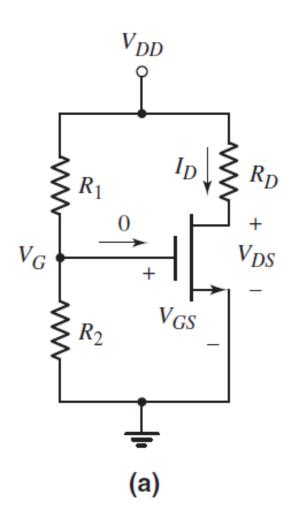


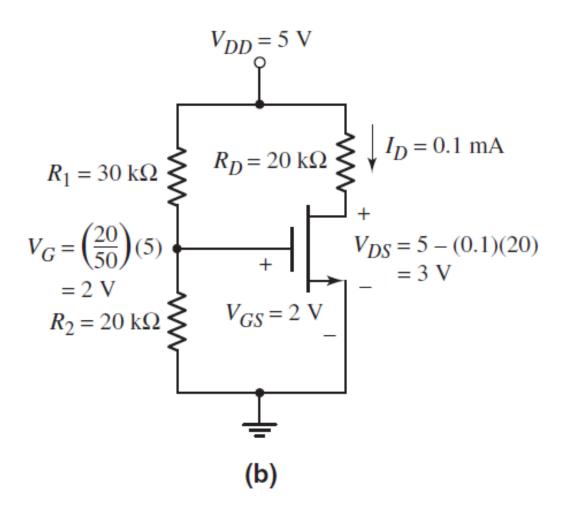
Region	NMOS
Nonsaturation	v _{DS} <v<sub>DS(sat)</v<sub>
	$i_D = K_n [2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$
Saturation	v _{DS} >v _{DS} (sat)
	$i_D = K_n [v_{GS} - V_{TN}]^2$
Transition Pt.	$V_{DS}(sat) = V_{GS} - V_{TN}$
Enhancement Mode	V _{TN} > 0V
Depletion Mode	V _{TN} < 0V

For the circuit shown in Figure 3.25(a), assume that $R_1 = 30 \,\mathrm{k}\Omega$, $R_2 = 20 \,\mathrm{k}\Omega$, $R_D = 20 \,\mathrm{k}\Omega$, $V_{DD} = 5 \,\mathrm{V}$, $V_{TN} = 1 \,\mathrm{V}$, and $K_n = 0.1 \,\mathrm{mA/V^2}$.

Determine the operating point of the MOSFET in DC Which operating region is the MOSFET in?

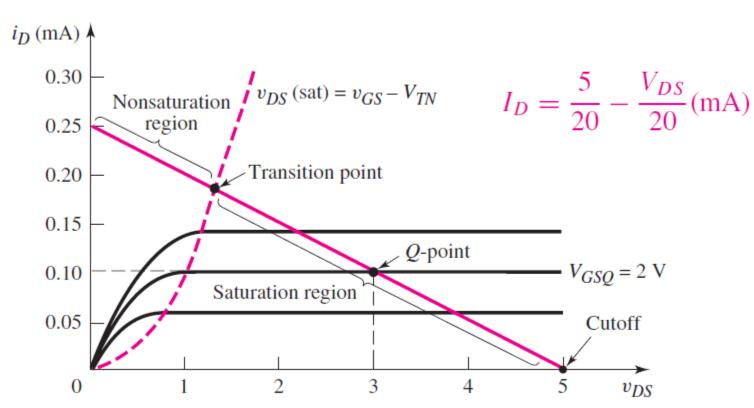
In-class question 4, Soln.





In-class question 4, Soln.

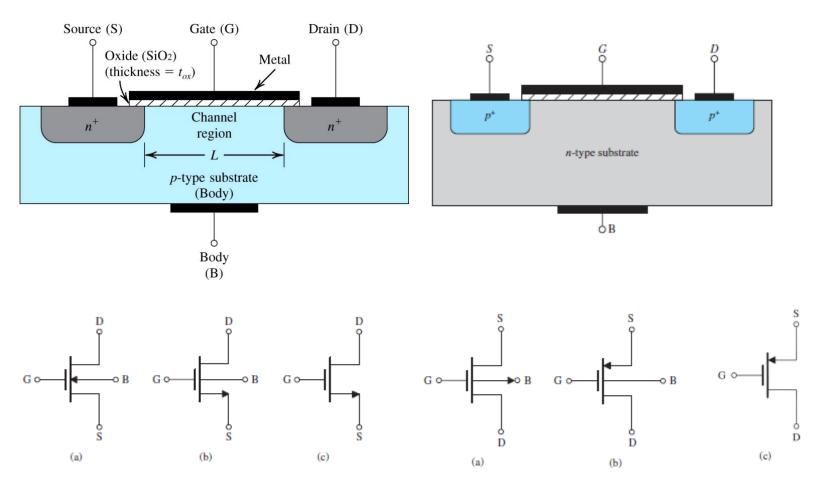
$$V_{DS} = V_{DD} - I_D R_D = 5 - I_D(20)$$



In-class question 5

Sketch the physical structure of an enhancement NMOS and an enhancement PMOS transistor.

In-class question 5, Soln.



Electron inversion channel Positive threshold voltage

Hole inversion channel Negative threshold voltage

Overview of Lecture 2 & References

- ➤ Review of MOSFET behavior (Neamen-3.1, S&S-5.1-5.2)
- ➤ Transistor as amplifier (S&S 5.4.1-5.4.4)
- Intro to DC analysis of transistor behavior

Q-point

Load-line

(Neamen 3.2, S&S 5.4.5-5.4.6)

Please see the lecture 2 slides on UNM learn.