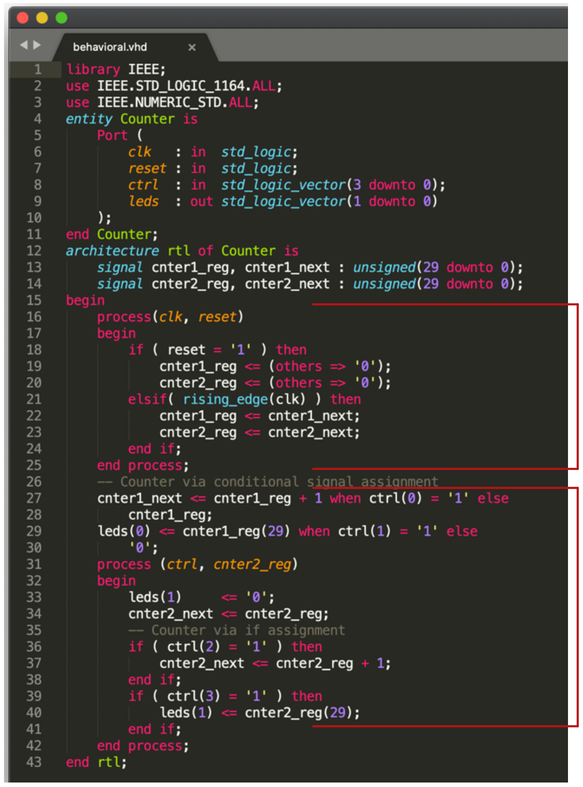
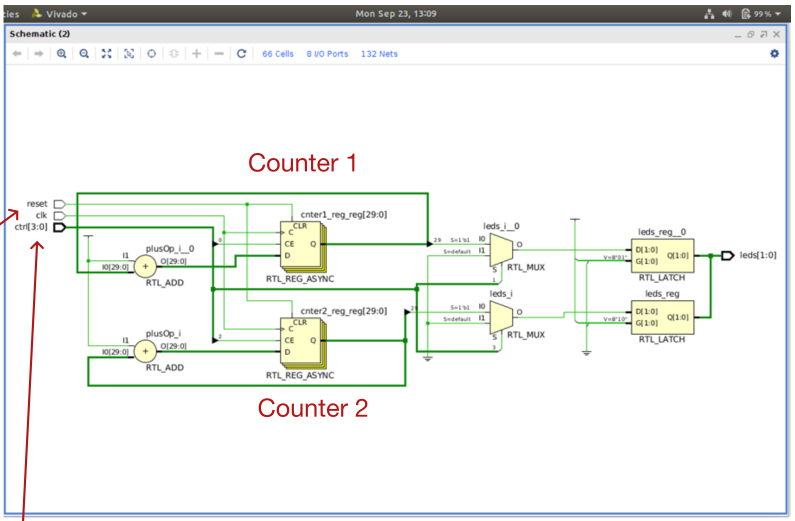
ECE338
Lab #4: Behavioral-to-Schematic Translation, Counter
David Kirby

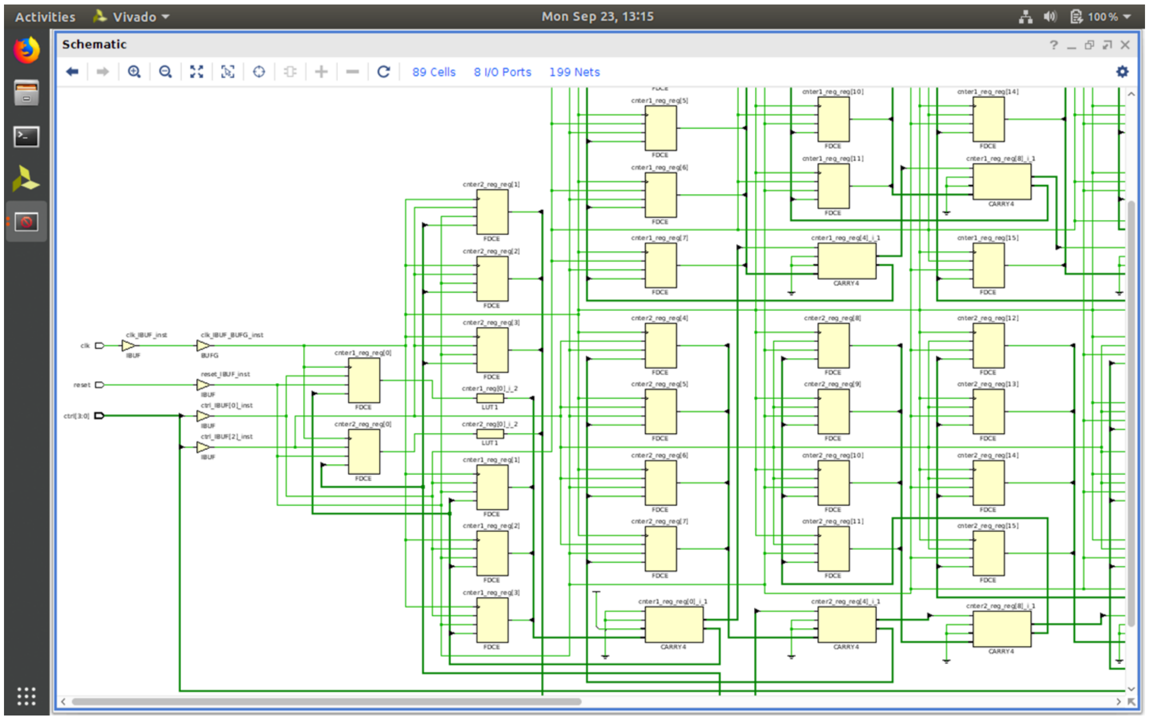
For Lab #4 we were tasked with implementing a set of counters within a process block. We used the switches on the Zybo board to toggle which counters to increment. The RTL Elaborated Design shows the counters, MUXs, and output to LEDs.



```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity Counter is
    Port (
        clk   : in  std_logic;
        reset : in  std_logic;
        ctrl  : in  std_logic_vector(3 downto 0);
        leds  : out std_logic_vector(1 downto 0)
    );
end Counter;
architecture rtl of Counter is
    signal cnter1_reg, cnter1_next : unsigned(29 downto 0);
    signal cnter2_reg, cnter2_next : unsigned(29 downto 0);
begin
    process(clk, reset)
    begin
        if ( reset = '1' ) then
            cnter1_reg <= (others => '0');
            cnter2_reg <= (others => '0');
        elsif( rising_edge(clk) ) then
            cnter1_reg <= cnter1_next;
            cnter2_reg <= cnter2_next;
        end if;
    end process;
    -- Counter via conditional signal assignment
    cnter1_next <= cnter1_reg + 1 when ctrl(0) = '1' else
        cnter1_reg;
    leds(0) <= cnter1_reg(29) when ctrl(1) = '1' else
        '0';
    process (ctrl, cnter2_reg)
    begin
        leds(1)     <= '0';
        cnter2_next <= cnter2_reg;
        -- Counter via if assignment
        if ( ctrl(2) = '1' ) then
            cnter2_next <= cnter2_reg + 1;
        end if;
        if ( ctrl(3) = '1' ) then
            leds(1) <= cnter2_reg(29);
        end if;
    end process;
end rtl;
```



In the Synthesized Design Schematic, the counter is shown as well as each separate incrementation. This produces a low-level, if not convoluted, view of our behavioral VHDL code.


Schematic
89 Cells
8 I/O Ports
199 Nets
clk
reset
ctrl[3:0]
clk_IBUF_inst
clk_IBUF_BUFG_inst
BUFG
IBUF
FDCE
CARRY4
LUT1