ECE 371
Materials and Devices

12/3/19 - Lecture 25

Ch. 10 – MOS Capacitor, Flat-Band Voltage, Threshold Voltage

General Information

- Homework 8 assigned, due on Thursday 12/5
- Final Exam (Tuesday 12/10, 12:30pm-2:30pm, cumulative but focused on ch. 7,8,10)
- Example final exam posted
- Review session Friday 12/6 at 3:30 pm in CHTM 103. I will record the session and post on the website.
- Reading for next time: 10.3

Threshold Inversion Point

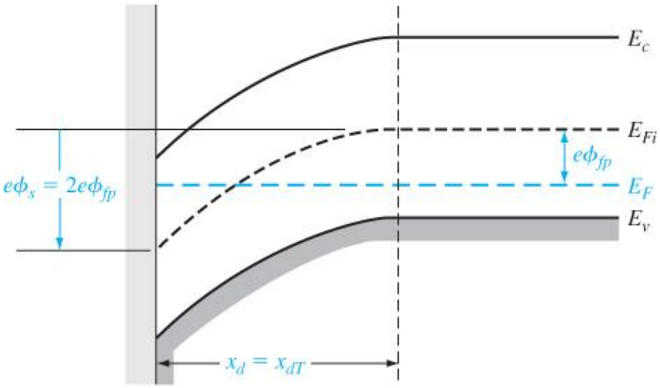


Figure 10.9 | The energy-band diagram in the p-type semiconductor at the threshold inversion point.

Maximum Depletion Widths

p-type

$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{Fp}}{eN_a}\right)^{\frac{1}{2}}$$

n-type

$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{Fn}}{eN_d}\right)^{\frac{1}{2}}$$

- Threshold Inversion Point: when the electron concentration at the surface is the same as the hole concentration in the bulk (p-type substrate)
- Occurs when $e\phi_s = 2e\phi_{Fp}$ (p-type) and $e\phi_s = 2e\phi_{Fn}$ (n-type)
- The depletion region width practically reaches a maximum at the threshold inversion point since the electron inversion layer "screens" any additional voltage applied to the gate from adding electric field to the semiconductor

Threshold Inversion Point

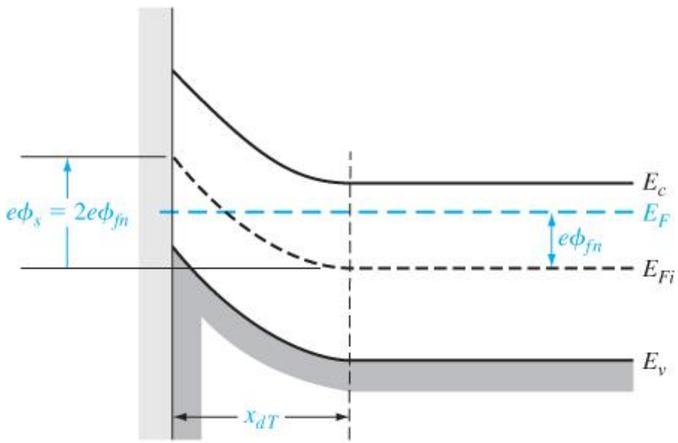


Figure 10.10 | The energy-band diagram in the n-type semiconductor at the threshold inversion point.

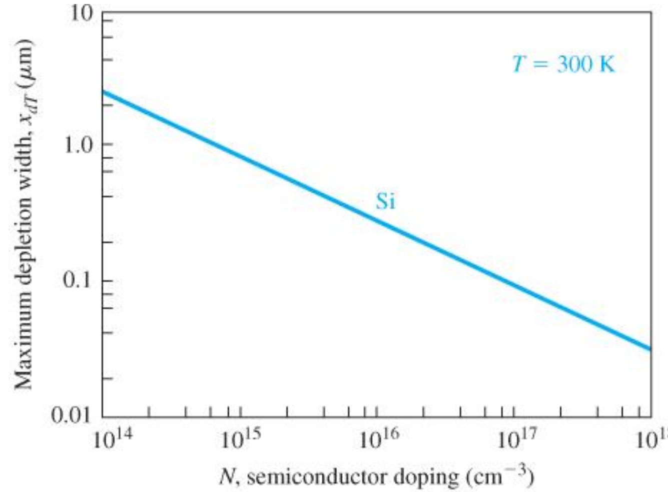


Figure 10.11 | Maximum induced space charge region width versus semiconductor doping.

- Similar condition exists for n-type substrates ($e\phi_s = 2e\phi_{Fn}$) when the hole concentration at the surface becomes equal to the electron concentration in the bulk
- The depletion width is inversely proportional to the square root of the doping concentration

Surface Charge Density

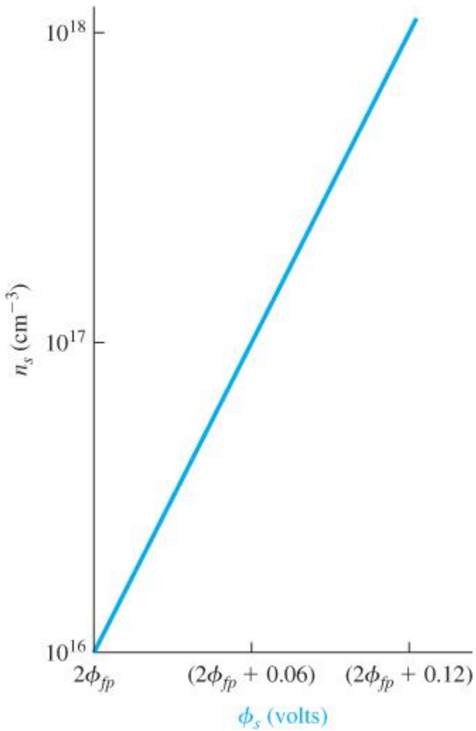


Figure 10.12 | Electron inversion charge density as a function of surface potential.

- How does the surface charge density (n_s) change as a function of change in surface potential ($\Delta\phi_s$)?

$$\boxed{n_s = n_{st} exp\left(\frac{\Delta\phi_s}{V_t}\right)}$$

surface charge density

- $\Delta\phi_s$ is the change in surface potential beyond the threshold inversion point
- n_{st} is the surface electron density at the threshold inversion point
- Inversion charge density increases very rapidly with a small increase in surface potential
- Screens gate charge → depletion width constant beyond inversion

Before : if bias applied = band bending
if no bias = flat

Non-Ideal MOS

- In the previous band diagram drawings for accumulation, inversion, and depletion, we assumed the MOS structure was “ideal,” meaning:
    1. The work functions in the metal and semiconductor were the same
    2. There was no charge within or at the surface of the oxide
- As a result, the energy bands in the semiconductor were flat under zero gate bias (see Figures 10.4 and 10.7, for example)
- In reality under non-ideal conditions, the work functions may be different and charges may exist within the oxide
- Under non-ideal conditions there will be band bending within the semiconductor near the oxide surface even under zero bias
- The shape of the band bending depends upon the sign of $\phi_m - \phi_{semi}$
- This band bending is important in determining the sign of the voltage that must be applied to reach flat band

Important Terminology

- Vacuum Level: the minimum energy an electron must posses to completely free itself from the material
- Work Function (ϕ): energy difference between the vacuum level and the Fermi energy
  - For metals ϕ_m is an invariant material constant $e\phi_m$
  - For semiconductors, ϕ_{semi} depends upon doping $e\phi_s$
- Electron Affinity (χ): the difference between the vacuum level and the conduction band energy
- Modified Metal Work Function (${\phi_m}'$): the potential required to inject an electron from the metal into the conduction band of the oxide
- Modified Electron Affinity (χ'): the difference between the conduction band energy at the semiconductor surface and the conduction band energy at the oxide surface
- V_{ox0}: the potential difference across the oxide at zero bias. Not necessarily zero.
- ϕ_{s0}: potential at the surface at zero bias

Work Function Difference

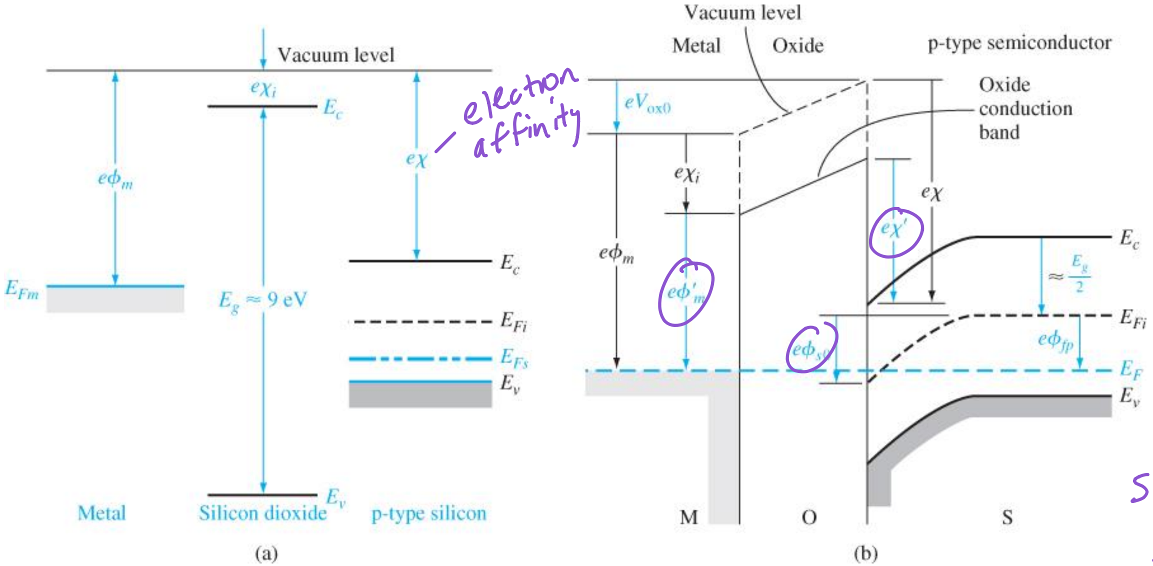


Figure 10.13 | (a) Energy levels in a MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

$E_{Fi} > E_F \rightarrow$ p type

band bend at surface

$$\boxed{\phi_{s0} = -(V_{ox0} + \phi_{ms})}$$

volt across ox

$\Delta\phi$

Sometimes need

- enhancement mode
-

- Under non-ideal conditions there is surface band bending even at zero gate bias
- Fermi levels must align between metal, oxide, and semiconductor
- Since $\phi_m - \phi_{semi}$ are constants, the vacuum level energy must change
- The band bending at the surface depends upon the oxide charge and the metal-semiconductor work function difference ($\phi_{ms} = \phi_m - \phi_{semi}$)

Work Function Difference

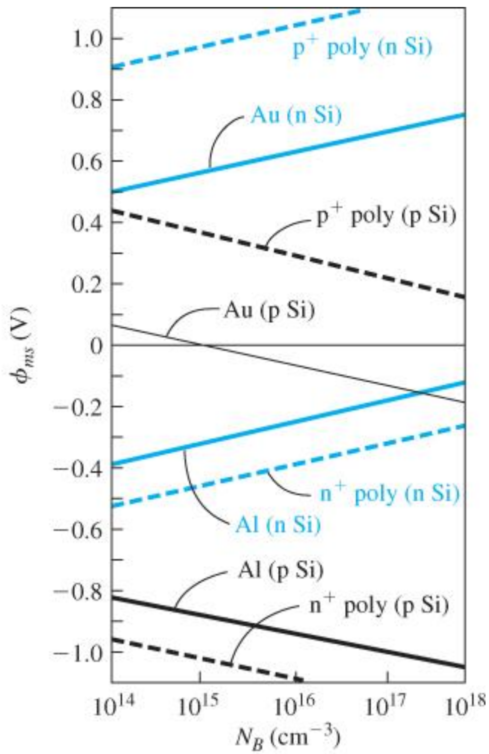


Figure 10.16 | Metal–semiconductor work function difference versus doping for aluminum, gold, and n^- and p^- polysilicon gates.
(From Sze [17] and Werner [20].)

- The direction of the band bending depends upon the sign of ϕ_{ms}
- The sign depends upon the gate and semiconductor materials and the semiconductor doping type and concentration

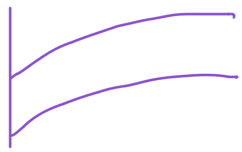
doping changes ϕ_{Fp}

p-type

$$\boxed{\phi_{ms} = \phi_m' - \left(\chi' + \frac{E_g}{2} + \phi_{Fp}\right)}$$

n-type

$$\boxed{\phi_{ms} = \phi_m' - \left(\chi' + \frac{E_g}{2} - \phi_{Fn}\right)}$$



$\phi_{ms} < 0$

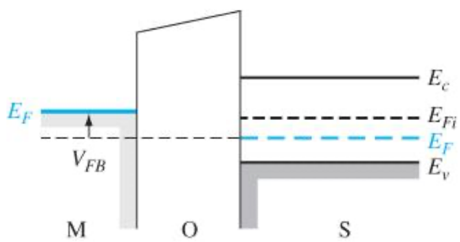
need neg work funct ($-V_g$) (y axis value, not slope)!

① look at doping (x axis)

② look at metal

$\phi_{ms} > 0$

need pos work funct. ($+V_g$) to reach flatband



$E_{Fi} > E_F$ p-type

Flat band condition

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}'}{C_{ox}}$$

fixed charge at interface (voltage drop in oxide)

(flatband voltage) assuming charge in oxide

Flat-Band Voltage

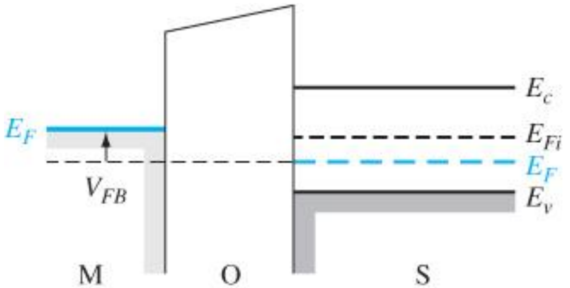


Figure 10.17 | Energy-band diagram of a MOS capacitor at flat band.

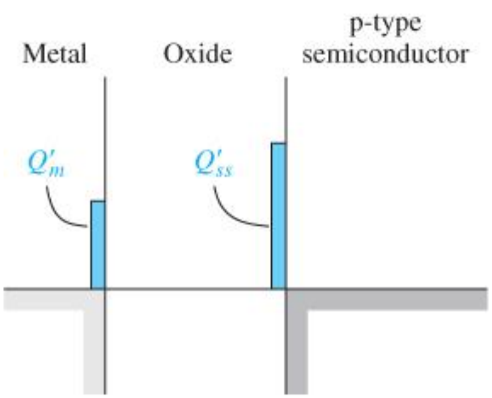


Figure 10.18 | Charge distribution in a MOS capacitor at flat band.

- Flat-Band Voltage: applied bias required such that there is no band bending in the semiconductor
- Bias needed to counteract $V_{ox0} + \phi_{ms}$
- If the oxide has some fixed charge (Q_{ss}') at the oxide-semiconductor interface, the flat-band voltage is given by

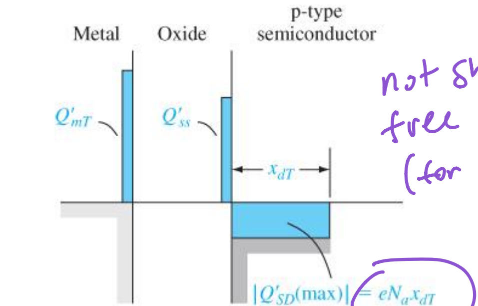
look up

$$\boxed{V_{FB} = \phi_{ms} - \frac{Q_{ss}'}{C_{ox}}}$$

- C_{ox} is the capacitance per unit area in the oxide
- With no charge in the oxide, the flat-band voltage is equal to the difference in work functions between the metal and semiconductor

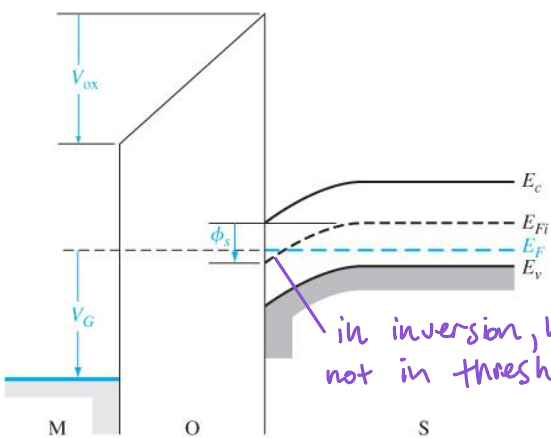
$V_{FB} = \phi_{ms}$

Threshold Voltage



not shown free electrons (for now)

Figure 10.19 | Charge distribution in a MOS capacitor with a p-type substrate at the threshold inversion point.



in inversion, but not in threshold yet

Figure 10.20 | Energy-band diagram through the MOS structure with a positive applied gate bias.

- **Threshold Voltage**: applied gate bias required to achieve the threshold inversion point ($e\phi_s = 2e\phi_{Fp}$ (p-type) and $e\phi_s = 2e\phi_{Fn}$ (n-type))
- Can be positive or negative
- Threshold voltage is a function of semiconductor doping, oxide charge, oxide thickness and dielectric constant

Threshold voltage to invert an electron channel on a p-type substrate:

total charge q/Area lookup doping

$$V_{TN} = (|Q'_{SD}(max)| - Q'_{ss})\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \phi_{ms} + 2\phi_{Fp}$$

voltage drop workfunct.

Threshold voltage to invert a hole channel on an n-type substrate:

$$V_{TP} = (-|Q'_{SD}(max)| - Q'_{ss})\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \phi_{ms} - 2\phi_{Fn}$$

prime = per cm^2

Example 10.4

EXAMPLE 10.4

Objective: Calculate the threshold voltage of a MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{15}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 12$ nm $= 120$ Å, and assume the oxide is silicon dioxide.

■ **Solution**

From Figure 10.16, we find $\phi_{ms} \cong -0.88$ V. The other parameters are

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{15}}{1.5 \times 10^{10}}\right) = 0.2877 \text{ V}$$

and

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.2877)}{(1.6 \times 10^{-19})(10^{15})}\right\}^{1/2} = 8.63 \times 10^{-5} \text{ cm}$$

Then

$$|Q'_{SD}(\max)| = eN_a x_{dT} = (1.6 \times 10^{-19})(10^{15})(8.63 \times 10^{-5}) = 1.381 \times 10^{-8} \text{ C/cm}^2$$

The threshold voltage is now found to be

$$V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$= [(1.381 \times 10^{-8}) - (10^{10})(1.6 \times 10^{-19})] \cdot \left[\frac{120 \times 10^{-8}}{(3.9)(8.85 \times 10^{-14})}\right]$$

$$+ (-0.88) + 2(0.2877)$$

or

$$V_{TN} = -0.262 \text{ V}$$

■ **Comment**

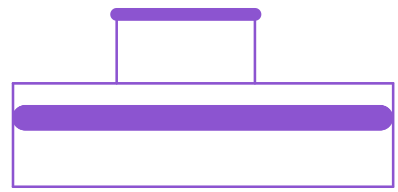
In this example, the semiconductor is fairly lightly doped, which, in conjunction with the positive charge in the oxide and the work function difference, is sufficient to induce an electron inversion layer charge even with zero applied gate voltage. This condition makes the threshold voltage negative.

EXAMPLE 10.4 **Objective:** Calculate the threshold voltage of a MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{15}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 12$ nm $= 120$ Å, and assume the oxide is silicon dioxide.

p-type   Al (gate metal) $N_a = 10^{15}\ cm^{-3}$ $Q'_{ss} = 10^{10}\ cm^{-2}$

$t_{ox} = 12nm = 120 \times 10^{-8}\ cm$



$$V_{TN} = \left(|Q'_{SD}(max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{Fp}$$

① Find ϕ_{ms} from Fig 10.16

Al (pSi) $\rightarrow -0.88V$

if no charge in ox, this is our V_{FB}

② Find ϕ_{Fp}

$$\phi_{Fp} = \frac{kT}{e} \ln\left(\frac{N_a}{n_i}\right) = 0.0259 \ln\left(\frac{10^{15}}{1.5\times10^{10}}\right) = 0.287V$$

③ Find $|Q'_{SD}(max)|$

$$|Q'_{SD}(max)| = eN_a x_{dT}$$

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{Fp}}{eN_a}\right)^{1/2} = 8.62 \times 10^{-5}\ cm$$

$$|Q'_{SD}(max)| = (1.6\times10^{-19}\ C)(10^{5}\ cm^{-3})(8.62\times10^{-5}\ cm)$$

$$= 1.379 \times 10^{-8}\ \frac{C}{cm^2}$$

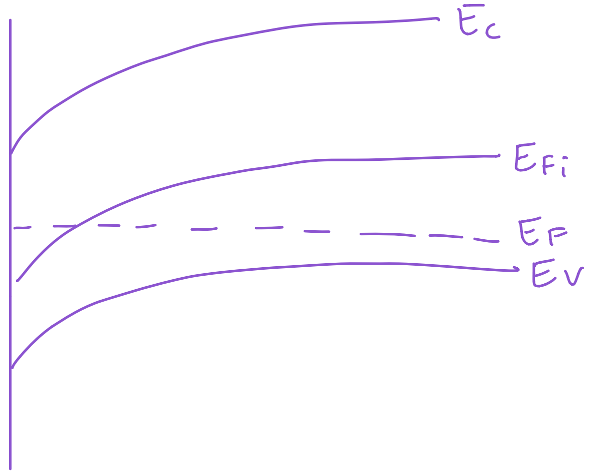
④ $V_{TN} = \left(\left|\left(1.379\times10^{-8}\ \frac{C}{cm^2}\right)\right| - 10^{10}\ cm^{-2}\right)(1.6\times10^{-19}\ C)\ldots$

don't forget to $\frac{C}{\ldots}$

convert Å to cm

$$\left(\frac{120\times10^{-8}\,\text{cm}}{(3.9)(8.85\times10^{-14}}\right) + (-0.88\,\text{V}) + 2(0.287\,\text{V})$$

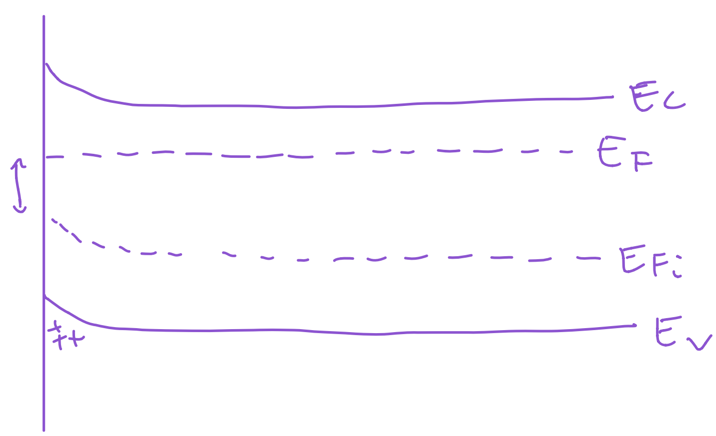
$$= -0.264\,\text{V}$$



$V_g = 0$

$V_{TN} = -0.264\ \text{V}$

For n-type



pmos

see FET Modes below

no inverted channel than off then enhancement

to invert need $-V_G$ (bend up)

to threshold need $--V_G$

to flat need $+V_G$

FET Modes of Operation

- **nMOS** (n-channel on p-substrate)
  - $V_T < 0 \rightarrow$ **depletion mode (on at $V_G = 0$)**. Need to apply a negative bias to turn the channel "off".
  - $V_T > 0 \rightarrow$ **enhancment mode (off at $V_G = 0$)**. Need to apply a positive bias to turn the channel "on".

- **pMOS** (p-channel on n-substrate)
  - $V_T < 0 \rightarrow$ **enhancement mode (off at $V_G = 0$)**. Need to apply a negative bias to turn the channel "on".
  - $V_T > 0 \rightarrow$ **depletion mode (on at $V_G = 0$)**. Need to apply a positive bias to turn the channel "off".

- Whether a device is enhancement mode or depletion mode depends upon the inherent surface band bending, which depends upon the doping, ϕ_{ms}, and the oxide thickness, charge, and dielectric constant

FET Modes of Operation

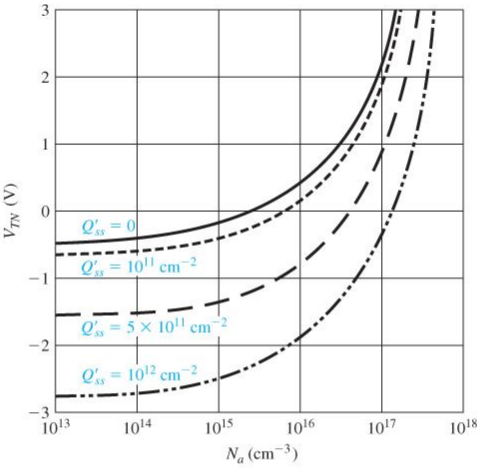


Figure 10.21 | Threshold voltage of an n-channel MOSFET versus the p-type substrate doping concentration for various values of oxide trapped charge (t_{ox} = 500 Å, aluminum gate).

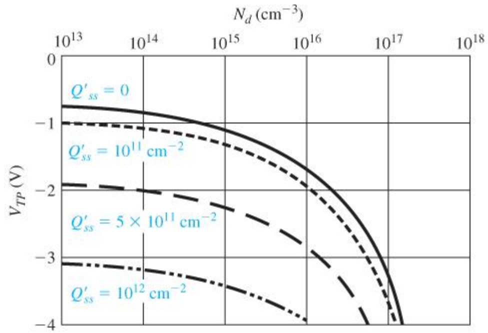


Figure 10.22 | Threshold voltage of a p-channel MOSFET versus the n-type substrate doping concentration for various values of oxide trapped charge (t_{ox} = 500 Å, aluminum gate).

- Achieving enhancement mode in nMOS requires high doping
- pMOS devices are almost always enhancement mode
- Enhancement mode is preferred for switching applications. Since the device is normally off at $V_G = 0$ there will be less leakage current (power dissipation in the off state).
- Depletion mode devices used as load resistors in logic circuits
- (100) silicon, poly-silicon gates, and ion implantation are all techniques to achieve enhancement-mode nMOS