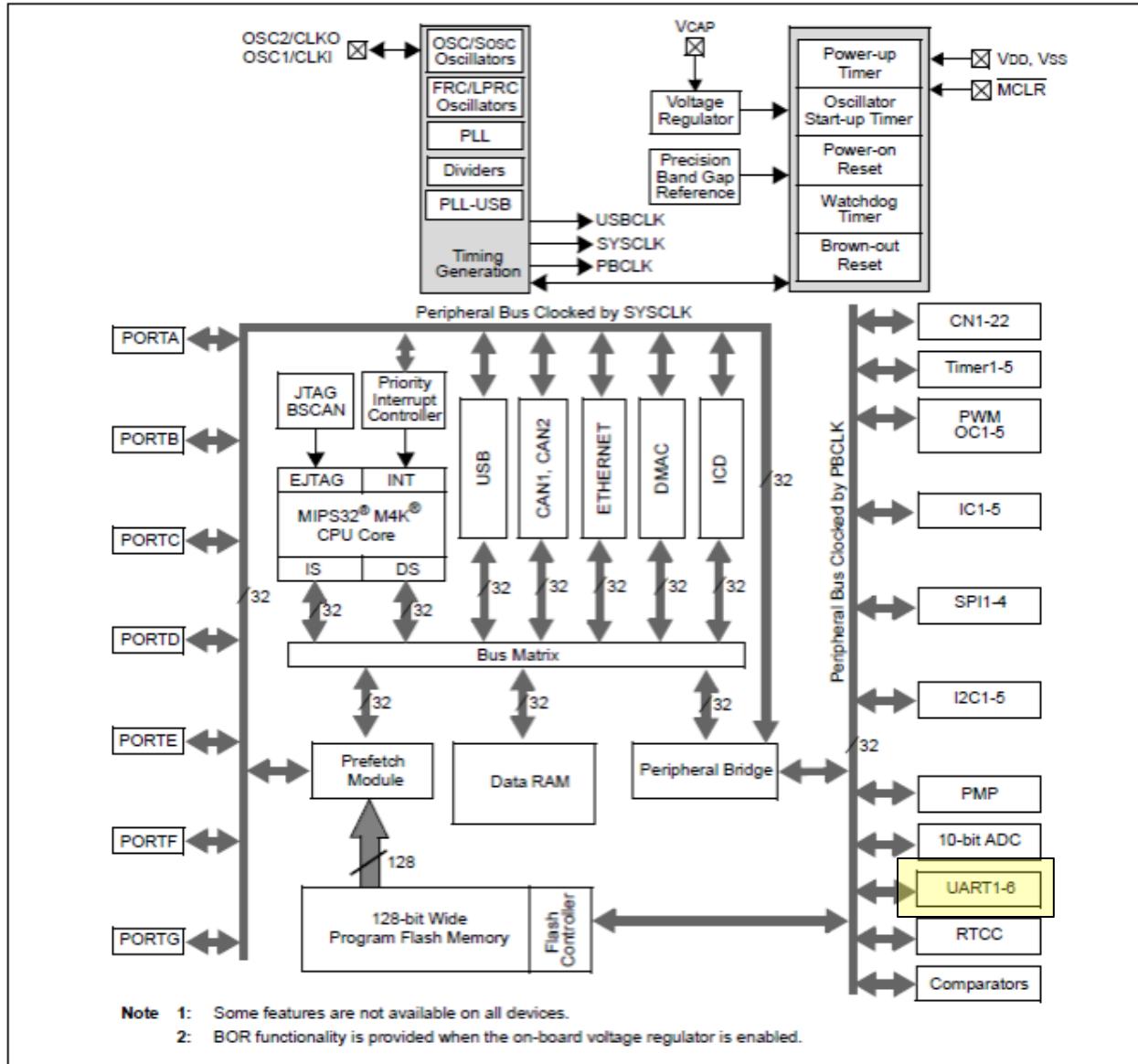


# UART Interface

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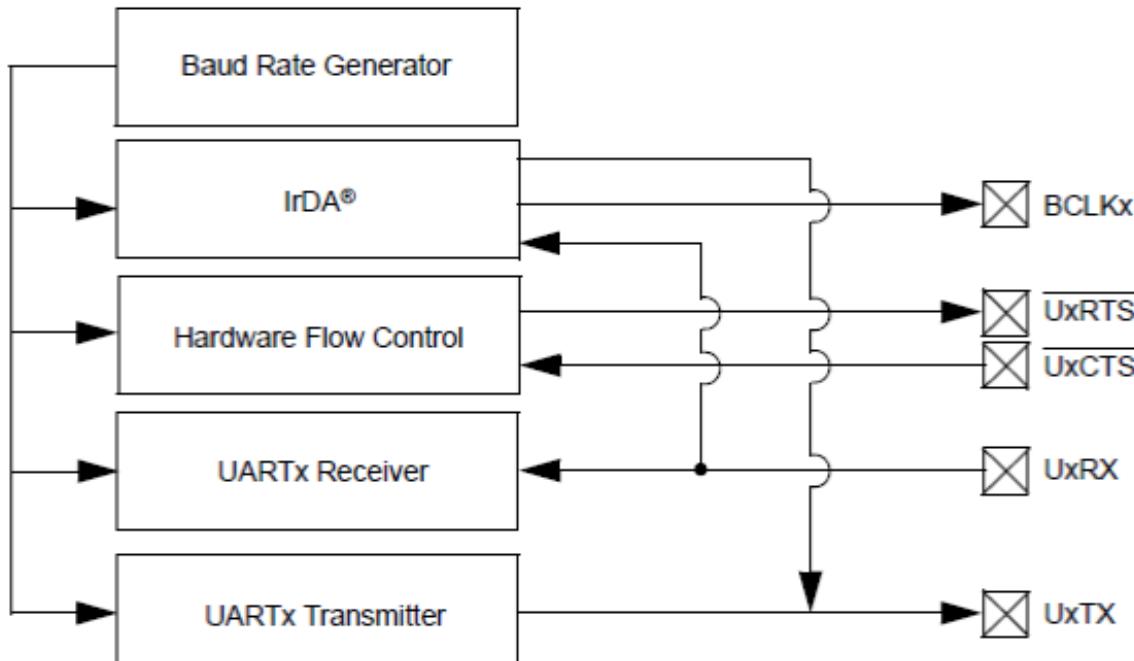
# PIC Architecture

FIGURE 1-1: BLOCK DIAGRAM<sup>(1,2)</sup>



# UART Block Diagram

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM



# UART Interface

- **Characteristics**
  - Asynchronous
  - Uses a minimum of two signal wires, Tx and Rx
  - Can use two optional flow control signals, Request to Send (RTS) and Clear to Send (CTS)
  - Full Duplex communication
  - Supports multiple protocols and configurations
  - Requires both Sender and Receiver configuration of data rates and protocol options.

# Communication Between Devices

- **When devices are transferring data between each other, they require:**
  - A protocol which defines how the data are to be extracted from the electrical signal.
  - A means by which to determine the start and the end of the transmission.

# Asynchronous Communication Protocol Detail

- For two UARTs to communicate with each other, both must be configured with identical values for:

## Bit Rate Clock

- Baud Rate

## Framing

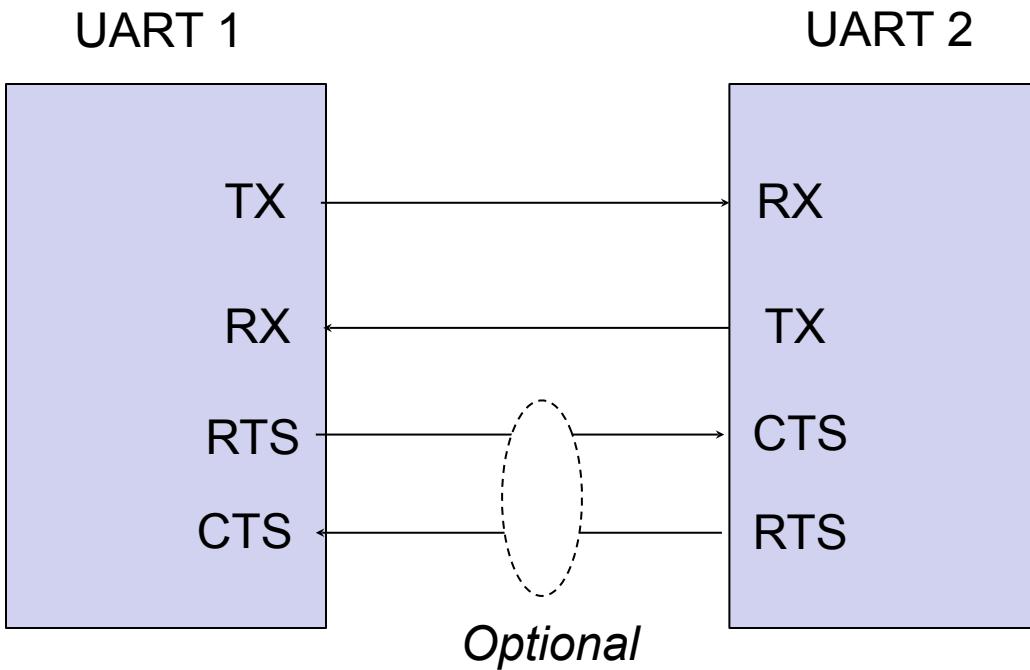
- Start Bit
- Data Bits
- Parity (if used)
- Stop Bits

# UART Signals

- **For wired communications, the following signals are used:**
  - Tx – Transmit Data
  - Rx – Receive Data
  - CTS – Clear to Send (Optional for hardware handshake)
  - RTS – Request to Sent (Optional for hardware handshake)

*Note: The Tx line of one of the communicating devices must be tied to the Rx line of the other device and vice versa.*

# Signal Interconnects

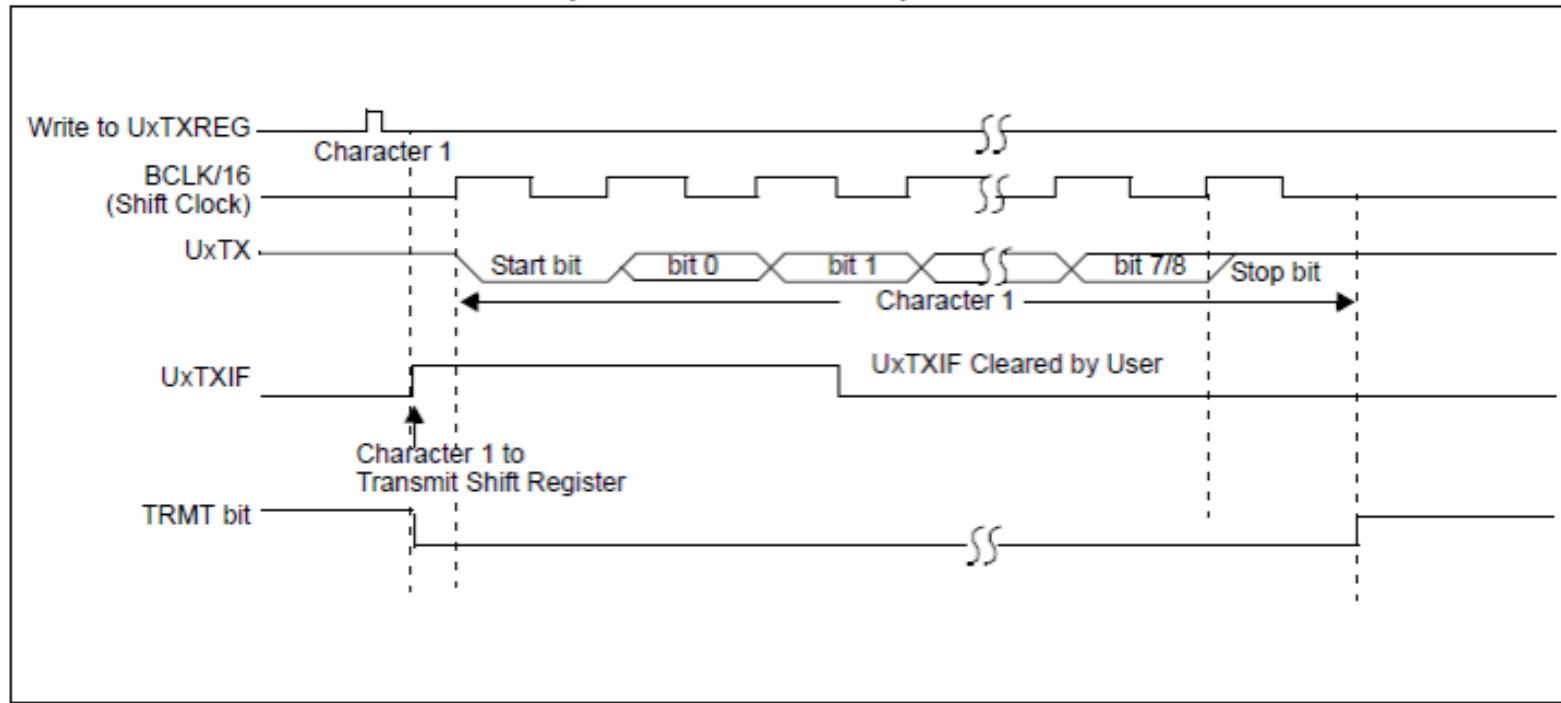


# UART Data Communication Protocol

- When the communication link is idle, the transmit line is at a logical one level.
- When a transmission is starting, the transmit line is lowered to a logical zero level and is held for one bit time. This is what is called the start bit.
- Following the start bit, 8 or 9 data bits are transmitted.
- If 8 data bits are being transmitted, an optional parity bit may be transmitted.
- After the data and parity bits have been transmitted, the transmit line is raised to a logic one level for one or two bit times, indicating the end of the transmission. The end bit(s) are called the stop bit(s).

# Single Character Transmission

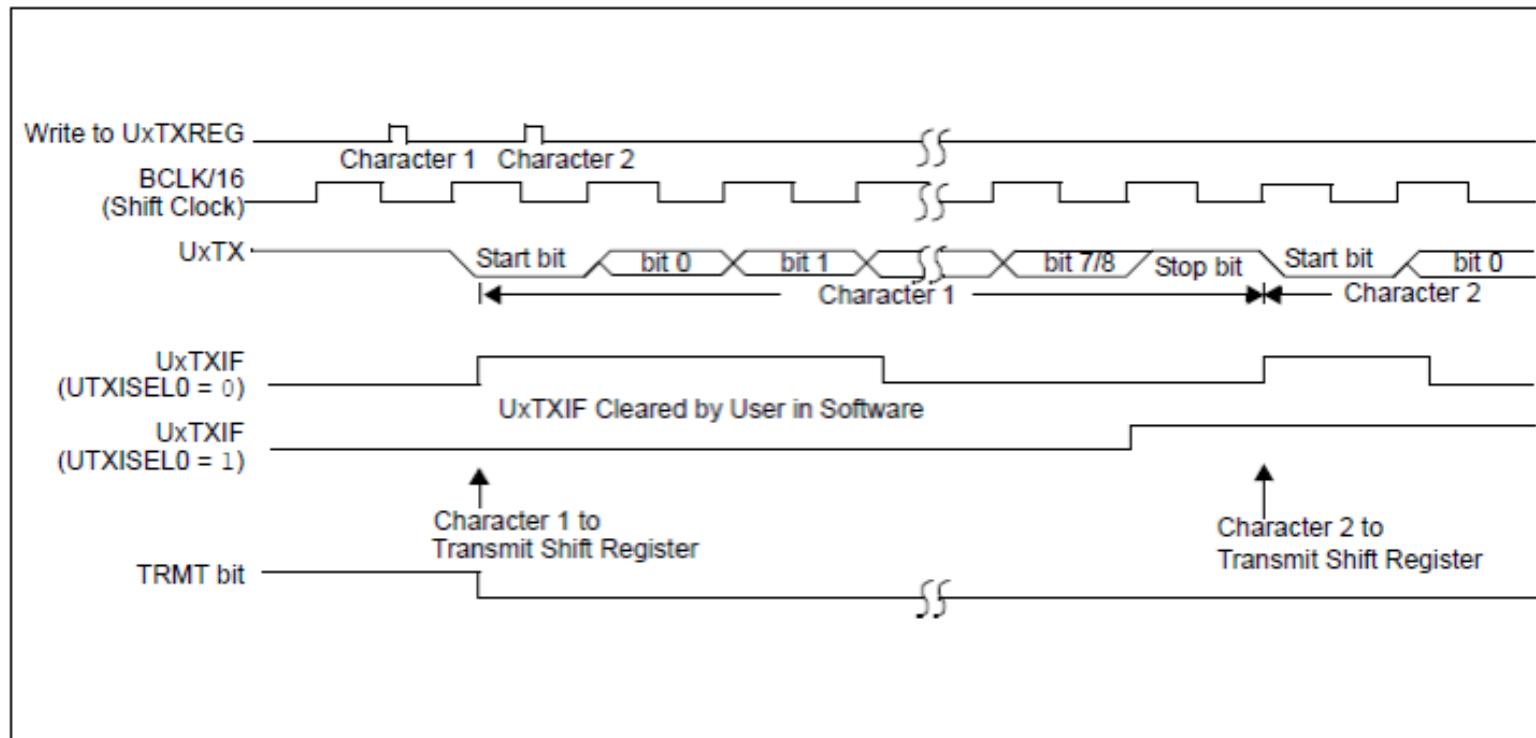
FIGURE 19-2: TRANSMISSION (8-BIT OR 9-BIT DATA)



The transmission begins with a start bit, which is followed by 8 or 9 data bits, then possibly a parity bit, and ends with one or more stop bits

# Sequential Transmissions

FIGURE 19-3: TWO CONSECUTIVE TRANSMISSIONS



With sequential transmissions, the start bit of the subsequent character(s) follows immediately after the prior transmission's stop bit(s)

# Vintage Data Terminal



# RS-232

- **RS-232 is a standard for serial communication that specifies:**
  - Connectors
  - Pin Assignments
  - Voltage Levels
  - Baud Rates
- **RS-232 uses a bipolar signal to represent logic values**
  - +3V to +12V – represents a logical 0
  - -12V to -3V – represents a logical 1
- **Terminology**
  - DTE – Data Terminal Equipment (Like a terminal)
  - DCE – Data-Circuit Terminating Equipment (Like a modem)

# PIC32 UARTs on MX7

- The PIC32 microcontroller has six UARTs
- Two UARTs are accessible on the MX-7 development board
- On the MX-7 board, UART1 is connected to the USB serial converter – Using this UART can cause problems when using the MPIDE development system.
- UART2 signals are accessible via connector JF

# UART SFRs

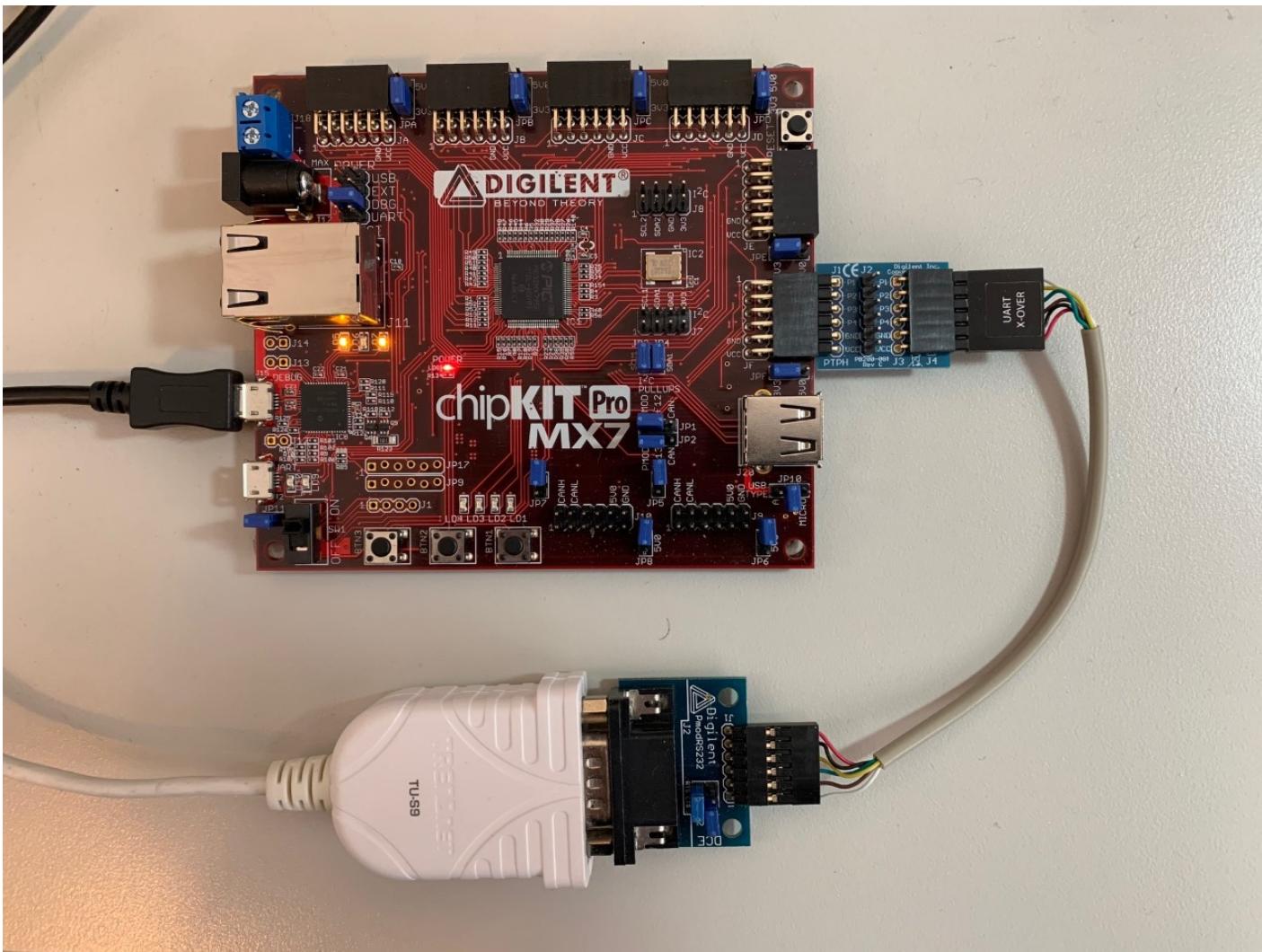
TABLE 20-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)

Virtual Address (BF00_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6620	U6TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	—	—	—	—	—	—	—	0000	
6630	U6RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	—	—	—	—	—	—	—	0000	
6640	U6BRG <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BRG<15:0>															0000	
6800	U2MODE <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>	STSEL	0000	
6810	U2STA <sup>(1)</sup>	31:16	—	—	—	—	—	—	ADM_EN	—	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	UTXISEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110		
6820	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	TX8	—	—	—	—	—	—	—	—	0000	
6830	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	RX8	—	—	—	—	—	—	—	—	0000	
6840	U2BRG <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BRG<15:0>															0000	
6A00	U5MODE <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	—	—	—	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>	STSEL	0000		
6A10	U5STA <sup>(1)</sup>	31:16	—	—	—	—	—	—	ADM_EN	—	ADDR<7:0>							0000	
		15:0	UTXISEL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	UTXISEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110		
6A20	U5TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	TX8	—	—	—	—	—	—	—	—	0000	
6A30	U5RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	RX8	—	—	—	—	—	—	—	—	0000	
6A40	U5BRG <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BRG<15:0>															0000	

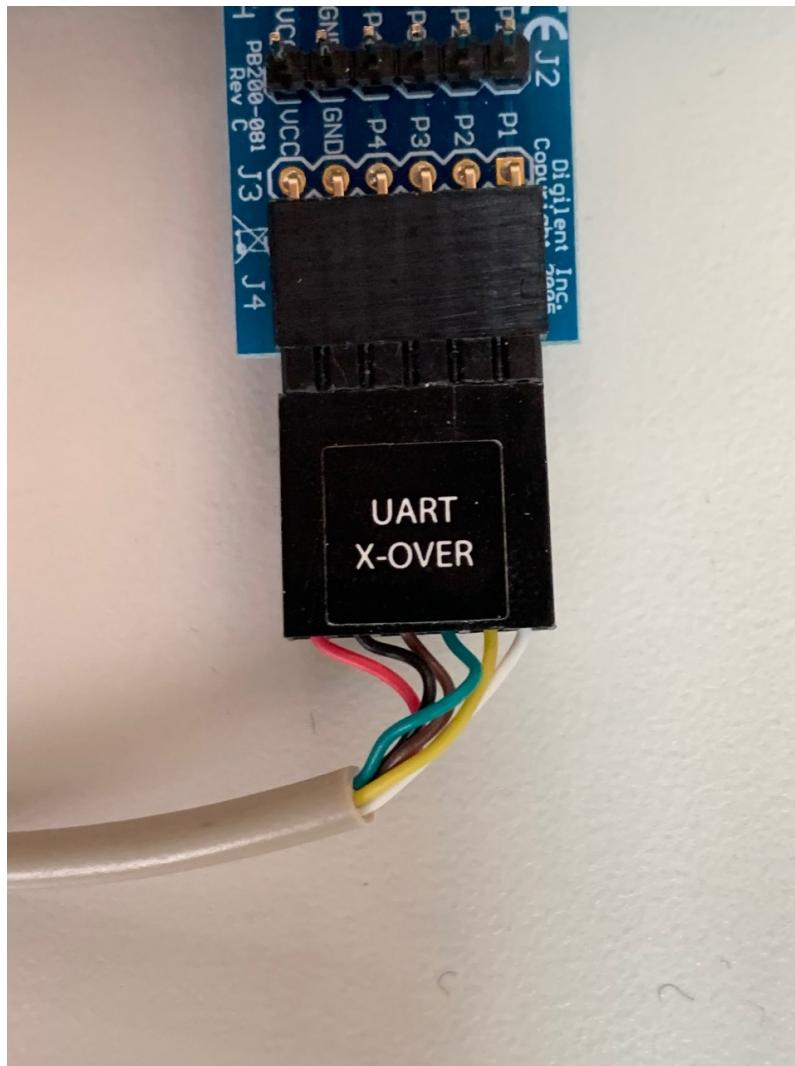
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See [Section 12.1.1 "CLR, SET and INV Registers"](#) for more information.

# UART2 Connection on MX7



# UART Crossover Cable



# Multi-Character Transmission

