Lecture 21 - Configuring I^{2}C

Thursday, April 16, 2020 10:39 AM

Objectives:	- Learn how to configure the I2C interface on the MX-7 using the c library functions - Learn how the TMP3 module works and how it is configured - Review

Handy I^{2}C Reference:
https://www.digikey.com/en/articles/why-the-inter-integrated-circuit-bus-makes-connecting-ics-so-easy?utm_medium=email&utm_source=mak&utm_campaign=67184_MAK2004C&utm_content=learnmore3_US&utm_cid=8524102&mkt_tok=eyJpIjoiWldWbU1HUXdNbVpsWkdObCIsInQiOiJDM1BFNzZoVEJLNzVENDVrYXpvNW1CQXowQXFMVXhxWmhBQzYrR3Q1dTNKbGRLV0Y5TEpjYmo0T0NWYWFtV2E5c2p3QVQ0VGk5RWtEUUZlNzFNamxKV2p6UHJsRGlORDhsWWNHOFk4Z0FPelBCSkNGZ012VCtMOTJMRmFHOU5wdiJ9

I2C SFRs

- I2CxCON - Enables control of module
- I2CxSTAT - Contains status flags
- I2CxBRG - Baud Rate Generator value
- I2CxTRN - Register to which data is written for TX
- I2CxRCV - Register from which data is read - RX
  In Slave mode, we also use:
- I2CxADD - Address of slave device
- I2CxMASK - Designates which address bits can be ignored - allows support for multiple addresses

Interrupts - Like other peripherals, I2C has multiple interrupt modes

- Tx
- Rx
- Errors (bus collision)

I2C Protocol Related Functions
StartI2Cx( ) - generates the start condition
StopI2Cx( ) - generates the stop condition
RestartI2Cx( ) - generates a restart

IdleI2Cx( ) - Waits for:	A start condition enable bit
	A stop condition enable bit
	A receive enable bit
	An ACK sequence bit

AckI2Cx( ) - generates and ACK condition
NotAckI2Cx ( ) - generates a NACK condition

STORED PROGRAM COMPUTERS

ARCHITECTURE
RISC - MIPS

NUMERIC FORMATS
UNSIGNED
SIGNED

REPRESENTATIONS
DECIMAL
HEXADECIMAL
BINARY

PIC 32 MICROCONTROLLER

CLOCKS - SYSCLK - 80 MHZ
PBCLK - 10 MHZ

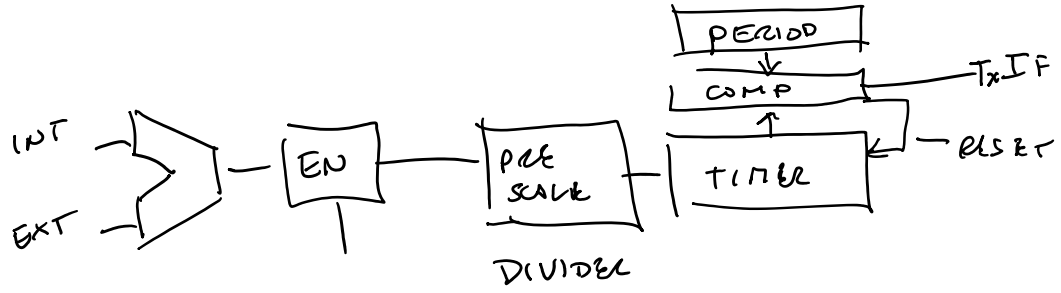
SFR's
CONFIG OF HW
" " PERIPHERALS
COMM. W/ PERIPHERALS
MONITOR STATUS

GP. REGS
DATA
ADDRESSES
NO. INSTRUCTIONS

I/O PORTS - DIGITAC FOR NOW
- CONFIGURATION
- OPEN DRAIN

SFR'S OFFSETS FOR CLR, INV, SET

TIMERS - 5 16-BIT TIMERS



INTERRUPTS

(1) - NEED A SOURCE
(2) - ENABLE SPECIFIC INTERRUPT - (SET PRIORITY)
(3) - NEED AN ISR

ISR's - INTERRUPT SERVICE ROUTINE
(1) NO ARGUMENTS PASSED TO AN ISR

② AN ISR CANNOT BE CALLED DIRECTLY

③ AN ISR CANNOT RETURN ANY VALUES

④ IDEALLY, AN ISR SHOULD NOT CALL ANY OTHER FUNCTIONS

IMPORTANT: AN ISR MUST CLEAR THE INTERRUPT FLAG.

COMMUNICATION – SERIAL

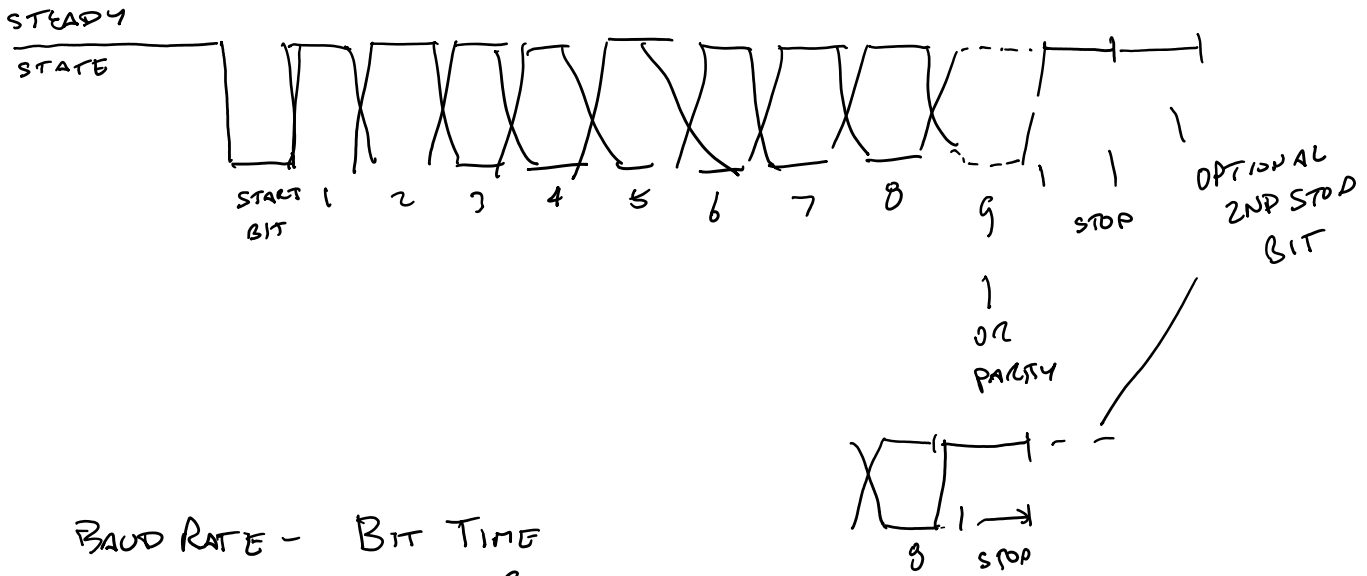
– ONE BIT AT A TIME

SYNCHRONOUS
ASYNCHRONOUS } –

FULL DUPLEX – TX & RX SIMULTANEOUSLY
HALF DUPLEX – ONE TX AT A TIME

POINT TO POINT
BUS ORIENTED

UART – FULL DUPLEX, ASYNCHRONOUS – USING RS-232 IMPLEMENT POINT TO POINT CONNECTION



BAUD RATE – BIT TIME
DATA BITS – 8 OR 9
PARITY (W/ 8 DATA BITS) O, E, N
NUMBER OF STOP BITS – 1 OR 2

8, N, 1 (data, parity, stop bits)

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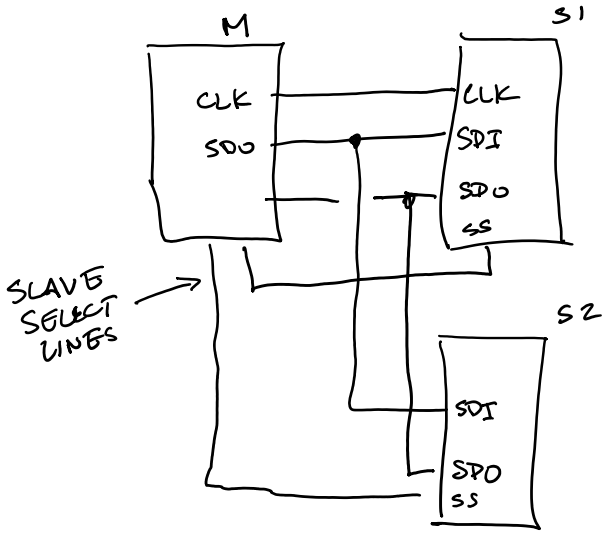
DATA ENCODING

ASCII - 7 BITS msb = 0

UNICODE - LISTING OF CHARACTERS - CODE POINT

UTF-8 - ENCODING SCHEME

SPI - SERIAL
SYNCHRONOUS
FULL-DUPLEX



I^2C - SYNCHRONOUS (TWO-WIRE)
HALF-DUPLEX
SERIAL