ECE338
Lab #7: Create a mixed C code/VHDL project that allows user data to be transferred between the PS and PL sides
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For Lab #7, we were tasked with taking the block diagram that we built in Labs 5 and 6, run SDK to generate an .elf (Linux executable file) from the C code provided, and to program our Zybo boards with this generated file. This will us to read and/or write a portion of the 8K 16-bit word BRAM. Passing a text file to this executable allows the C code to read the data file (also supplied) and transfer it, one 16-bit word at a time, to the GPIO register. As it does so, the VHDL state machine reads the GPIO register and stores it in the BRAM. Once the C code loads the memory with data, a second routine is called that simply unloads it, one 16-bit word at a time and prints the results in the terminal window (Figure 1).

In order to transfer the files to be run on the board, we were tasked with creating a network connection between the host machine and the Zybo. This task seemed to be the most difficult part of the process for most students; however, once mastered, I was able to set up various “alias” scripts to streamline the process (Figure 2).