Using the PIC Timers

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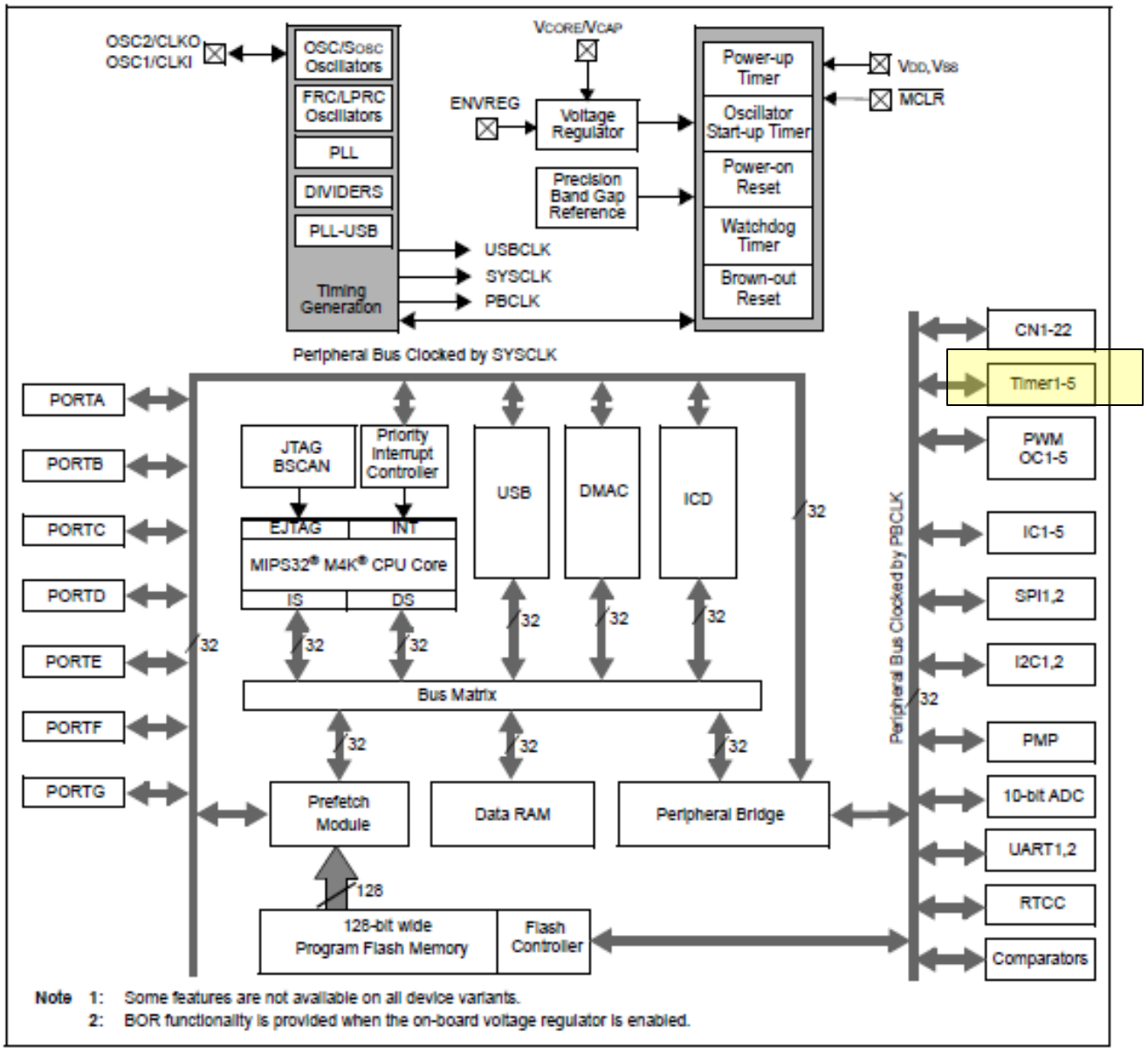
PIC Architecture



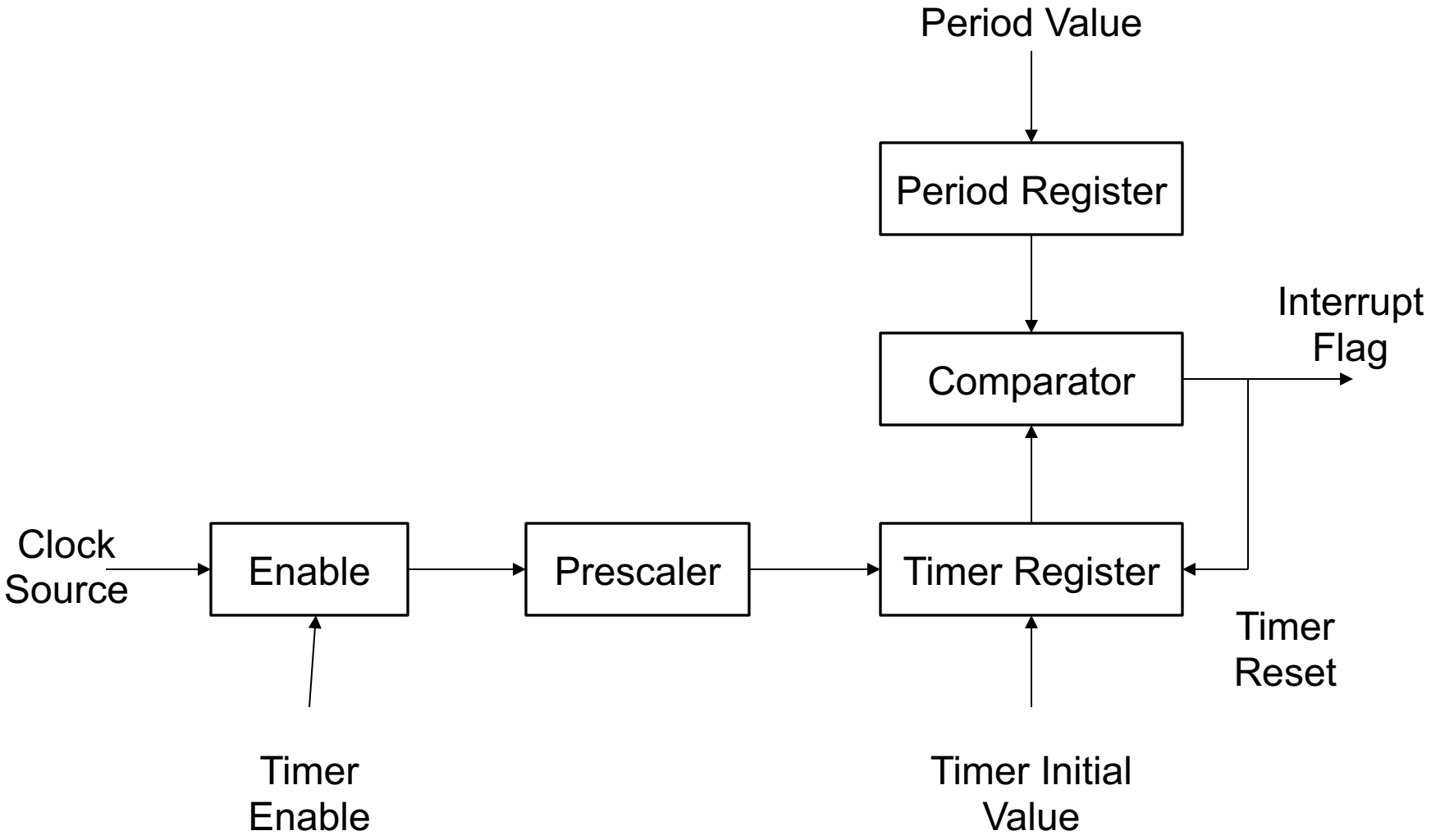
Timers

- **The PIC32 has five 16-bit timers.**

- **Timers can be used to:**
  - Implement delays.
  - Generate accurate time-based periodic interrupt events for software applications or real-time operating systems.
  - Count external pulses or perform accurate timing measurement of external events by using the timer's gate feature

- **We will drive the timers using the peripheral bus clock.**

Timer Operation

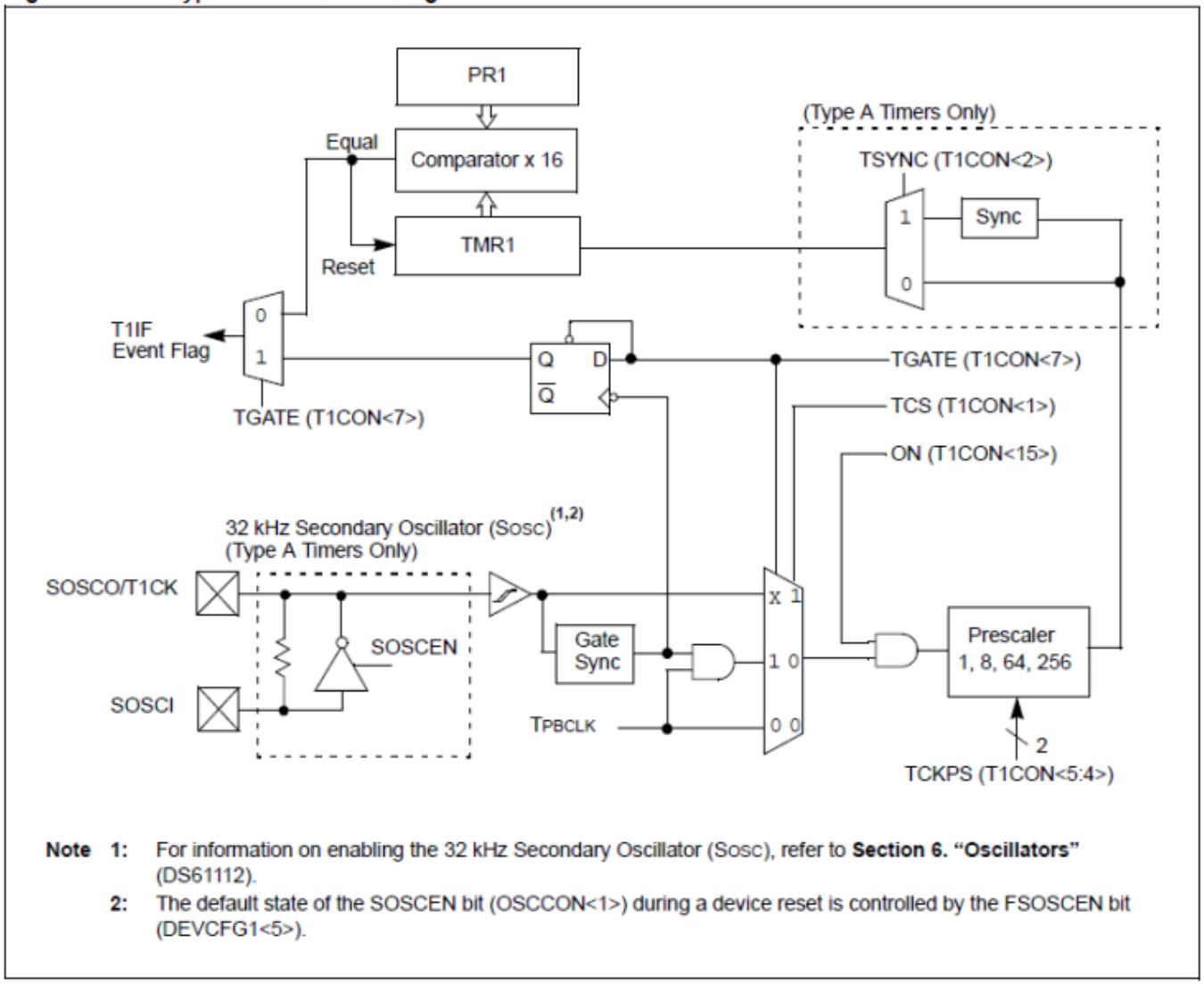


Timer Features

- **The PIC32 has two types of timers:**
  - Type A
    - Timer 1
    - 16 bit only
    - Limited pre-scale
  - Type B
    - Timers 2 – 5
    - Can be combined into 32 timers
    - More extensive pre-scale options

Type A Timer

Figure 14-1: Type A Timer Block Diagram

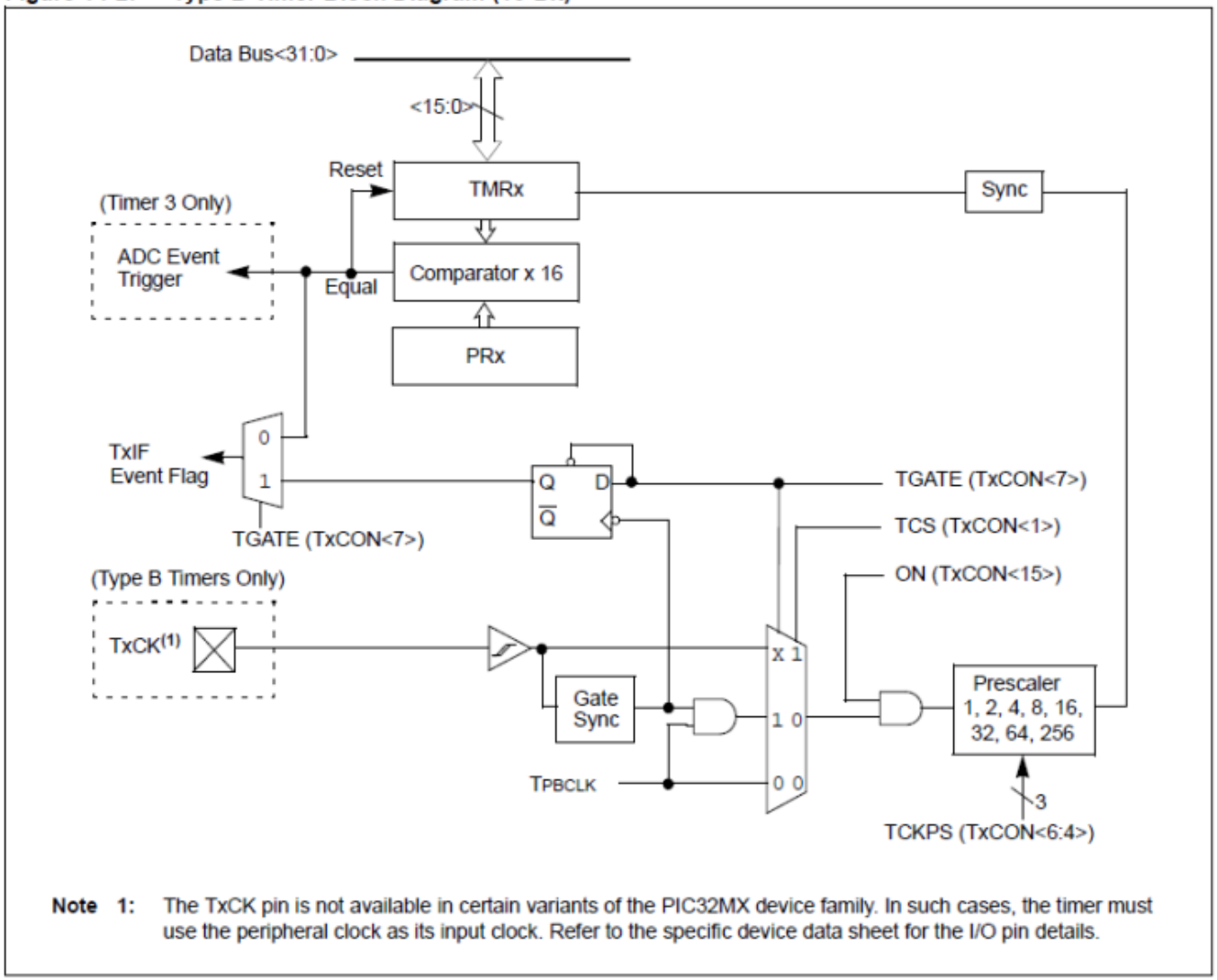


Note 1: For information on enabling the 32 kHz Secondary Oscillator (Sosc), refer to **Section 6. "Oscillators"** (DS61112).

2: The default state of the SOSCEN bit (OSCCON<1>) during a device reset is controlled by the FSOSCEN bit (DEVCFG1<5>).

Type B Timer

Figure 14-2: Type B Timer Block Diagram (16-Bit)



Note 1: The TxCK pin is not available in certain variants of the PIC32MX device family. In such cases, the timer must use the peripheral clock as its input clock. Refer to the specific device data sheet for the I/O pin details.

Timer Registers

- **A PIC32 timer has three SFRs:**
  - A Control Register (TxCON)
    - Timer configuration
  - A Counter Register (TMRx)
    - Counts clock cycles
  - A Period Register (PRx)
    - Can be used to generate an interrupt when the value in the counter register equals the value in the period register. When the two registers have equal values, the counter register is reset on the next clock input.

Timers 1 – 5 SFRs

TABLE 4-7: TIMER1-5 REGISTERS MAP(1)

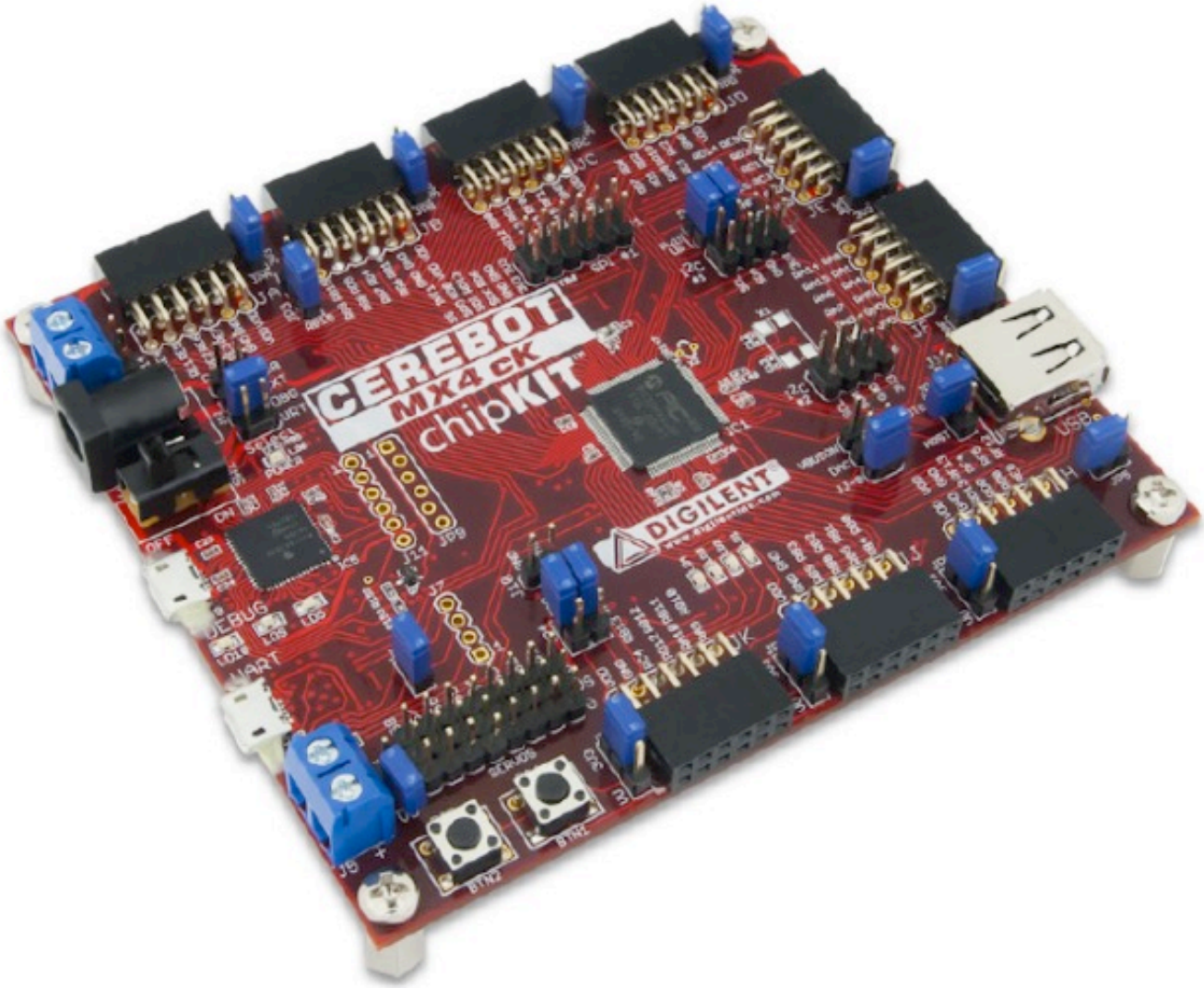
Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS(2)	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS(2)	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS(2)	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS(2)	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: This bit is not available on 64-pin devices.

chipKIT MX4 Board



Timer Registers

- **On the MX7 Board, we have timer external clock input capabilities:**

  (Pmod connector position, chipKIT pin number, & microcontroller I/O port and bit number)

- TCK1 – not available
- TCK2 – JC-01, digital pin 16, RC01
- TCK3 – not available
- TCK4 – not available
- TCK5 – JD-03, digital pin 26, RC04