Output Compare

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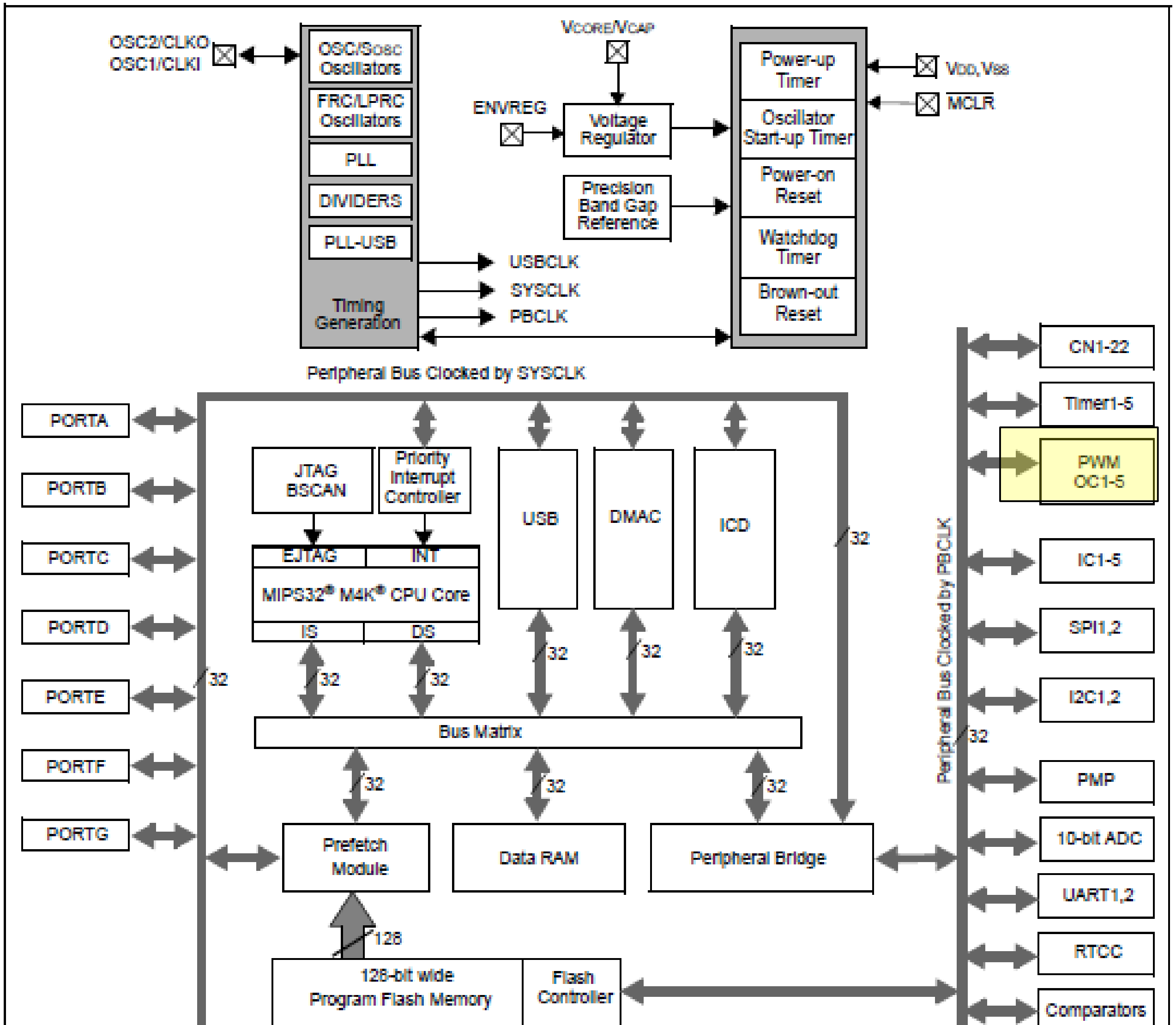
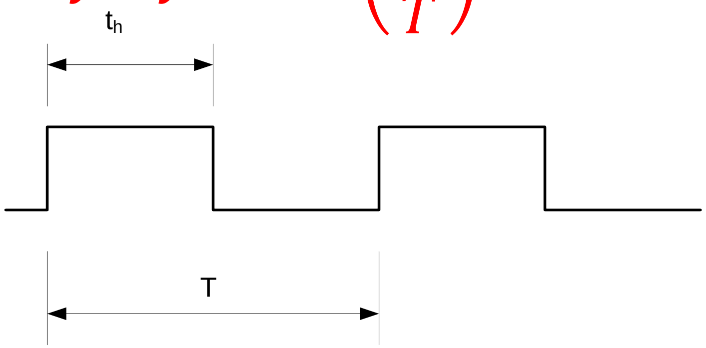
PIC Architecture



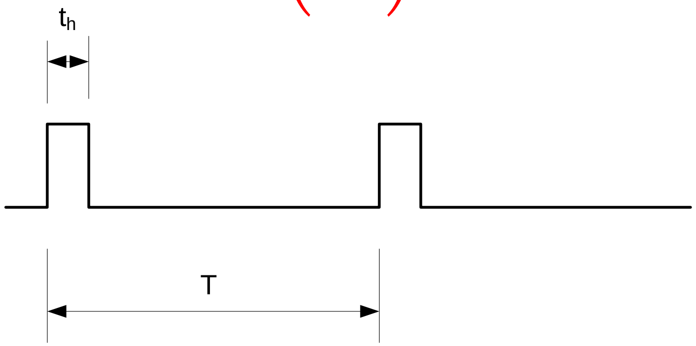
Note 1: Some features are not available on all device variants.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

Pulse Width Modulated Signals

$$Duty\ Cycle = \left(\frac{t_h}{T}\right) * 100\ \%$$



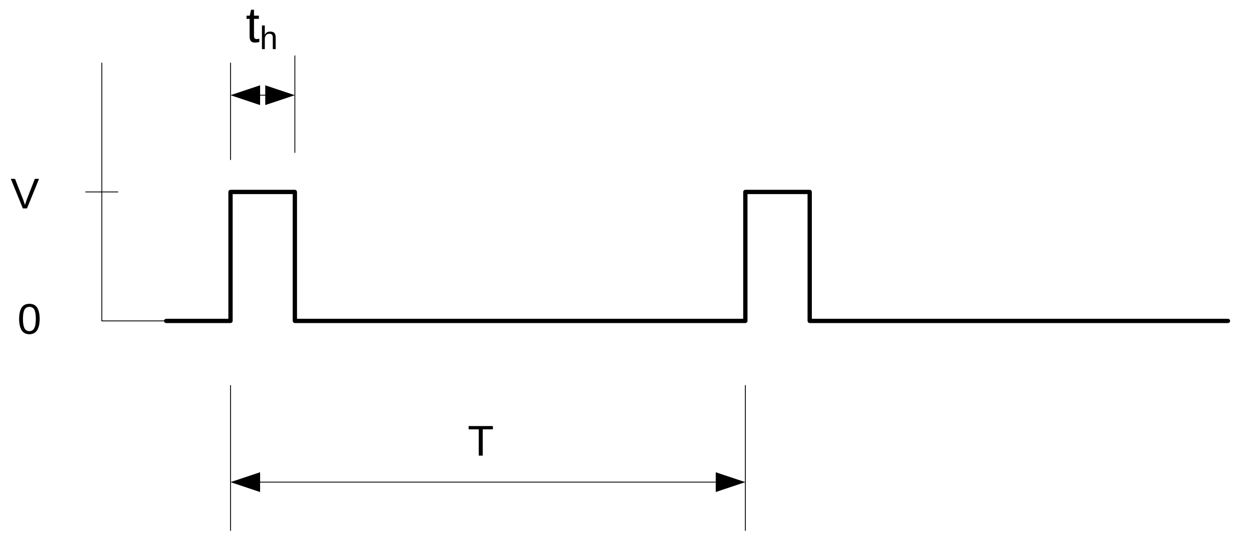
$$Duty\ Cycle = \left(\frac{.5T}{T}\right) * 100\ \% = 50\ \%$$



$$Duty\ Cycle = \left(\frac{.125T}{T}\right) * 100\ \% = 12.5\ \%$$

PWM Signal Applications

- By varying the duty cycle of a pulse train, the average DC value can be varied



$$V_{avg} = V * \frac{t_h}{T}$$

By varying the duty cycle, V_{avg} can be varied from 0 to V

Using PWM Signals

- Because we can change the duty cycle dynamically, a PWM signal can used for a variety of applications:
  - Speed control of a DC motor
  - Dimming of LED lights
  - Controlling the position of the armature of a Servo-Motor.

Generating Tones using PWM

Using a PWM wave with a duty cycle of 50%, we can generate tones.

Recall:

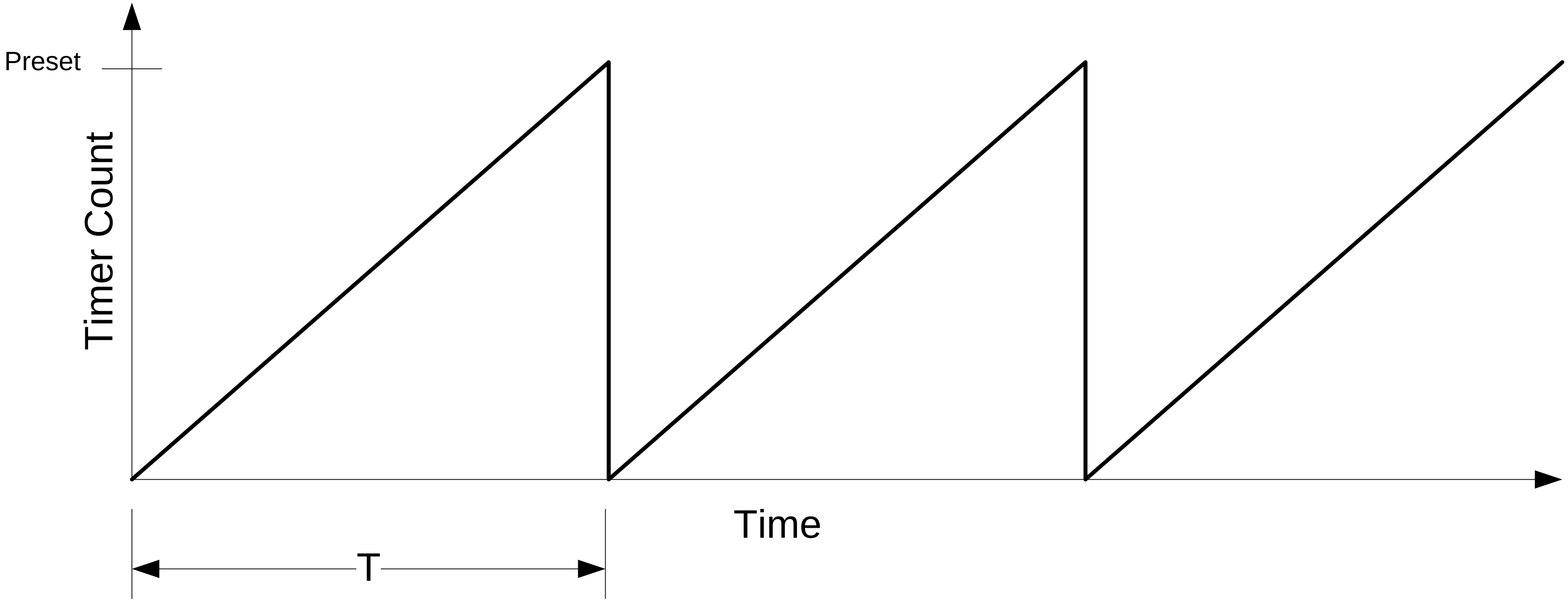
$$\boldsymbol{x(t)_{Square} = \frac{4}{\pi}\left[\sin(2\pi f t) + \frac{1}{3}\sin(3(2\pi f t)) + \frac{1}{5}\sin\big(5(2\pi f t)\big) + \ldots\right]}$$

= fundamental frequency + odd harmonics

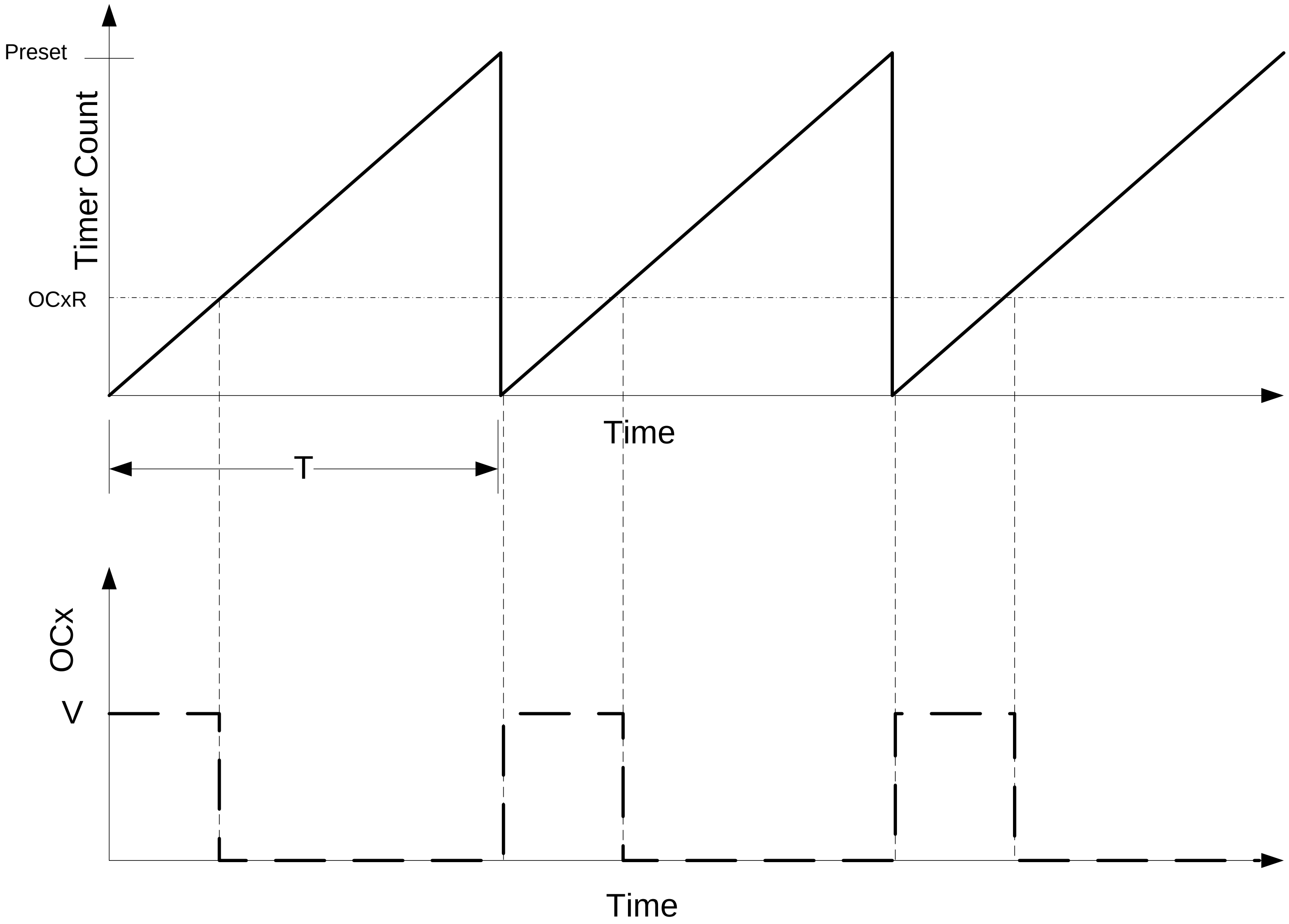
By varying the period of the square wave, we vary the fundamental frequency and the harmonics

Generating PWM Signals

- PWM signals are generated using a timer.
- The PWM signal period corresponds to the value set in the timer preset register.

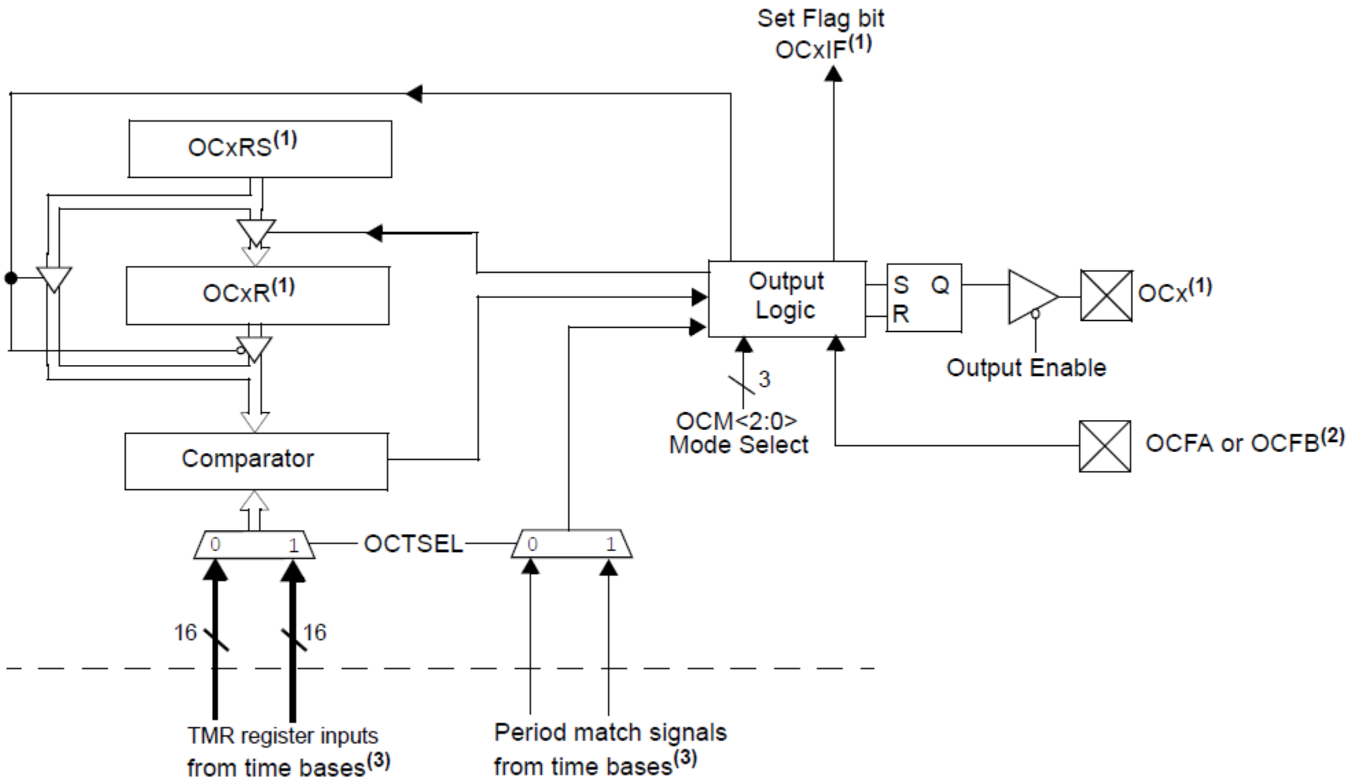


Generating The Output Compare Signal



Output Compare Operation

Figure 16-1: Output Compare Module Block Diagram



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels 1 through 5.

2: OCFA pin controls OC1-OC4 channels. OCFB pin controls OC5 channels.

3: Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit time base. Refer to the specific device data sheet for the time bases associated with the module.

Output Compare SFRs

TABLE 4-9: OUTPUT COMPARE1-5 REGISTERS MAP[1]

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
3020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
3220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
3420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
3620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
3820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.