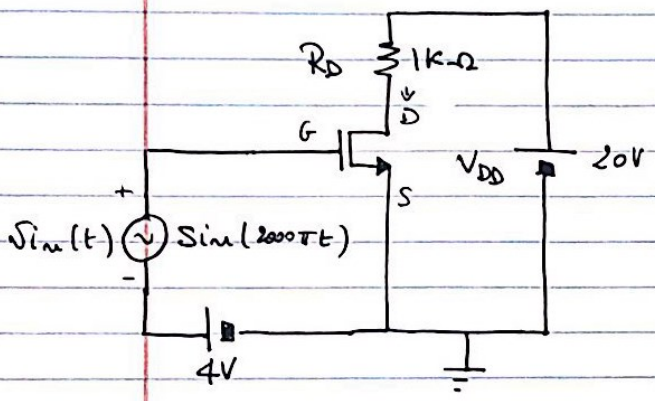
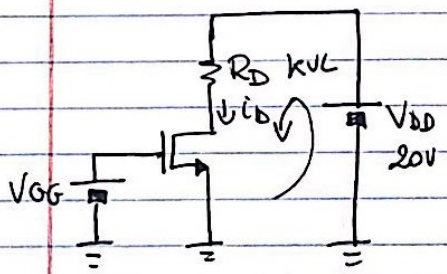
Lecture 2-In class problem 1-Solution



In order to sketch the load line for the circuit above one needs to analyze the DC circuit. Thus, one needs to set $v_{in}(t)=0$. The resulting circuit to be analyzed is then shown below.



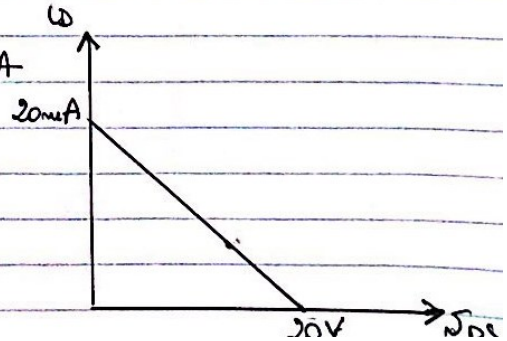
The load line can be obtained by writing a KVL on the output branch and using Ohm's law.

Equation of the load line: $V_{DD} - R_D I_D - V_{DS} = 0$

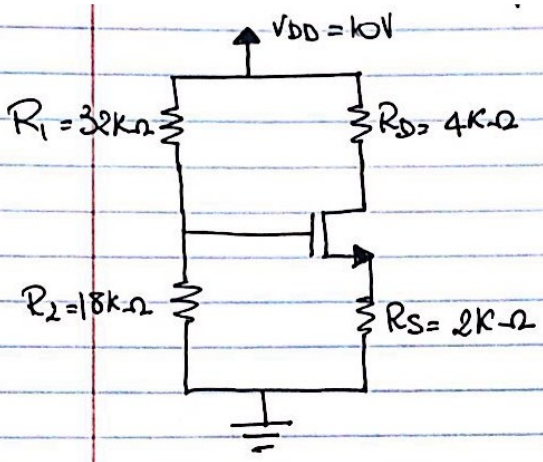
$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

At $I_D = 0$, $V_{DS} = V_{DD} = 20V$

At $V_{DS} = 0$, $I_D = \frac{V_{DD}}{R_D} = 20mA$



Lecture 2-In class problem 2-Solution



$V_{TN} = 0.8V \quad K_n = 0.5 mA/V^2$

Note that only the DC circuit is shown here.

In order to sketch the load line and calculate the Q point, one needs to determine the values of V_{GS}, V_{DS}, and I_D.

A possible strategy is to start by using linear circuit analysis to find useful values of voltages such as the voltage between the gate and ground, the voltage between source and ground, and the voltage between drain and ground. One can also use the Ohm's law to relate these voltages to currents in the circuit, such as the drain current.

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD} = \frac{18}{18+32} \cdot 10 = 3.6V$$

$$V_S = V_G - V_{GS}$$

$$I_D = \frac{V_S}{R_S} \qquad V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Now assume that the transistor is biased in saturation or that $V_{GS} > V_{TN}$ and $V_{DS} > V_{GS} - V_{TN}$.

Thus $I_D = K_n (V_{GS} - V_{TN})^2$.
Previously we wrote a linear relationship between I_D and V_{GS} using linear circuit analysis. We can equate the two expressions of the I_D as a function of V_{GS} to obtain an equation in V_{GS}.

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S} = K_n (V_{GS} - V_{TN})^2$$

$$3.6 - V_{GS} = (0.5)(2)(V_{GS} - 0.8)^2$$

$$3.6 - V_{GS} = V_{GS}^2 - 1.6 V_{GS} + 0.64$$

$$V_{GS}^2 - 0.6 V_{GS} - 2.96 = 0$$

$$V_{GS} = \frac{0.6 \pm \sqrt{(0.6)^2 + (4 \cdot 2.96)}}{2} = \frac{0.6 \pm 3.43}{2}$$

~~-1.41V~~

2.046 ✓

$V_{GSQ} = 2.046\,V$

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{3.6 - 2.046}{2k} = 0.777\,mA \;;\; I_{DQ} = 0.777\,mA$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 10 - (0.777)(4+2) = 5.34\,V$$

$V_{DSQ} = 5.34\,V$

Now we need to verify that our assumption of the transistor operating in saturation was correct.

$V_{GS} = V_{GSQ} = 2.046V > V_{TN} = 0.8V$ ✓

$V_{DS} = V_{DSQ} = 5.34V > V_{GSQ} - V_{TN} = 2.046 - 0.8\,V$ ✓

The Q point has coordinates $V_{GSQ} = 2.046V$;
$V_{DSQ} = 5.34V$
$I_{DQ} = 0.777\,mA$

The equation of the load line is written below

$$I_D = \frac{V_{DD} - V_{DS}}{R_S + R_D} \Rightarrow \begin{matrix} I_D = 0 & V_{DS} = V_{DD} = 10V \\ V_{DS} = 0 & I_D = \frac{V_{DD}}{R_S + R_D} = 1.66mA \end{matrix}$$