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ECE 520: VLSI Design
Spring 2022

Homework #1

1. In order to estimate the fabrication cost, we need to determine the number of dies in a wafer. Prove the equations in slide 61 of Lecture 1. Then, use the equations in the slide to determine the percentage of wasted silicon (due to the edge of the wafer), as a function of die size. Plot the % wasted area as a function of die size for die sizes from 1 cm to 5 cm in an 8 inch wafer.

$$\text{yield} = \frac{\text{\# good chips per wafer}}{\text{total \# of chips per wafer}} \tag{1}$$

$$\text{die cost} = \frac{\text{wafer cost}}{\frac{\text{dies}}{\text{wafer}} \times \text{die yield}} \tag{2}$$

$$\frac{\text{dies}}{\text{wafer}} = \frac{\pi \left(\frac{\text{wafer diameter}}{2}\right)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}} \tag{3}$$

$$\text{wasted area} = (1 - \text{yield}) \times 100\% \tag{4}$$

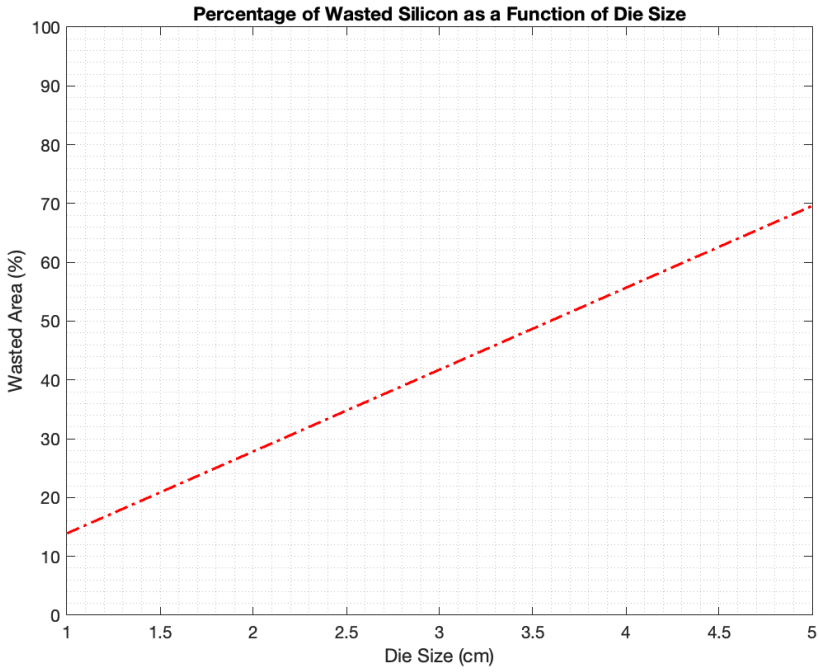

Figure 1: Percentage of Wasted Silicon as a Function of Die Size

2. In this problem, we would like to derive the equation for drain current in saturation region considering channel-length modulation. Assume that the change in channel length is proportional to VDS (i.e. $\Delta L/L = \lambda V_{DS}$). Show how equation (3.29) in your textbook becomes (3.30) when you include channel length modulation.

Channel length modulation gives: $L = L - \Delta L$

$$I_D = \frac{K'n}{2}\left(\frac{W}{L-\Delta L}\right)(V_{gs}-V_t)^2$$

$$= \frac{K'n}{2}\left[\frac{W}{L}\left(1+\frac{\Delta L}{L}\right)\right](V_{gs}-V_t)^2$$

$$= \frac{K'n}{2}\left[\frac{W}{L}(1+\lambda V_{DS})\right](V_{gs}-V_t)^2$$

$$= I'_D(1+\lambda V_{DS})$$

3. Based on the list of previous VLSI projects for ECE520/424 that we discussed in Lecture 1, please suggest at least one new project that you will be interested to design and work on this semester. Please explain in one paragraph the detail of your suggested project. Feel free to use online resources, if you need to.

   I missed the first few lectures, so I do not know the specifics of the project yet, but in my Advanced Computer Architecture class we discussed a hardware-software codesign using ASICs. I am interested in exploring those more and possibly attempting to design one.