Lecture 12 - Review

Thursday, March 5, 2020 10:44 AM

Objectives: - Review materials and concepts covered to date.

1 BYTE - 8 BITS

HALF WORD* - 2 BYTES - 16 bits

WORD* - 4 BYTES - 32 bits

* PIC32

ALIGNMENT REQ'S

ADDRESSES

BYTES - No LIMITS

HALF WORD - MULTIPLES OF 2 ($lsb = 0$)

WORD - - MULTIPLES OF 4 ($2\ lsbs = 0$)

NUMERICAL REPRESENTATION

Values given $X = \{x_{w-1}, x_{w-2} \cdots x_0\}$

UNSIGNED

$$Val = \sum_{i=0}^{w-1} x_i 2^i$$

bit weights

$2^{w-1} \cdots 2^2\ 2^1\ 2^0$

$\cdots\ 4\ 2\ 1$

Max Value

$2^w - 1$

Min Value

0

SIGNED

$$Val = -2^{w-1} x_{w-1} + \sum_{i=0}^{w-2} x_i 2^i$$

Max Value = $2^{w-1} - 1$

Min value = -2^{w-1}

$w = 6$

111 111

-32 16 8 4 2 1

1 0 1 0 1 1

$-32 + 8 + 3 = -21$

HANDY NUMBERS

$2^{10} = 1024 = 1K$

$2^{20} = (1024)^2 = 1M$

STORED PROGRAM COMPUTER

FETCH ⇒ DECODE ⇒ EXECUTE

ARCHITECTURE

VON NEUMANN - COMINGLE DATA & INSTR.

HARVARD - SEGREGATED " & "

ISA

CISC - VARING LENGTH
- ONE TO MANY CLOCK CYCLES
- MANY ADDR MODES
- INSTRUCTIONS ACCESS MEMORY DIRECTLY
- FEW G.P. REGISTERS

RISC - FIXED LENGTH INSTR
- FEW ADDRESSING MODES
- MANY GENERAL PURP. REGS
- FEW ADDR. MODES

ONE INSTR/CLOCK CYCLE

LOAD/STORE - ONLY 2 INST THAT ACCESS MEMORY

GEN PURP REGS - DATA & ADDRESSES

SPECIAL FUNCTION REGISTERS - SFRs
CONFIG HW & PERIPHERALS
COMMUNICATE WITH PERIPHERALS

MIPS ADDRESSING

LW $t1, 20($t0)

$20_{10} = 14_{16}$

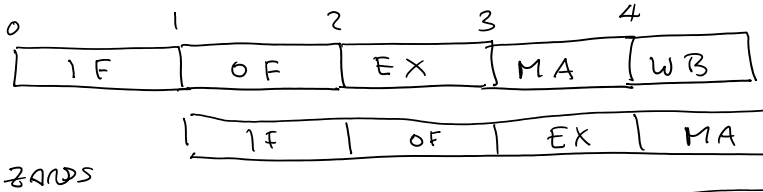
$t0 = 0x\ BF80\ 0000$
$+ \quad 14$
$0x\ BF80\ 0014$

LW $t1, 18($t0)

$0x\ BF80\ 0000$
$+12$
$0x\ BF80\ 0012$

1011 1111 1000 0000 0000 0000 0001 0010

MIPS PIPELINE



DATA HAZARDS

NOT A PROBLEM WITH MIPS

add $t0, $t0, 1

THIS IS A PROBLEM

add $t0, $t0, 1
add $t2, $a0, $t0

THIS IS A PROBLEM
lw $t0, 0x10($t1)
add $a0, $t2, $t0

INSERT A NOP OR AN INSTR NOT USING $t0

CONTROL HAZARD -
BRANCH DELAY
DELAY SLOT - INSTRUCTION FOLLOWING BRANCH

WRITING CODE
STACK OPERATIONS -
USE lw
sw

FUNCTIONS
jal label
jr $ra

MEMORY -
VIRTUAL ADDRESSES
PHYSICAL ADDRESSES -
FIXED MAP TRANSLATION FMT

CONFIGURING THE CLOCK
SYSCLK - 80 MHz
PBCLK - 10 MHz
USBCLK - PRECISE 48 MHz

USE #PRAGMA CONFIG DIRECTIVES FOR CLOCK

PORTS -
TRIS - INPUT OR OUTPUT
LAT - WRITE TO
PORT - READ FROM
ODC - FOR OUTPUT ONLY

OFFSETS FROM SFR ADDRESS TO

CLR, SET & INV

4 8 0xC

TIMERS