ECE338
Lab #2: Behavioral-to-Schematic Translation, index statement
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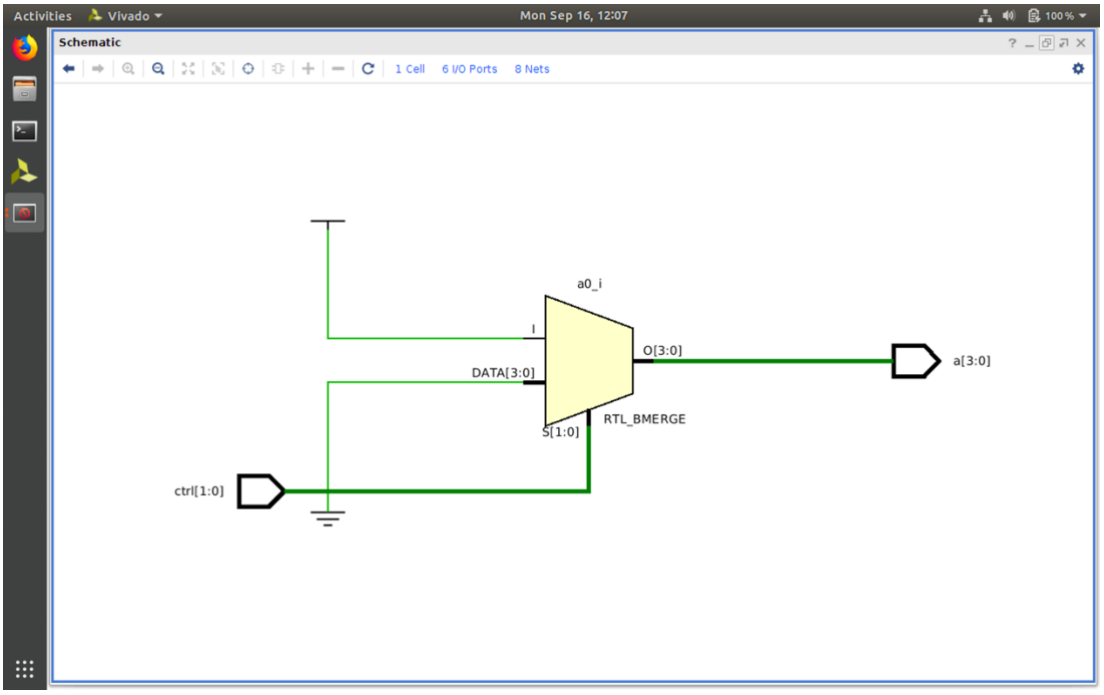
For Lab #2, we were tasked with implementing an indexed simple assignment within a process block that assigns a value to our signal *au* (a unsigned) outside the process block, then assigns subsequent values to *au* inside the process block. We made sure to follow the Golden Rules (i.e. all signals read in process blocks are in the sensitivity list, last assignments take precedent, all assignments have default values, no signals are on both sides of equations, and we only assigned a value to *au* outside the process block once).



In the Synthesized Design Schematic, all of the multiplexers are represented by LUTs (lookup tables). This provides us with a detailed view of our behavioral VHDL code, as *a* receives the output of the unsigned value of *au*.