ECE 322L
Electronics 2

01/23/20 - Lecture 2

MOSFETs, transistors as amplifiers, Q point and DC analysis

Updates

- First lab next week. Lab assignments will be posted on UNM learn in advance of the lab sessions.
- Lab sessions have been consolidated into one that will occur on Wednesday 3:30-6:00 pm.
- The first homework will be posted on UNM Learn on Thu, Jan 30th 2020 and it will be due a week later. Both soft and hard copies will be accepted. The TA will post a link for online submission of soft copies. I will collect hard copies in class.
- I will post selected practice problems on UNM Learn.
- I will post draft slides of the following lecture on UNM Learn. Download the final version of the slides after class.

What are you going to learn in module 1?

- Physical structure of the MOS transistor and how it works.
- How the transistor can be used to make an amplifier.
- How to obtain linear amplification from the fundamentally nonlinear MOS transistor.
- The three basic ways for connecting a MOSFET to construct amplifiers with different properties.
- Practical circuits for MOS-transistor amplifiers that can be constructed using discrete components.

Overview of Lecture 2

- Review of MOSFET behavior

  (Neamen-3.1, S&S-5.1-5.2)
- Transistor as amplifier

  (S&S 5.4.1-5.4.4)
- Intro to DC analysis of transistor behavior

  Q-point

  Load-line

  (Neamen 3.2, S&S 5.4.5-5.4.6)

Structure of MOSFET

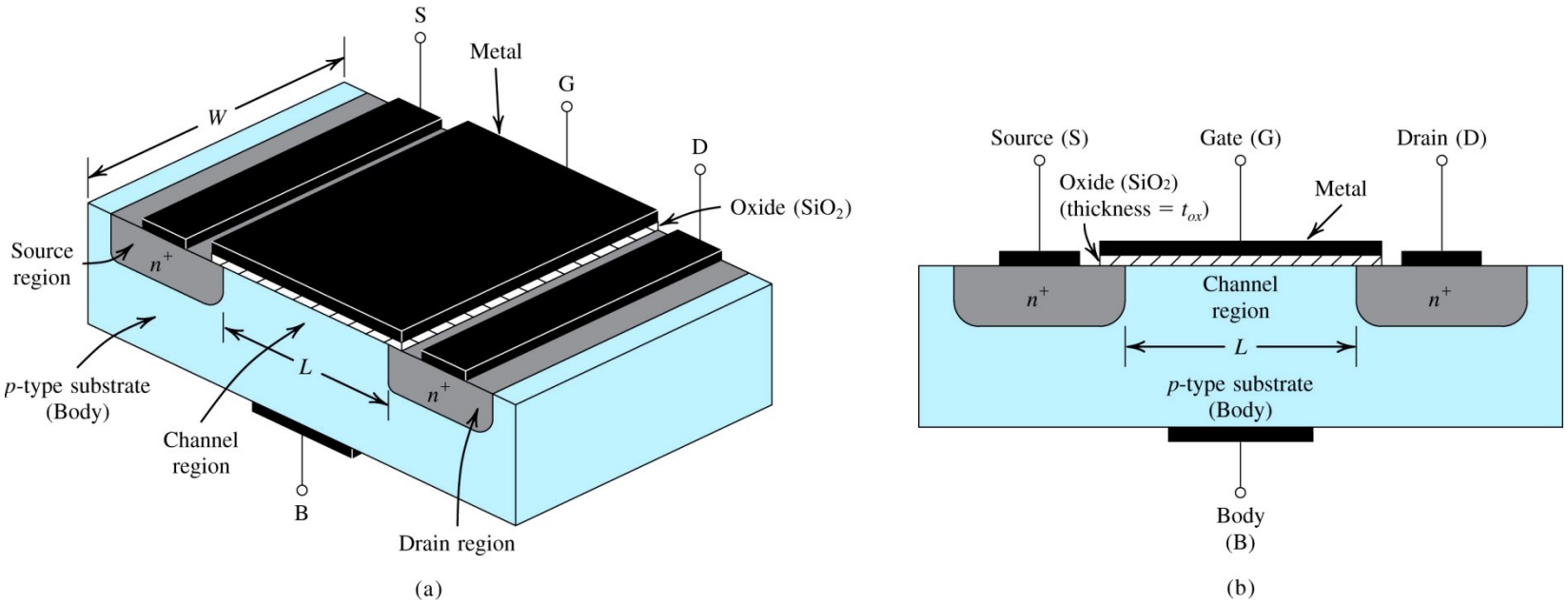
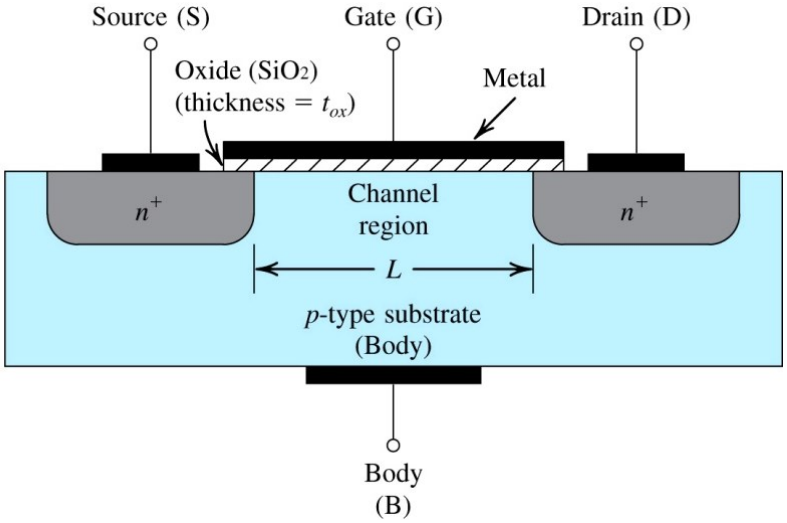
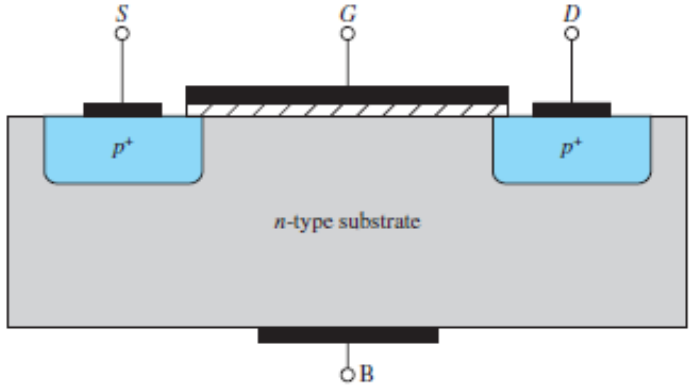
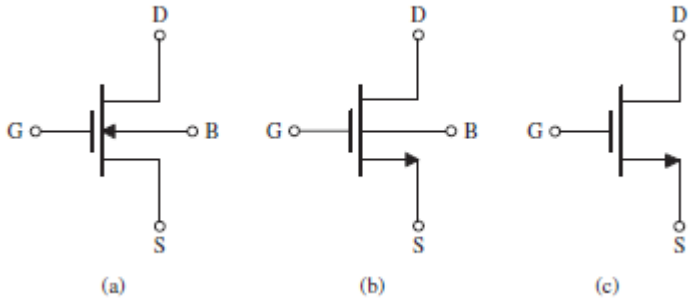


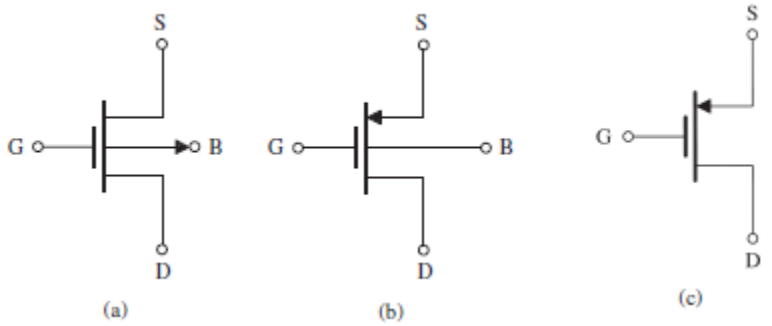
Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 0.03 μm to 1 μm, W = 0.1 μm to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.

n-channel and p-channel FETs





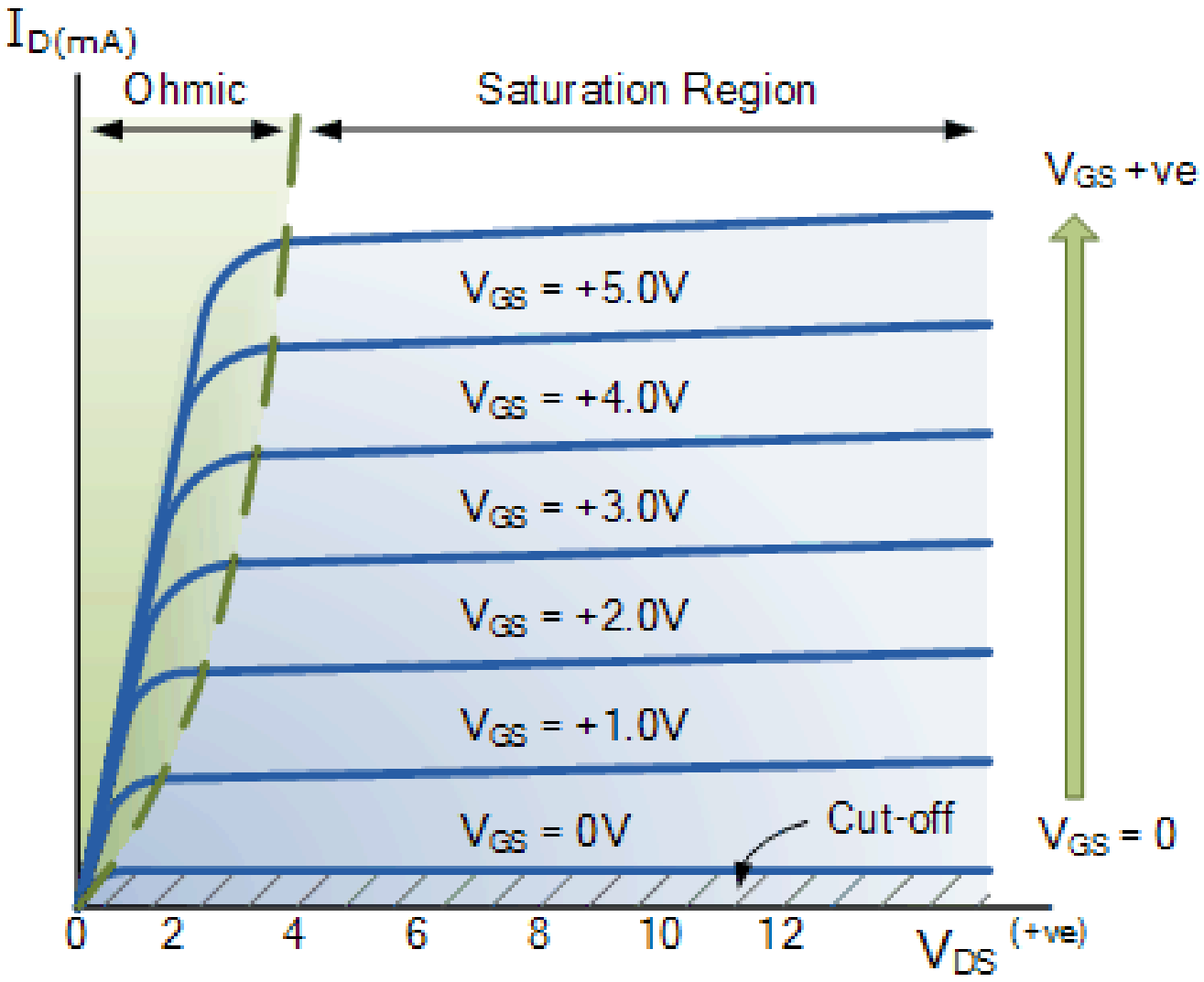




Electron inversion channel
Positive threshold voltage

Hole inversion channel
Negative threshold voltage

NMOS (output) characteristics



(Cut-off) Operation at zero V_{GS}

- With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
- "They" prevent current conduction from drain to source when a voltage v_{DS} is applied.
  - yielding very high resistance ($10^{12} ohms$)

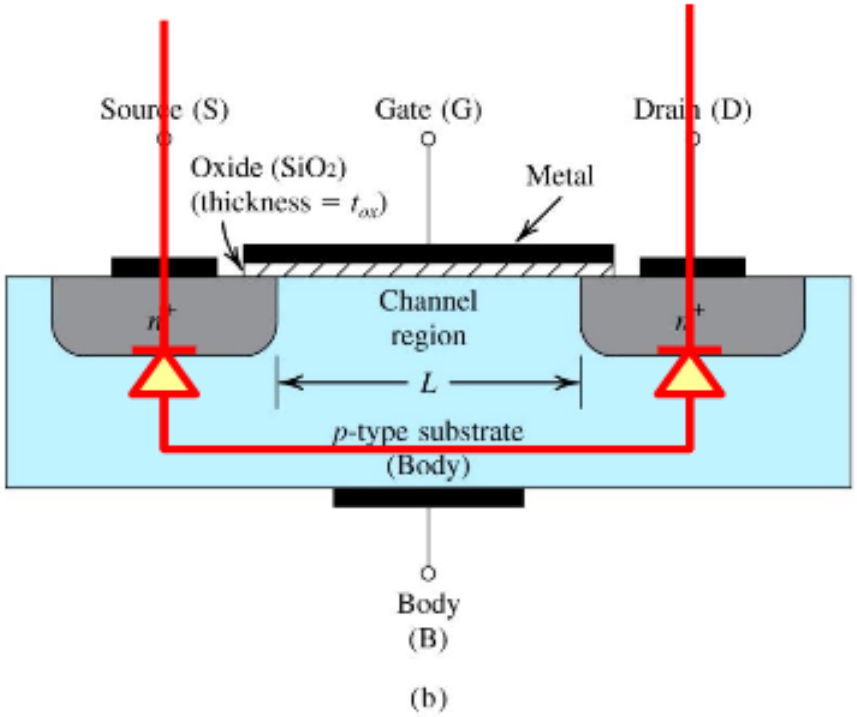


Figure 5.1: Physical structure...

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(Cut-off) Operation at $0<V_{GS}<V_{TN}$

Q: What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? Refer to figure to right.

v_{GS} is applied to the gate terminal, causing a positive build up of positive charge along metal electrode.

This "build up" causes free holes to be repelled from region of *p*-type substrate under gate.

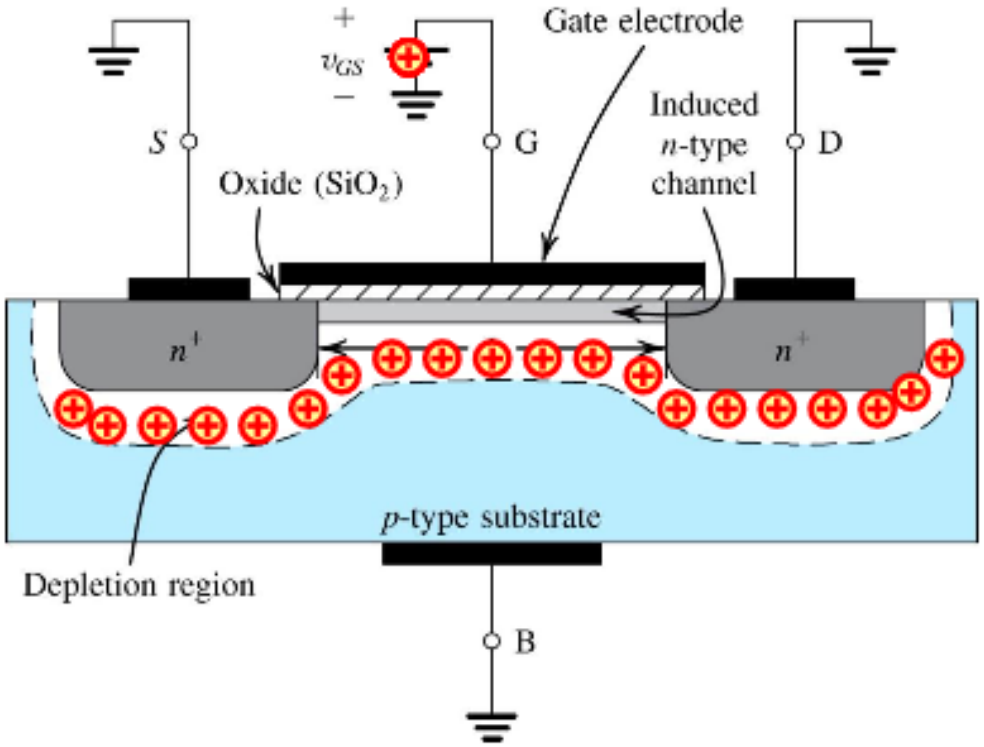

Figure 5.2: The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate

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(Cut-off) Operation at $0<V_{GS}<V_{TN}$

This "migration" results in the uncovering of negative **bound charges**, originally neutralized by the free holes

The positive gate voltage also attracts electrons from the n^+ source and drain regions into the channel.

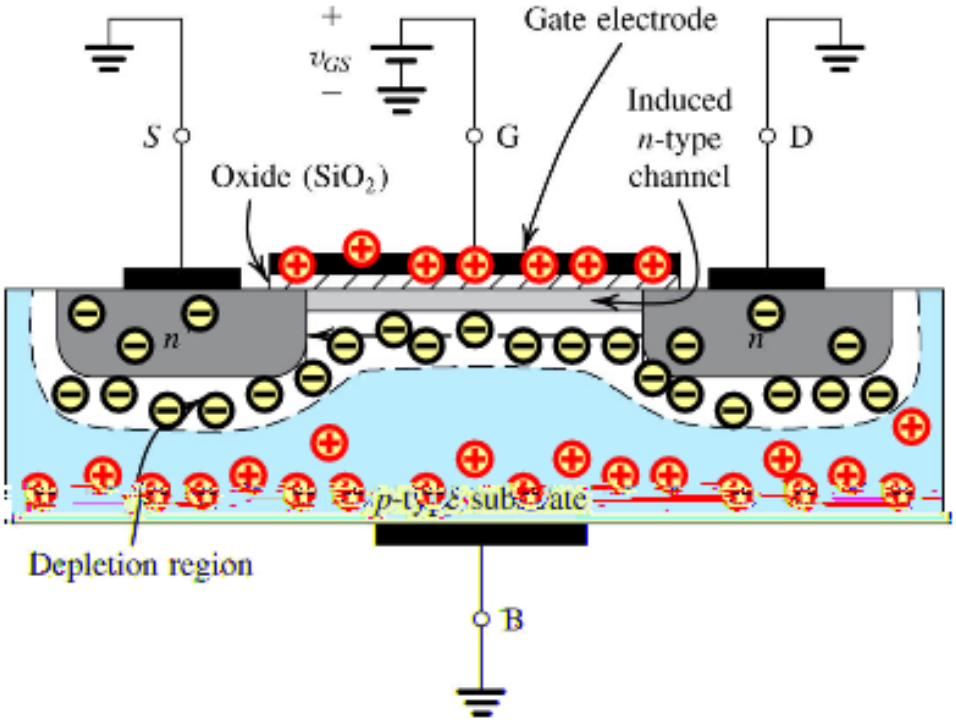

Figure 5.2: The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate

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Operation at Threshold ($V_{GS}=V_{TN}$)

Once a sufficient number of "these" electrons accumulate, an *n*-region is created…

- …connecting the source and drain regions

This provides path for current flow between *D* and *S*.

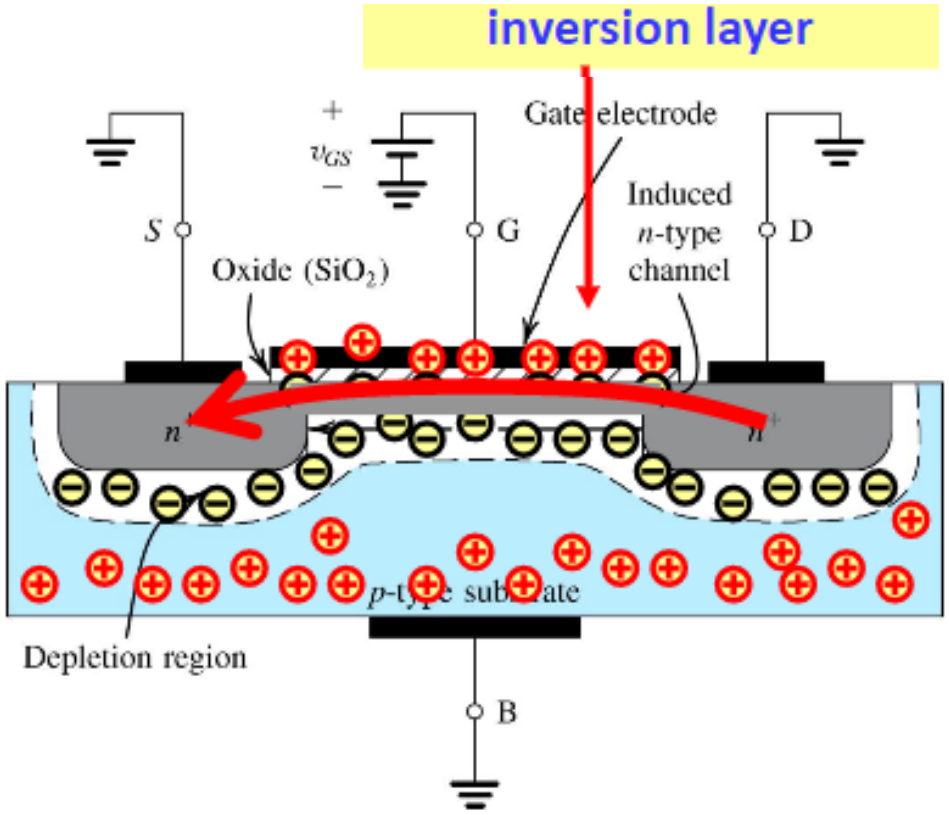

Figure 5.2: The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate

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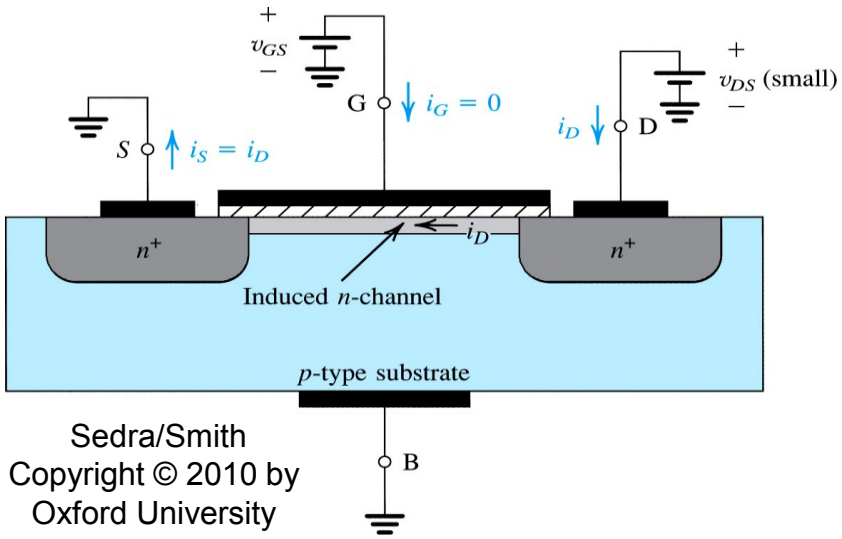
Operation in Triode or Linear Region



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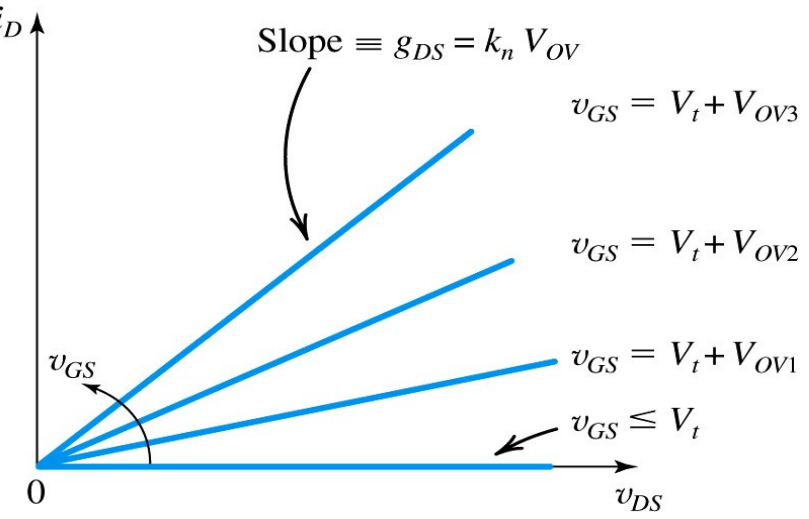


Figure 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

Figure 5.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistance whose value is controlled by v_{GS}.

$$i_D = \left(C_{ox} W v_{OV}\right)\left(\frac{\mu_n v_{DS}}{L}\right) \text{ in } A$$

$$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{\left(\mu_n C_{ox}\right)\left(\frac{W}{L}\right)v_{OV}} \text{ in } \Omega$$

$$v_{OV} \equiv v_{GS} - V_t$$

Triode to Saturation

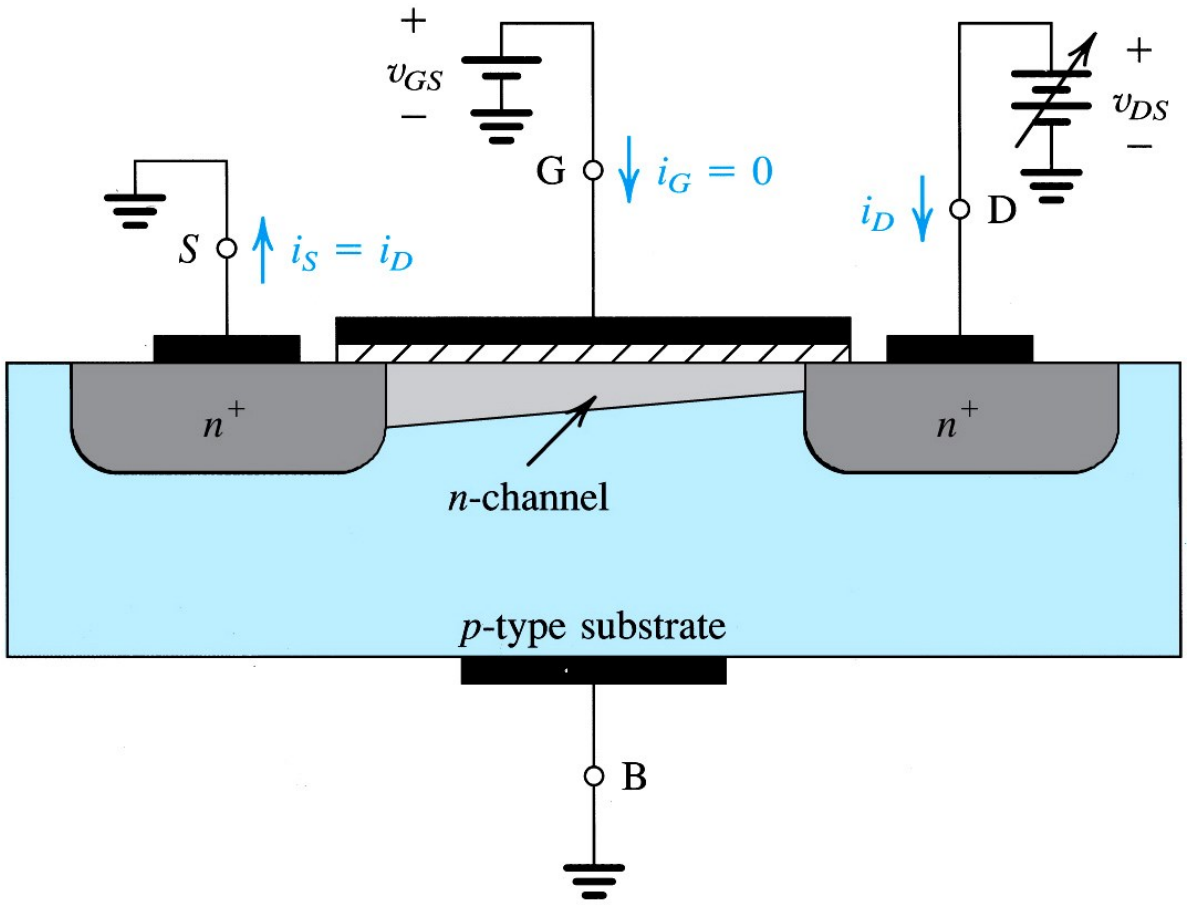
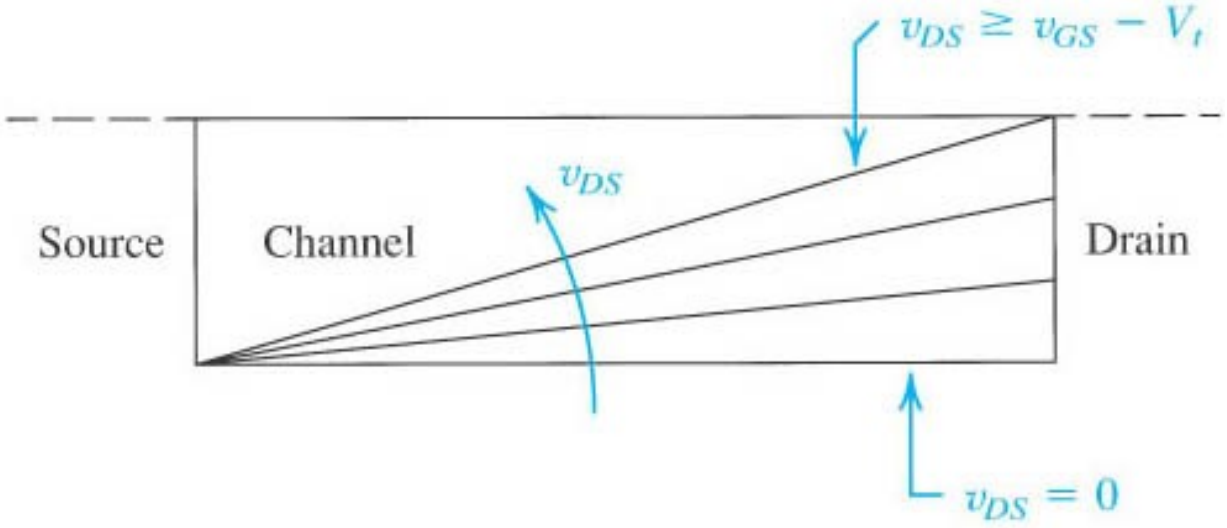


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t; $v_{GS} = V_t + V_{OV}$.

Operation in Saturation



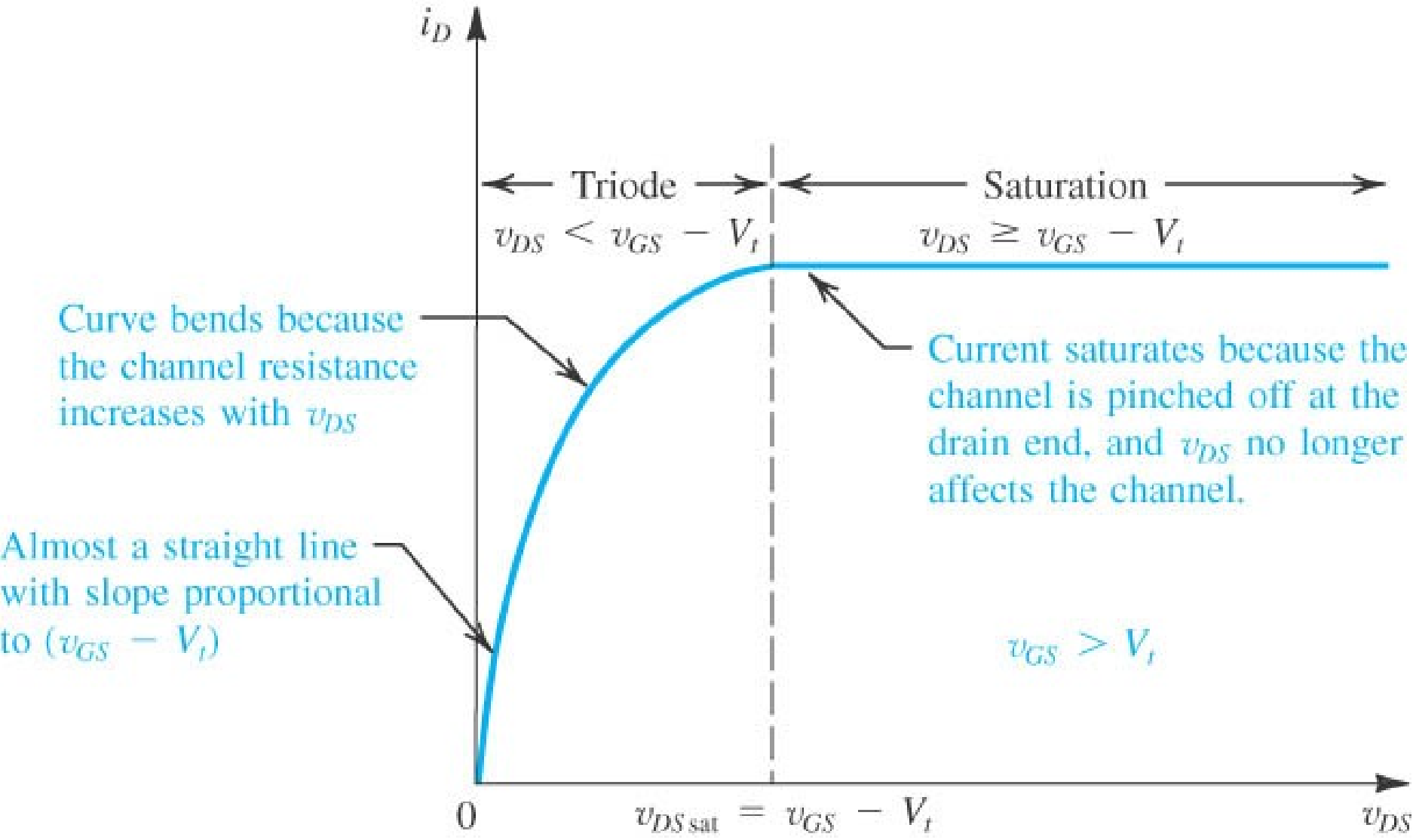
- Increase V_{DS} → Decrease V_{GD} → less electrons at the drain side of the channel

- When $V_{DS} \geq V_{GS} - V_t$ then $V_{GD} \leq V_t$ so no channel exists at the drain side. The channel "***pinches-off***"

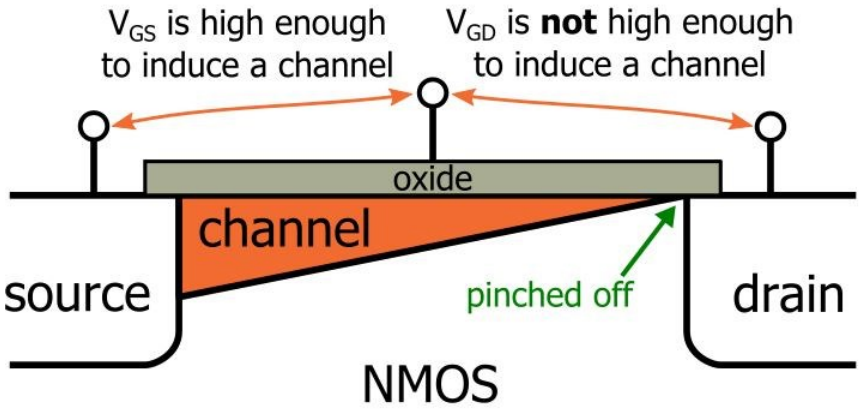
- When channel pinches off, electrons still flows from S to D
  - ✓ Electrons are diffused from the channel to the depletion region near D, where they are drifted by the lateral *E-field to the D*

- Further increase of V_{DS} - no effect on the channel - current is "saturated" and the transistor is in "***Saturation Mode***"

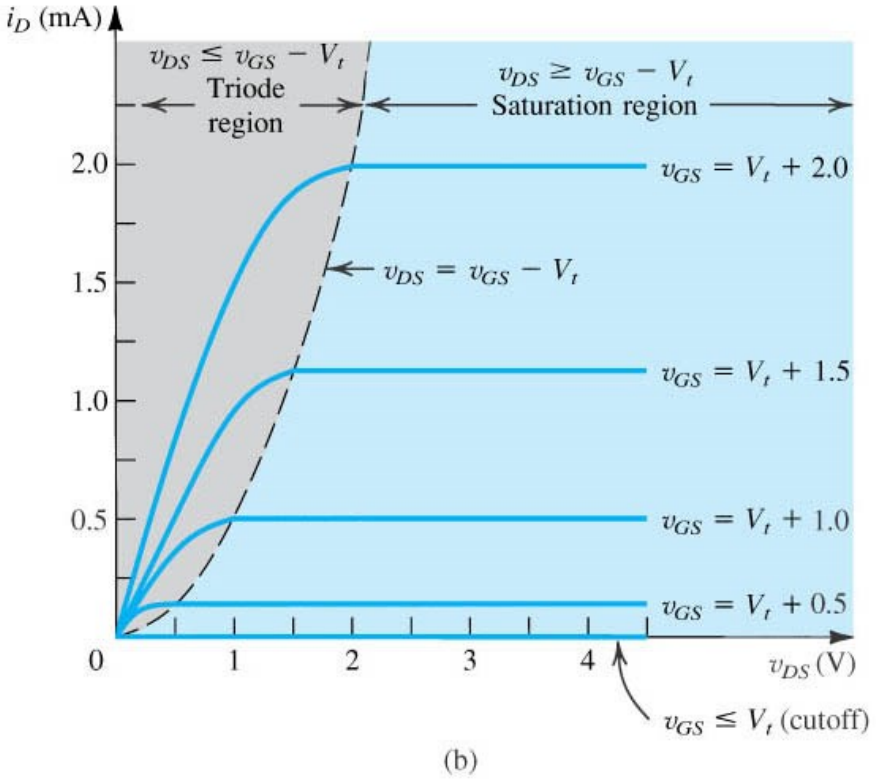
I-V characteristics: summary



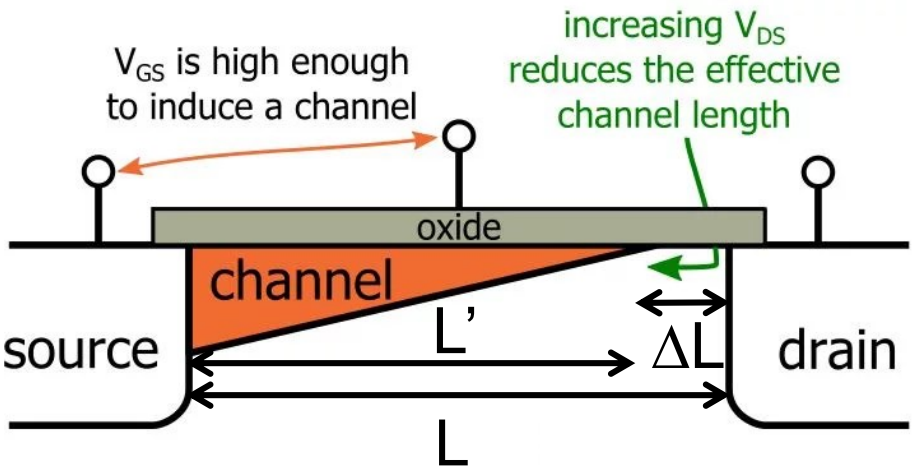
MOSFET in Saturation



- At $V_{DS}>V_{GS}- V_T$ the V_{GD} is lower than V_T. Thus, the channel pinches off at the drain side or the inversion charge is zero at the drain side.
- Carriers can still reach the drain as they are swept through the depletion region at the drain side by the electric field across it.
- Any increase of V_{DS} above $V_{GS}-V_T$ drops across this depletion region and hence it does lead to any increase of the I_D. Thus there is a finite resistance between drain and source



Channel modulation effect in MOSFETs



Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

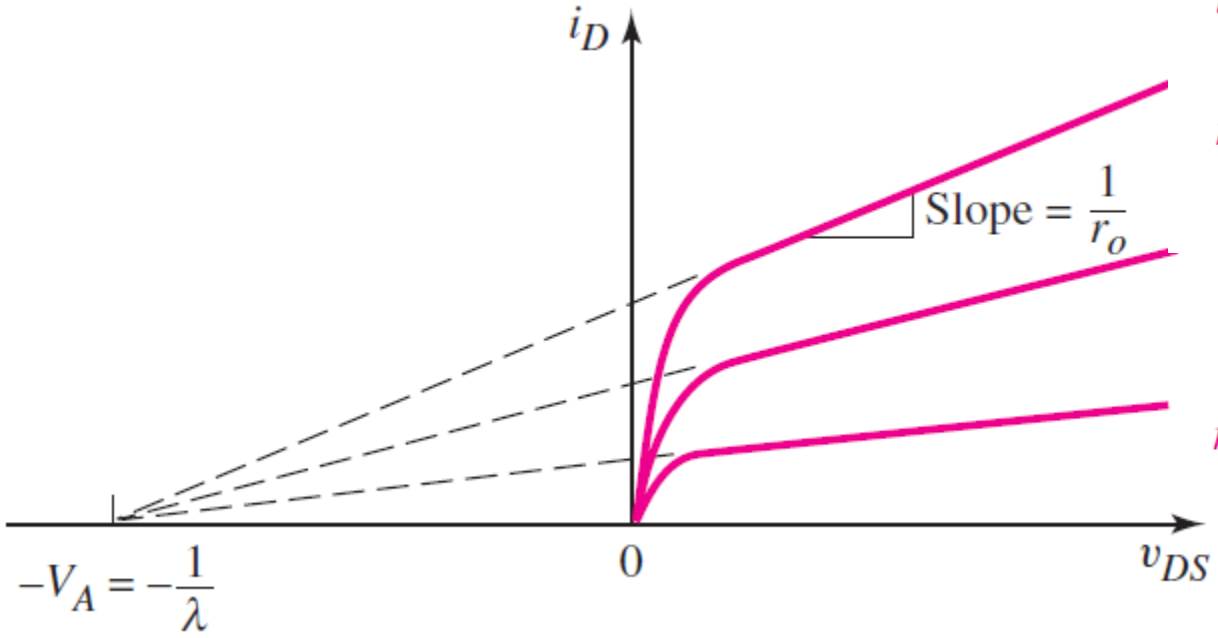
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS}-V_{TH})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L-\Delta L}(V_{GS}-V_{TH})^2 \qquad \frac{\Delta L}{L}<1 \Rightarrow I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\frac{\Delta L}{L})$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) \qquad \frac{\Delta L}{L}=\lambda V_{DS}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\frac{V_{DS}}{V_A})$$

Channel modulation effect in MOSFETs



$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})]$$

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}}$$

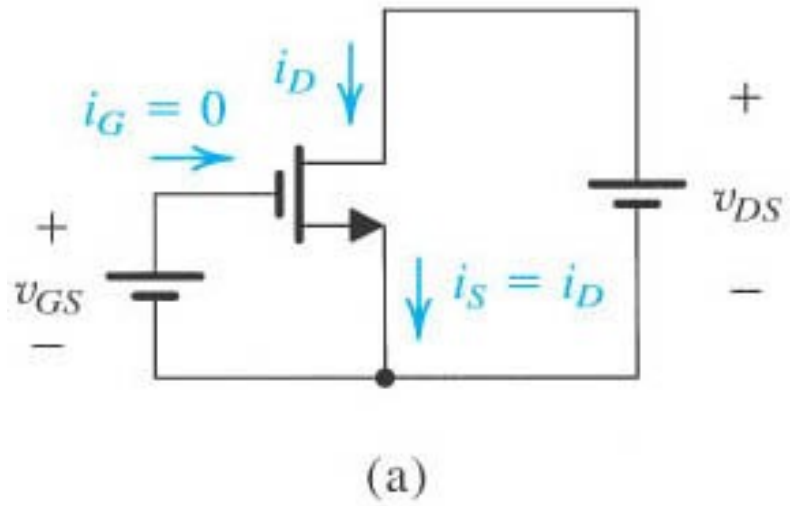
$$r_o = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1}$$

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

V_A: *Early voltage*

λ: *Modulation channel parameter*

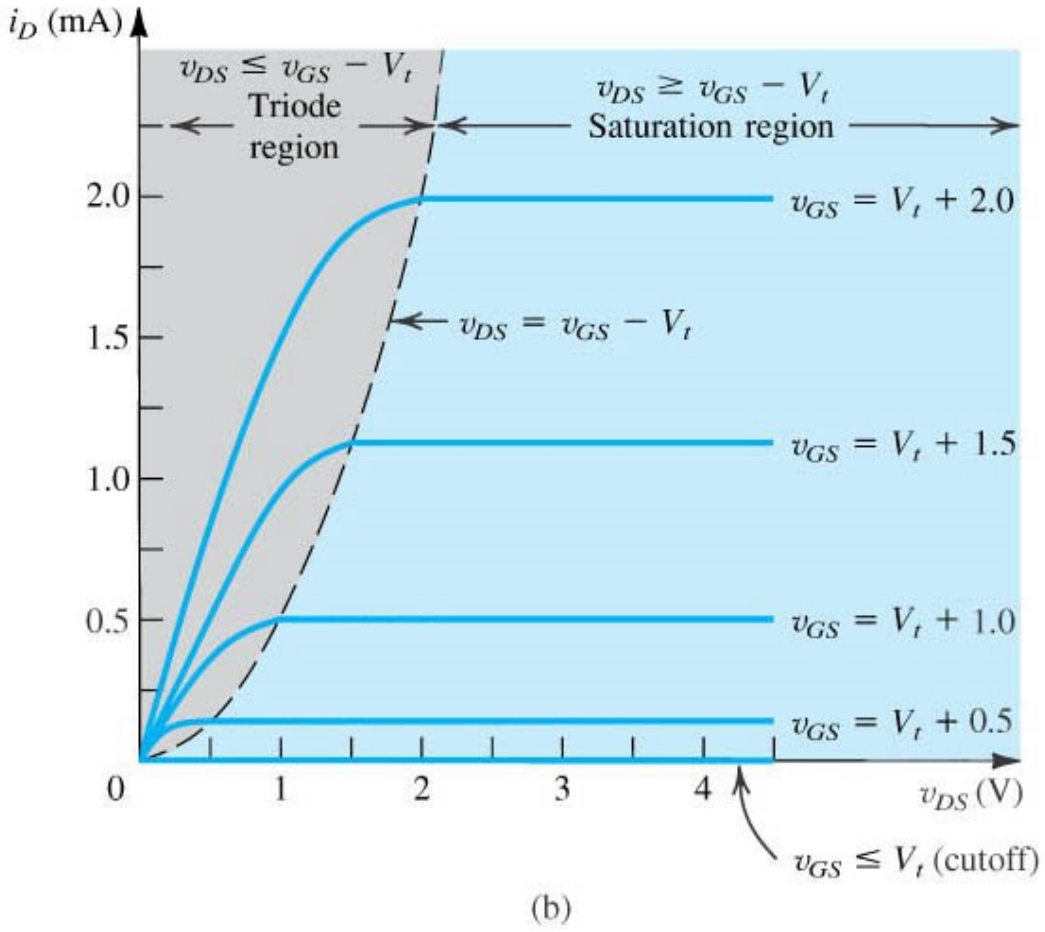
I-V characteristics: summary



(a)

$\lambda = 0$

$V_A = \infty$



(b)

Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.

I-V characteristics: summary

Region	NMOS	PMOS
Nonsaturation	$v_{DS} < v_{DS}(sat)$ $i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$v_{SD} < v_{SD}(sat)$ $i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation	$v_{DS} > v_{DS}(sat)$ $i_D = K_n[v_{GS} - V_{TN}]^2$	$v_{SD} > v_{SD}(sat)$ $i_D = K_p[v_{SG} + V_{TP}]^2$
Transition Pt.	$v_{DS}(sat) = v_{GS} - V_{TN}$	$v_{SD}(sat) = v_{SG} + V_{TP}$
Enhancement Mode	$V_{TN} > 0V$	$V_{TP} < 0V$
Depletion Mode	$V_{TN} < 0V$	$V_{TP} > 0V$

$\lambda = 0 \; V_A = \infty$

Transconductance Parameter

Process transconduction/ transconductance/conduction parameter

$$k'_{n,p} = \mu_{n,p} C_{ox} \qquad [A/V^2]$$

$C_{ox} = \varepsilon_{ox} / t_{ox}$: gate oxide capacitance per unit area [F/cm^2]

$\mu_{n,p}$ is the mobility of the electrons/holes in the inversion layer [cm^2/Vs]

Transconduction/ transconductance/conduction parameter

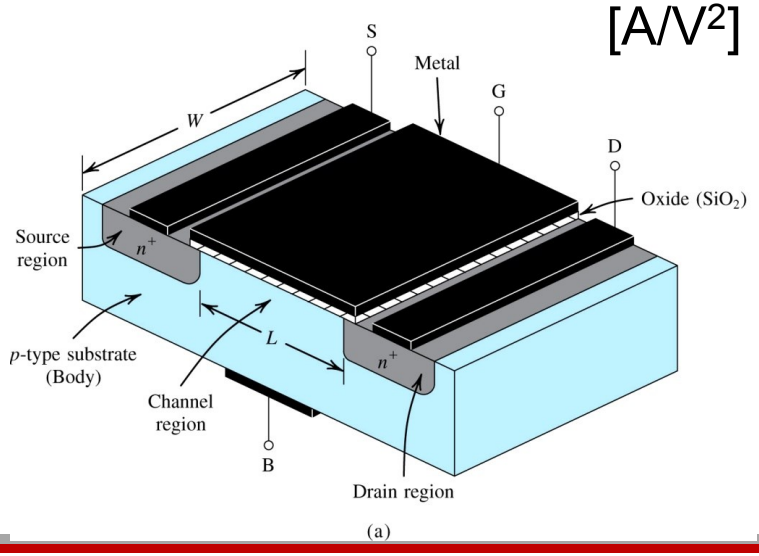
Neamen

$$K_{n,p} = \frac{W \mu_{n,p} C_{ox}}{2L} = \frac{k'_{n,p}}{2} \frac{W}{L} \qquad [A/V^2]$$

W: Channel width; L: Channel length; W/L: Aspect ratio

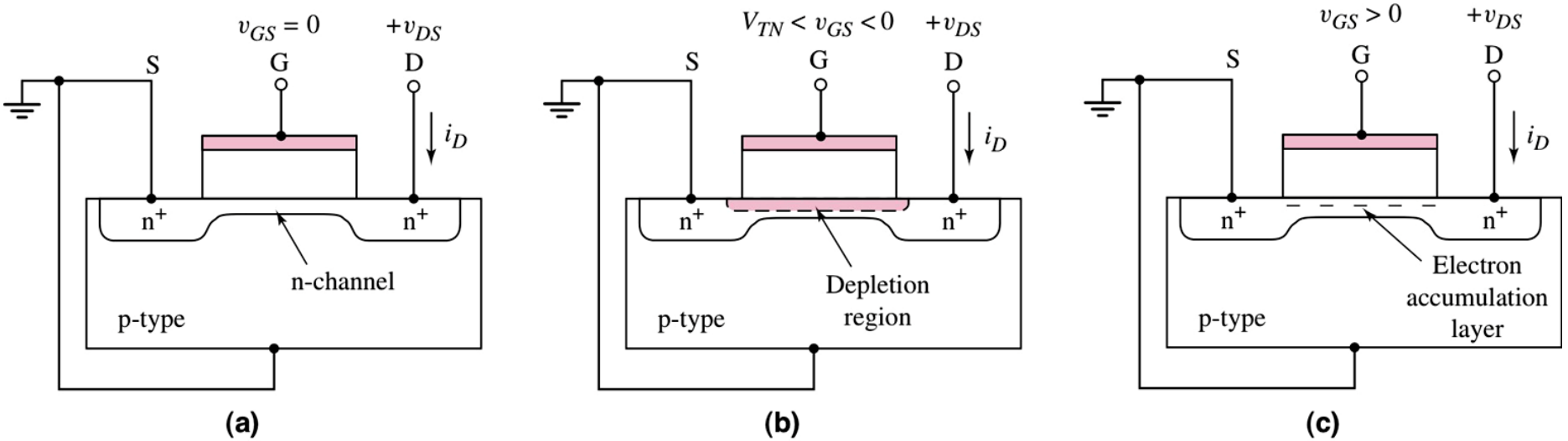
Sedra&Smith

$$k_{n,p} = \frac{W \mu_{n,p} C_{ox}}{L} = k'_{n,p} \frac{W}{L} \qquad [A/V^2]$$



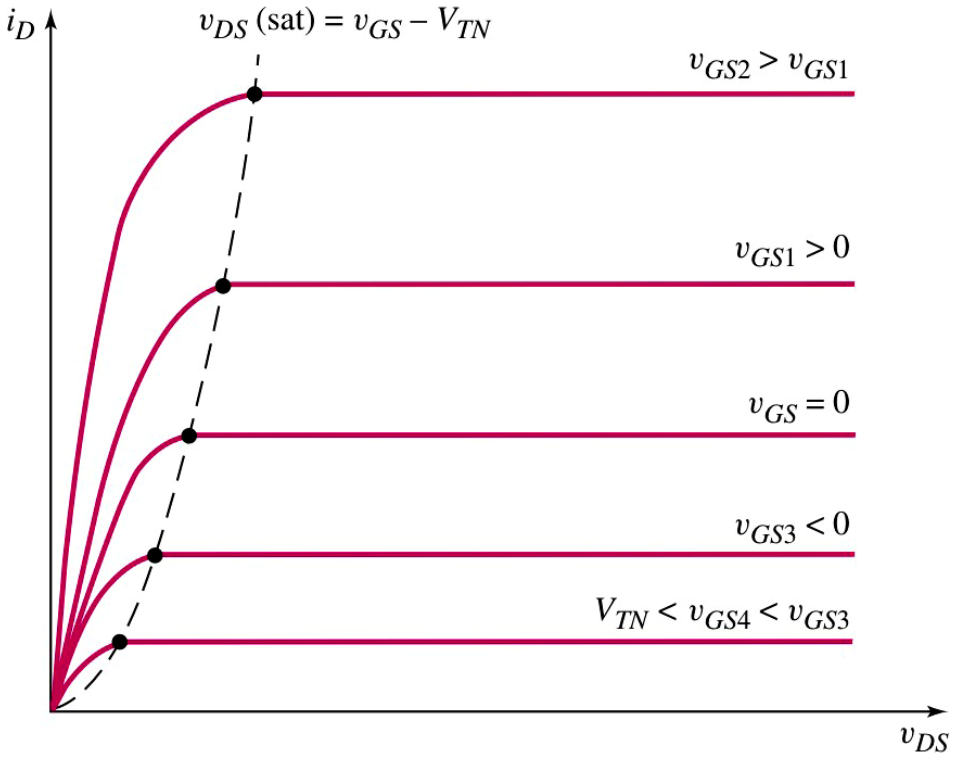
(a)

Depletion-mode N-MOSFET

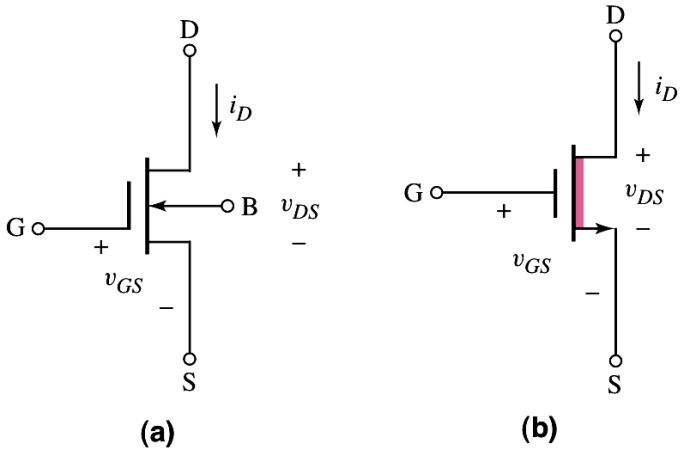


Depletion-mode N-MOSFET

Output characteristics

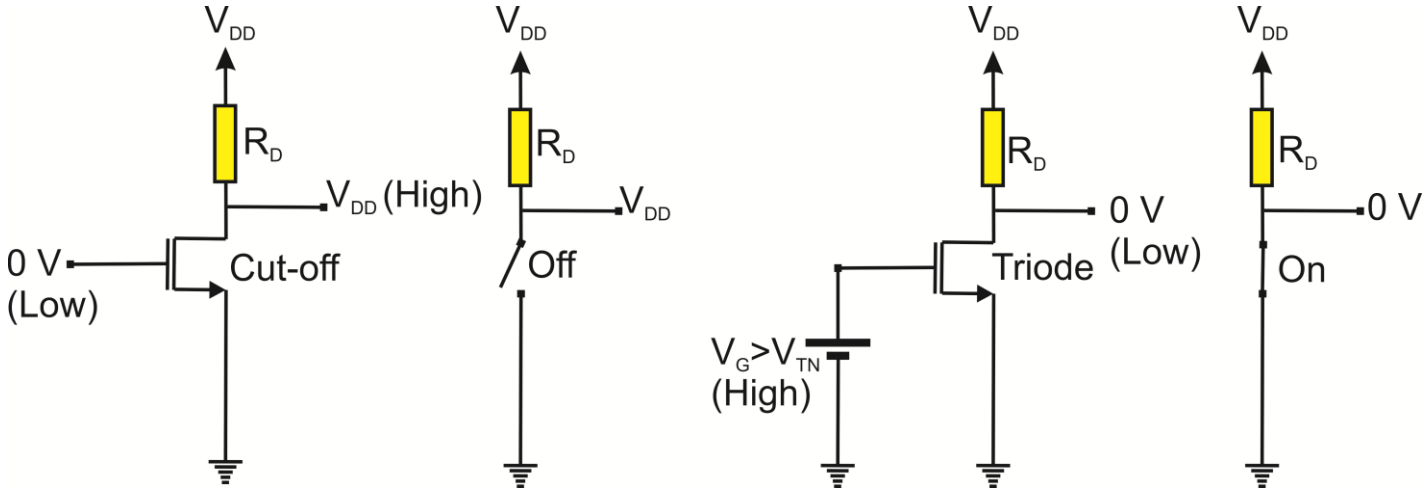


Symbols



Transistors in Digital and Analog Electronics

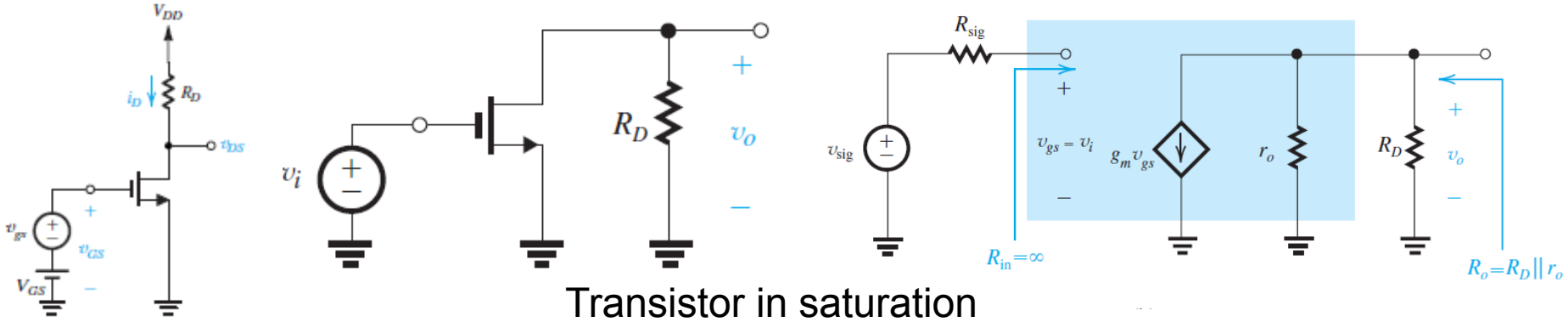
Digital electronics: Transistors as switches



Transistor in cut-off

Transistor in triode

Analog electronics: Transistors as amplifiers

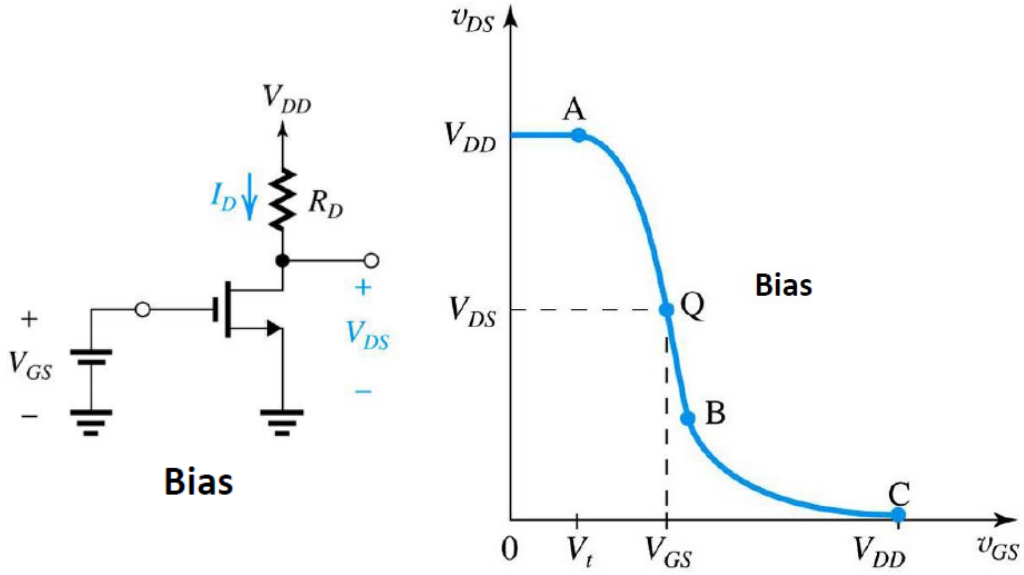


Transistor in saturation

Different applications require transistors to operate in different regions

The Q point

The operating point of a device, also known as bias point, quiescent point, or **Q-point**, is the steady-state (DC) voltage or current at a specified terminal of an active device with no input signal applied.

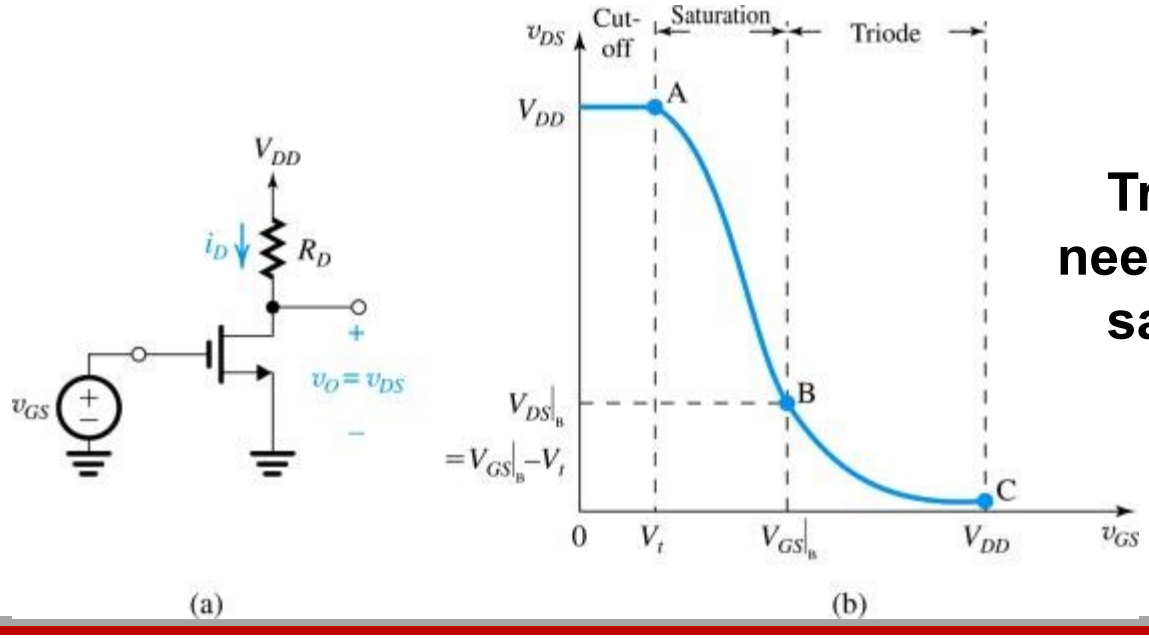


The Q point of the device is determined by the DC network which supplies this steady current or voltage. This network is called the bias circuit or the biasing circuit.

Transistors as Amplifiers

The job of an amplifier is to increase the amplitude of an input signal without altering its waveform.

Ideally, amplifiers will have a linear transfer function (Output/input)



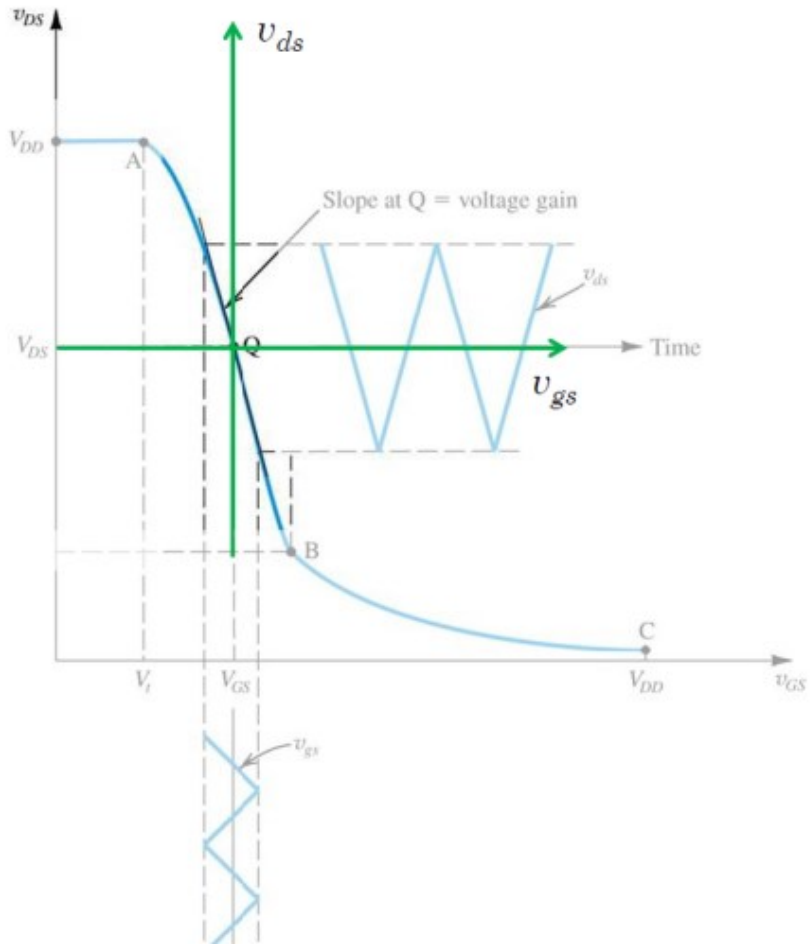
Transistor needs to be in saturation

Transistors as Amplifiers

Signal and response

$$v_{GS} = V_{GS} + v_{gs}$$
$$v_{DS} = V_{DS} + v_{ds}$$
$$i_D = I_{DS} + i_d$$

Bias

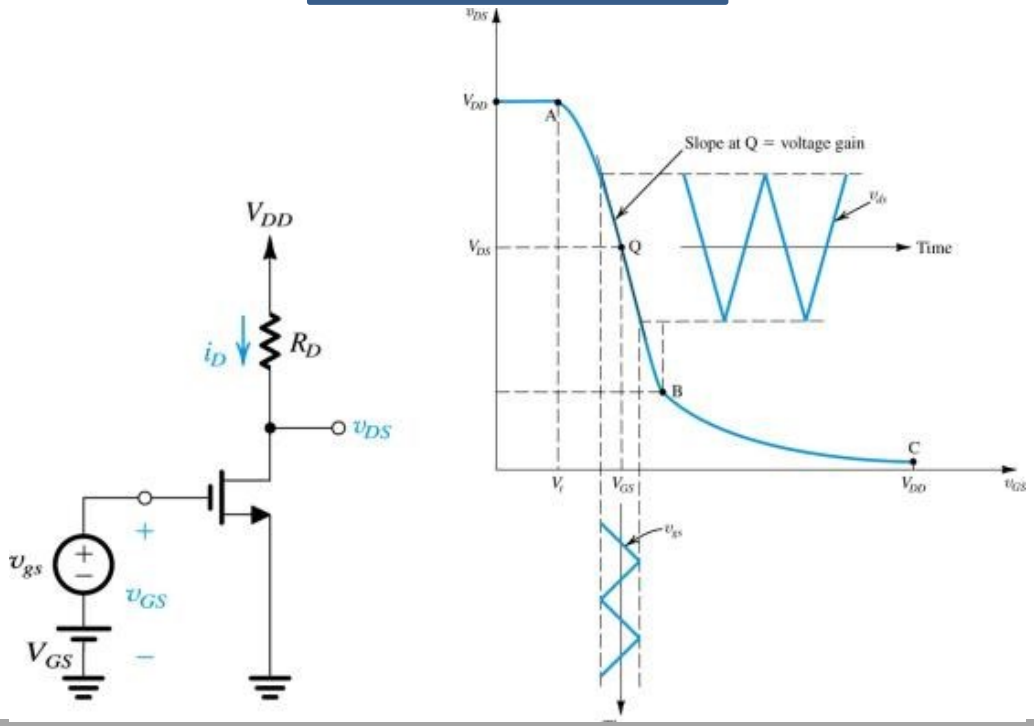


1. Design/Determine the operating point (DC)
2. Design/Determine response to the input (DC+AC)

Transistors as Amplifiers

Essential step in the design of an amplifier circuit is to establish an appropriate operating point for the transistor (Bias design).

V_{in}(DC bias)+V_{in}(AC) → **Amplifier A=constant** → A*[V_{in}(DC bias)+V_{in}(AC)]

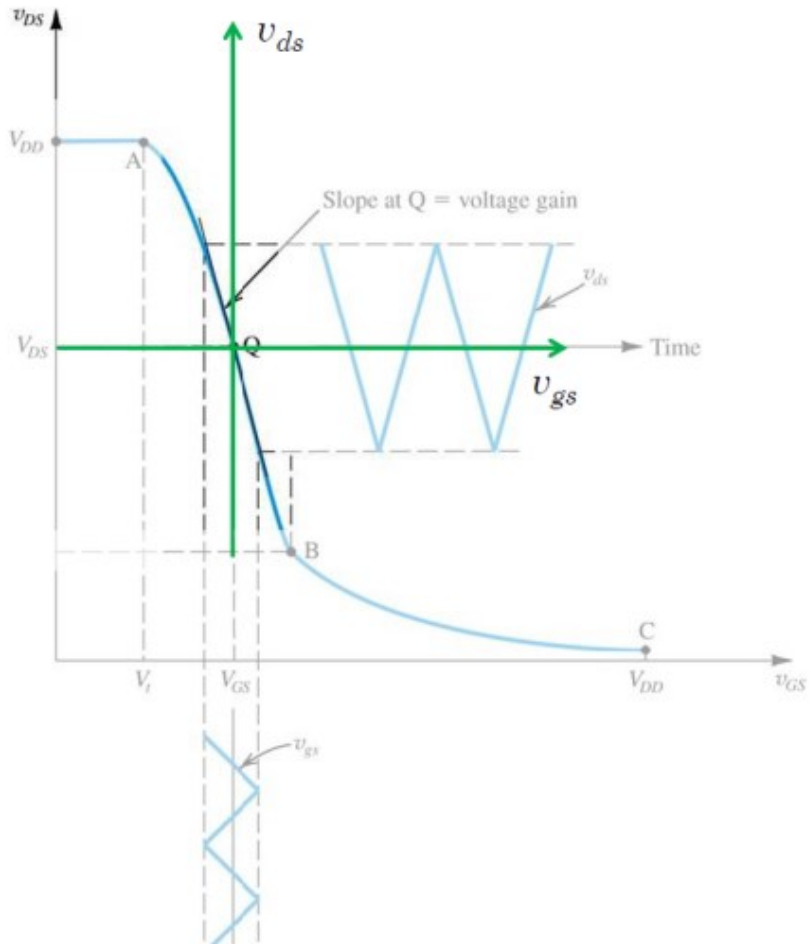


Desired Characteristics of the Operating Point

Signal and response

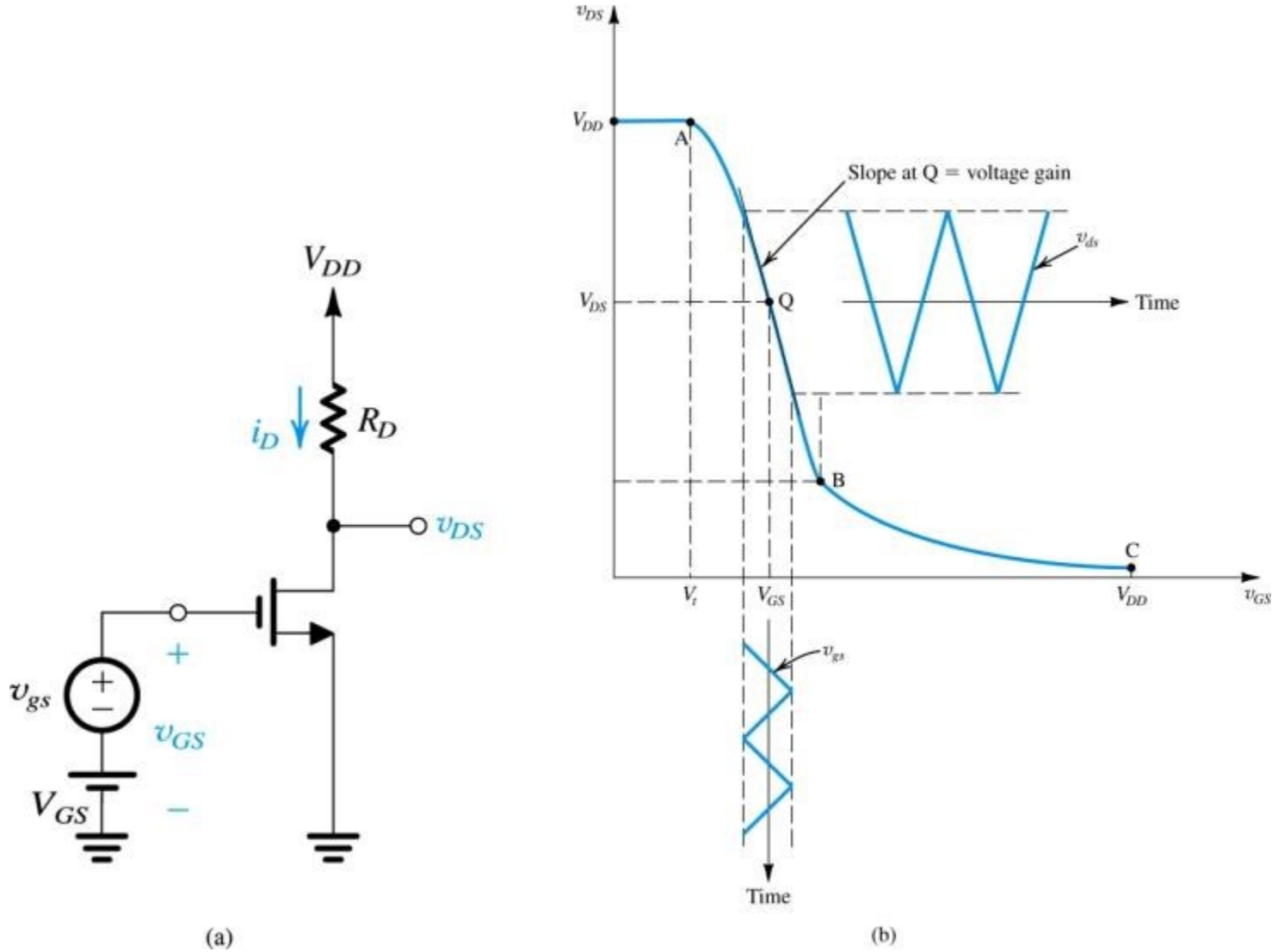
$$v_{GS} = V_{GS} + v_{gs}$$
$$v_{DS} = V_{DS} + v_{ds}$$
$$i_D = I_{DS} + i_d$$

Bias



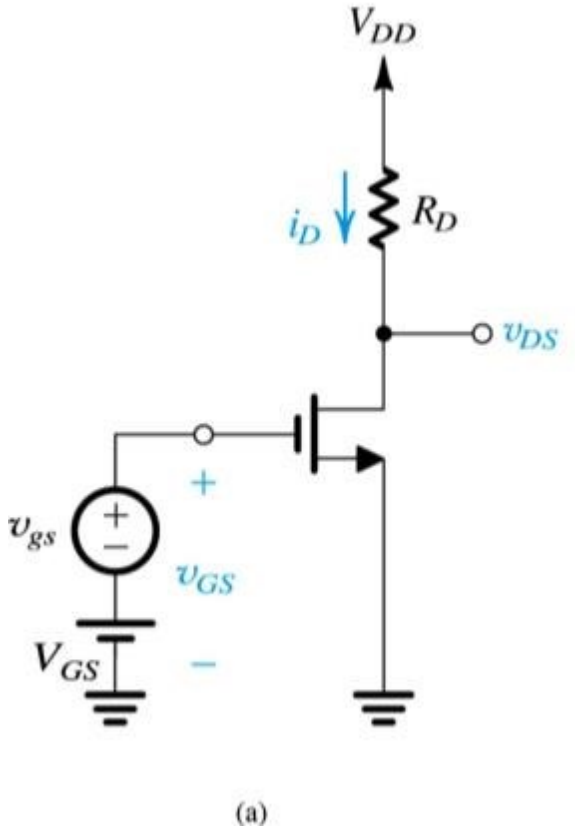
Stable and predictable I_D,V_{GS}, and V_{DS} that ensure operation in the saturation region for all expected input signal levels.

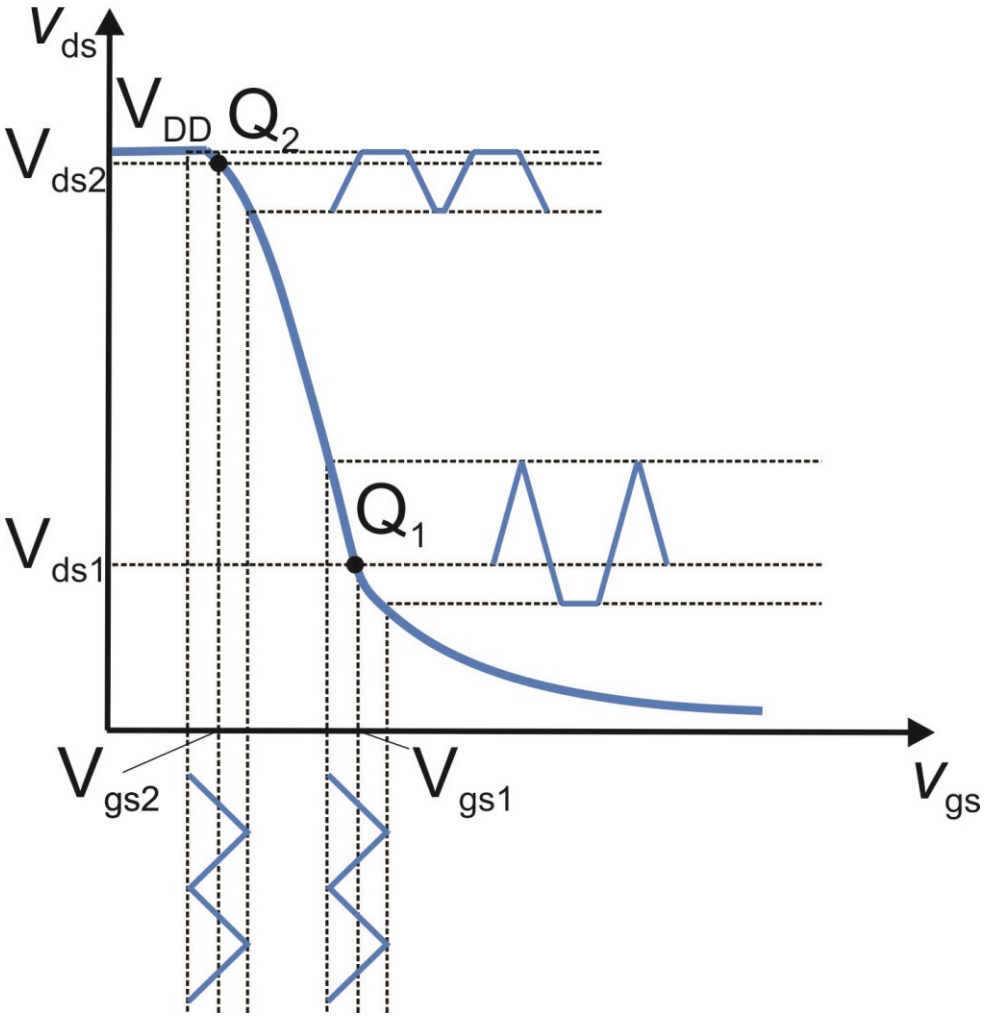
Desired Characteristics of the Operating Point



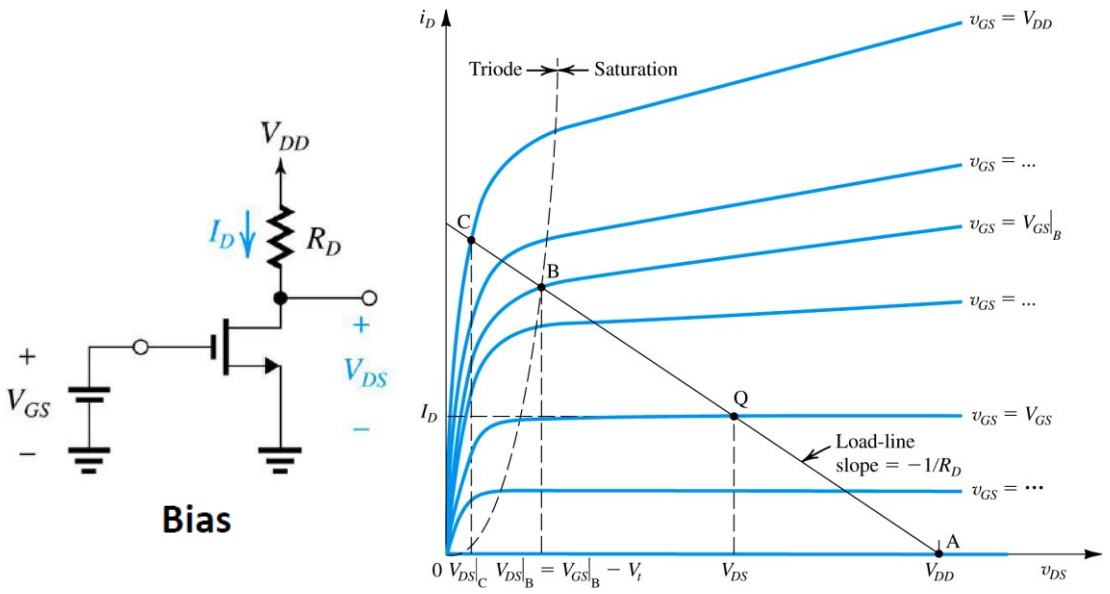
What's the best operating point within saturation?

Desired Characteristics of the Operating Point



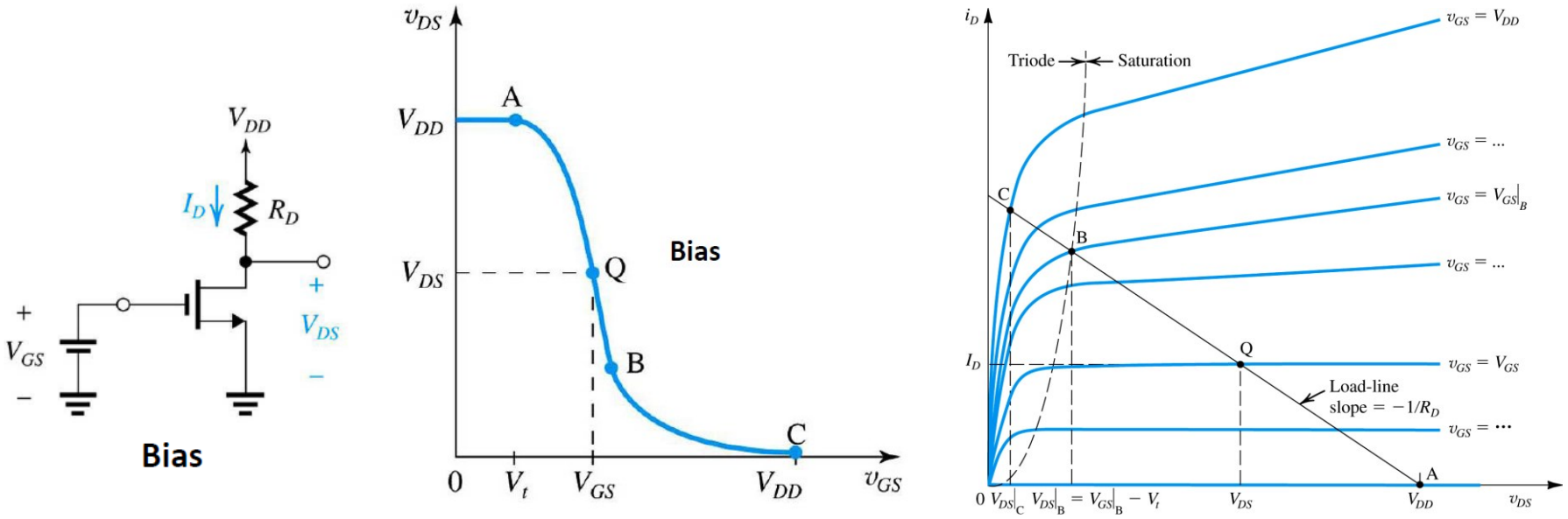


The Load Line



- Represents the constraint that the linear part of the circuit places on a non-linear device, like a diode or a transistor.
- Unless otherwise specified, the load line is sketched in the plane of the output current-voltage characteristic of the non-linear device.
- The points where the characteristic of the non-linear device and the load line intersect are the possible operating point(s) (Q points) of the circuit; at these points the current and voltage parameters of both parts of the circuit match.

The Load Line



The load line is a useful tool to determine the Q point of a device and to verify that a transistor operates (or it is biased) in the desired region, i.e., in saturation, if used as an amplifier.

In-class problem 1

Sketch the load line for the circuit below

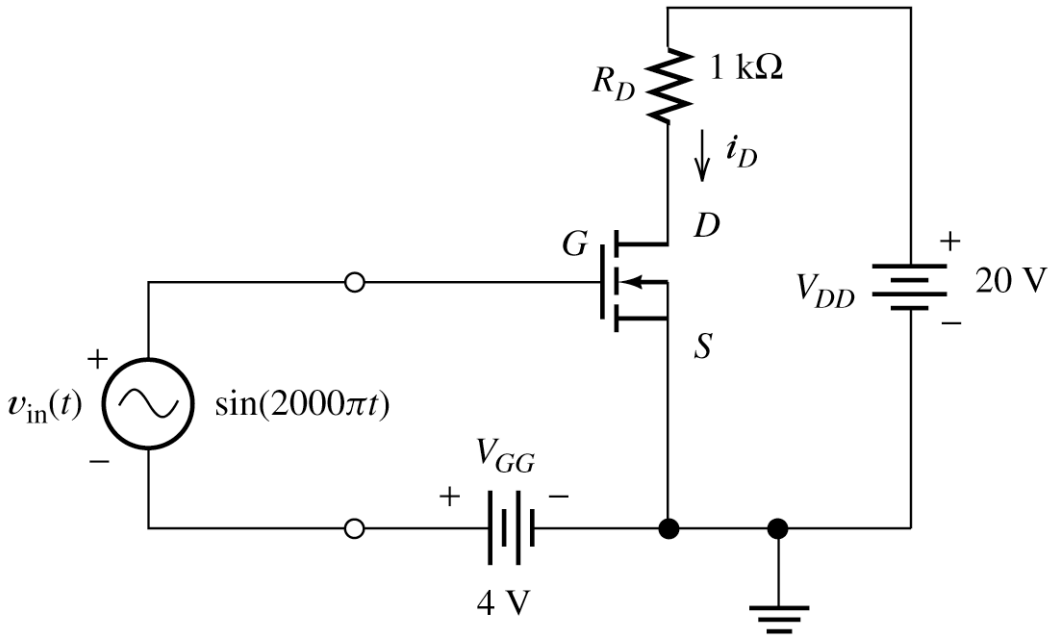
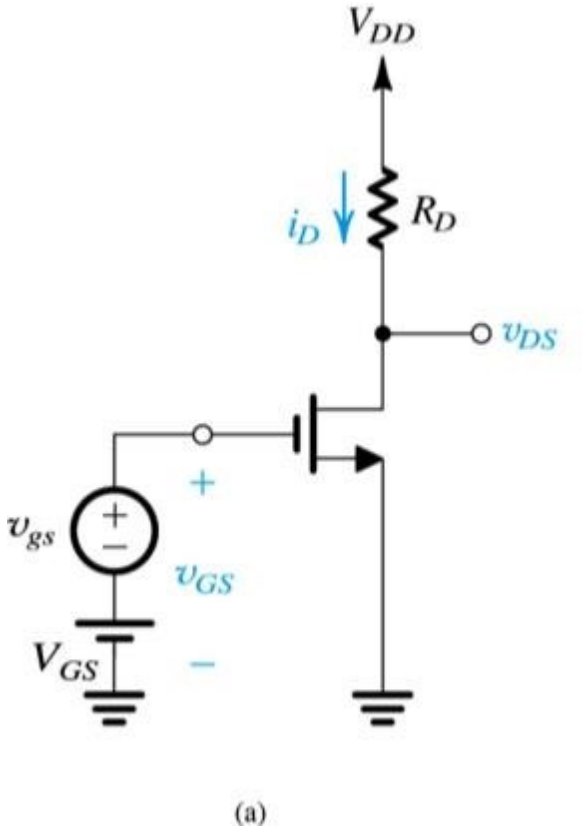


Figure 12.10 Simple NMOS amplifier circuit.

How to sketch the load line



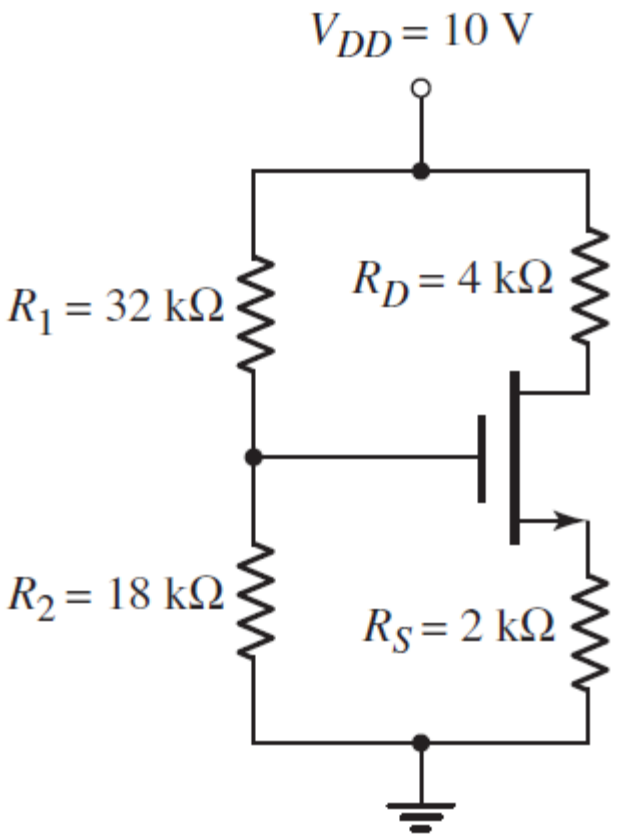
(a)

- Shut down the ac input signal
- Determine an equation that relates output current and output voltage of the non-linear device.
- This I_D -V_{DS} relationship will be determined by the circuit the non-linear device is connected to.
- Find the output voltage at I_D=0
- Find the output current at V_{DS}=0
- Identify these two points in the I_D -V_{DS} plane
- Sketch a line connecting these two points in the I_D -V_{DS} plane

In-class problem 2

Sketch the load line and calculate the Q point for the circuit below

$V_{TN} = 0.8$ V $K_n = 0.5$ mA/V^2



Region	NMOS
Nonsaturation	$v_{DS} < v_{DS}(sat)$ $i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$
Saturation	$v_{DS} > v_{DS}(sat)$ $i_D = K_n[v_{GS} - V_{TN}]^2$
Transition Pt.	$v_{DS}(sat) = v_{GS} - V_{TN}$
Enhancement Mode	$V_{TN} > 0V$
Depletion Mode	$V_{TN} < 0V$

Problem-Solving Technique I

Given V_{DS}, V_{GS}, and V_{TN}

1. Determine the operating region of the transistor
   a. $V_{GS} > V_{TN}$, $I_D > 0$, & $V_{DS} \geq V_{DS}(sat)$
2. Analyze circuit using the appropriate I_D -V_{DS} relations of the transistor given its operating region.

Problem-Solving Technique II

One or more unknowns among I_D,V_{DS} and V_{GS}

1. Assume the transistor is in saturation.
   a. $V_{GS} > V_{TN}$, $I_D > 0$, & $V_{DS} \geq V_{DS}(sat)$
2. Analyze circuit using saturation I-V relations.
3. Evaluate resulting bias condition of transistor.
   a. If $V_{GS} < V_{TN}$, transistor is likely in cutoff
   b. If $V_{DS} < V_{DS}(sat)$, transistor is likely in non-saturation region
4. If initial assumption is proven incorrect, make new assumption and repeat Steps 2 and 3.

Overview of Lecture 3

- DC analysis of transistor behavior and elements of bias design for amplifiers (Neamen 3.2-S&S 5.3).
- Examples of biasing circuits 1

(Neamen 3.2,3.4, S&S 5.3, 5.4, 5.7)