ECE 322L
Electronics 2

02/20/20- Lecture 9

Amplifiers with active loads

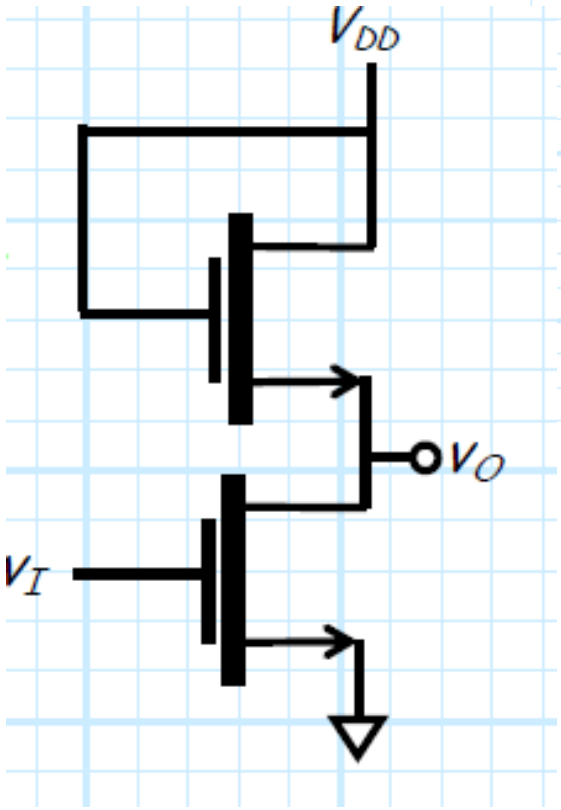
Multi-stage amplifiers

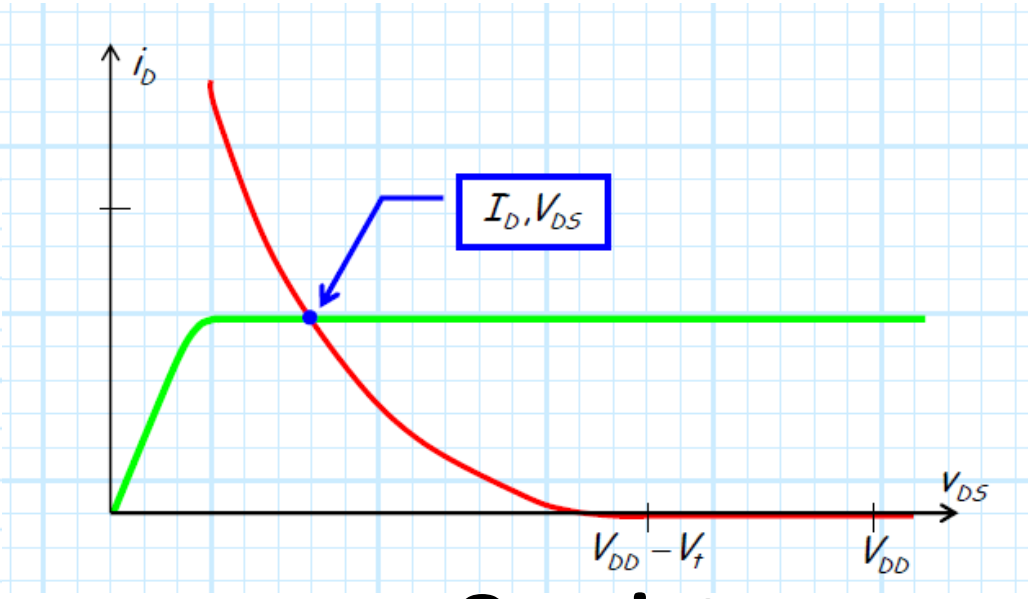
Updates and overview

- Homework 4 is online
- Lab 5: practice lab for your design-project
- Single-stage IC MOSFET amplifiers-Amplifiers with active loads (Neamen 4.7.4)

  Multi-stage MOSFET amplifiers (Neamen 4.8.1).

NMOS amplifier with enhancement load





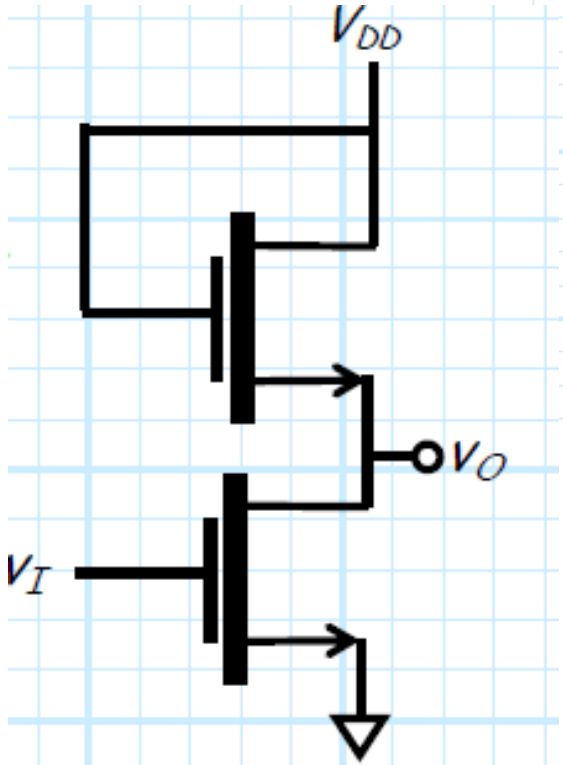
Q-point

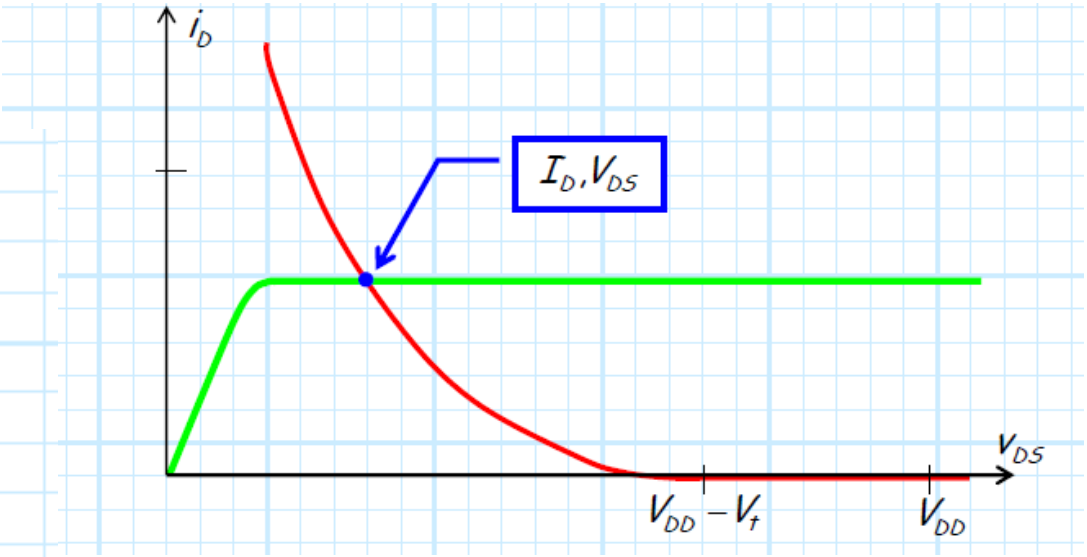
$$A_v = \frac{-g_{m1}}{g_{m2}} = \frac{2\sqrt{K_1}\sqrt{I_D}}{2\sqrt{K_2}\sqrt{I_D}} = \sqrt{\frac{K_1}{K_2}} = \frac{\sqrt{\left(W/L\right)_1}}{\sqrt{\left(W/L\right)_2}}$$

Gain

Possible issues with this configuration??

NMOS amplifier with enhancement load





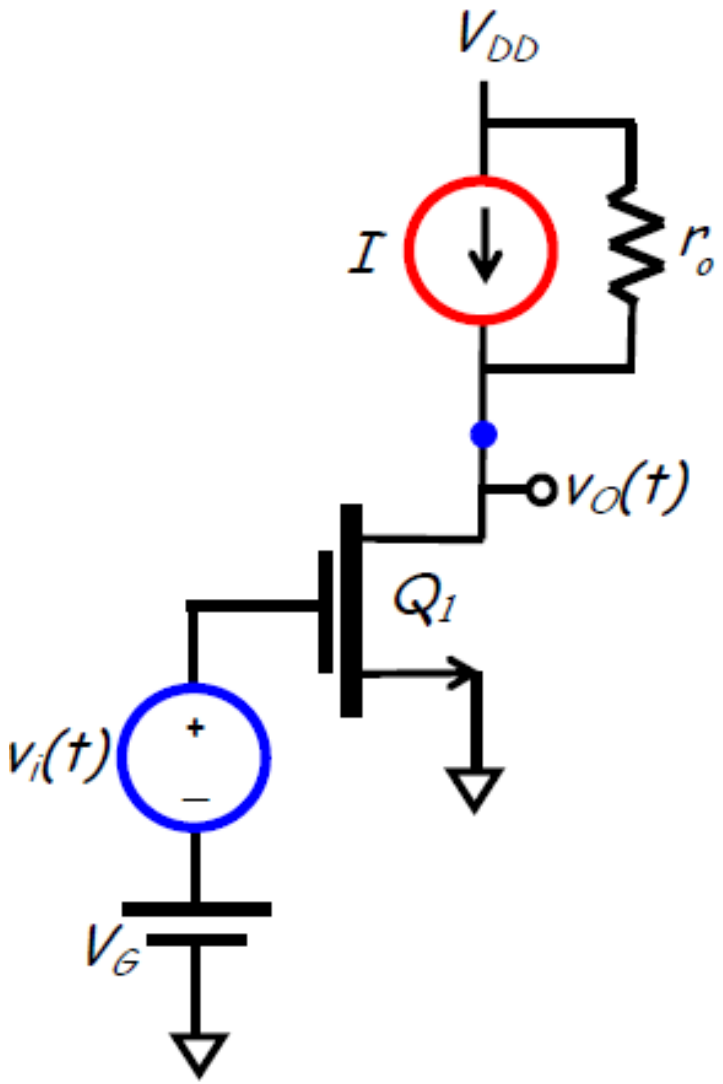
Q-point

$$A_v = \frac{-g_{m1}}{g_{m2}} = \frac{2\sqrt{K_1}\sqrt{I_D}}{2\sqrt{K_2}\sqrt{I_D}} = \sqrt{\frac{K_1}{K_2}} = \frac{\sqrt{\left(W/L\right)_1}}{\sqrt{\left(W/L\right)_2}}$$

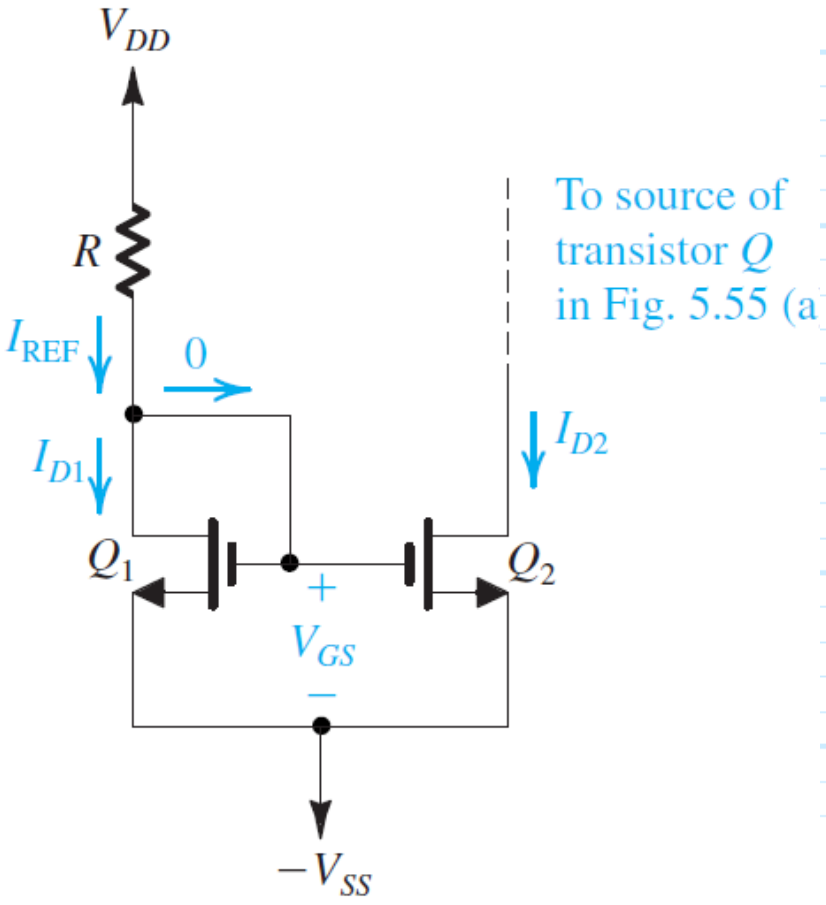
Gain

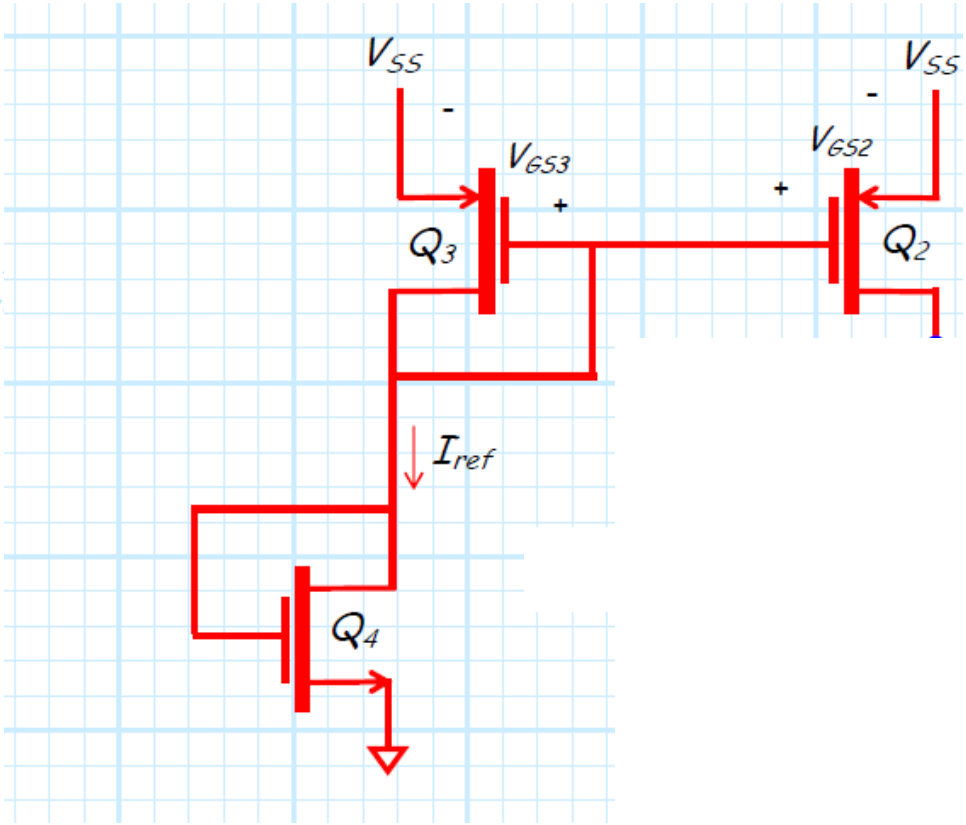
- **Q-point is not stable against temperature and variation of transistor parameters**
- **Gain is limited as it is not practical to make transistors very different in size on the same chip**

NMOS amplifier using a real current source as load

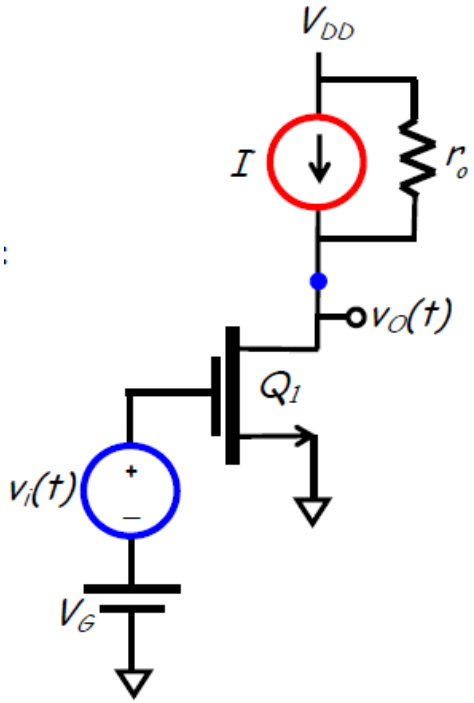


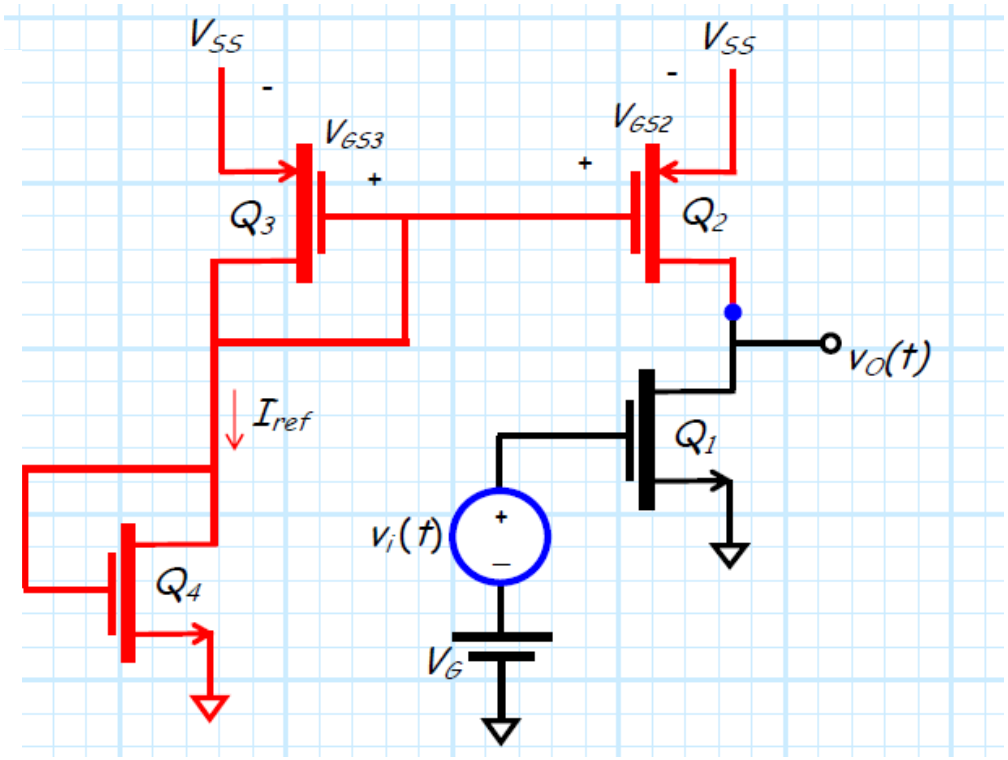
Current source: IC Implementation





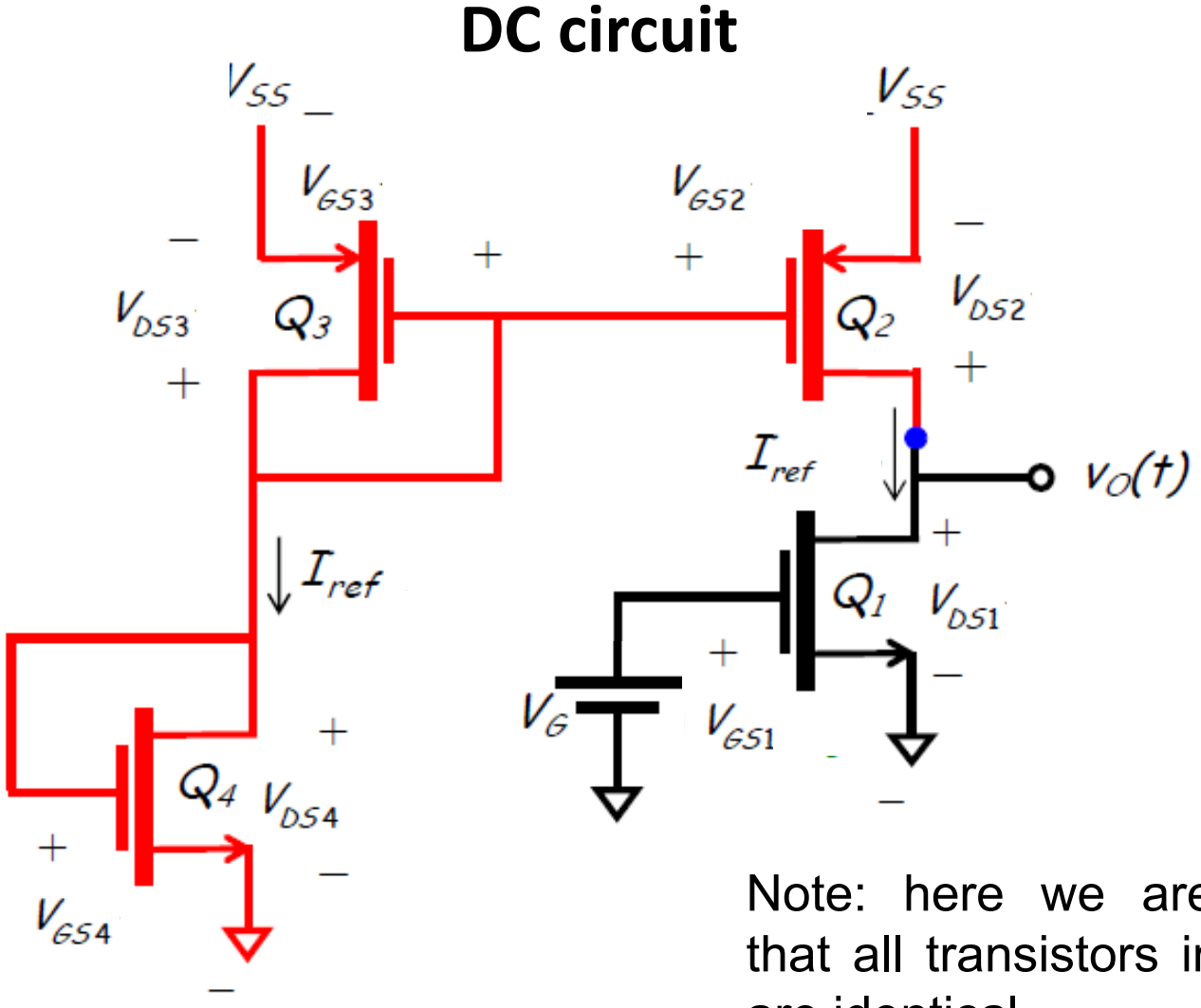
CMOS amplifier using a current source as load





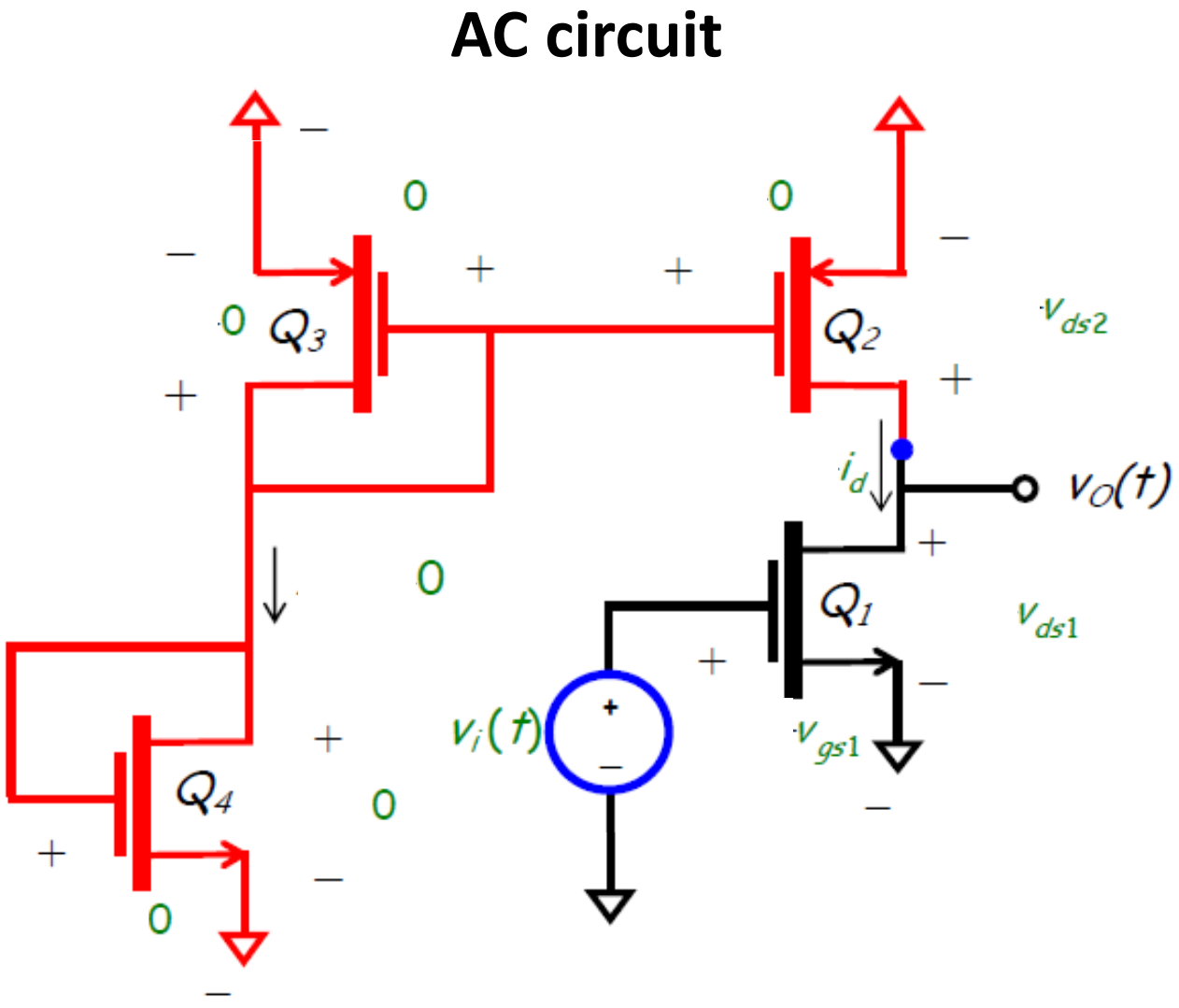
- **In ICs the current source is implemented by a current mirror**
- **r_o is then the output resistance of the current mirror as seen by Q_1**

CMOS amplifier using a current source as load

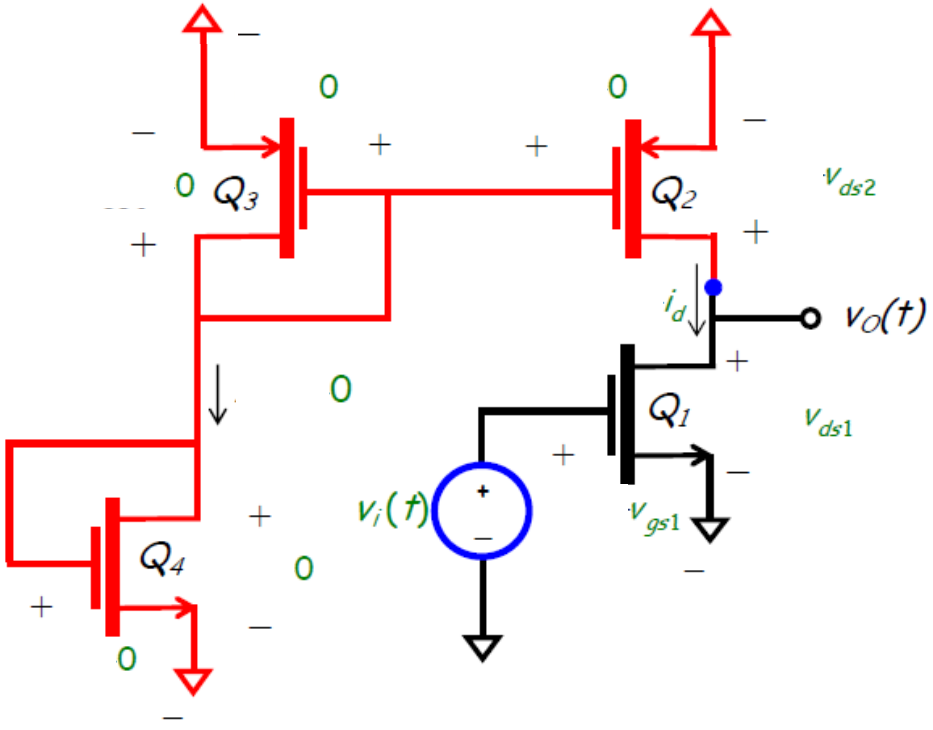


Note: here we are assuming that all transistors in the circuit are identical.

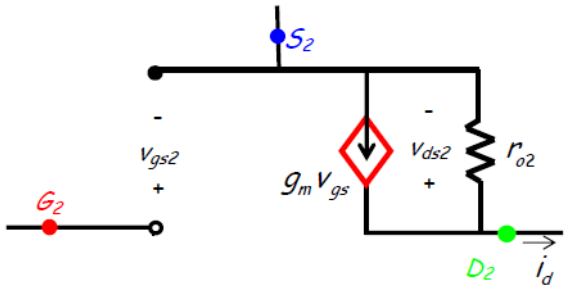
CMOS amplifier using a current source as load



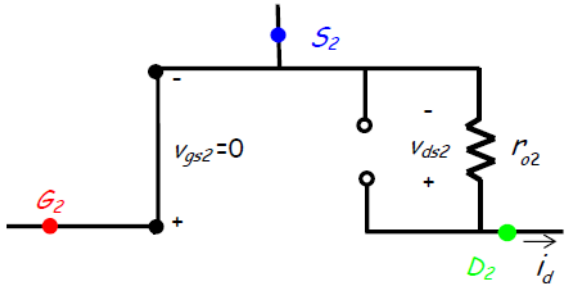
Small-signal Model of the Current Mirror



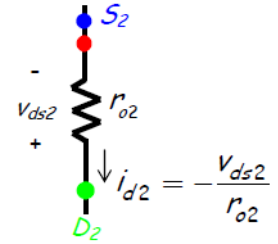
Equivalently, the **small-signal PMOS model** is:



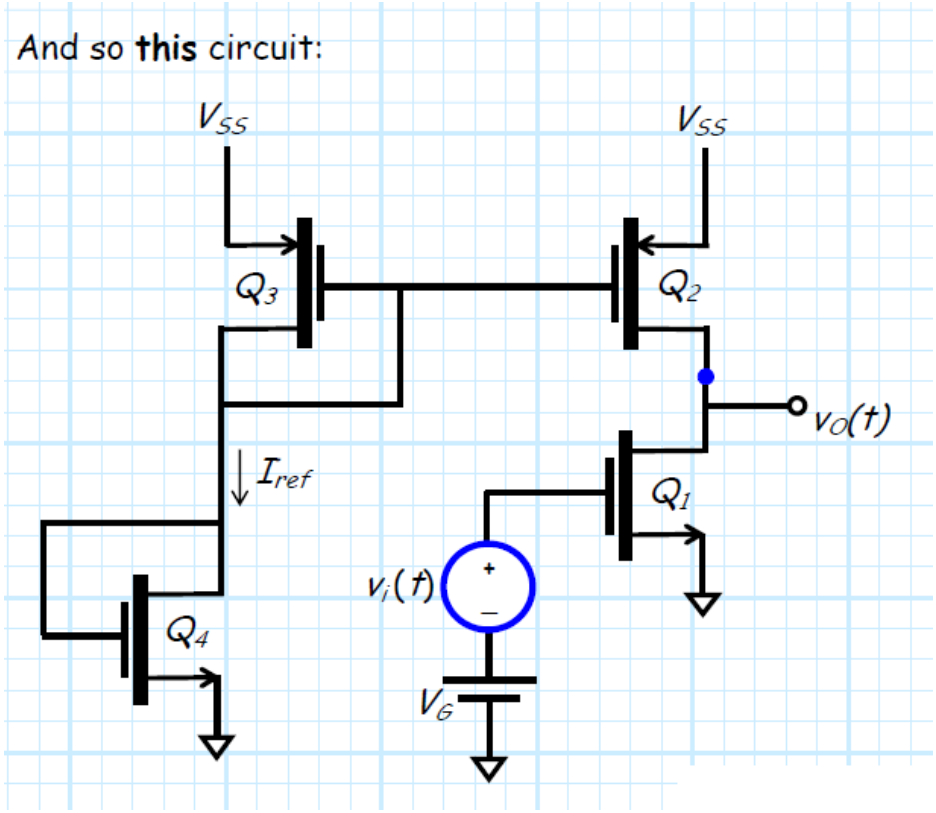
Thus for $v_{gs2}=0$, the small-signal model becomes:

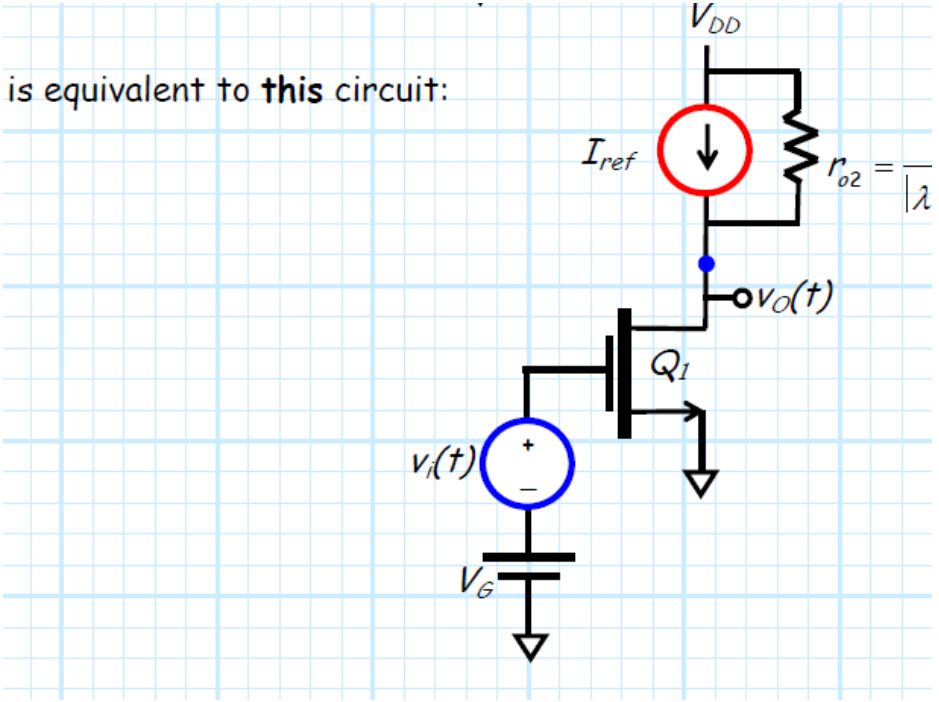


Or, simplifying further:

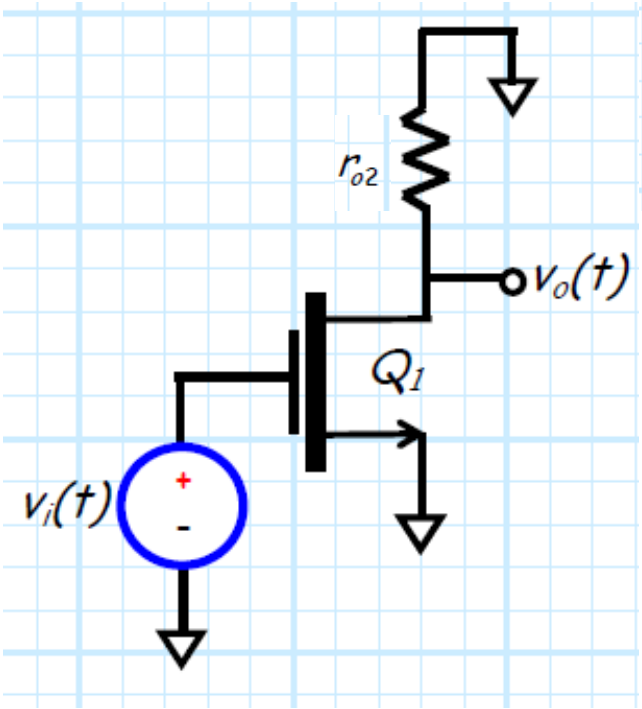


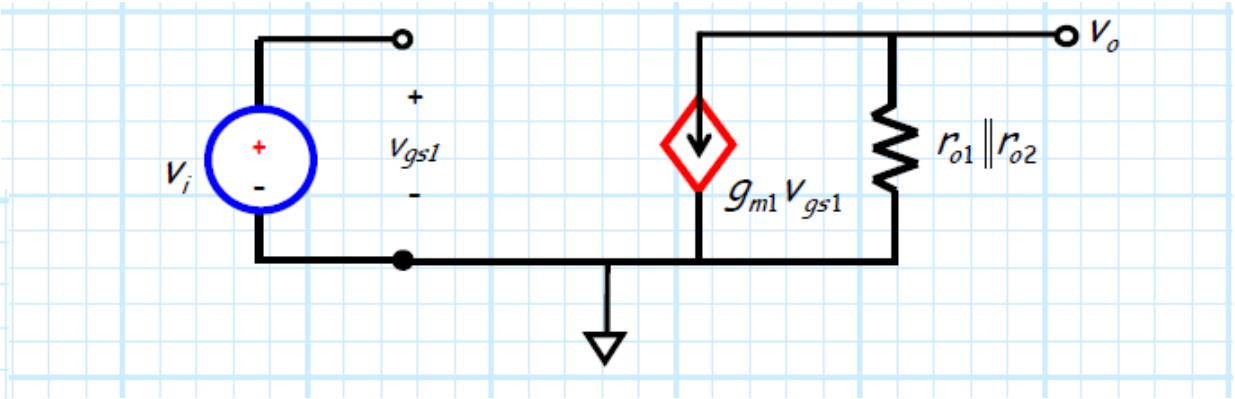
CMOS amplifier using a current source as load





CMOS amplifier using a current source as load





$$R_i = \infty \qquad R_o = r_{o1} \| r_{o2}$$

$$A_{vo} = -g_{m1}\left(r_{o1} \| r_{o2}\right)$$

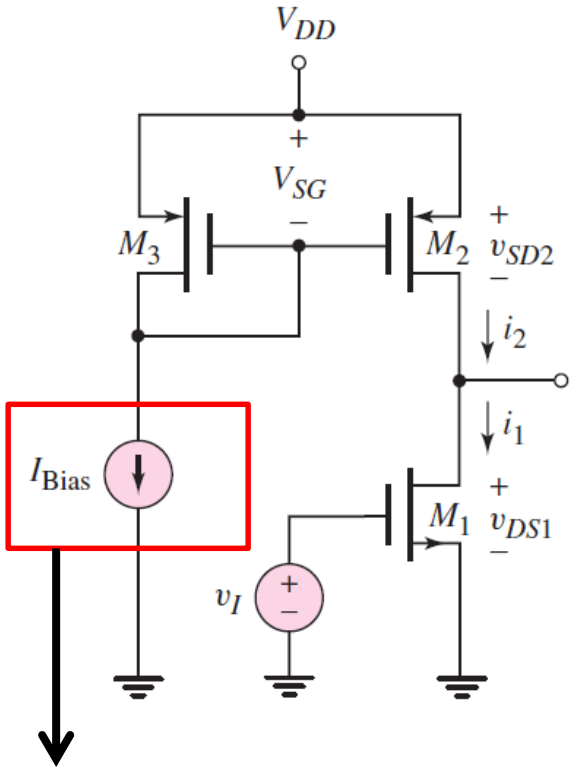
Note **this** result is **far different** (i.e., larger) than the result when using the **enhancement load** for R_D:

$$A_{vo} = -\sqrt{\frac{K_1}{K_2}}$$

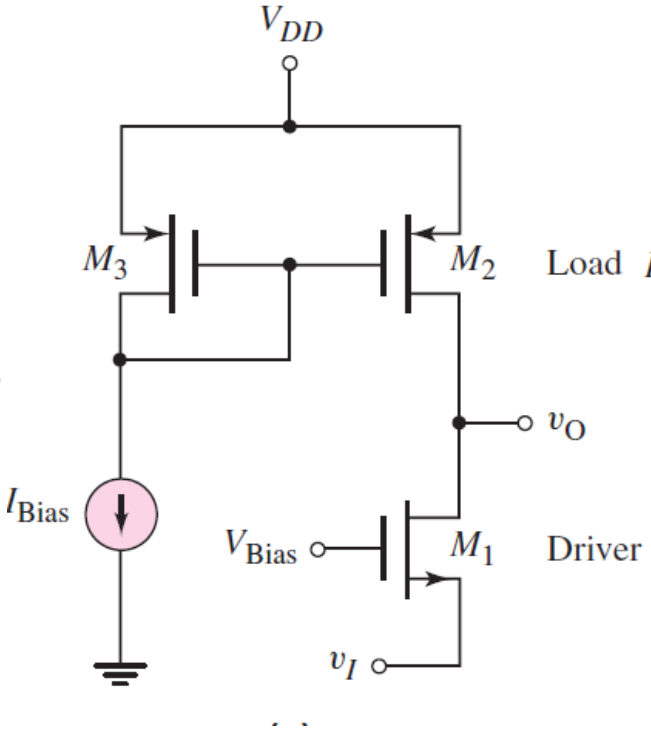
However, we find that the **output** and **input** resistances of this amplifier are the **same** as with the enhancement load:

MOS Amplifiers Using a current source as load

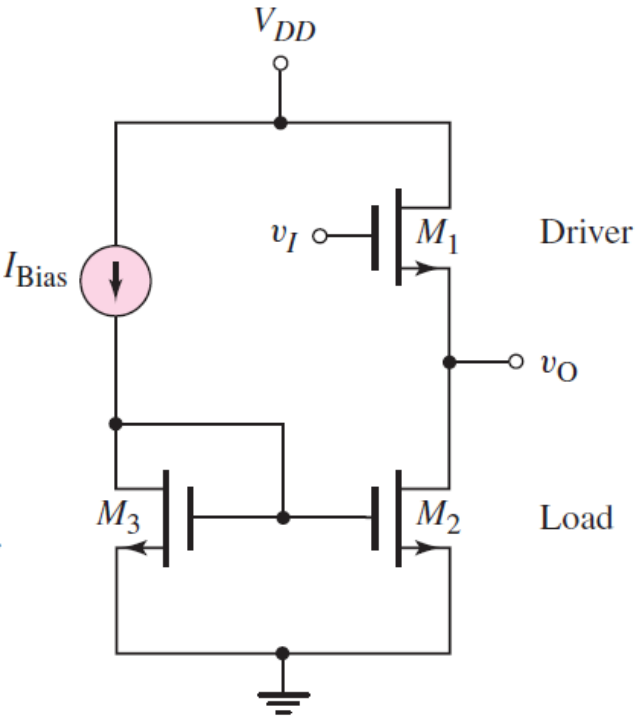
Common source



Common gate



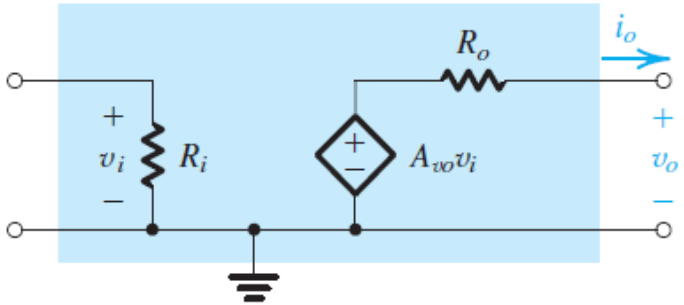
Common drain



It can be any FET based network which fixes a current

Multi-stage amplifiers

Why do we need them?

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \left.\frac{v_o}{v_i}\right\|_{i_o=0}$ (V/V)	$R_i = \infty$ $R_o = 0$

Common Source

- Large $A_v < 0$
- Infinite R_{in}
- Moderate R_o

Common Gate

- Large $A_v > 0$
- Small R_{in}
- Moderate R_o

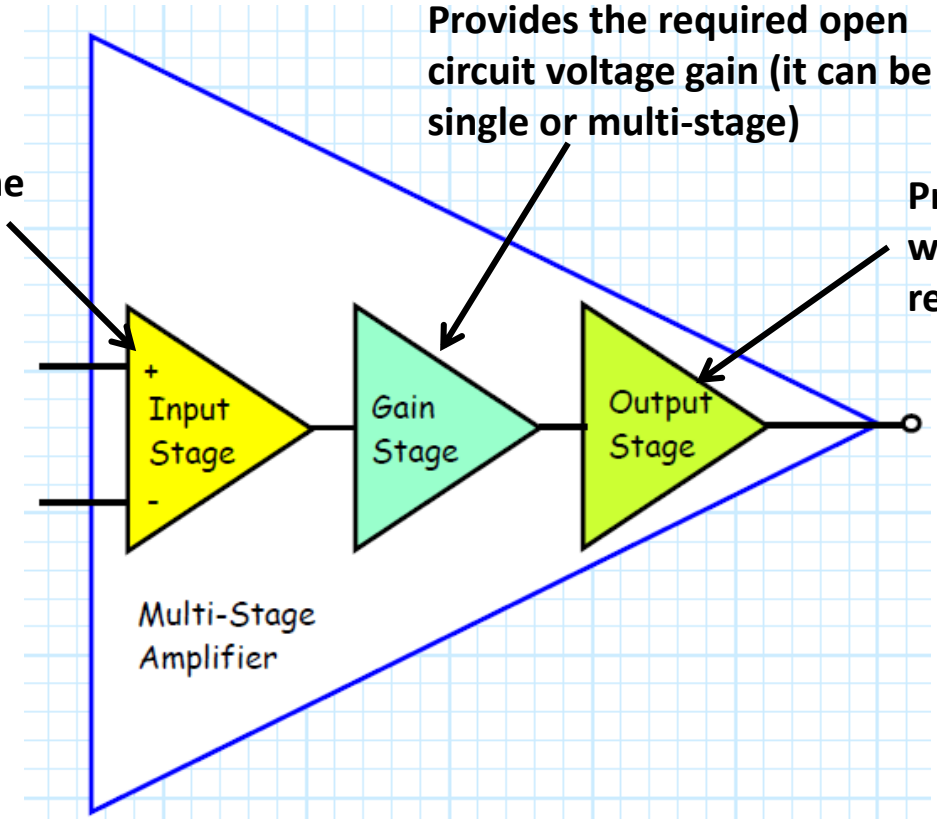
Source Follower

- $0 < A_v \leq 1$
- Infinite R_{in}
- Small R_o

All the amplifiers that we know of have at least one attractive feature but also at least one sub-optimal feature

Multi-stage amplifiers

Multi-stage amplifiers combine basic designs in such a way that they take advantage of the attractive characteristic and compensate for the sub-optimal features of each design.

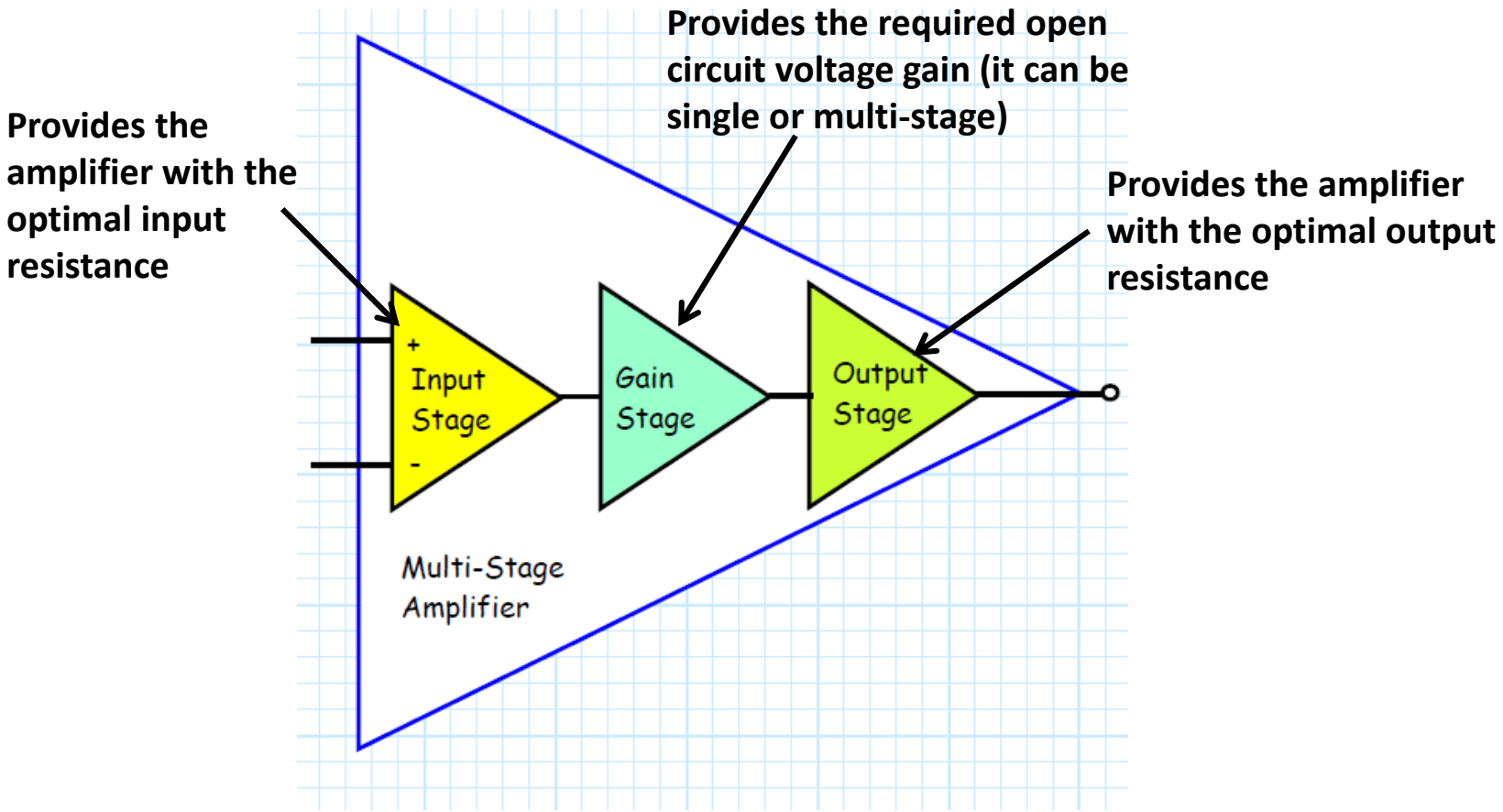


They typically consist of 3 sections

Basic designs:

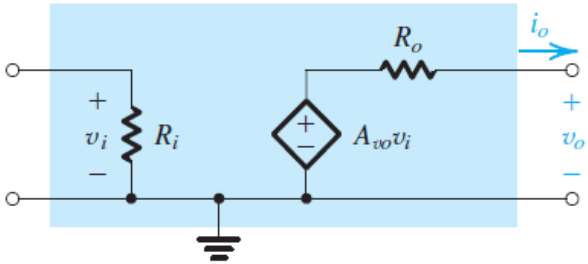
- **CS**
- **CG**
- **CD**

Multi-stage amplifiers



It is important to understand which basic configurations to select per each stage, and how placing two basic configurations in series affects their performance.

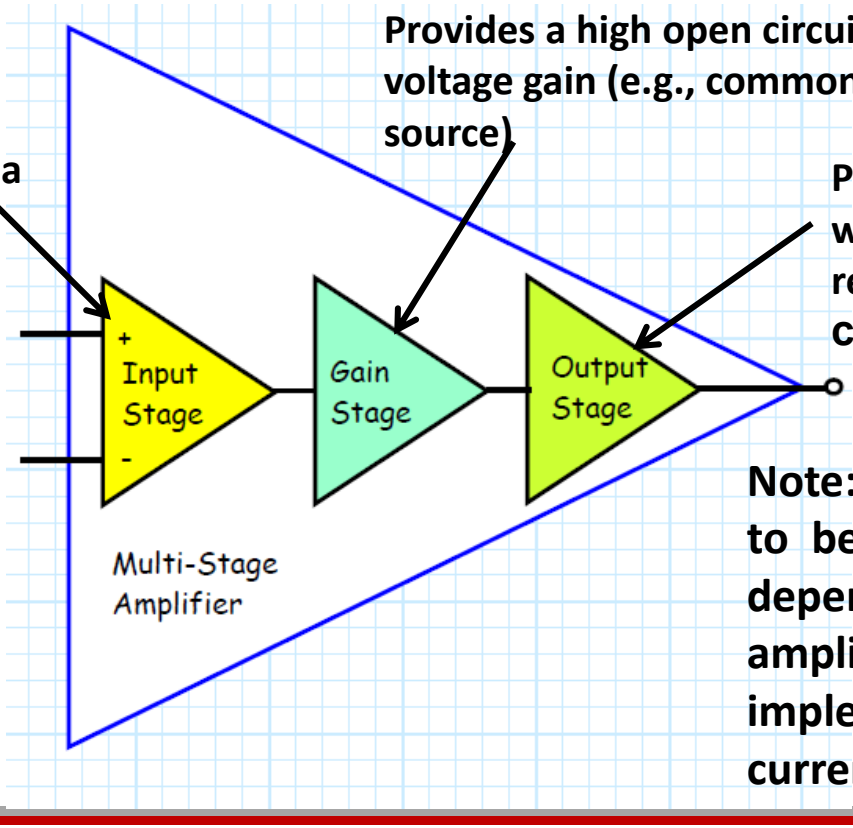
Multi-stage amplifiers

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \left.\frac{v_o}{v_i}\right\|_{i_o=0}$ (V/V)	$R_i = \infty$ $R_o = 0$

Provides the amplifier with a high input resistance (e.g., common source)

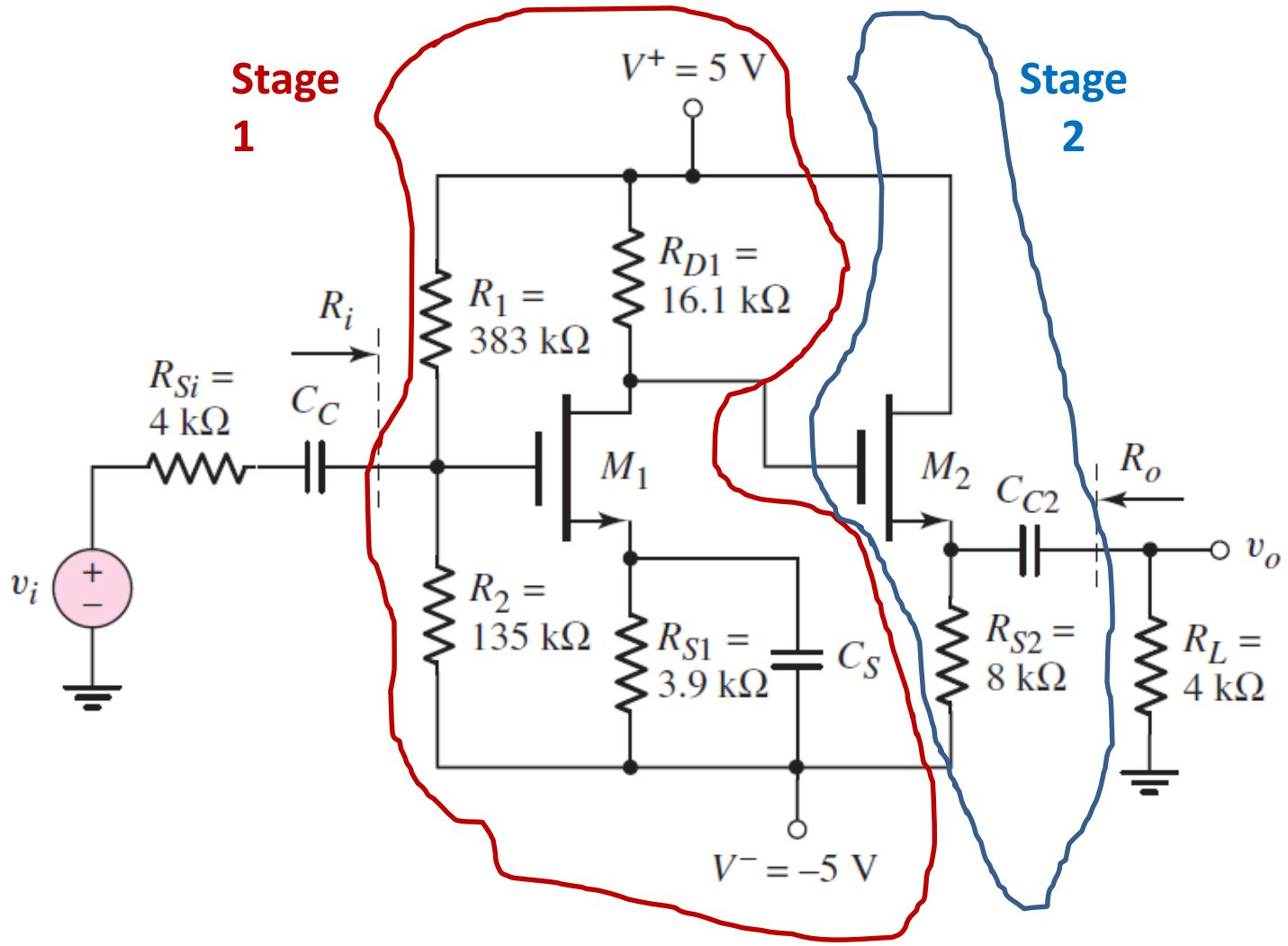
Provides a high open circuit voltage gain (e.g., common source)

Provides the amplifier with a low output resistance (e.g., common drain)



Note: The basic configuration to be selected per each stage depends on the type of amplifier one wants to implement, e.g., a voltage or a current amplifier.

Cascade amplifier



In-class problem

4.68 The transistor parameters in the circuit in Figure P4.68 are $V_{TN1} = 0.6$ V, $V_{TP2} = -0.6$ V, $K_{n1} = 0.2$ mA/V^2, $K_{p2} = 1.0$ mA/V^2, and $\lambda_1 = \lambda_2 = 0$. The circuit parameters are $V_{DD} = 5$ V and $R_{\text{in}} = 400$ kΩ. (a) Design the circuit such that $I_{DQ1} = 0.2$ mA, $I_{DQ2} = 0.5$ mA, $V_{DSQ1} = 2$ V, and $V_{SDQ2} = 3$ V. The voltage across R_{S1} is to be 0.6 V. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$.

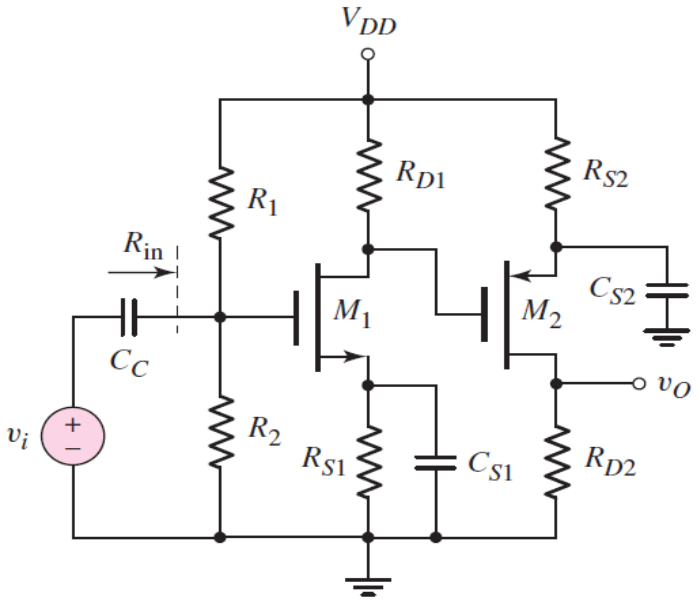


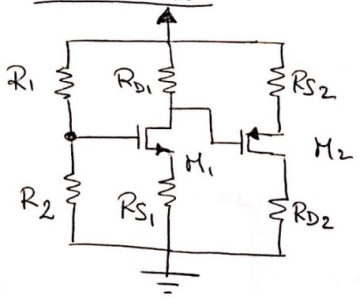
Figure P4.68

In addition determine the input and output resistance.

At home compare the characteristics of the two stages as isolated with the characteristics of the cascade amplifier

In-class problem, solution

DC circuit



$R_{S1} = \frac{V_{S1}}{I_{D1}} = \frac{0.6}{0.2m} = 3K\Omega$ $R_{D1} = \frac{V_{DD} - V_{D1}}{I_{D1}}$ $V_{D1} = V_{DS} + V_{S1} = 2 + 0.6 = 2.6\,V$

$R_{D1} = \frac{5 - 2.6}{0.2m} = 12K\Omega$

Assuming M_1 in saturation: $I_{D1} = K_n (V_{GS1} - V_{TN})^2 \Rightarrow 0.2m = 0.2m (V_{GS1} - 0.6)^2$

$V_{GS1} = 1.6\,V$

$V_{G1} = V_{GS1} + V_{S1} = 1.6 + 0.6 = 2.2\,V$ $V_{G1} = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{R_1 // R_2}{R_1} \cdot V_{DD}$

$R_i = R_1 // R_2 = 400K\Omega \Rightarrow \frac{400K \cdot 5}{R_1} = 2.2V \Rightarrow R_1 = 909K\Omega$

$\frac{909K \cdot R_2}{R_2 + 909K} = 400K\Omega \Rightarrow R_2 = 714K\Omega$

$V_{DS1} > V_{GS1} - V_{TN}$ (Saturation assumption is verified)

Assuming M_2 in saturation: $I_{D2} = K_p (V_{SG} + V_{TP})^2 \Rightarrow 0.5m = 1m (V_{SG2} - 0.6)^2$

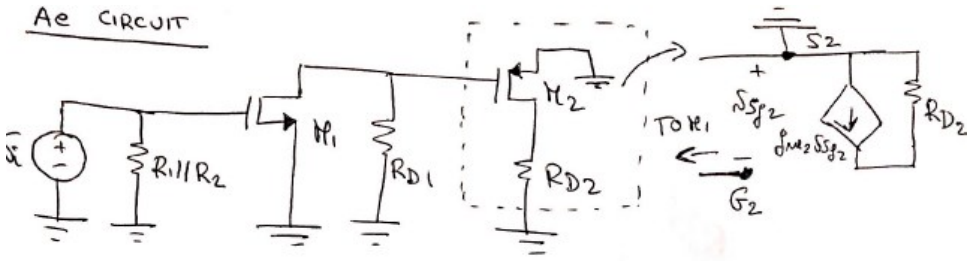
$V_{SG2} = 1.307\,V$ $V_{S2} = V_{D1} + V_{SG2} = 2.6 + 1.307 = 3.907\,V$

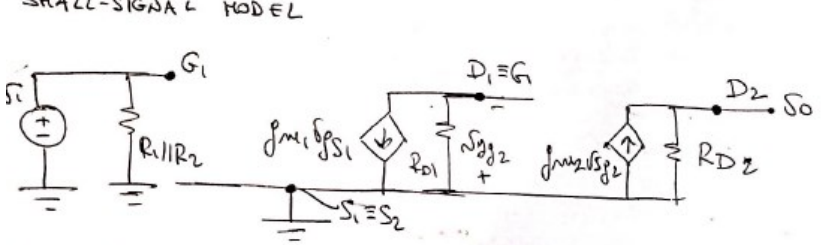
$R_{S2} = \frac{V_{DD} - V_{S2}}{I_{D2}} = \frac{5 - 3.907}{0.5m} = 2.2K\Omega$

$R_{D2} = \frac{V_{D2}}{I_{D2}}$ $V_{D2} = V_{S2} - V_{SD2} = 3.907 - 3 = 0.907\,V$ $R_{D2} = \frac{0.907}{0.5m} = 1.8K$

$V_{SD2} > V_{SG2} + V_{TP}$ (V_{SD2}=3 V; V_{SG2}=1.307 V; V_{TP}=-0.6)

In-class problem, solution





$R_i = R_1 // R_2 = 400\ k\Omega$

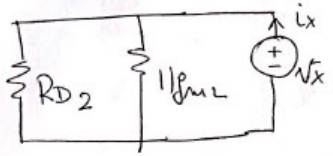
$A_V = \frac{v_o}{v_i}$ $\quad v_o = g_{m2} v_{sg2} R_{D2}$ $\quad v_{sg2} = g_{m1} v_{gs1} R_{D1}$

$v_{gs1} = v_i$ $\quad v_o = g_{m1} g_{m2} R_{D1} R_{D2}$

$g_{m1} = 2\sqrt{K_n I_{D1}} = 2 \cdot \sqrt{0.2m \cdot 0.2m} = 0.4\ mA/V$

$g_{m2} = 2\sqrt{K_p I_{D2}} = 2 \cdot \sqrt{1m \cdot 0.5m} = 1.414\ mA/V$

$A_V = (0.4m)(1.414m)(12K)(1.8K) = 12.3$



$R_o = \frac{v_x}{i_x} = \frac{1}{g_{m2}} // R_{D2} = 500\ \Omega$

Overview of lecture 10

- Cascode amplifiers (Neamen 4.8.2)
- The Bipolar Junction Transistor (BJT):

  Structure, Operating regions,DC analysis,

  Load lines (Neamen-From 5.1.1 to 5.1.5)