ECE 322L
Electronics 2

02/04/20 - Lecture 5

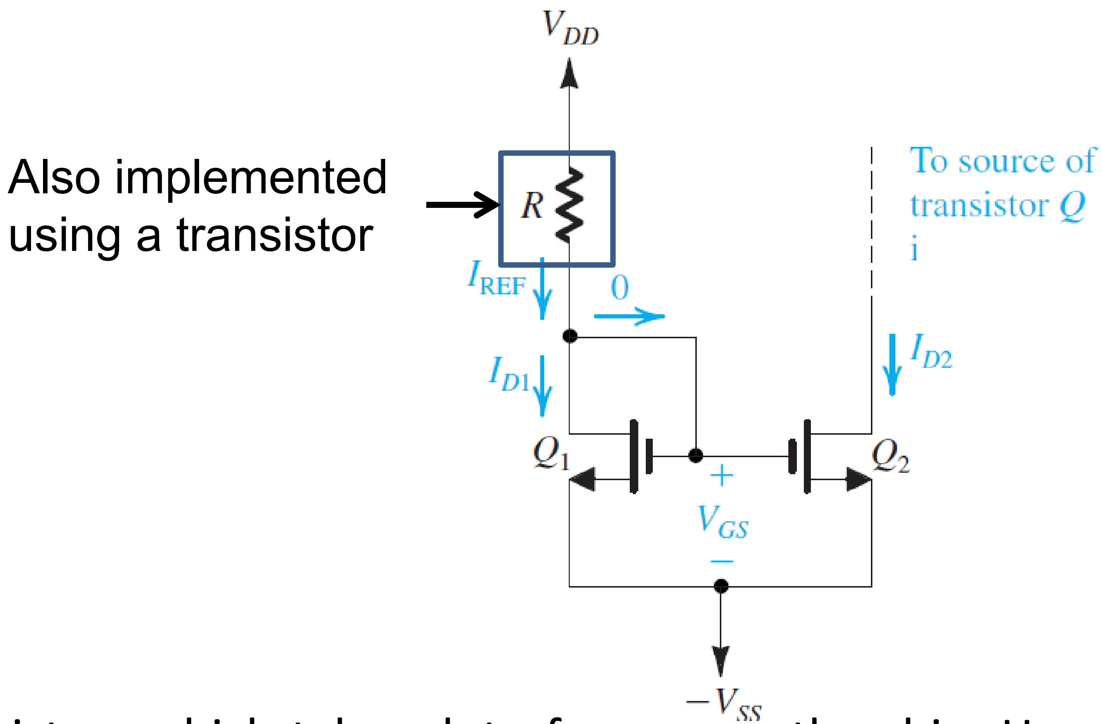
Total components and small signal analysis

Updates and Overview

- Lab reports may be submitted via e-mail to the TA after each lab. The TA will provide informal feedback on the lab reports upon request.
- Office hours 9-11 am on Wed (CHTM 110B). Please, double check UNM learn before heading to CHTM on Wed as last-minute changes of the office hours may occur.
- Lecture 5: IC current mirrors, FETs as amplifiers; total components and small signal analysis

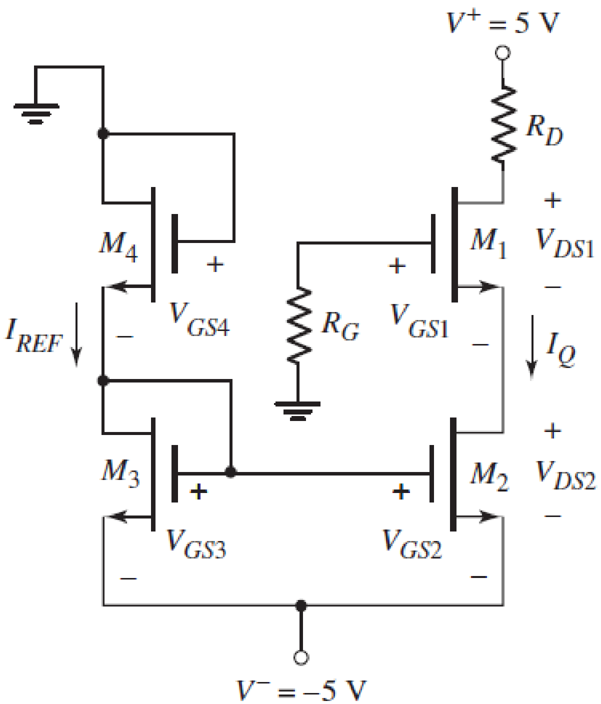
(Neamen 4.1.1, 4.1.2- S&S from 5.5.1 to 5.5.6).

Biasing by a Current Source (IC)



- Resistors which take a lot of space on the chip. Hence they need to be replaced with a different component.
- On a multistage amplifier IC chip, a constant dc current source is generated at one location and is then reproduced at different locations for biasing the various amplification stages. As a result the biasing of the multiple stages track each other in case of parameter changes, such as voltage supply or temperature fluctuations.

Biasing in IC



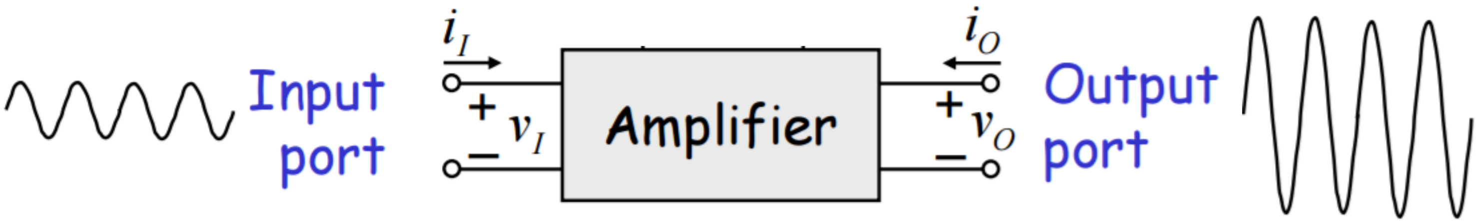
$$V_{GS3} = \frac{\sqrt{\frac{K_{n4}}{K_{n3}}}[(-V^-) - V_{TN4}] + V_{TN3}}{1 + \sqrt{\frac{K_{n4}}{K_{n3}}}}$$

$$I_Q = K_{n2}(V_{GS3} - V_{TN2})^2$$

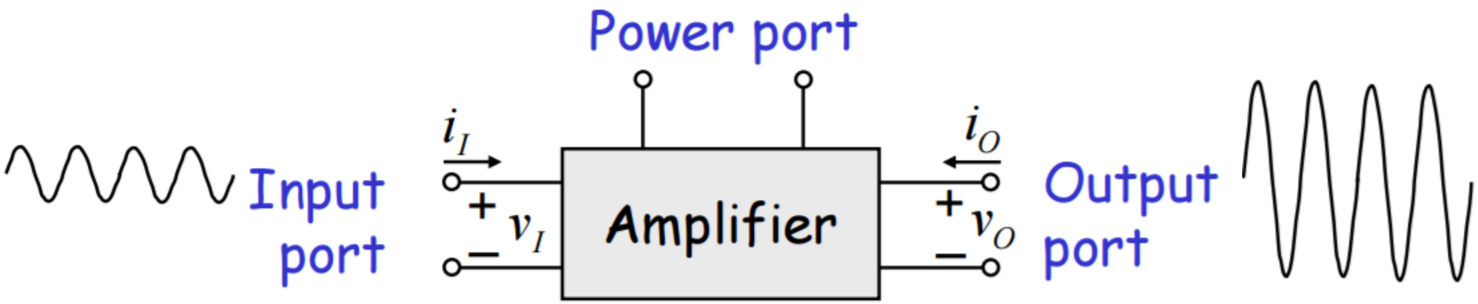
Figure 3.50 Implementation of a MOSFET constant-current source

Design parameters are the threshold voltages of M_3 and M_4 and the ratio K_{n4}/K_{n3}.

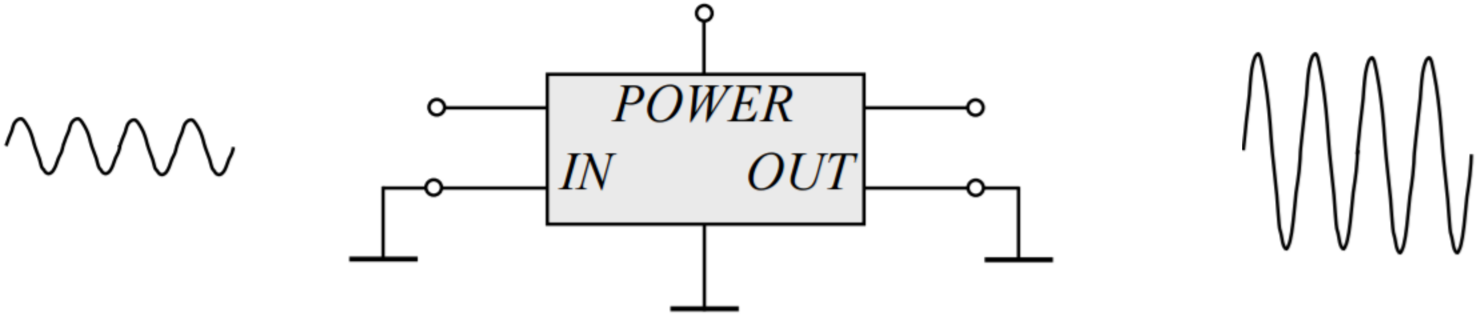
Amplifiers



Input port
i_I
v_I
Amplifier
i_O
v_O
Output port

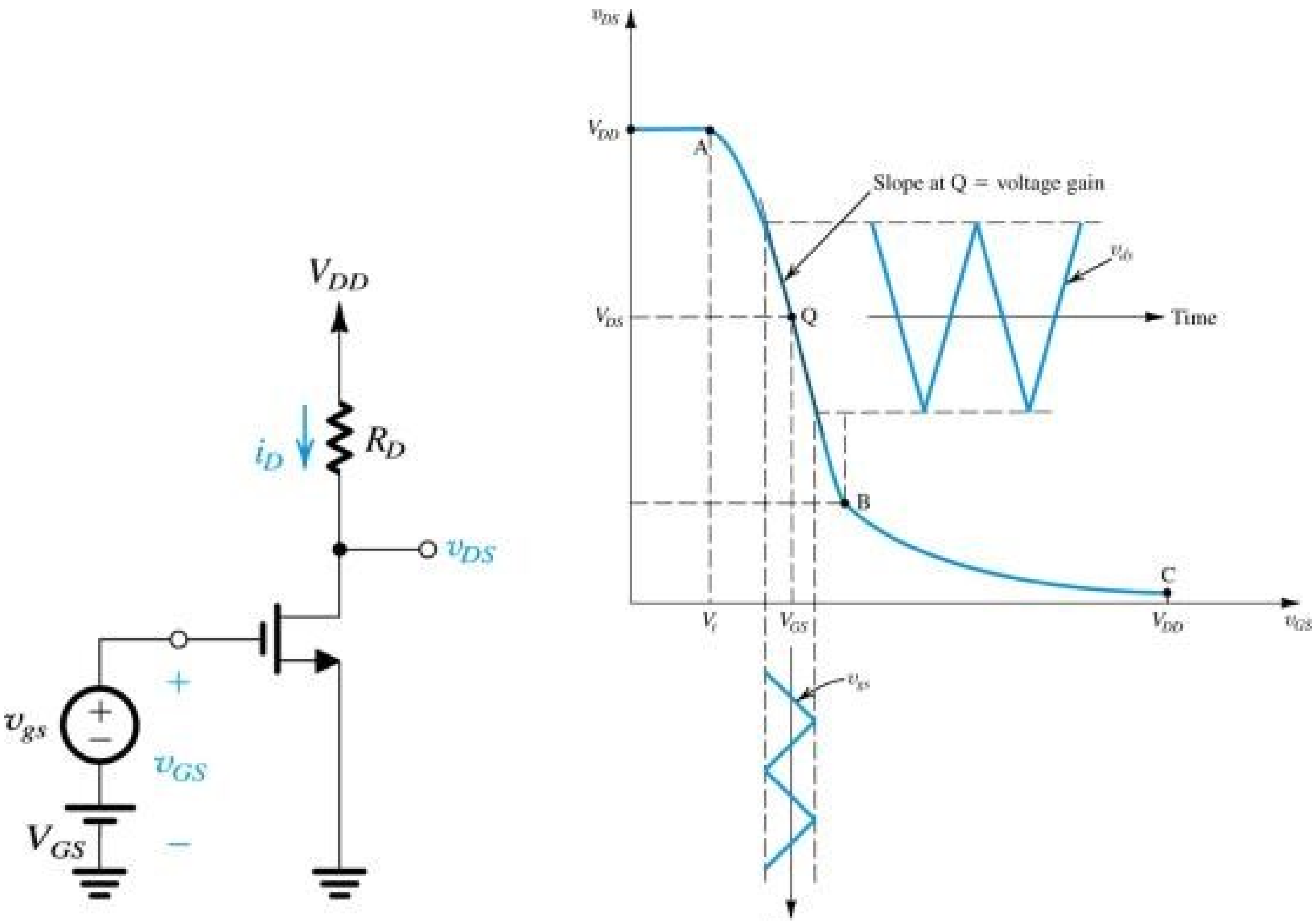


Power port
Input port
i_I
v_I
Amplifier
i_O
v_O
Output port



POWER
IN
OUT

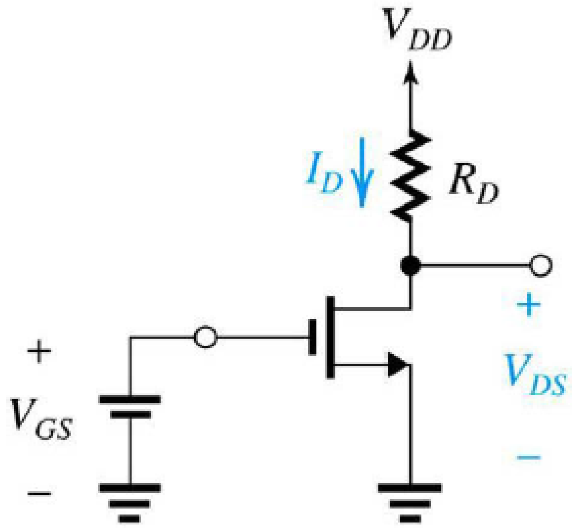
FET-based Amplifiers



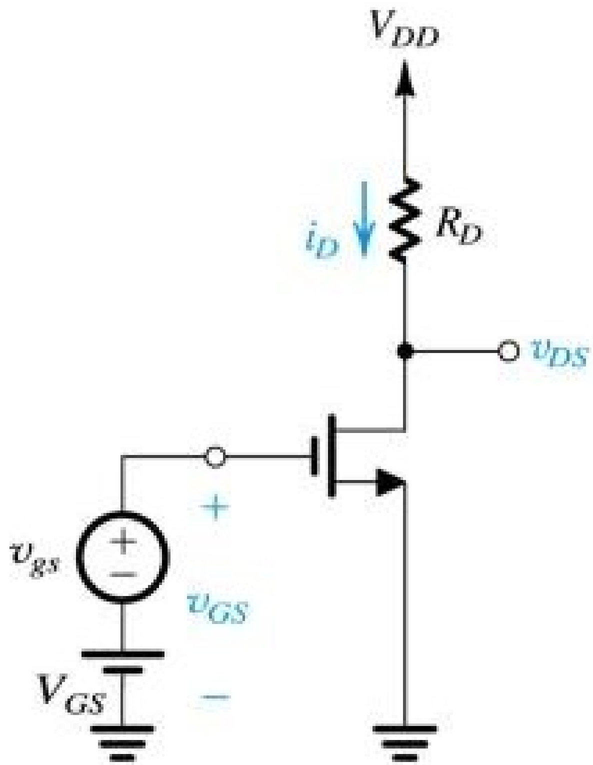
Notation:
V_A:DC signal
v_a:AC signal
v_A:DC+AC signal

1. Determine the Q point of the transistor (DC analysis)
2. Determine the response of the circuit to an input signal (DC&AC analysis)

FET-based Amplifiers-Analysis



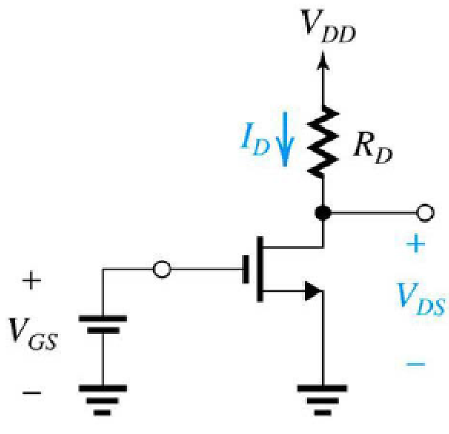
DC circuit



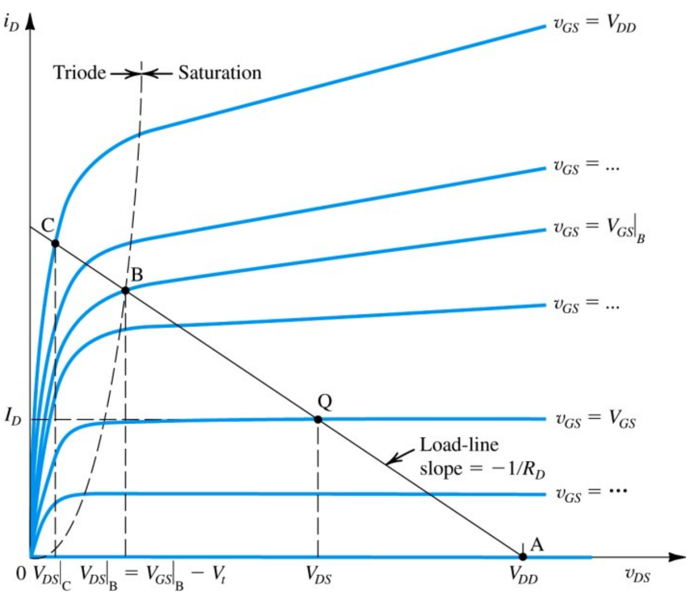
Total components circuit

1. Determine the Q point of the transistor (DC analysis)
2. Determine the response of the circuit to an input signal (DC&AC analysis)

DC Analysis



Bias



$$\begin{cases} I_D = \frac{1}{2} \frac{\varepsilon_{ox}}{t_{ox}} \mu_n \frac{W}{L} (V_{GS} - V_T)^2 \\ V_{DS} = V_{DD} - R_D I_D \end{cases}$$

To ensure saturation:

$$\begin{cases} V_{GS} > V_T \\ V_{DS} > V_{GS} - V_T \end{cases}$$

From the equations above we can find the coordinates of the Q point, namely I_{DQ}, V_{DSQ}, and V_{GSQ}

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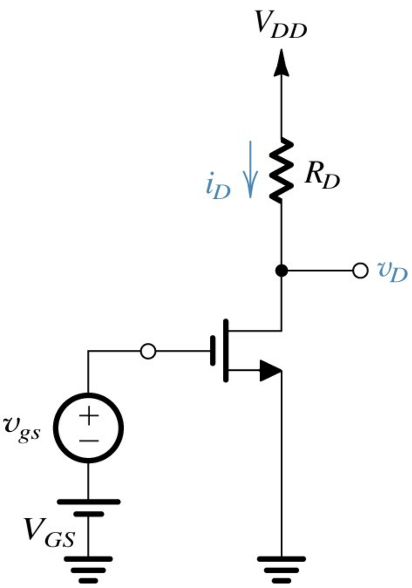
Total Components Analysis (1)



Bias (DC) +signal (AC) analysis

$$v_{GS} = V_{GS} + v_{gs}$$

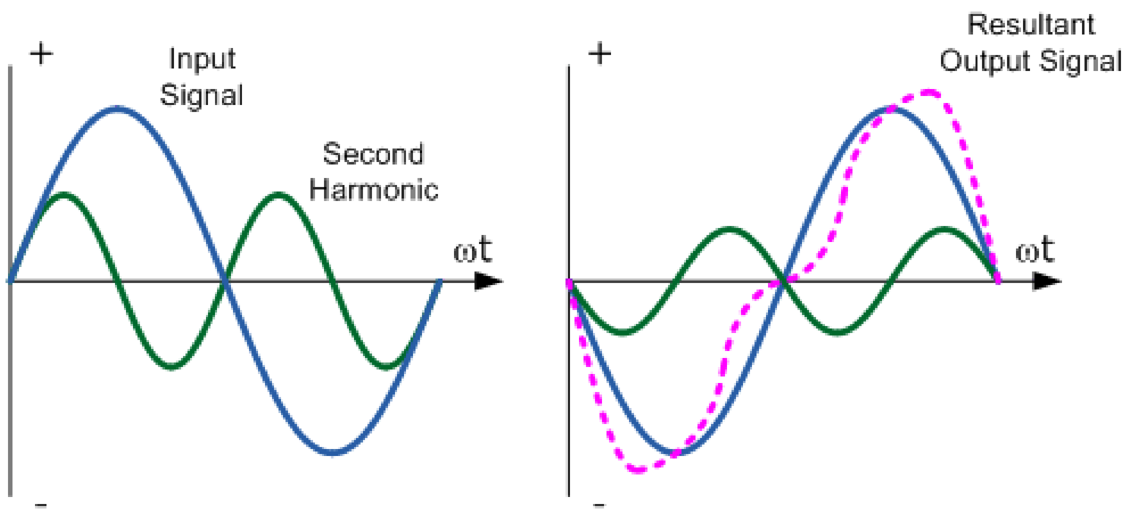
$$i_D = \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}\left(V_{GS} + v_{gs} - V_T\right)^2 =$$

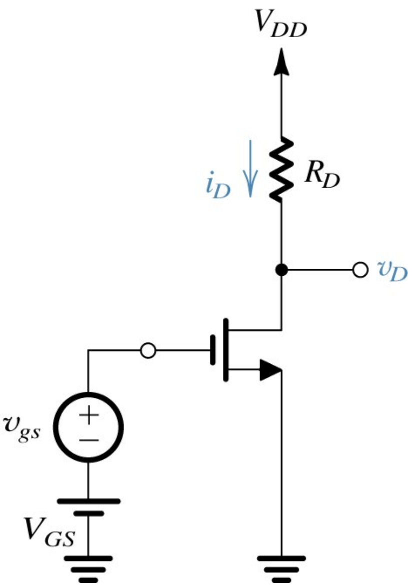
$$= \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}\left(V_{GS} - V_T\right)^2 + \quad \leftarrow \text{DC BIAS CURRENT}$$

$$+ \frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}\left(V_{GS} - V_T\right)v_{gs} + \quad \leftarrow \text{CURRENT COMPONENT DIRECTLY PROPORTIONAL TO THE INPUT SIGNAL } v_{gs}$$

$$+ \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}v_{gs}^2 \quad \leftarrow \text{NON LINEAR DISTORSION}$$

Distortion in Large Signals





$$v_{GS} = V_{GS} + v_{gs}$$

$$i_D = \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n \frac{W}{L}\left(V_{GS} + v_{gs} - V_T\right)^2 =$$

$$= \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n \frac{W}{L}\left(V_{GS} - V_T\right)^2 + \quad \leftarrow$$ DC BIAS CURRENT

$$+ \frac{\varepsilon_{ox}}{t_{ox}}\mu_n \frac{W}{L}\left(V_{GS} - V_T\right) v_{gs} + \quad \leftarrow$$ CURRENT COMPONENT DIRECTLY PROPORTIONAL TO THE INPUT SIGNAL v_{gs}

$$+ \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n \frac{W}{L} v_{gs}^2 \leftarrow$$ NON LINEAR DISTORSION

Small Signal Approximation

If the input signal is kept small so that:

$$\frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}v_{gs}^2 \ll \frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}(V_{GS}-V_T)v_{gs}$$

$$\updownarrow$$

$$v_{gs} \ll 2(V_{GS}-V_T) \leftarrow \boxed{\text{"SMALL SIGNAL CONDITION"}}$$

we can neglect the last term and express:

$$i_D \simeq I_D + i_d$$

$$I_D = \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}(V_{GS}-V_T)^2$$

$$i_d = \underbrace{\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}(V_{GS}-V_T)}_{=\,g_m}v_{gs}$$

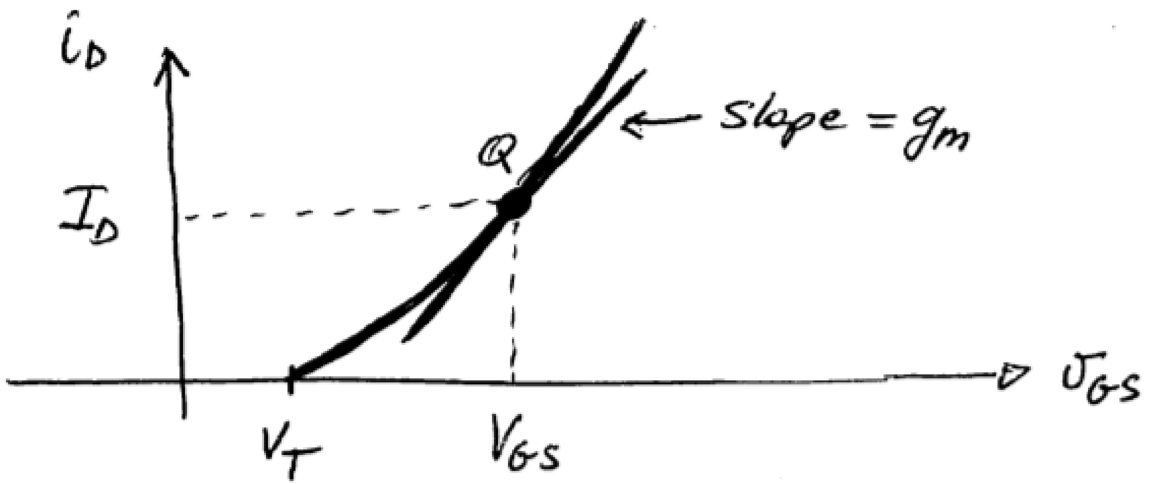
Small Signal Analysis

$$g_m = \frac{i_d}{v_{gs}} = \frac{\varepsilon_{ox}}{t_{ox}} \mu_n \frac{W}{L} \left(V_{GS} - V_T \right)$$

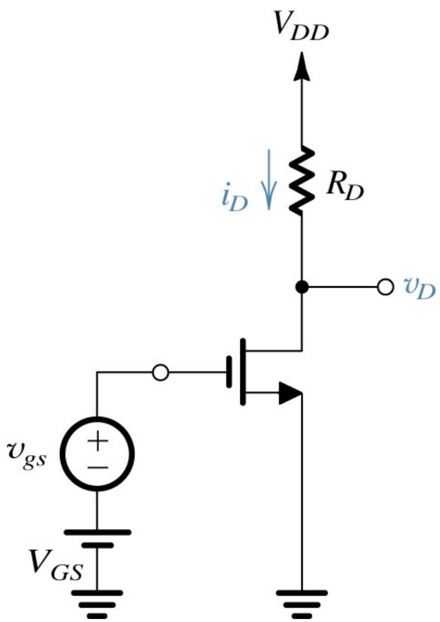
$$g_m = 2\sqrt{K_n I_{DQ}}$$

MOSFET TRANSCONDUCTANCE

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS} = V_{GS}}$$



Small Signal Analysis



$$v_{DS} = V_{DD} - R_D\, i_D \rightarrow$$

$$v_{DS} \simeq V_{DD} - R_D\,(I_D + i_d) \rightarrow$$

SMALL SIGNAL CONDITION

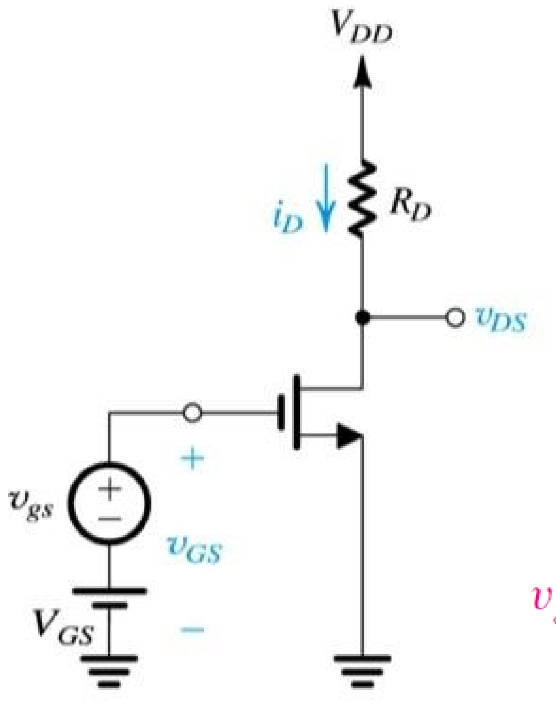
$$v_{DS} = \underbrace{V_{DD} - R_D \cdot I_D}_{V_{DS}} - R_D \cdot i_d \rightarrow$$

$$\underbrace{v_{DS} - V_{DS}}_{v_{ds}} = - R_D \cdot i_d \rightarrow$$

$$v_{ds} = - R_D \cdot i_d = - R_D \cdot g_m\, v_{gs}$$

$$\frac{v_{ds}}{v_{gs}} = - g_m R_D \leftarrow \boxed{\text{VOLTAGE GAIN}}$$

Strategy for Small Signals



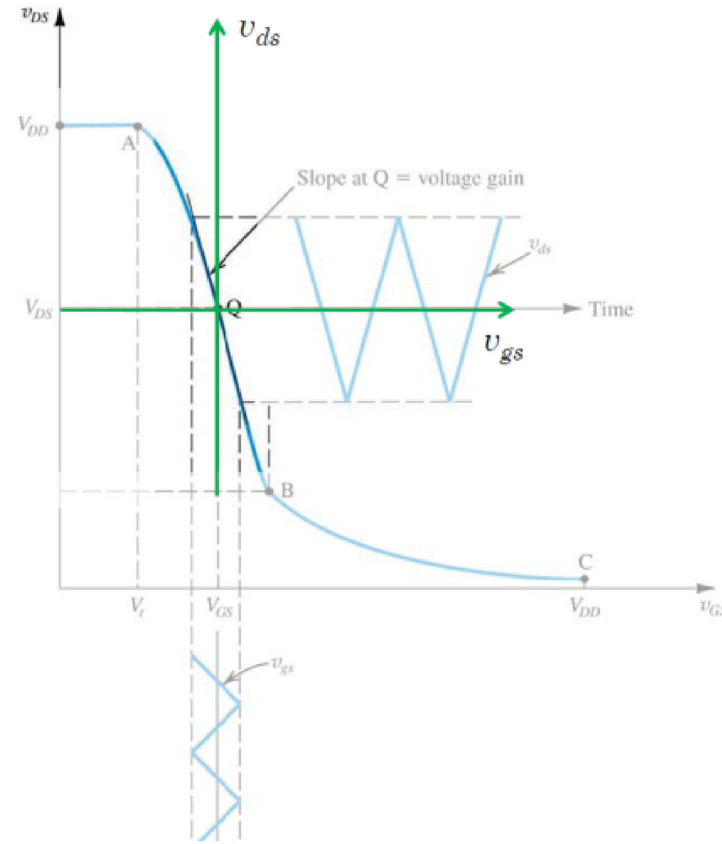
(a)

Signal and response

$$v_{GS} = \boxed{V_{GS}} + \boxed{v_{gs}}$$
$$v_{DS} = \boxed{V_{DS}} + \boxed{v_{ds}}$$
$$i_D = \boxed{I_{DS}} + \boxed{i_d}$$

Bias

$$v_{gs} \ll 2(V_{GSQ} - V_{TN})$$

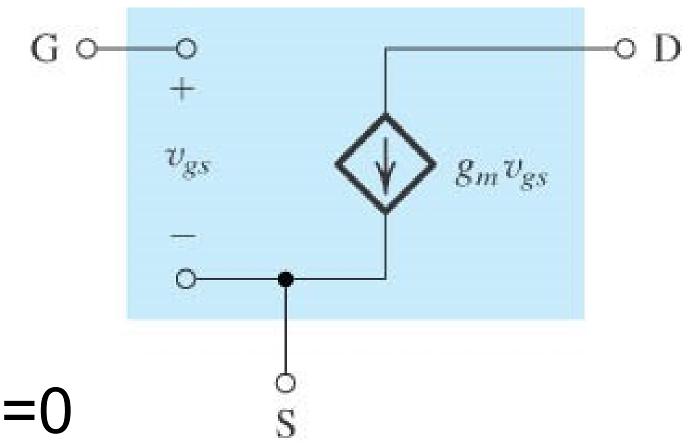


1. Determine the operating point (DC)
2. Determine response to the input (AC)
3. Perform superposition of the AC and DC responses

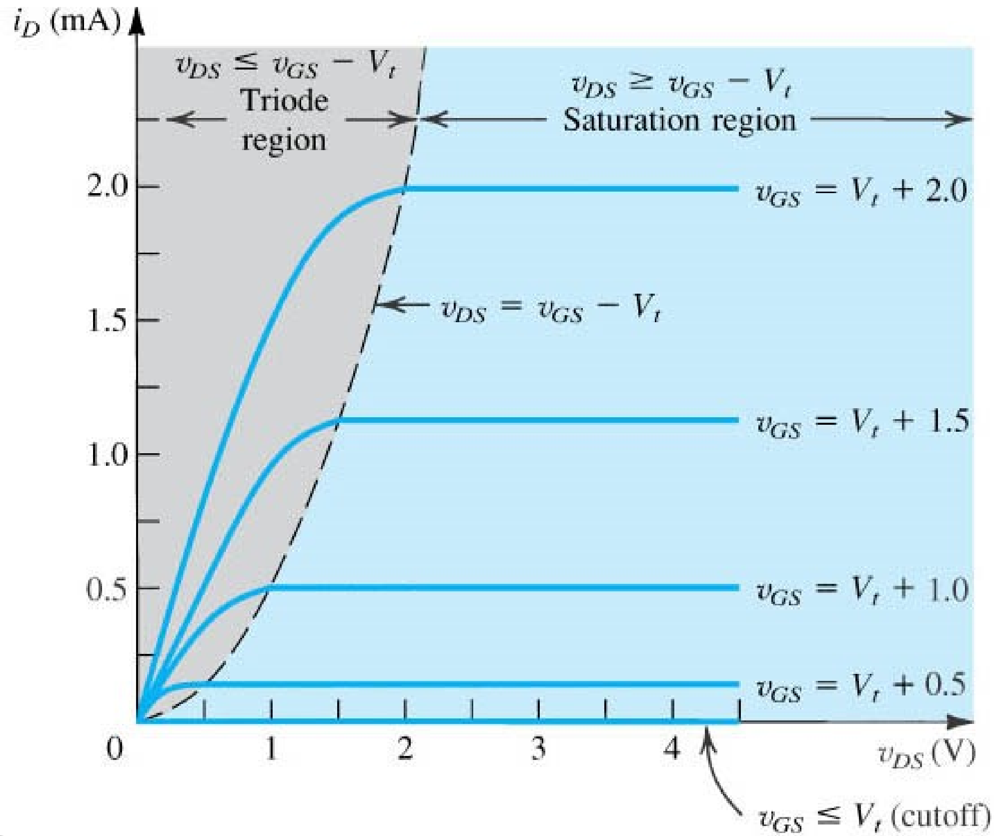
Small-signal equivalent circuit (NMOS)

The circuit below is valid at low enough frequency for the gate capacitance to act as an open circuit

π circuit



λ=0



(b)

$$i_D \simeq I_D + i_d$$

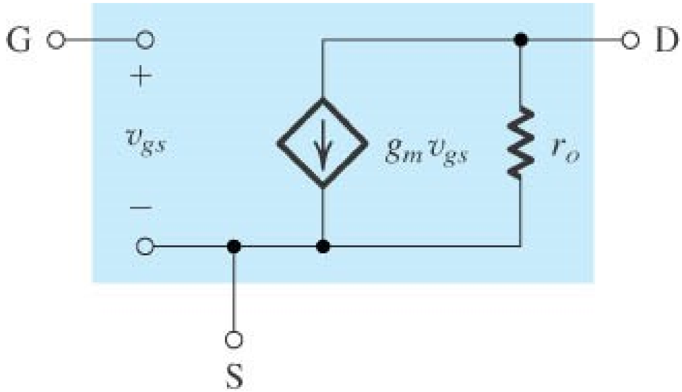
$$I_D = \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}(V_{GS}-V_T)^2$$

$$i_d = \underbrace{\frac{\varepsilon_{ox}}{t_{ox}}\mu_n\frac{W}{L}(V_{GS}-V_T)}_{= g_m} v_{gs}$$

$$v_{gs} \ll 2(V_{GSQ} - V_{TN})$$

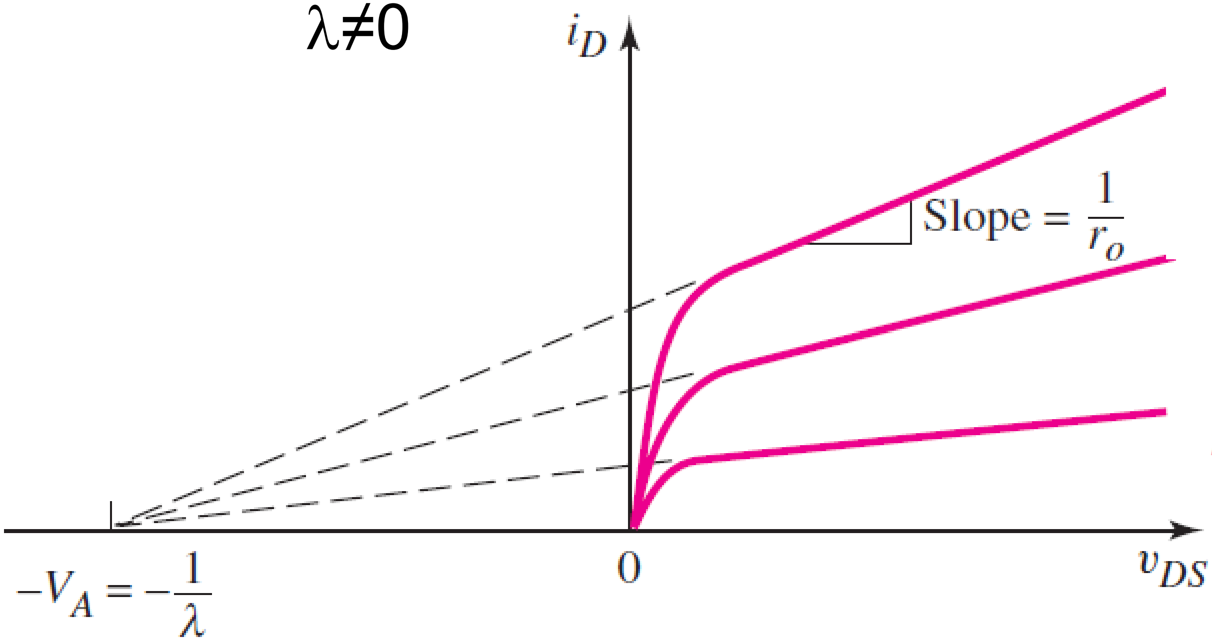
Channel modulation effect in MOSFETs

π circuit



This small signal equivalent circuit is valid at low enough frequency for the gate capacitance to act as an open circuit

λ≠0



$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})]$$

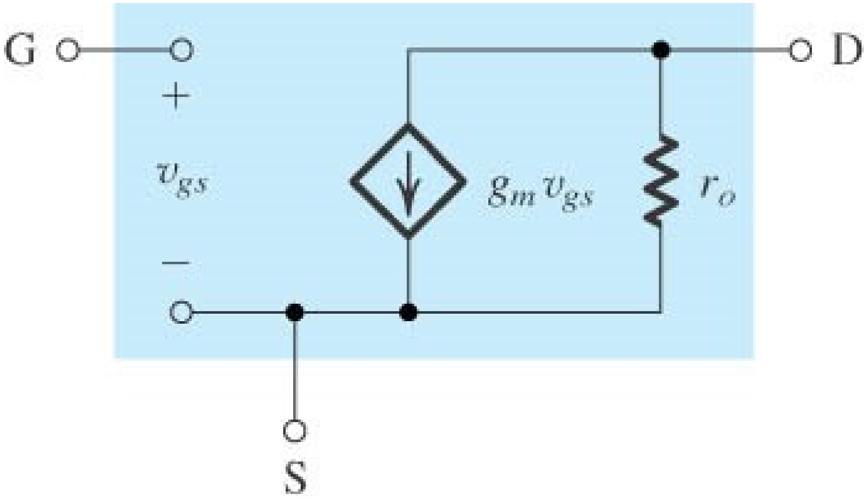
$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}}$$

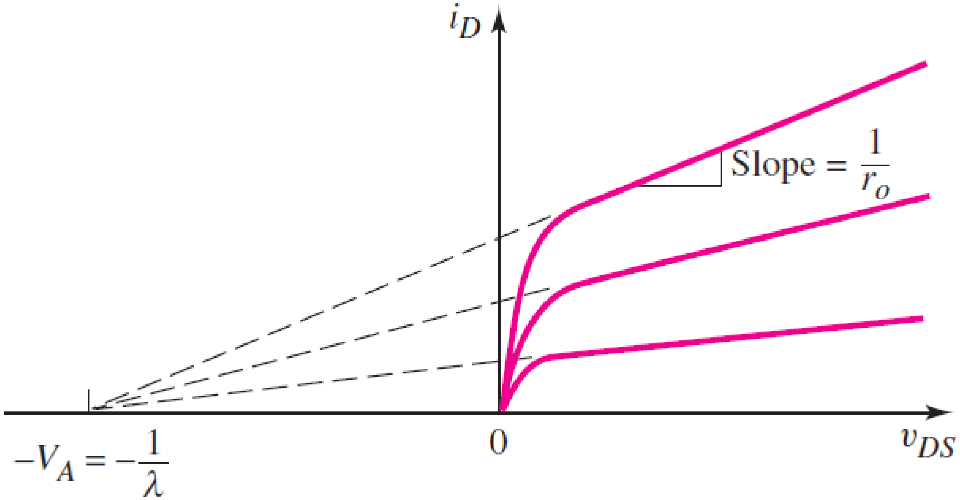
$$r_o = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1}$$

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

Small-signal equivalent circuit (NMOS)

This small signal equivalent circuit is valid at low enough frequency for the gate capacitance to act as an open circuit





$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GSQ}=\text{const.}} = 2K_n(V_{GSQ} - V_{TN})$$

$$r_o = \left.\left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\right|_{v_{GS}=\text{const.}}$$

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

Small-signal equivalent circuit (PMOS)

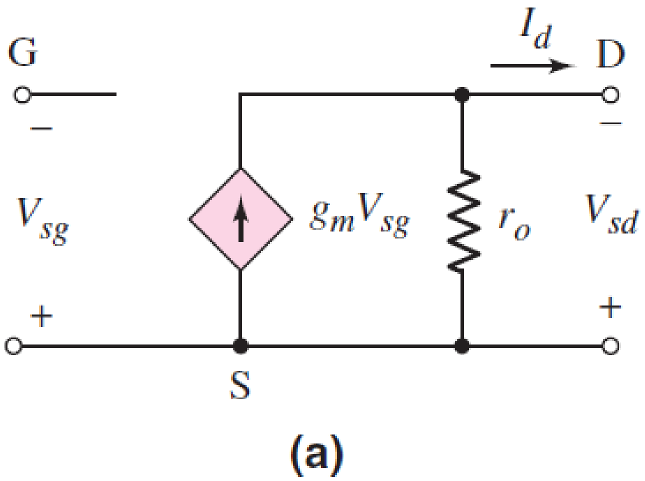


Figure 4.11 Small signal equivalent circuit of a p-channel MOSFET showing (a) the conventional voltage polarities and current directions and (b) the case when the voltage polarities and current directions are reversed.

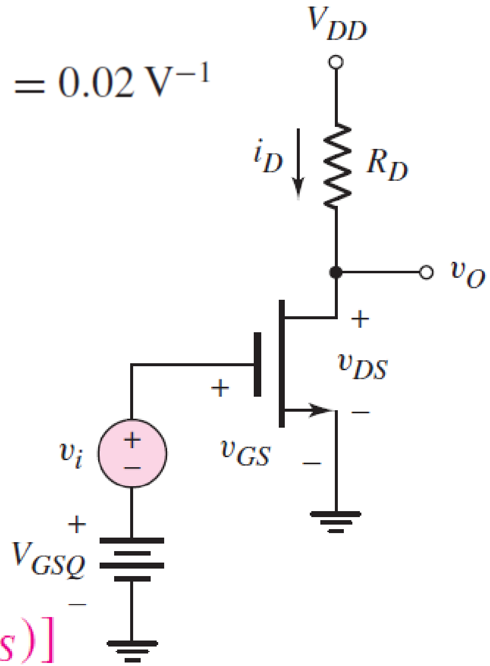
In class problem 1

TYU 4.3 For the circuit in Figure 4.1, the circuit and transistor parameters are given in Exercise TYU 4.2. If $v_i = 25 \sin \omega t$ (mV), determine i_D and v_{DS}.

$V_{TN} = 0.4$ V, $K_n = 0.5$ mA/V^2, and $\lambda = 0.02$ V^{-1}

$V_{DD} = 3.3$ V and $R_D = 8$ kΩ.

$I_{DQ} = 0.15$ mA



$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})]$$

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

$$g_m = 2\sqrt{K_n I_{DQ}}$$

Overview of lecture 6

- Amplifiers: Models and Characteristics (S&S 1.5.1, 1.5.3, 1.5.5, 5.6.2)
- FET amplifiers configurations: overview (Neamen 4.2, S&S 5.6.1)
- Common source (CS) amplifier configurations (Neamen 4.3, S&S 5.6.3, 5.6.4)