ECE 322L
Electronics 2

04/21/20 - Lecture 23

Class AB amplifiers

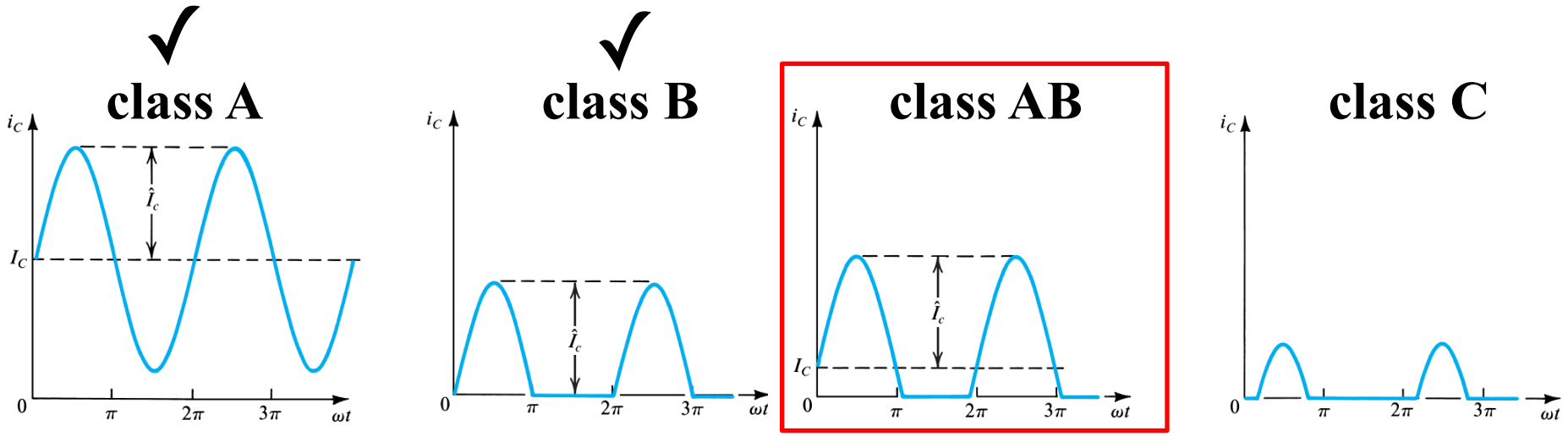
Overview

Class AB amplifiers

- Definition and general architecture
- Voltage-transfer characteristic (VTC)
- Output resistance
- Biasing configurations

(Neamen 8.3.3 and from 8.5.1 to 8.5.4-S&S, 6th edition, 11.5)

Classes of amplifiers



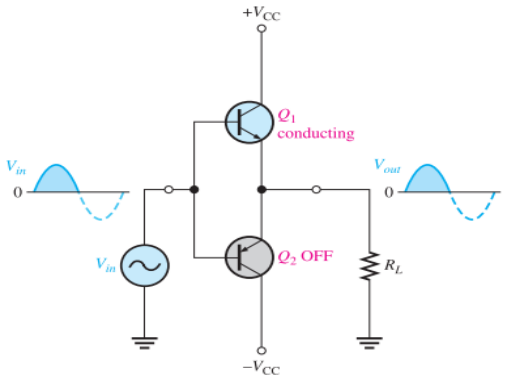
- **Class-A:** Output device(s) conduct through 360 degrees of input cycle (never switch off).
- **Class-B:** Output devices conduct for 180 degrees (1/2 of input cycle).
- **Class-AB:** Halfway (or partway) between the above two examples (181 to 200 degrees typical).
- **Class-C:** Output device(s) conduct for less than 180 degrees (100 to 150 degrees typical)

Class A and class B amplifiers

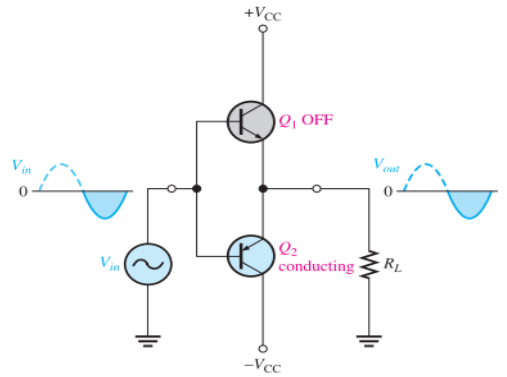
- Class A output stage is a simple linear amplifier.
- It is also very inefficient, typical maximum efficiency is between 10 and 20 %.
- Only suitable for low power applications.
- A class B output stage can be far more efficient than a class A stage (78.5 % maximum efficiency compared with 25 %).
- It also requires twice as many output transistors…
- …and it isn't very linear; cross-over distortion can be significant.

Class B amplifiers

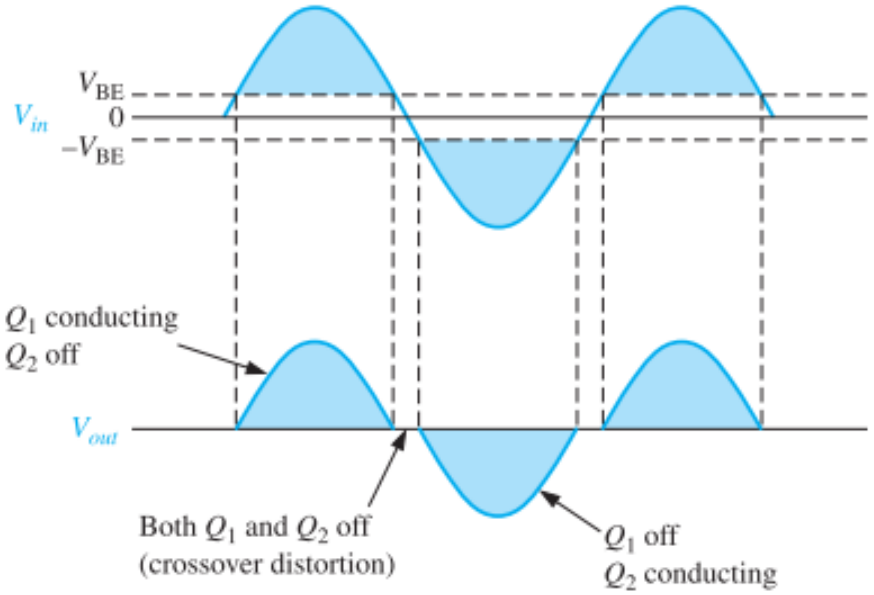
- ✓ When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts.
- ✓ Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting.
- ✓ The resulting distortion in the output waveform is called **crossover distortion**.



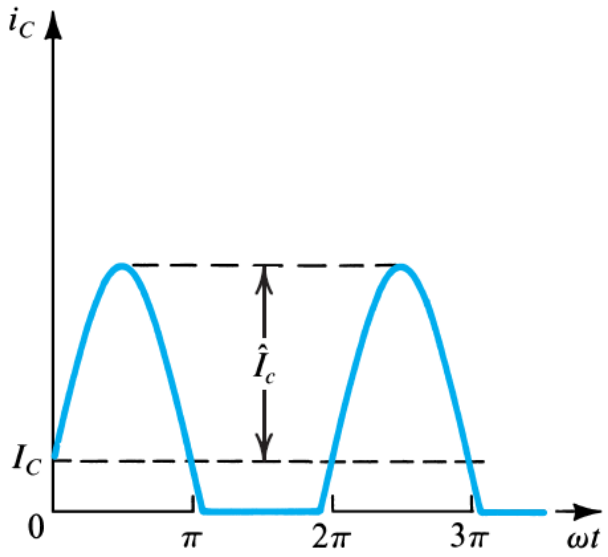
(a) During a positive half-cycle

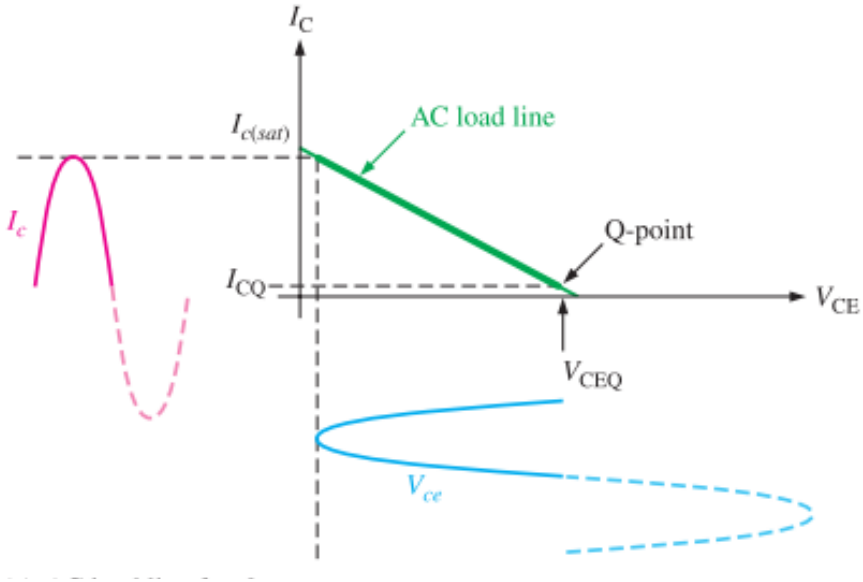


(b) During a negative half-cycle



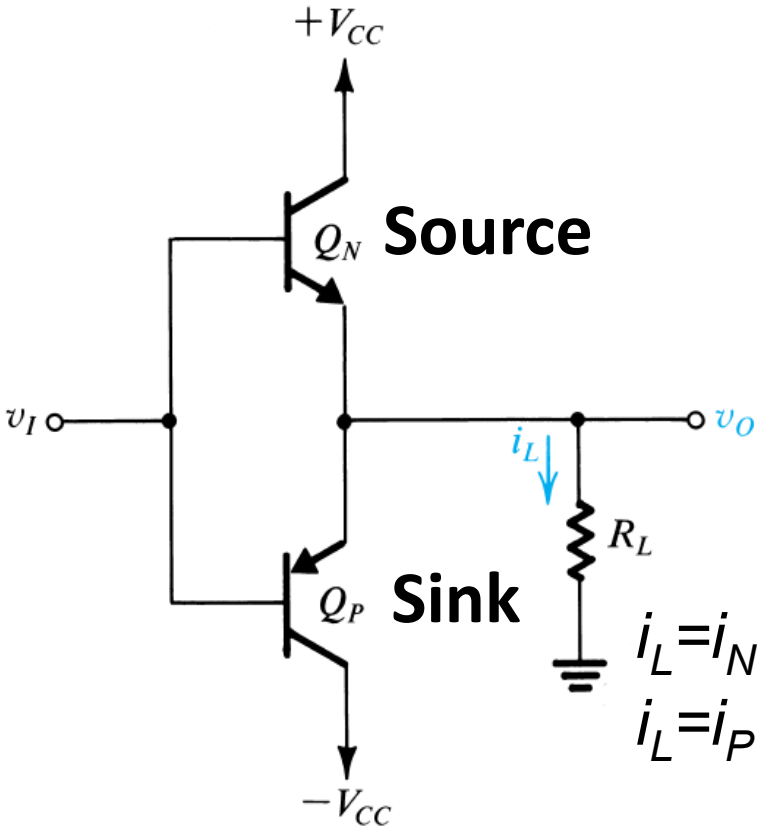
Class AB amplifiers





- The DC collector current is NOT zero!
- The DC collector current is lower than the peak amplitude of the ac collector current.
- The DC collector current is very small, i.e., the Q point is close to the cut-off region.
- Devices at the output stage conduct for more than 180 degrees (181 to 200 degrees typical).

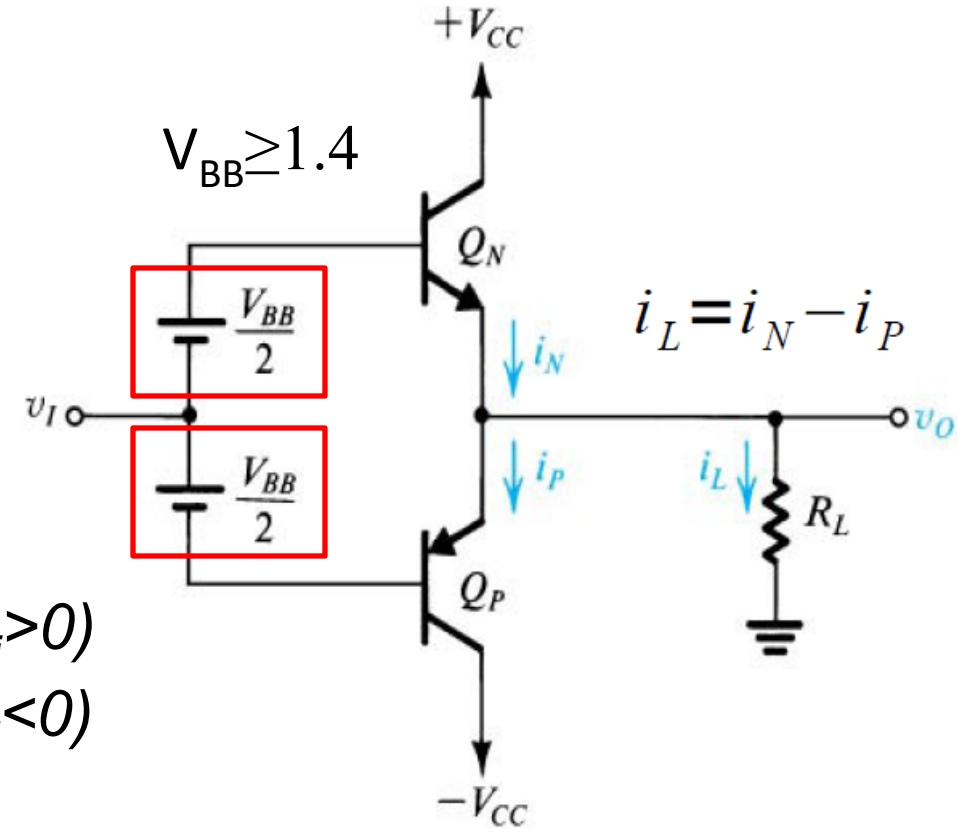
Push-pull: Class B vs Class AB



$i_L = i_N$ ($v_i > 0$)

$i_L = i_P$ ($v_i < 0$)

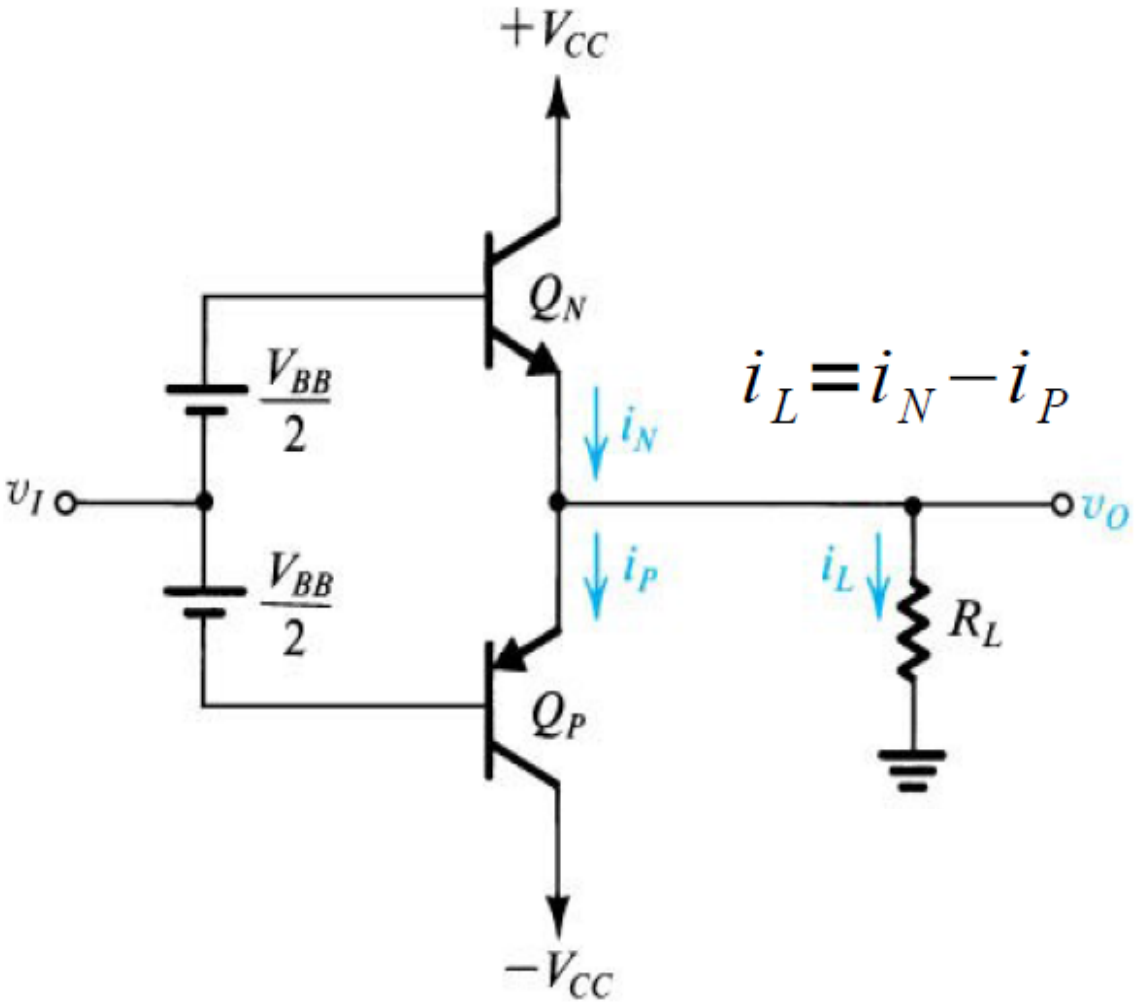
Class B



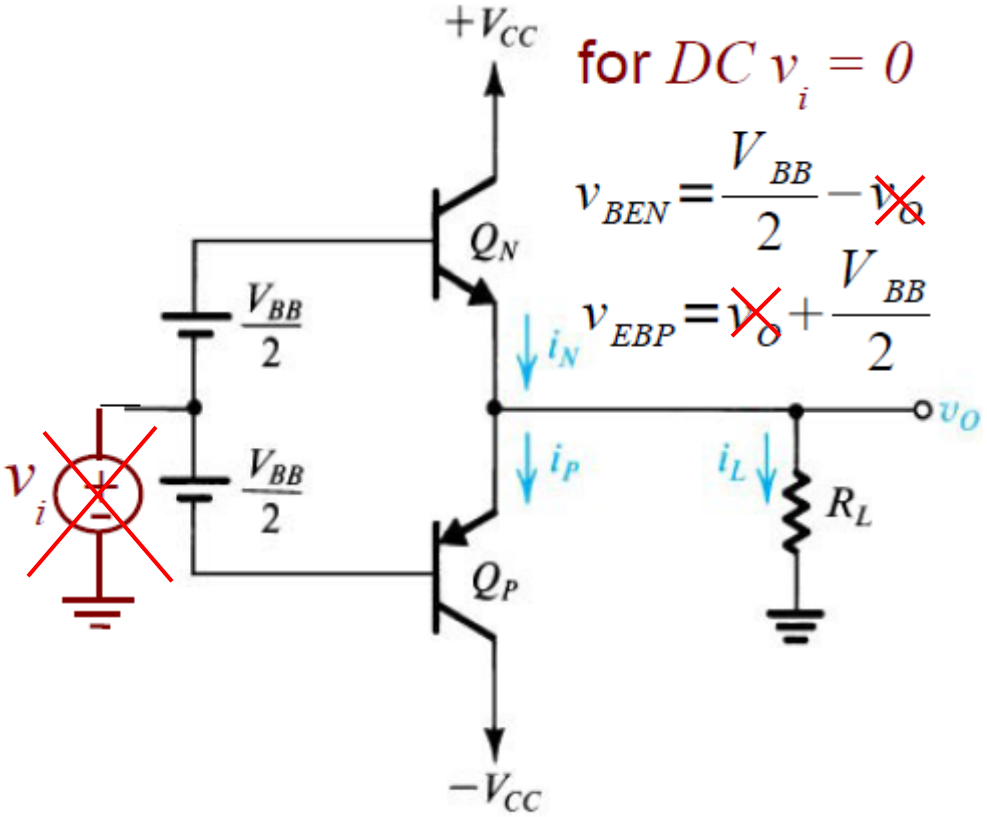
$i_L = i_N - i_P$

Class AB

Class AB amplifier



DC analysis

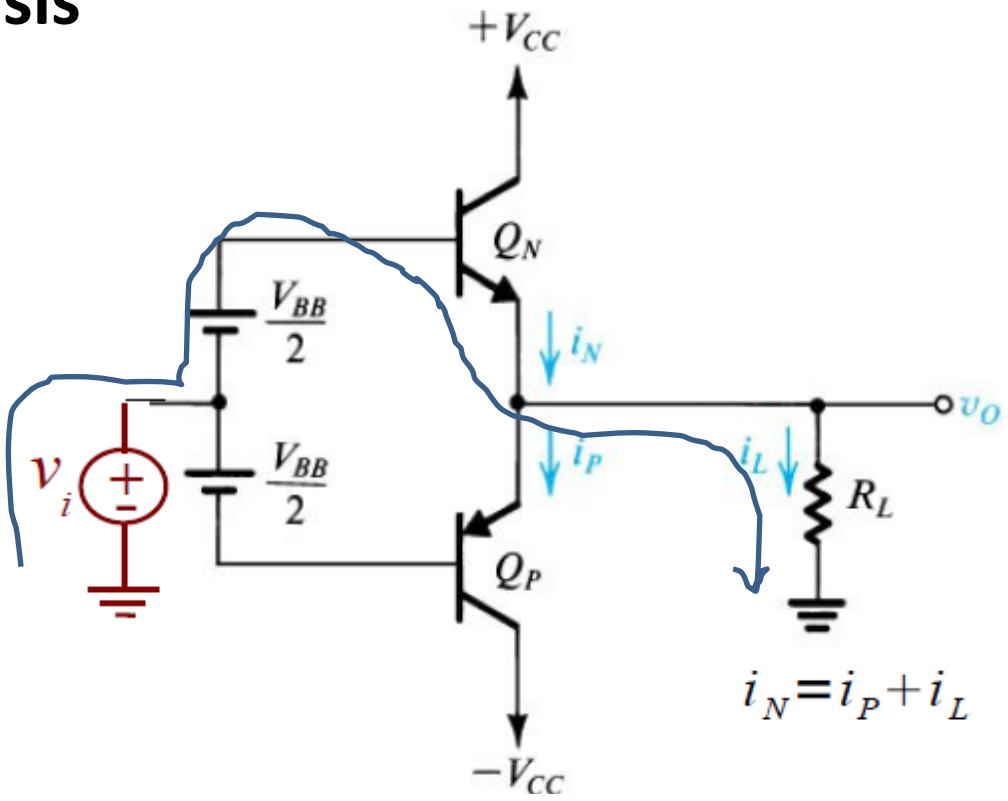


Bias (Q_N & Q_P matched):

$$I_N = I_P = I_Q = I_S e^{\frac{V_{BB}}{2V_T}}$$

Devices are biased at a non-zero collector current!

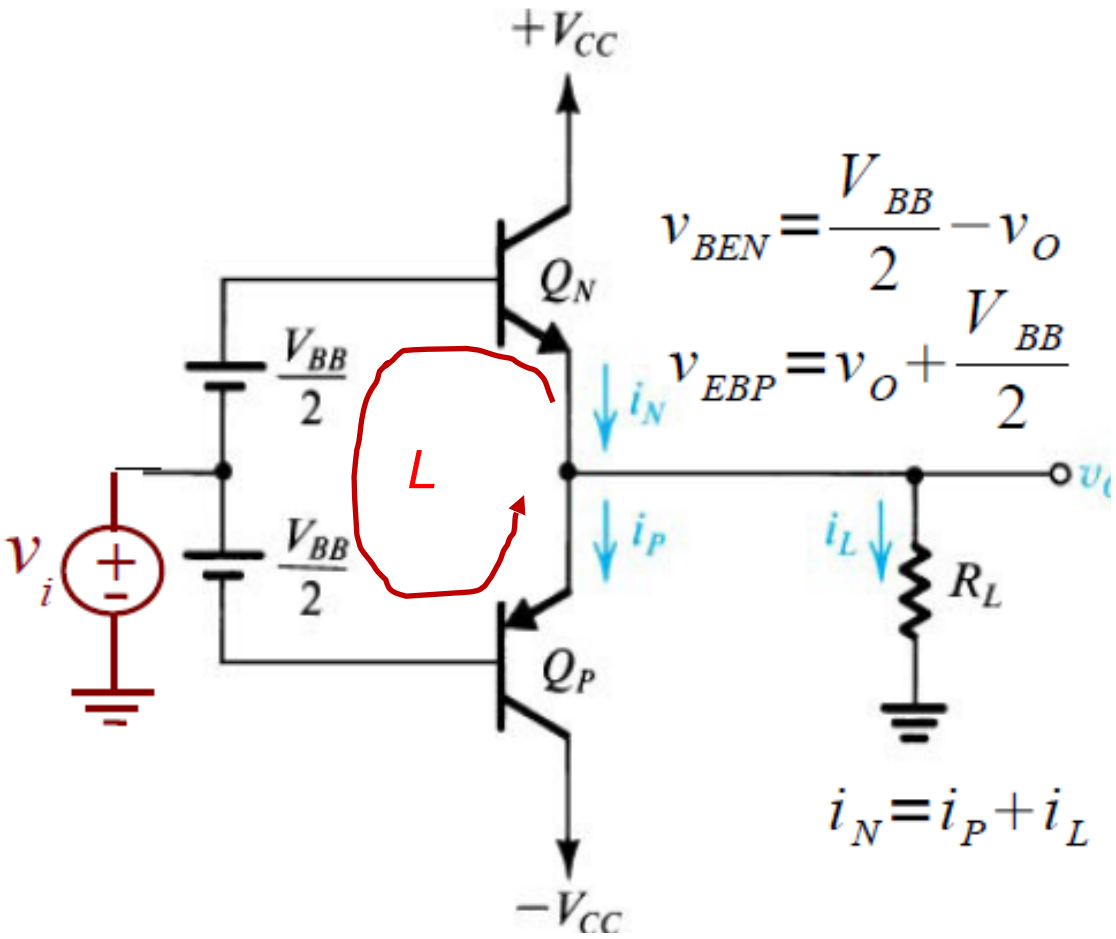
AC analysis



When v_I goes positive by a certain amount, the voltage at the base of Q_N increases by the same amount and the output becomes positive at an almost equal value,

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN} \qquad (11.24)$$

AC analysis



KVL at loop L

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

Constant base voltage condition

$$i_N i_P = I_Q^2$$

The constant base voltage condition $i_P i_N = I_Q^2$ where I_Q is typically small.

For example let $I_Q = 1\ mA$ and $i_N = 10\ mA$.

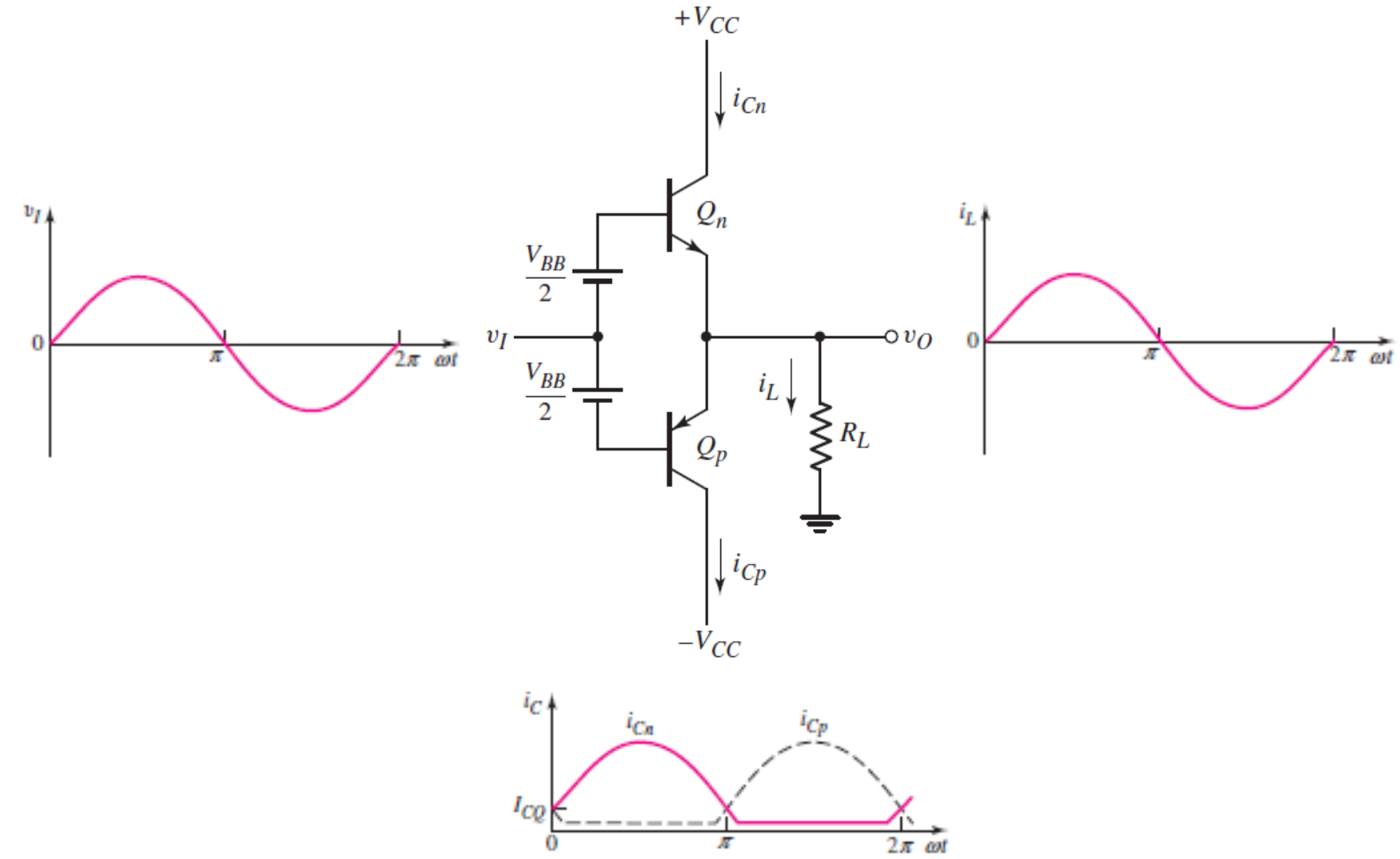
$$i_P = \frac{I_Q^2}{i_N} = \frac{1 \cdot 10^{-6}}{10 \cdot 10^{-3}} = 0.1\ mA = \frac{1}{100} i_N$$

The Class AB circuit, over most of its input signal range, operates as if either the Q_N or Q_P transistor is conducting and the Q_P or Q_N transistor is cut off.

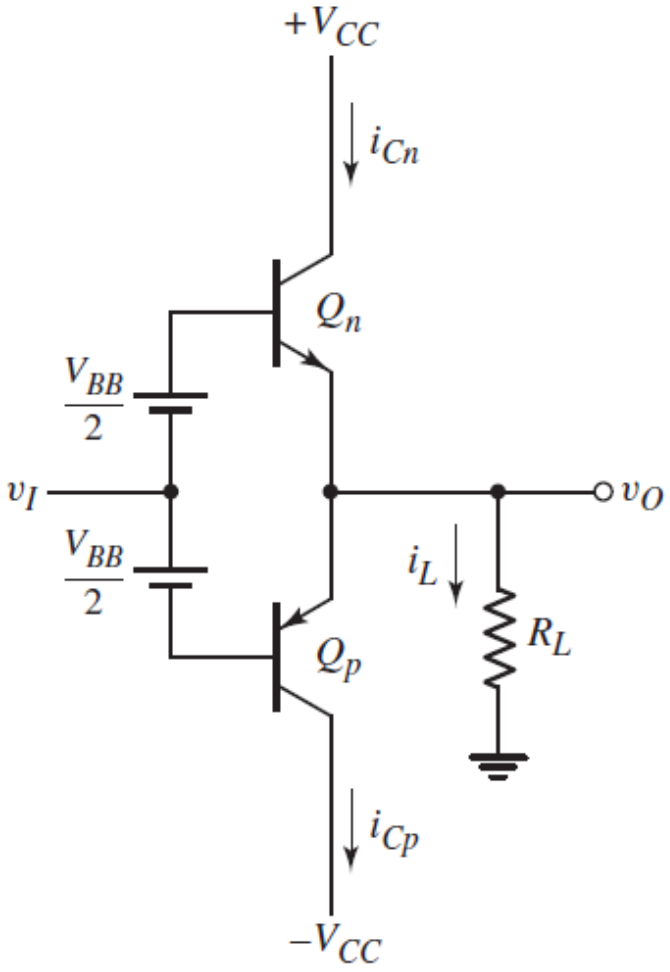
For small values of v_I both Q_N and Q_P conduct, and as v_I is increased or decreased, the conduction of Q_N or Q_P dominates, respectively.

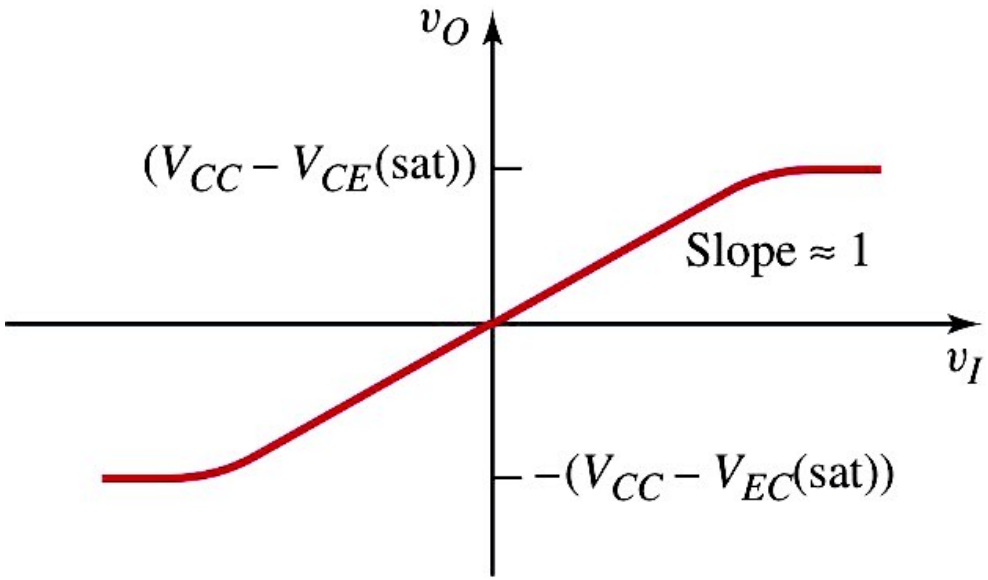
Using this approximation we see that a class AB amplifier acts much like a class B amplifier; but without the dead zone.

Signal voltages and currents

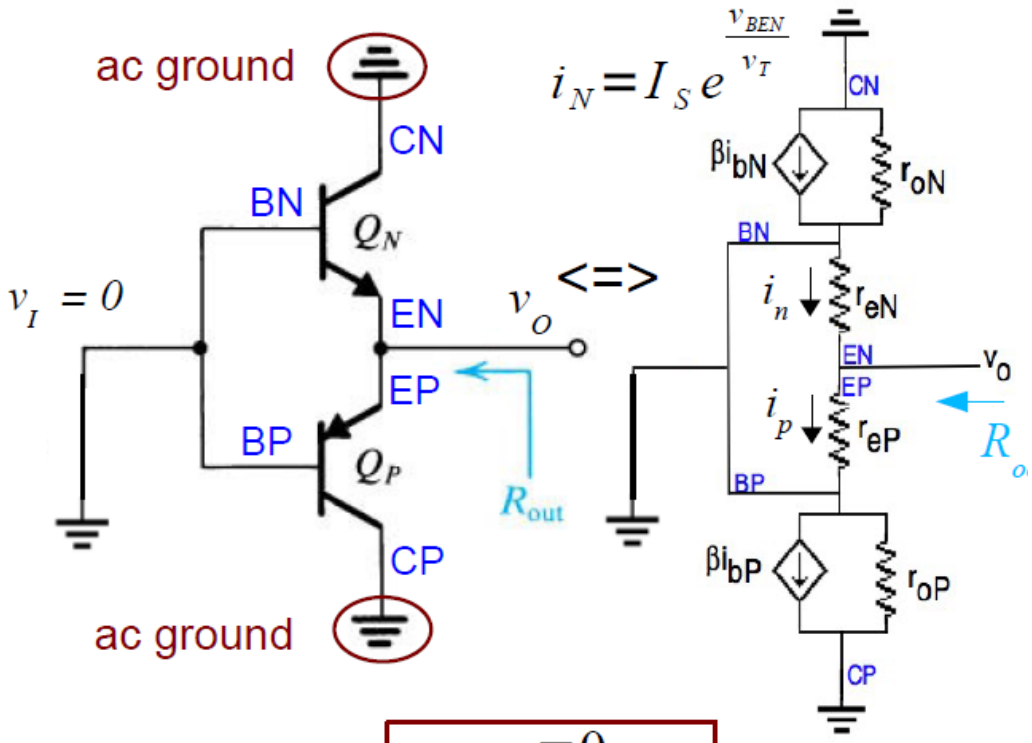


Voltage-transfer characteristic





Output resistance



$$v_I = 0$$
$$R_{out} = r_{eN} \| r_{eP}$$

$v_I > 0\ V$: $i_N > i_P \Rightarrow R_{out} \approx r_{eN}$

$v_I < 0\ V$: $i_P > i_N \Rightarrow R_{out} \approx r_{eP}$

The output resistance is low. Great!

Output resistance

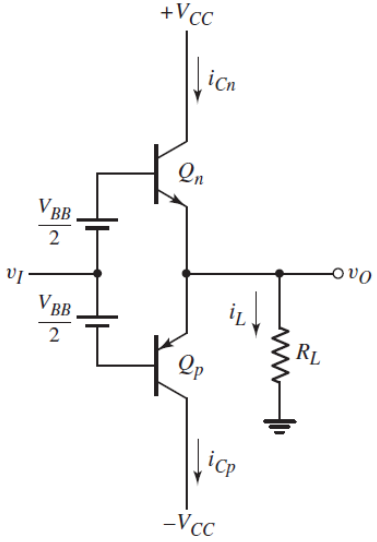
The two emitter resistors are in parallel:

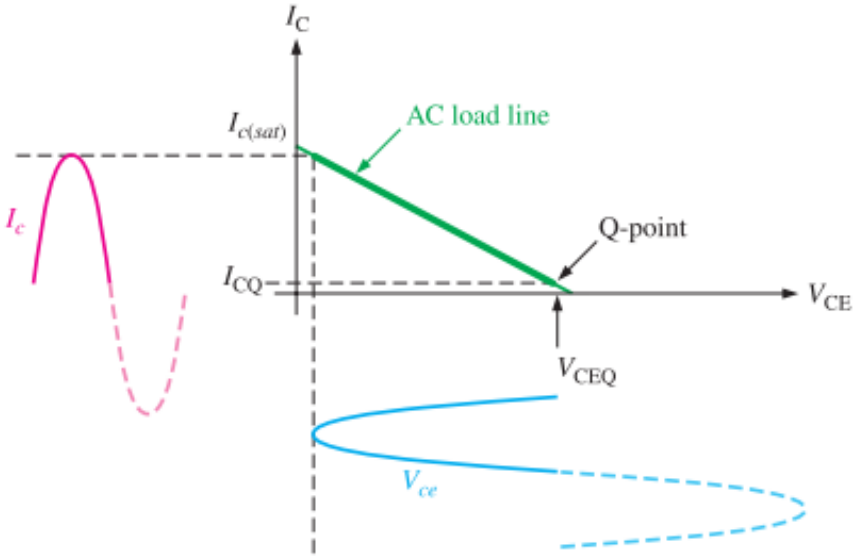
$$R_{out} = r_{eN} \| r_{eP} = \frac{\frac{V_T^2}{i_N i_P}}{\frac{V_T}{i_N} + \frac{V_T}{i_P}} = \frac{V_T}{i_N i_P \left(\frac{1}{i_N} + \frac{1}{i_P} \right)} = \frac{V_T}{i_N + i_P} \qquad \text{and} \qquad i_L = \frac{v_O}{R_L} = i_N - i_P$$

At $i_N = i_P$ (the no-signal condition i.e. $v_O = 0 \Rightarrow i_L = 0$): $i_N = i_P = I_Q$

$$R_{out} = \frac{V_T}{2 I_Q}$$

Efficiency





$$\eta = \frac{\text{signal load power}(\bar{P}_L)}{\text{supply power}(\bar{P}_S)} \qquad \eta_{max} = \frac{\bar{P}_{L,max}}{\bar{P}_S}$$

$$v_O = V_p \sin \omega t$$

$$\bar{P}_L = V_{o,rms} I_{o,rms} = \frac{V_{o,p}}{\sqrt{2}} \frac{I_{o,p}}{\sqrt{2}}$$

$$\bar{P}_L = \frac{V_{o,p,max}}{\sqrt{2}} \frac{I_{o,p,max}}{\sqrt{2}} \sim \frac{1}{2} V_{CEQ} I_{C(sat)}$$

$$\bar{P}_S = 2 V_{CC} I_{CQ}$$

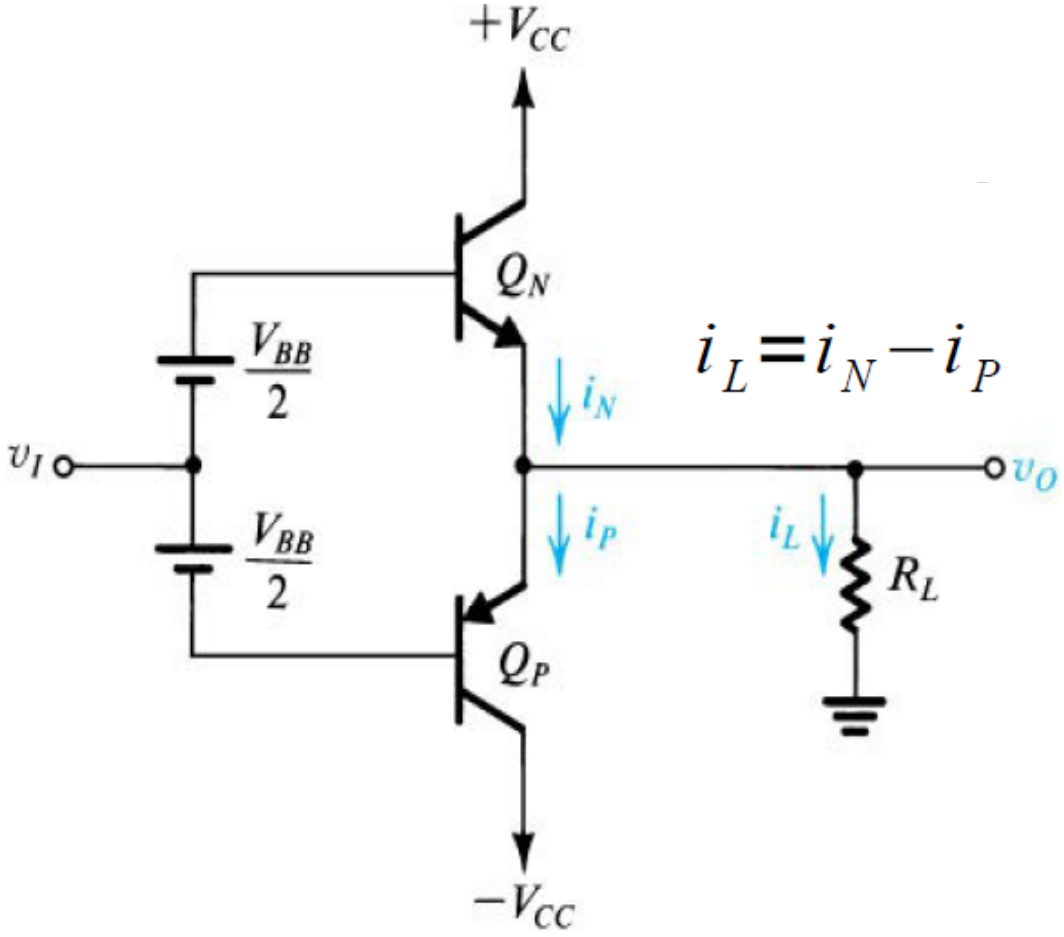
$$\eta_{max} \sim \frac{\frac{1}{2} V_{CEQ} I_{C(sat)}}{2 V_{CC} I_{CQ}} \sim 0.40 - 0.65$$

Class AB amplifiers

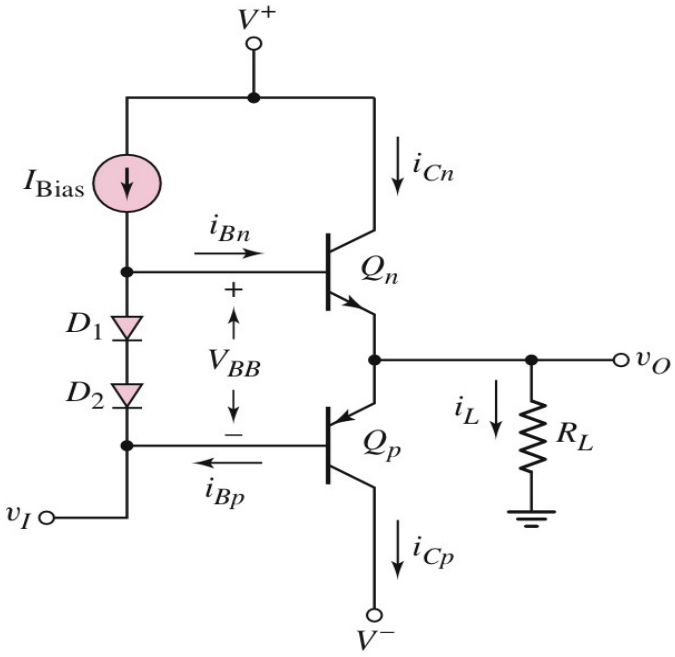
- A class B output stage can be far more efficient than a class A stage (~40-65% maximum efficiency compared with 25 %) but less efficient than a class B stage (~40-65 % maximum efficiency compared with 78.5 %).
- No cross-over distortion
- Suitable for large signals
- Intermediate characteristics between class A and B.

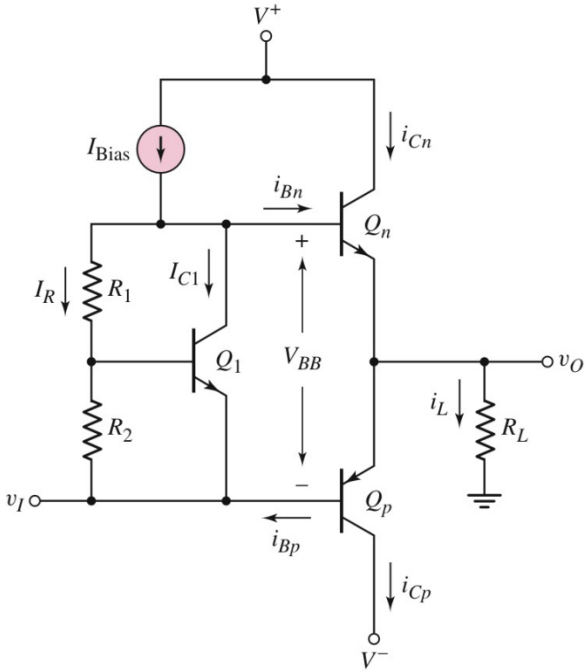
Class AB amplifier

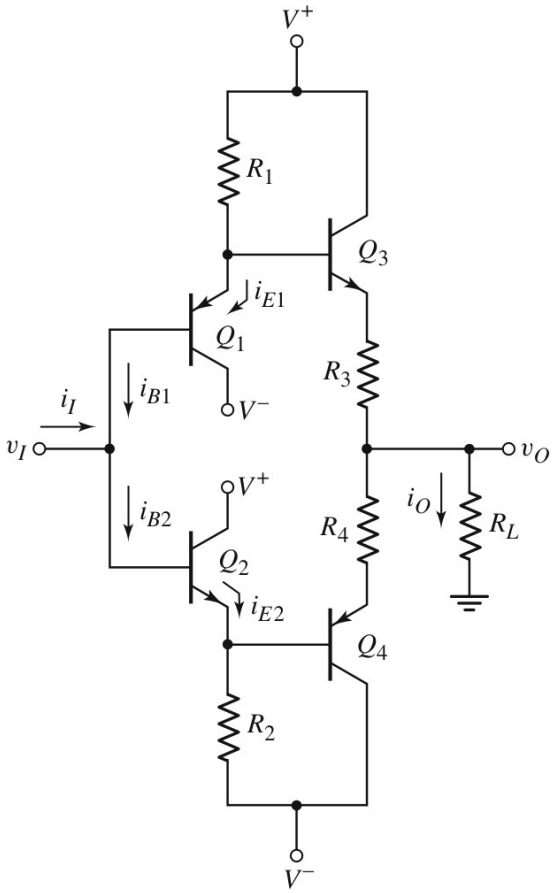
How can one practically realize the DC voltage V_{BB}?



- **Diode biasing**
- **Biasing with V_{BE} multiplier**
- **Biasing with input buffer transistor**

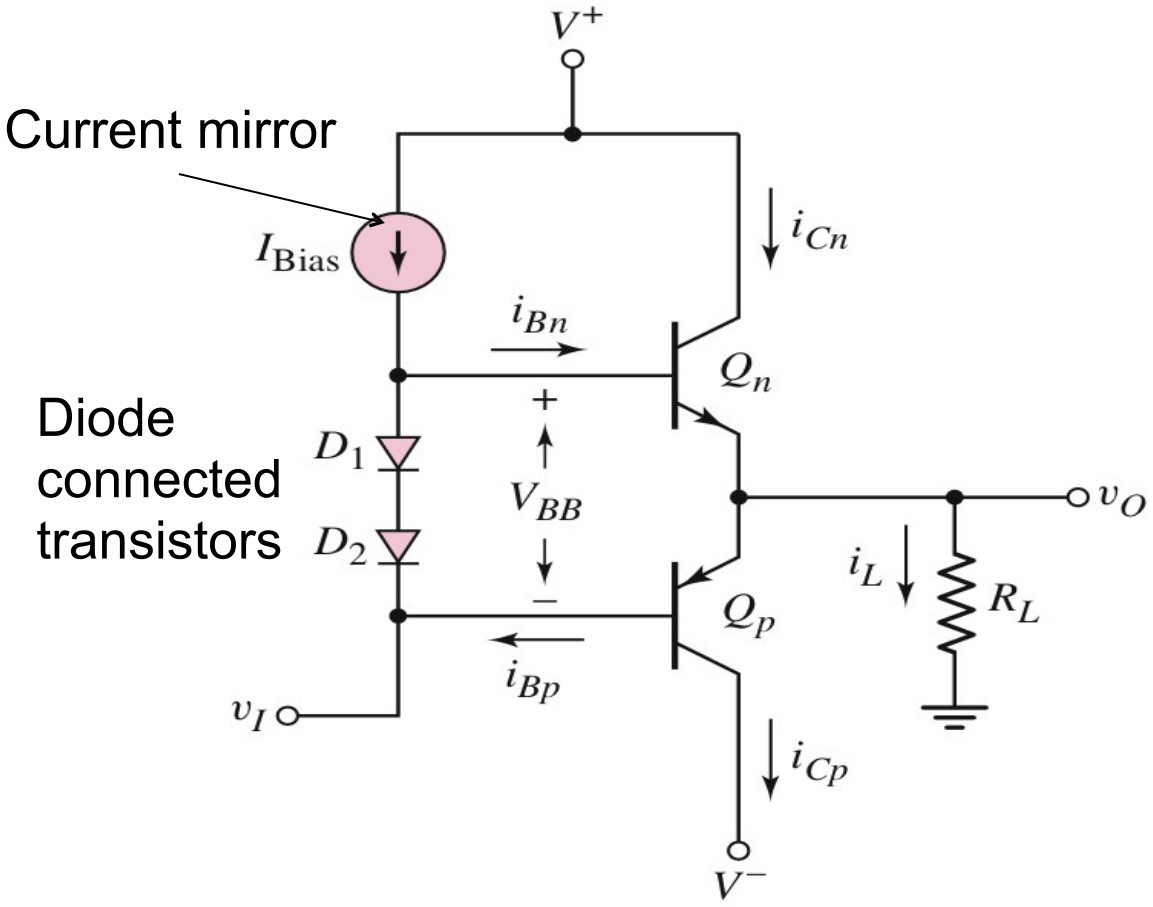




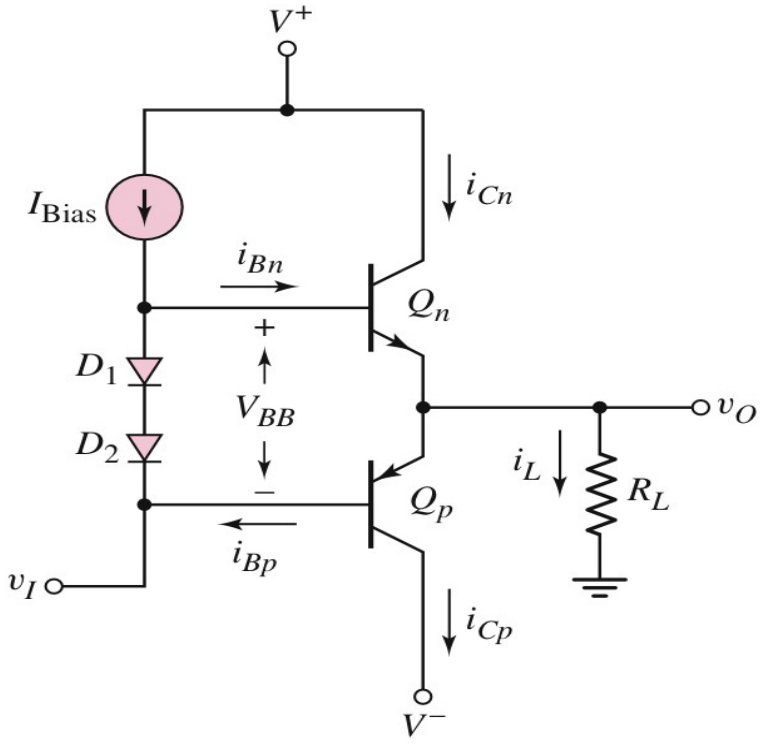


Diode biasing

The biasing circuit comprising D_1, D_2, I_{Bias}, *and* V^+ provides the biasing voltage V_{BB}.



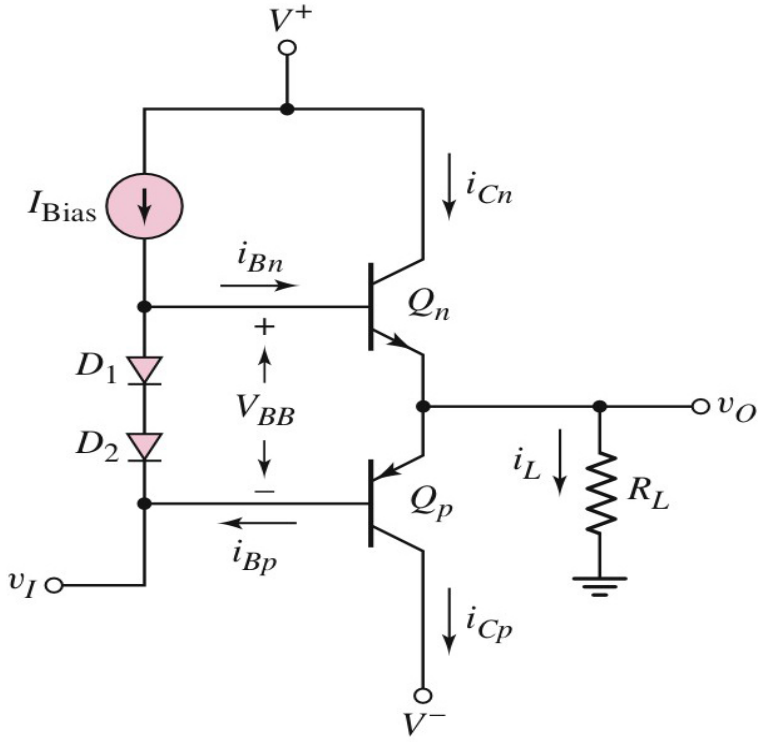
Diode biasing



Disadvantage:
V_{BB} is not stable against variations of the output voltage.

As the input voltage increases, the output voltage increases, causing an increase in i_{Cn}. This in turn produces an increase in the base current i_{Bn}. Since the increase in base current is supplied by I_{Bias}, the current through D_1 and D_2, and hence the voltage V_{BB}, decreases slightly.

Diode biasing



Benefit: prevents thermal runaway in the output devices if D_1 and D_2 are in thermal contact with them.

As the the temperature of the B-E junctions of the output devices increases, the biasing diodes that are in thermal contact with the emitter junctions will see an increase in temperature. As result the diode currents are going to increase and the base currents of the transistors are going to decrease, which leads to a decrease of the V_{BEn} (V_{EBp}) and of the i_{Cn} (i_{Cp}).

Biasing using a V_{BE} multiplier

The biasing circuit comprising Q_1, R_1, R_2 and I_{Bias}, provides the biasing voltage V_{BB}.

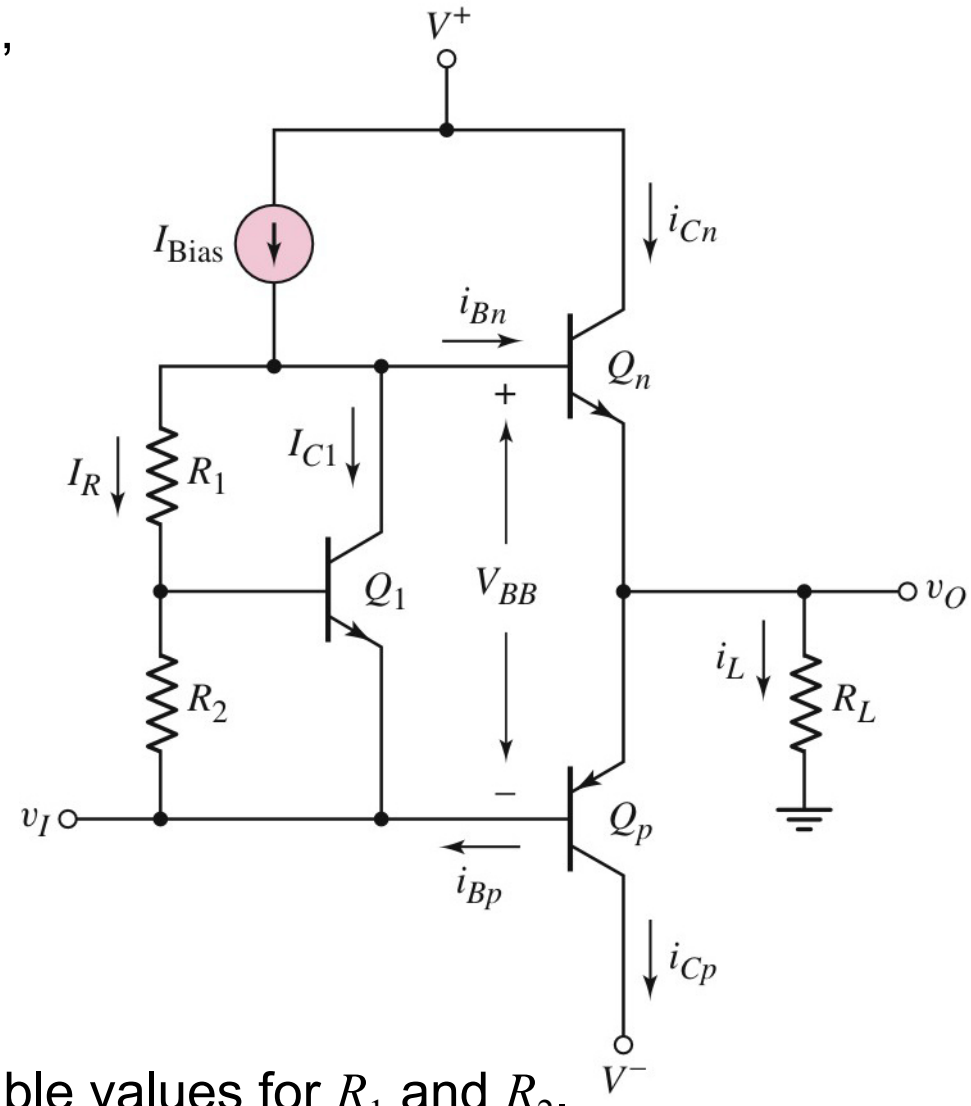
Neglecting the base current of Q_1;

$$I_R = \frac{V_{BE1}}{R_2}$$

$$V_{BB} = I_R\left(R_1 + R_2\right)$$

$$= V_{BE1}\left(1 + \frac{R_1}{R_2}\right)$$

Design parameters



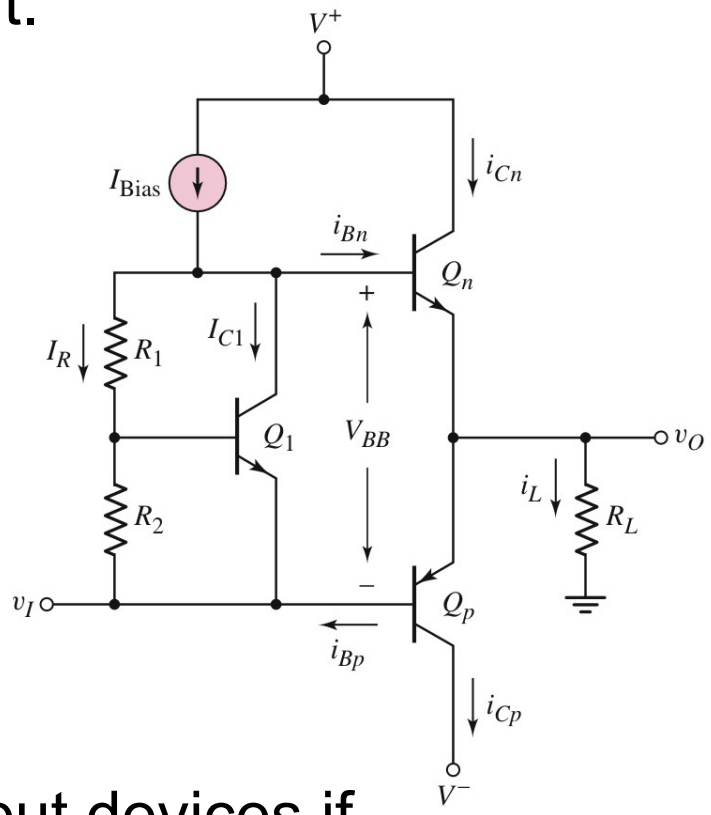
Thus, V_{BB} can be set by selecting suitable values for R_1 and R_2.

Biasing using a V_{BE} multiplier

As v_I increases, i_{Cn} increases followed by an increase of i_{Bn}. i_{C1} decreases but v_{BE1} is almost constant.

$$v_{BE1} = V_T \ln\left(\frac{i_{Cn}}{I_{S1}}\right)$$

$$I_R = \frac{V_{BE1}}{R_2}$$

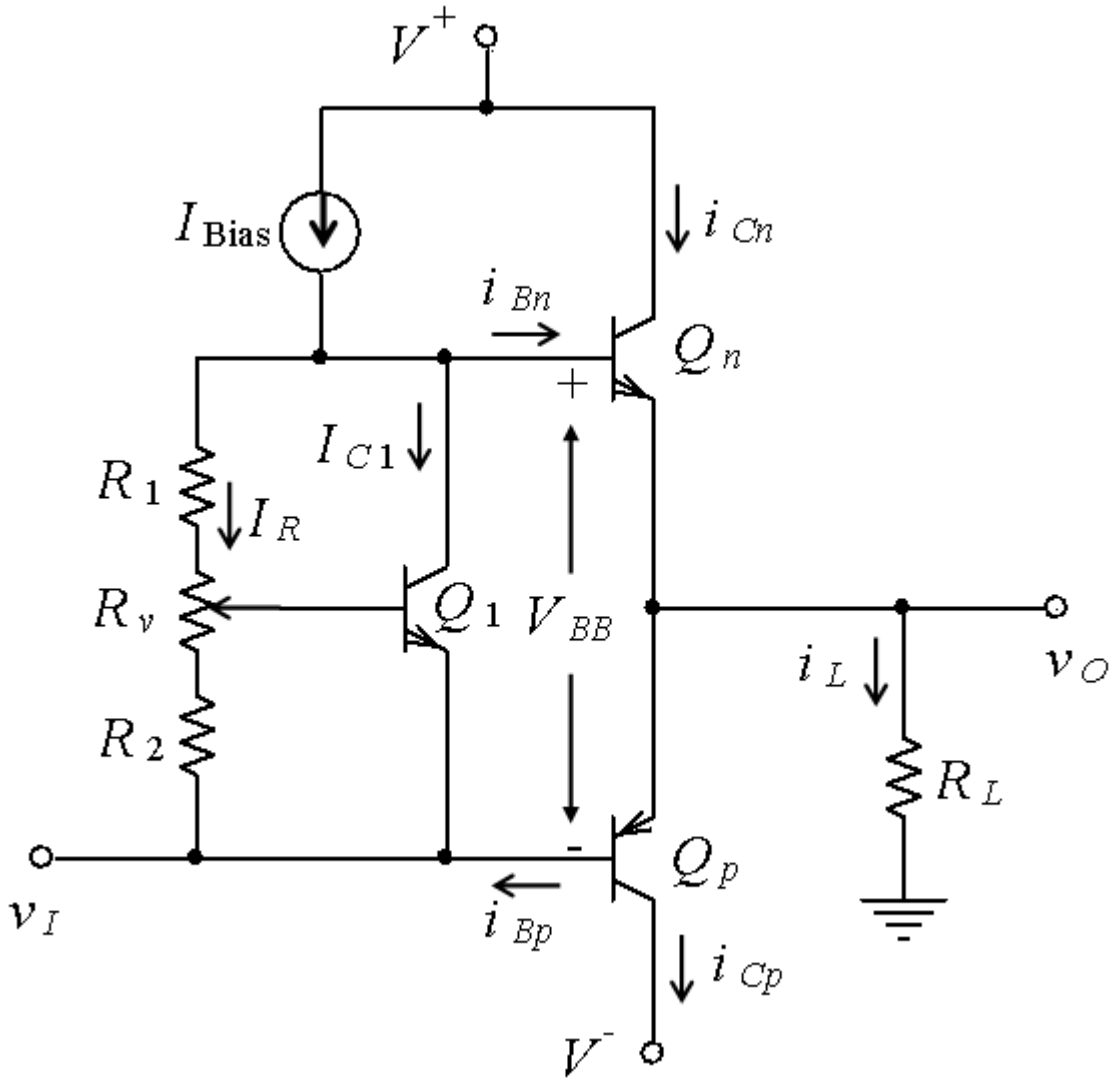


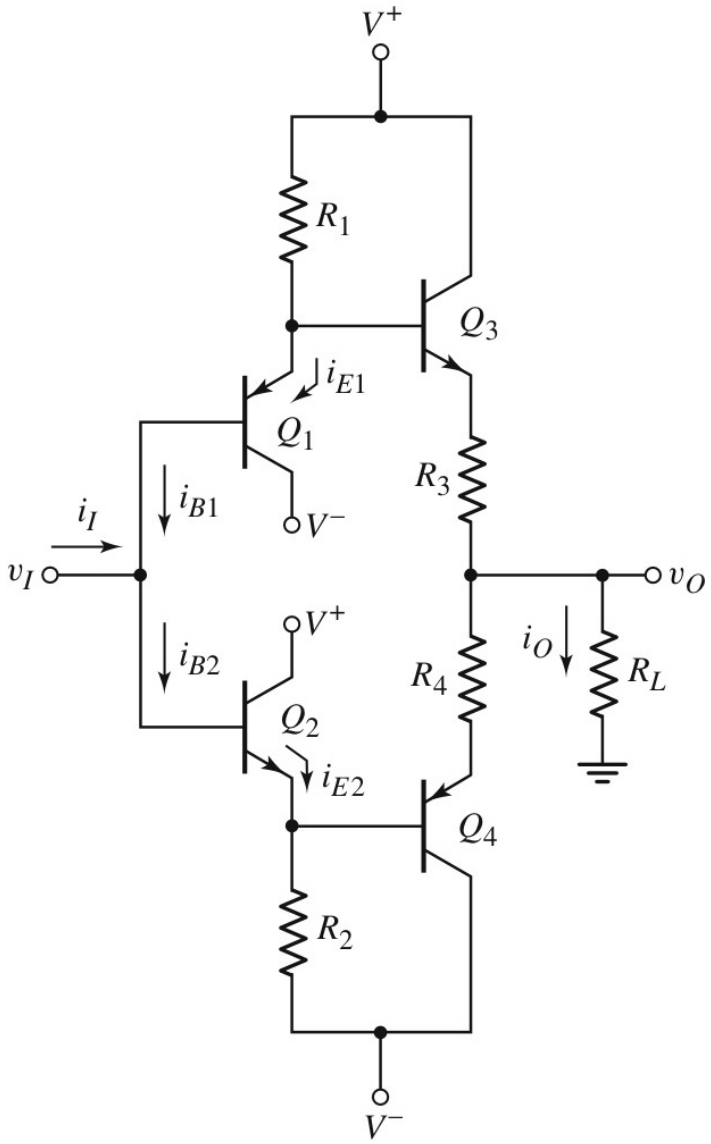
Bias is relatively stable against large variations of the output current.

It prevents thermal runaway in the output devices if Q_1 is in thermal contact with them. (Why? Test your understanding trying to answer)

Biasing using a V_{BE} multiplier

To facilitate adjustment of the ratio R_1/R_2 and hence, the value of V_{BB}, a third resistor R_v is typically included in the circuit.



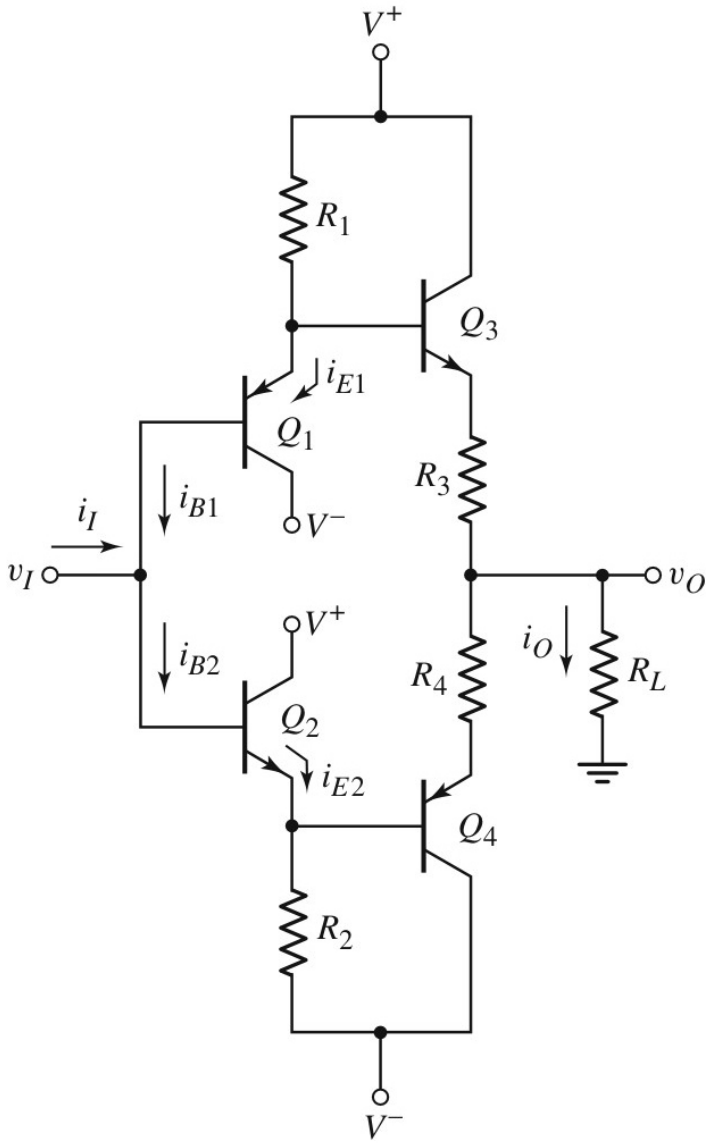


R_1, R_2 and the emitter-followers Q_1 and Q_2 establish the required quiescent bias.

The outputs of Q_1 and Q_2 follow the input signal and drive Q_3 and Q_4.

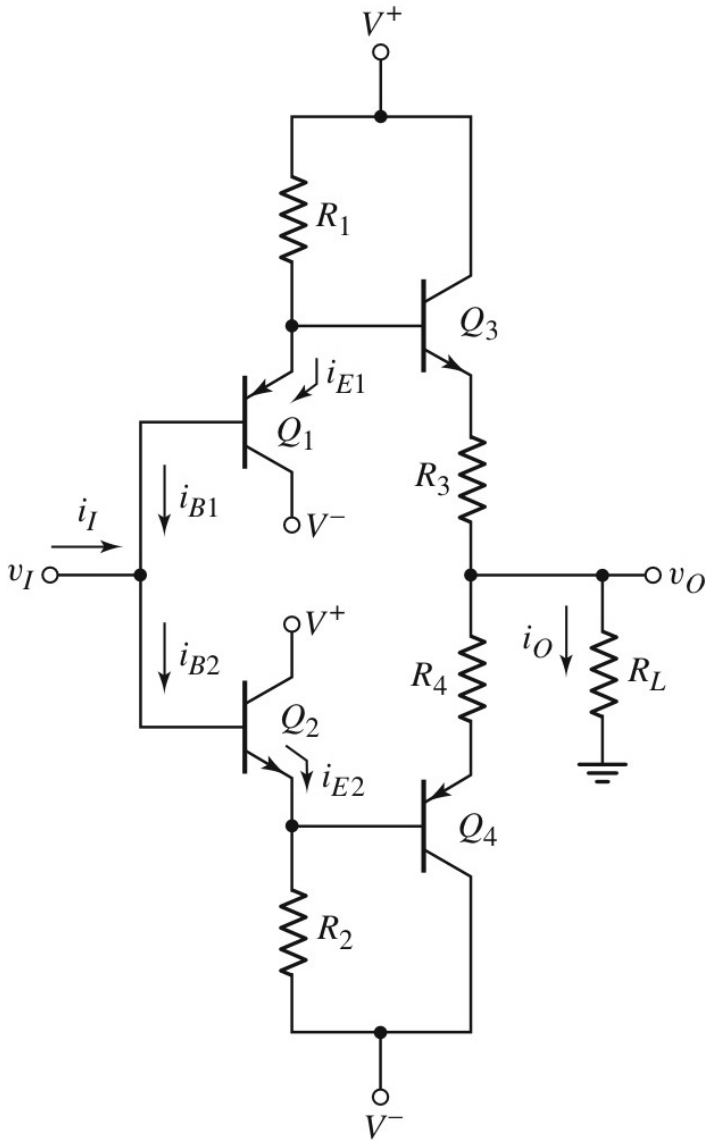
Benefits: stability and high current gain.

Stability



When the input voltage v_I increases, the base voltage of Q_3 increases and the output voltage v_O increases. The emitter current of Q_3 increases to supply the load current i_O.

The base current and the base voltage of of Q_3 both increase. The increase in base voltage of Q_3 reduces the voltage across, and the current through R_1. This means that i_{B1} and i_{E1} also decrease and the v_{BE1} stays more or less constant.



$$A_i = \frac{i_O}{i_I}$$

$$i_I = i_{B2} - i_{B1}$$

Neglecting i_{B3} and i_{B4} we have;

$$i_{B2} = \frac{(v_I - V_{BE}) - V^-}{(1+\beta_n)R_2}$$

and;

$$i_{B1} = \frac{V^+ - (v_I + V_{EB})}{(1+\beta_p)R_1}$$

Current gain

If;

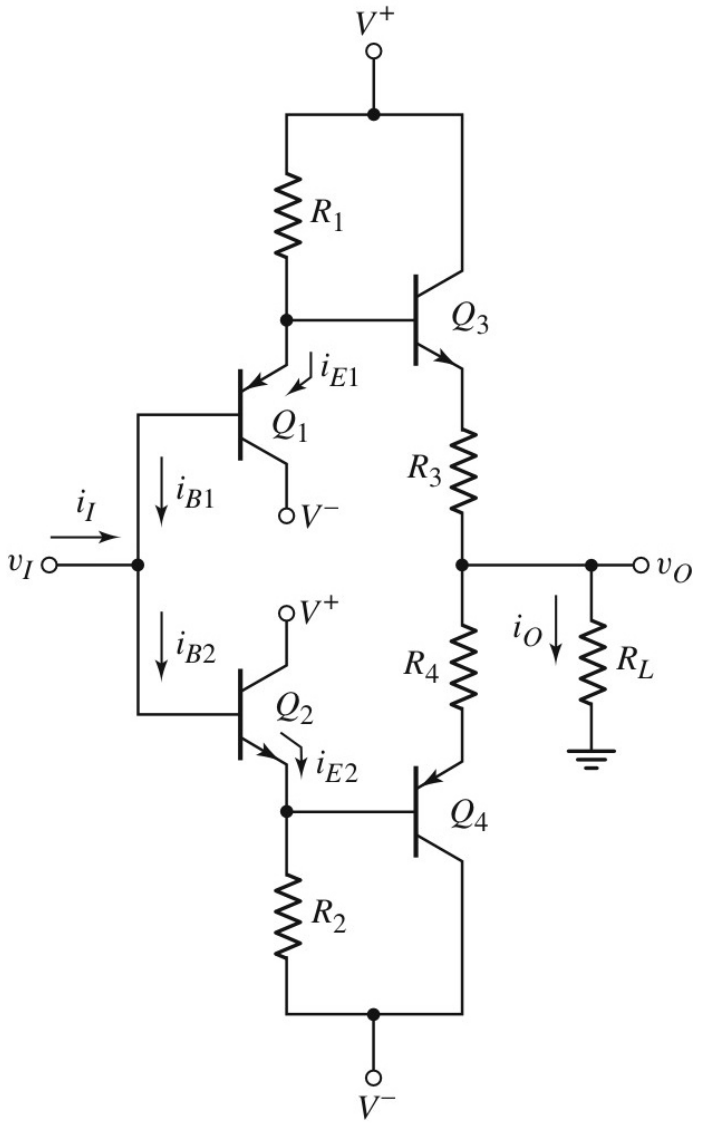
$$V^+ = -V^-,\ V_{BE} = V_{EB},\ R_1 = R_2 \equiv R$$

and; $\beta_n = \beta_p \equiv \beta$

then;

$$i_I = \frac{v_I - V_{BE} - V^-}{(1+\beta)R} - \frac{V^+ - v_I - V_{EB}}{(1+\beta)R}$$

$$= \frac{2v_I}{(1+\beta)R}$$



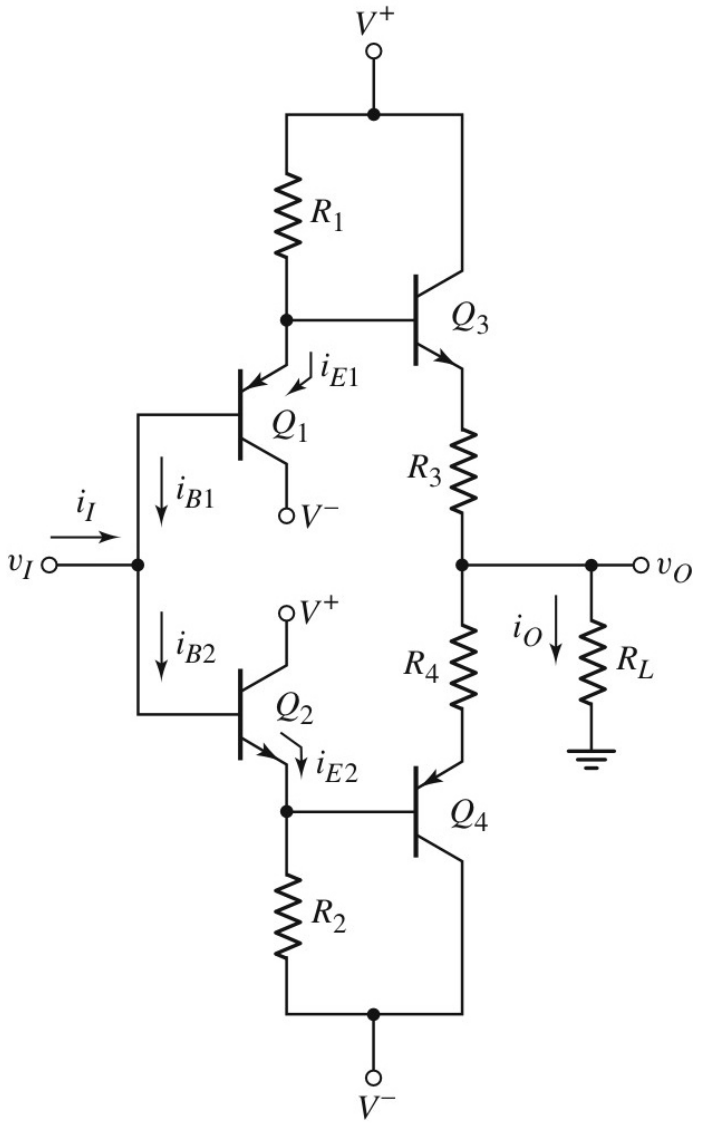
Since the voltage gain is approximately unity, the output current is;

$$i_O = \frac{v_O}{R_L} \cong \frac{v_I}{R_L}$$

The current gain is;

$$A_i = \frac{i_O}{i_I} = \frac{(1+\beta)R}{2R_L}$$

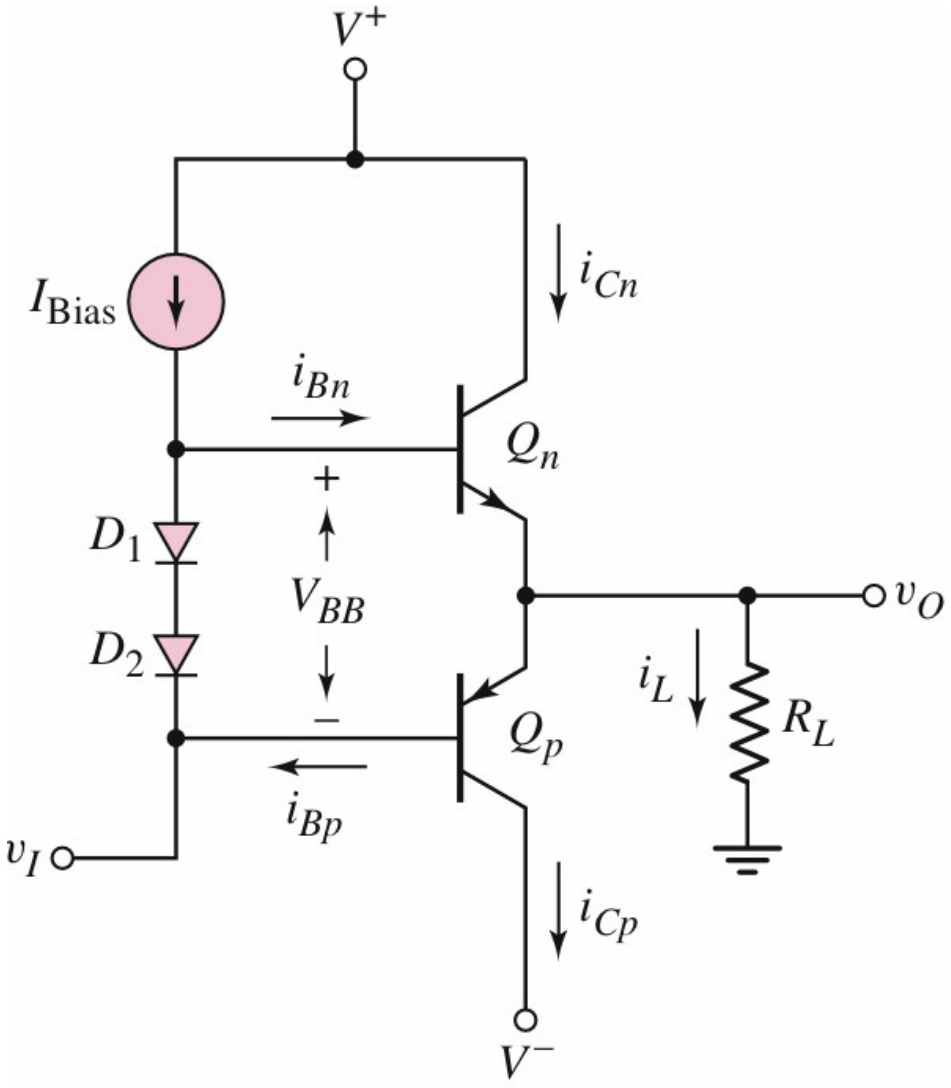
which is quite substantial. A large current gain is desirable since the output stage must typically deliver large currents to a load



In-class problem 1

A diode biasing class AB power amplifier is to meet the following specifications:

- R_L = 8 Ω;
- Average output power delivered to the load P_L = 5 W;
- peak output voltage to be not more than 80% of V_{CC};
- minimum value of I_D to be no less than 5 mA



In-class problem 1

For both Q_n and Q_p;

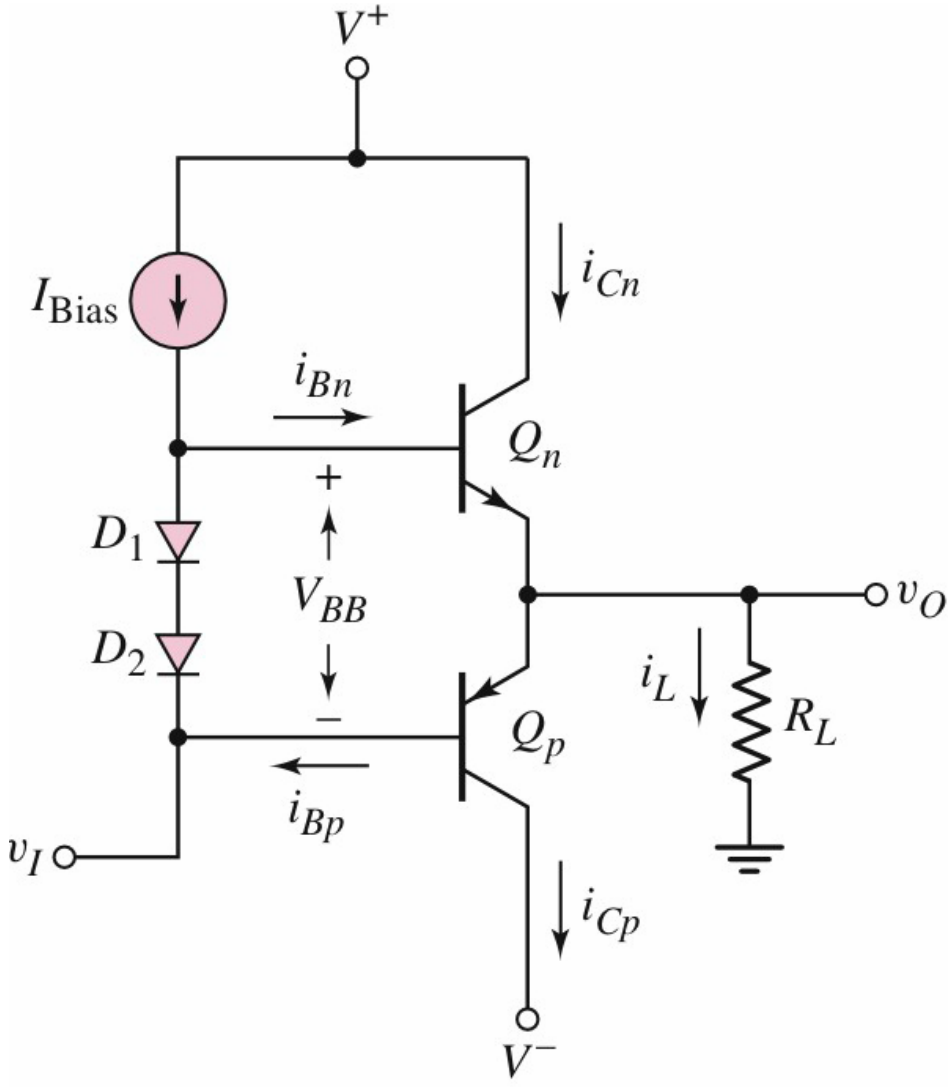
$$I_{SQ} = 10^{-13}\ \text{A};\ \beta = 75$$

For D_1 and D_2

$$I_{SD} = 3\times10^{-14}\ \text{A}$$

Determine;

a) I_{Bias} and V_{CC};
b) The quiescent collector current
c) i_{Cn} and i_{Cp} and V_{BB} when the output voltage is at its peak positive value



In-class problem 1, solution

a)

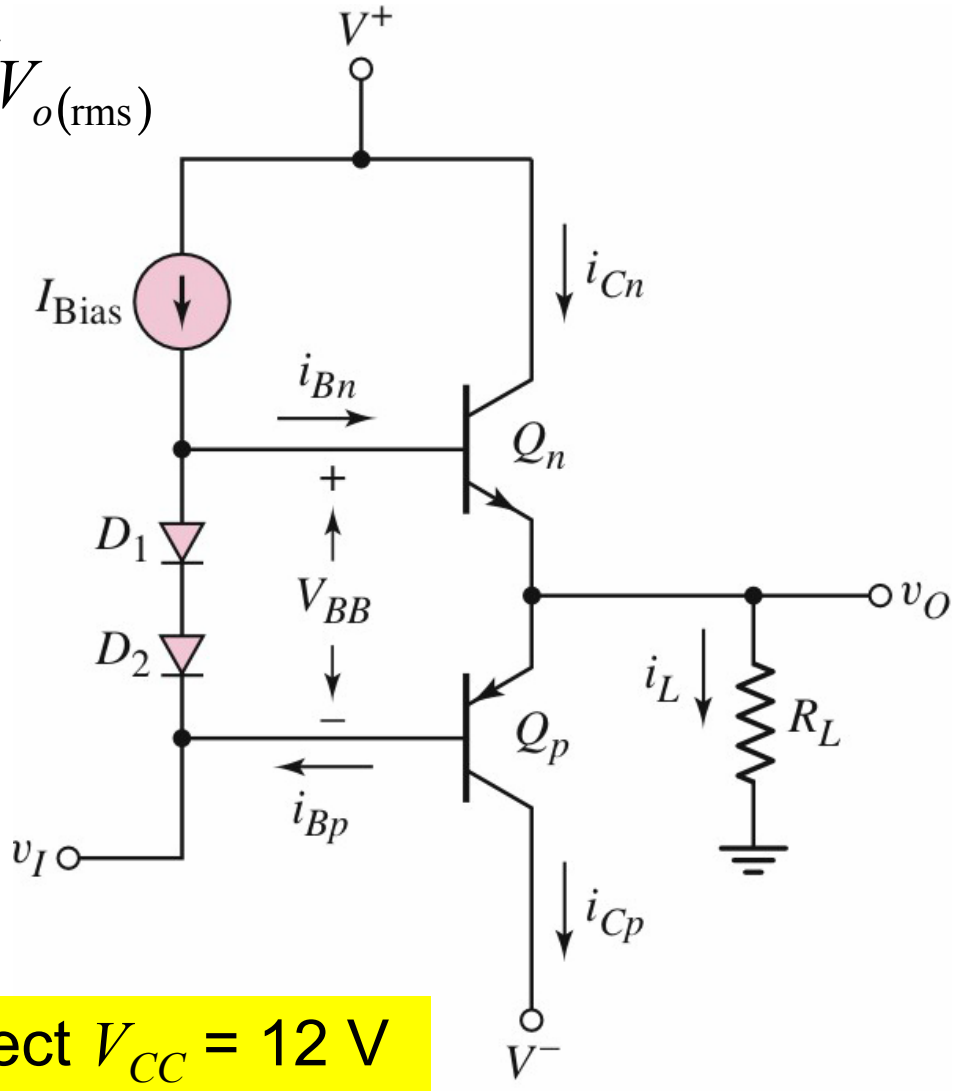
$$V_{CC} = \frac{V_{o(\text{peak})}}{0.8} \quad V_{o(\text{peak})} = \sqrt{2}V_{o(\text{rms})}$$

$$V_{o(\text{rms})} = \sqrt{P_L R_L}$$

$$= \sqrt{5 \times 8} = 6.32 \text{ V}$$

$$V_{o(\text{peak})} = \sqrt{2}V_{o(\text{rms})} = 8.94 \text{ V}$$

$$V_{CC} = \frac{V_{o(\text{peak})}}{0.8} = 11.8 \text{ V}$$



Select V_{CC} = 12 V

In-class problem 1, solution

$$I_{\text{Bias}} = i_{Bn} + I_D$$

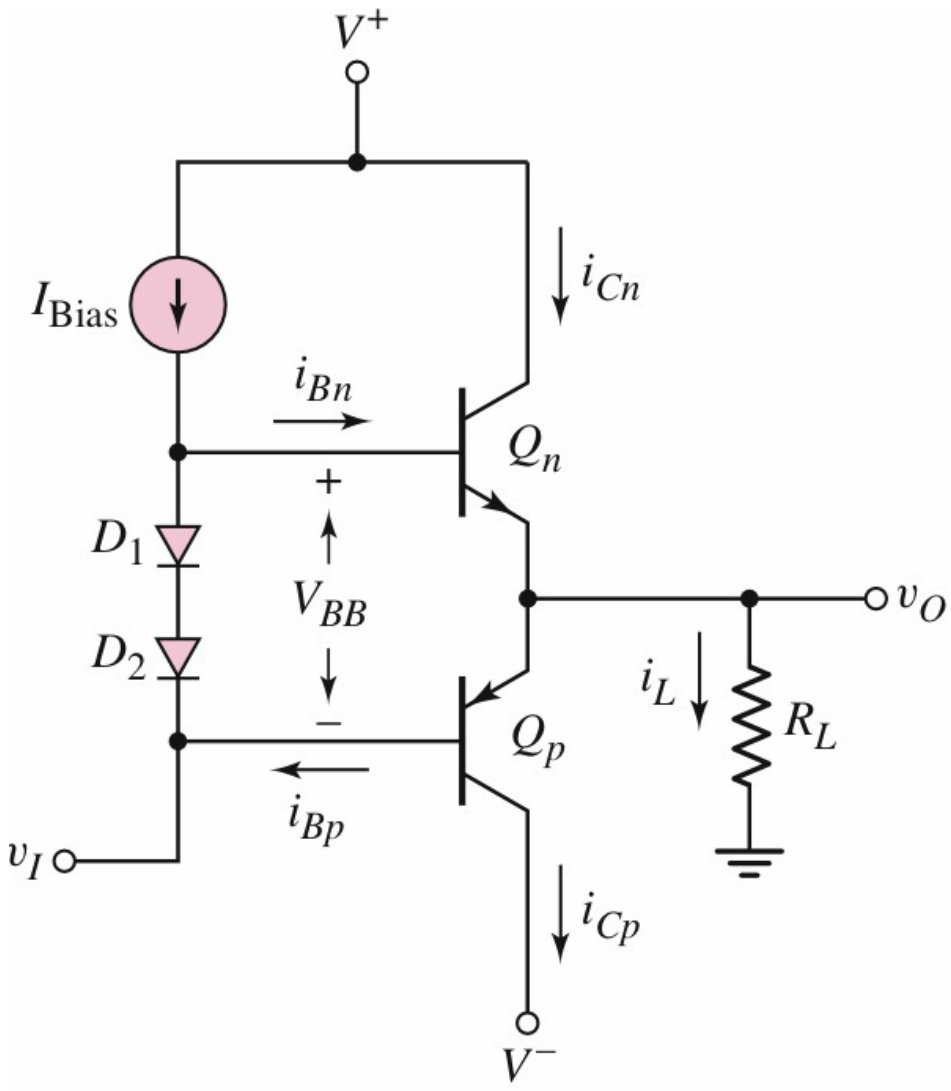
At the positive peak of the output voltage;

$$i_{En(\text{peak})} \cong i_{L(\text{max})} = \frac{V_{o(\text{peak})}}{R_L}$$

$$= \frac{8.94}{8} = 1.12 \text{ A}$$

$$i_{Bn(\text{peak})} = \frac{i_{En(\text{peak})}}{1+\beta}$$

$$= \frac{1.12}{76} = 14.7 \text{ mA}$$



In-class problem 1, solution

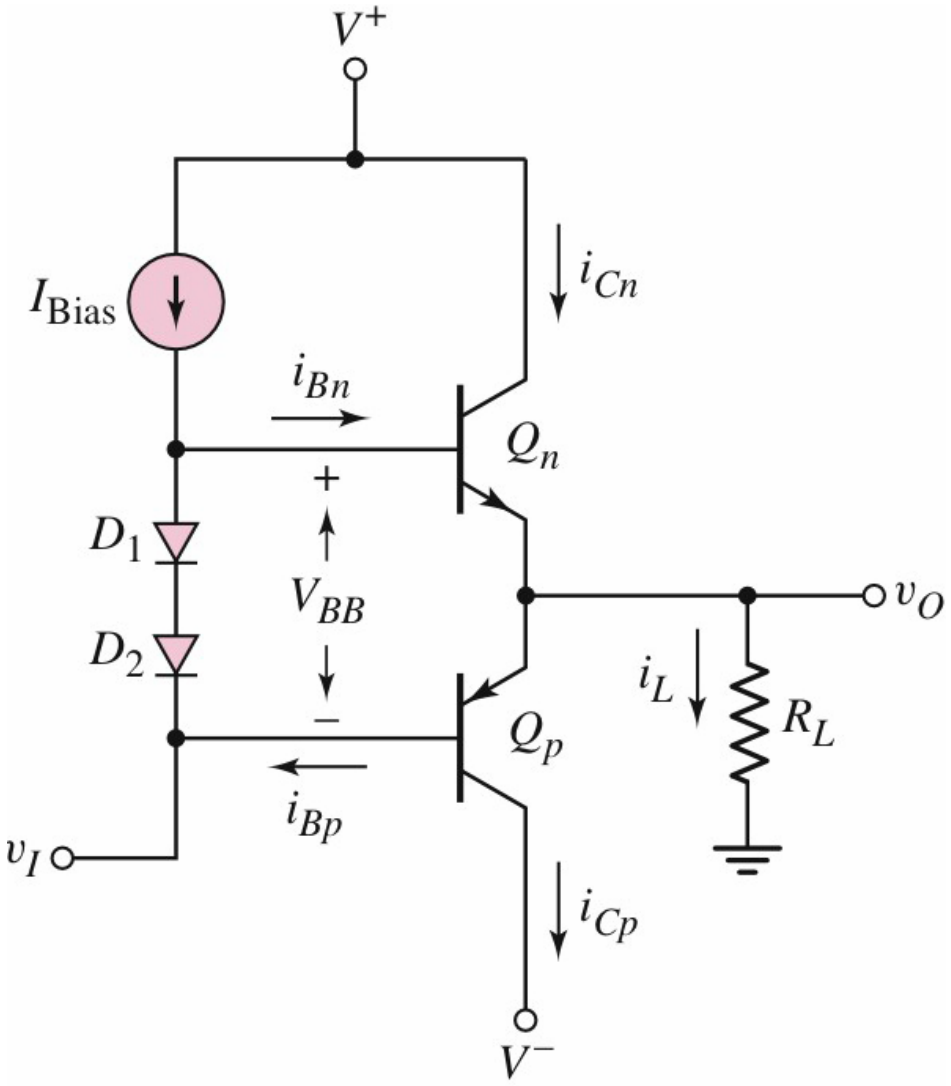
To maintain a minimum of 5 mA through the diodes;

$$I_{\text{Bias}} = i_{Bn} + I_D$$

$$= 14.7 + 5$$

$$= 19.7 \text{ mA}$$

Select I_{Bias} = 20 mA



In-class problem 1, solution

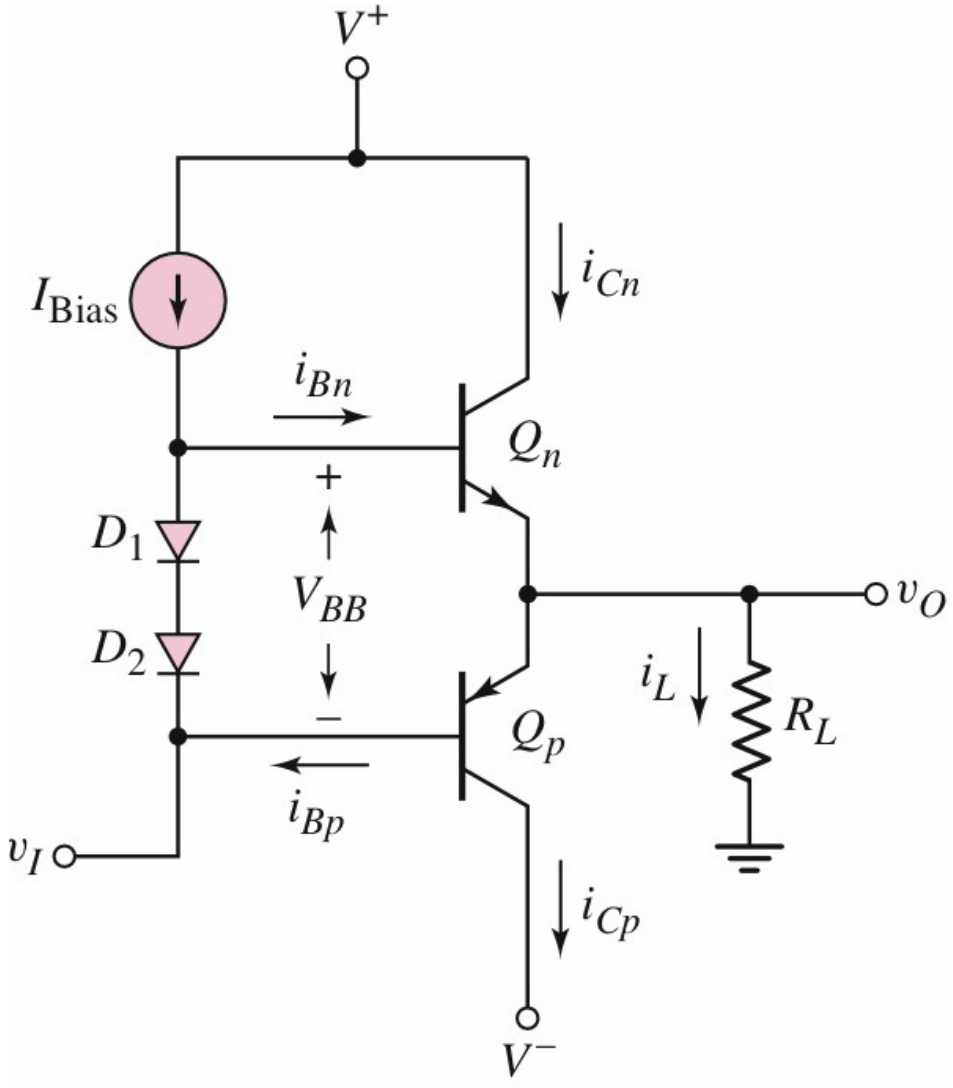
b) $I_{CQ} = I_{SQ} e^{V_{BB}/2V_T}$

Under quiescent condition ($v_I = 0$), $I_D = 20$ mA (neglecting i_{Bn});

$$V_{BB} = 2V_T \ln\left(\frac{I_D}{I_{SD}}\right)$$

$$= 2 \times 0.026 \ln\left(\frac{20 \times 10^{-3}}{3 \times 10^{-14}}\right)$$

$$= 1.416 \text{ V}$$



In-class problem 1, solution

Assuming Q_n and Q_p are matched transistors;

$$V_{BEn} = V_{BEp}$$

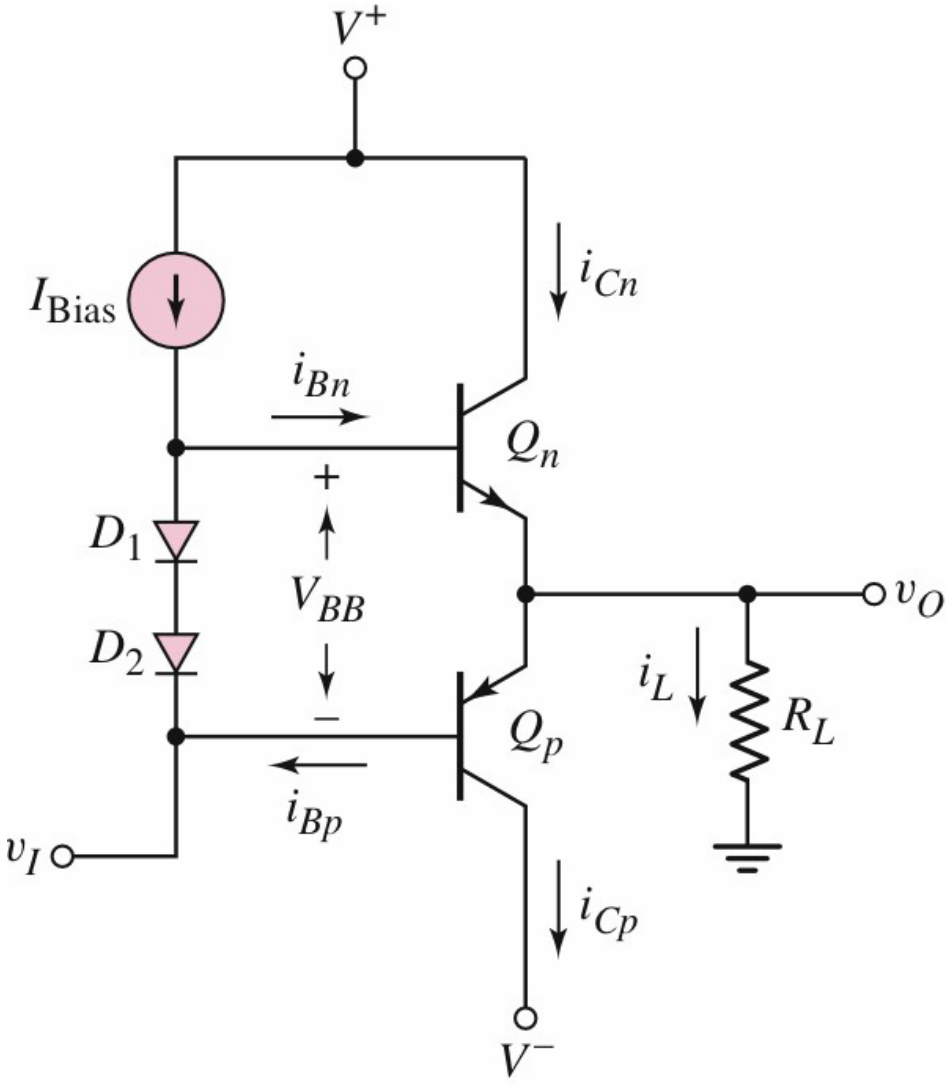
$$= \frac{V_{BB}}{2} = 0.708\ \text{V}$$

Hence;

$$I_{CQ} = I_{SQ} e^{V_{BB}/2V_T}$$

$$= 10^{-13} e^{0.708/0.026}$$

$$I_{CQ} = 67\ \text{mA}$$



In-class problem 1, solution

c) At the peak positive value of output voltage;

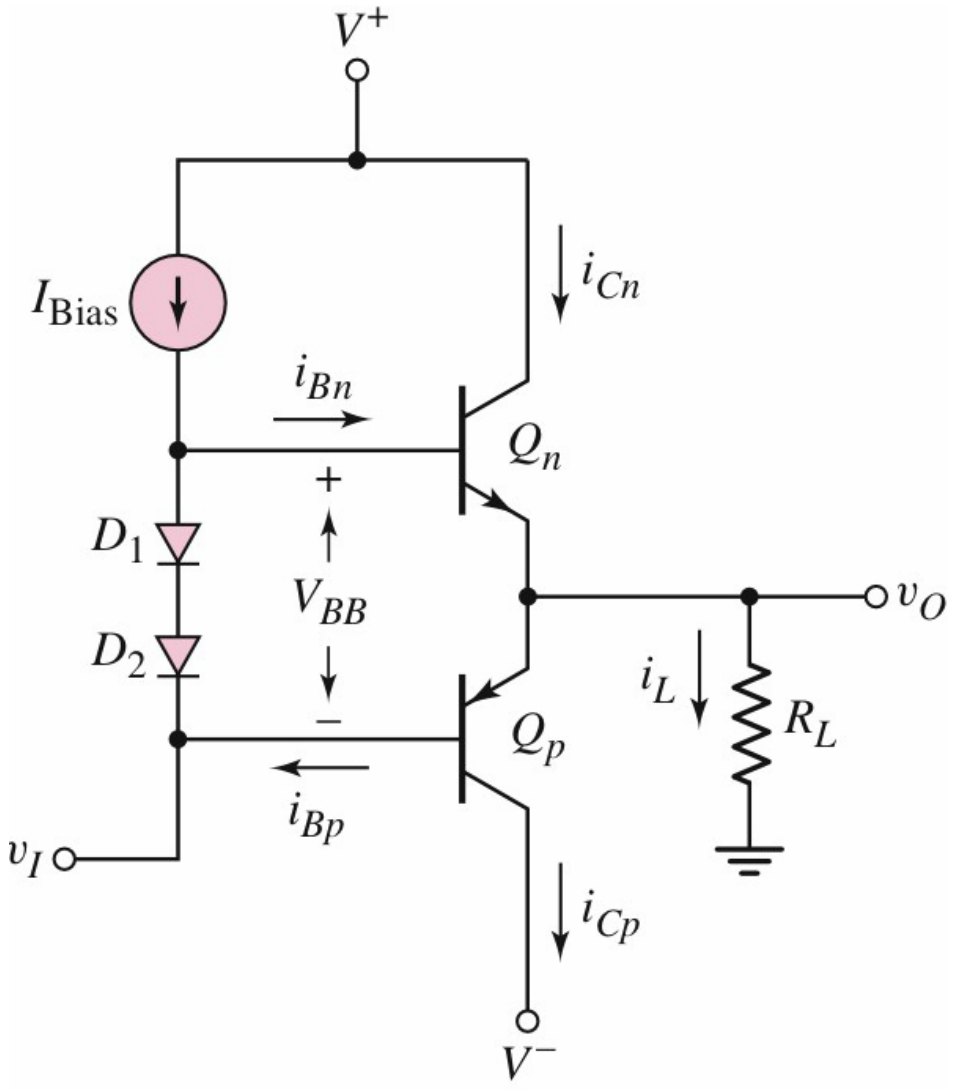
$$i_{En(\max)} \cong i_{L(\text{peak})}$$

$$= 1.12\ \text{mA}$$

$$i_{Bn(\max)} = 14.7\ \text{mA}$$

$$I_D = I_{\text{Bias}} - i_{Bn(\max)}$$

$$= 20 - 14.7 = 5.3\ \text{mA}$$



In-class problem 1, solution

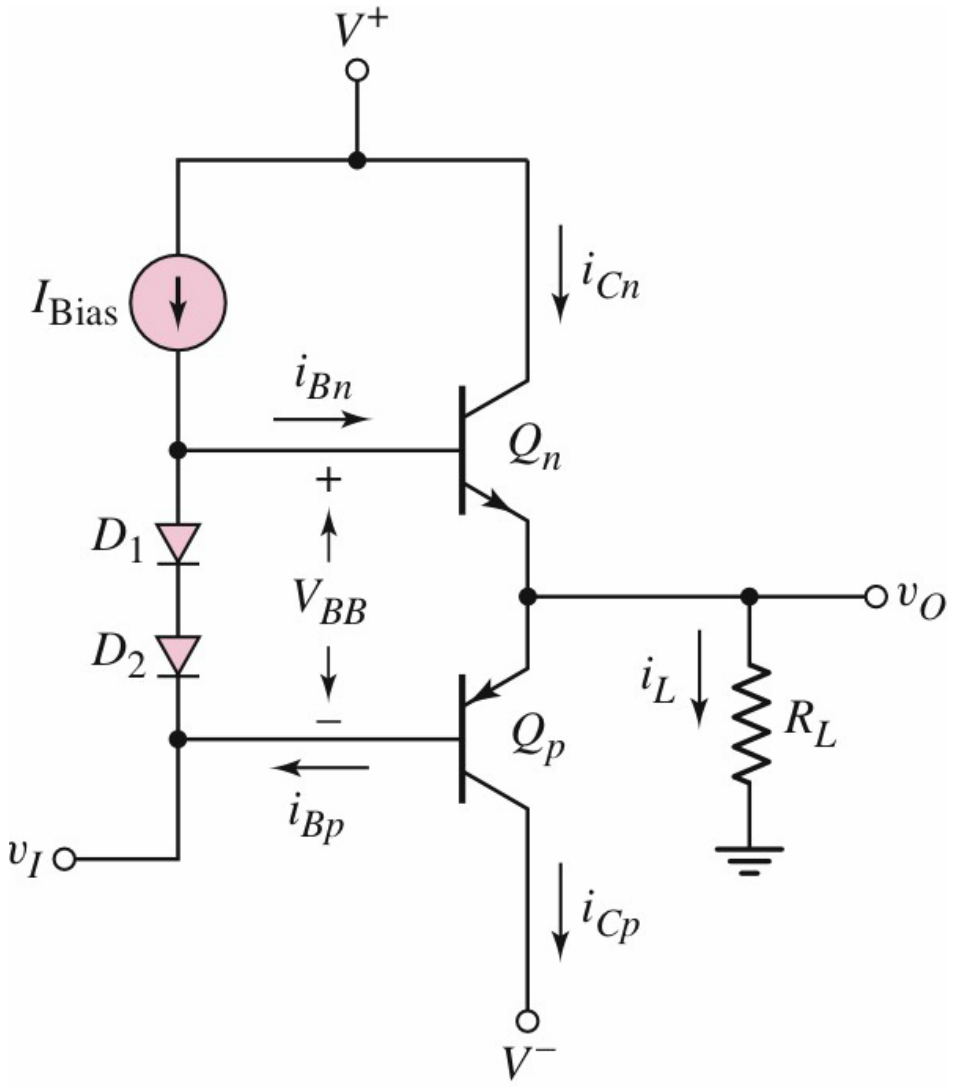
$$V_{BB} = 2 \times 0.026 \ln\left(\frac{5.3 \times 10^{-3}}{3 \times 10^{-14}}\right)$$

$$= 1.347 \text{ V}$$

$$i_{Cn(\max)} = \frac{\beta}{1+\beta} i_{En(\max)}$$

$$= \frac{75}{1+75} \times 1.12$$

$$= 1.105 \text{ A}$$



In-class problem 1, solution

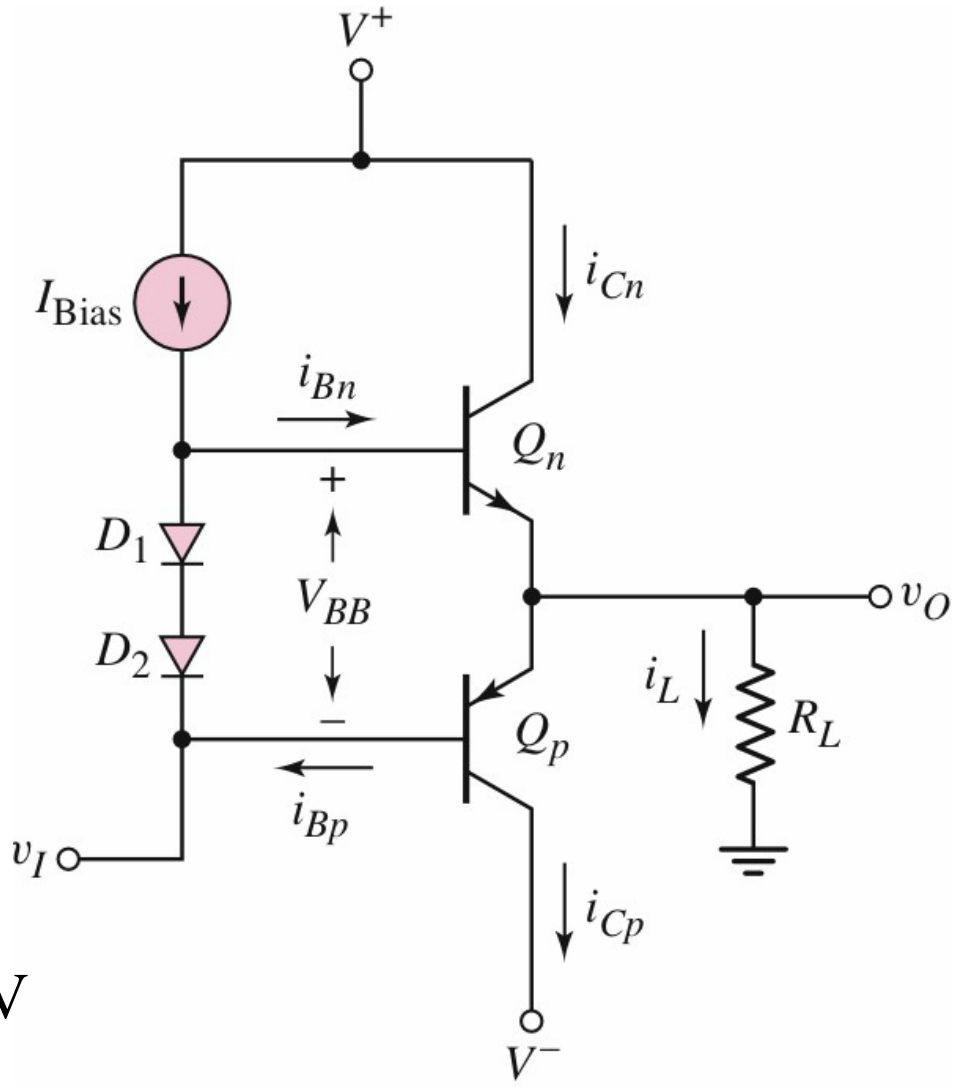
$$V_{BEn} = V_T \ln\left(\frac{i_{Cn}(\max)}{I_{SQ}}\right)$$

$$= 26\ln\left(\frac{1.105}{10^{-13}}\right)$$

$$= 781\,\text{mV}$$

$$V_{BEp} = V_{BB} - V_{BEn}$$

$$= 1.347 - 0.781 = 0.566\,\text{V}$$



In-class problem 1, solution

$$i_{Cp} = I_{SQ} e^{V_{BEp}/V_T}$$

$$= 10^{-13} e^{0.566/0.026}$$

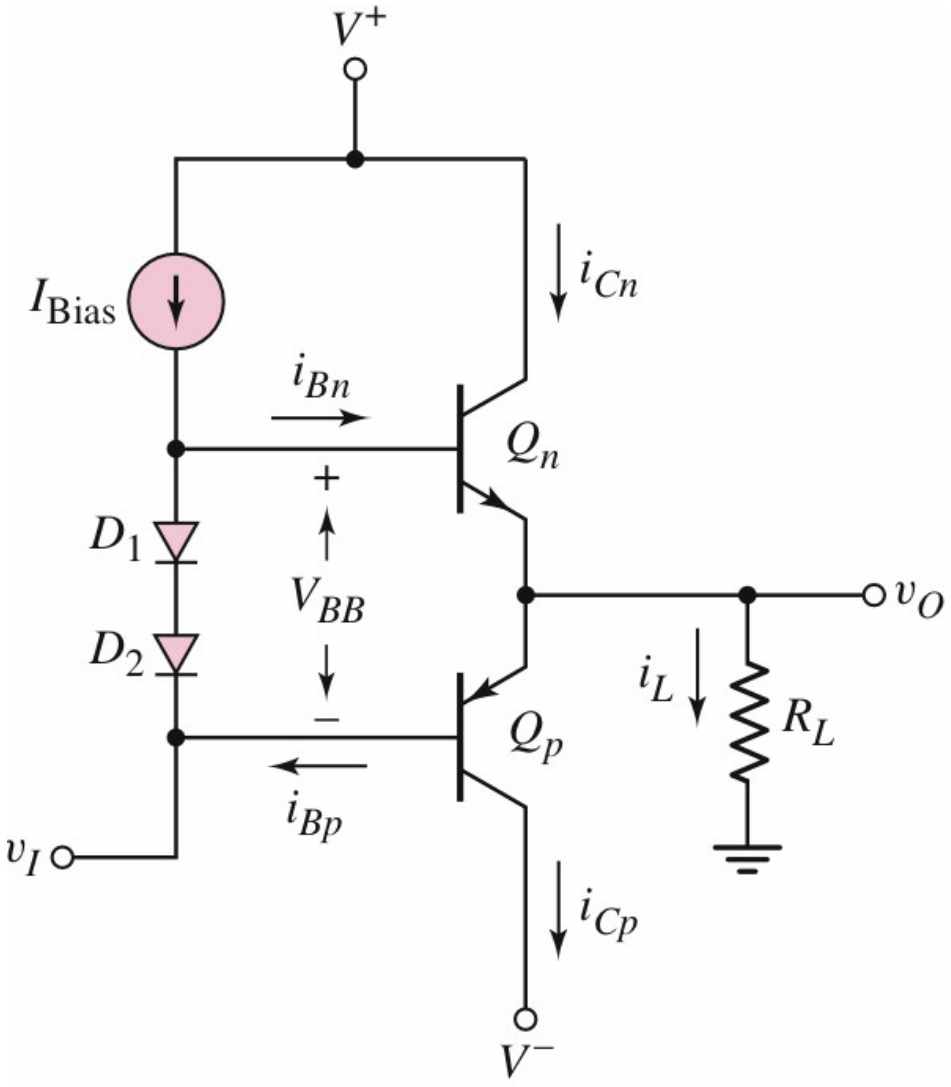
$$= 0.285\,\text{mA}$$

Hence, when the output voltage is at its peak positive value;

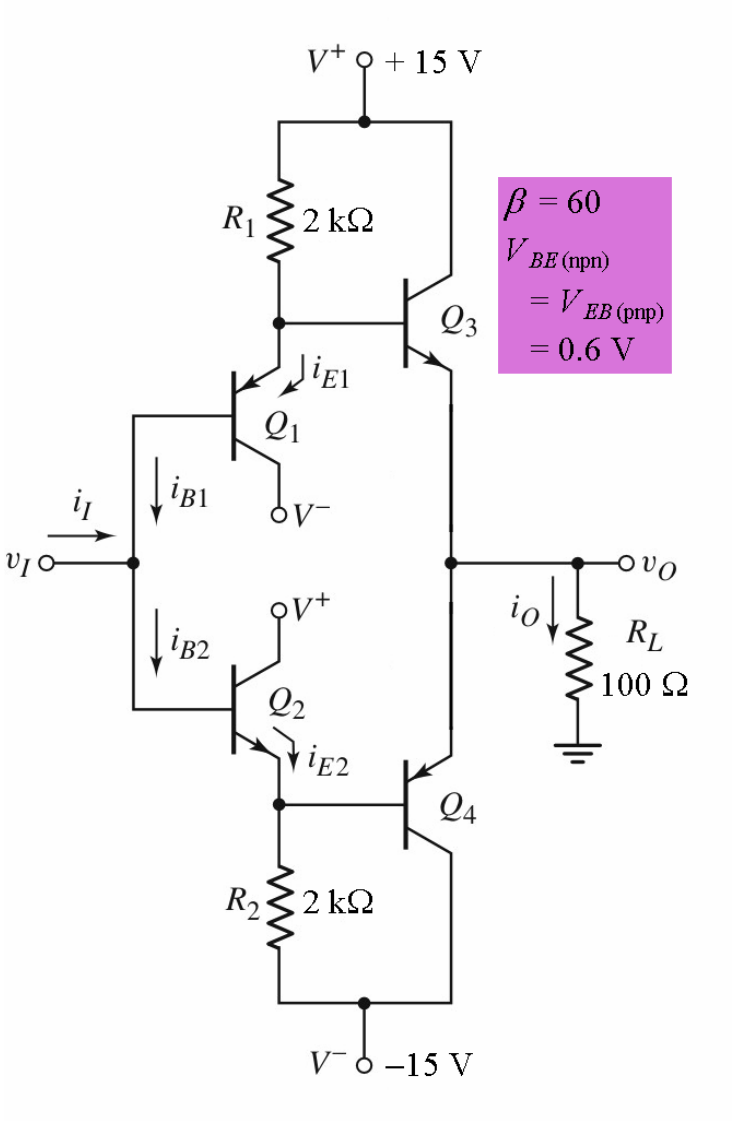
$$i_{Cn} = 1.105\ \text{A}$$

and;

$$i_{Cp} = 0.285\,\text{mA}$$



Take-home problem 1



(a) Determine the quiescent bias currents in all transistors;

(b) Calculate all the currents labeled in the figure and the current gain when v_I = 10 V.

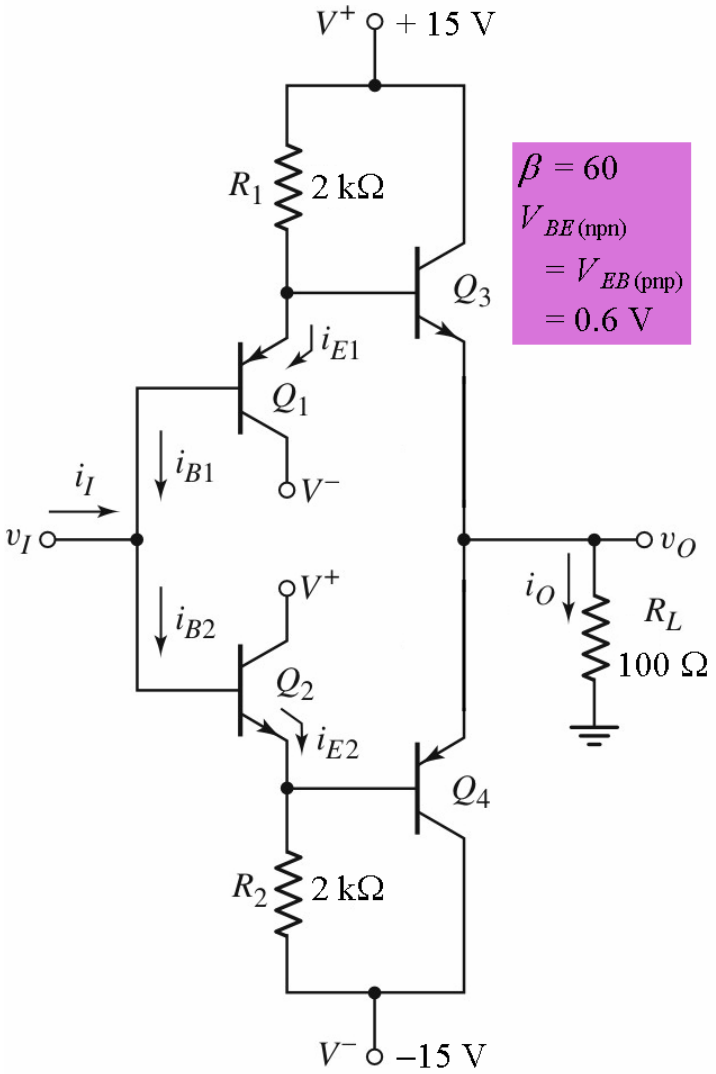
Take-home problem 1, solution

(a) For $v_I = 0$ (quiescent currents);

$$i_{R1} = i_{R2} \cong i_{E1} = i_{E2}$$

$$= \frac{15 - 0.6}{2} = 7.2\ \text{mA}$$

Assuming all transistors are matched, the bias currents in Q_3 and Q_4 are also approximately 7.2 mA since the base-emitter voltages of Q_1 and Q_3 are equal and those of Q_2 and Q_4 are equal.



Take-home problem 1, solution

(b) For $v_I = 10$;

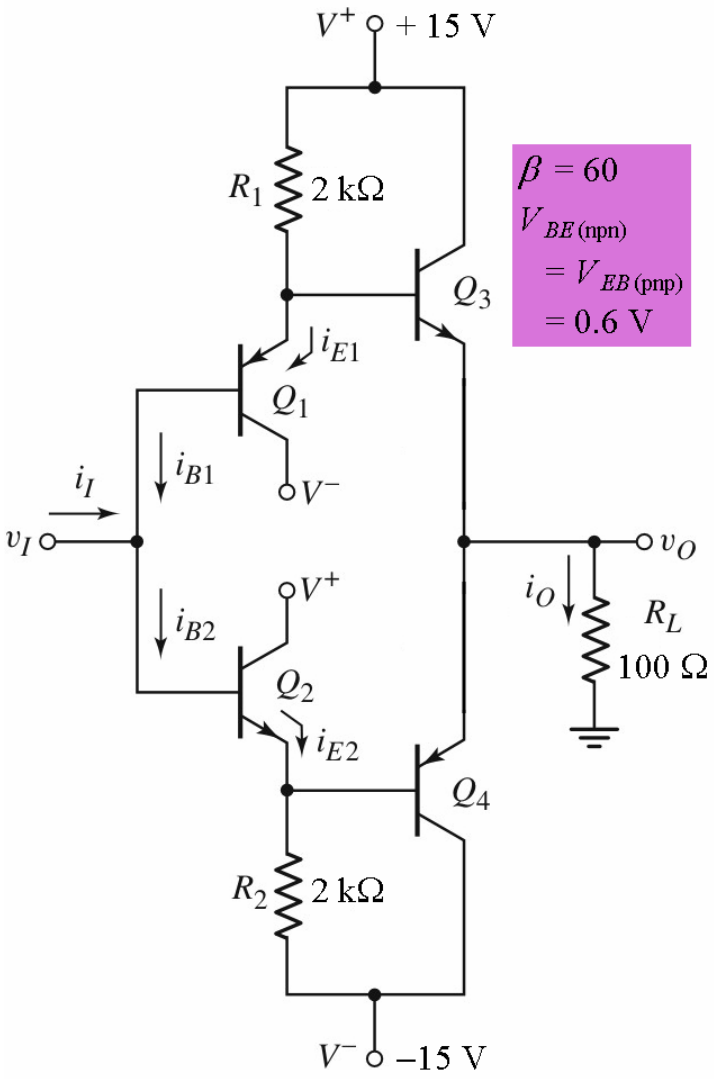
Because the voltage gain is approx. unity;

$$i_O = \frac{v_O}{R_L} \cong \frac{v_I}{R_L}$$

$$= \frac{10}{100} = 100\,\text{mA}$$

$$i_{E3} \cong i_O = 100\,\text{mA}$$

$$i_{B3} = \frac{i_{E3}}{1+\beta} = \frac{100}{61} = 1.64\,\text{mA}$$



Take-home problem 1, solution

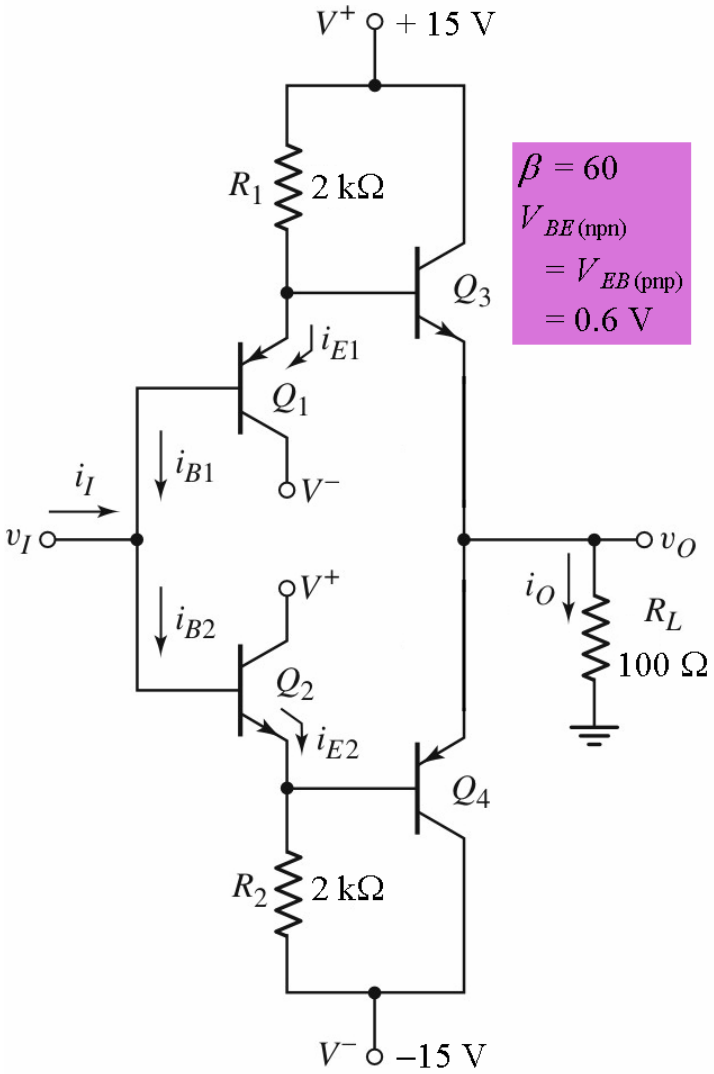
$$i_{R1} = \frac{V^+ - (V_{BE} + v_I)}{R_1}$$

$$= \frac{15 - (0.6 + 10)}{2} = 2.2\ \text{mA}$$

$$i_{E1} = i_{R1} - i_{B3}$$

$$= 2.2 - 1.64 = 0.56\ \text{mA}$$

$$i_{B1} = \frac{i_{E1}}{1 + \beta} = \frac{0.56}{61} = 9.18\ \mu\text{A}$$



Take-home problem 1, solution

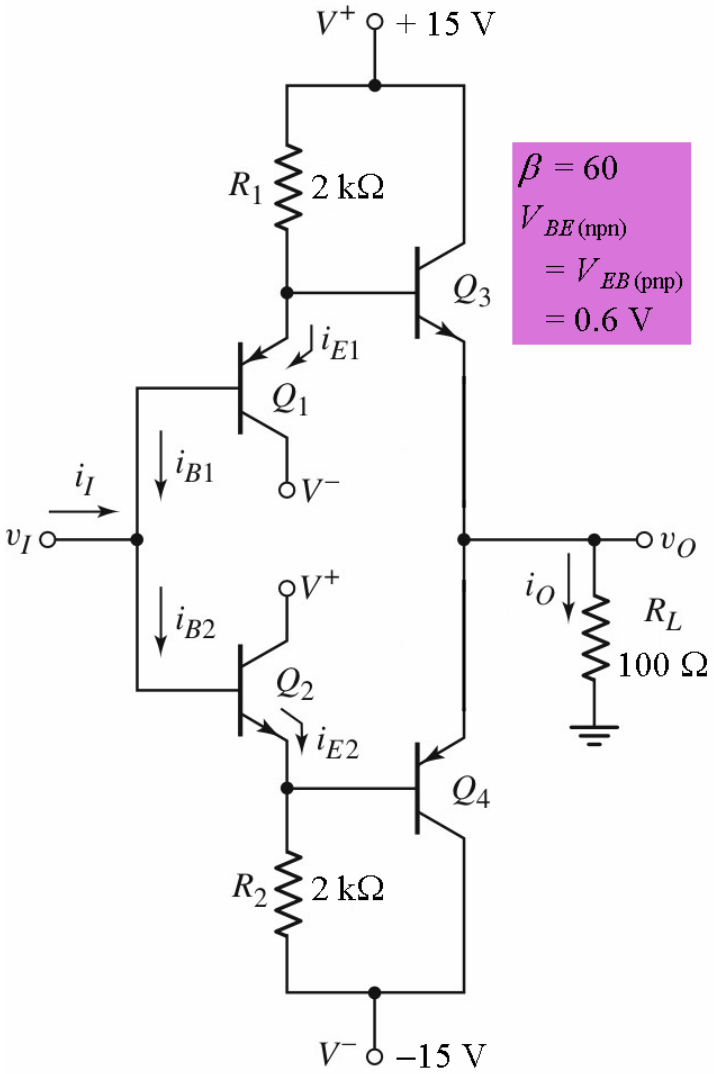
Since Q_4 tends to turn off when v_I increases, i_{B4} is negligible. Therefore;

$$i_{E2} \cong i_{R2} = \frac{v_I - v_{EB} - V^-}{R_2}$$

$$= \frac{10 - 0.6 - (-15)}{2}$$

$$= 12.2\,\text{mA}$$

$$i_{B2} = \frac{i_{E2}}{1+\beta} = \frac{12.2\,\text{mA}}{61} = 200\,\mu\text{A}$$



Take-home problem 1, solution

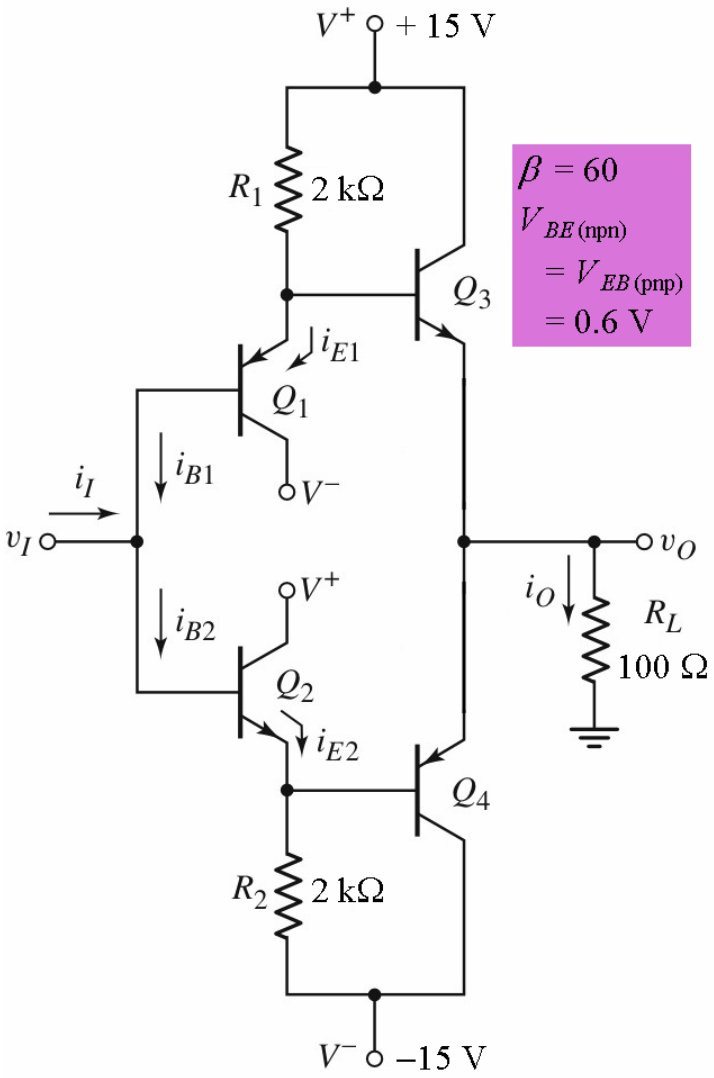
The input current;

$$i_I = i_{B2} - i_{B1}$$

$$= 200 - 9.18 \cong 191\,\mu\text{A}$$

The current gain;

$$A_i = \frac{i_O}{i_I} = \frac{100}{0.191} = 524$$



Take-home problem 1, solution

If the previous expression i.e. $A_i = \frac{(1+\beta)R}{2R_L}$ is used, we have;

$$A_i = \frac{(1+60)(2)}{2\times 0.1} = 610$$

The higher gain is due the fact that the base currents of Q_3 and Q_4 are neglected in deriving the expression.