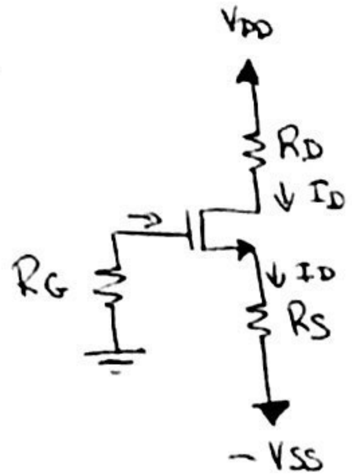

$I_D = 0.5\,mA$ $V_D = 2\,V$

$V_{DD} = V_{SS} = 5\,V$ $\lambda = 0$

$V_{TN} = 1\,V$ $k_n' \frac{W}{L} = 1\,mA/V^2$

Designing the circuit to obtain the required values of I_D and V_D is equivalent to selecting appropriate values of RG, RS, and RD

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5-2}{0.5m} = 6\,k\Omega$$

Using 5% resistor values. $R_D = 6.2\,k\Omega$

Assuming that the FET is in saturation:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{TN})^2 =$$

$$0.5m = \frac{1}{2} \cdot 1m\,(V_G - V_{TN})^2 \Rightarrow (V_{GS} - V_{TN}) = \pm 1$$

2 V

0 V (cut-off ⇒ NOT ACCEPTABLE VALUE)

$$V_{GS} = 2V \Rightarrow V_S = V_G - V_{GS} = 0 - 2V = -2V$$

$$R_S = \frac{V_S + V_{SS}}{I_D} = \frac{-2+5}{0.5m} = 6\,k\Omega$$

$R_S = 6\,k\Omega$ using the 5% resistor values: $R_S = 6.2\,k\Omega$

RG can be selected in the few M-Ω range to ensure that the circuits has a large input impedance.

$R_G = 5.1\,M\Omega$

At this point we need to back-track to calculate I_D, V_G, V_{DS} and V_{GS}. We do that for 2 reasons: 1) Verify that by using 5% resistor values the actual values of I_D and V_D don't significantly differ from the required values;

) Verify the assumption that the FET operates in saturation.

$$I_D = \frac{V_{SS} - V_{GS}}{R_S} \Rightarrow V_{GS} = -V_S = 5 - R_S I_D$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - 1)^2 = \frac{1}{2} \cdot 1m \cdot (V_{GS} - 1)^2$$

$$2 I_D = (4 - 6.2 I_D)^2 \Rightarrow 38.44 I_D^2 - 51.61 I_D + 16 = 0$$

$$I_{D_1} = 0.48 mA \quad I_{D_2} = 0.86 mA$$

I_{D1} is the closest to the required I_D value (i.e., 0.5 mA)

Also $I_D = 0.86 mA$ yields $V_{GS} < 0$ which is not acceptable.

$$I_D = 0.48 mA$$

$$V_S = -5 + 6.2 \cdot 0.48 = -1.86 V \qquad V_{GS} = 1.86 V \Rightarrow V_{GS} - V_{TN} = 0.86 V$$

$$V_D = 5 - 6.2 \cdot 0.48 = 1.86 V \qquad V_{DS} = 3.72 V$$

CLOSE TO THE REQUIRED VALUE.

$V_{DS} > V_{GS} - V_{TN}$ THE SATURATION ASSUMPTION IS VERIFIED

R_G can be selected to be 1 MΩ