ECE 371
Materials and Devices

11/21/19 - Lecture 23

Ch. 10 – MOS Capacitor

General Information

- Homework 8 assigned today, due on Wednesday 12/5
- Homework 7 due today before class
- Reading for next time: 10.1

MOSFET

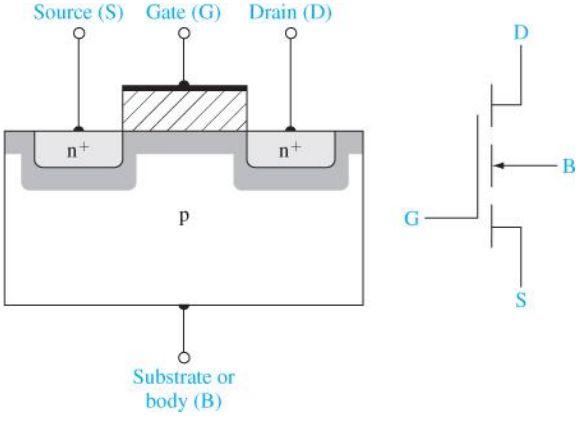

Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

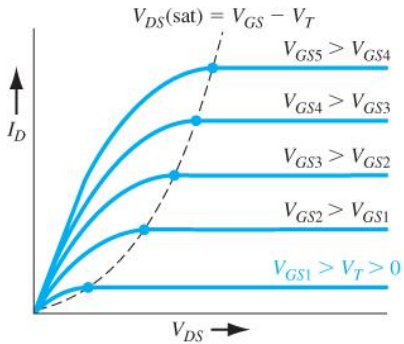

Figure 10.40 | Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET.

- Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
- Figure shows n-channel enhancement-mode FET
- Enhancement mode and depletion mode devices
- nMOS and pMOS devices
- Complimentary Metal Oxide Semiconductor (CMOS) combines nMOS and pMOS
- Circuits with current/voltage/power gain
- Logic functions

MOS Capacitor/p-Type with Negative Bias

apply voltage → acts like parallel plate cap.

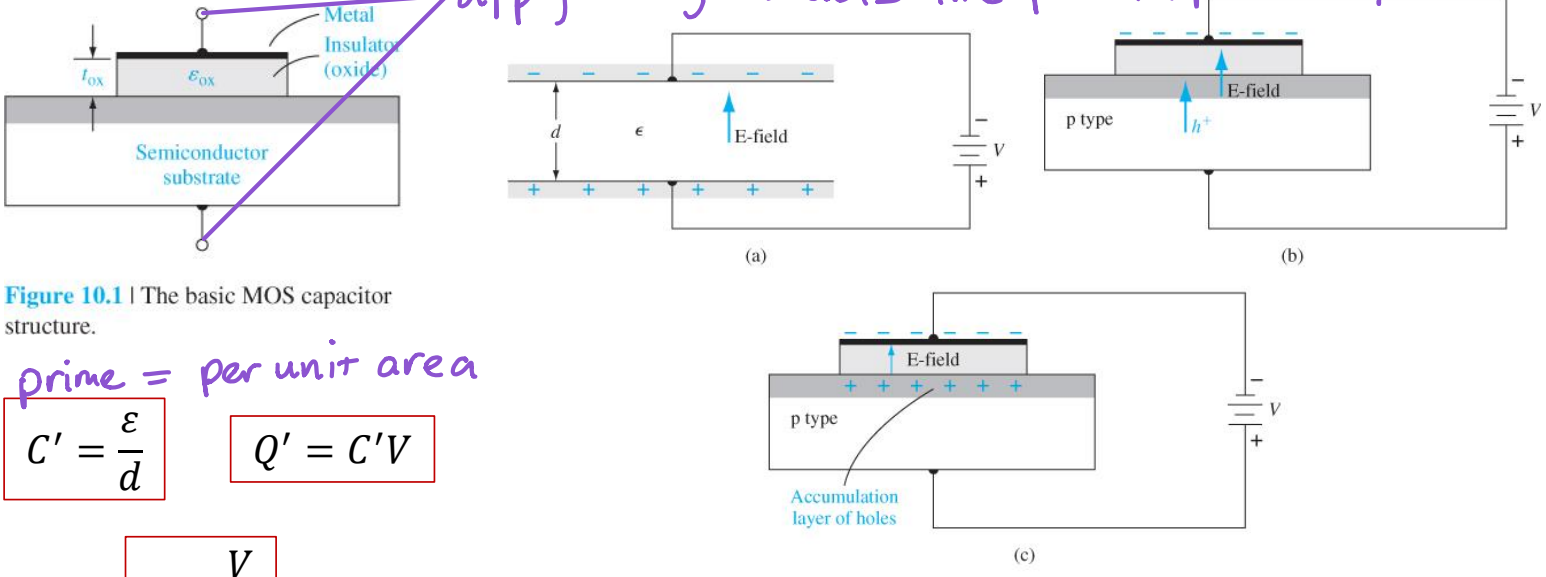

Figure 10.1 | The basic MOS capacitor structure.

Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges. (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

prime = per unit area

$$C' = \frac{\varepsilon}{d}$$

$$Q' = C'V$$

$$E = \frac{V}{d}$$

- Top metal gate is at a negative voltage with respect to the substrate
- Electric field forces holes to the oxide-semiconductor interface
- Accumulation of holes forms near the interface

p-Type with Positive Bias

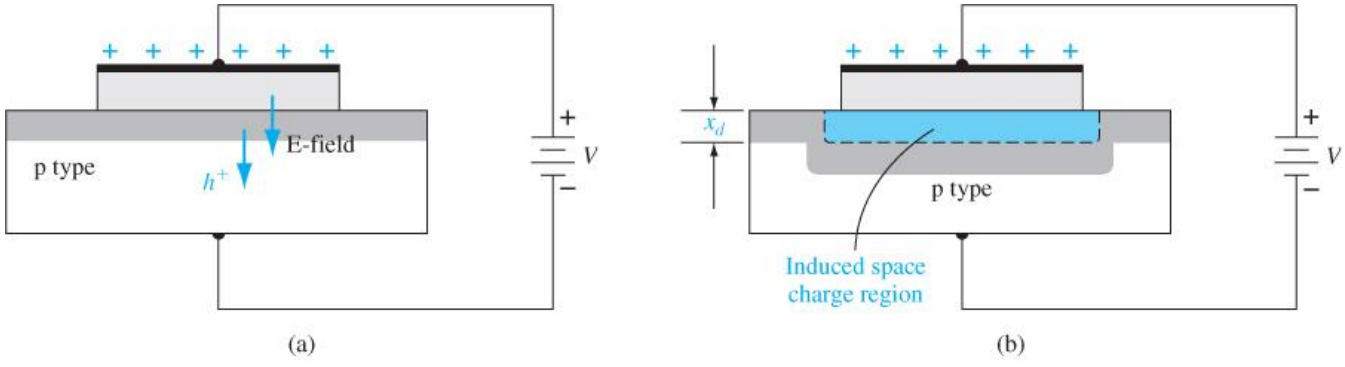

Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

- Top metal gate is at a positive voltage with respect to the substrate
- Electric field forces holes away from the oxide-semiconductor interface
- Negative space-charge region forms near the interface (depletion of holes)

MOS Capacitor: p-type Band Diagrams

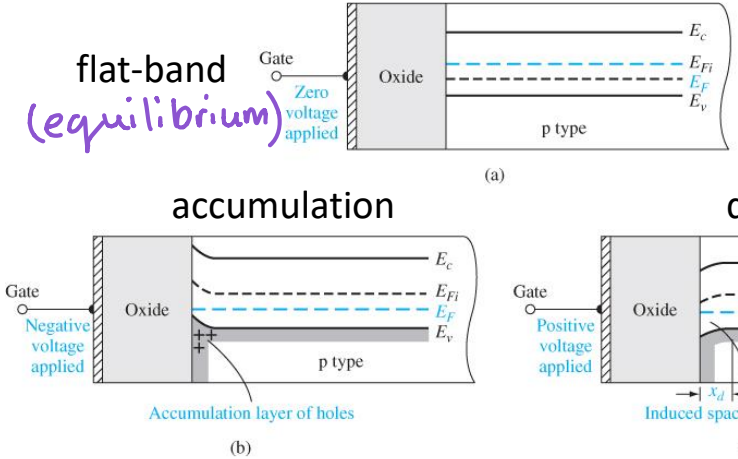

Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case, (b) a negative gate bias, and (c) a moderate positive gate bias.

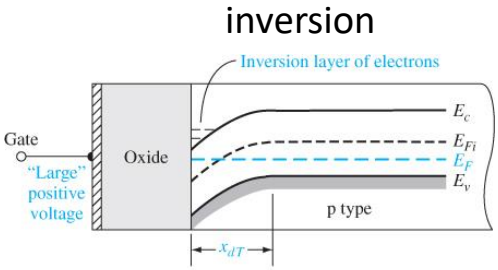

Figure 10.5 | The energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.

- Zero bias is the "flat band" condition
- Negative bias causes ***accumulation*** of holes near the surface since E_v-E_F is smaller near the surface. Surface appears more "p-type."
- Positive bias causes ***depletion*** of holes near the surface. A space-charge region forms where holes are depleted and ionized acceptors remain. E_v-E_F is larger near the surface.
- Larger positive bias causes a higher E-field, more band bending, and a larger depletion width. E_F-E_{Fi} > 0 near the surface, which means surface is "n-type." An ***inversion*** layer of electrons forms.
- Devices are in thermal equilibrium (e.g. $-\frac{dE_F}{dx} = 0$) since no current can flow

MOS Capacitor: n-Type Substrate

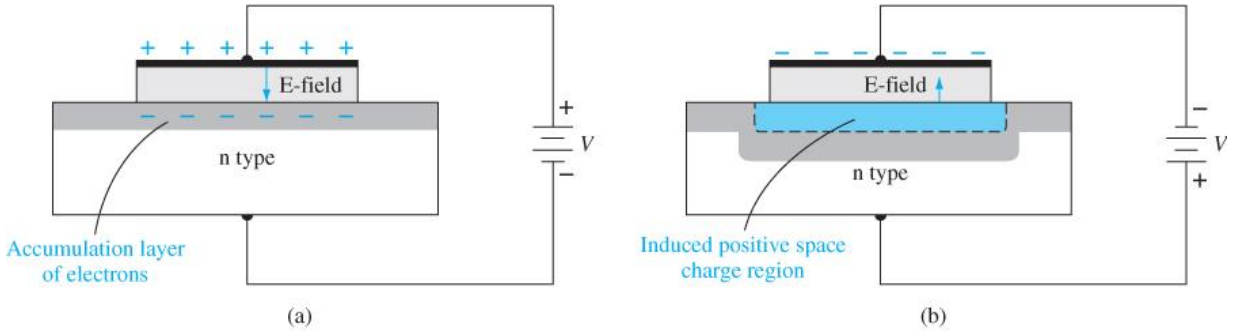

Figure 10.6 | The MOS capacitor with an n-type substrate for (a) a positive gate bias and (b) a moderate negative gate bias.

- Positive voltage causes accumulation of electrons near the surface
- Negative voltage causes depletion of electrons near the surface

Notes on biasing & band bending

- electron $E = -e\phi$ → higher voltage = lower energy
- hole $E = +e\phi$ → higher voltage = higher energy

MOS Capacitor: n-Type Band Diagrams

accumulation

depletion

inversion

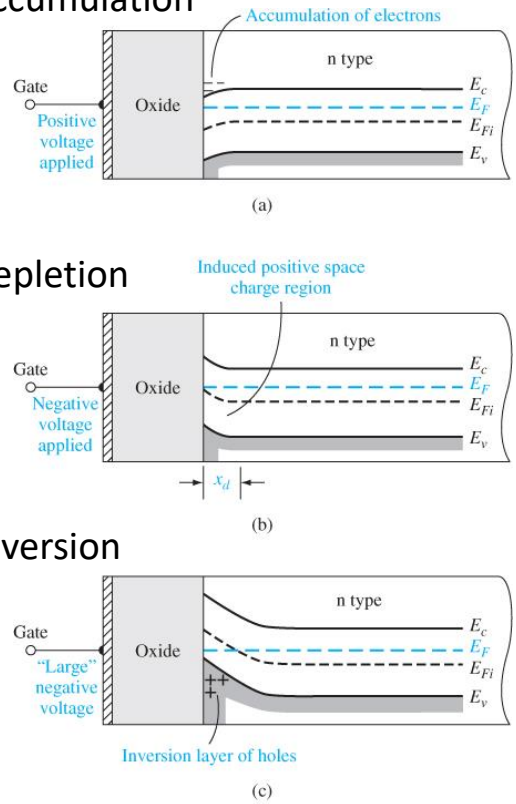

Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias, (b) a moderate negative bias, and (c) a "large" negative gate bias.

- Positive bias causes ***accumulation*** of electrons near the surface since E_c-E_F is smaller near the surface. Surface appears more "n-type."
- Negative bias causes ***depletion*** of electrons near the surface. A space-charge region forms where electrons are depleted and ionized donors remain. E_c-E_F is larger near the surface.
- Larger negative bias causes a higher E-field, more band bending, and a larger depletion width. E_{Fi}-E_F > 0 near the surface, which means surface is "p-type." An ***inversion*** layer of holes forms.

Depletion Layer Thickness

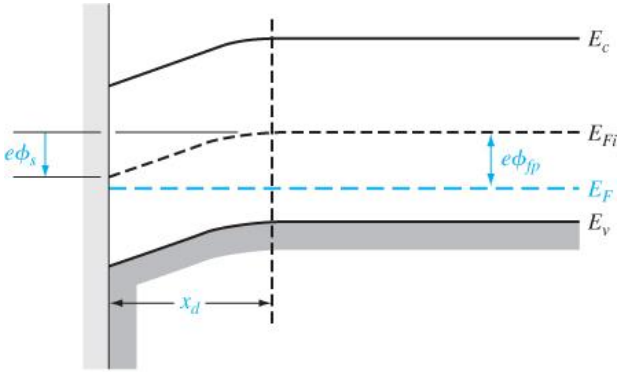

Figure 10.8 | The energy-band diagram in the p-type semiconductor, indicating surface potential.

p-type

$$\phi_{Fp} = \frac{kT}{e} ln\left(\frac{N_a}{n_i}\right)$$

$$x_d = \left(\frac{2\varepsilon_s \phi_s}{eN_a}\right)^{\frac{1}{2}}$$

n-type

$$\phi_{Fn} = \frac{kT}{e} ln\left(\frac{N_d}{n_i}\right)$$

$$x_d = \left(\frac{2\varepsilon_s \phi_s}{eN_d}\right)^{\frac{1}{2}}$$

- What is the width of the space-charge region near the surface?
- ϕ_s is the surface potential (i.e., the potential across the space-charge region)
- ϕ_s can be found with a similar procedure to that used for V_{bi} of a pn-junction. Try it!
- Looks like a one-sided (asymmetric) pn-junction