Take Test: ECE 344L Final Exam Spring 2020

Test Information

Description	This is the online final exam for ECE 344L - Spring 2020
Instructions	There is no time limit to complete the exam other than it must be be submitted by the due date. You have one attempt.
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	This test can be saved and resumed later.

Question Completion Status:

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

QUESTION 1

5 points Saved

Which peripheral on the PIC32MX795F512L could we use if we need to implement an asynchronous, full-duplex serial communication channel

Terminal 3 (12pt)

Click Save and Submit to save and submit. Click Save All Answers to save all answers.

Path: p » span Words:1

QUESTION 2

5 points Saved

The MIPS processor uses a pipelined architecture, which introduces the possibility of data hazards and control hazards. Explain what a data hazard is, give a specific example of where we will encounter a data hazard, and describe what measures you would take when writing your assembly language programs to avoid problems with data hazards

Terminal 3 (12pt)

Data hazards exist when there are data dependencies between nearby instructions. For example:

```
lw $s0, 20($t1)

add $t2, $s0, $t3
```

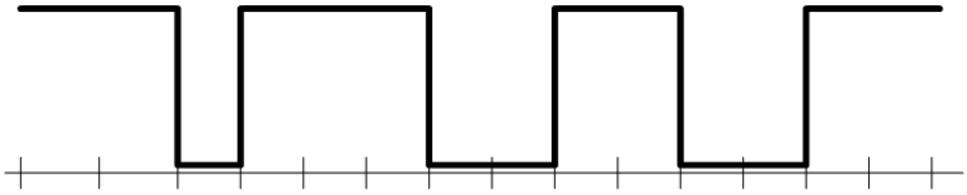
In this example, add is trying to consume data $s0, but lw has not finished producing it. To mitigate this, we would need to stall the pipeline, for example with a nop.

Path: p » span Words:52

QUESTION 3

10 points Saved

You are examining a burst of digital data that has been transmitted by the UART to the RS-232 adapter in order to verify that you have configured the system properly.



Based on this measured signal, which of the following configurations could be correct for this burst of data? (Recall we use a shorthand notation of Data Bits,

Parity, and Number of Stop Bits.)

- [x] A. 9,N,1
- [x] B. 8,N,1
- [ ] C. 8,E,1
- [ ] D. 8,O,1

QUESTION 4

10 points (Extra Credit) Saved

When using interrupts, we must use Interrupt Service Routines (ISRs). There are restrictions on how we can use ISRs. List the restrictions, or constraints, that apply when using ISRs

Terminal 3 (12pt)

1. Need an interrupt source

2. Enable specific interrupt

3. Need an ISR (interrupt service routine)

Path: div.page » div.section » div.layoutArea » div.column » p » span Words:16

QUESTION 5

5 points Saved

Using table 7.2 above specify the address and the 32-bit word (expressed as a hexadecimal values) that must be written to it, in order to enable the interrupt for Timer 1.

TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	SPI1TXIF	SPI1RXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	CAN2IF(2)	CAN1IF	USBIF	FCEIF	DMA7IF(2)	DMA6IF(2)	DMA5IF(2)	DMA4IF(2)	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	SPI1TXIE	SPI1RXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	CAN2IE(2)	CAN1IE	USBIE	FCEIE	DMA7IE(2)	DMA6IE(2)	DMA5IE(2)	DMA4IE(2)	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.
2: This bit is unimplemented on PIC32MX764F128L device.
3: This register does not have associated CLR, SET, and INV registers.

Terminal 3 (12pt)

bit 4 of IEC0 SFR

Address: 0xBF881060

Hex Value: 0x10

Path: p » span Words:11

QUESTION 6

5 points Saved

With a word size of 10 bits, what is the minimum signed integer that we can represent?

Terminal 3 (12pt)

-512

Path: p » span Words:1

QUESTION 7 **5 points** Saved

With a word size of 10 bits, using a two's complement representation, what is the **binary** value that represent the value -10

Terminal 3 (12pt)

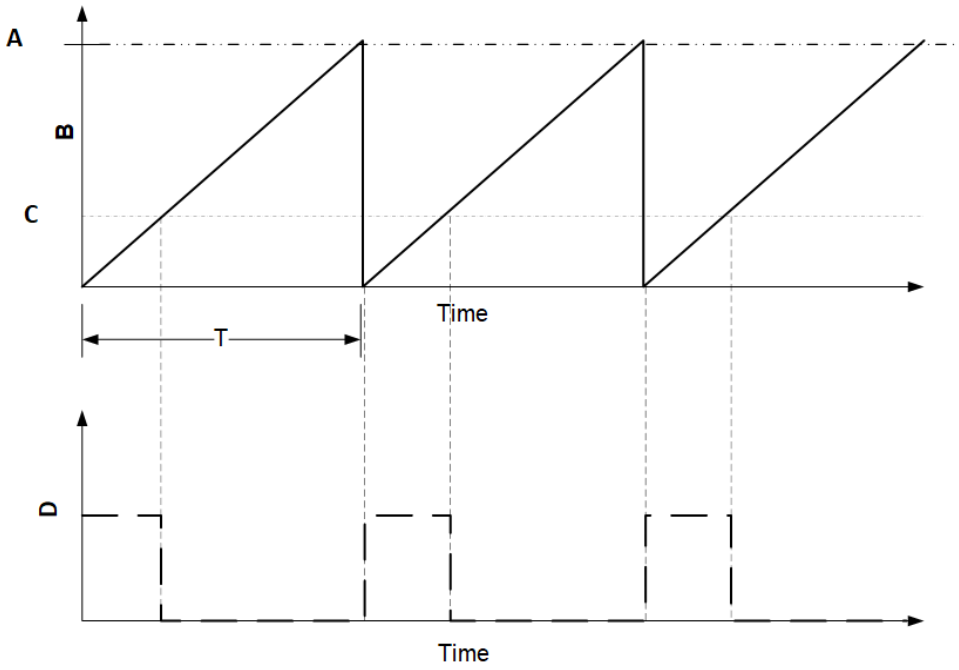
1111110110

Path: p » span Words:1

QUESTION 8 **10 points** Saved

1. A
4. B
2. C
3. D

1. Period Register Value
2. Output Compare x Compare Register
3. Output Compare x Output
4. Timer Register Value



Given the above figure, identify each of the items indicated by the letters:

QUESTION 9

10 points Saved

Given the following list of attributes, fill in which type of architecture class to which each attribute corresponds. For example, complex instructions would correspond to a CISC architecture.

D. Fixed length instructions

C. Separate Instruction and Data Storage and Transmission

B. Many addressing modes

D. Many general purpose registers

B. One to many clock cycles per instruction

D. Load/Store Architecture

A. Co-mingled data and instructions

A. Von Neumann

B. CISC

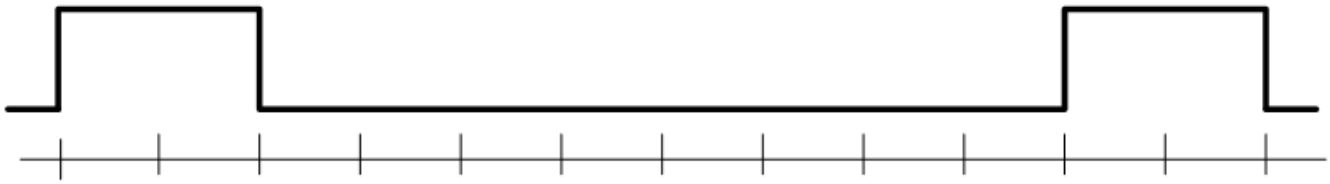
C. Harvard

D. RISC

QUESTION 10

5 points Saved

Given the pulse width modulated (PWM) signal below, calculate the duty cycle of the signal.



Terminal 3 (12pt)

(2/10)*100 = 20% duty cycle

Path: p » span Words:5

QUESTION 11 **10 points** Saved

1.

	Address
0XCD99	0xB000
0xA100	0xB004
0x4888	0xB008
0x6541	0xB00C
$t0 0x722B	0xB010
0x4220	0xB014
0xCA0A	0xB018
0x1BB7	0xB01C
0x2000	0xB020
0x78B0	0xB024

Our MIPS code has the following instruction:

lw $t1, -8($t0)

The $t0 register contains the value 0xB010

A. What value will be written into $t1?

B. Provide the instruction that will write the contents of $t1 to the memory address 0xB020

Terminal 3 (12pt)

A. 0x4888

B. sw $t1, 20($t0)

Path: p » span » span Words:6

QUESTION 12 **5 points** Saved

With a word size of 10 bits, what is the maximum signed integer that we can represent?

Terminal 3 (12pt)

511

Path: p » span Words:1

QUESTION 13 **5 points** Saved

Explain the difference(s) between a servo motor and a stepper motor.

Terminal 3 (12pt)

Servo Motors – range of motion is limited

Stepper Motors – full 360° range of motion – moves in step increments

Unlike servo motors, most steppers do not have integral feedback for position.

Path: p » span Words:30

QUESTION 14

10 points Saved

TABLE 12-1: PORTA REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
6010	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6020	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6030	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

The LAT register is the register used to write data to the port I/O pins. Assume we have configured all of the Port A pins as outputs, and each is pin is currently set to a desired value. Now, we need to clear bit 6 while not affecting any of the other bits. What is the hexadecimal value and the address that we must write it to, in order to clear the specific bit while not affecting any of the other bits?

Terminal 3 (12pt)

Address: 0xBF886024

Hex Value: 0x40

Path: p » span Words:5

QUESTION 15

5 points Saved

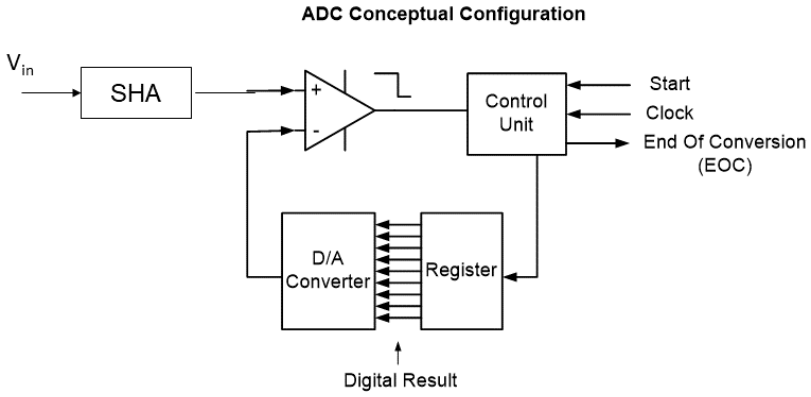
The micro-controller you are using has an **8-bit** Analog to Digital Converter. In your use, $+V_{ref}$ is set at 3.3 Volts and $-V_{ref}$ is set at ground (0. Volts). What is the resolution of the digital estimate of the unknown analog input signal, or put another way, what is the weight of the least significant bit of the digital result

- (•) 12.9mV
- ( ) 3.3V
- ( ) 3.3mV
- ( ) 3.22mV
- ( ) 412.5mV

QUESTION 16

5 points Saved

The conceptual block diagram for the PIC32 successive approximation Analog to Digital Converter (ADC) is shown below. We use a Sample and Hold Amplifier (SHA) when sampling analog signals. Explain what an SHA does and why it is needed.



For the toolbar, press ALT+F10 (PC) or ALT+FN+F10 (Mac).

Terminal 3 (12pt)

Because the input voltage of our analog signal will vary during the time we're doing our conversion process, we need to keep a constant sample steady to which we can to compare our known reference. This is the role of the Sample and Hold Amplifier.

Path: p » span Words:45