Lecture 21 Quiz

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1. **Describe the performance differences between i486 and the SPARC and R3000 architectures. What benchmarks were used to compare the machines? How did the i486 compare against these other two RISC machines?**

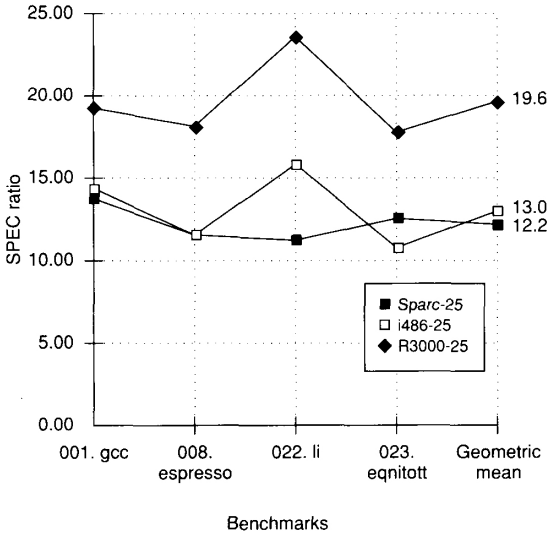
   The i486 was an improvement on the i386 by having a one-cycle-per-instruction throughput which reduced the load delay. SPARC supported branch delay allowing for jumps to execute in one cycle, whereas the x86 series had no concept of branch delay, it wasn't built into the ISA. This was one of the reasons that the x86 series suffered so badly on jump instructions.

   The benchmarks used to compare the machines were Dhrystone benchmark and SPEC benchmark. Dhrystone, while better than simply using instruction counts to compare, was still susceptible to compiler optimizations and wasn't representative of real application code.

   As shown in the figures below (taken from the i486 manual), the i486 showed significant improvement in load word and store word instructions, but was hindered in jump (especially jump-taken) instructions when compared to the other two RISC machines. The i486 was sandwiched between the SPARC (worse) and the R3000 (better) in terms of benchmark scores.

Table 3.
Clock cycle counts for basic instructions.

Instruction type	Counts 386	486	Sparc	88100
Load	4	1	2	1-3
Store	2	1	3	1
ALU	2	1	1	1
Jump taken/	9	3	1	2
not taken	3	1	2	1
Call	9	3	3	1



2. **What technique did the R4000 use to improve performance over the R3000? How well did it do?**

Most of the extra pipelining that was done in the R4000 was to speed up the caching. It did that by splitting the fetch and the memory stages (the critical path) into two stages each. The memory stage also gained a cache stage. This brought the entire pipeline up to eight total stages.

This superpipelining resulted in a SPEC ratio of 63 for the R4000 versus about 20 for the R3000, somewhere between 2-3 times speedup.

3. **What technique did the Pentium use to improve performance over the i486? How well did it do?**

   The Pentium is 8-micron technology (same as the R4000) and essentially smashed two i486 pipelines together. The Pentium also implemented superscalar pipelining which fetched more instructions per cycle.

   The i486 used a unified cache while the Pentium used split caches for the instructions and the data.

   The SPEC ratio on the i486 was about 20 (at 33MHz) while the Pentium achieved 60 at 66MHz, comparable to the R4000 and three times speedup over the i486.

4. **What structure does an out-of-order machine employ to maintain precise exceptions?**

   The instruction fetch and decode unit uses Reservation Stations to buffer everything into Functional Units which then execute the instructions out of order to speed things along. These executed instructions are then put back into order by a reorder buffer before they are allowed to commit to memory.