Using the PIC Ports

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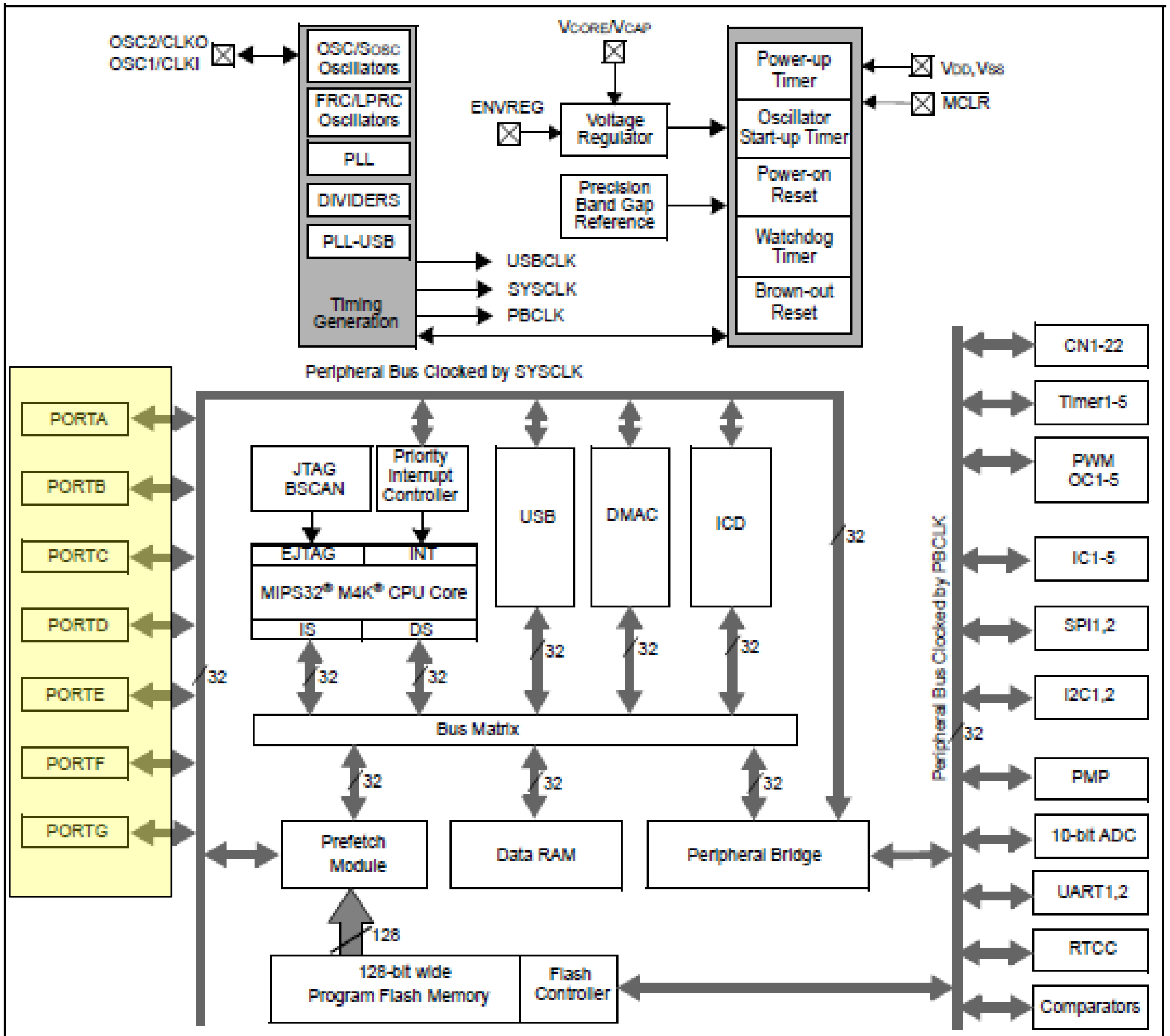
PIC Architecture



Note 1: Some features are not available on all device variants.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

I/O Ports

- **The general purpose I/O pins can be considered the simplest of peripherals. They allow the PIC32MX microcontroller to monitor and control other devices.**
- **To add flexibility and functionality to a device, some pins are multiplexed with alternate function(s).**
  - These functions depend on which peripheral features are on the device.
  - In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

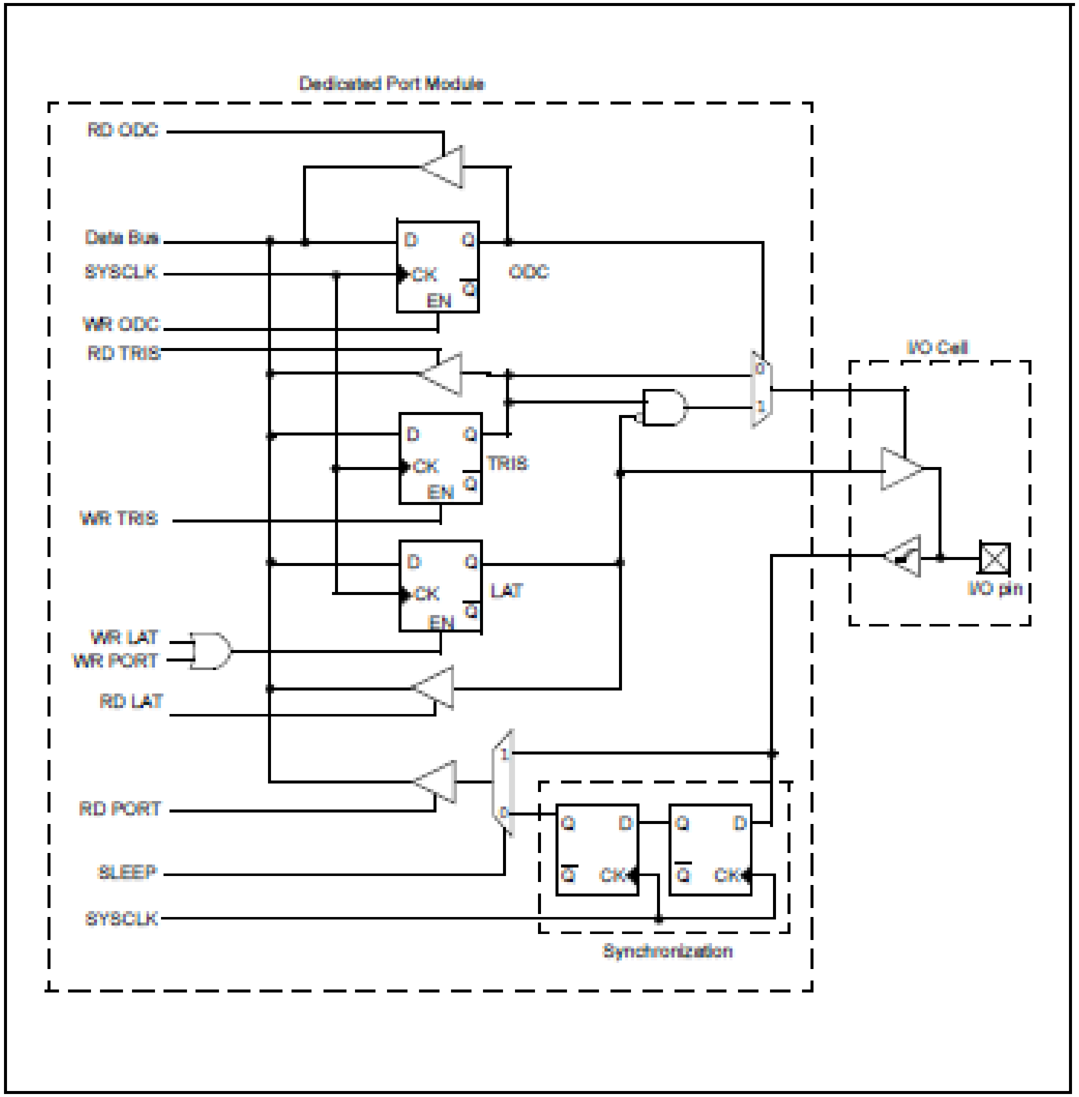
I/O Port Features

- **Following are some of the key features of this module:**
  - Individual output pin open-drain enable/disable
  - Individual input pin pull-up enable/disable
  - Monitor select inputs and generate interrupt on mismatch condition
  - Operate during CPU SLEEP and IDLE modes
  - Fast bit manipulation using CLR, SET and INV registers

Before reading and writing any I/O port, the desired pin or pins should be properly configured for the application

I/O Ports

Figure 12-1: Typical Port Structure Block Diagram



I/O Port Configuration

- Each I/O port has multiple registers directly associated with the operation of the port and one control register
- Each I/O port pin has a corresponding bit in these registers.
- Throughout this description, the letter ‘x’, denotes any or all Port module instances. For example, TRISx would represent TRISA, TRISB, TRISC, and so on.
- Any bit and its associated data and control registers that is not valid for a particular device will be disabled and will read as zeros.

I/O Port Configuration

- **The I/O Ports module consists of the following Special Function Registers (SFRs):**
  - TRISx: Data Direction register for the module ‘x’
  - PORTx: PORT register for the module ‘x’
  - LATx: Latch register for the module ‘x’
  - ODCx: Open-Drain Control register for the module ‘x’
  - CNCON: Interrupt-on-Change Control register
  - CNEN: Input Change Notification Interrupt Enable register
  - CNPUE: Input Change Notification Pull-up Enable register

Registers for Configuring Tri-state Functions (TRISx)

- **The TRISx registers configure the data direction flow through port I/O pins. The TRISx register bits determine whether a PORTx I/O pin is an input or an output:**
  - If a data direction bit is ‘1’, the corresponding I/O port pin is an input
  - If a data direction bit is ‘0’, the corresponding I/O port pin is an output
  - A read from a TRISx register reads the last value written to that register
  - All I/O port pins are defined as inputs after a Power-on Reset (POR)

Registers for Configuring PORT Functions (PORTx)

- **The PORTx registers allow I/O pins to be accessed:**
  - A write to a PORTx register writes to the corresponding LATx register (PORTx data latch). Those I/O port pin(s) configured as outputs are updated.
  - A write to a PORTx register is the effectively the same as a write to a LATx register
  - A read from a PORTx register reads the synchronized signal applied to the port I/O pins

Registers for Configuring Latch Functions (LATx)

- **The LATx registers (PORTx data latch) hold data written to port I/O pins:**
  - A write to a LATx register latches data to corresponding port I/O pins. Those I/O port pins configured as outputs are updated.
  - A read from LATx register reads the data held in the PORTx data latch, **not from the port I/O pins**

Registers for Open-Drain Configuration (ODCx)

- **Each I/O pin can be individually configured for either normal digital output or open-drain output.**
- **This is controlled by the Open-Drain Control register, ODCx, associated with each I/O pin.**
  - If the ODCx bit for an I/O pin is a ‘1’, the pin acts as an open-drain output.
  - If the ODCx bit for an I/O pin is a ‘0’, the pin is configured for a normal digital output (the ODCx bit is valid only for output pins).
  - After a Reset, the status of all the bits of the ODCx register is set to ‘0’.

Port A and B SFRs

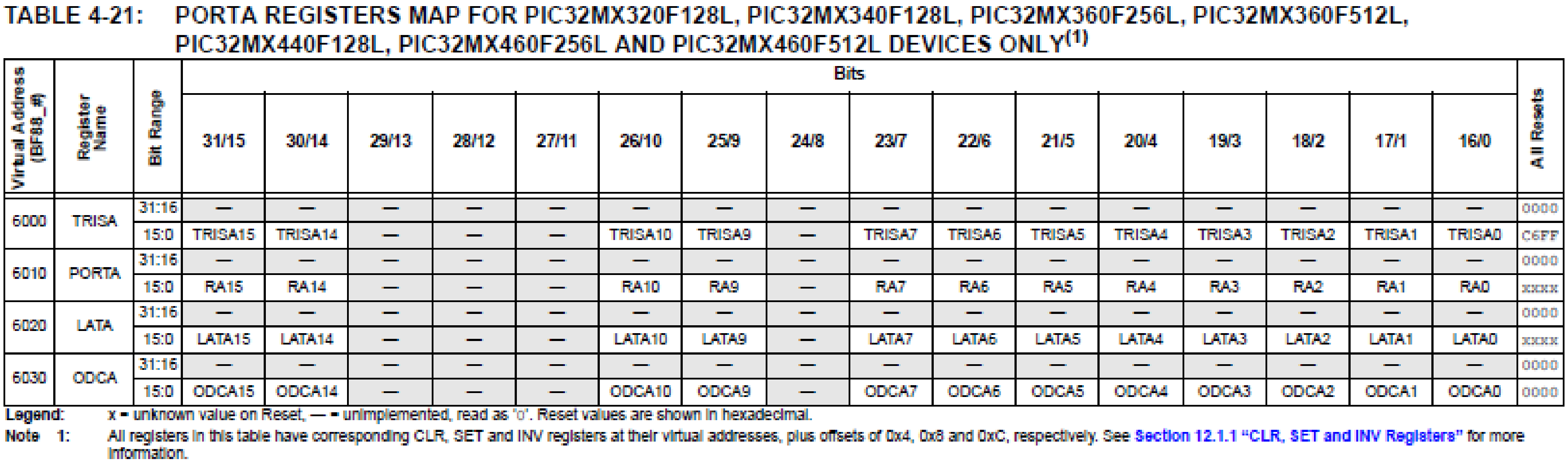


TABLE 4-21: PORTA REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY[(1)]

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
6010	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6020	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6030	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

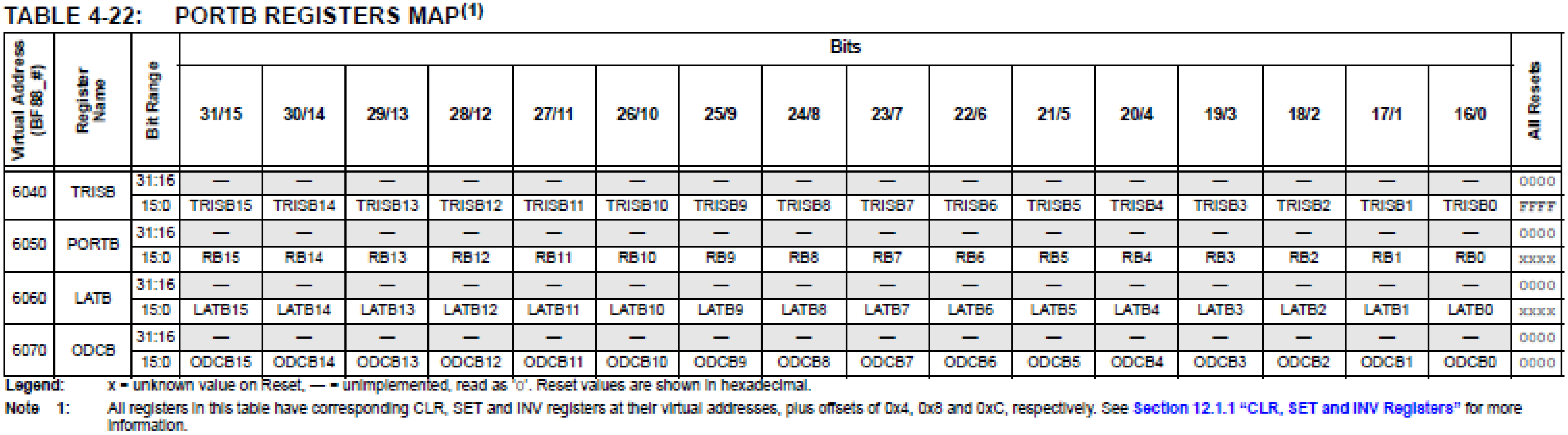


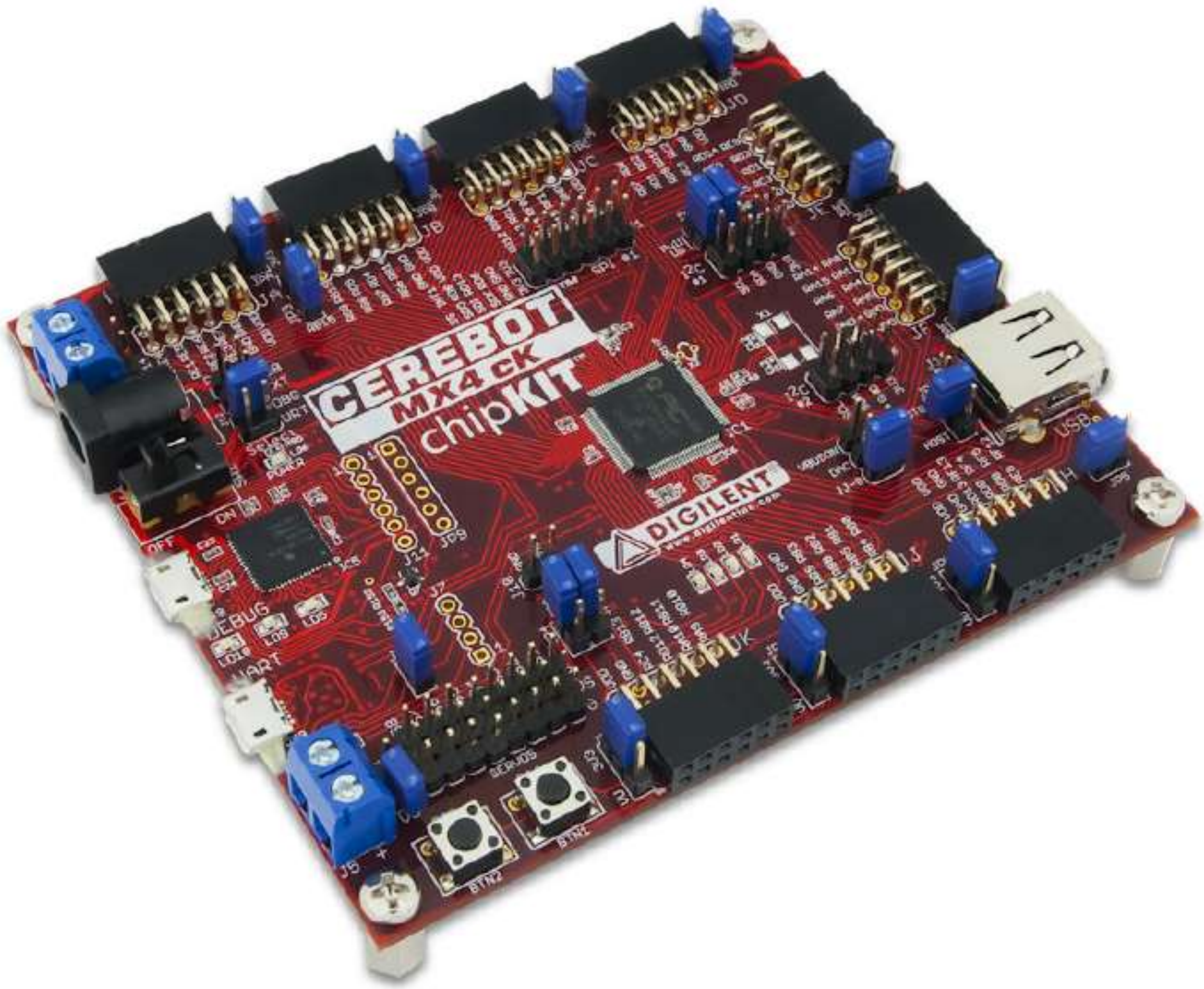
TABLE 4-22: PORTB REGISTERS MAP[(1)]

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6040	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6050	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
6060	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
6070	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

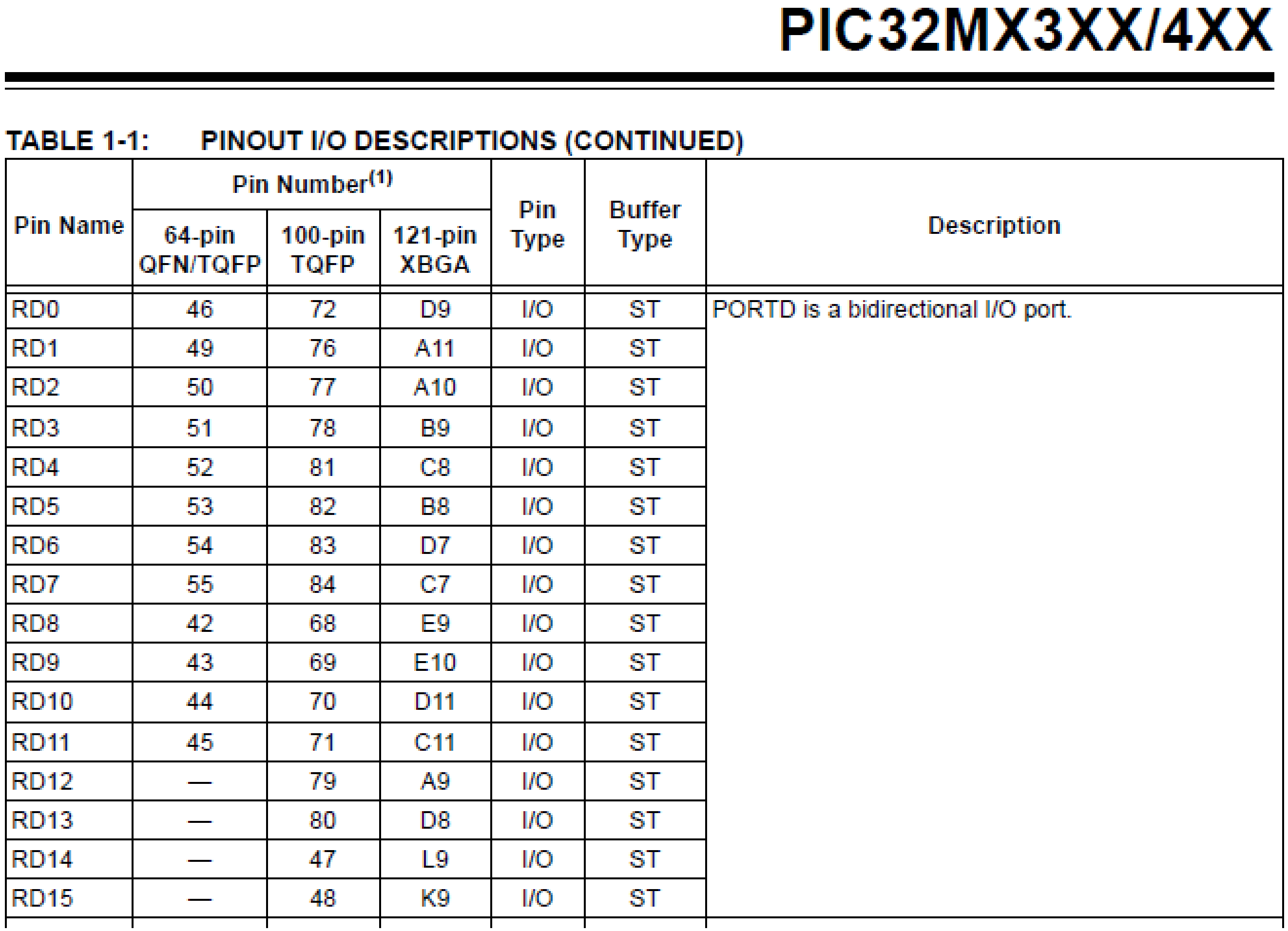
Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

chipKIT MX4 Board



I/O Port Pins – Example – Port D



PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[(1)]			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RD0	46	72	D9	I/O	ST	PORTD is a bidirectional I/O port.
RD1	49	76	A11	I/O	ST	
RD2	50	77	A10	I/O	ST	
RD3	51	78	B9	I/O	ST	
RD4	52	81	C8	I/O	ST	
RD5	53	82	B8	I/O	ST	
RD6	54	83	D7	I/O	ST	
RD7	55	84	C7	I/O	ST	
RD8	42	68	E9	I/O	ST	
RD9	43	69	E10	I/O	ST	
RD10	44	70	D11	I/O	ST	
RD11	45	71	C11	I/O	ST	
RD12	—	79	A9	I/O	ST	
RD13	—	80	D8	I/O	ST	
RD14	—	47	L9	I/O	ST	
RD15	—	48	K9	I/O	ST	

Cerebot MX4cK Digital I/O Devices

- For our experiments, we will use on-board devices connected to digital I/O lines:

Inputs	Port/Pin	
BTN1	RA6	Port A Bit 6
BTN2	RA7	Port A Bit 7

Outputs	Port/Pin	
LD1	RB10	Port B Bit 10
LD2	RB11	Port B Bit 11
LD3	RB12	Port B Bit 12
LD4	RB13	Port B Bit 13