Lecture 22 Quiz

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1. **What components are part of the forwarding path the SW in the pipeline you are design in lab?**

   The forwarding unit is responsible for generating the correct selection bits for the ALU source multiplexers, as well as the data memory forwarding multiplexers.

2. **What is the primary purpose of the Pipeline Control Unit? What does it need to do in the case of a branch being resolved as taken in the execute stage?**

   The pipeline control unit orchestrates the flow of instructions through the pipeline by controlling the stalling and flushing of the pipeline registers as well as selecting the correct next PC address. When a taken branch is detected in the execute stage, the pipeline control unit must flush the instruction in the fetch stage and resume fetching at the branch target address.

3. **How much main memory did the Apple II have? Did it make use of cache? Why or why not?**

   The Apple II had 64 kilobytes of main memory and no cache. The memory was small enough and the processor was approximately at the same speed as the DRAM, so cache wasn't needed.

4. **Why is Level 3 cache large for server class processor?**

   In the server market, you're going to have a much larger level 3 cache because it can be distributed across the different cores that are typically found in servers.