ECE338
Lab #1: Behavioral-to-Schematic Translation, if statement
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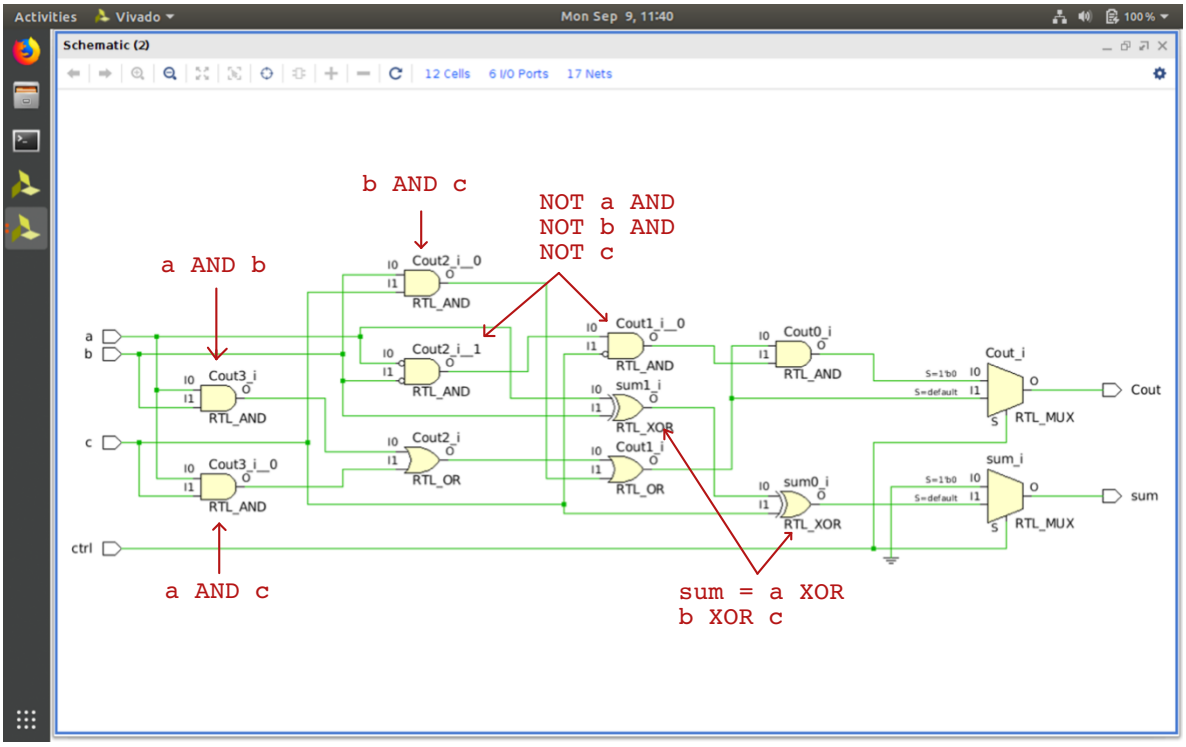
For Lab #1, we were tasked with implementing a *behavioral if* statement that takes three inputs (a,b,c) and uses a combination of logic gates such as AND, OR, and XOR statements to create an if-else example. Please see marked up RTL Analysis Schematic for corresponding logic gate descriptions.



In the Synthesized Design Schematic, all of the logic gates and multiplexers are condensed and represented by LUTs (lookup tables). This makes for a more organized, if less detailed, view of our behavioral VHDL code.