ECE 371
Materials and Devices

12/05/19 - Lecture 26

Ch. 10 – Basic MOSFET Operation

General Information

- Homework #8 due today.
- Solutions to homework #8 will be posted later today.
- Example final exam posted.
- Review session Friday 12/6 at 3:30 pm in CHTM 103. I will record the session and post on the website.
- Final Exam (Tuesday 12/10, 12:30pm-2:30pm, cumulative but focused on ch. 7,8,10)
  - Two hours long
  - Two sheets of notes (8.5 inch x 11 inch, front and back). Closed book.
  - 4-5 problems mostly covering Ch. 7, 8, 10
  - Several multiple choice and short answer questions covering the whole course
- Reading for next time: review ☺

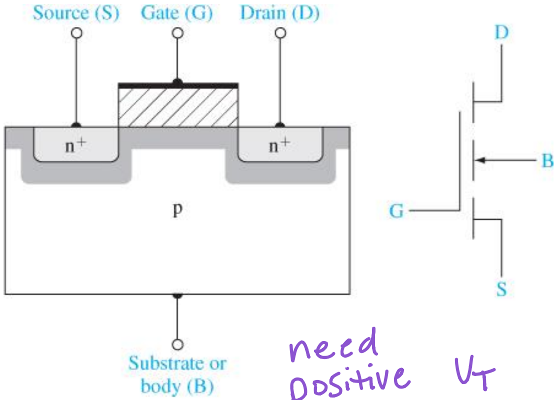
FET Modes of Operation

- **nMOS** (n-channel on p-substrate)
  - $V_T < 0 \rightarrow$ **depletion mode (on at V_G = 0)**. Need to apply a negative bias to turn the channel "off".
  - $V_T > 0 \rightarrow$ **enhancment mode (off at V_G = 0)**. Need to apply a positive bias to turn the channel "on".

- **pMOS** (p-channel on n-substrate)
  - $V_T < 0 \rightarrow$ **enhancement mode (off at V_G = 0)**. Need to apply a negative bias to turn the channel "on".
  - $V_T > 0 \rightarrow$ **depletion mode (on at V_G = 0)**. Need to apply a positive bias to turn the channel "off".

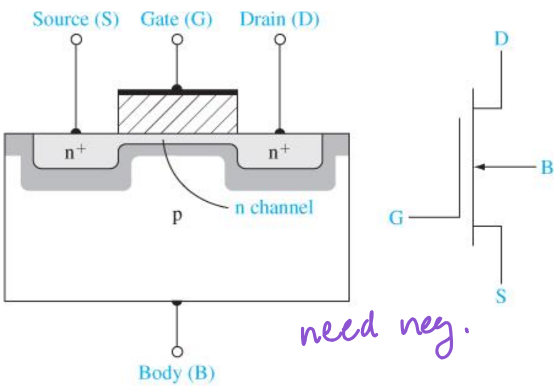
- Whether a device is enhancement mode or depletion mode depends upon the inherent surface band bending, which depends upon the doping, ϕ_{ms}, and the oxide thickness, charge, and dielectric constant

n-Channel MOSFETs



need positive V_T

Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.



need neg.

Figure 10.35 | Cross section and circuit symbol for an n-channel depletion mode MOSFET. nMOS

- Flow of charge is within the inversion layer (channel) adjacent to the oxide-semiconductor interface
- Inversion layer of electrons "connects" source (S) and drain (D)
- Electrons flow from source to drain
- Current flows from drain to source
- Drain and gate biased positive with respect to source
- Enhancement mode (E-mode) requires positive gate voltage to induce the channel
- Depletion mode (D-mode) has inversion channel at zero gate bias

p-Channel MOSFETs

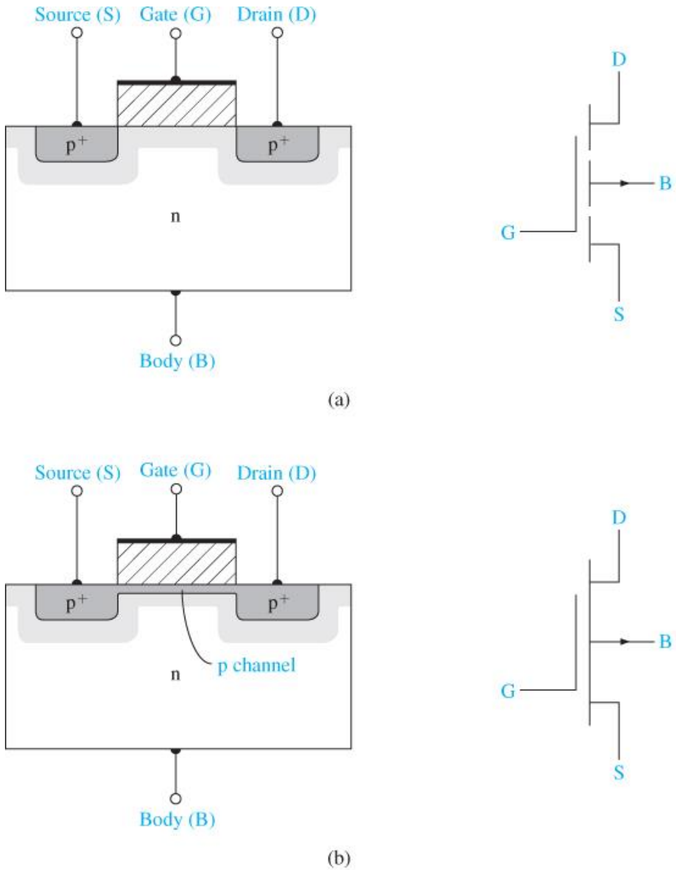


Figure 10.36 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET and (b) a p-channel depletion mode MOSFET.

- Holes flow from the source to the drain
- Current flows from the source to the drain
- Inversion layer of holes "connects" source and drain
- Drain and gate biased negative with respect to source
- V_T negative for E-mode and positive for D-mode

MOSFET: Basic Operation

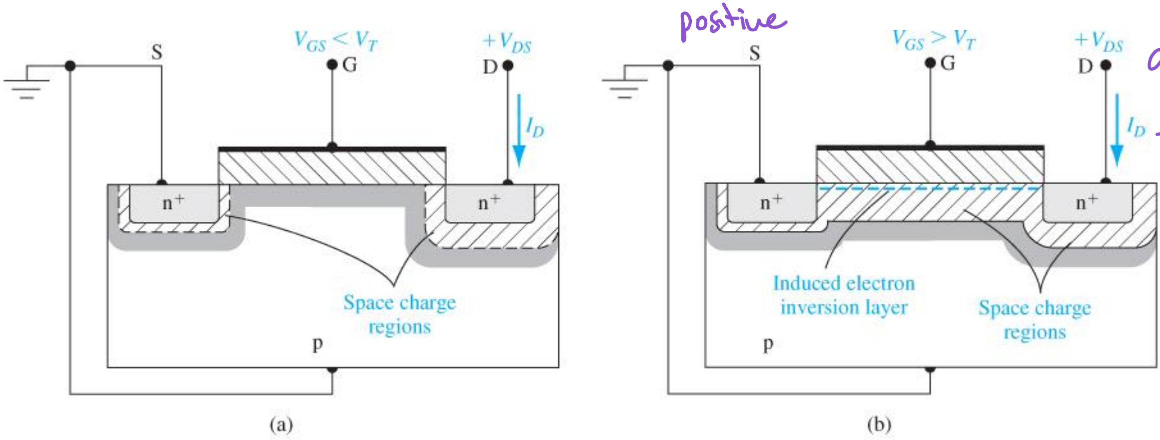


Figure 10.37 | The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ and (b) with an applied gate voltage $V_{GS} > V_T$.

always reverse biased so that current flows through channel

$$\boxed{I_D = g_d V_{DS}}$$

g_d is transconductance

$$\boxed{g_d = \frac{W}{L}\mu_n |Q_n'|}$$

reversed for pMOS

- For V_{GS} < V_T and V_{DS} small, there is no inversion channel
- Drain-to-substrate pn junction is always reverse biased. Reverse current contributes negligible amount to I_D
- For V_{GS} > V_T and V_{DS} positive, current flows from the drain to the source (nMOS)
- ***Basic MOSFET operation is the modulation of the channel transconductance by the gate voltage ($V_G \rightarrow g_d \rightarrow I_D$)***

Increasing V_{GS} for Small V_{DS}

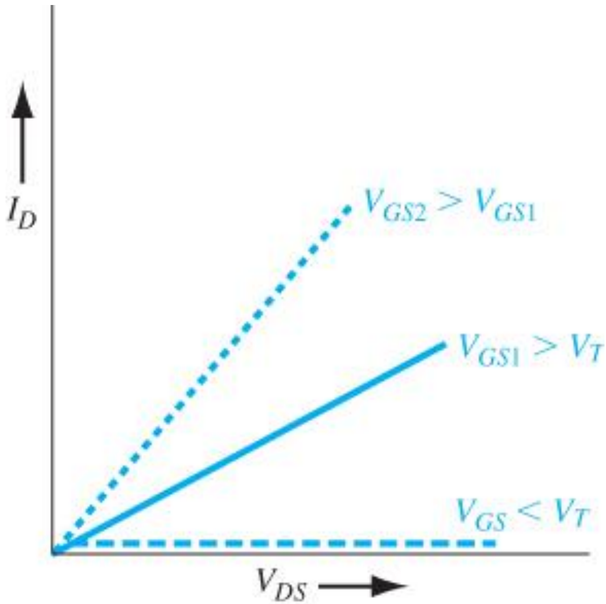
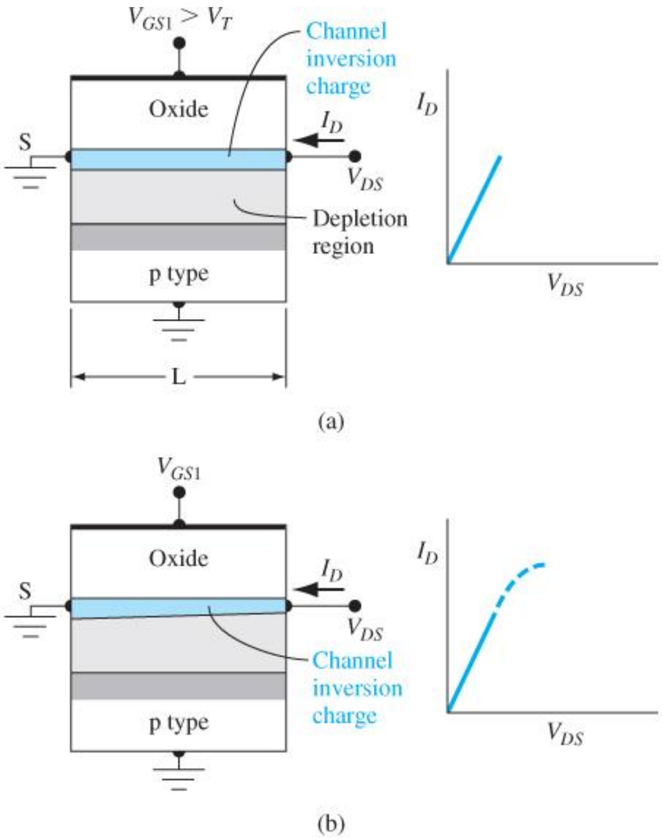


Figure 10.38 | I_D versus V_{DS} characteristics for small values of V_{DS} at three V_{GS} voltages.

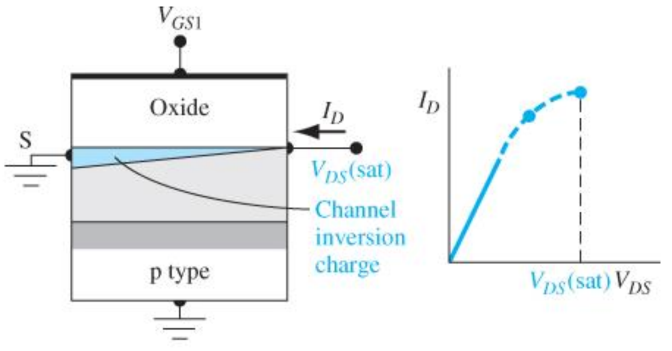
- Gate voltage modulates the charge density and transconductance in the channel
- For $V_{GS} < V_T$, no current flows in n-channel E-mode FET
- For $V_{GS} > V_T$, current flows
- Larger V_{GS} gives larger slope of I_D vs. V_{DS} curve
- Small V_{DS} usually implies operation in the linear region

Increasing V_{DS} for a Given V_{GS}

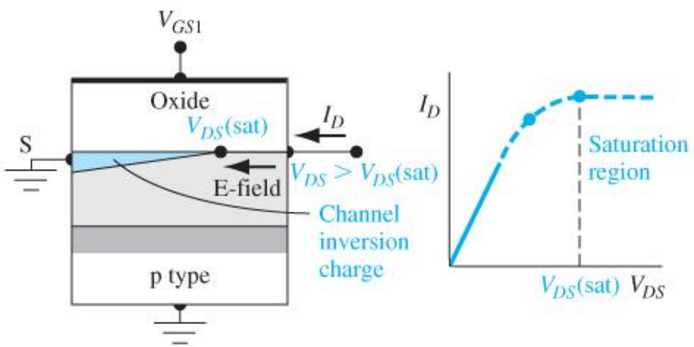


- As V_{DS} increases, the voltage across the drain side of the oxide becomes closer to the drain voltage, so the charge density and g_d are reduced near the drain
- Channel thickness is reduced near the drain
- The I_D vs. V_{DS} curve begins to roll-over

Increasing V_{DS} for a Given V_{GS}



(c)



(d)

$$\boxed{V_{DS(sat)} = V_{GS} - V_T}$$

- As V_{DS} increases more, the voltage drop across the oxide on the drain side is lowered to the point of V_T and there is no inversion charge at the edge of the drain
- This point is called the “pinch off” or “saturation” point
- Beyond $V_{DS(sat)}$, the pinch off moves closer to the source and a space charge region is left under the gate near the drain
- The I_D vs. V_{DS} curve saturates
- Electrons reach the end of the inversion layer and are injected into the depletion layer where the built-in E-field sweeps them toward the drain

I_D vs. V_{DS} for Various V_{GS} (n-Channel)

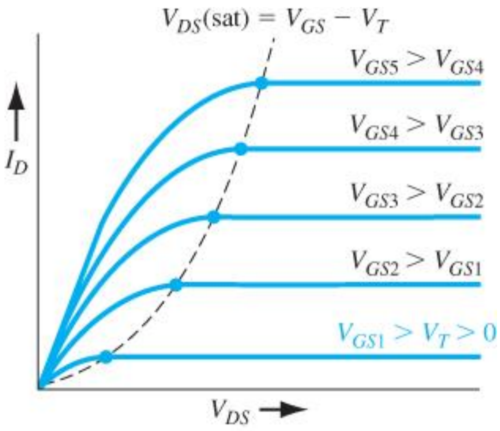


Figure 10.40 | Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET.

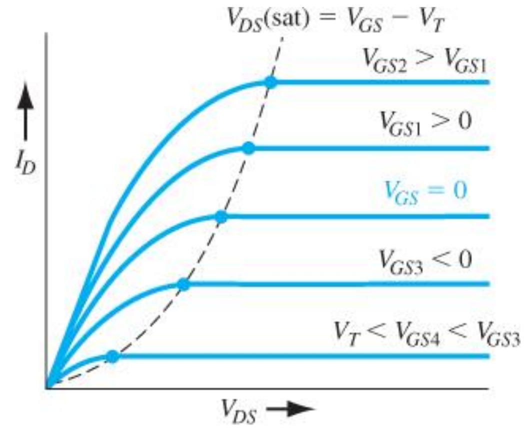


Figure 10.42 | Family of I_D versus V_{DS} curves for an n-channel depletion mode MOSFET.

Linear region for $0 \leq V_{DS} \leq V_{DS(sat)}$

$$\boxed{I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]}$$

Saturation region for $V_{DS} \geq V_{DS(sat)}$

$$\boxed{I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2}$$

p-Channel MOSFET I_D vs. V_{DS}

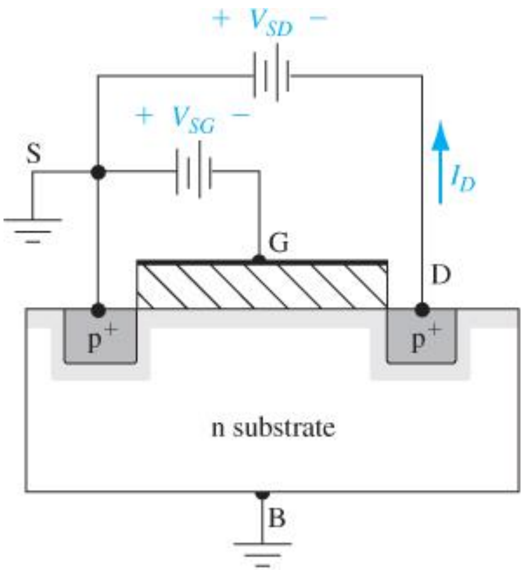


Figure 10.49 | Cross section and bias configuration for a p-channel enhancement mode MOSFET.

- Drain voltage negative with respect to the source
- Gate voltage negative with respect to the source
- $V_{SD(sat)} = V_{SG} + V_T$
- V_T is negative for E-mode and positive for D-mode

Linear region for $0 \leq V_{SD} \leq V_{SD(sat)}$

$$\boxed{I_D = \frac{W\mu_p C_{ox}}{2L}\left[2(V_{SG} - V_T)V_{SD} - V_{SD}^2\right]}$$

Saturation region for $V_{SD} \geq V_{SD(sat)}$

$$\boxed{I_D = \frac{W\mu_p C_{ox}}{2L}(V_{SG} - V_T)^2}$$