ECE 322L
Electronics 2

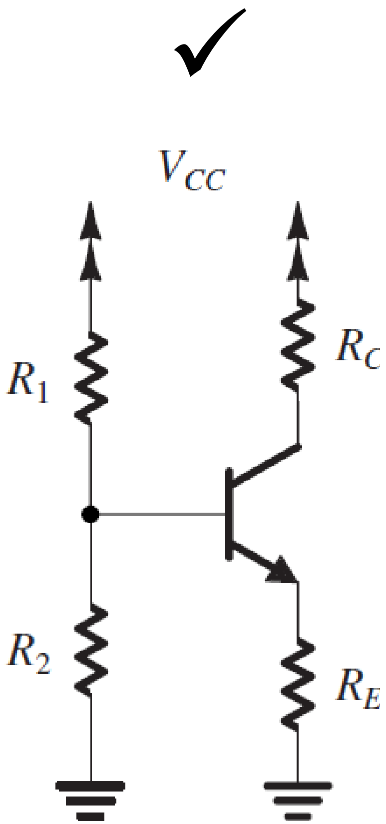
03/05/20- Lecture 13

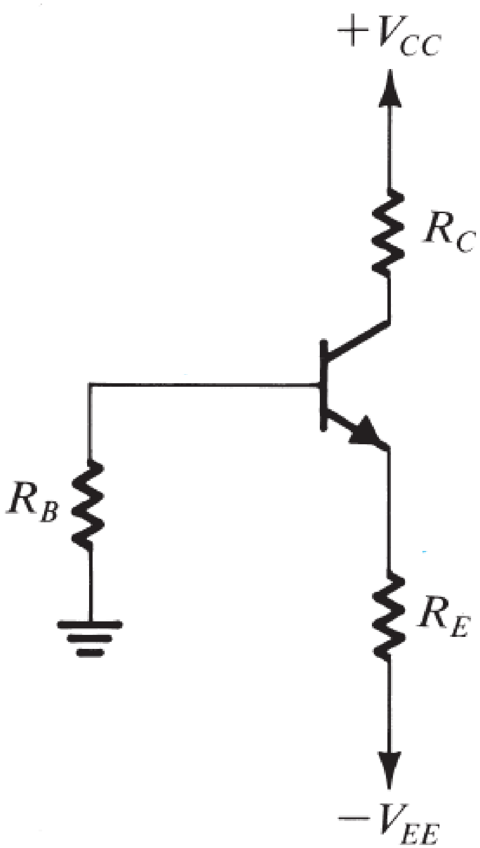
Biasing the BJT 2

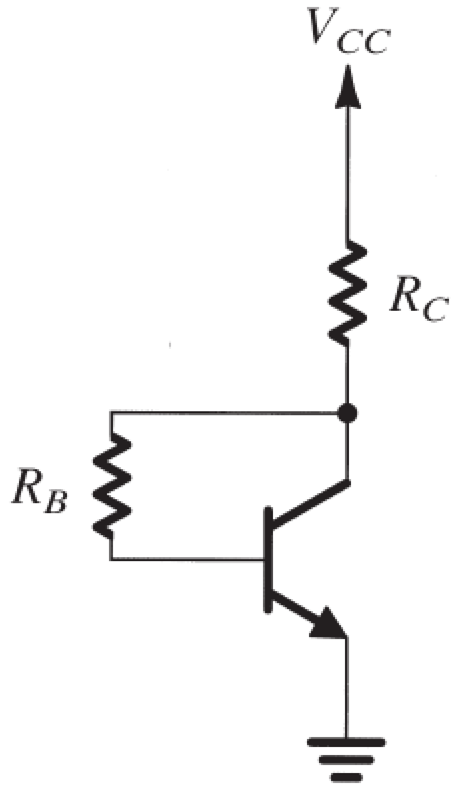
Updates and overview

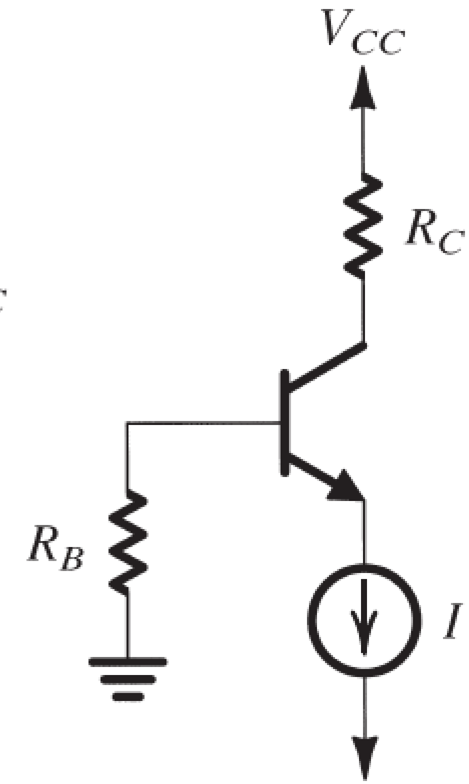
- There have been issues with UNM Learn reporting incorrect due dates for the assignment. The problem has been rectified.
- Lecture 13- Biasing the BJT 1 (Neamen 5.2 and 5.4, S&S 6.7)

Biasing configurations



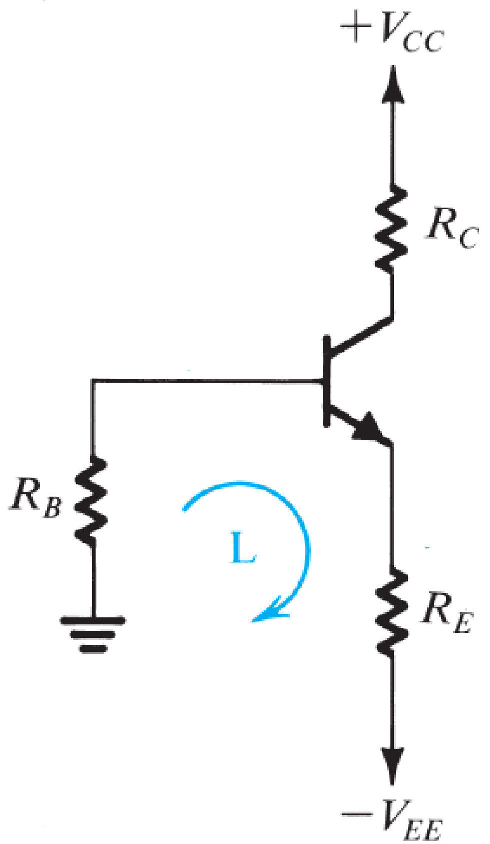






Biasing configurations (2)

* See next slide for more details



Note: The V_{BE} on these slide is equivalent to $V_{BE}(on)$ on the slides of lecture 12 and on the handout

KVL on loop L $\quad I_E = \dfrac{V_{EE} - V_{BE}}{R_E + R_B/(\beta+1)}$

$$I_{CQ} = \alpha I_{EQ} = \frac{\beta}{\beta+1} I_{EQ} \cong \frac{\beta(V_{EE} - V_{BE})}{(\beta+1)R_E + R_B}$$

$$R_B \ll (\beta+1)\,R_E \rightarrow I_{CQ} \cong \frac{\beta(V_{EE} - V_{BE})}{(\beta+1)R_E}$$

$$\beta \gg 1 \quad \beta/(1+\beta) \cong 1 \qquad I_{CQ} \cong \frac{(V_{EE} - V_{BE})}{R_E}$$

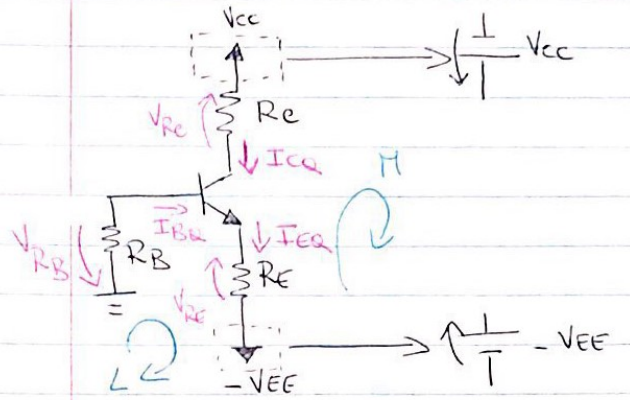
$$V_{EE} \gg V_{BE} \qquad I_{CQ} \cong \frac{V_{EE}}{R_E}$$

$$\boxed{V_{EE} \gg V_{BE} \;\&\; R_B \ll (\beta+1)\,R_E}$$

Condition for a bias-stable circuit against variations of temperature and ß.

$$V_{EE} \cong \frac{V_{EE} + V_{CC}}{3} \;\&\; R_B \cong 0.1(\beta+1)\,R_E$$ Rule of thumb

Biasing configurations (2)



1) KVL on loop L:

$$-V_{RB} - V_{BE(on)} - V_{RE} - (-V_{EE}) = 0 \quad (1)$$

2) Using Ohm's law

$$-R_B I_{BQ} - V_{BE(on)} - R_E I_{EQ} + V_{EE} = 0 \quad (2)$$

3) Assuming that the BJT is in active mode

$$I_{BQ} = I_{EQ} / (\beta+1) \quad (3)$$

4) Combining (3) and (2)

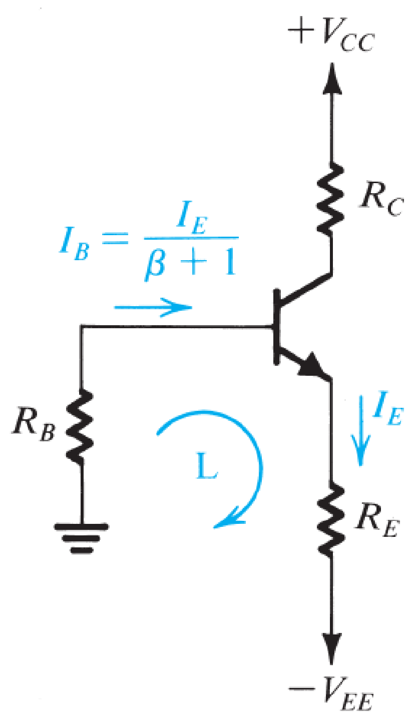
$$-R_B \frac{I_{EQ}}{\beta+1} - V_{BE(on)} - R_E I_{EQ} + V_{EE} = 0 \quad (4)$$

$$I_{EQ} = \frac{V_{EE} - V_{BE(on)}}{R_E + \frac{R_B}{\beta+1}} \quad (5)$$

5) $I_{CQ} = \alpha I_{EQ} = \frac{\beta}{\beta+1} I_{EQ} = \frac{\beta (V_{EE} - V_{BE(on)})}{R_E(\beta+1) + R_B} \quad (6)$

In-class problem 1

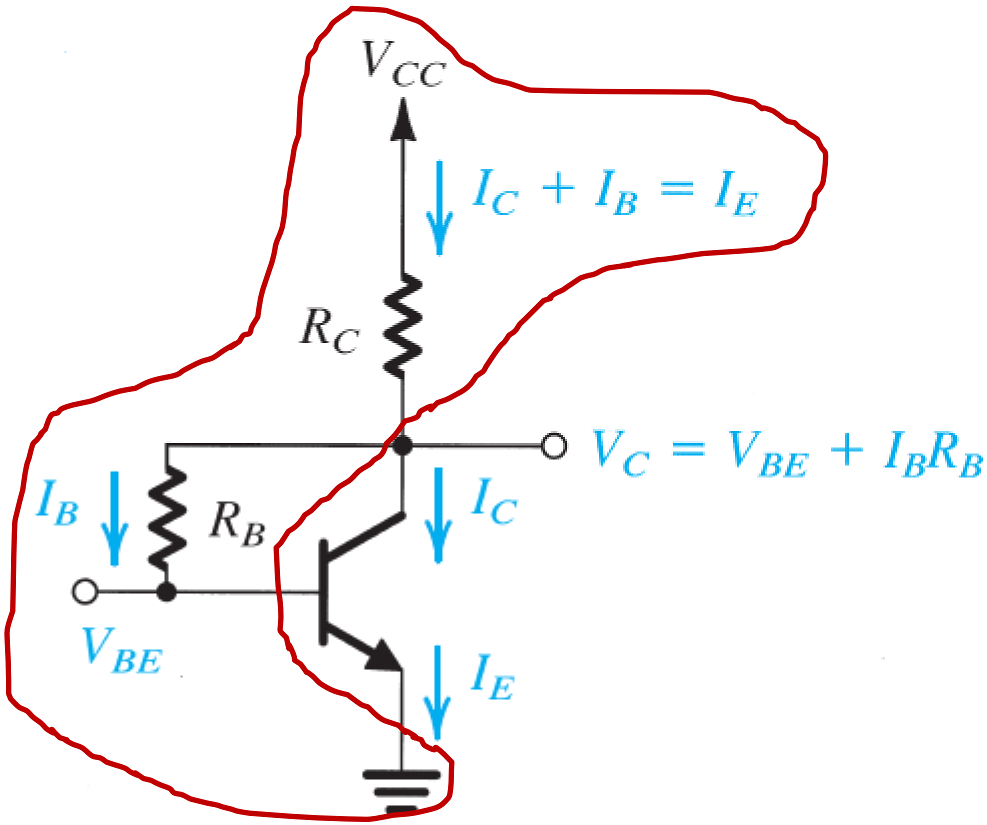
The bias arrangement below is to be used for a common-emitter amplifier. Design the circuit to establish a DC collector current of 1mA and provide the highest possible open-circuit voltage gain while allowing a maximum signal swing of $\pm$ 2 V at the output of the amplifier. Use V_{CC}=10 V and V_{EE}=5 V power supplies. Assume that the peak-to-peak value of the ac signal on the emitter is $v_{e,pp}$=0.04 V and that β=200. Specify where within the Q point is located (e.g. in the middle of the forward active region, close to the cut-off region or close to the saturation region).



* See handout for solution

Biasing configurations (3)

Loop L



KVL on loop L

$$V_{CC} = I_E R_C + I_B R_B + V_{BE}$$

$$= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE}$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)}$$

$$R_B/(\beta + 1) \ll R_C$$

$$V_{CC} - V_{BE}$$

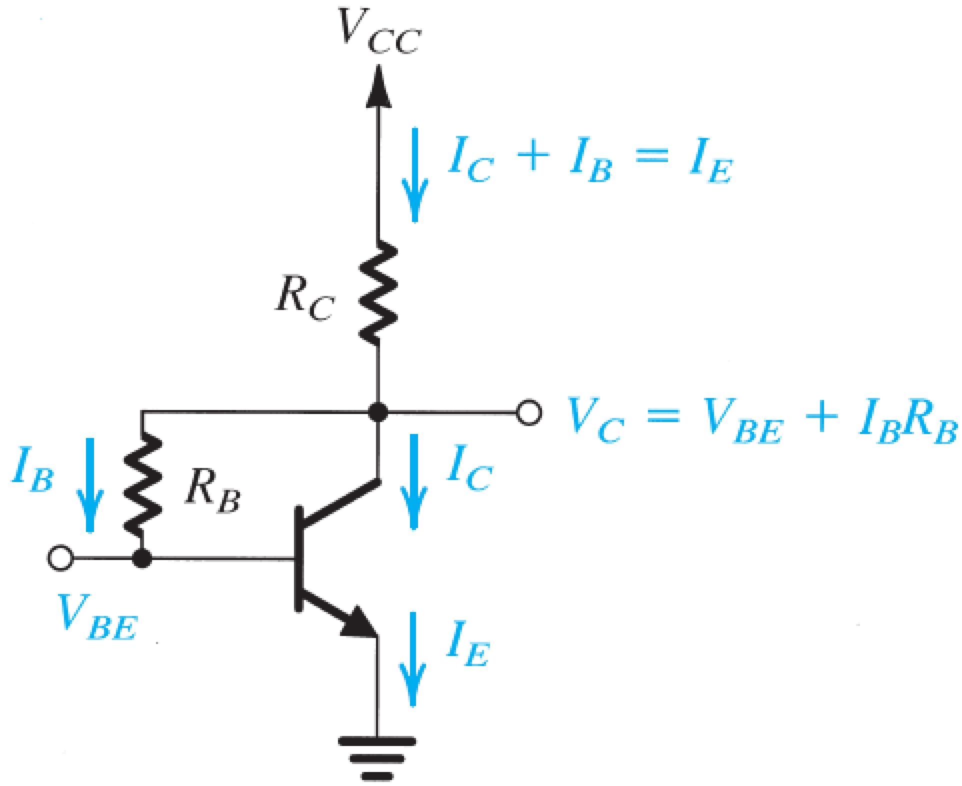
$$V_{CC} \gg V_{BE} \;\&\; R_B \cong 0.1(\beta + 1)\, R_C$$

Condition for a bias-stable circuit against variations of temperature and β

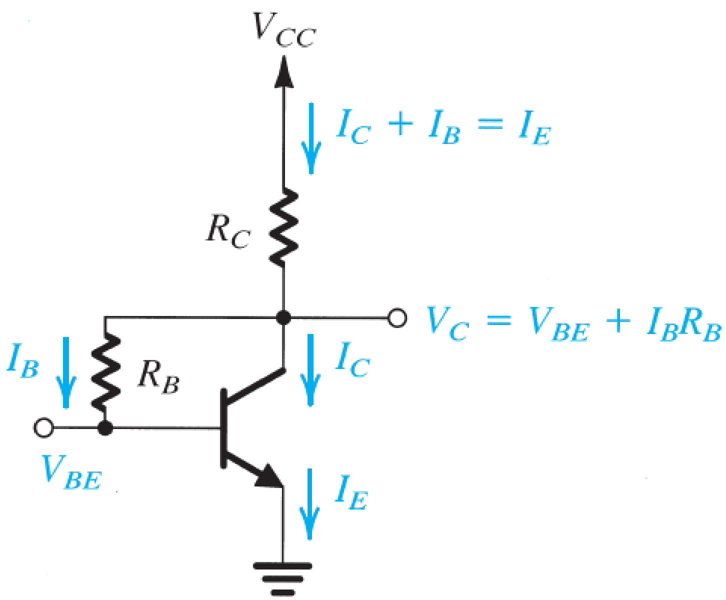
Note: The V_{BE} on these slide is equivalent to V_{BE}(on) on the previous slides

Take-home problem 1

D6.49 Design the circuit of Fig. 6.62 to obtain a dc emitter current of 1 mA, maximum gain, and a ±2-V signal swing at the collector; that is, design for $V_{CE} = +2.3$ V. Let $V_{CC} = 10$ V and $\beta = 100$.



Take-home problem 1, solution



$I_E = 1\,mA$ $\quad |A_V| = |A_{Vmax}|$ $\quad \beta = 100$ $\quad V_{CE,SAT} = 0.3\,V$

$V_{CE} - 2V = V_{CE,SAT} \Rightarrow V_{CE} = 2.3\,V$ $\quad I_C \simeq I_E$

$$I_E = \frac{V_{CC} - V_{CE}}{R_e} \Rightarrow R_e = \frac{7.7}{I_E} = 7.7\,k\Omega$$

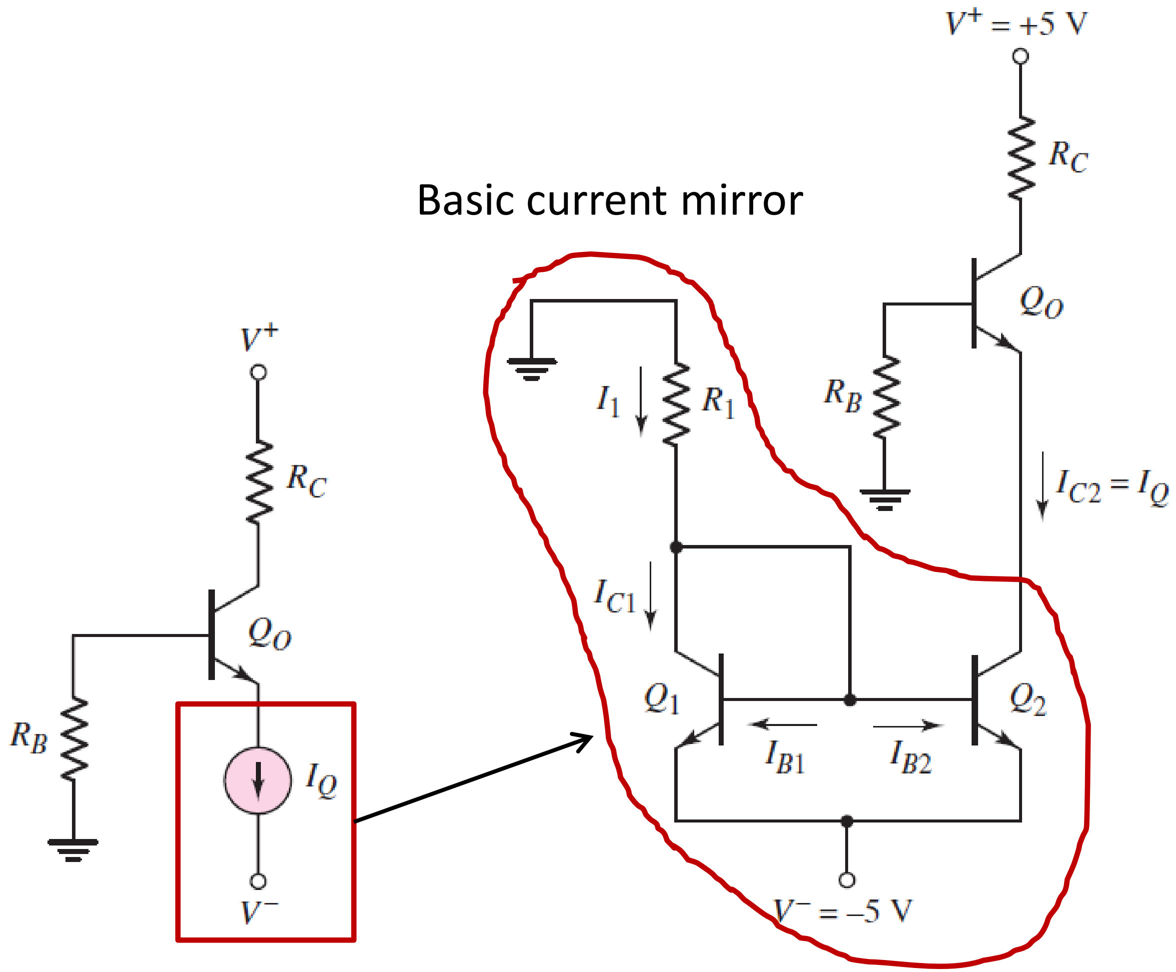
$V_{CB} = V_{CE} - V_{BE} = 2.3 - 0.7 = 1.6\,V$

$$I_B R_B = 1.6\,V \Rightarrow \frac{I_E}{\beta+1} R_B = 1.6\,V$$

$$R_B = \frac{101 \cdot 1.6}{1m} = 160\,k\Omega$$

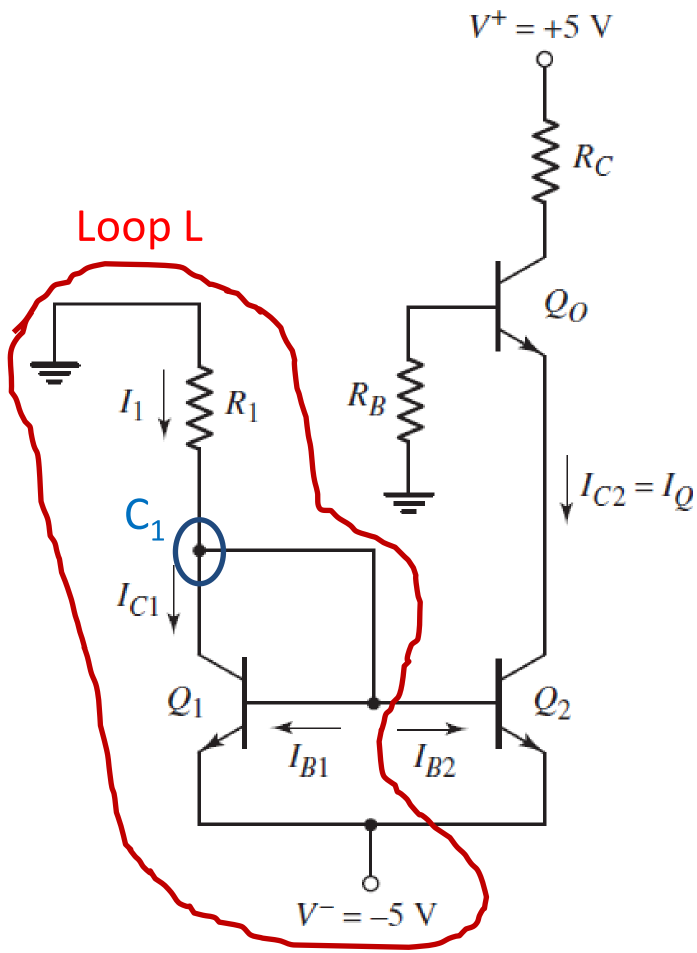
Biasing configurations (4)

Basic current mirror



Q_1 and Q_2 are two identical transistors held at the same temperature

Biasing configurations (4)



KVL at loop L $\quad 0 = I_1 R_1 + V_{BE}\,(\text{on}) + V^-$

$$I_1 = \frac{-(V^- + V_{BE}\,(\text{on}))}{R_1}$$

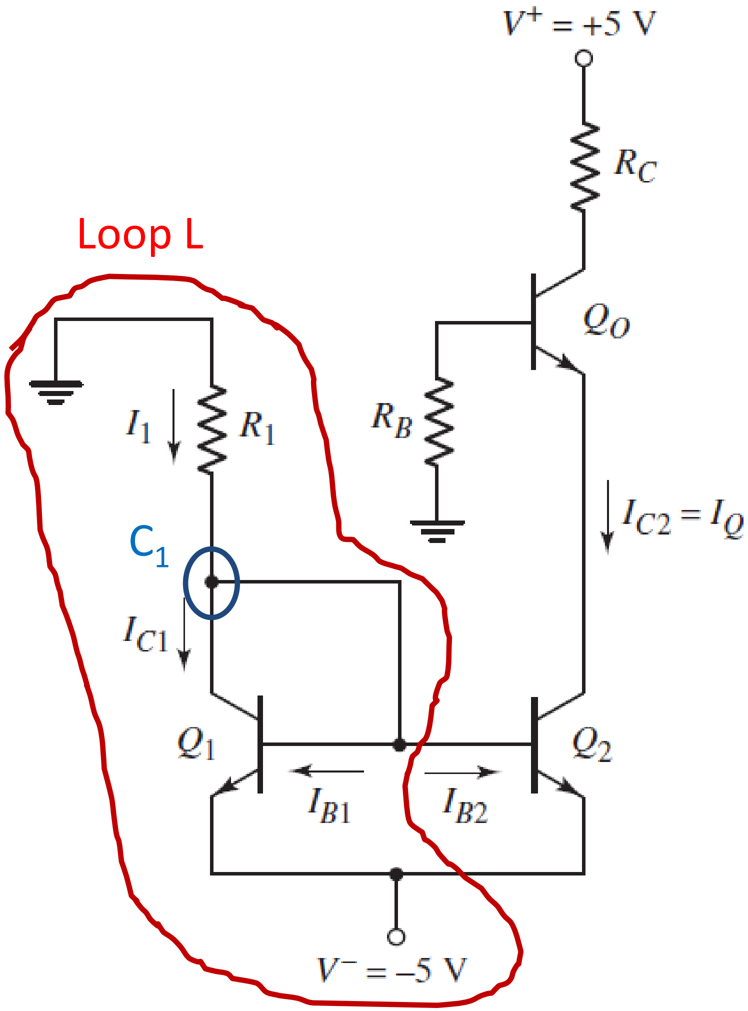
KCL at node C1 $\quad I_1 = I_{C1} + I_{B1} + I_{B2}$

$$I_1 = I_{C1} + 2I_{B2} = I_{C2} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C2} = I_Q = \frac{I_1}{\left(1 + \frac{2}{\beta}\right)}$$

Q_1 operates in the active region since V_{CB}=0 and (V_{CE}=$V_{BE(on)}$)>$V_{CE,SAT}$)

Biasing configurations (4)



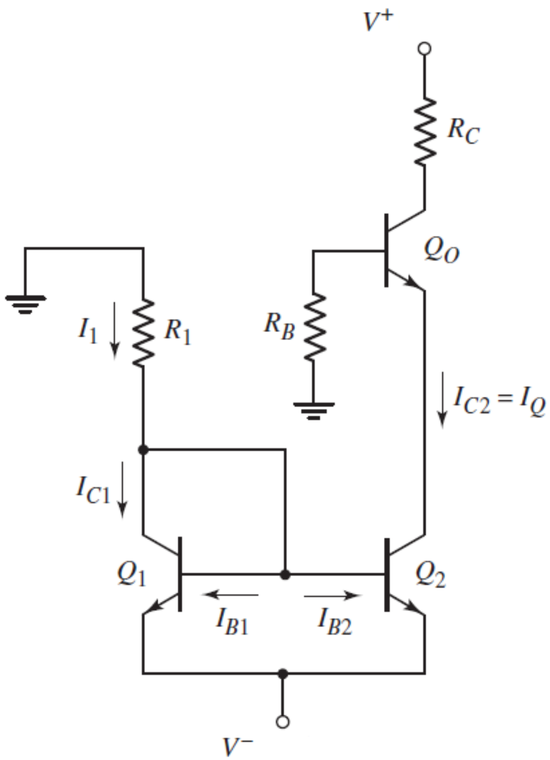
$$I_1 = \frac{-(V^- + V_{BE}(\text{on}))}{R_1}$$

$$I_{C2} = I_Q = \frac{I_1}{\left(1 + \frac{2}{\beta}\right)}$$

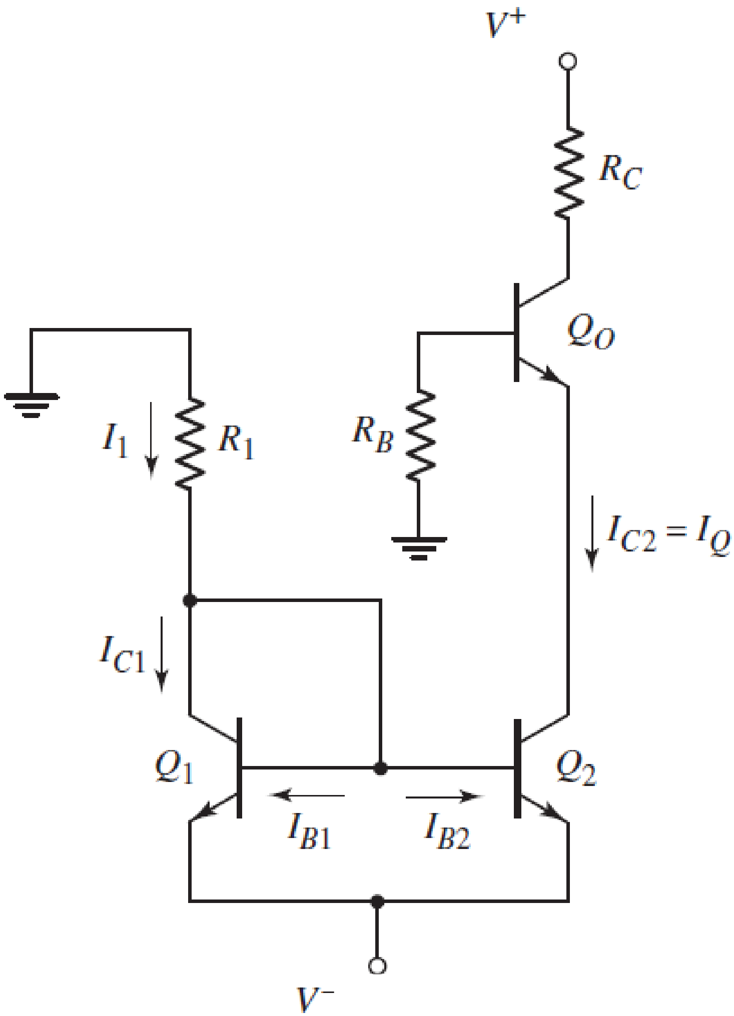
- For reasonable values of β the Q point is stable against variations of β.
- The Q point is also independent from R_B, hence one can select R_B to optimize the input resistance of a CE voltage amplifier.
- Biasing by a current mirror guarantees stability against variation of temperature if $V^- >> V_{BE}(\text{on})$.

Take-home problem 2

Ex 5.18: In the circuit shown in Figure 5.60, the parameters are $V^+ = 3.3$ V, $V^- = -3.3$ V, and $R_B = 0$. The transistor parameters are $\beta = 60$ and $V_{BE}(\text{on}) = 0.7$ V. Design the circuit such that $I_{CQ}(Q_O) = 0.12$ mA and $V_{CEQ}(Q_O) = 1.6$ V. What are the values of I_Q and I_1? (Ans. $I_Q = 0.122$ mA, $I_1 = 0.126$ mA, $R_1 = 20.6\ \text{k}\Omega$, $R_C = 20\ \text{k}\Omega$)



Take-home problem 2, solution



$$V_{EO} = -0.7 \text{ V}, \quad V_{CO} = -0.7 + 1.6 = 0.9 \text{ V}$$

$$R_C = \frac{V^+ - V_{CO}}{I_{CQO}} = \frac{3.3 - 0.9}{0.12} = 20 \text{ k}\Omega$$

$$I_Q = \left(\frac{1+\beta}{\beta}\right) I_{CQO} = \left(\frac{61}{60}\right)(0.12) = 0.122 \text{ mA}$$

$$I_1 = \left(1 + \frac{2}{\beta}\right) I_Q = \left(1 + \frac{2}{60}\right)(0.122) = 0.126 \text{ mA}$$

$$I_1 = 0.126 = \frac{0 - V_{BE}(on) - (-3.3)}{R_1} = \frac{3.3 - 0.7}{R_1} \Rightarrow R_1 = 20.6 \text{ k}\Omega$$

Overview of lecture 14

- Signal response of the BJT

  BJT small-signal model

  (Neamen From 6.2.1 to 6.2.4)

  BJT amplifier configurations: overview (Neamen 6.3)

  Common emitter configurations (Neamen 6.4)