ECE338
Lab #5: Block Diagram of the Zynq processor
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For Lab #5 we were tasked with exploring the Block Diagram of the Zynq processor, the GPIO, and Block RAM.

design_1_wrapper.vhd

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```
1  --Copyright 1986-2018 Xilinx, Inc. All Rights Reserved...
10 library IEEE;
11 use IEEE.STD_LOGIC_1164.ALL;
12 library UNISIM;
13 use UNISIM.VCOMPONENTS.ALL;
14 entity design_1_wrapper is
15   port (
16     DDR_0_addr : inout STD_LOGIC_VECTOR ( 14 downto 0 );
17     DDR_0_ba : inout STD_LOGIC_VECTOR ( 2 downto 0 );
18     DDR_0_cas_n : inout STD_LOGIC;
19     DDR_0_ck_n : inout STD_LOGIC;
20     DDR_0_ck_p : inout STD_LOGIC;
21     DDR_0_cke : inout STD_LOGIC;
22     DDR_0_cs_n : inout STD_LOGIC;
23     DDR_0_dm : inout STD_LOGIC_VECTOR ( 3 downto 0 );
24     DDR_0_dq : inout STD_LOGIC_VECTOR ( 31 downto 0 );
25     DDR_0_dqs_n : inout STD_LOGIC_VECTOR ( 3 downto 0 );
26     DDR_0_dqs_p : inout STD_LOGIC_VECTOR ( 3 downto 0 );
27     DDR_0_odt : inout STD_LOGIC;
28     DDR_0_ras_n : inout STD_LOGIC;
29     DDR_0_reset_n : inout STD_LOGIC;
30     DDR_0_we_n : inout STD_LOGIC;
31     FCLK_CLK0 : out STD_LOGIC;
32     FCLK_RESET0_N : out STD_LOGIC;
33     FIXED_IO_0_ddr_vrn : inout STD_LOGIC;
34     FIXED_IO_0_ddr_vrp : inout STD_LOGIC;
35     FIXED_IO_0_mio : inout STD_LOGIC_VECTOR ( 53 downto 0 );
36     FIXED_IO_0_ps_clk : inout STD_LOGIC;
37     FIXED_IO_0_ps_porb : inout STD_LOGIC;
38     FIXED_IO_0_ps_srstb : inout STD_LOGIC;
39     GPIO_Ins_tri_i : in STD_LOGIC_VECTOR ( 31 downto 0 );
40     GPIO_Outs_tri_o : out STD_LOGIC_VECTOR ( 31 downto 0 );
41     PNL_BRAM_addr : in STD_LOGIC_VECTOR ( 12 downto 0 );
42     PNL_BRAM_din : in STD_LOGIC_VECTOR ( 15 downto 0 );
43     PNL_BRAM_dout : out STD_LOGIC_VECTOR ( 15 downto 0 );
44     PNL_BRAM_we : in STD_LOGIC_VECTOR ( 0 to 0 )
45   );
46 end design_1_wrapper;
```