Appendix B

Operation Theory

B.1 Analog Input Operation

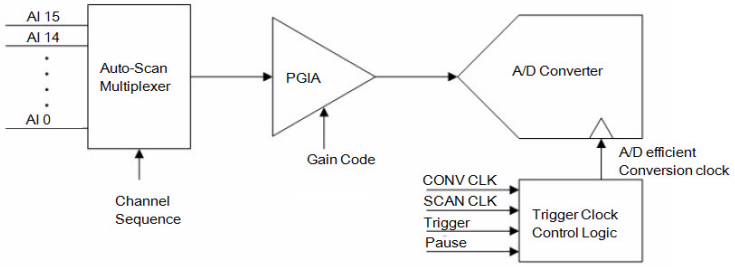
This section describes the following features of analog input that can help you realize how to configure the functions and parameters to match various applications.

- AI Hardware Structure
- Analog input ranges and gains
- Analog data acquisition mechanism
- Analog input acquisition modes
- AI SCAN/CONV clock source
- AI trigger sources
- Analog input data format

B.1.1 AI Hardware Structure

The AI conversion hardware structure includes four major parts:

- **Auto-scan multiplexer** routes the analog input signals into AI converter channel by channel in a software-defined sequence.
- **PGIA** (Programmable Gain Instrument Amplifier) rectifies the input range and amplify/alleviate input signal to match the input range of A/ D converter.
- **AI converter** conceives the rectified voltage from PGIA and transfers it into the corresponding digital data format.
- **Trigger/Clock control logic** enables/disables the whole process and determines acquisition timing interval.



AI Conversion Hardware Structure

B.1.2 Analog Input Ranges and Gains

The PCIE-1816/1816H can measure both unipolar and bipolar analog input signals. A unipolar signal can range from 0 to 10 V FSR (Full Scale Range), while a bipolar signal extends within ±10 V FSR. The PCIE-1816/1816H provides various programmable gain levels and each channel is allowed to set its own input range individually. Table B.1 lists the effective ranges supported by the PCIE-1816/1816H with gains.

Table B.1: Gains and Analog Input Range

Gain	Unipolar Analog Input Range	Bipolar Analog Input Range
0.5	N/A	±10 V
1	0 ~ 10 V	±5 V
2	0 ~ 5 V	±2.5 V
4	0 ~ 2.5 V	±1.25 V
8	0 ~ 1.25 V	±0.625 V

For each channel, choose the gain level providing the most optimal range that can accommodate the signal range you want to measure.

B.1.3 Analog Input Acquisition Mode

The PCIE-1816/1816H can acquire data in either single value or pacer mode.

■ Single Value Acquisition (Polling) Mode

The single value acquisition mode is the simplest way to acquire data. User can simply poll the data register of the desired channel to get the latest acquired value. Each analog input channel has its own dedicated data register (buffer) and in this mode the PCIE-1816/1816H updates each channel cyclically. The update rate is sampling rate/ num. of active channels.

■ Buffer Mode

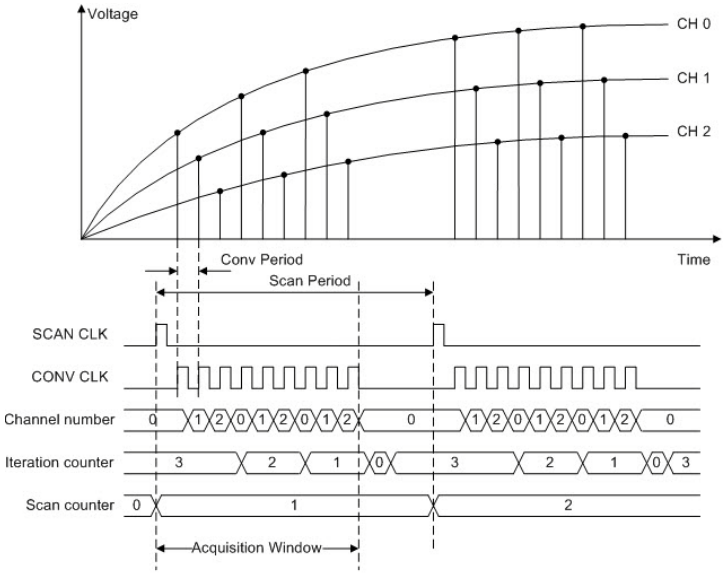
Adopt buffer mode to acquire data if you wanna accurately control the time interval between conversions. AI conversion clocks come from internal clock sources or external signals on connector. AI conversion starts when the clocks signal come in, and will not stop if the clocks are continuously sent. Conversion data is accumulated into the on-board AI buffer and waiting the transfer to PC memory. Further, you can specify Trigger to acquire the desired periods. We will discuss the detail in the next sections.

■ AI Data Acquisition Clock Timing

The PCIE-1816/1816H introduces a double-clock system, with SCAN clock and CONV clock, to generate efficient AI conversion clocks at dedicated timing. You can control acquisition timing interval precisely and just acquire the desired period. It can save the waste of PCI bandwidth with continuing acquisition and post data processing by filtering-out the redundant data beforehand. In this section, we will describe how it works and its timing reference in detail.

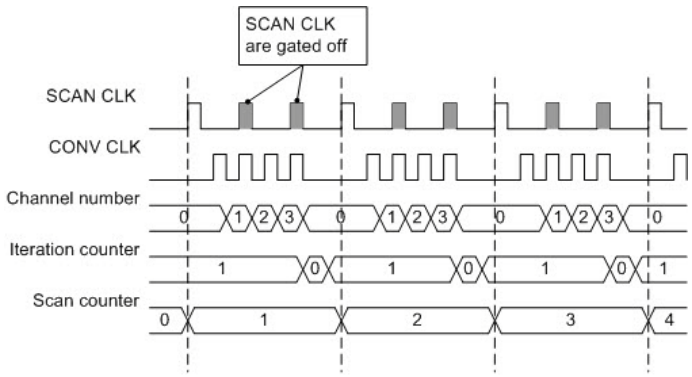
Double-Clock Procedure

Double clock procedure is the fundamental AI conversion mechanism of the PCIE-1816/1816H, regardless of which mode selected. The incoming SCAN CLK launches an acquisition period called Acquisition Window. The arriving CONV CLKs within the Acquisition Window will become an efficient AI conversion clock to trigger AI converter. The number of efficient CONV CLK depends on the number of active scanning (multiplex) channels and software-programed iteration counters. One scanning iteration is defined as the time auto-scan multiplexer routes input channels from Start channel to Stop channel once. On the other words, all the active channels are sampled once in a single iteration. After the iteration counter counts down to zero, the Acquisition Window will be disable automatically and wait for the next incoming SCAN CLK. The end of Acquisition Window resets the iteration counter to its user-specified value. Users can specify the iteration counter by software and read back the number of incoming SCAN CLKs from SCAN CLK counter.

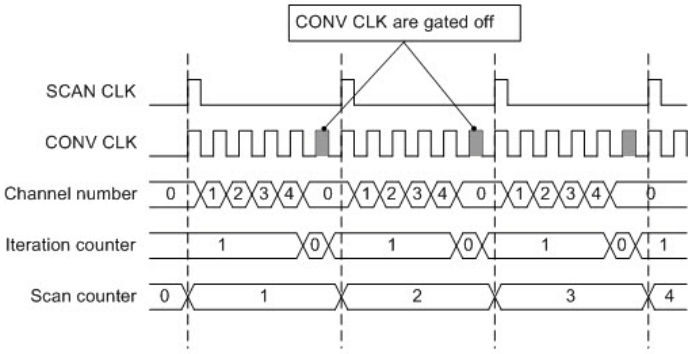


Double Clock timing Diagram

Once the acquisition procedure inside Acquisition Windows is set, the incoming CLKs must fit in the user-specified acquisition sequence, or the CLKs may be gated off. Refer to the following figures for more details.

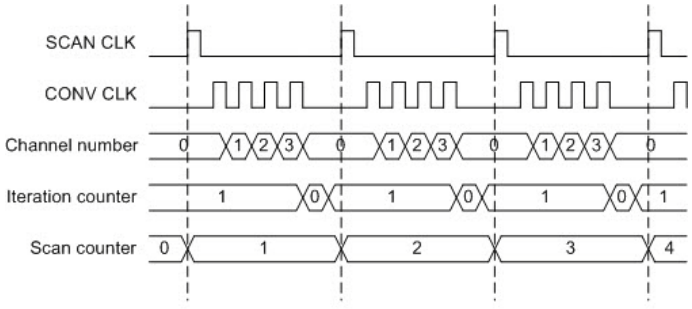


SCAN CLK is too fast

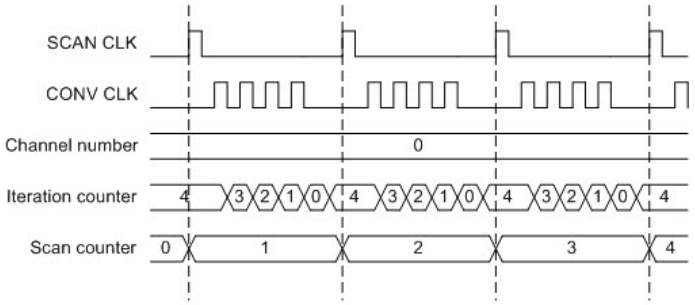


CONV CLK is too fast

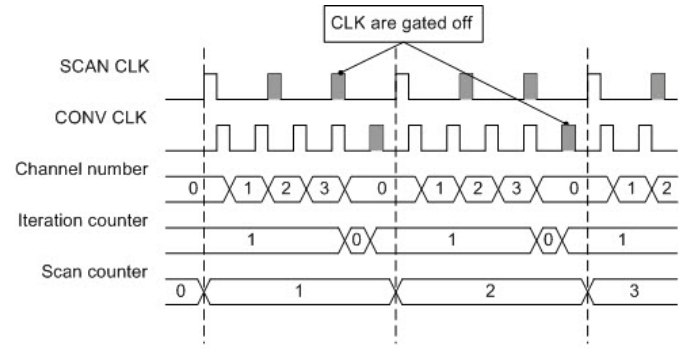
Other scanning procedure applications timing diagram.



Single Iteration



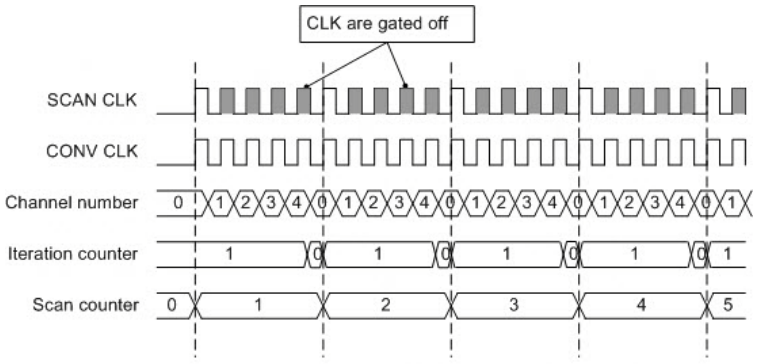
Multiple Iteration timing with fixed channel



Improperly matched SCAN CLK and CONV CLK

- **Single Clock Source Driving**

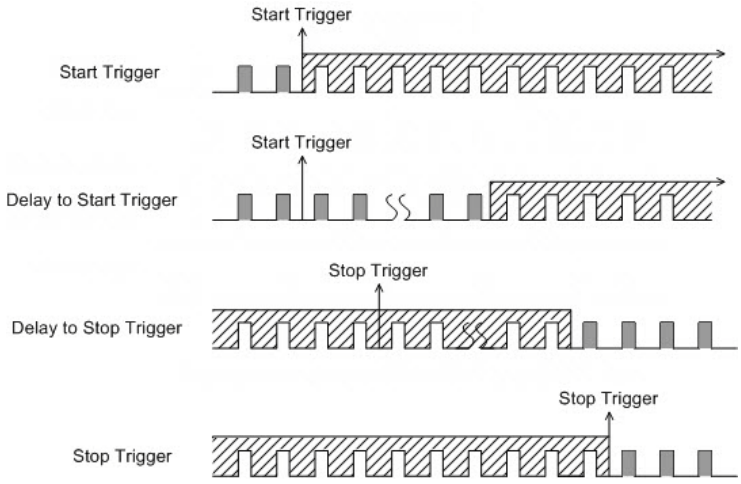
Single clock source driving is a specific function well-suited for consecutive data acquisition while there is only one clock signal available. CONV CLKs will be internally routed as SCAN CLKs. And the external SCAN CLKs input will not be accepted. Figure describes how it works.



Single clock source driving both CLKs

B.1.4 AI Trigger Modes

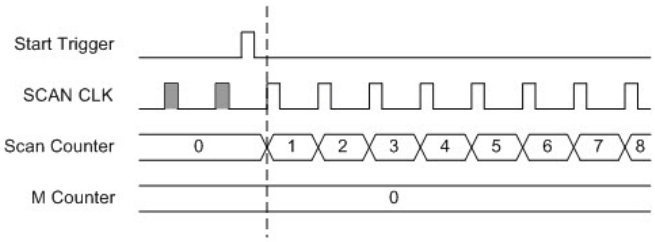
The PCIE-1816/1816H supports four trigger modes and pause function. User can start or stop the operation by trigger mode selection. An extra 32-bit counter is dedicated to delay-trigger mode and about-trigger mode, and user can set it as the number of delay SCAN CLKs before trigger or the number of holding SCAN CLKs after trigger. Figure shows the four different trigger modes.



Trigger Modes

- **Start Trigger Acquisition Mode**

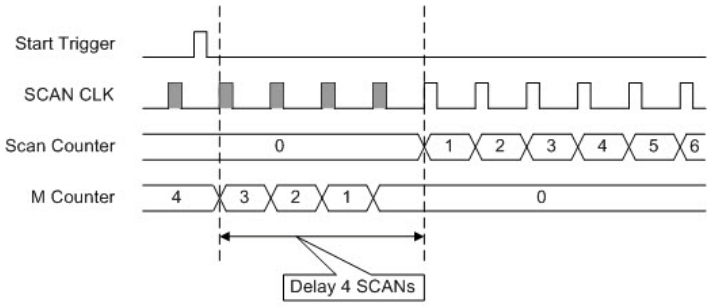
Start trigger acquisition starts when the PCIE-1816/1816H detects the trigger event and stops when you stop the operation. The SCAN CLKs before Trigger will be blocked out. You can set post-trigger acquisition mode by software.



Start Trigger (M = 0)

Delay to Start Trigger Acquisition Mode

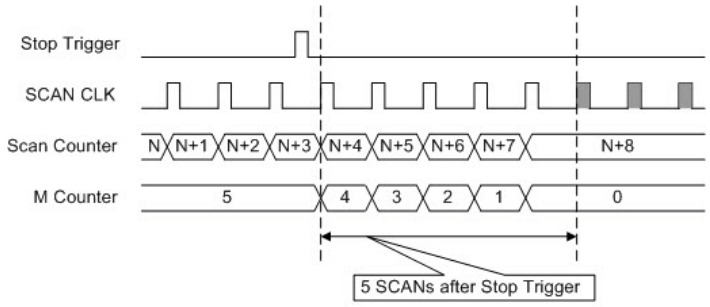
In delay to start trigger mode, data acquisition will be activated after a preset delay number of SCAN CLKs has been taken after the trigger event. User can set the delay number of SCAN CLKs by a 32-bit counter. Delay to start trigger acquisition starts when the PCIE-1816/1816H detects the trig-ger event and stops when you stop the operation.



Delay to Start Trigger (M = 4)

Delay to Stop Trigger Acquisition Mode

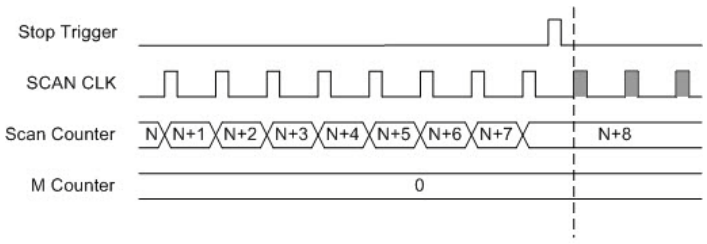
When you want to acquire data both before and after a specific trigger event occurs, users should take advantage of the delay to stop trigger mode. First designate the size of the allocated memory and the amount of samples to be snatched after the trigger event happens. The trigger acquisition starts when the first SCAN CLK signal comes in. Once a trigger event happens, the on-going data acquisition will continue until the designated amount of SCAN CLKs have been reached. When the PCIE-1816/1816H detects the selected about-trigger event, the card keeps acquiring the preset number of samples, and keeps them in the buffer.



Delay to Stop Trigger (M = 5)

Stop Trigger Acquisition Mode

Stop trigger mode is a particular application of about-trigger mode. Use pre-trigger acquisition mode when you want to acquire data before a specific trigger event occurs. Stop-trigger acquisition starts when you start the operation and stops when the trigger event happens.



Stop Trigger (M = 0)

B.1.5 AI SCAN/CONV Clock Source

The PCIE-1816/1816H can adopt both internal and external clock sources to accomplish pacer acquisition. You can set the clock and trigger sources conveniently by software. The figure can help you understand the routing route of clock and trigger generation.

SCAN Clock

- Internal AI SCAN clock derived from 32-bit divider
- External AI SCAN clock from terminal board
- External AI CONV clock from terminal board

■ Internal AI SCAN Clock

The internal AI SCAN clock uses a 100 MHz time base divided by a 32-bit divider programmable by software. You can program SCAN clock source to internal and its frequency the clock source as internal and the frequency, 500 KS/s maximum for the PCIE-1816 multi-channel and 1 MS/s maximum for the PCIE-1816H multi-channel, to activate AI conversions. To ensure system stability, SCAN clock frequency should be less or equal to CONV clock.

■ External AI SCAN Clock

The external AI SCAN clock is useful when you want to execute acquisitions at rates not available from the internal AI SCAN clock, or when you want to pace at uneven intervals. Acquisitions will start the rising edge of the external AI SCAN clock input. And the frequency for PCIE-1816 and PCIE-1816H should be always limited under 500 KHz and 1 MHz. The exceeding frequency may result in data loss or unexpected data acquisition.

■ External AI CONV clock

This setting is useful when single external clock source is available. Instead of hardwire, the internal routing can protect signals from different line transmission delay.

CONV Clock

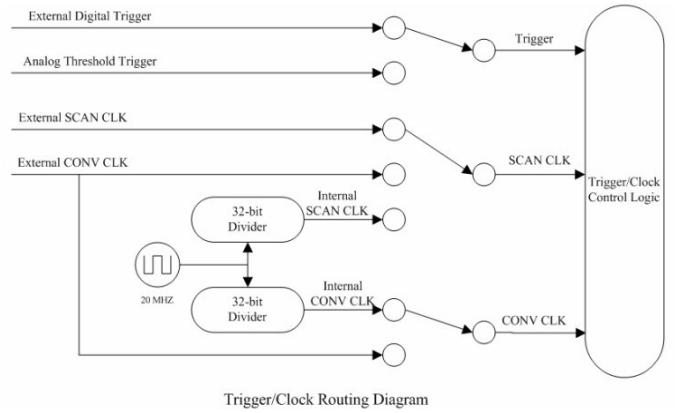
- Internal AI CONV clock derived from 32-bit divider
- External AI CONV clock from terminal board

■ Internal AI CONV Clock

The same as internal SCAN clock, the internal AI CONV clock applies 100 MHz time base accompanied with 32-bit divider. The maximum frequency is 500 KS/s. According to the sampling theory (Nyquist Theorem), you must specify a frequency that is at least twice as fast as the input's highest frequency component to achieve a valid sampling. For example, to accurately sample a 20 kHz signal, you have to specify a sampling frequency of at least 40 kHz. This consideration can avoid an error condition often know as aliasing, in which high frequency input components appear erroneously as lower frequencies when sampling.

- **External AI CONV Clock**

The external AI CONV Clock is convenient in uneven sampling internal. AI conversion will start by each arriving rising edge. The sampling frequency is always limited to a maximum of 500 KHz.



Trigger/Clock Routing Diagram

B.1.6 AI Trigger Source

The PCIE-1816/1816H supports the following trigger sources for start, delay to start, delay to stop, stop trigger acquisition modes:

- External digital (TTL) trigger
- Analog threshold trigger

With PCIE-1816/1816H, user can also define the type of trigger source as rising-edge or falling-edge. These following sections describe these trigger sources in more detail.

- **External Digital (TTL) Trigger**

For analog input operations, an external digital trigger event occurs when the PCIE-1816/1816H detects either a rising or falling edge on the External AI TTL trigger input. The trigger signal is TTL compatible.

- **Analog Threshold Trigger**

For analog input operations, an analog trigger event occurs when the PCIE-1816/1816H detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). User should connect analog signals from external device or analog output channel on board to external input signal ATRG0/1. On the PCIE-1816/1816H, the threshold level is set using a dedicated 16-bit DAC. By software, you can program the threshold level by writing a voltage value to this DAC; this value can range from -10 V to +10 V.

Table B.2: Analog Input Data Format

AI Code		Mapping Voltage	
Hex.	Dec.	Unipolar	Bipolar
0000 h	0 d	0	- FS/2
7FFF h	32767 d	FS/2 - 1 LSB	- 1LSB
8000 h	32768 d	FS/2	0
FFFF h	65535 d	FS - 1 LSB	FS/2 - 1 LSB
1 LSB		FS/65536	FS/65536

Table B.3: Full Scale Values for Input Voltage Ranges				
Gain	Unipolar		Bipolar	
	Range	FS	Range	FS
0.5	N/A	N/A	± 10 V	20
1	0 ~ 10 V	10	± 5 V	10
2	0 ~ 5 V	5	± 2.5 V	5
4	0 ~ 2.5 V	2.5	± 1.25 V	2.5
8	0 ~ 1.25 V	1.25	± 0.625 V	1.25

B.2 PCIE-1816/1816H Analog Output Operation

The PCIE-1816/1816H card provides two 16-bit multi-range analog output (D/ A) channels. This section describes the following features:

- Analog output ranges
- Analog output operation modes
- Synchronous Analog output waveform
- AO clock sources
- AO Trigger sources
- Analog Output Data Format

B.2.1 Analog Output Ranges

The PCIE-1816/1816H provides two 16-bit analog output channels, both of which can be configured internally to be applicable within 0 ~ 5 V, 0 ~ 10 V, ± 5 V, ± 10 V output voltage range. Otherwise, users can use external reference voltage to apply 0 ~ x V or ± x V output range, where the value x is from -10 to +10. Users can configure the output range during driver installation or in software programming.

B.2.2 Analog Output Operation Modes

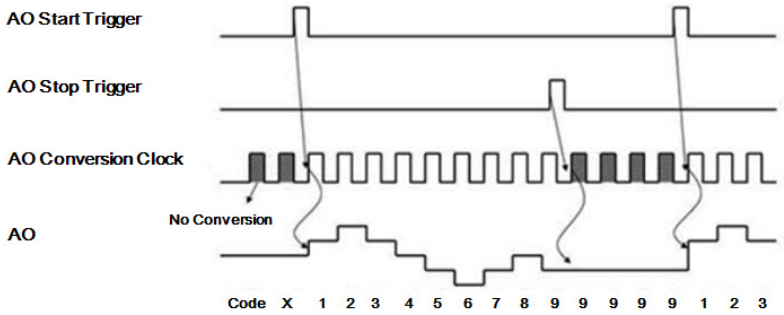
- **Single Value Operation Mode**

The single value conversion mode is the simplest way for analog output operation. Users can set the mode of each channel individually. Then users just need to use software to write output data to specific register. The analog output channels will output the corresponding voltage immediately. In the single value operation mode, users need not set any clock source and trigger source, but only output voltage range.

- **Waveform Mode**

In waveform mode, all AO channels can change output voltage at the same time. Users can accurately control the update rate (up to 3 MS/s) between conversions of individual analog output channels, and takes full advantage of the PCIE-1816/1816H. In this mode you can specify a clock and trigger source and either of the two analog output channels to work in this mode.

Before operating in this mode, users need to set the clock and trigger source first, and then generate the output data stored in the memory buffers of host PC. The host computer then transfers that data to the DACs' buffers on PCIE-1816/1816H. When PCIE-1816/1816H detects a trigger, it outputs the values stored in its buffer. When the buffer's storage decreases, the card sends an interrupt request to the host PC which in turn sends samples to the buffer. This output operation will repeat until either all the data is sent from the buffers or until you stop the operation. If the two AO channels are both operating in continuous output mode, the data in buffer will be sent in an interlaced manner, i.e. the "Even Address" samples in the buffer are sent to AO channel 0, while the "Odd Address" samples to AO channel 1.



Waveform Mode Output

B.2.3 AO Clock Sources

The PCIE-1816/1816H can adopt both internal and external clock sources for pacing the analog output of each channel:

- Internal AO output clock with 32-bit Divider
- External AO output clock from connector

The internal and external AO output clocks are described in more detail as follows:

- Internal AO Output Clock

The internal AO output clock applies a 100 MHz time base divided by a 32-bit counter. Conversions start on the rising edges of counter output. Through software, user can specify the clock source and clock frequency to pace the analog output operation. The maximum frequency is 3 MS/s.

- External AO Output Clock

The external AO output clock is useful when you want to pace analog output operations at rates not available with the internal AO output clock, or when you want to pace at uneven intervals. Connect an external AO output clock to the pin and then the conversions will start on input signal's rising edge. You can use software to specify the clock source as external. The maximum input clock frequency is 3 MS/s.

B.2.4 AO Trigger Sources

The PCIE-1816/1816H supports External digital (TTL) trigger to activate AO conversions for waveform mode. An external digital trigger event occurs when the PCIE-1816/1816H detects either a rising or falling edge on the External AO TTL trigger input signal from the pin of connector. User can define the type of trigger source as rising-edge or falling-edge by software. The trigger signal is TTL-compatible.

Table B.4: Analog Output Data Format

AO Code		Mapping Voltage	
Hex.	Dec.	Unipolar	Bipolar
0000 h	0 d	0	- FS/2
7FFF h	32767 d	FS/2 - 1 LSB	- 1LSB
8000 h	32768 d	FS/2	0
FFFF h	65535 d	FS - 1 LSB	FS/2 - 1 LSB
1 LSB		FS/65536	FS/65536

Table B.5: Full Scale Values for Output Voltage Ranges

Reference Source	Unipolar		Bipolar	
	Range	FS	Range	FS
Internal	0 ~ 5 V	5	± 5 V	10
	0 ~ 10 V	10	± 10 V	20
External	0 ~ x V	x	± x V	2x