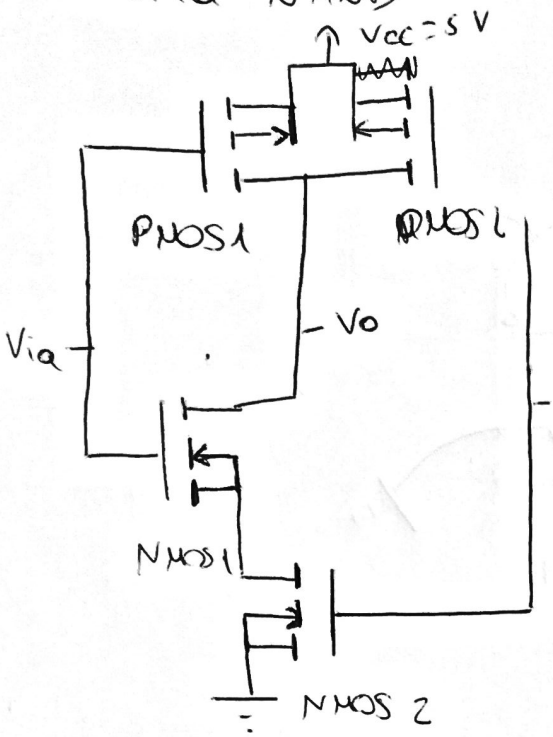
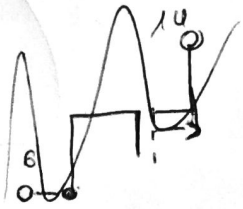
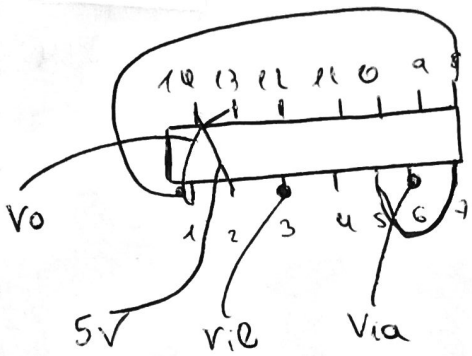
Puerta NAND



NMOS 1 (6, 7, 8)

NMOS 2 (3, 4, 5)





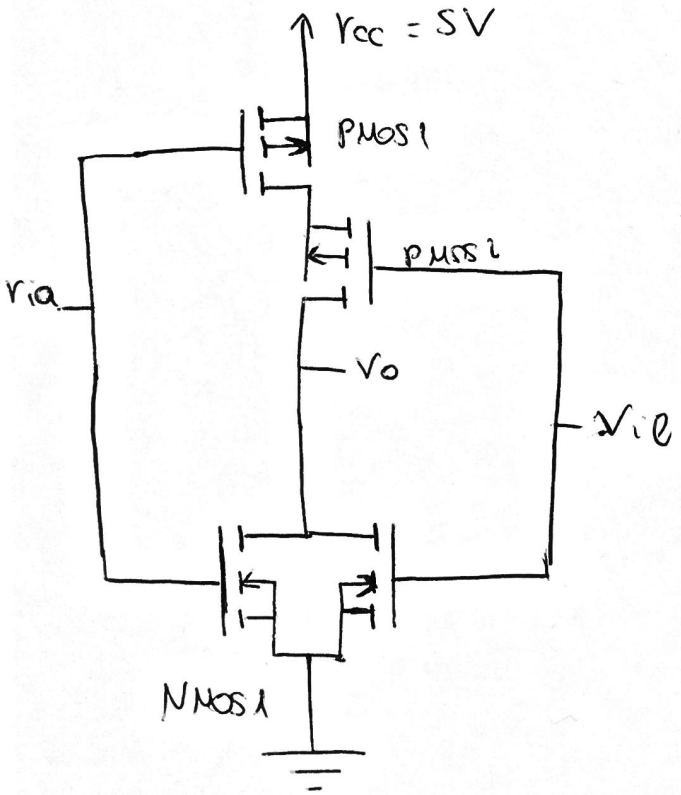
(1) Fuente NOS 1 → Dr NMOS 2

(2) Dr PMOS 1 → Dr PMOS 2

↓

(3) Dr NMOS 1

Puerta NOR



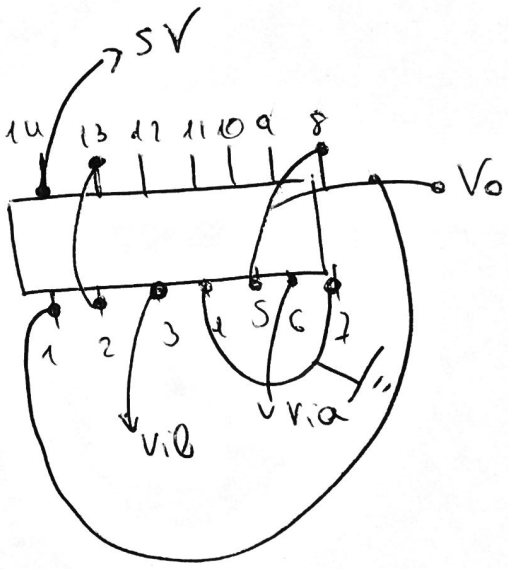


Figura 7.3