Day 8

Friday, September 20, 2013 10:01 AM

The SCRAM

- memory 16 x 8 bit "RAM"
- instruction OR data
- two more registers
  - AC accumulator 8-bit arithmatic
  - PC Program Counter 4-bit address of the next instruction

Instructions:

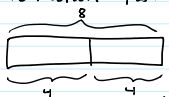
LDA address: load accumulator
AC ← M[addr]

JMP address: sets program counter
PC ← address

Address	Instruction		In Memory
0	LDA	4	0001 0100
1	ADD	5	0101 0101
2	STA	4	0011 0100
3	JMP	0	0111 0000
4	DAT	0	0000 0000
5	DAT	1	0000 0001

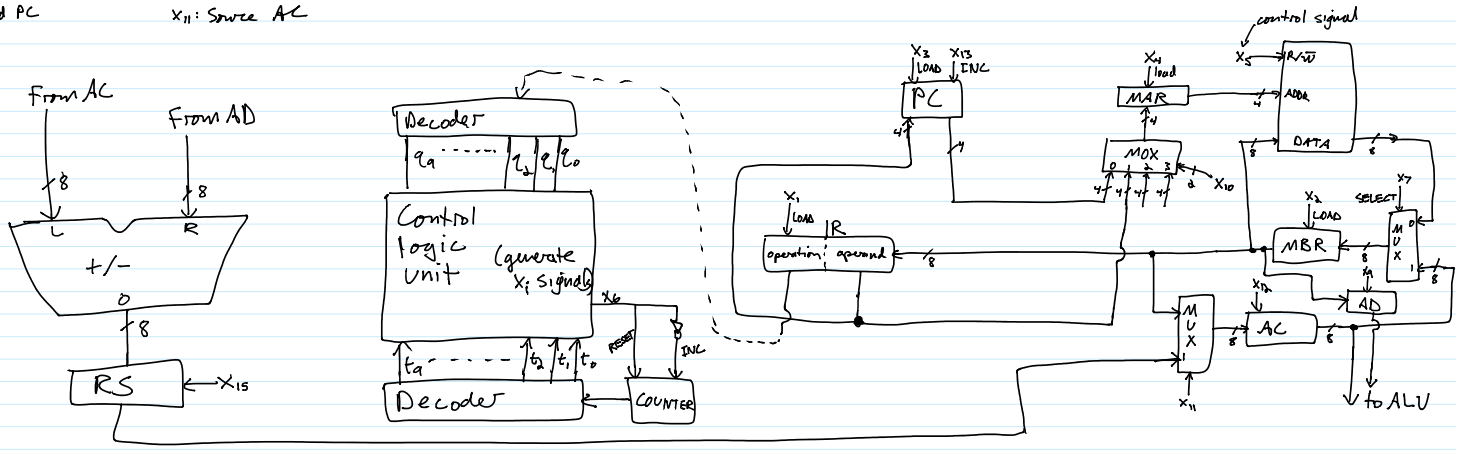
pseudo-instruction

Instruction Format



Build a circuit to make this run

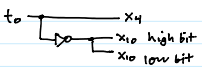
x_5: read / write memory
x_4: load MAR
x_{10}: source for MAR
x_2: load MBR
x_7: source for MBR
x_3: load PC
x_{13}: PC++
x_1: Load IR
x_6: timer control
x_{12}: Load AC
x_{11}: Source AC



Fetch - Execute Cycle

instruction Fetch

t_0 MAR ← PC
$x_{10}=00$, $x_4=1$

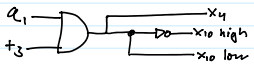


t_1 MBR ← MEM, PC ← PC+1
$x_7=0$ $x_2=1$, $x_{13}=1$

t_2 IR ← MBR t_2 — x_1
$x_1=1$

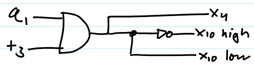
LDA instruction

$q_1 t_3$: MAR ← IR (low)
$x_{10}=01$, $x_4=1$



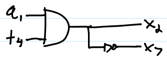
$q_1 t_3$: MAR ← IR (low)

$x_{10} = 01$, $x_4 = 1$



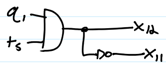
$q_1 t_4$: MBR ← MEM

$x_7 = 0$ $x_2 = 1$



$q_1 t_5$: AC ← MBR

$x_{11} = 0$, $x_{12} = 1$



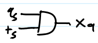
ADD Instruction AC ← AC + M[x]

$q_5 t_3$ MAR ← IR (low)

$q_5 t_4$ MBR ← MEM

$q_5 t_5$ AD ← MBR

$x_9 = 1$



$q_5 t_6$ RS ← AC + AD

$x_{15} = 1$

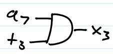
$q_5 t_7$ AC ← RS

$x_{11} = 1$, $x_{12} = 1$

JMP Instruction PC ← IR (low)

$q_7 t_3$ PC ← IR (low)

$x_3 = 1$



SUB ....

JMZ ...

.s → ".z" → .scram

text instruction bits