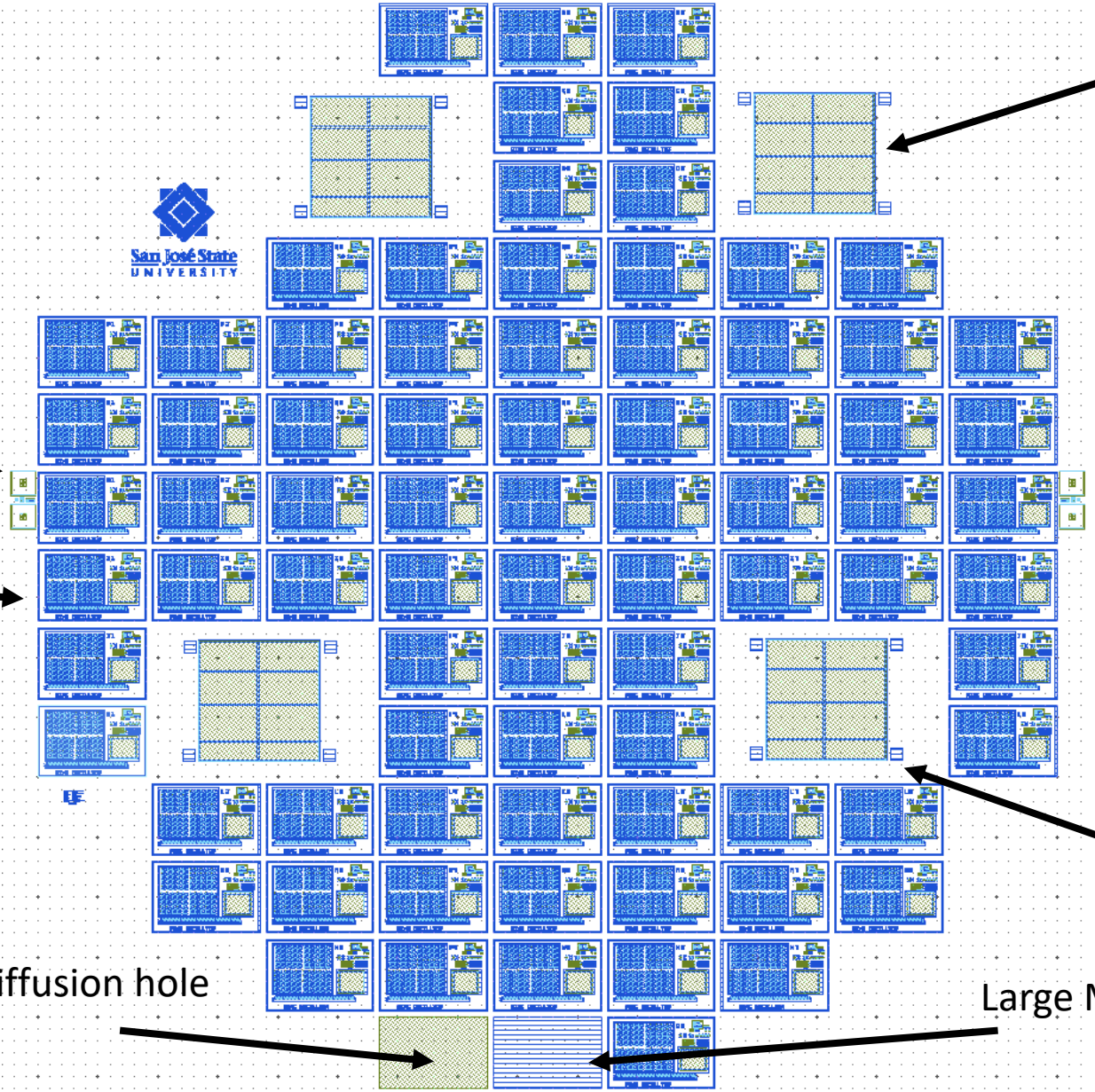
2 MASK NMOS Mask SET Documentation

D. W. Parent

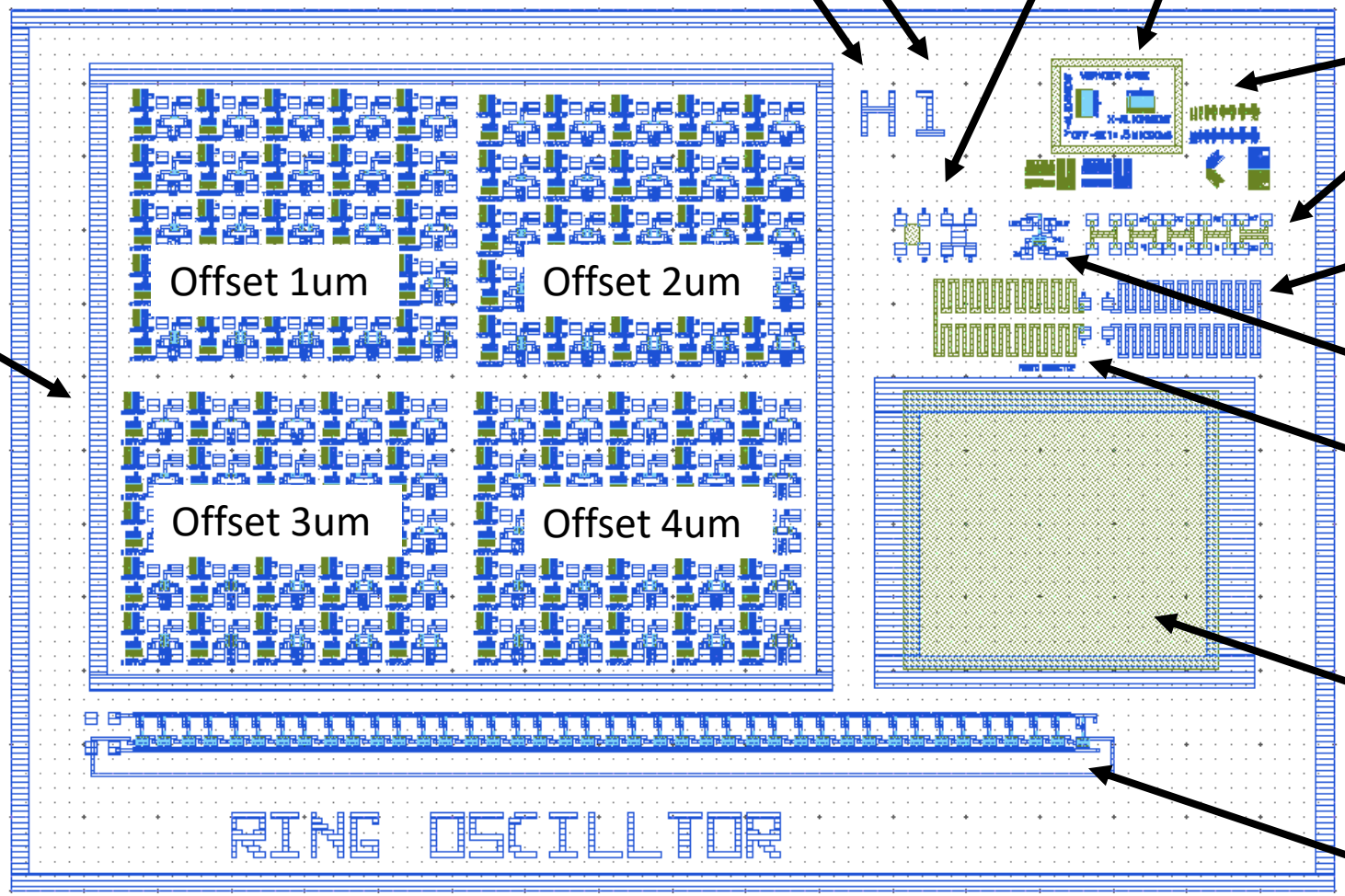
2MASK NMOS Set

Mask 1: N-type Diffusion

Mask 2: Metal 1 (Al)



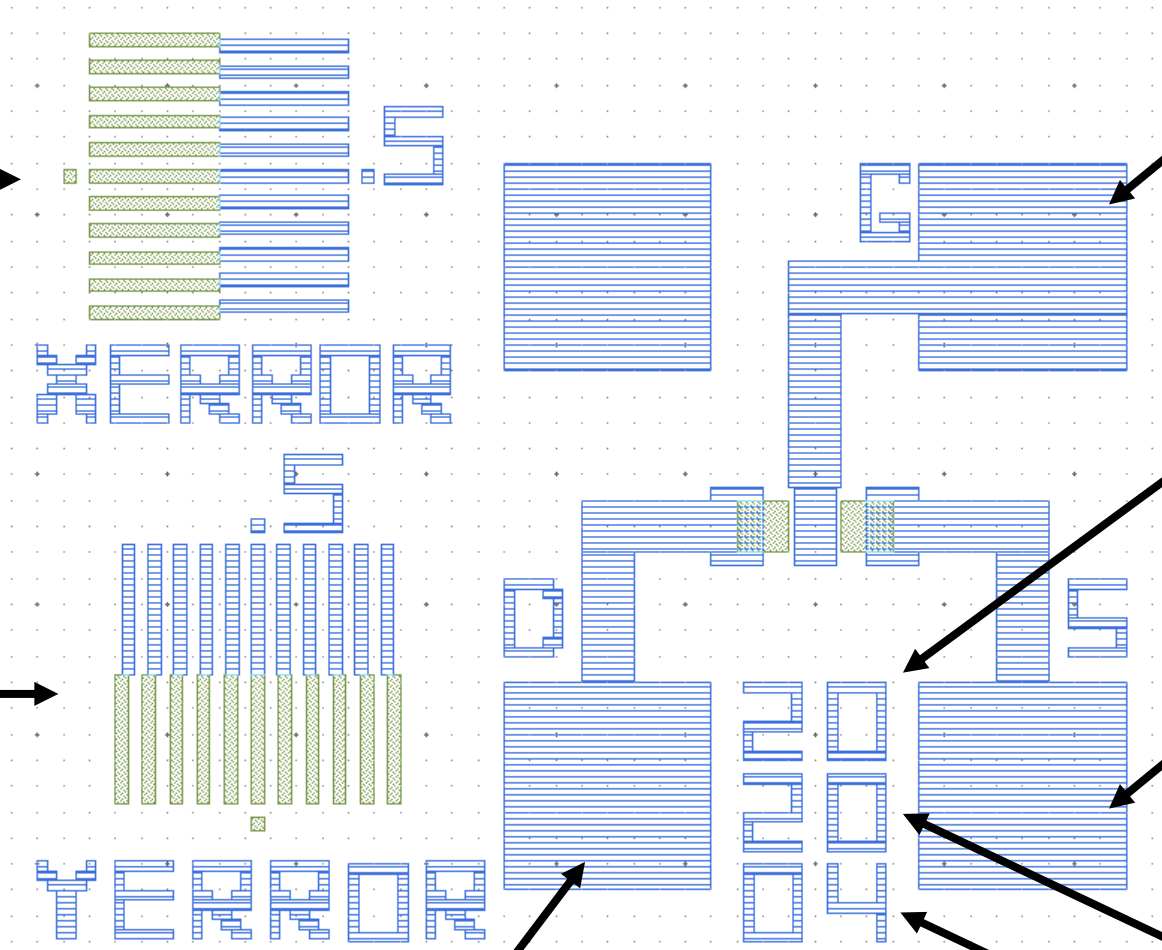
2MASK NMOS Set: Test Cells



Sample NMOS Transistor

Mask one (yellow) are holes in the chrome mask so the PR is removed from the yellow areas.

Mask two (blue) are made of chrome mask so the PR is retained in the blue areas.



Vernier Gauge
For x registration error

Vernier Gauge
For y registration error

Gate

Width

Source

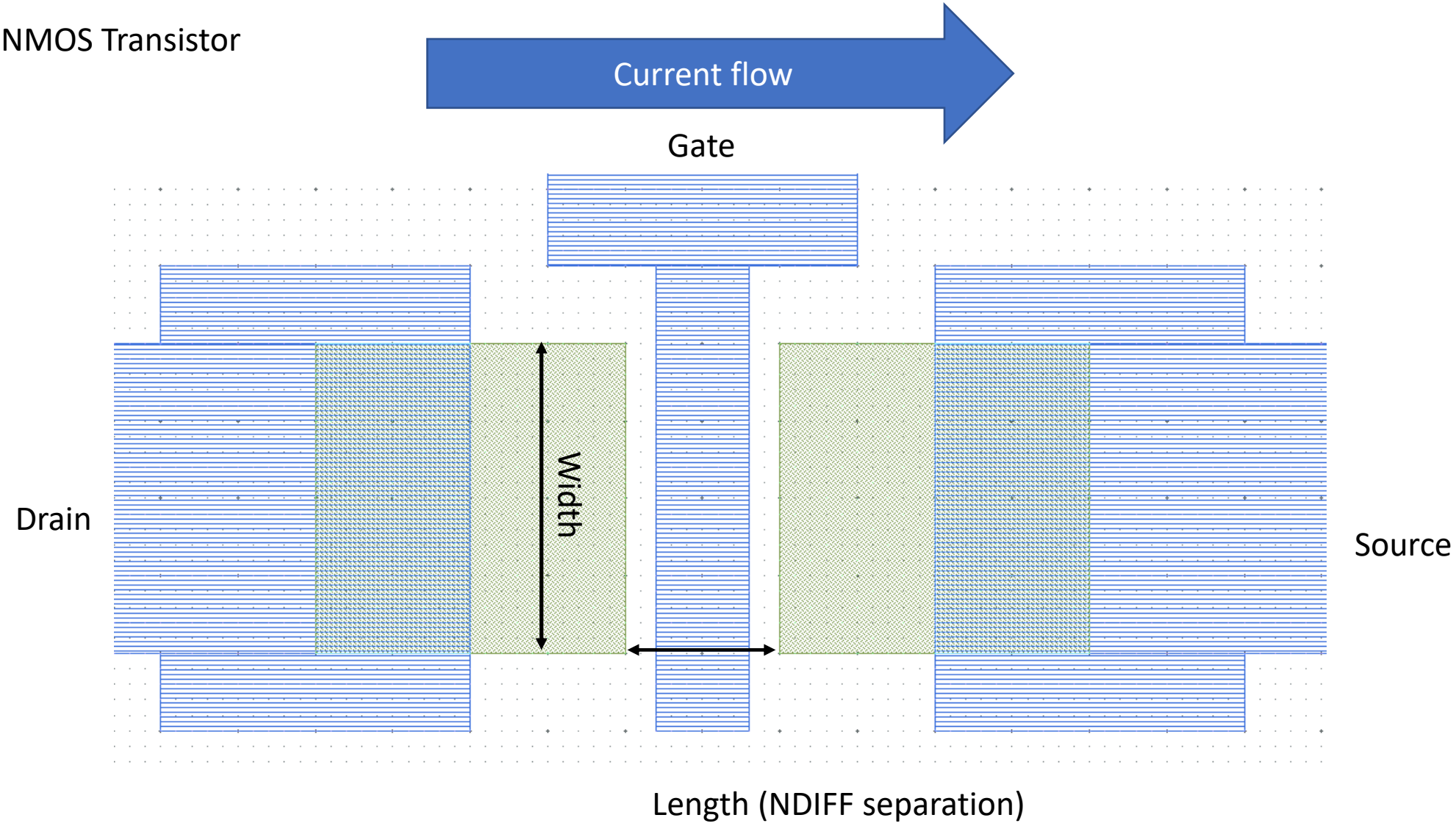
Length

Drain

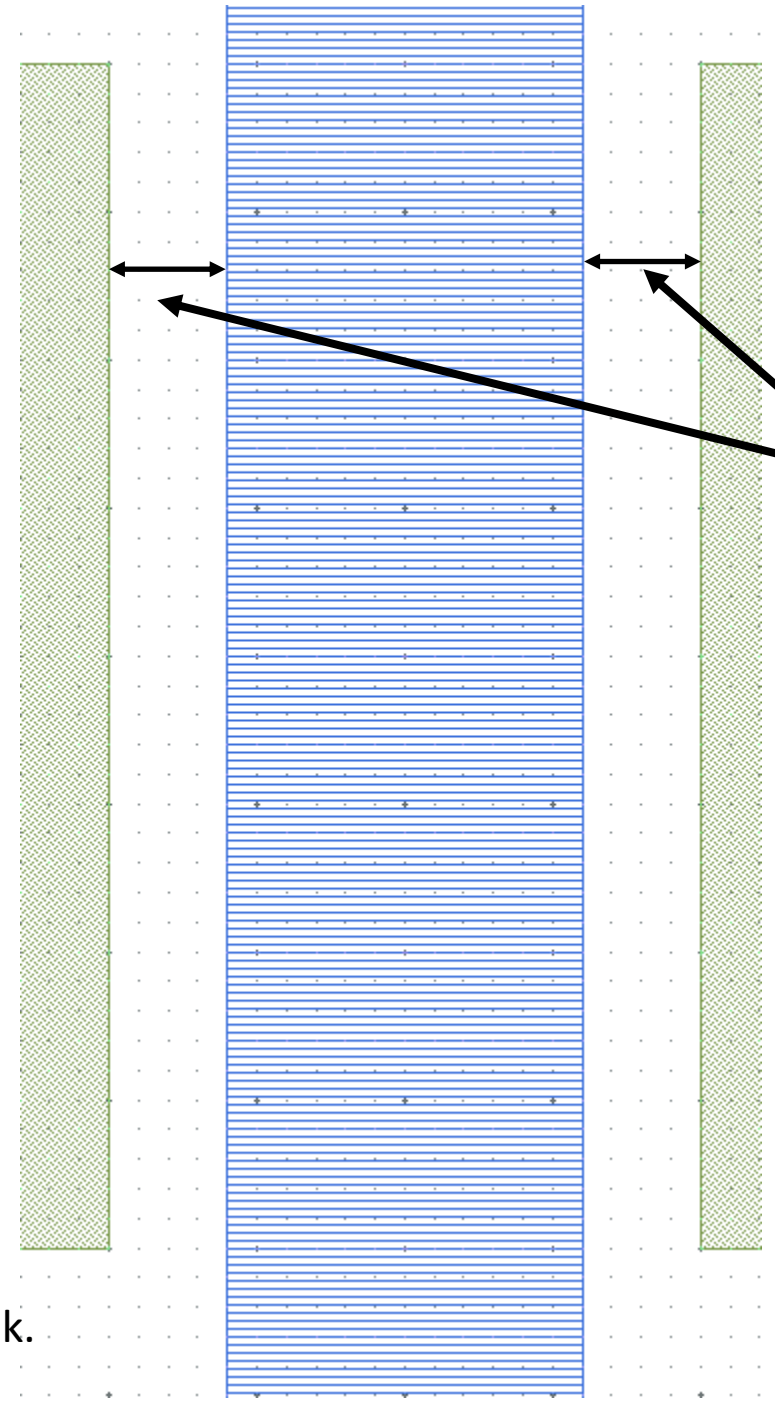
Offset from drain or source

The body connection is taken from the bottom of the wafer.

Blow up NMOS Transistor



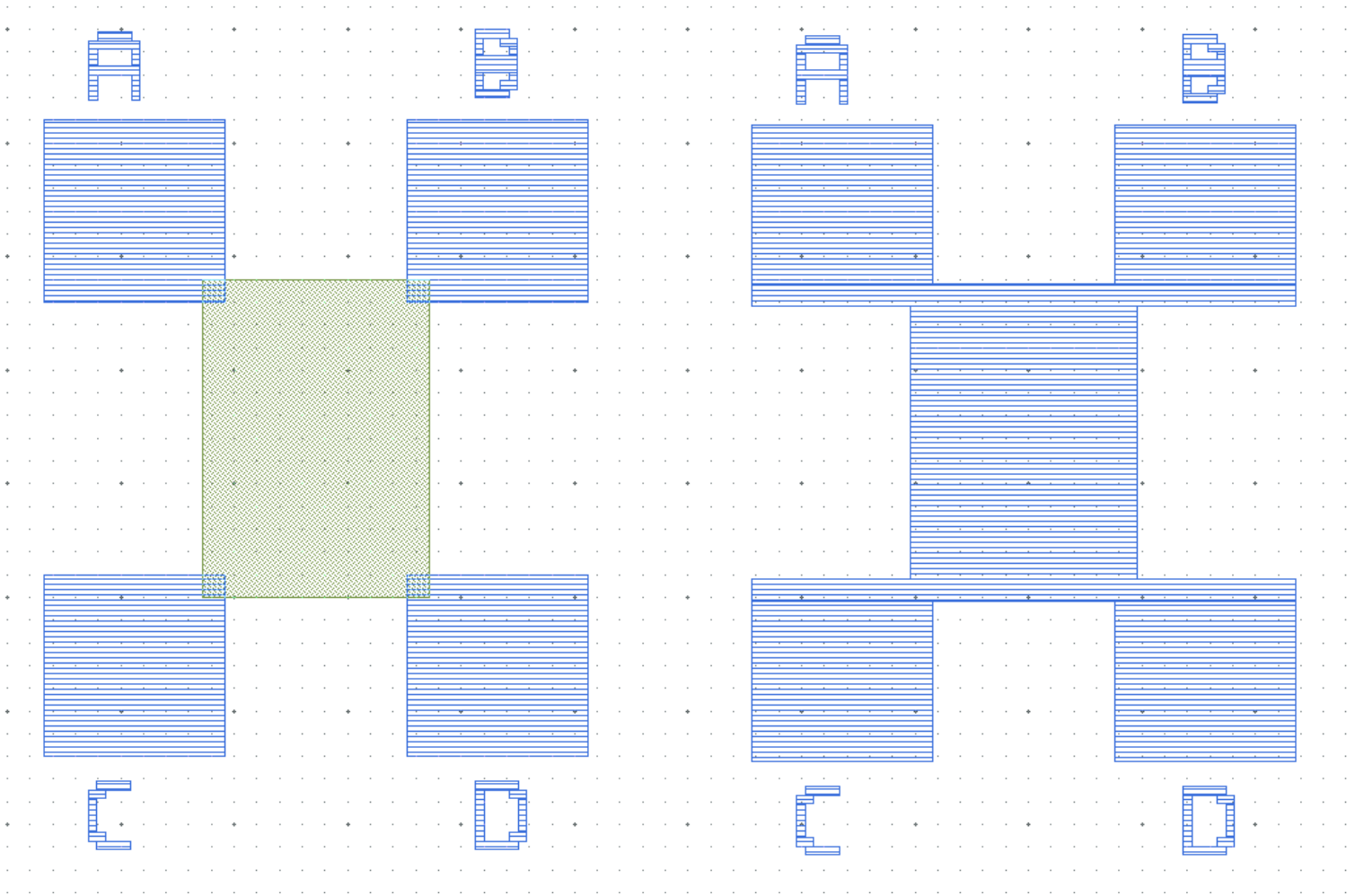
The offset is added to prevent the
X direction alignment error from having
the drain or source be shorted by the gate.



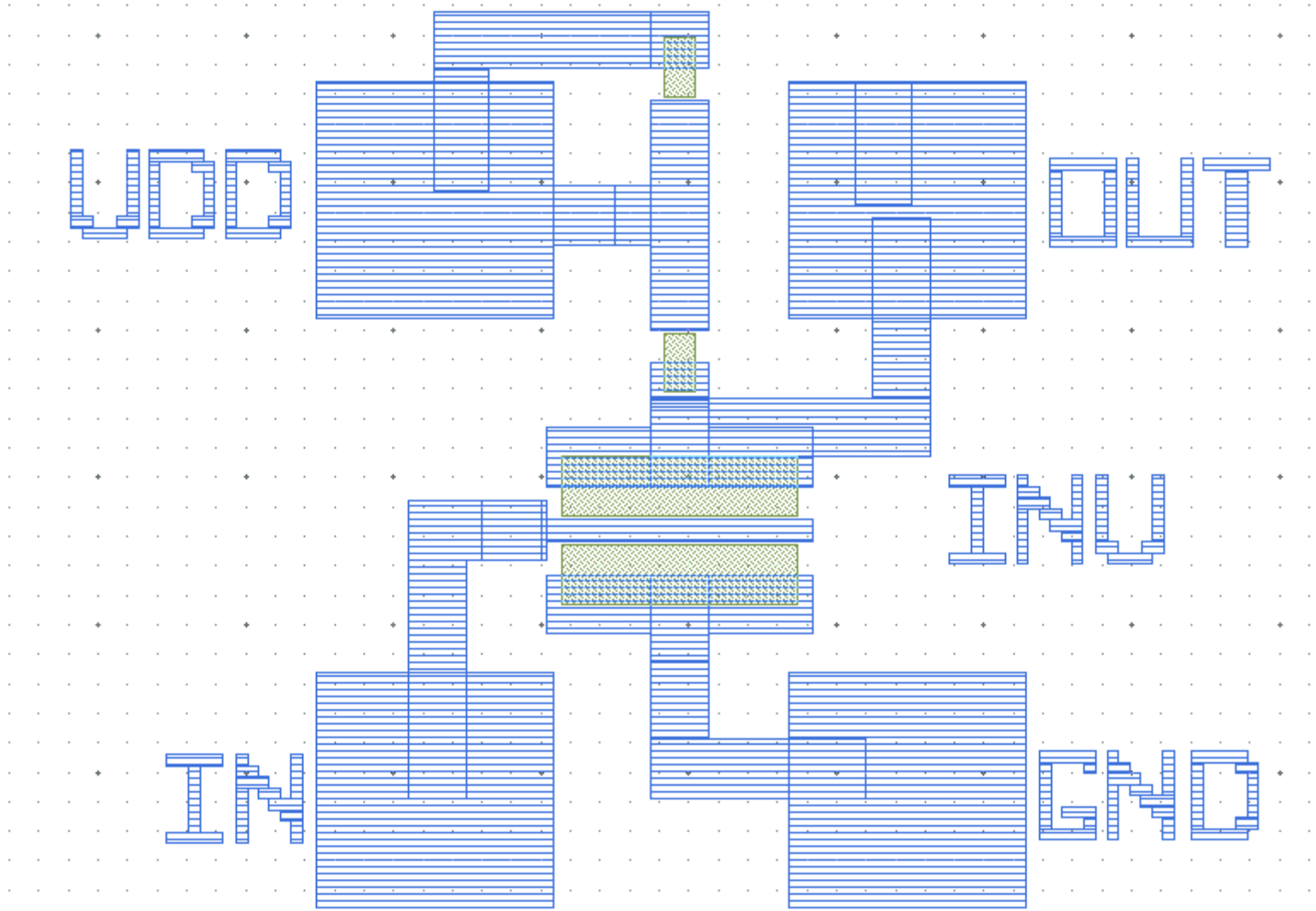
Mask 2 with –x alignment error that
Puts gate into drain area.

This error is due to the fact this
process does not have a contact mask.

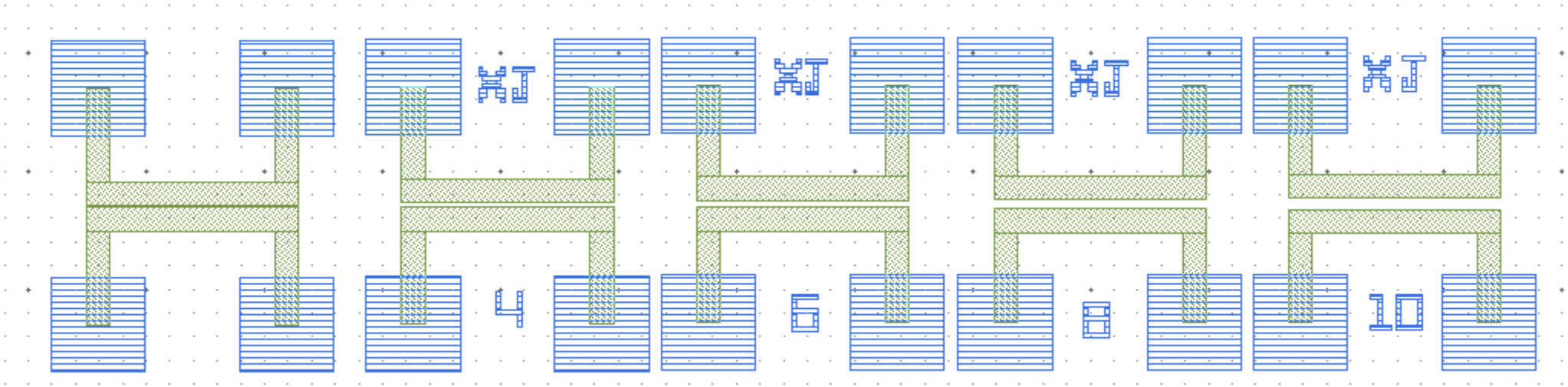
Van Der Paw sheet resistance structures for NDIFF and metal 1



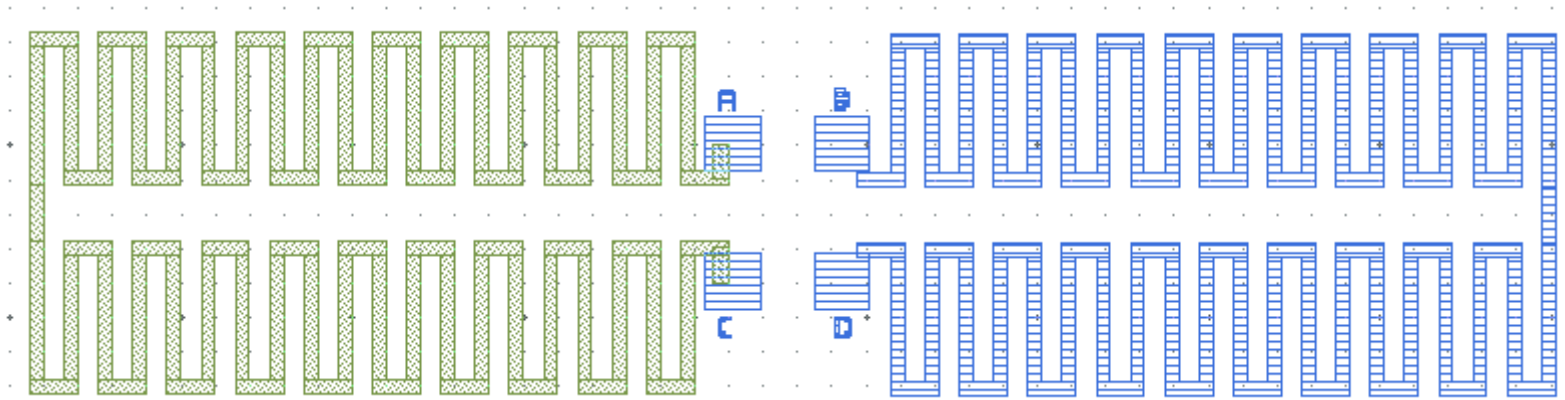
Enhancement mode NMOS inverter



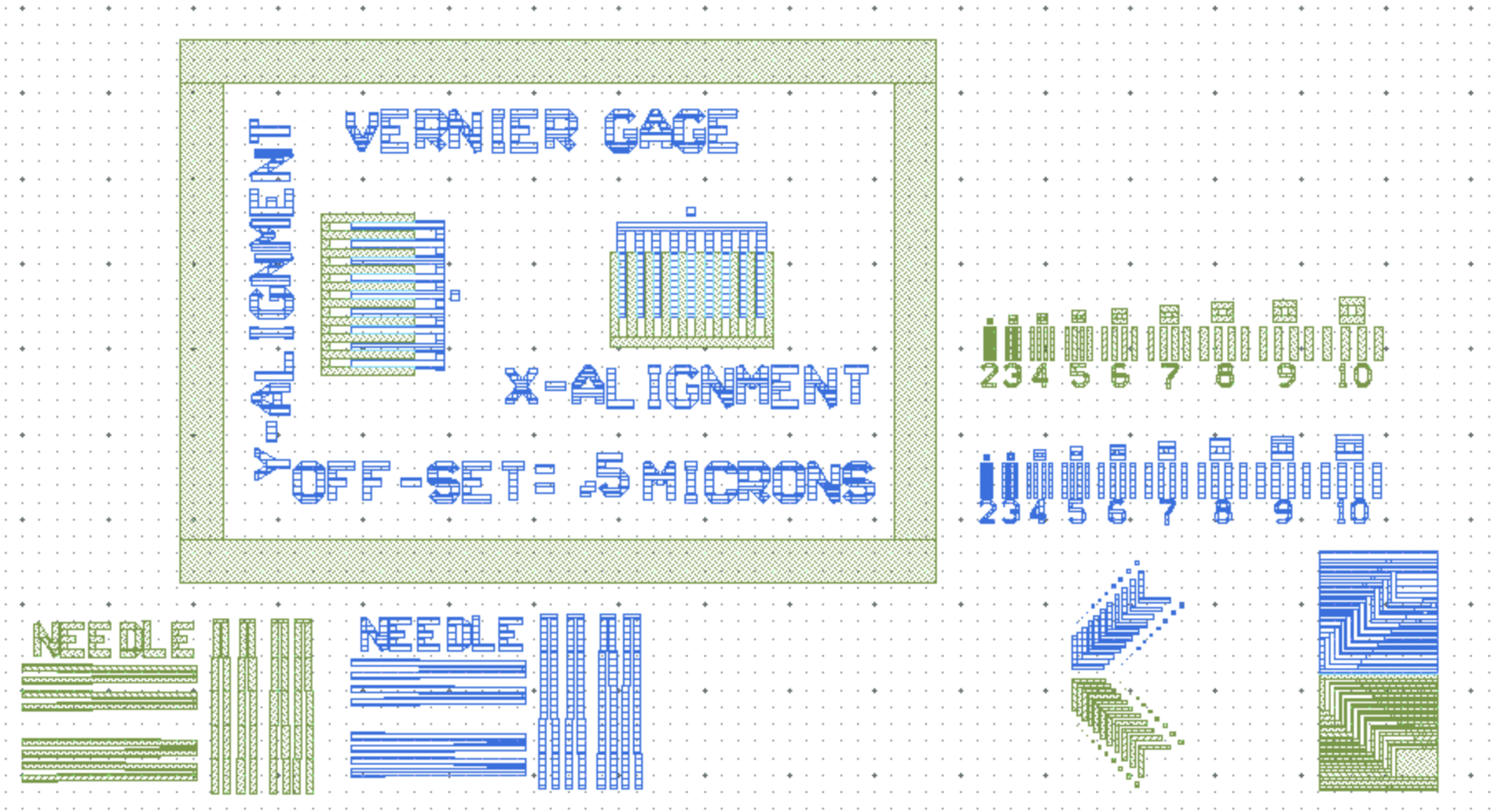
Lateral
Junction
depth
measurement
.



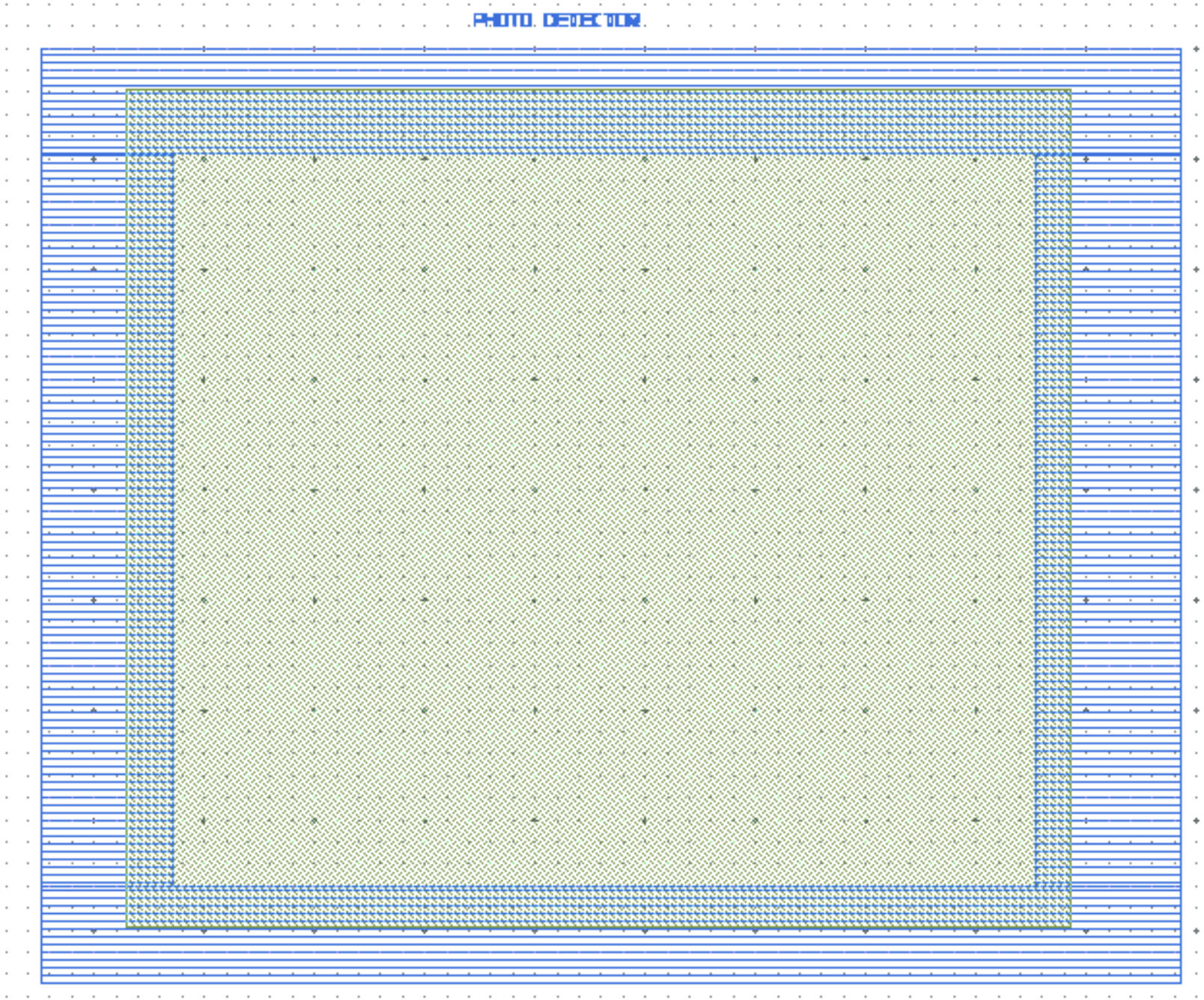
NDIFF and Metal 1 meander resistance test structures.



PL test structures



N+ on top P on bottom Photodetector



41 inverter ring oscillator.