Improvements to a Microelectronic Design and Fabrication Course

David Parent, *Member, IEEE*, Eric Basham, *Member, IEEE*, Yasser Dessouky, Stacy Gleixner, Gregory Young, and Emily Allen

***Abstract*—This paper presents improvements made to a complimentary metal–oxide–semiconductor (CMOS) fabrication laboratory course to increase student learning and student impact (enrollment). The three main improvements to the course discussed include: 1) use of a two-mask MOS process that significantly reduced the time students took previously to design, fabricate, and verify the electrical properties of a metal–oxide–semiconductor field-effect transistor (MOSFET) process; 2) students' use of a semicustom integrated circuit (IC) design that significantly reduced the average design and processing time of previous years; and 3) development and implementation of a system of course prerequisites, which allowed a larger number of students to enroll in the course.**

***Index Terms*—Complimentary metal–oxide–semiconductor (CMOS) fabrication, electronic design automation (EDA) software, multidisciplinary, prerequisites, semicustom analog design flow.**

I. Introduction

THREE years ago the authors introduced a CMOS processing course (EE/MatE167, Microelectronics Manufacturing Methods) to seniors and graduate students in chemical, electrical, industrial, materials, and microelectronic-processing engineering (MPE) at San Jose State University (SJSU) [1]. This course was developed as part of a NSF grant to develop a microelectronics-manufacturing program, and it covered two of the most important factors for graduating Microelectronic-Process Engineers to know, as identified by representatives of the semiconductor fabrication industry [2]: complementary metal–oxide–semiconductor (CMOS) circuit fabrication techniques and statistical process control (SPC). The other factors identified by Kerns [2], such as device physics, are covered in other courses offered by the Chemical, Electrical and Materials Engineering departments in the SJSU College of Engineering.

Even though student feedback gave indications of the success of the course in teaching students CMOS fabrication and SPC, one realized that student learning could be improved. Instructors also became aware that student impact needed to be increased. Based on class observations, student evaluations, and discussions during staff meetings, several problems and solutions were identified related to student learning and student impact. This paper will first discuss the problems related to student learning and impact, and then present the solutions developed to address these problems. Finally, the revised laboratory activities to implement the laboratory improvements will be presented.

A. Problems Related to Student Learning

- The seven-mask CMOS process used in the course was too ambitious for a lab that only met 14 times during the semester. There was not sufficient time for students to design, fabricate, and test full custom CMOS circuits using the previous process. Given the time constraints, students were not involved in circuit or process design, a situation that was taking away from students the sense of ownership for the work they did in the lab. This situation needed to be improved for experience had proven that when students are able to work on their own designs, they take ownership of the lab work, have more pride in their work, invest more effort in the lab, and thus learn more.
- Having students process a seven-mask CMOS wafer set every semester was extremely time consuming. The excessive time spent fabricating the wafers came at the expense of testing time. In fabrication-based courses the students often do not really understand what they have been processing until they test their circuits. If testing time is limited, then student understanding is limited.
- To be involved actively in the design phase of process, students needed to learn IC CAD software. The course could not dedicate much time to IC CAD tools, for additional time constraints would be added to an already ambitious lab.
- There were low circuit/device yields. These increased the testing time because students had to take extra time to find working devices, thus reducing the amount of time students could spend analyzing the data.
- Students who did not fully participate in group activities did not learn as much as students who did. However, the group grading system in place gave the same grade (deserved or not at the individual level) to the whole group.

B. Problems Related to Student Impact

- Student impact was very low (five students) the first time the course was offered. This situation needed to be improved since the minimum enrolment had been set to 20 students because of budgetary reasons.

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The authors are with the College of Engineering, San Jose State University, San Jose CA 95192-0084 USA (e-mail: dparent@email.sjsu.edu; ebasham32@earthlink.net; ydessouk@email.sjsu.edu; glyoung@email.sjsu.edu; elallen@sjsu.edu).

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- The student impact needed to be increased beyond just the students who were currently enrolled because the instructors relied on external funding from local industry to offer this course. External funding to offer this course was required because this course is expensive to teach in terms of extra faculty time and resources. (Approximately $1000 per student is needed to offer this course, and student laboratory fees are only $25 per student.)

II. Improvements

A. Improvements to Address Student Learning

To give the students a chance to design, fabricate, and test a complete semiconductor process (and thus increase student ownership), they were asked to design with the Athena process simulation tool and fabricate in the lab a simple two-mask semiconductor device process. The students had a choice between a two-mask N-type metal–oxide–semiconductor (NMOS) transistor, a two-mask P-type metal–oxide–semiconductor (PMOS) transistor, or a solar cell process. The two-mask MOS process was chosen because it only had two photolithography steps and three layers: Diffusion, Oxide, and Metal. The two-mask NMOS or PMOS process was based on an aluminum gate [3], with spin on glass as a dopant source and a gate that overlaps the source and drain. Since this process was very simple, the simulation time saved from the two-mask process compared with the previously used seven-mask CMOS was 40 min/run. The time saved in the lab fabricating the two-mask process versus the seven-mask process was at least eight weeks. The time saved was used by the students to do more testing and analysis of the fabricated devices. For example, the students were able to incorporate the SPC data they had gathered monitoring the registration error of the aligner to ensure 95% circuit yield.

To increase the time available for testing of the student's CMOS circuit designs, the students who were currently enrolled were asked to, design and fabricate the final metal layer mask of a semicustom digital or analog CMOS design with wafers that have been preprocessed to mask six (Contact Cut) by the previously enrolled students. This change saved time because the wafers had been preprocessed to the point where only one mask layer needed to be designed and processed in the lab. Since there were fewer steps to complete before testing could begin, more time was available for testing. The time saved was also increased because the semicustom design flow was faster than the previous full custom design flow that was being used. Previously, in order to have a full custom design on a current wafer run, the design had to be completed in another course in the previous semester. Another method to increase the time available for testing was to have students' complete designs that are easy to test, such as pseudorandom bit stream (PRBS) generators.

To make sure that there will be preprocessed wafers for next year's students to use, the students who were currently enrolled were asked to preprocess next year's wafers. Since the waferswere for next year and would not have to be tested, the fabrication steps were stretched out over the whole semester. In previous semesters, the process had to be completed in 12 weeks, in order to leave two weeks available for testing. When these students were unable to finish all the fabrication steps for next year's wafers in the semester, the TAs and technician were able to complete them at a later time. This procedure allowed the instructor flexibility in deciding what to do with the class when equipment broke down during lab meeting times.

TABLE I
Previous and Revised Layout Rules

Layer	Rule #	Rule	SCMOS (Previous) (μm)	Revised (μm)
P-Well	1.1	Min Width	10	15
	1.1	Min Width	10	15
	1.2	Min Spacing (DP)	9	9
	1.3	Min Spacing (SP)	6	6
ACTIVE	2.1	Min Width	3	3
	2.2	Min Spacing	3	3
	2.3	S/D Active to Edge of Well	5	6.5
POLY	3.1	Min width	2	2
	3.2	Min spacing	2	3
	3.3	Min gate extension	2	3
	3.4	Min active extension to Poly	3	10.5
	3.5	Min Field poly to active	1	3
Select	4.1	Min overlap with gate	3	3
	4.2	Min overlap of active	2	5
	4.3	Min overlap of Contact	1	2.5
	4.4	Min width and Spacing	2	2.5
Contact	5.1	Exact Contact Size	2	2.5
	5.2	Min poly overlap	1.5	2.5
	5.3	Min spacing	2	2.5
	5.4	Min spacing to Gate	2	5
	6.1	Exact Contact Size	2	2.5
	6.2	Min active overlap	1.5	5
	6.3	Min spacing	2	2.5
	6.4	Min spacing to gate	2	3
Metal	7.1	Min width	3	3
	7.2.a	Min spacing	3	3
	7.3	Min overlap of any contact	1	2.5

Since low circuit yield increased testing time, the authors improved circuit yield by changing the layout rules of the process based on the statistics of alignment registration errors (Table I). Other university labs that used scalable-CMOS (SCMOS) rules have reported low yields as well (∼50%) [4]. Another improvement was making sure every device or connection had at least two contacts. Additionally, the contact size was increased from 1.6 to 2 μm so that it would be easier to fabricate, and there would be less contact resistance. (A silicon/aluminum alloy was used to prevent junction spiking which increases the contact resistance [5].) Also the minimum spacing of the polysilicon to make sure that the gates would be isolated from each other.

Because most of each student's grade in this class is based on a group grade, assessment methods had to be developed to make sure all students were participating in lab. First, a simple survey was used in which students anonymously wrote about how they felt others in the team were participating. All the students responded that their teammates were participating fully.

TABLE II
SAMPLE QUESTIONS FOR THE SCREENING HOMEWORK

Subject Area	Question
Solid State Physics	Given doping levels, minority carrier lifetimes, area, and mobilities of an abrupt junction diode, calculate Fermi levels, and draw the energy band diagram of a Silicon-based diode. Determine the breakdown voltage and explain the breakdown mechanism
Solid State Physics	For the diode described in the first question, calculate the current at reverse bias, thermal equilibrium and, forward bias.
Solid State Physics	For the diode describe above calculate the same currents except change the material from silicon to germanium.
Solid State Physics	Draw the cross section of an NMOS transistor; label Source, Drain, Gate, Body, and the inverted channel.
Solid State Physics	Given all the pertinent material parameters, calculate the threshold voltage of a MOS capacitor.
Solid State Physics	Given two MOS capacitors with the same doping and fixed oxide charge, but different oxide thickness, choose the capacitor with the largest threshold voltage.
Solid State Physics	Given the threshold voltage, W, L, mobility, and oxide thickness draw the IV characteristic of a long channel MOSFET.
IC Design (CAD tools)	Given an inverter schematic and layout, find the layout vs. schematic error.
Athena knowledge	Given the code for a starting grid in an Athena run deck, explain what would happen to the simulation time and accuracy of the simulation if the grid were increased/decreased.
IC Fabrication knowledge	Given a silicon wafer with a doping density, design a process to fabricate a PN junction with a specified surface doping density, doping profile, and junction depth.

These responses were contrary to what instructors had observed in lab; thus, a lab practical exam consisting of four tasks was developed to assess at least whether the students had the basic skills that would have been acquired by participating fully in the lab activities. The four tasks were measuring an oxide thickness, identifying registration error in a mask, using an HP4145 tester to extract sheet resistance from a test structure, and running a simple Athena process deck.

The students were told two weeks in advance what skills were to be tested. They were also told that they could bring in any documentation they wanted to assist them in demonstrating the tasks. The students were graded either with a "Go" or a "No-Go." All the students who received two "No-Go" scores or more were grouped together in one team. From that point on one could see who was really participating in lab. At first the "No-Go" team seemed to pull together and participate more than they had during the first part of the semester, but after a few weeks they stopped trying. The "No-Go" team did not complete their design projects. Unfortunately, this technique only measured student participation too late to change student behavior. Since instructors believed the results would be better if student participation were increased rather than just measured, the next semester students' skills were verified before they started their projects.

B. Improvements to Address Student Impact

Increasing student impact was approached in several different ways. The first was to have more students enroll directly into the course by changing the prerequisites from having a mandatory "Introduction to IC fabrication" course [6], to having three separate paths into the course. The three paths are prior experience in IC processes/fabrication [6], IC circuit design (knowledge of Cadence tools), or advanced device physics knowledge with T-CAD (Silvaco/Athena) knowledge. Since adopting the new prerequisite system, the instructors have seen enrolment grow from 5 to 21 students.

An important side effect of having more than one prerequisite path is that now each student (once the teams are created) has a different educational background. Each student brought a different skill set to his or her team. This side effect was actually an advantage because employees of semiconductor manufacturing or IC design companies will increasingly have to work in an interdisciplinary environment [7]. Another advantage of having multidisciplinary teams was that each team included a student who knew either the IC design CAD tool set or the Athena T-CAD tool. This knowledge cut down the time the teams needed to learn the tools.

On the other hand, having three different paths into the course made presentation of material and assessment of student knowledge more difficult. After trying this technique for one semester, the instructors realized that students needed a strong background in device physics. To ensure that all the students had a common background, more than the two years of math and physics required of all engineering majors was needed. Having a common background of device physics gave the instructor a starting point for presenting the material. The second most important perequisite was having either good IC processing knowledge or IC design knowledge. Such knowledge made sure that each student brought a unique skill set to the multidisciplinary teams, and still had the common knowledge base required to learn the new material.

To ensure that the incoming students had a solid device physics background and a special skill set, the instructors designed a homework assignment that was due two days after the first class meeting (see Table II). To be given permission to enroll in the course, students must have tried all the solid-state

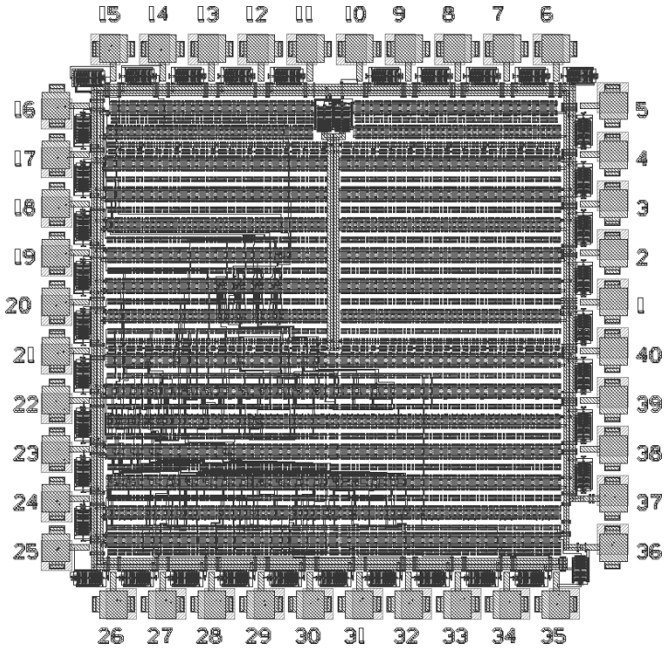

Fig. 1. A 4-bit arithmetic logic unit (ALU) using the gate array.

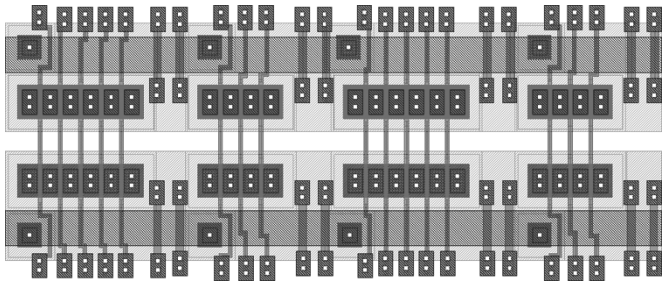

Fig. 2. Expanded view of a simple cell of the gate array.

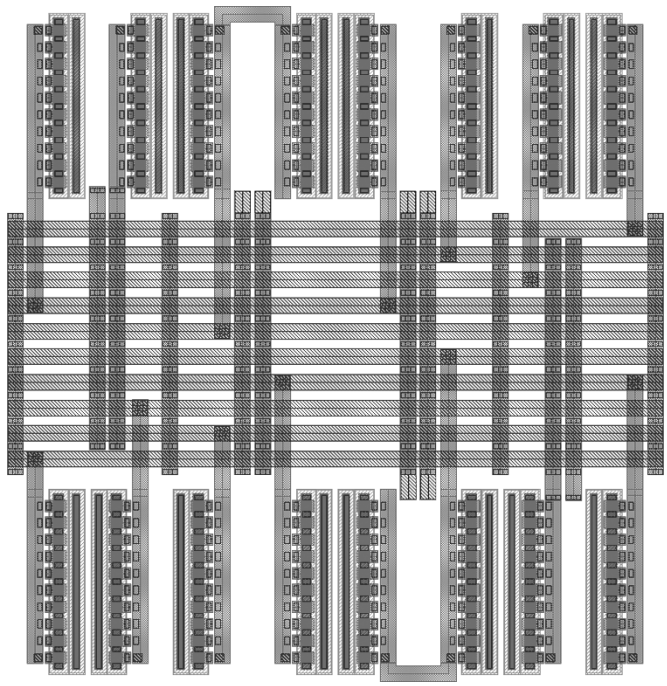

Fig. 3. Layout of a full analog leaf cell.

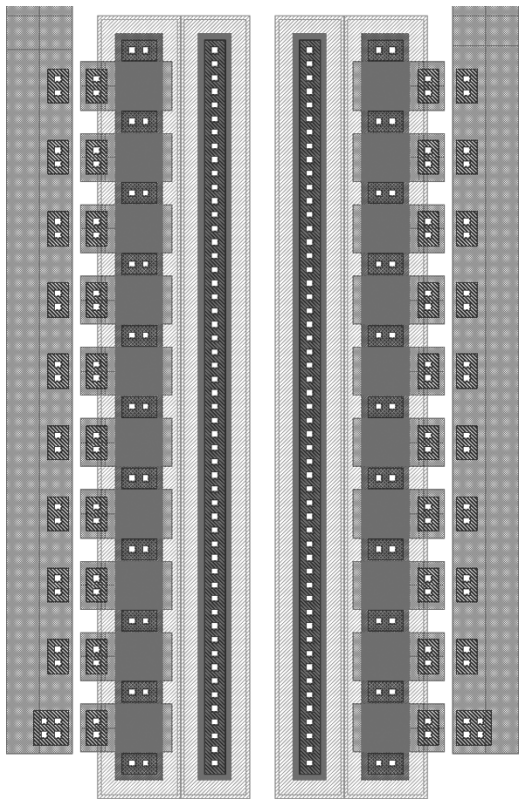

Fig. 4. Expanded view of the analog leaf cell NMOS transistors.

physics questions and completed one of the area questions correctly. Students who did not try each solid-state question were not given permission to enroll or were dropped if they were preregistered. Those students who tried, but did not do well, were counseled to determine why they did not do well. Then a plan of action was set up to resolve the problem. Once the enrollment was stabilized during the first week of the semester, the homework assignment was then used as a guide to make sure that each team had a member who knew IC processing or IC design knowledge.

Even though the upper limit of students who could take the course (21 out of 24) was reached, the need to increase the student impact beyond the students enrolled in class existed because of the large cost to offer this course. This expansion was achieved by having students enrolled in the course act as an IC foundry [8], [9] for other class designs using the gate array (see Figs. 1 and 2), or analog leaf cell [10] (Figs. 3 and 4) semicustom environments. (A tutorial and design examples can be found at: http://www.engr.sjsu.edu/~dparent/ICGROUP/analogleafcell.pdf)

At this time, only one student design from a required EE laboratory course has been fabricated, but fabrication could grow to include all BSEE students in the department if the semicustom IC curriculum was adopted by a required EE laboratory course. To facilitate expansion, a standard cell library is being developed for the gate array for automatic place and route using Cadence Design Systems Place and Route Tool. The student impact should become limited only by the amount of IC test equipment and the interest of other professors to have their students use our design flow.

An additional method of increasing student impact was to include novel device structures for future integration with the gate array or analog leaf cell whenever a new mask set needed to be created. These included charge-coupled devices (CCDs) and laterally diffused metal oxide semiconductor (LDMOS) structures.

III. Revised Laboratory Activities

In order to address student learning and impact, the laboratory activities had to be changed. During the first part of the semester students would learn the Athena CAD tool and review microelectronic processing skills. Then the teams would rotate from processing the device wafers to completing simple SPC0 projects [1] until the devices were ready for testing at the end of the semester (usually during finals week). Now students complete several long-term projects (two-mask MOS process, gate array or analog leaf cell, and one statistical process control activity), while still rotating into the processing lab to fabricate CMOS device wafers for next year.

The flow of activities is as follows. After learning or reviewing the Athena CAD tool by following a simple tutorial (http://www.engr.sjsu.edu/~dparent/Silvaco/silvaco.pdf), and reviewing microelectronic processing skills at the beginning of the semester, students design a two-mask NMOS or PMOS process. The second major activity after this miniproject is measuring and reporting registration error, recommending design rule changes to increase circuit yield. The registration error data is collected from vernier scales processed during previous courses. The students then finalize their two mask MOS process designs based on this information.

The third major activity consists of learning or reviewing Cadence Design System IC design software and then completing a gate array or analog leaf cell design. The level of design complexity depends on the student's background. Some of the advanced students are able to complete the design of 4-bit ALUs in the gate array (see Fig. 1), while others can design operational amplifiers (OPAMPS) using the analog leaf cell. Those without previous IC design experience can design inverters and NAND gates that are part of larger gate array design or current mirrors that use the analog leaf cell. After the designs have been verified to work at the output pin level, the instructor generates the final mask layer for outside fabrication through a local company. While the class waits for the mask fabrication, final patterning, and annealing step (three weeks), students fabricate and test their two mask MOS device wafers. When the CMOS gate array and analog leaf cell device wafers are ready, students should be finished with the two-mask MOS process project. Then they can begin testing their gate array or analog leaf cell design project. Each week a different team processes next year's device wafers in rotation.

A. Student Feedback

The student feedback about the changes in the course was very positive based on course evaluations collected from the students at the end of the semester. The students enjoyed being able to design a process and follow the process in lab to make their devices. They liked the gate array and analog leaf cell semicustom IC design project, but were frustrated that the tutorials were written for someone with some Cadence-tool knowledge. There were also some errors in the technology file that had to be corrected while the students were taking the course, a situation which increased student frustration levels as well. Even though these problems have been corrected, the instructors determined that the hand-stitched gate array designs were too much work for this course. Therefore, in the future, all students would perform only a simple analog design with the analog leaf cell.

IV. Conclusion

Student learning was enhanced by allowing students to a design, fabricate, and test a semicustom design flow gate array or analog leaf cell and a simple two-mask MOS process design flow. By switching to a semicustom flow and a simpler semiconductor process flow, the time available for testing was increased.

By having three separate paths into the senior level IC processing laboratory, the instructors were able to increase student impact significantly. They expect to increase the student impact of this course dramatically by offering a gate array or analog leaf cell design experience to students in core EE courses (for instance, a current mirror in the Circuits I course). Creating a design-process kit to be used by other universities might expand this impact further.

After by making all these changes students should be able to learn more in the CMOS processing course. Also, the impact of the course has been expanded beyond those students enrolled in the course. In addition, students were able to link the concepts of a CMOS circuit design flow with a semiconductor process design flow because there was enough time for students to use both flows in one semester.

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David Parent (S'96–M'99) received the Ph.D. degree in electrical engineering in 1999 from the University of Connecticut, Storrs.

Currently, he is an Assistant Professor in the Electrical Engineering Department at San Jose State University (SJSU), San Jose, CA, where he teaches CMOS processing and device physics and conducts solar cell research.

Eric Basham (M'00) received the B.S. degree in biotechnology from Rutgers University, New Brunswick, NJ, in 1997 and is currently working towards the M.S. degree in electrical engineering at San Jose State University, San Jose, CA.

He has worked at Hewlett Packard and enjoyed internship opportunities at Marigenetics, Intel, and Aclara Biosciences. He is planning to pursue the Ph.D. degree at University of California Santa Cruz, Santa Cruz, CA, in biomedical engineering.

Yasser Dessouky received the Ph.D. degree in industrial and management systems engineering from Arizona State University, Tempe, in 1993.

Currently, he is an Associate Professor in the Department of Industrial and Systems Engineering at San Jose State University (SJSU), San Jose, CA. He teaches statistical process control and conducts research on operations management.

Stacy Gleixner received the Ph.D. degree in materials science and engineering from Stanford University, Stanford, CA, in 1998.

Currently, she is an Assistant Professor in the Department of Chemical and Materials Engineering at San Jose State University (SJSU), San Jose, CA. She teaches courses on electronic materials, solid-state kinetics, and thin-film deposition. Her research focuses on development and processing of microelectricalmechanical systems (MEMS) devices.

Gregory Young received the Ph.D. degree in chemical engineering from the University of California at Davis in 1990.

Currently, he is an Assistant Professor in the Department of Chemical and Materials Engineering at San Jose State University (SJSU), San Jose, CA. He teaches transport and semiconductor processing courses and conducts research on electroplating of copper.

Emily Allen received the Ph.D. degree in materials science and engineering from Stanford University, Stanford, CA, in 1992.

Currently, she is Chair of the Department of Chemical and Materials Engineering at San Jose State University (SJSU), San Jose, CA. She teaches courses on electronic materials, IC processing, and solid-state kinetics, and conducts research on magnetic thin films and semiconductor processing.