Microelectronics Process Engineering Program at SJSU

David Parent, Yasser Dessouky, Stacy Gleixner, Gregory Young, Emily Allen
College of Engineering
San Jose State University
One Washington Square
San Jose Ca 95192

{ HYPERLINK "mailto:dparent@email.sjsu.edu" }

Abstract

1. Introduction

Currently there is a need for engineers with CMOS processing knowledge, Statistical Process Control (SPC) skills, and the ability to work in an interdisciplinary team environment and assume leadership roles[1].

We are developing an interdisciplinary lab-based microelectronics process engineering program that introduces SPC and DOE to our students in a microelectronics manufacturing environment. At the heart of our program are three courses, each of which is imagined to be a division of a fictitious semiconductor fabrication company (Spartan Semiconductor Services, Inc., or S3i). The divisions are: Digital NMOS division (MatE/EE129: Introduction to IC Fabrication), Thin Film Research Division (MatE/ChE 166: Advanced Thin Film Processes) and CMOS Division and SPC task force (MatE/EE 167: Microelectronics Manufacturing Methods).

Several unique features of our program are its introduction of statistical process control (SPC) in a microelectronics manufacturing environment, the inclusion of design of experiments (DOE) topics, and the faculty-faculty, faculty-student and student-student interaction among the three courses (divisions).

Ultimately, we are trying to provide a learning environment that will allow our students to be immediately productive in an IC production facility, to be able to communicate with IC Process engineers, and to be prepared for graduate school programs.

2. Background

The CMOS/SPC course seeks to build upon the success of our previous PMOS fabrication course [2, 3]. The key aspects of this course were that the students participated in an interdisciplinary team environment to fabricate PMOS circuits, and the lecture used active learning techniques to improve student participation and thus learning. The laboratory and lecture parts of the course were all run in the context of a start up company. Eighty percent of students thought that they learned more in this type of environment than in traditional "cook book" type laboratory experiences. The technology for this course has recently been converted from PMOS to NMOS.

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The CMOS/SPC course is run in the same interdisciplinary, team-based method as the NMOS course. The teaching team is altered from a ChemE/MatE/EE team to an EE/ISE team, and the processing experiments are replaced with statistical studies of oxidation, diffusion, and metalization processes used in the lab. Team building exercises are continued with the addition of leadership building activities.

3. New Course content

Our new course, Microelectronics Manufacturing Methods ((MatE/EE 167)), is a laboratory-based course on fabrication of CMOS integrated circuits. The lecture and lab cover CMOS semiconductor processes and process control. The general learning objectives for the course are:

- CMOS Inverter modeling layout and physics
- T-CAD Modeling of a CMOS process
- Metrology
- Team Work
- Process Control

The lecture was comprised of two 50-minute lecture periods per week, one on statistical process control and the other on device physics and process modeling. The lab met once a week for three to four hours. The laboratory was run with two teams that alternated duties between processing CMOS circuits and conducting SPC assignments in the lab.

a. CMOS Process

The process we used was based on an n-well process developed in the 80's [4] due to its use of ion implantation and self aligned gate technology. We modified it to a p-well process so we could drop the channel stop implantation step. We wanted to introduce ion implantation, poly-Si growth and etch aspects, and photolithography of modern CMOS processing, without burdening the lab with too much off line processing. The process was designed and simulated by the instructor for 1.5-micron features with TSUPREM-4 (Silvaco's Athena). Table 1 lists the main processes carried out and the Athena run deck is available from the authors. The ion implantation and the poly deposition and etch were performed at local vendors [5,6] and the photolithography carried out according to [7].

Process	Process Parameters	Mask
1) Grow Screening oxide	Dry oxidation 30 minutes at 1100°C	NA
2) Implant "n-well"	1e11/140/Phos, tilt=7, rotation=0	NA
3) p-well Photolithography		PWELL
4) Implant pwell	3e13/100/bf2, tilt=7 rot=0	NA
5) Etch pwell/Strip PR	RIE	NA

6) Grow Field oxide/ Well drive	1100°C for 30 min wet ox 1150°C for 180 minutes N_2	NA
7) Active Photolithography		NA
8) Etch and Strip	RIE	NA
9) Grow Active layer	30 min dry O2 1100°C, 90 min post oxidation anneal 1100°C, N_2	NA
10) VT adjust implant	3.5e11/25/bf2 tilt=7, rotation=0	NA
11) Poly-Si Growth	.5 microns undoped (SNF)	NA
12) Poly-Si implant	1e15/130/P tilt=7, rotation=0	NA
13) Poly gate photolithography and etch (Do not Strip PR)		POLY
14) PMOS S/D Photolithography and Implant (PR Strip)	1.5e15/60/bf2, tilt=7, rotation=0	PSELLECT
15) NMOS S/D Photolithography and Implant (PR Strip)	5e15/50/Arsenic, tilt=7, rotation=0	NSELLECT
16) Apply P SOG	Emulsitone, spin speed 3000 rpm, 20 seconds	NA
17) Anneal/Activate impurities	900°C 30 minutes, N_2 Should have used 1000°C 30 minutes, N_2	NA
18) Contact PL and Etch	RIE	CONTACT
19) Metalize	1 micron sputtered Al/Si	NA
20) Metal PL /Etch/Strip PR	Heated Al etch	METAL1
21) Anneal (Ohmic contact formation)	475°C 30 minutes, forming gas	NA
22) Test Devices		NA

Table { SEQ Table * ARABIC }: Process Outline

b. SPC

While one team worked on part of the CMOS process, the other team acted as a SPC resource for the NMOS processing lab. An example SPC project was an analysis of our wet field oxidation process. The students in the NMOS class noticed a large variation in the field oxidation, and needed to know if they had to redo the field oxidation step. They asked the SPC task force to conduct SPC analysis on the expected yields due to this variance, and how to improve the process. The results from the SPC task force showed that the yields should still be above 90% even with the variance encountered, and that the large special cause variation was due to a temperature gradient in the oven. This allowed the students in the NMOS processing course to continue processing their wafers, thus

preventing wasted lab time by starting over. The solution to the temperature gradient will be discussed under leadership activities.

Table 2 lists all the SPC assignments conducted in lab. The students had to communicate to collect the data from the three NMOS class sections, and answer the following questions given upper and lower limits for the process. Is the process under control? If there is special cause variation what is the cause? If nothing is done to improve the process, what will our yields be? The students had to present their findings in oral and written reports.

Assignment	Process Used	What was measured	Metrology tool
Field Oxidation	Steam oxidation	Film thickness	Filmetrics
Source/Drain Predeposition	P SOG 950oC	Sheet resistivity	4 point probe
Gate Oxidation	Dry Oxidation 1100oC	Film thickness	Filmetrics
Metalization	Sputtered Al with 1% Si	Sheet resistivity	4 point probe

Table { SEQ Table * ARABIC }: In LAB SPC Assignments.

c. Teamwork/Leadership activities

There were two activities added to the course to develop teamwork and leadership skills of the students. The first is an in-class leadership exercise, and the second is the addition of After Action Reviews (AAR) conducted at the end of each lab session.

The in-class leadership exercise demonstrates some of the problems with a strictly hierarchical management style. In this exercise, students are broken up into teams. Each team has a team leader, a deputy team leader, two sub team leaders and four to six team members. Once the teams are formed and the roles assigned, the "rules of communication" are explained to the students. The rules are as follows. All communication is through hand written notes. The team leader can communicate only with the deputy team leader. The deputy team leader can only communicate with the team leader and the two sub team leaders. Each sub team leader can communicate with the deputy team leader and the team members on his or her sub-team. Each sub-team member can only communicate to the respective sub-team leader. After the rules of the game are explained, each team member from the team leader down to the team member receive a 3x5 card with a random symbol or letter printed on it. Once this is done, each team leader receives a card with the "goal" or mission that the team has to complete within five minutes. The goal is simple: collect the symbols or letters that each team member has in the given amount of time. Once the team leaders receive the mission start

the clock. While running the exercise, it is important for the proctor to keep mentioning that time is running out, or some active byplay to put pressure on the team leader. After the time runs out, the proctor conducts an After Action Review (AAR).

An AAR is a feedback session in which the participants of any activity discuss the activity. It is important to conduct AAR's immediately after the activity, and the following topics are a minimum. What was the mission? Did we meet the mission? What went right about the mission? What went wrong? What are the improvements that need to be made? The proctor begins the ARR process by asking the team members if they knew what the mission was, and if the team completed the mission. The Proctor then asks the same question of each member in the hierarchy. Usually the team members have no clue what the whole exercise was about, because the team leaders failed to pass the mission statement on. The proctor should then ask how each team member felt during the exercise. Typical feelings for team members are feeling left out and clueless. Deputy leaders feel under enormous pressure from both the team leader and the sub team leaders. The team leaders usually feel frustrated. The proctor then asks the students what could have been improved about the way the team communicated. The result is that students learn what it is like to be leader and a follower in one exercise, and the students propose better ways to communicate. The students also learn how to conduct an ARR.

The ability to conduct an AAR was used to come up with solutions to the field oxide problem the NMOS students were facing. Once the SPC team discovered the problem and the source of the error, an AAR was conducted by the students to fix the problem. It turned out that the NMOS students were putting the wafers into the wrong zone of the furnace instead of the flat zone. The students proposed several solutions to prevent this type of error. The first was to write a document standardizing the proper wafer loading procedure, and the second was to simply mark the push rod so that a new operator would know exactly when the wafer carrier was in the flat zone. The students seemed to take great pride in solving this problem and stayed long beyond the scheduled class time to discuss it.

The documentation provided an alternative method to our previous hierarchical style of passing on processing information. Previously, the Lab instructor would verbally issue instructions to the lab TA's and the TA's would verbally instruct the students. With the addition of written protocols for each step, there was an improvement in the uniformity of subsequent steps.

4. Results and Discussion

Currently the PMOS devices work while the As implants do not seem to be activated thus the NMOS devices are not working. The measured threshold voltages for the 10 micron devices match the predicted values to within 15%. We kept some wafers back from full processing so that we can change the anneal temperature to improve the As implant activation and we hope to demonstrate a fully functional CMOS process.

One improvement the students suggested was that the SPC lecture and the CMOS processing lecture should be back to back. The SPC is introduced in a theoretical manner, and then a real world CMOS example is worked out in the second part of lecture. There were four SPC assignments in lab, each one dedicated to improving the NMOS processing course. This seemed to spark enthusiasm in the students, and forced them to not only communicate with their team members but the team members in the NMOS course. Student surveys show that they felt it was valuable to teach SPC concurrently with a real world CMOS process.

5. Conclusion

We believe that this new course taught our students CMOS processing, Statistical Process Control skills, and enhanced their abilities to work as both team leader and team member. Many parts of this program (the leadership exercise and the statistics examples) can be implemented at other schools. The result of our teaching approach is that the students feel ownership of the learning process, and seem to give more effort in these interactive classes.

6. Acknowledgements

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7. References

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[2] A.J.Muscat, E.L. Allen, E.D.H. Green and L.S. Vanasupa, "Interdisciplinary Teaching and Learning in a Semiconductor Processing Course," *Journal of Engineering Education* **87** (1998), 413.

[3] Emily L. Allen and Anthony J. Muscat, "Spartan Semiconductor Services, Inc.: an Entrepreneurial Environment," *Proceedings of the 13th Biennial IEEE University/Government/Industry Microelectronics Symposium,"* Minneapolis, MN (1999).

[4] T. Ohzone, H. Shimura, K. Tsuji, and T. Hirao, "Silicon-Gate n-Well CMOS Proess by Full Ion-Implantation Technology", *IEEE Transactions on Electron Devcies,* Vol. ED-27, No. 9, (1980).

[5] The poly-silicon growth and etch were conducted at the Stanford Nanofabrication facility (http://snf.stanford.edu/)

[6] The ion implantation was performed at The Implant Center, 2121 Zanker Road San Jose, CA 95131-2109 .

[7] Arch Chemical Data sheet for 825 series photoresist.