2 MASK NMOS Process

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SJSU

Process Engineering is expensive to teach.

TCAD tools have a steep learning curve.

The process lab is expensive to run. $

A 4 mask process can take all semester to finish.

TCAD tools have a steep learning curve

Creating a run deck from scratch is a very tedious process.

Modify a working run deck.

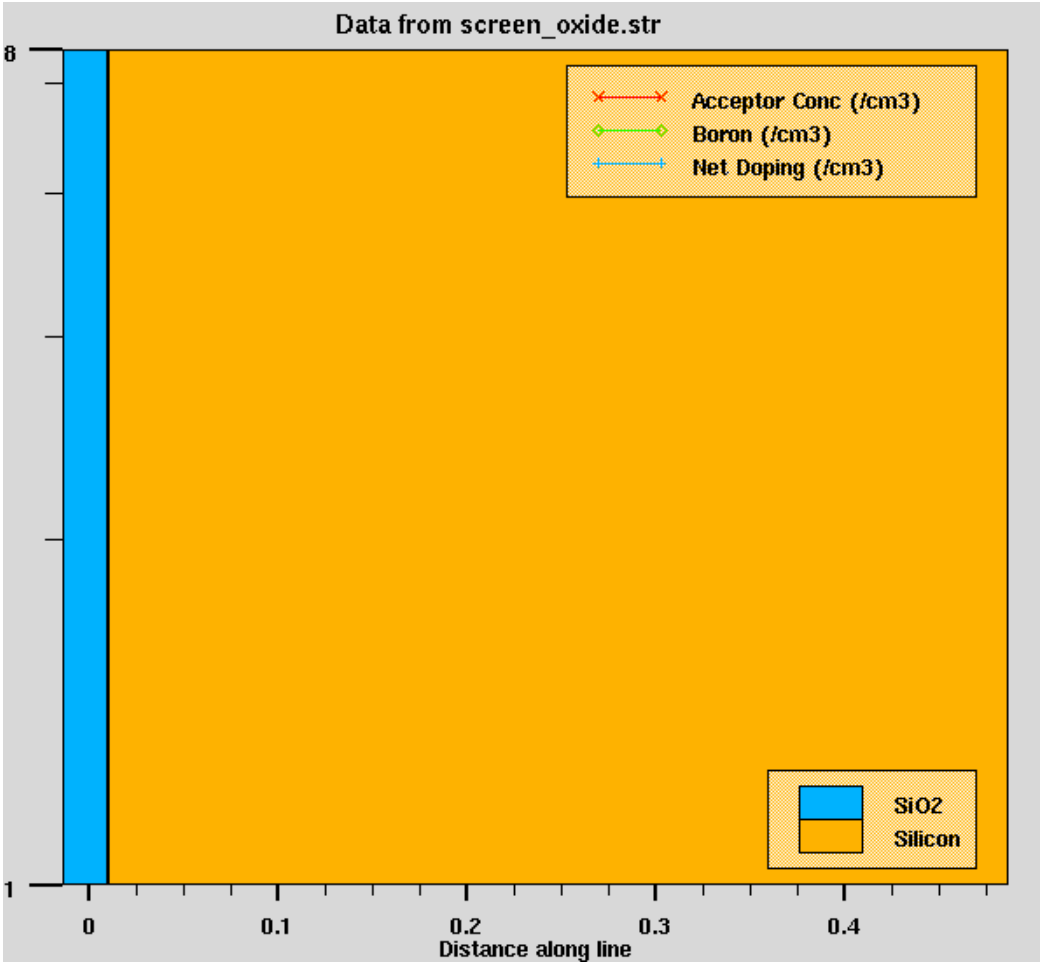
Use less masks

Design for high yield.

Our two mask process saves time and money.

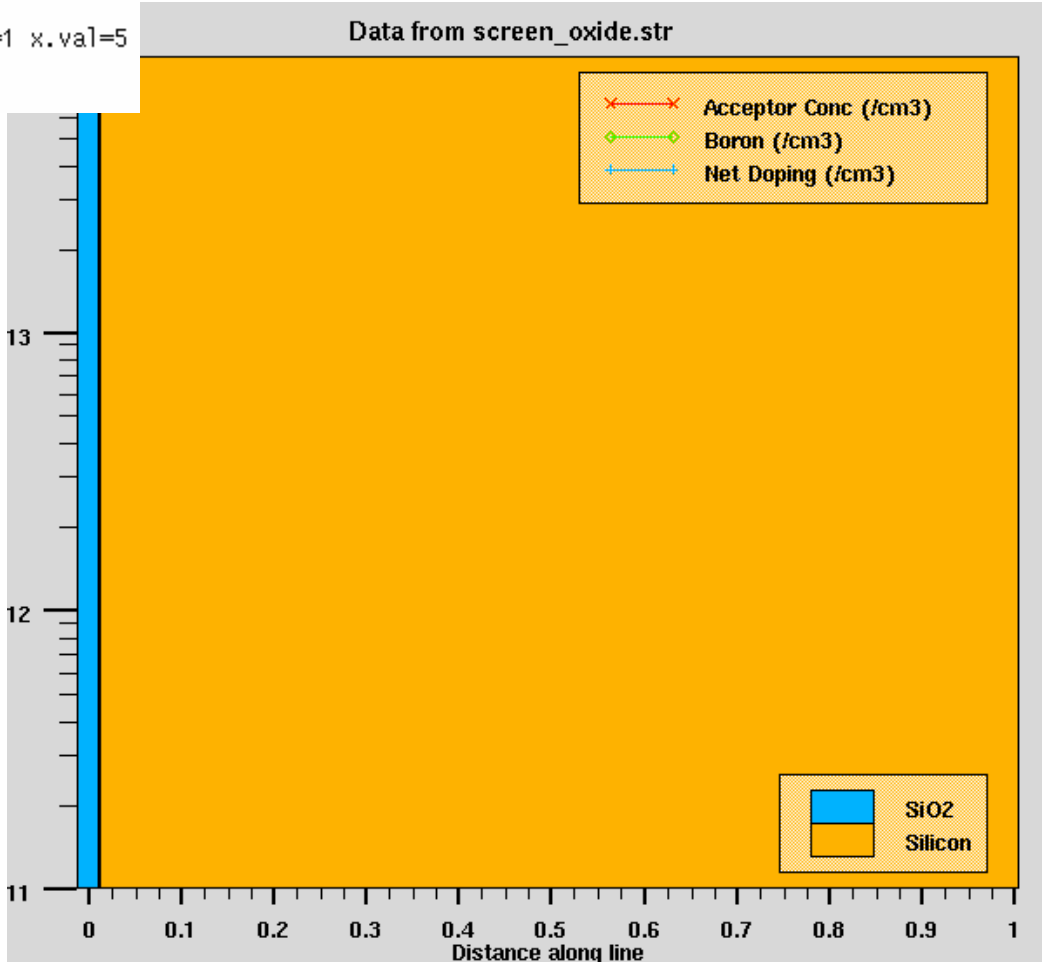
Set the mesh and initial doping level

```
go athena
#DEFINE THE GRID
line x loc=0.00   spac=0.1
line x loc=2.89 spac=.05
line x loc=4.6 spac=.2
line x loc=10 spac=2
#
line y loc=0.00 spac=0.1
line y loc=3.0   spac=0.5
line y loc=5 spac=2
#
# THIS IS WHERE YOU SET THE TYPE OF WAFER YOU WILL USE
init silicon boron resistivity=7 orientation=100
# THE PROPGRAM ASSUMES YOU HAVE CLEANED THE WAFERS AND DONE STEPS 1.0-1.10
```



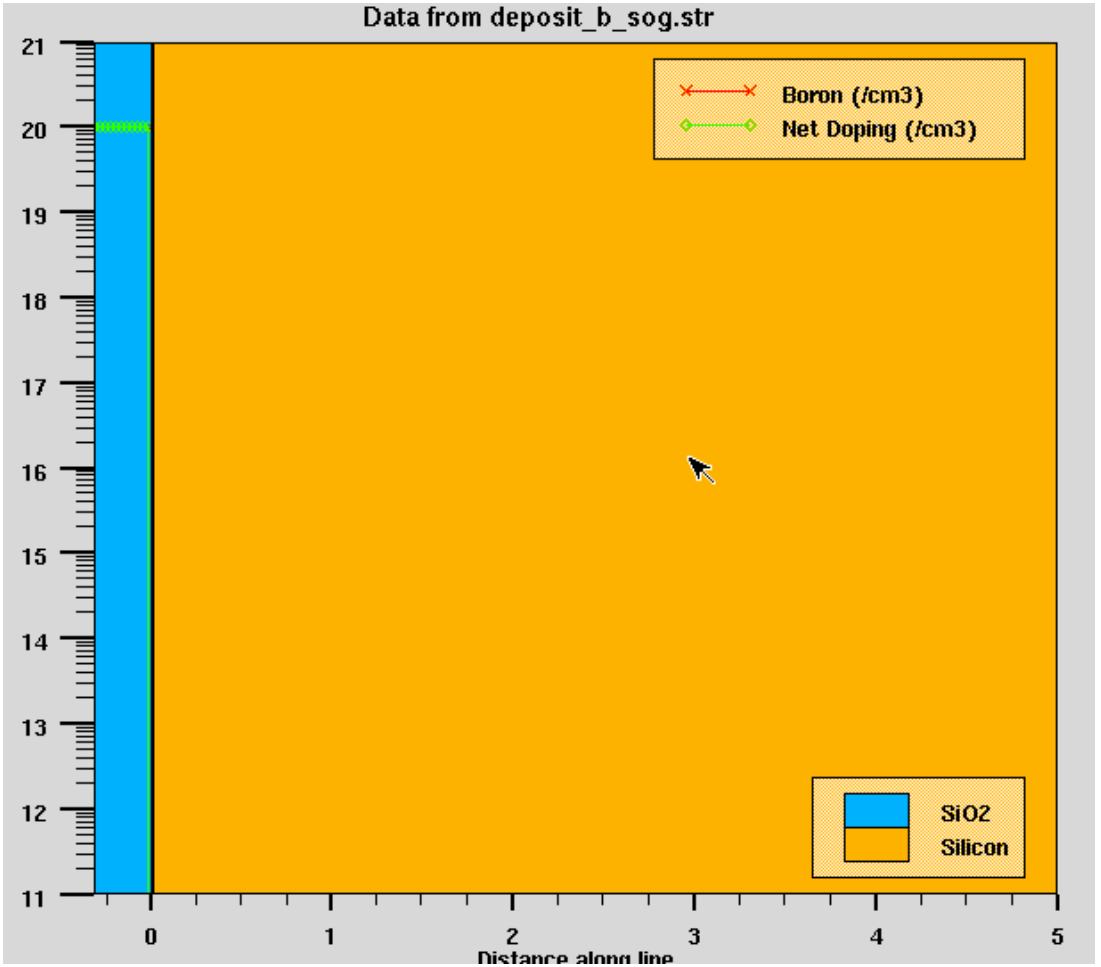
Grow Screening Oxide

```
#SCREENING OXIDE GROWTH STEP 2.0 ASSUMED
method fermi compress grid.ox=.003 gridinit.ox=.003
# STEP 2.0 IS ASSUMED
# STEP 2.1 PUSH
diffus time=15   temp=400 t.final=700  nitro
# STEP 2.2 RAMP UP
diffus time=13.3 temp=900 t.final=1000  nitro
# STEP 2.2 STABILIZE
diffus time=10   temp=900   nitro
# STEP 2.2 SOAK
diffus time=100   temp=900   dryo2
#STEP 2.2 PURGE
diffus time=10   temp=900 nitro press=1.00
#STEP 2.2 RAMP DOWN
#diffus time=30   temp=900 t.final=700   nitro
#STEP 2.3 PULL
diffus time=15   temp=700 t.final=400  nitro
#
#STEP 3.0 MEASURE OXIDE THICKNESS
extract name="SCREEN OX" thickness material="SiO~2" mat.occno=1 x.val=5
structure outfile=screen_oxide.str
tonyplot -st screen_oxide.str
```



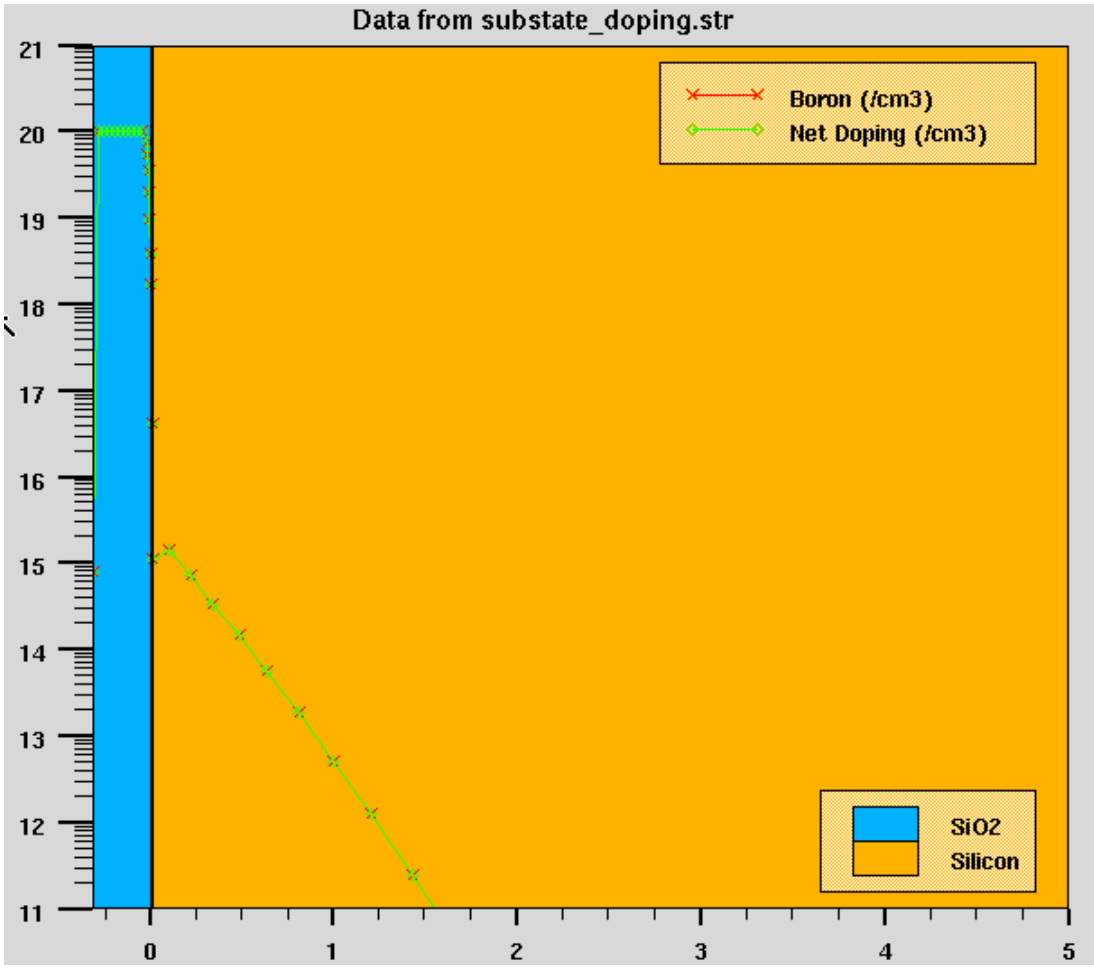
```
#STEP 3.1 ASSUMED
#STEPS 3.2-3.4 APPLY SOG
#
deposit oxide thick=0.3 c.boron=1.0e20 divisions=10

structure outfile=deposit_b_sog.str
tonyplot -st deposit_b_sog.str
```

Apply B Doped SOG



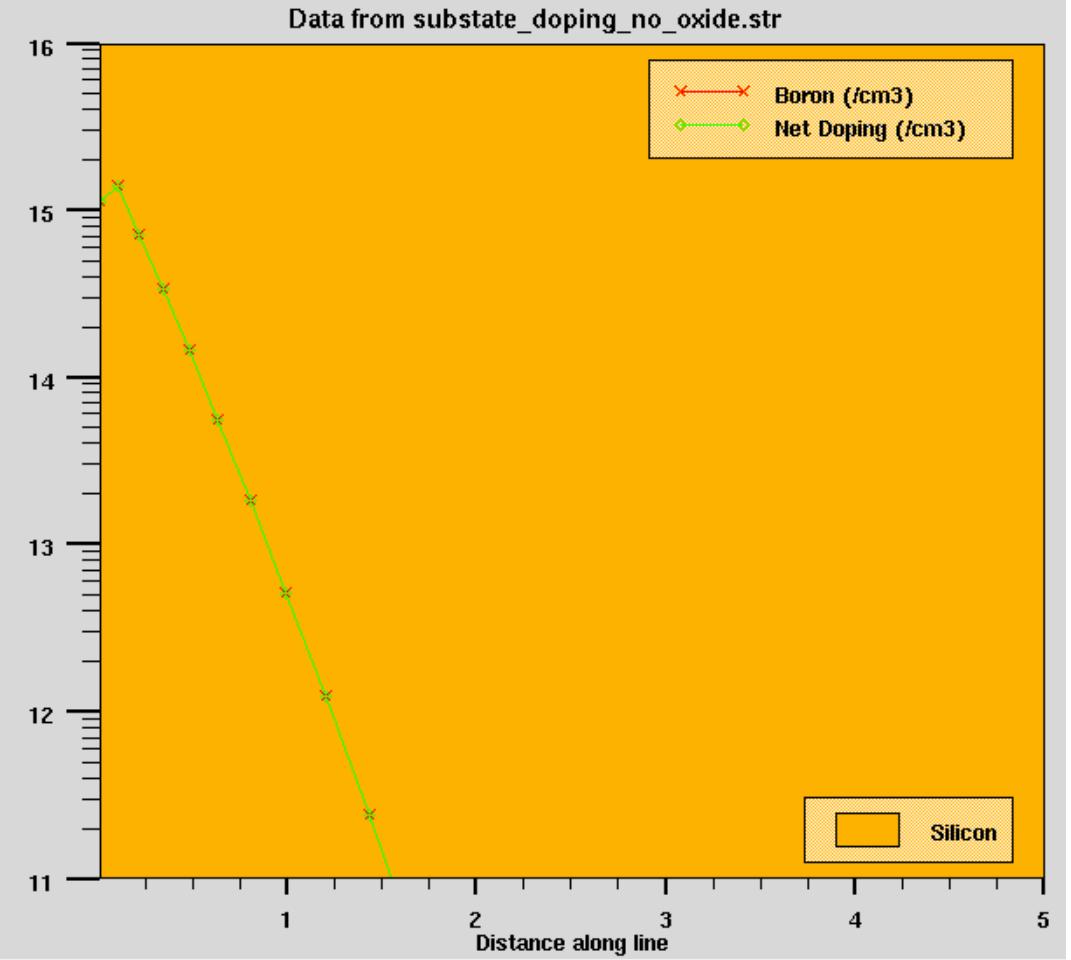
Dope the substrate

```
#B DIFFUSION STEP 4.0 ASSUMED
#STEP 4.1 PUSH IN
diffus time=15   temp=400 t.final=900  nitro
#STEP 4.2 RAMP UP
diffus time=13.3 temp=900 t.final=1100  nitro
#STEP 4.2 STABILIZE
diffus time=5   temp=1100 nitro press=1.0
#STEP 4.2 SOAK
diffus time=180   temp=1100 nitro press=1.00
#STEP 4.2 RAMP DOWN
diffus time=40   temp=1100 t.final=900   nitro
#STEP 4.3 PULL
diffus time=15   temp=900 t.final=400  nitro
structure outfile=substate_doping.str
tonyplot -st substate_doping.str
#
```



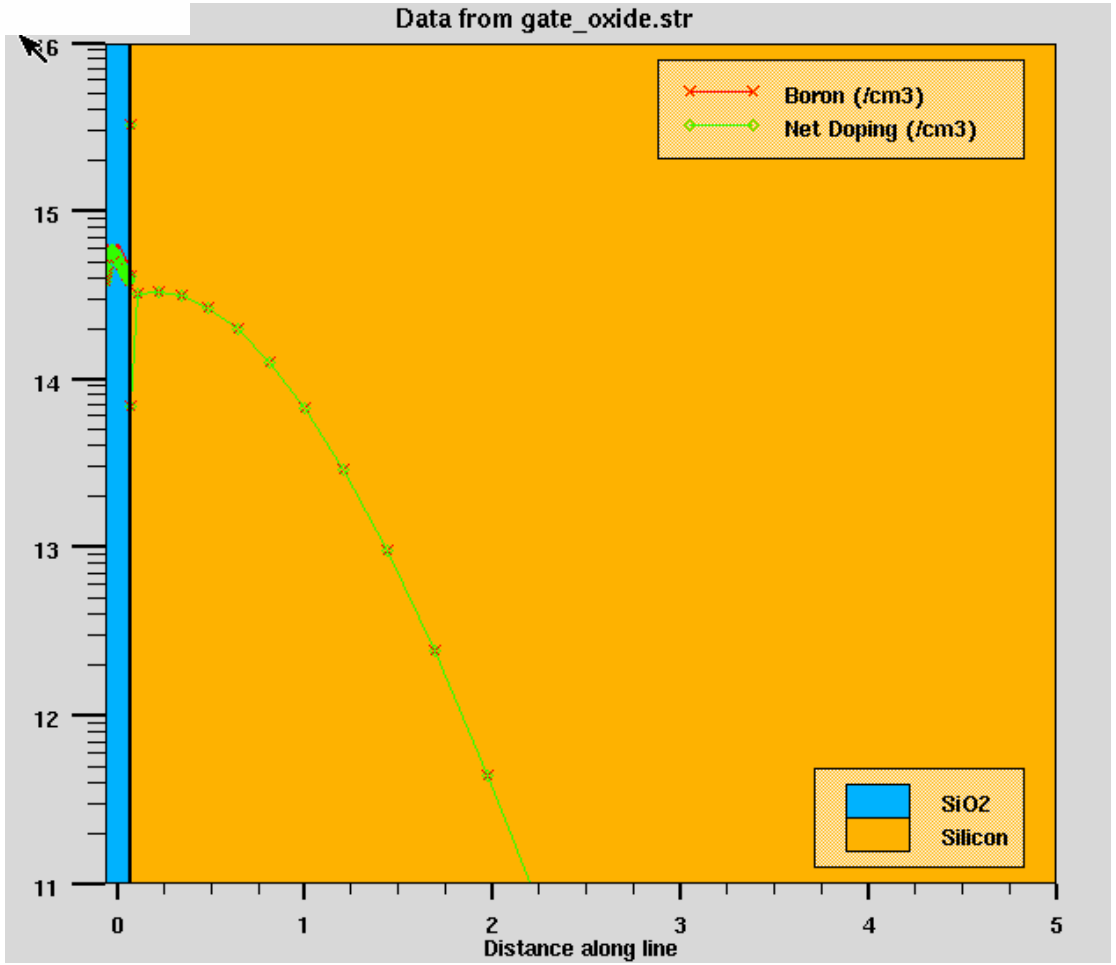
```
#
# STEP 5.0 ETCH SCREEN OX AN B SOG
etch oxide all
structure outfile=substate_doping_no_oxide.str
tonyplot -st substate_doping_no_oxide.str
```

Strip screen oxide and B SOG



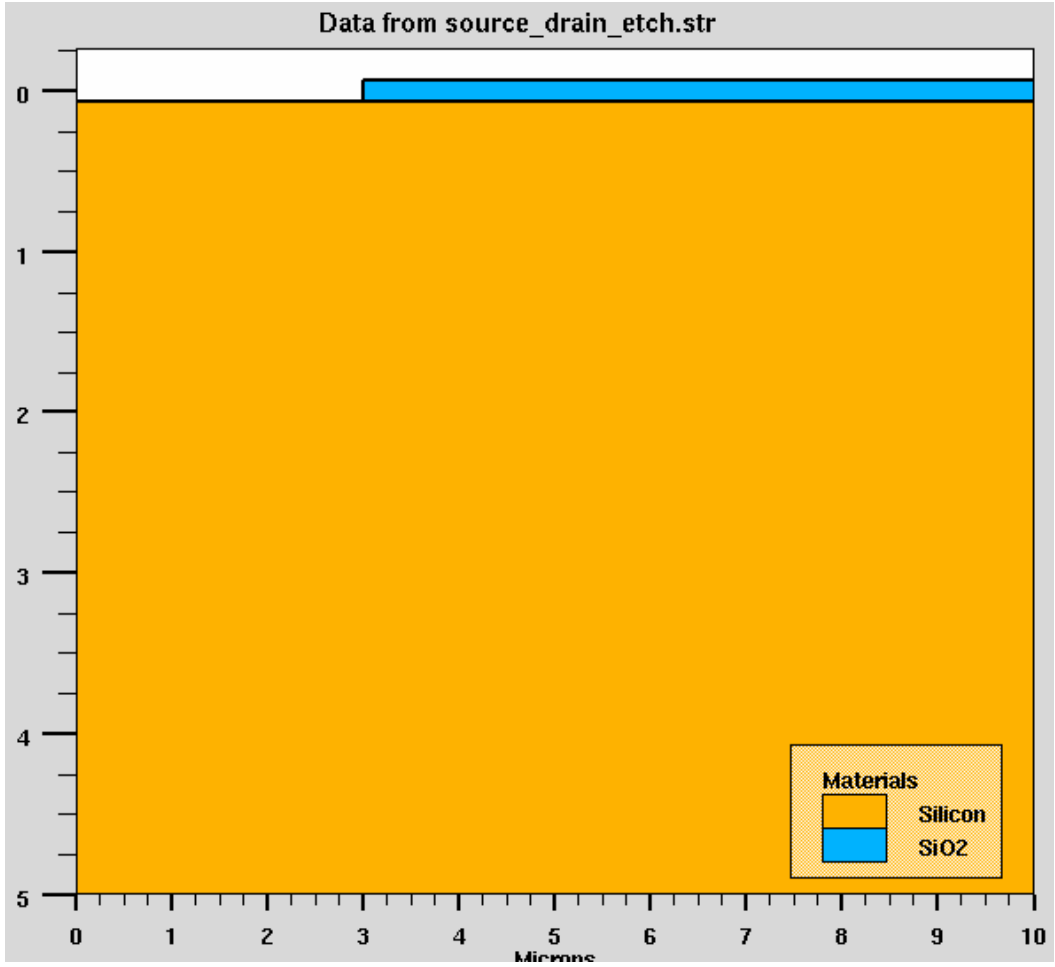
Gate Oxide

```
#  STEP 5.2 ASSUMED
#GATE OXIDE GROWTH STEP 6.0 ASSUMED
#STEP 6.1 PSUH IN
diffus time=15   temp=400 t.final=900  nitro
#STEP 6.2 RAMP UP
diffus time=13.3 temp=900 t.final=1100  nitro
#STEP 6.2 STABILIZE
diffus time=5 temp=1100 nitro press=1.00 hcl.pc=0
#STEP 6.2 SOAK
diffus time=90 temp=1100 dryo2 press=1.00 hcl.pc=0
#STEP 6.2 RAMP DOWN
diffus time=40   temp=1100 t.final=900   nitro
#STEP 6.3 PULL
diffus time=15   temp=900 t.final=400  nitro
#STEP 6.4 MEASURE OXIDE
extract name="GATEOX" thickness material="SiO~2" mat.occno=1 x.val=
structure outfile=gate_oxide.str
tonyplot -st gate_oxide.str
```



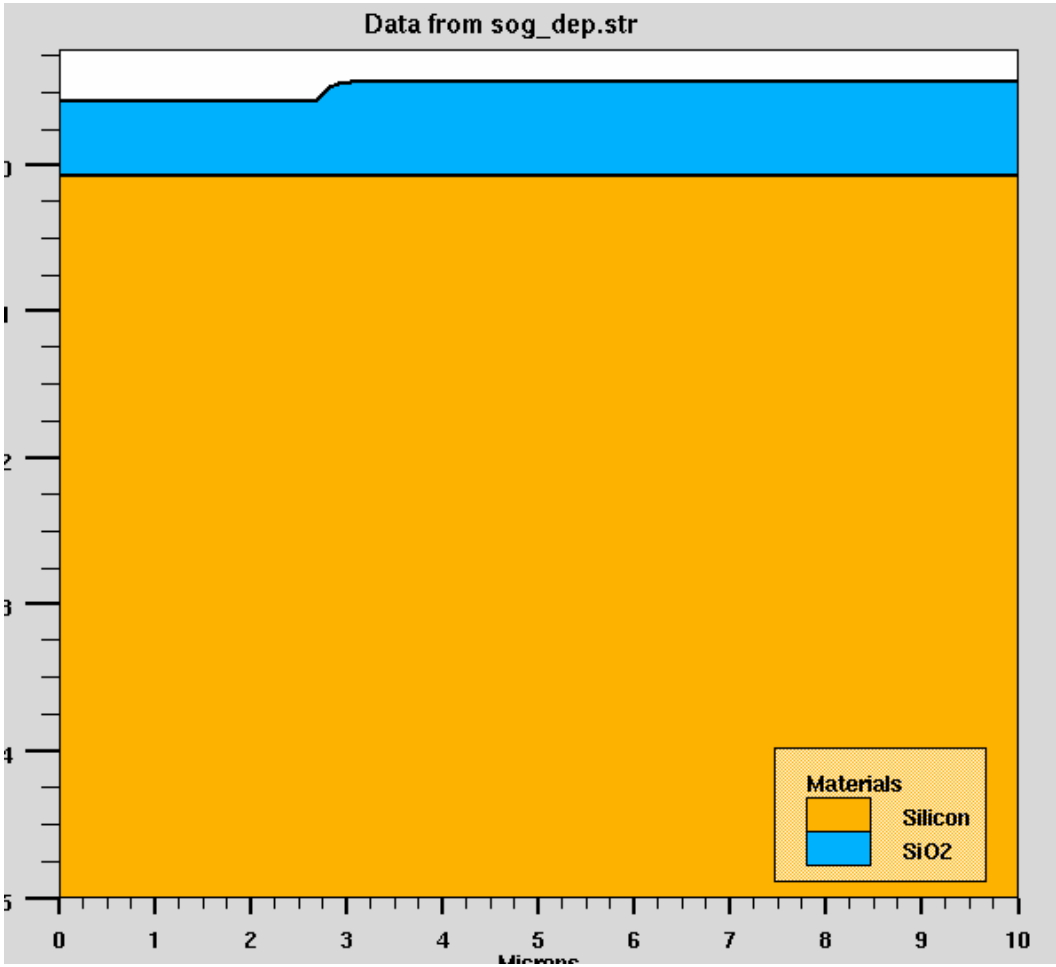
```
# MASK 1 PL ALL of STEPS 7 AND 8 ARE ASSUMED
#
etch oxide left p1.x=3
structure outfile=source_drain_etch.str
tonyplot -st source_drain_etch.str
```

S/D MASK 1



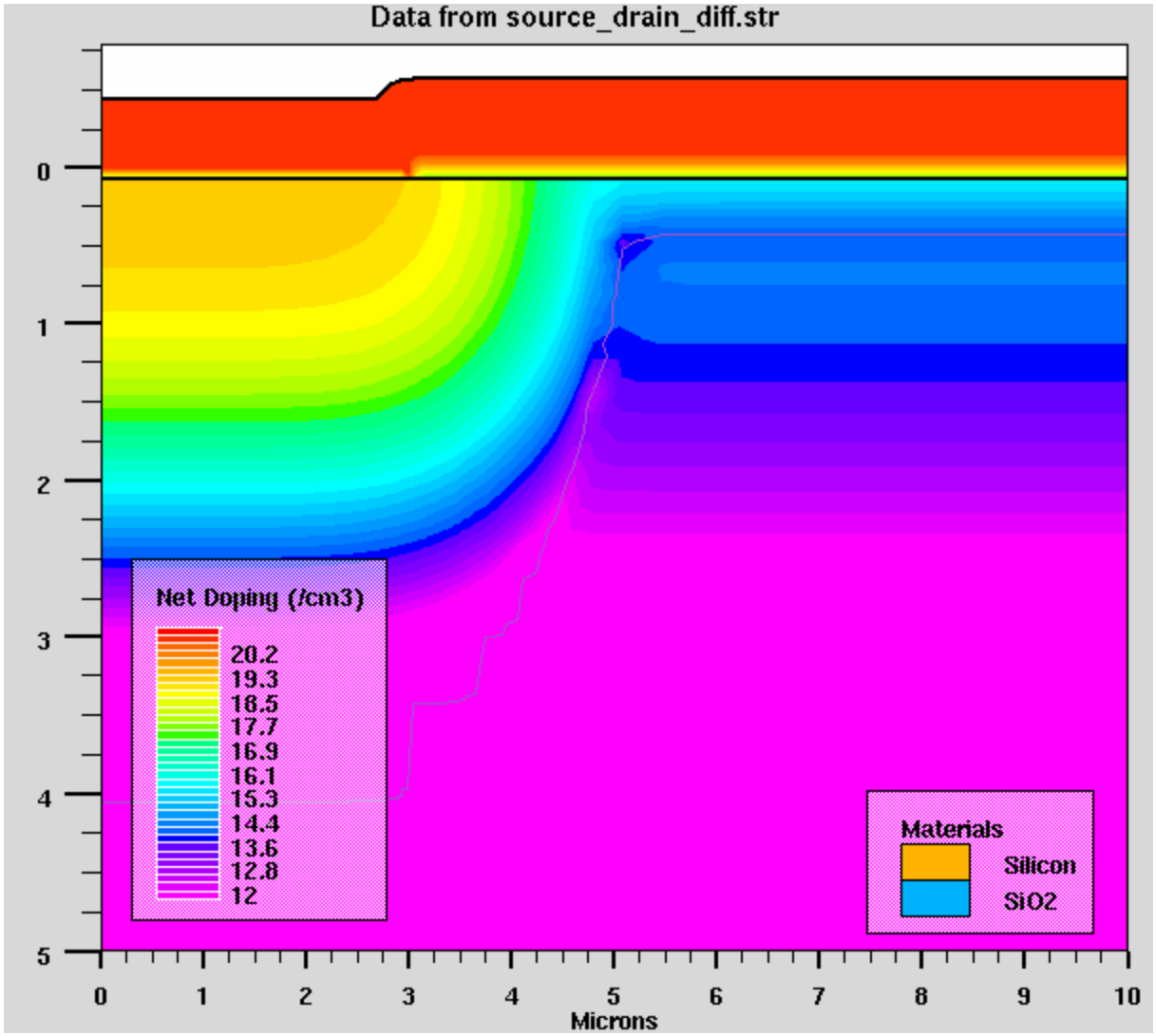
```
#STEP 9.0 APPLY P SOG STEP 9.1 ASSUMED
deposit oxide thick=0.50 c.phos=5e20 divisions=10
structure outfile=sog_dep.str
tonyplot -st sog_dep.str
```

P SOG



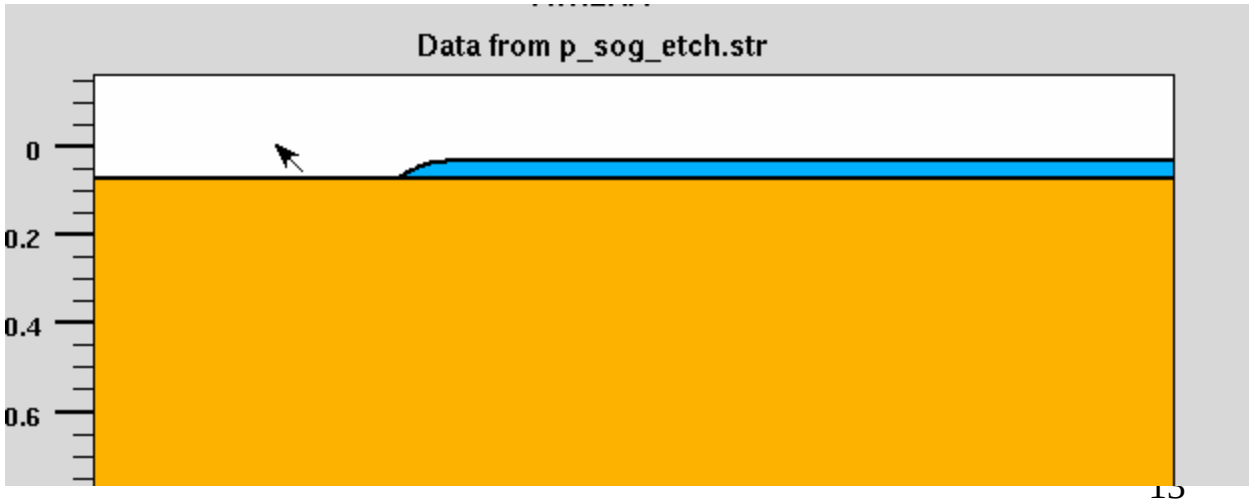
```
# P S/D DIFFUSION STEP 10.0 ASSUMED
#STEP 10.1 PUSH
diffus time=15   temp=400 t.final=900  nitro
#STEP 10.2 RAMP UP
diffus time=13.3 temp=900 t.final=1100  nitro
#STEP 10.2 STABILIZE
diffus time=5   temp=1100 nitro press=1.00
#STEP 10.2 SOAK
diffus time=100   temp=1100 nitro press=1.00
#STEP 10.2 RAMP DOWN
diffus time=40   temp=1100 t.final=900   nitro
#STEP 10.3 PULL
diffus time=15   temp=900 t.final=400  nitro
```

Diffuse Source and Drain

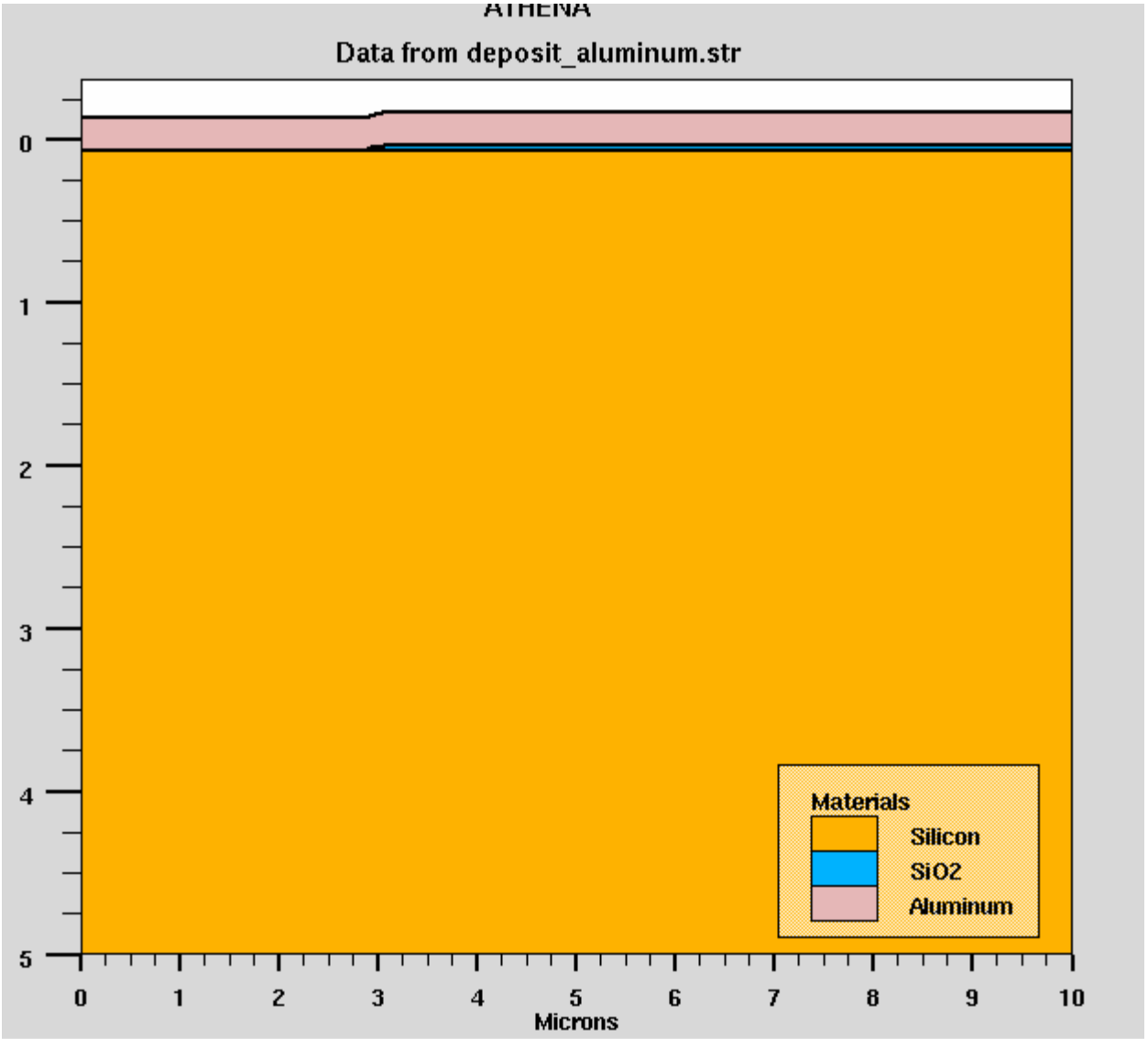


```
# STEP 11.0 ETCH SOG  THIS STEP IS FAR FROM REALITY  WE ENDED UP ETCHING over a 1000A MORE GATE OX THAN WE
EXPECTED
#
#
rate.etch machine=ETCHER oxide a.s  rie isotropic=1000 dir=0.00 chem=0.00 \
        div=0.01
#
etch machine=ETCHER time=6 seconds dx.mult=1.0 dt.fact=0.25 dt.max=0.25
structure outfile=p_sog_etch.str
tonyplot -st p_sog_etch.str
# STEP 12 DEPOSIT AL
deposit alumin thick=0.2000
structure outfile=deposit_aluminum.str
tonyplot -st deposit_aluminum.str
#
```

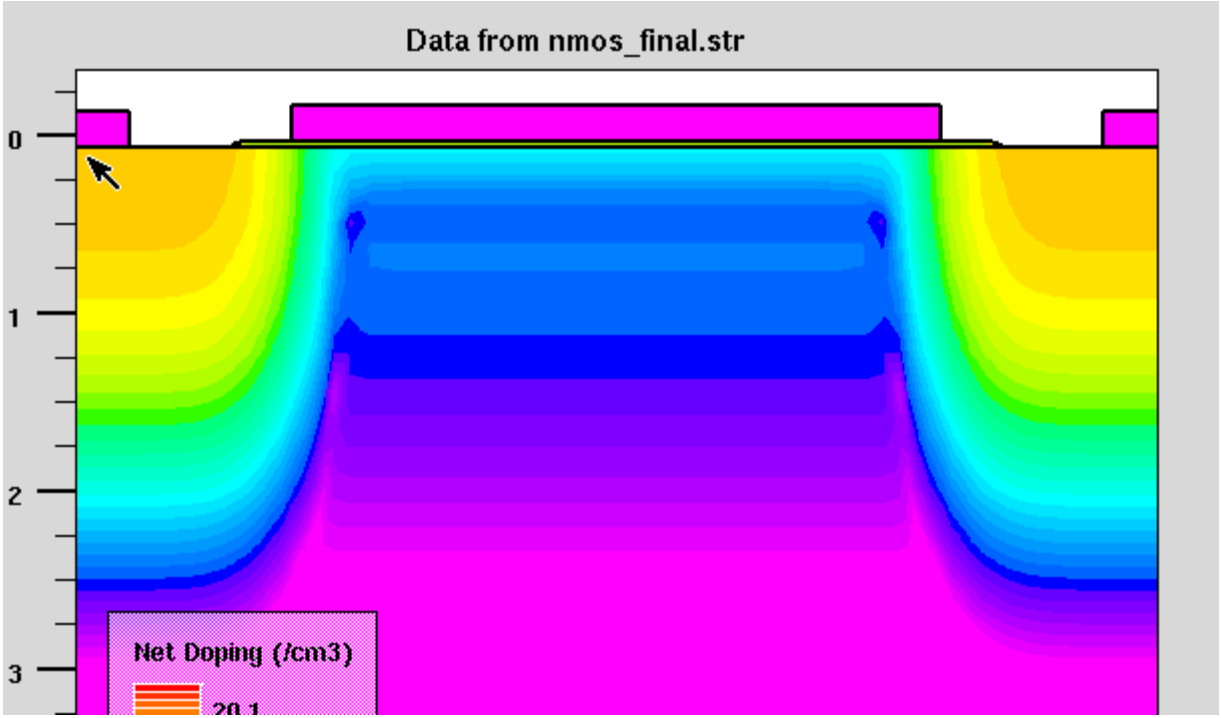
Etch P SOG, and in the process much of the gate/field oxide



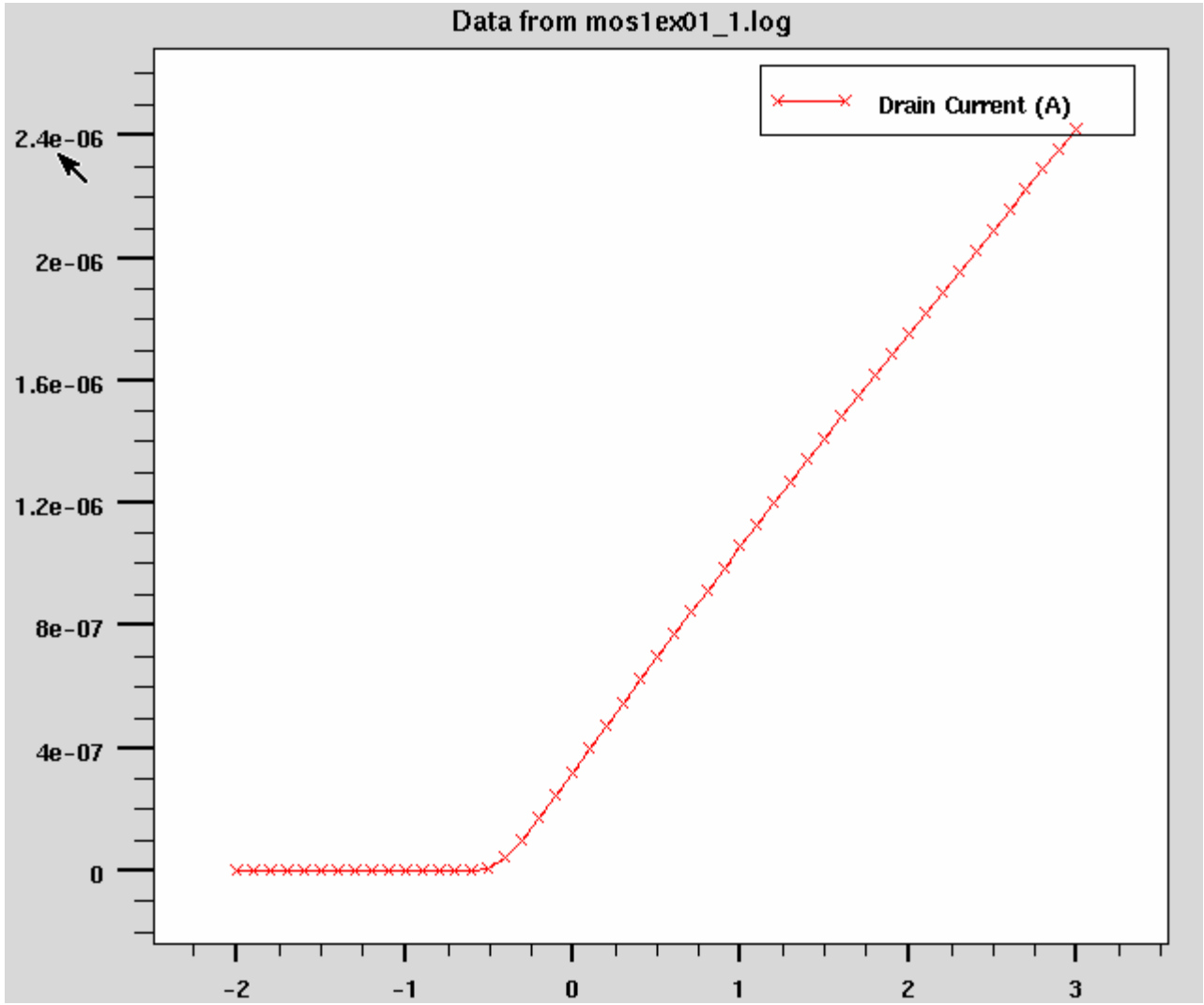
Coat with Al.


ATHENA
Data from deposit_aluminum.str
0
1
2
3
4
5
0
1
2
3
4
5
6
7
8
9
10
Microns
Materials
Silicon
SiO2
Aluminum

Etch AL and Flip Structure

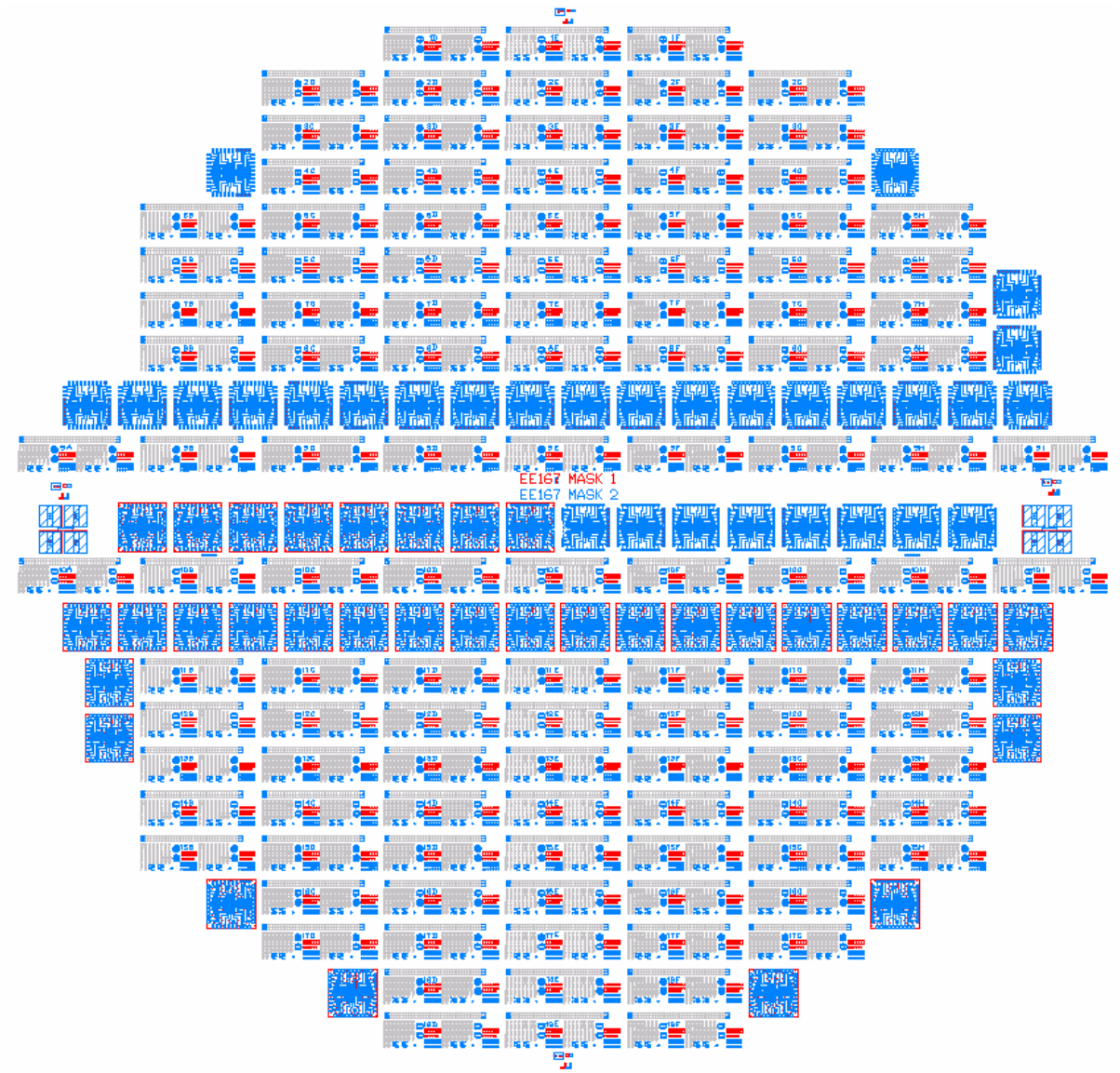


VT is Negative!

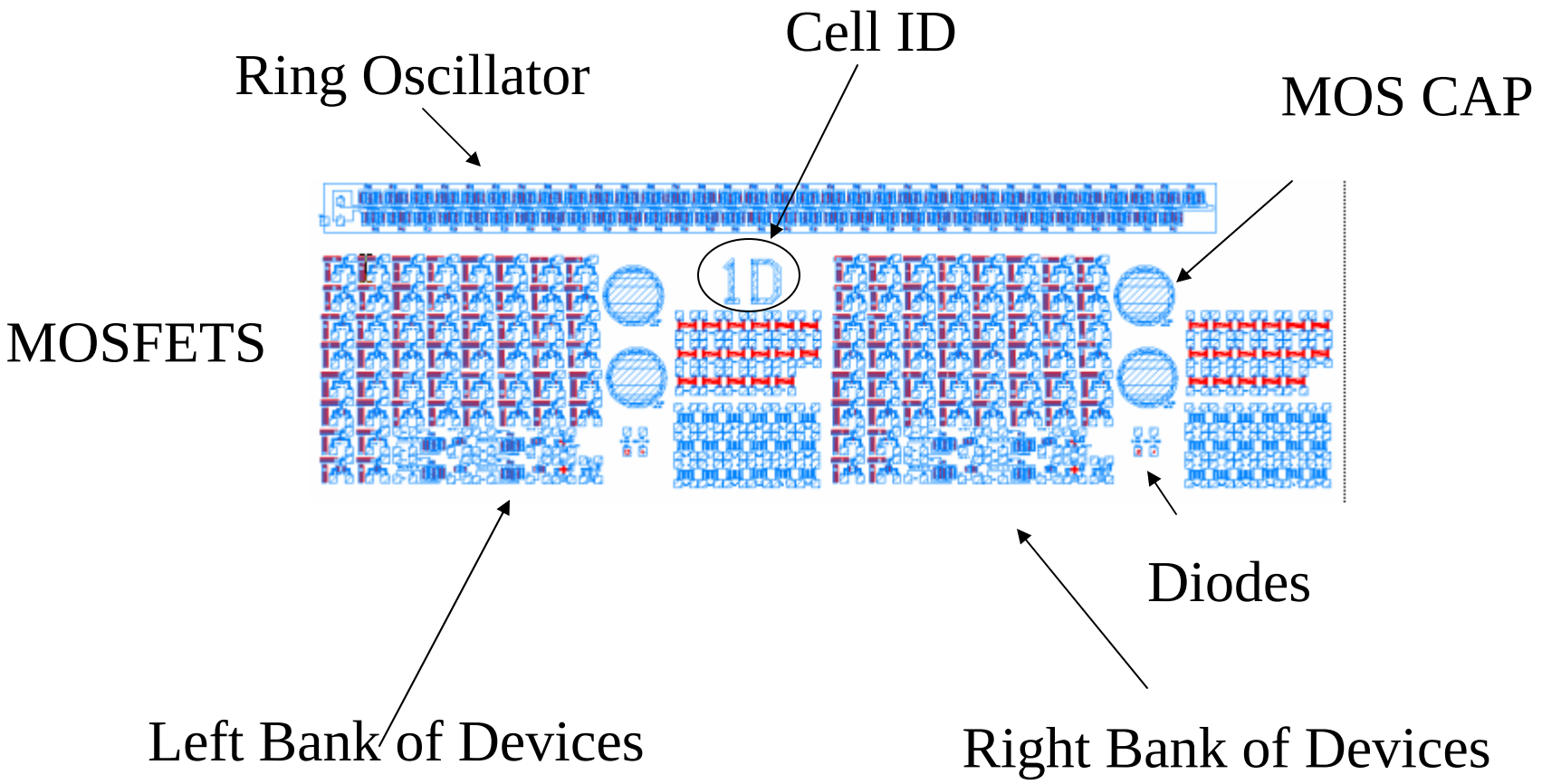


Your Mission is to Make VT positive

Top view of Wafer

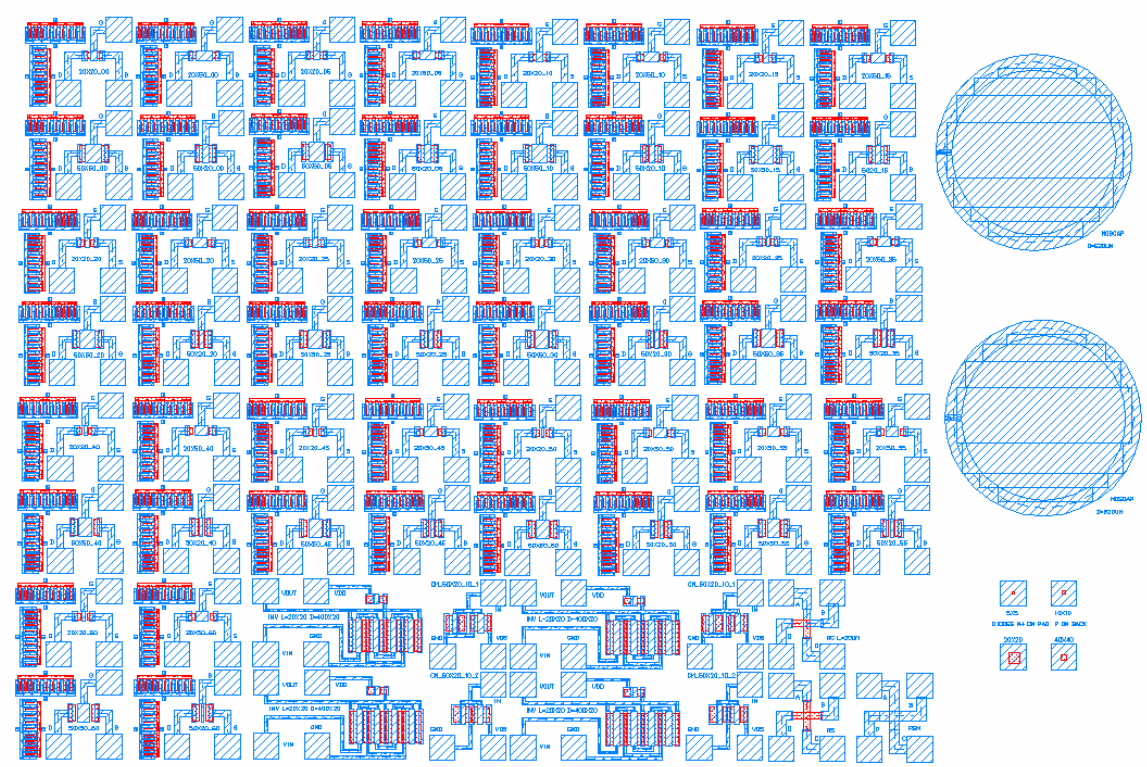


TOP View of Cell



Left or Right Bank of Devices

MOSFETS

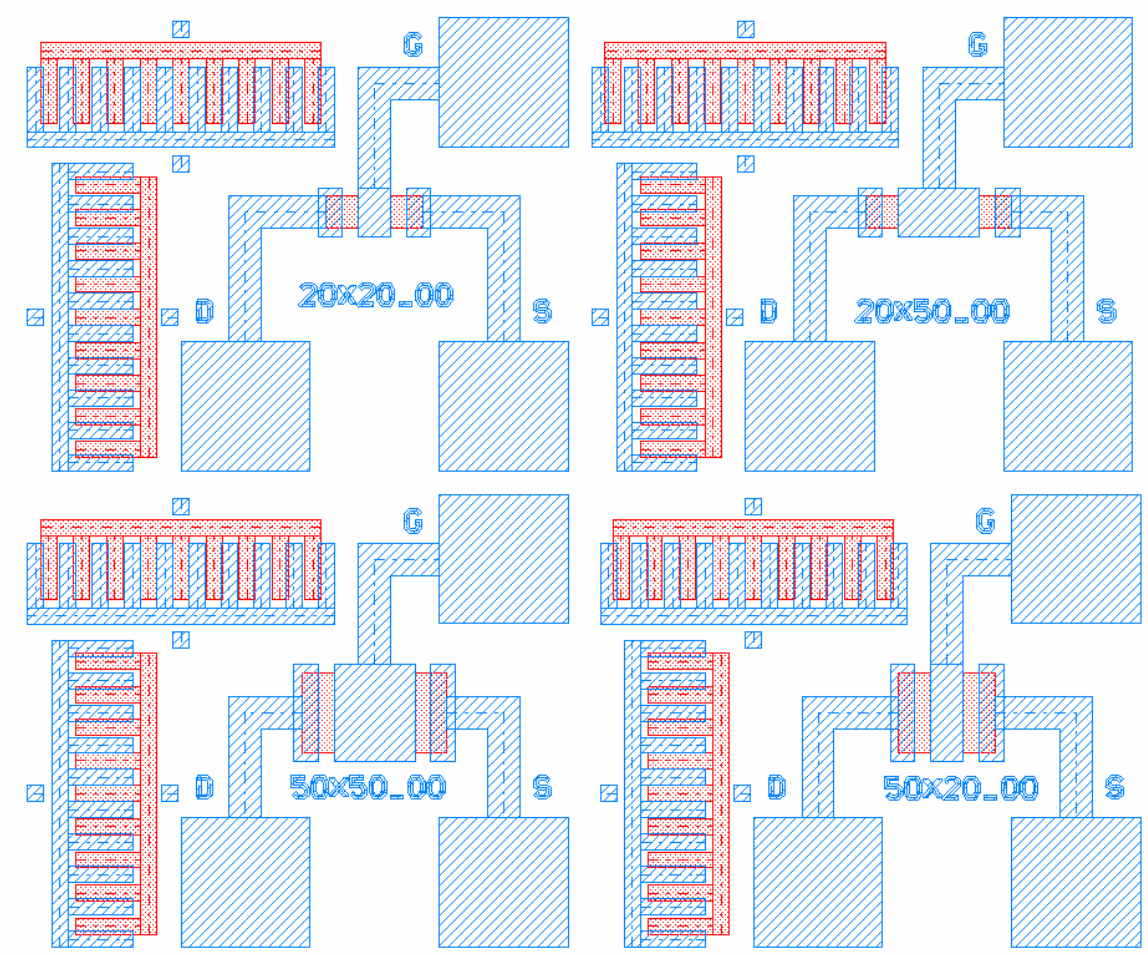


MOSCAPS

DIODES

Current Mirrors and Inverters

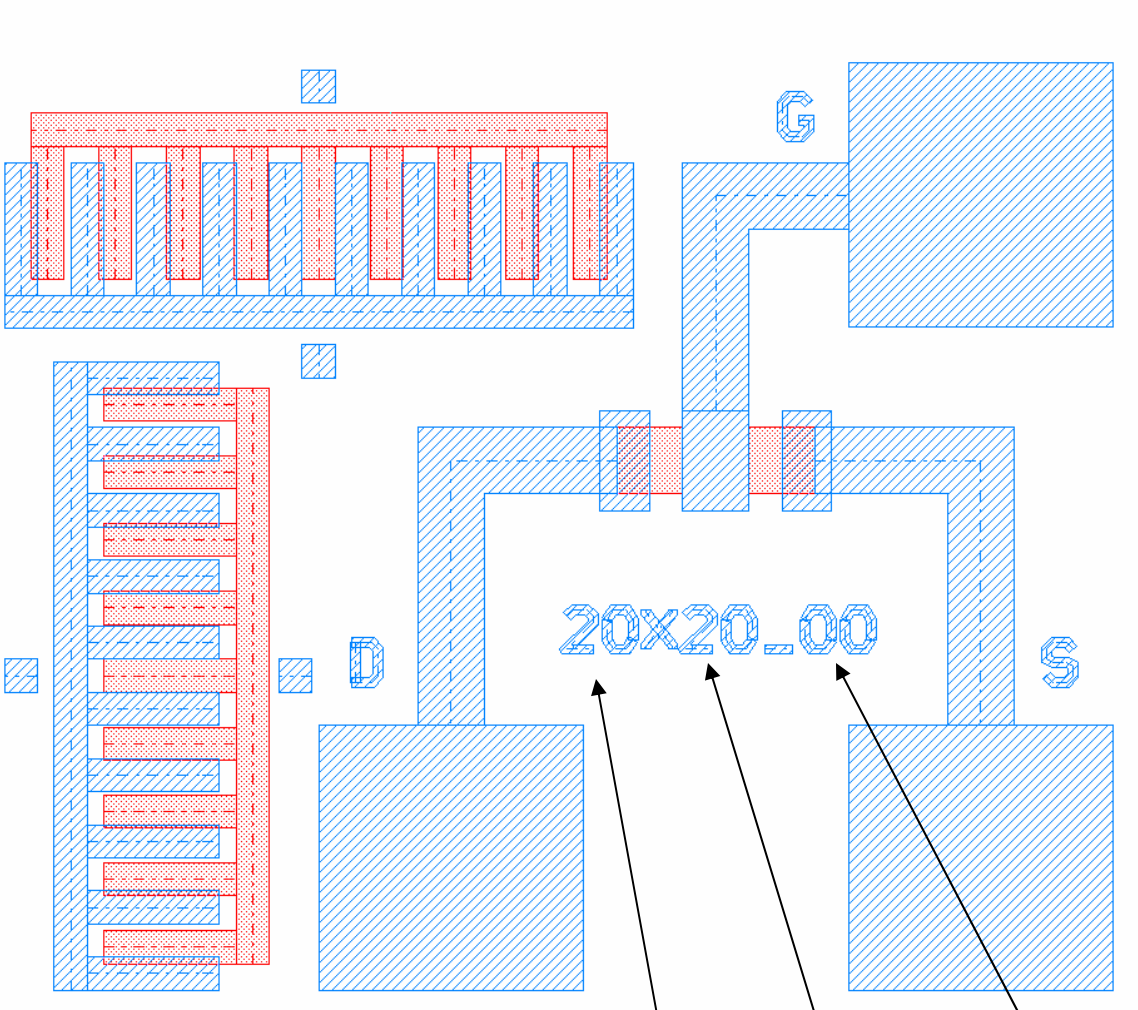
MOSFETs with various W/L ratios



MOSFET

GATE

Venier scales in .5µm increments.

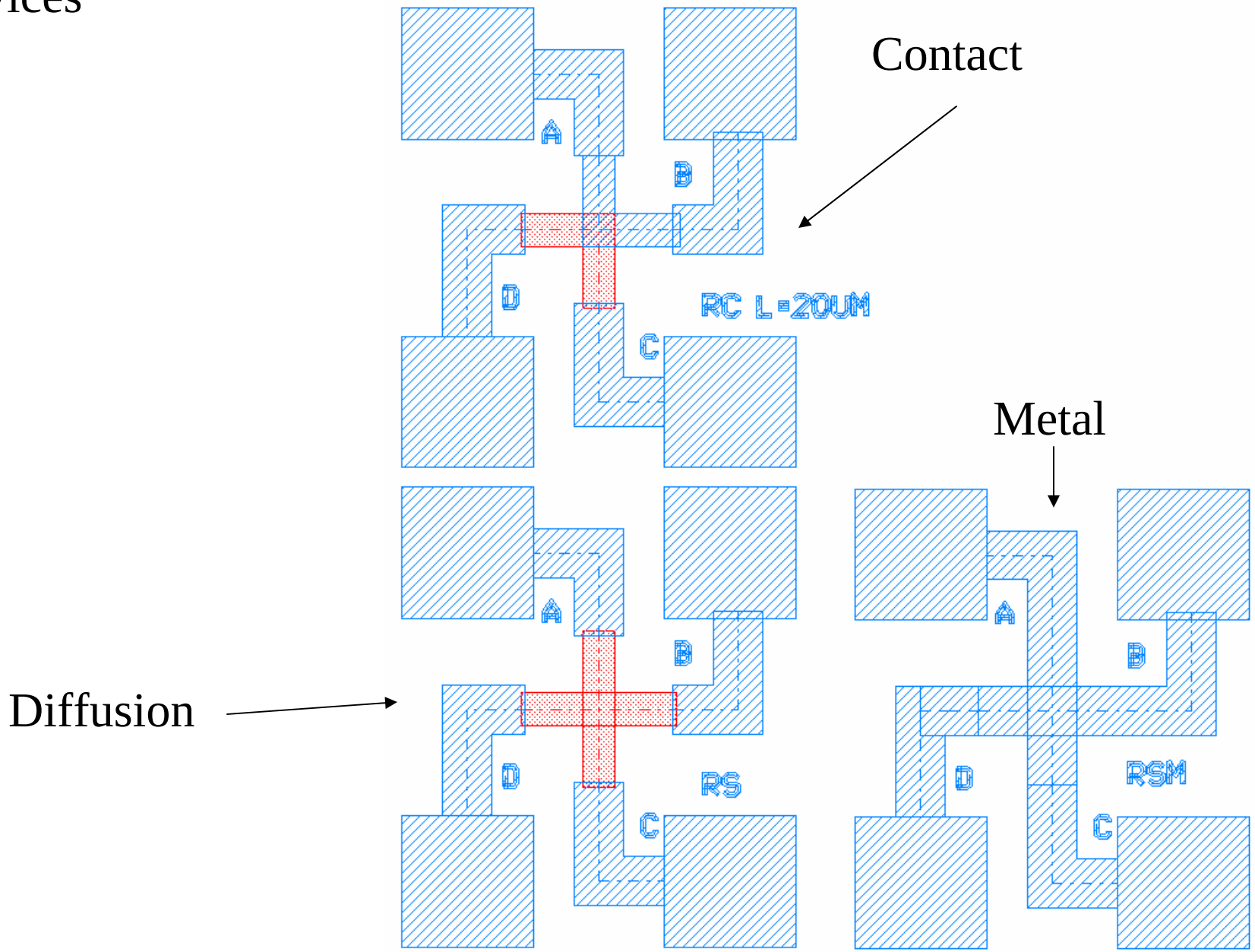


SOURCE

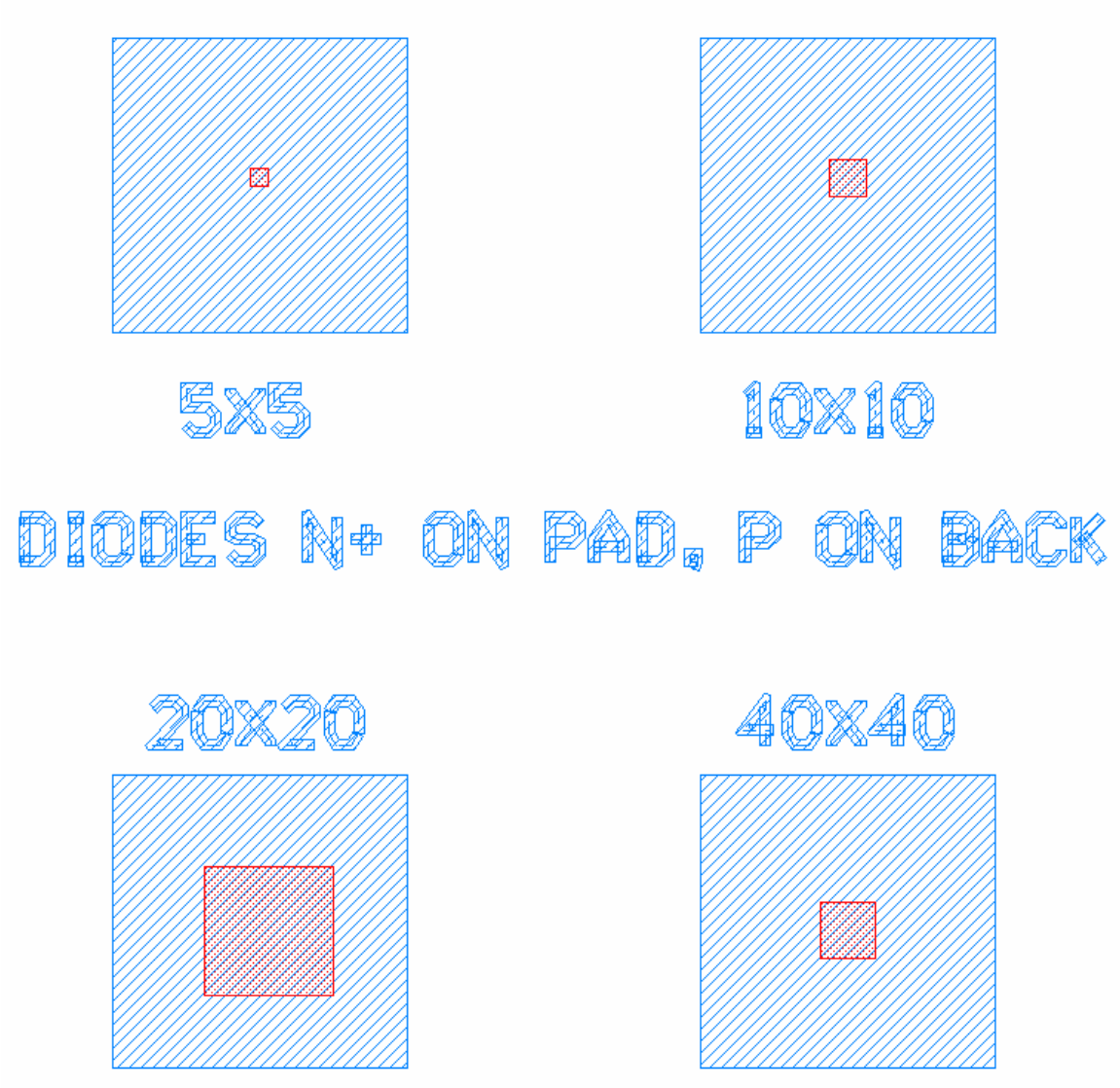
DRAIN

Width Length Offset

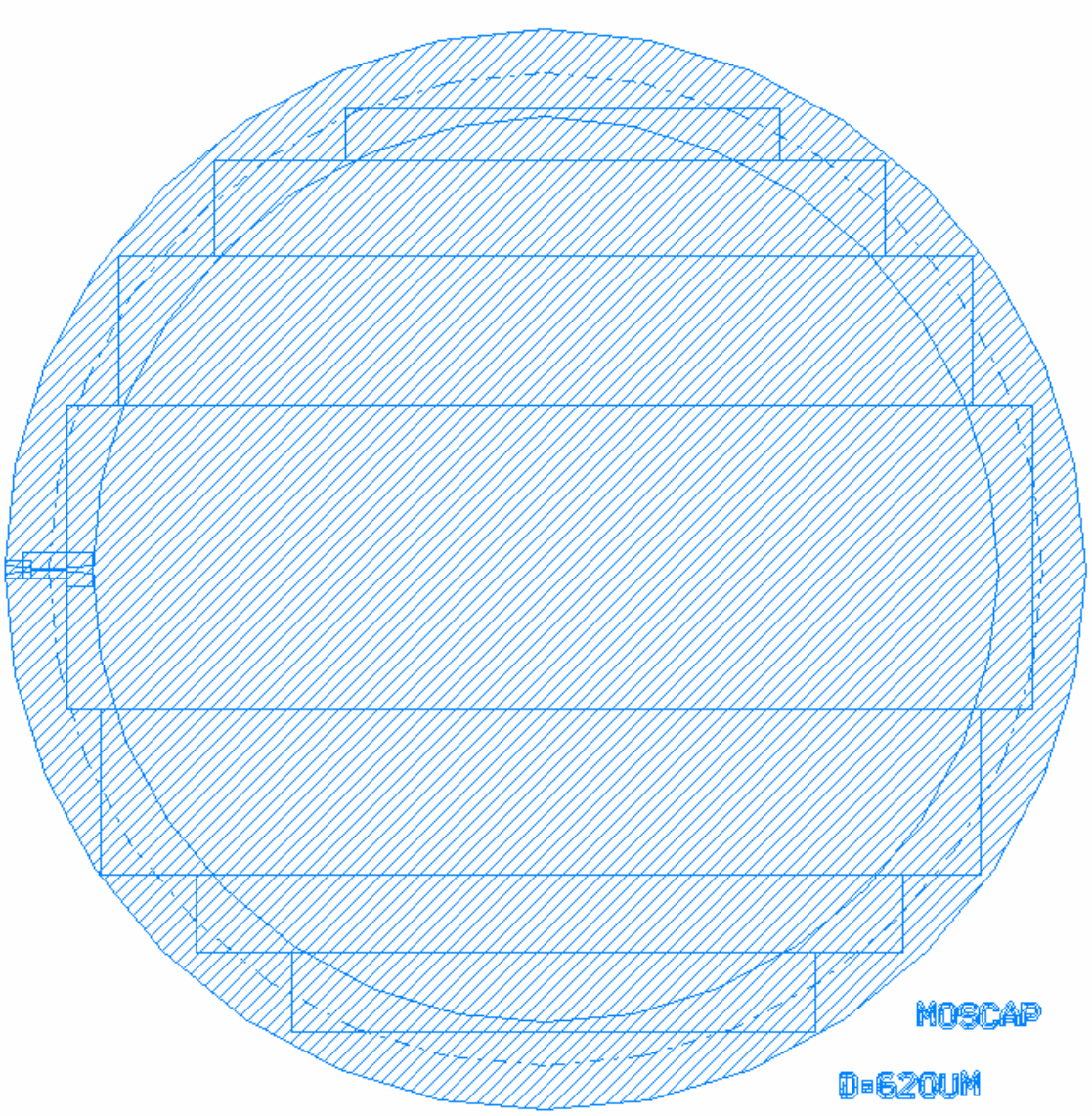
Resistance Extraction Devices



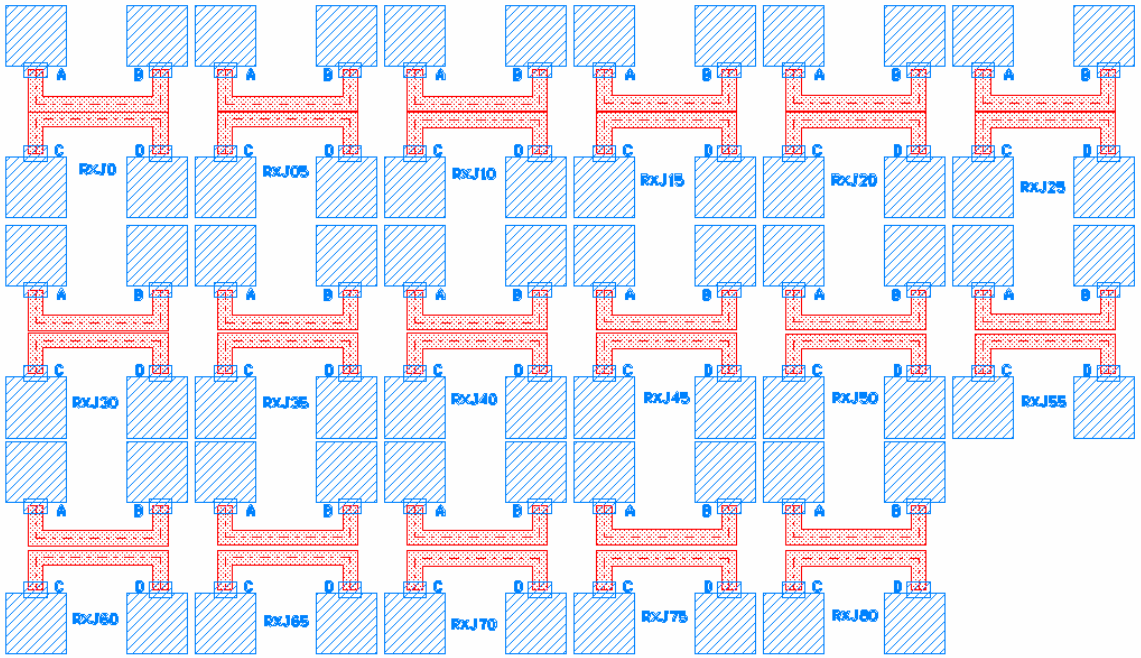
Diodes



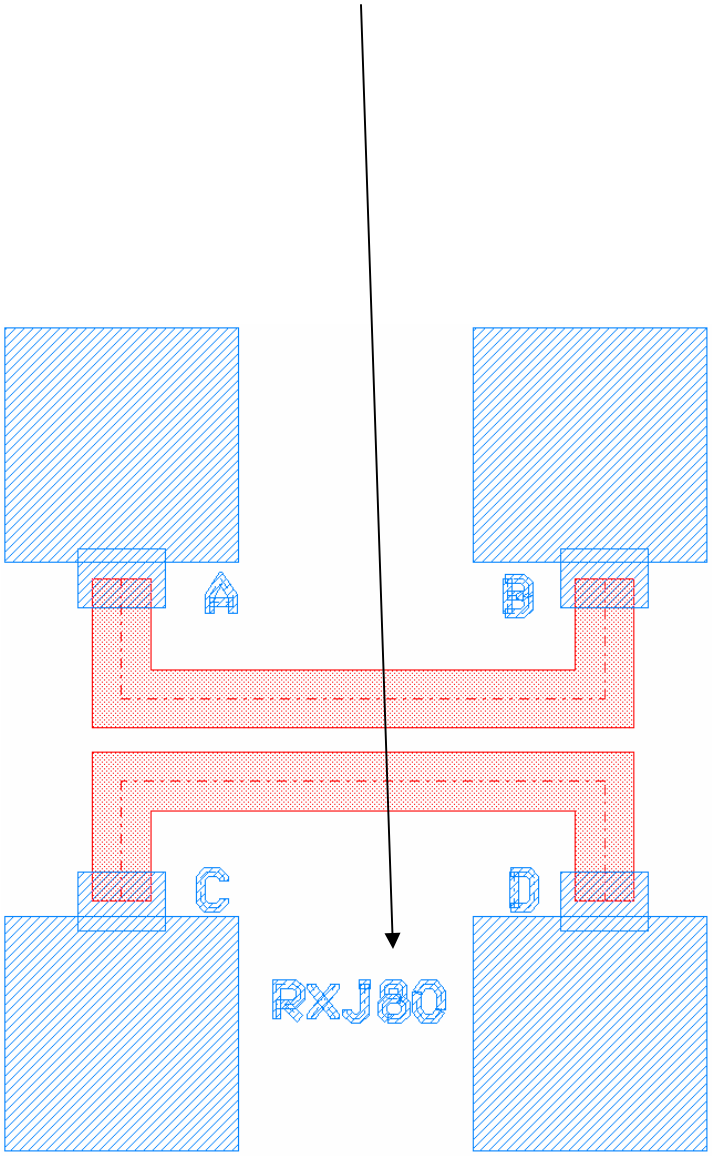
MOSCAP



Electrical Junction Depth Devices

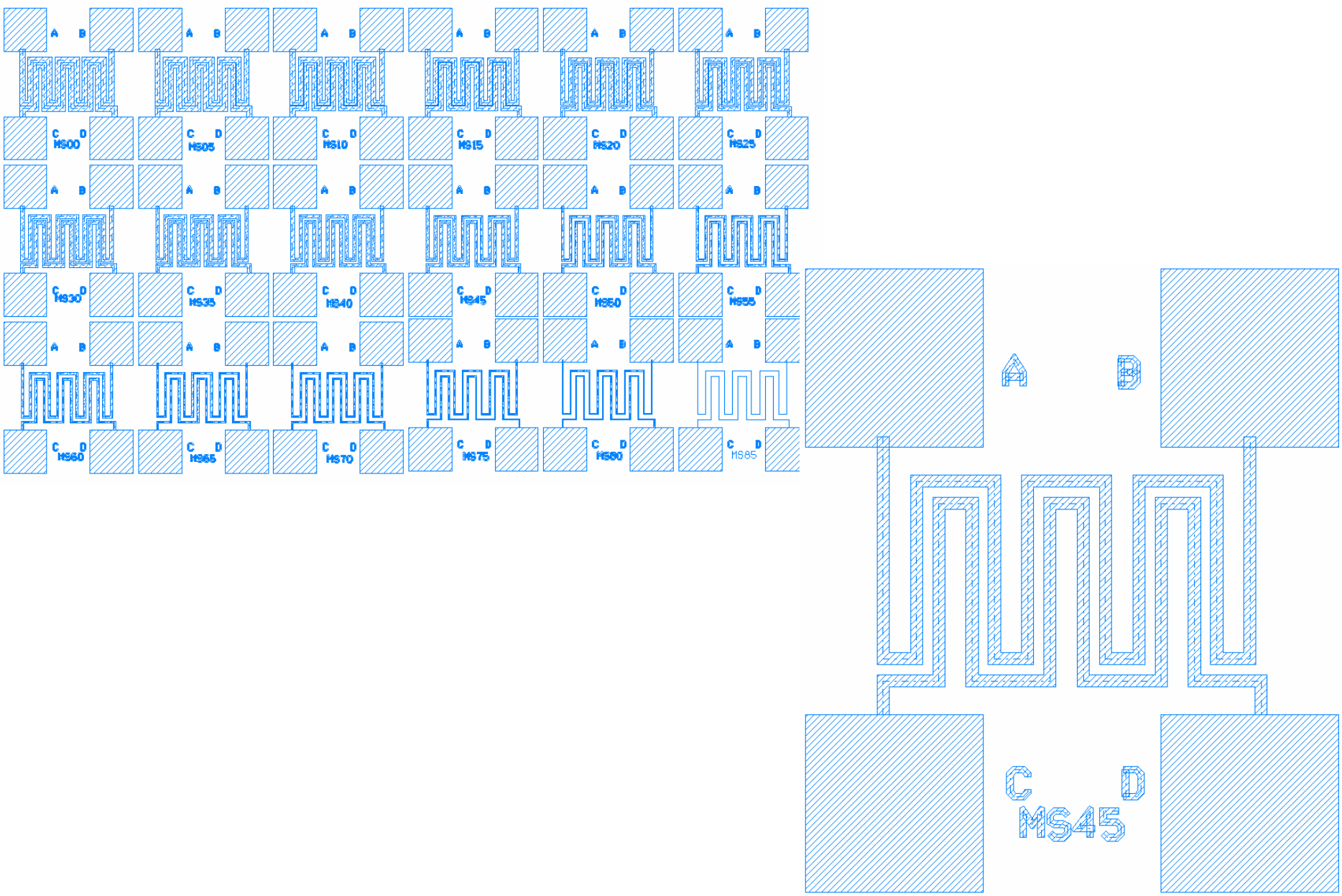


8.0 microns separation



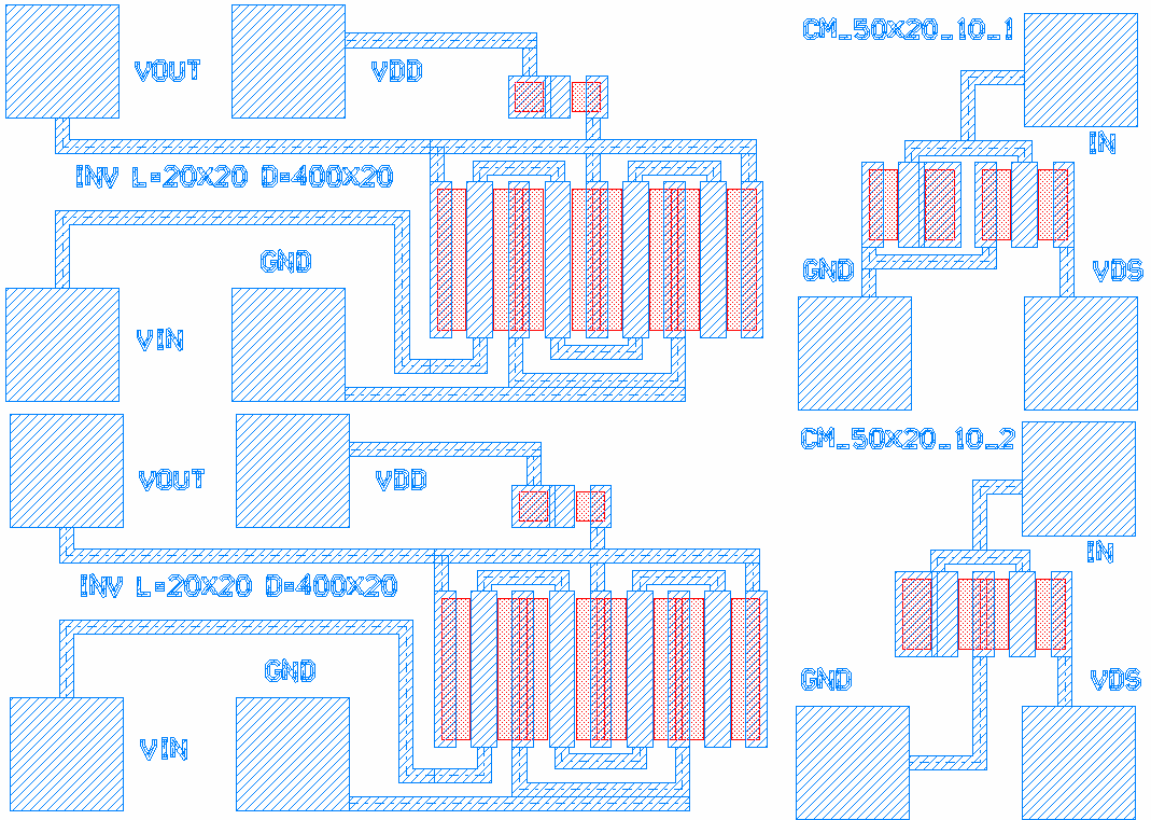
This consist of two diffused resistors separated by a gap. If the depletion widths do not touch
then no current should flow from A to C or D
Current flow form a to B or C to D mean the probes are properly connected.

Metal Serpentine test structure



Circuits

Inverters



Current Mirrors

Various Equations for resistance extraction

Device	Test	Set up	Equation	Notes
NSEL Greek Cross	Sheet Resistance Ω/square	Pass Current from pin A to B and measure voltage from D to C.	$R_S = \frac{\pi}{\ln 2} \times \frac{V_{DC}}{I_{AB}}$	
NSEL/METAL1 Contact	Contact Resistance Ω/cm^2	Pass Current from pin A to C and measure voltage from pin B to D.	$\rho_C = \frac{V_{BD}}{I_{AC}} \times l^2$	l=20x10^{-4}cm This will vary across chip. This is the as drawn length of the contact.
METAL1 Greek Cross	Sheet Resistance Ω/square	Pass Current from pin A to B and measure voltage from D to C.	$R_S = \frac{\pi}{\ln 2} \times \frac{V_{DC}}{I_{AB}}$	

Your Mission

- Develop a process to make the VT between .5 and 1 volt.
- Determine what is the optimum gate offset based on the SPC of the lithography