嵌入式系统结构与设计课程实验

实验报告 9

ALU (Arithmetic and Logic Unit) Design and ALU Pipeline

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Content

1. Target

- Design an ALU (arithmetic logic unit)
- Further understand and use timing/area/power report to optimize the design

2. Arithmetic and Logic Unit

2.1 Designing

The most important step is to design the available operation list. By following the operation list, actual ALU implementation is much easier.

Since the available operations of ALU are directly affected what the CPU can execute, and the optimization of the ALU is related to the CPU requirements, I have to wait until our CPU design instruction comes out. I'm sorry for the latency of my assignment, but I really want to implement a complete and optimal ALU.

The available ALU operations are as followed.

(*See Appendix 2: ALU Operation List*)

In accord to special CPU design for optimization, only a half of the CPU's instructions are necessary being an individual operation within the ALU, thus a 5-bit-instruction CPU requires only a 4-bit-opcode ALU. And these operation codes are allocated after `10000` of the instruction code table.

2.2 Simulation

Test is based on texture test bench, and the result is as followed.

```
TEST 01 : (1)0000 [ADD]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0000:f002:0fff:0   :0001:1   :0   :0

TEST 02 : (1)0001 [ADDI]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0001:102c:59ff:0   :6a2b:0   :0   :0

TEST 03 : (1)0010 [ADDC]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0010:2008:0108:1   :2111:0   :0   :0
```

```
TEST 04 : (1)0011 [SUB]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0011:1000:08ff:0   :0701:0   :0   :0

TEST 05 : (1)0100 [SUBI]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0100:0001:1000:0   :f001:0   :0   :1

TEST 06 : (1)0101 [SUBC]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0101:1000:0fff:1   :0000:0   :1   :0

TEST 07 : (1)0110 [INC]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0110:0fff:0000:0   :1000:0   :0   :0

TEST 08 : (1)0111 [CMP] - less
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0111:21fc:2f56:0   :0000:0   :1   :0

TEST 09 : (1)0111 [CMP] - equal
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0111:64ff:64ff:0   :0000:0   :1   :0

TEST 10 : (1)0111 [CMP] - larger
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
0111:b9a8:975f:0   :0000:0   :1   :0

TEST 11 : (1)1000 [TRAN]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1000:56fc:0000:0   :56fc:0   :0   :0

TEST 12 : (1)1001 [XOR]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1001:ff0f:f0fa:0   :0ff5:0   :0   :0

TEST 13 : (1)1010 [AND]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1010:f00f:ff0a:0   :f00a:0   :0   :0

TEST 14 : (1)1011 [OR]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1011:f00f:ff0a:0   :ff0f:0   :0   :0
```

```
TEST 15 : (1)1100 [SLL]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1100:f0f0:0004:0   :0f00:1   :0   :0

TEST 16 : (1)1101 [SLA]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1101:0f0f:0004:0   :f0f0:0   :0   :0

TEST 17 : (1)1110 [SRL]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1110:f000:0004:0   :0f00:0   :0   :0

TEST 18 : (1)1111 [SRA]
OPC :IN1 :IN2 :ICF :OUT :OCF :OZF :ONF
1111:f0ff:0004:0   :ff0f:1   :0   :0
```

2.3 Synthesization and RTL diagram

After Synthesization RTL diagram of the design is generated.

The RTL diagram of the core module, the `ALU` module, generated from Synthesization is as below.

(*See Appendix 3: RTL Diagram*)

2.4 Design Summary

Device utilization summary:

```
Slice Logic Utilization:
 Number of Slice LUTs:                  246  out of   9112     2%
    Number used as Logic:               246  out of   9112     2%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    246
   Number with an unused Flip Flop:     246  out of    246   100%
   Number with an unused LUT:             0  out of    246     0%
   Number of fully used LUT-FF pairs:     0  out of    246     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                          56
 Number of bonded IOBs:                  56  out of    232    24%

Specific Feature Utilization:
```

Timing Constraints:

The timing constraints report is as follow.

(*See Appendix 4: Timing Constraints Report*)

Power Report:

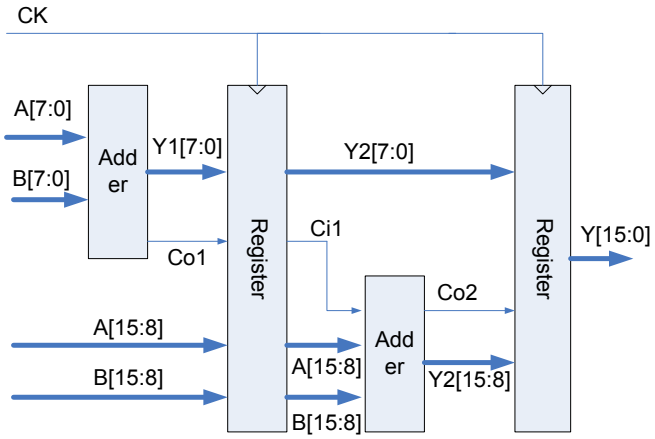
On-Chip Power Summary

On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	0.00	0	---	---
Logic	0.00	235	9112	3
Signals	0.00	274	---	---
IOs	0.00	56	232	24
Quiescent	14.84			
Total	14.84			

3. ALU Pipeline Example

3.1 Design

In pipeline ALU design, the implementation is not complete, rather only addition operation is implemented as an example. The design follows the following architecture.



There are 2 stages of pipeline in this design, with each computing 8 bits of the inputs.

3.2 Simulation

The simulation involves 4 clock trigger pulses, and inputs of each pulse are as followed.

Clock#	Input		
	IN1	IN2	Carry
1	01FF	0102	0
2	1F05	0100	0
3	0	0	0
4	0	0	0

The result of simulation is as followed.

```
Pipeline ALU example testing
IN1 :IN2 :ICF ::OUT :OCF :OZF :ONF
01ff:0102:0   ::0000:0   :x   :x
1f05:0100:0   ::0000:0   :x   :x
0000:0000:0   ::0301:0   :0   :0
0000:0000:0   ::2005:0   :0   :0
0000:0000:0   ::0000:0   :0   :0
```

2.3 Synthesization and RTL diagram

After Synthesization RTL diagram of the design is generated.

The RTL diagram of the core module, the `ALUP2` module, generated from Synthesization is as below.

(*See Appendix 5: RTL Diagram of ALU Pipeline Example*)

2.4 Design Summary

Device utilization summary:

```
Slice Logic Utilization:
 Number of Slice Registers:              36  out of  18224     0%
 Number of Slice LUTs:                   27  out of   9112     0%
    Number used as Logic:                19  out of   9112     0%
    Number used as Memory:                8  out of   2176     0%
       Number used as SRL:                8

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     46
   Number with an unused Flip Flop:      10  out of     46    21%
   Number with an unused LUT:            19  out of     46    41%
   Number of fully used LUT-FF pairs:    17  out of     46    36%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                          53
 Number of bonded IOBs:                  53  out of    232    22%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%
```

Timing Report:

The timing report is as follow.

```
Clock to Setup on destination clock CLK
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
CLK            |    2.863|         |         |         |
---------------+---------+---------+---------+---------+
```

Power Report:

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	0.01	1	---	---
Logic	0.00	24	9112	0
Signals	0.00	82	---	---
IOs	0.00	53	232	23
Quiescent	14.84			
Total	14.86			

Afterthought

CPU design is a big topic: a lot of technologies, theories, techniques and knowledge are required. Since the CPU is exact a highly coupling module, one has to think hard to optimize the design until the final product comes out. Hence, I am half exciting and half worrying about this assignment.

As I once thought, merely the design of ALU, a component of the CPU, costs me a lot of time.

To build an experimental, or says example, ALU is easy with the guidance from our teacher. However, what I want to build is an ALU fit and optimized for the later CPU design, which means these two designs is highly coupling but quite optimized that they seem to be exactly one piece.

So I had to wait for the final assignment of our CPU design, before I could start to build my ALU. What's more, I consider this project a real one, so I pushed it as a currently not visible open source project. What I mean by invisible is because I do not want my homework be copied, so I just hide it from the public currently, but later I will make it visible. A lot of documentation and details are required in my design. So I design the both the operation tables of CPU and ALU together, actually. To apply a lot of tricks in the design actually cost a majority of my time on this project, for example, the order of operation code allocation.

I wanted to optimize this design as far as possible, but the payment is time. I am so sorry that I submit my homework so late. But the outcome is not so bad, because merely all my initial expectations finally come true in my design.

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2013.12.24

Appendix 1: Attachment List

1. ALU

    \ ALU.v

    \ ALU_test01.v

2. ALU pipeline example

    \ ALUP2_example.v

    \ ALUP2_example_test01.v

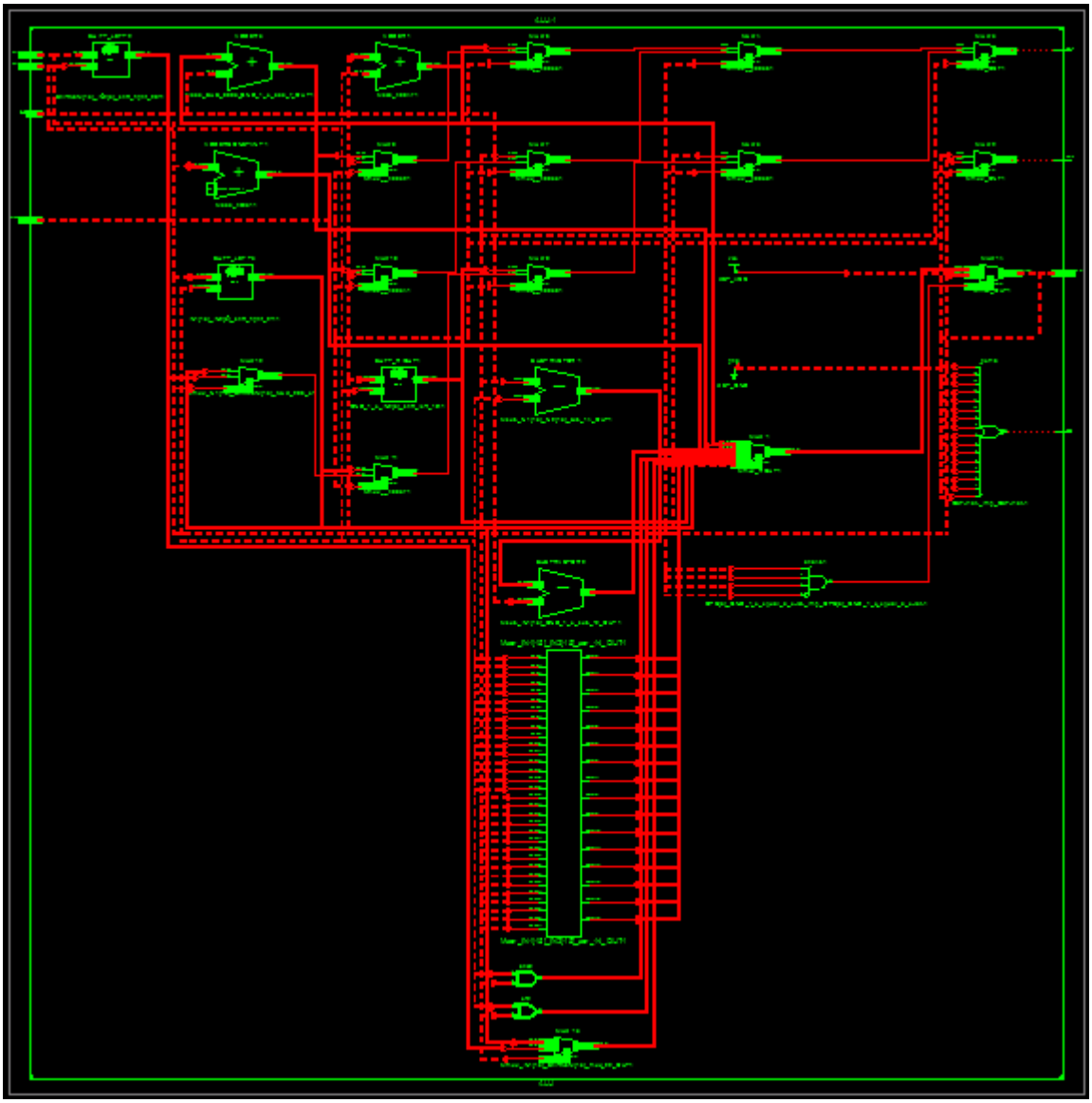
X.v files are primary code files; X_test.v files are test files.

Appendix 2: ALU Operation List

Arithmetic and Logic Unit Operation List

Category	Mnemonic	Input1	Input2	Input Flags	Output	Output Flags	Opcode	Full Name	Operation
Arithmetic	ADD	bit[16]	bit[16]	/	bit[16]	CF, ZF, NF	0000	ADD	Input1+Input2 -> Output
	ADDI	bit[16]	bit[16]	/	bit[16]	CF, ZF, NF	0001	ADD IMMEDIATE	Input1+Input2 -> Output
	ADDC	bit[16]	bit[16]	CF	bit[16]	CF, ZF, NF	0010	ADD CARRY	Input1+Input2+Carry -> Output
	SUB	bit[16]	bit[16]	/	bit[16]	CF, ZF, NF	0011	SUBTRACT	Input1-Input2 -> Output
	SUBI	bit[16]	bit[16]	/	bit[16]	CF, ZF, NF	0100	SUBTRACT IMMEDIATE	Input1-Input2 -> Output
	SUBC	bit[16]	bit[16]	CF	bit[16]	CF, ZF, NF	0101	SUBTRACT CARRY	Input1-Input2-Borrow -> Output
	INC	bit[16]	/	/	bit[16]	CF, ZF, NF	0110	INCREASE	Input1+1 -> Output
	CMP	bit[16]	bit[16]	/	0	CF, ZF, NF	0111	COMPARE	Input1-Input2
Special	TRAN	bit[16]	/	/	bit[16]	ZF	1000	TRANSFER	Input1 -> Output
Logic	XOR	bit[16]	bit[16]	/	bit[16]	ZF	1001	EXCLUSIVE OR	Input1 XOR Input2 -> Output
	AND	bit[16]	bit[16]	/	bit[16]	ZF	1010	AND	Input1 AND Input2 -> Output
	OR	bit[16]	bit[16]	/	bit[16]	ZF	1011	OR	Input1 OR Input2 -> Output
Shift	SLL	bit[16]	bit[16]	/	bit[16]	CF, ZF	1100	SHIFT LEFT LOGICAL	{CF, Input1, 0} << Input2[3:0] -> Output
	SLA	bit[16]	bit[16]	/	bit[16]	CF, ZF	1101	SHIFT LEFT ARITHMETICAL	{CF, Input1, 0} << Input2[3:0] -> Output
	SRL	bit[16]	bit[16]	/	bit[16]	CF, ZF	1110	SHIFT RIGHT LOGICAL	{0, Input1, CF} >> Input2[3:0] -> Output
	SRA	bit[16]	bit[16]	/	bit[16]	CF, ZF	1111	SHIFT RIGHT ARITHETICAL	{Input1[0], Input1, CF} >> Input2[3:0] -> Output

Appendix 3: RTL Diagram



Appendix 4: Timing Constraints Report

All values displayed in nanoseconds (ns)

Pad to Pad

Source Pad	Destination Pad	Delay
ICF	OCF	12.463
ICF	ONF	12.773
ICF	OUT<0>	12.032
ICF	OUT<1>	12.327
ICF	OUT<2>	11.515
ICF	OUT<3>	12.177
ICF	OUT<4>	13.068
ICF	OUT<5>	11.950
ICF	OUT<6>	12.756
ICF	OUT<7>	12.149
ICF	OUT<8>	12.227
ICF	OUT<9>	13.008
ICF	OUT<10>	12.944
ICF	OUT<11>	12.878
ICF	OUT<12>	13.428
ICF	OUT<13>	13.128
ICF	OUT<14>	12.531
ICF	OUT<15>	13.458
ICF	OZF	15.103
IN1<0>	OCF	13.174
IN1<0>	ONF	14.526
IN1<0>	OUT<0>	12.970
IN1<0>	OUT<1>	14.613
IN1<0>	OUT<2>	13.583
IN1<0>	OUT<3>	15.084
IN1<0>	OUT<4>	14.173
IN1<0>	OUT<5>	13.683
IN1<0>	OUT<6>	14.047
IN1<0>	OUT<7>	13.692
IN1<0>	OUT<8>	14.116
IN1<0>	OUT<9>	15.145
IN1<0>	OUT<10>	14.369
IN1<0>	OUT<11>	13.902
IN1<0>	OUT<12>	14.734
IN1<0>	OUT<13>	13.849
IN1<0>	OUT<14>	13.242
IN1<0>	OUT<15>	15.059
IN1<0>	OZF	17.591
IN1<1>	OCF	13.650
IN1<1>	ONF	14.651
IN1<1>	OUT<0>	11.071
IN1<1>	OUT<1>	14.689
IN1<1>	OUT<2>	13.659
IN1<1>	OUT<3>	15.160
IN1<1>	OUT<4>	14.249
IN1<1>	OUT<5>	13.759
IN1<1>	OUT<6>	14.123
IN1<1>	OUT<7>	13.768
IN1<1>	OUT<8>	14.192
IN1<1>	OUT<9>	15.221
IN1<1>	OUT<10>	14.445
IN1<1>	OUT<11>	14.050
IN1<1>	OUT<12>	14.810
IN1<1>	OUT<13>	14.315
IN1<1>	OUT<14>	13.718
IN1<1>	OUT<15>	15.184
IN1<1>	OZF	17.667
IN1<2>	OCF	13.174
IN1<2>	ONF	13.912
IN1<2>	OUT<0>	11.083
IN1<2>	OUT<1>	10.237
IN1<2>	OUT<2>	12.488
IN1<2>	OUT<3>	13.985
IN1<2>	OUT<4>	13.305
IN1<2>	OUT<5>	12.602
IN1<2>	OUT<6>	13.272
IN1<2>	OUT<7>	12.917
IN1<2>	OUT<8>	13.364
IN1<2>	OUT<9>	14.393
IN1<2>	OUT<10>	13.636
IN1<2>	OUT<11>	13.574
IN1<2>	OUT<12>	14.139
IN1<2>	OUT<13>	13.839
IN1<2>	OUT<14>	13.242
IN1<2>	OUT<15>	14.445
IN1<2>	OZF	16.492

IN1<3>	OCF	12.946
IN1<3>	ONF	14.101
IN1<3>	OUT<0>	10.740
IN1<3>	OUT<1>	10.619
IN1<3>	OUT<2>	12.057
IN1<3>	OUT<3>	14.027
IN1<3>	OUT<4>	13.214
IN1<3>	OUT<5>	12.710
IN1<3>	OUT<6>	13.461
IN1<3>	OUT<7>	13.106
IN1<3>	OUT<8>	13.553
IN1<3>	OUT<9>	14.582
IN1<3>	OUT<10>	13.806
IN1<3>	OUT<11>	13.346
IN1<3>	OUT<12>	14.171
IN1<3>	OUT<13>	13.611
IN1<3>	OUT<14>	13.014
IN1<3>	OUT<15>	14.634
IN1<3>	OZF	16.534
IN1<4>	OCF	13.482
IN1<4>	ONF	14.339
IN1<4>	OUT<0>	10.801
IN1<4>	OUT<1>	10.438
IN1<4>	OUT<2>	11.993
IN1<4>	OUT<3>	10.861
IN1<4>	OUT<4>	13.468
IN1<4>	OUT<5>	12.809
IN1<4>	OUT<6>	13.665
IN1<4>	OUT<7>	13.310
IN1<4>	OUT<8>	13.788
IN1<4>	OUT<9>	14.817
IN1<4>	OUT<10>	14.041
IN1<4>	OUT<11>	13.882
IN1<4>	OUT<12>	14.447
IN1<4>	OUT<13>	14.147
IN1<4>	OUT<14>	13.550
IN1<4>	OUT<15>	14.872
IN1<4>	OZF	16.517
IN1<5>	OCF	13.849
IN1<5>	ONF	14.644
IN1<5>	OUT<0>	11.029
IN1<5>	OUT<1>	10.304
IN1<5>	OUT<2>	12.331
IN1<5>	OUT<3>	10.703
IN1<5>	OUT<4>	11.566
IN1<5>	OUT<5>	13.357
IN1<5>	OUT<6>	13.971
IN1<5>	OUT<7>	13.616
IN1<5>	OUT<8>	14.094
IN1<5>	OUT<9>	15.123
IN1<5>	OUT<10>	14.347
IN1<5>	OUT<11>	14.249
IN1<5>	OUT<12>	14.814
IN1<5>	OUT<13>	14.514
IN1<5>	OUT<14>	13.917
IN1<5>	OUT<15>	15.177
IN1<5>	OZF	16.822
IN1<6>	OCF	12.913
IN1<6>	ONF	14.698
IN1<6>	OUT<0>	10.869
IN1<6>	OUT<1>	9.863
IN1<6>	OUT<2>	12.275
IN1<6>	OUT<3>	10.419
IN1<6>	OUT<4>	11.406
IN1<6>	OUT<5>	12.916
IN1<6>	OUT<6>	14.004
IN1<6>	OUT<7>	13.649
IN1<6>	OUT<8>	14.120
IN1<6>	OUT<9>	15.149
IN1<6>	OUT<10>	14.373
IN1<6>	OUT<11>	13.906
IN1<6>	OUT<12>	14.738
IN1<6>	OUT<13>	13.853
IN1<6>	OUT<14>	13.218
IN1<6>	OUT<15>	15.231
IN1<6>	OZF	16.876
IN1<7>	OCF	12.653
IN1<7>	ONF	14.528
IN1<7>	OUT<0>	10.831
IN1<7>	OUT<1>	10.460
IN1<7>	OUT<2>	12.345
IN1<7>	OUT<3>	10.383
IN1<7>	OUT<4>	11.368
IN1<7>	OUT<5>	13.513
IN1<7>	OUT<6>	11.976
IN1<7>	OUT<7>	13.438
IN1<7>	OUT<8>	13.938
IN1<7>	OUT<9>	14.967

IN1<7>	OUT<10>	14.191
IN1<7>	OUT<11>	13.724
IN1<7>	OUT<12>	14.556
IN1<7>	OUT<13>	13.671
IN1<7>	OUT<14>	13.048
IN1<7>	OUT<15>	15.061
IN1<7>	OZF	16.706
IN1<8>	OCF	12.962
IN1<8>	ONF	14.640
IN1<8>	OUT<0>	10.193
IN1<8>	OUT<1>	10.061
IN1<8>	OUT<2>	11.794
IN1<8>	OUT<3>	10.337
IN1<8>	OUT<4>	10.444
IN1<8>	OUT<5>	13.114
IN1<8>	OUT<6>	11.425
IN1<8>	OUT<7>	11.488
IN1<8>	OUT<8>	13.554
IN1<8>	OUT<9>	14.571
IN1<8>	OUT<10>	14.012
IN1<8>	OUT<11>	13.549
IN1<8>	OUT<12>	14.619
IN1<8>	OUT<13>	13.720
IN1<8>	OUT<14>	13.160
IN1<8>	OUT<15>	15.173
IN1<8>	OZF	16.818
IN1<9>	OCF	13.483
IN1<9>	ONF	14.440
IN1<9>	OUT<0>	10.275
IN1<9>	OUT<1>	10.026
IN1<9>	OUT<2>	12.476
IN1<9>	OUT<3>	10.500
IN1<9>	OUT<4>	10.526
IN1<9>	OUT<5>	11.402
IN1<9>	OUT<6>	12.107
IN1<9>	OUT<7>	11.651
IN1<9>	OUT<8>	10.735
IN1<9>	OUT<9>	14.304
IN1<9>	OUT<10>	13.945
IN1<9>	OUT<11>	13.883
IN1<9>	OUT<12>	14.448
IN1<9>	OUT<13>	14.148
IN1<9>	OUT<14>	13.551
IN1<9>	OUT<15>	14.973
IN1<9>	OZF	16.618
IN1<10>	OCF	12.820
IN1<10>	ONF	14.193
IN1<10>	OUT<0>	10.228
IN1<10>	OUT<1>	10.178
IN1<10>	OUT<2>	12.110
IN1<10>	OUT<3>	10.750
IN1<10>	OUT<4>	10.479
IN1<10>	OUT<5>	11.554
IN1<10>	OUT<6>	11.869
IN1<10>	OUT<7>	11.901
IN1<10>	OUT<8>	10.688
IN1<10>	OUT<9>	11.599
IN1<10>	OUT<10>	13.412
IN1<10>	OUT<11>	12.982
IN1<10>	OUT<12>	14.172
IN1<10>	OUT<13>	13.273
IN1<10>	OUT<14>	12.713
IN1<10>	OUT<15>	14.726
IN1<10>	OZF	16.371
IN1<11>	OCF	13.531
IN1<11>	ONF	14.404
IN1<11>	OUT<0>	10.740
IN1<11>	OUT<1>	10.360
IN1<11>	OUT<2>	12.755
IN1<11>	OUT<3>	10.391
IN1<11>	OUT<4>	10.991
IN1<11>	OUT<5>	11.736
IN1<11>	OUT<6>	12.514
IN1<11>	OUT<7>	11.242
IN1<11>	OUT<8>	11.200
IN1<11>	OUT<9>	11.781
IN1<11>	OUT<10>	12.062
IN1<11>	OUT<11>	13.181
IN1<11>	OUT<12>	14.383
IN1<11>	OUT<13>	13.484
IN1<11>	OUT<14>	13.060
IN1<11>	OUT<15>	14.937
IN1<11>	OZF	16.582
IN1<12>	OCF	12.442
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Appendix 5: RTL Diagram of ALU Pipeline Example