Lab 06 FSM

Traffic controller

Target:

Understand the High level design for FSM

Task:

Design a Traffic controller by HDL in Fig. 3.23-3.24 in your text book. Use switches in your board as the inputs T_A and T_B, LEDs as the outputs L_A and L_B. Use 2 approaches below to complete this design respectively. Note that the traffic sensors are scanned every 5 seconds.

1) Use Moore FSM like Fig. 3.25 to design your verilog.
2) Use Mealy FSM to design your verilog. Note that you need to design state transition diagram by yourself

Submission:

verilog code, testbench file, ucf file, simulation snapshot, RTL circuit, board running picture, and *state transition diagram*