lab 05

Section 1: Latch with MUX

Target:

Find out and understand the occasions when ***latch*** produced.

Task:

1) Normally design a 4-input MUX with verilog, simulation, synthesis in ISE, and configuration in Nexys3 board. Use switches as inputs, and LED as output in Nexys3 board.
2) Abnormally design a 4-input MUX with verilog, simulation, synthesis in ISE, and configuration in Nexys 3 board, but with incomplete "`case`" assignment. Use switches as inputs, and LED as output in Nexys3 board.
3) Compare them with the deference of synthesized circuits and running results on board. Explain them.

Mandatory study by yourself:

Learn how to read the synthesized circuits.

Submission:

Design: verilog code, testbench file, ucf file, simulation snapshot, RTL circuit, board running picture.
Explanation in your words.

Optional study by yourself:

Your further study with your own designed experiment related to this topic is strongly welcome, and an extra evaluation may be given. Try to read the synthesis report and timing report in ISE.
Some hints for your reference: 1) drawback of latch; 2) compare "`if`" and "`case`" assignment in circuits and timing, use synthesis report and timing report; 3) others...

Section 2: More for Shifter

Target:

Understand shifter more deeply.
Getting started to design your own verilog, and evaluate in your board.

Task:

You have designed a 4 bits shifter and ran in your board last week, now think about these further:
1) Use your 4 bits shifter to work as a serial-input-parallel-output module, write your code and run in your board (so called *board evaluation*);
2.1) Use your 4 bits shifter to generate a pseudo-random sequence.
2.2) Find out the maximal length in bits of your designed sequence. Select 8 bits to display with LEDs in your board (*board evaluation*).
Hints: LFSR

Submission:

For task 1: verilog code, ucf file, board running picture.

For task 2: verilog code, testbench file, ucf file, simulation snapshot, RTL circuit, board running picture. Your explanation of "maximal length of your sequence" should be also included.