David Quach

dquach05@calpoly.edu davidmquach

Education

California Polytechnic State University, San Luis Obispo **Sep. 2021 – Jun 2025**

Bachelor of Science in Computer Engineering, GPA: 3.73 *San Luis Obispo, CA*

- **Related Coursework:** Computer Architecture, Microcontrollers & Embedded Applications, Electrical & Electronic Circuits, Data Structures, Discrete Structures, Digital Design, Computer Design & Assembly Language, Object-Oriented Programming, Applied Parallel Computing & GPU Programming, Computer Networks

Experience

Marvell Technology **Jun 2024 – Sep 2024**

Systems Software Hardware Intern *Santa Clara, CA*

- Designed **FPGA-based validation models** to emulate and verify evaluation boards, enabling early testing of serial communication protocols and reducing hardware development risks.
- Developed a Python automation framework for power module characterization, orchestrating multiple test instruments to analyze efficiency patterns; **reduced testing duration by 83%.**
- Conducted post-silicon validation testing on 500+ PHY chip evaluation boards using oscilloscopes and logic analyzers, documenting performance metrics and identifying anomalies

Cal Poly Information Technology Services **May 2022 – Present**

Service Desk Assistant *San Luis Obispo, CA*

- Provided expert technical support to 3,000+ students and faculty through on-call assistance and in-person consultations, maintaining a 97% first-contact resolution rate for diverse IT issues.
- Managed and resolved over 500 JIRA Service Management tickets with an average response time of under 30 minutes, exceeding service level agreements by 25%.

Projects

RISC-V Otter Microprocessor | *System Verilog, AMD Vivado, RISC-V* **Jan 2024**

- Delivered a pipelined RISC-V CPU with 37 instructions, designing sub-modules in SystemVerilog HDL and implementing the design onto Artix-7 FPGA.
- Integrated branch prediction and forwarding units, reducing pipeline stalls by 37% and improving cycles per instruction from 1.8 to 1.13.
- Implemented a 4-way set-associative cache memory system that increased program execution by 22%.

Thrash Detection Disconnector | *C++, Python, Arduino, Tkinter, MATLAB* **Feb 2025**

- Engineered a low-power microcontroller-based tension release system for marine buoys, leveraging advanced peak detection algorithms to ensure marine life safety.
- Designed a dynamic Tkinter GUI to visualize peak detection and system operation, enabling seamless calibration and real-time monitoring of tension data.
- Developed efficient peak detection and deep sleep interrupts to reduce power dissipation, extending device lifespan to 1 year.

Digital Microcontroller Synthesizer | *C++, USART, SPI, STM32* **May 2024**

- Engineered a digital synthesizer featuring real-time frequency modulation, envelope control, and dynamic audio effects processing.
- Engineered high-performance digital-to-analog conversion system achieving 16-bit audio fidelity at 44.1kHz through optimized STM32 timer configurations and custom SPI protocol implementation
- Developed an intuitive human-interface system combining UART-based MIDI keyboard integration with analog joystick controls for expressive sound manipulation

Technical Skills

Languages: C#, C++, Python, SQL, Java, RISC-V Assembly, CUDA, MATLAB
Tools: AMD Vivado, LTspice, Git, SVN, Visual Studio Code, Serial Protocols (SPI, I2C, USART)
Interests: FPGA Programming, ASIC Design, Computer Architecture, Embedded Systems, Hardware Development