

# PipeDiT: Accelerating Diffusion Transformers in Video Generation with Task Pipelining and Model Decoupling

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## Abstract

Video generation has been advancing rapidly, and diffusion transformer (DiT) based models have demonstrated remarkable capabilities. However, their practical deployment is often hindered by slow inference speeds and high memory consumption. In this paper, we propose a novel pipelining framework named PipeDiT to accelerate video generation, which is equipped with three main innovations. First, we design a pipelining algorithm (PipeSP) for sequence parallelism (SP) to enable the computation of latent generation and communication among multiple GPUs to be pipelined, thus reducing inference latency. Second, we propose DeDiVAE to decouple the diffusion module and the variational autoencoder (VAE) module into two GPU groups, the executions of which can also be pipelined to reduce memory consumption and inference latency. Third, to better utilize the GPU resources in the VAE group, we propose an attention co-processing (Aco) method to further reduce the overall video generation latency. We integrate our PipeDiT into both OpenSoraPlan and HunyuanVideo, two state-of-the-art open-source video generation frameworks, and conduct extensive experiments on two 8-GPU systems. Experimental results show that, under many common resolution and timestep configurations, our PipeDiT achieves  $1.06\times$  to  $4.02\times$  speedups over OpenSoraPlan and HunyuanVideo.

## 1 Introduction

Video generation models (Li et al. 2024a; Cho et al. 2024; Sun et al. 2024a; Blattmann et al. 2023) have advanced rapidly over the past two years. Such models take textual or visual inputs and synthesize a continuous video as output. Diffusion Transformers (DiT) (Fan et al. 2025; Ma et al. 2024; Yang et al. 2024) have emerged as the primary framework for video generation due to the high quality of the videos they produce. The key idea of DiT is to adopt a progressive denoising process (Ho, Jain, and Abbeel 2020; Sohl-Dickstein et al. 2015; Song and Ermon 2019): starting from pure noise, the model iteratively refines the signal through a reverse diffusion process until a high-quality video is generated as shown in Fig. 1. However, the inherently sequential nature of its reverse diffusion process severely restricts parallelism during inference (Li et al. 2023b; Shih et al. 2023; Chen et al. 2024a).

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Current inference optimizations for DiT target both image and video generation (Liu et al. 2024; Zhang, Luo, and Lu 2024; Luo et al. 2025). For image generation, DistriFusion(Li et al. 2024b) accelerates inference by splitting the input into multiple patches and distributing them across different GPUs. It reuses intermediate feature maps from the previous timestep to provide context for the current step, and hides communication overhead via asynchronous communication in the computation pipeline. PipeFusion (Fang et al. 2024b) also divides images into patches and distributes network layers across multiple GPUs to address memory limitations during generation. For video generation, methods (Chen et al. 2024c; Selvaraju et al. 2024) like Teachache (Liu et al. 2025) analyze the correlation between features across adjacent timesteps and reuse outputs from the previous step to reduce the number of timesteps, thus improving inference efficiency (Ma, Fang, and Wang 2024; Zhao et al. 2024b). However, these approaches may theoretically introduce degradation in generation quality. Consequently, the majority of current video generation models utilize system-level optimizations such as sequence parallelism (SP) (Li et al. 2023a; Sun et al. 2024b; Zhao et al. 2024a) to expedite the generation process while preserving the quality of the generated videos.

Currently, two main SP paradigms have been proposed. The first is DeepSpeed-Ulysses (termed as Ulysses afterward) (Jacobs et al. 2023). By splitting the attention heads and forming complete Query ( $\mathbf{Q}$ ), Key ( $\mathbf{K}$ ) and Value ( $\mathbf{V}$ ) sequences, Ulysses parallelizes attention calculation across multiple GPUs. Its primary advantage lies in its communication pattern, which involves three All-to-All operations before attention computation and one afterward, resulting in relatively low communication overhead. *However, its scalability is limited by the number of attention heads, and existing implementations do not overlap computation and communication, leaving GPU resources underutilized.* The second is Ring-Attention (Li et al. 2021), which performs local attention computations on a partial sequence, and then gathers the  $\mathbf{K}$  and  $\mathbf{V}$  tensors across all devices using Peer-to-Peer (P2P) communication to complete global attention. This method supports much higher degrees of parallelism, *but the increased communication overhead can negate its benefits*, making Ulysses generally preferable when parallelism is not inherently restricted. Some prior works have combined

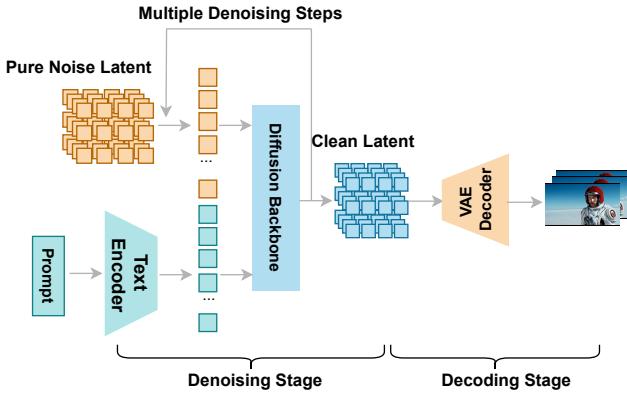


Figure 1: Text-to-video generation starts with encoding the input text and a pure noise latent into a semantic representation, which guides a diffusion model to iteratively refine a latent. The refined latent is then upsampled by a VAE decoder to generate the final video.

both methods into Unified Ulysses-Ring SP (USP) (Fang and Zhao 2024; Fang et al. 2024a), mitigating the limited parallelism of Ulysses at the cost of additional communication overhead.

While current system-level optimizations aim to speed up DiT-based video generation inference reserving the video quality, they still face two key issues: 1) communication between GPUs during the denoising phase often hampers inference efficiency, and 2) using a decoding VAE can quickly result in out-of-memory (OOM) errors, rendering decoding inefficient. In this paper, we introduce PipeDiT, a system-level optimized inference framework, which employs three innovative methods to reduce video generation latency while maintaining video output quality. First, we design a pipeline algorithm, named PipeSP, that overlaps communication and computation within Ulysses to hide some communication overhead and improve GPU utilization. Second, to address the GPU memory explosion in the decoding stage caused by colocation, we propose DeDiVAE to decouple the diffusion module and VAE decoder and onto two GPU groups. DeDiVAE greatly reduces peak GPU memory usage while allowing pipelined execution of decoding and denoising computations. Third, to address the suboptimal utilization of some GPUs caused by DeDiVAE, we further propose an attention co-processing (Aco) module which breaks down DiT into its linear-layer and attention-computation components. This fine-grained breakdown allows attention computation to proceed concurrently across both GPU groups in DeDiVAE, thereby improving GPU utilization. The main contributions of this paper are summarized as follows:

- We analyze the computation and communication patterns of Ulysses and propose an optimized version by pipelining communication and computation tasks in the denoising stage.
- To tackle GPU memory limitations during video generation and inefficiency caused by offloading, we propose a module-level pipeline parallelism that separates diffusion

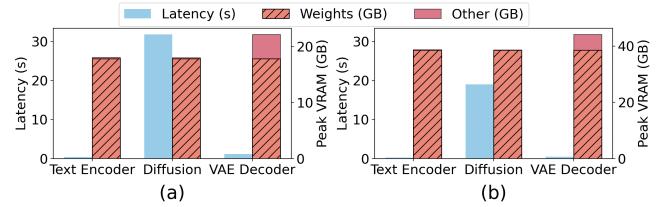


Figure 2: Latency and peak GPU memory usage of each component during inference (using eight GPUs with SP) for a single prompt in (a) OpenSoraPlan (PKU-YuanGroup 2025) model with a resolution of 480×352×65 and 50 timesteps (b) HunyuanVideo (Kong et al. 2024) model with a resolution of 256×128×33 and 50 timesteps.

denoising and VAE decoding across different GPUs, significantly reducing peak memory consumption and improving the generation efficiency.

- To enhance GPU utilization in the decoupled setup, we introduce a fine-grained decoupling strategy that further decouples DiTs into its linear-layer and attention-computation components, allowing attention operations to be distributed across all GPUs.
- Building upon OpenSoraPlan (PKU-YuanGroup 2025) and HunyuanVideo (Tencent-Hunyuan 2025), we evaluate PipeDiT by measuring single-timestep runtime and multi-prompt inference latency under various configurations on two 8-GPU systems. The experimental results demonstrate the effectiveness and scalability of our optimizations.

## 2 Preliminaries & Motivations

**Diffusion-based video generation** comprises two stages as shown in Fig. 1: a Diffusion-based denoising stage that refines a latent representation over multiple timesteps and a variational autoencoder (VAE)-based decoding stage that upsamples the latent into a full-resolution video. The denoising stage is computationally heavy due to attention operations, while the decoding stage is highly memory-intensive due to upsampling to target resolution and frame rate. We conduct a preliminary benchmark using two state-of-the-art video generation frameworks, OpenSoraPlan (PKU-YuanGroup 2025) and HunyuanVideo (Tencent-Hunyuan 2025) as shown in Fig. 2. This indicates that the diffusion stage takes significantly longer than the other two stages, but its memory usage is relatively small. Without offloading enabled, the VAE Decoder peaks at 44GB of memory when decoding the 256×128×33 latent, which is largely because the model parameters occupy a substantial amount of GPU memory. It is evident that during the entire diffusion-based video generation process, the denoising of the latent becomes the time bottleneck, while the decoding of the latent is the memory bottleneck.

In current mainstream video generation models, the diffusion backbone and the VAE decoder are typically collocated, which leads to serialized execution of diffusion computation and VAE upsampling. Without employing offloading or other memory-saving techniques, this design results

in significant additional and inefficient memory consumption. Therefore, colocating the diffusion model and the VAE decoder is unfavorable for parallel video generation and hinders the generation of higher-resolution videos. The experimental results show that under the single-GPU memory constraint of 48 GB, OpenSoraPlan is unable to generate videos with resolutions larger than  $1024 \times 576 \times 97$  without offloading. Due to its larger model weights, HunyuanVideo cannot generate videos beyond  $256 \times 128 \times 33$  in resolution (see the experimental section for details).

**Offloading** is a commonly used strategy to reduce GPU memory consumption during inference (Abul-Fazl, Dina, and Fairuza 2025; Chen et al. 2024b). This strategy saves GPU memory by dynamically transferring model weights between the CPU and GPU. The primary advantage of this strategy is its implementation simplicity and its effectiveness in enabling higher-resolution video generation with limited GPU memory. Accordingly, offloading is adopted by several large-scale video generation systems—such as HunyuanVideo (Tencent-Hunyuan 2025), Wan (Wan et al. 2025), and OpenSoraPlan (PKU-YuanGroup 2025). *However, offloading introduces significant CPU-GPU data transfer overhead, which depends on model size and bandwidth.* The offloading overhead may easily dominate and hurt efficiency, while it cannot run the inference without offloading due to the high memory consumption of video generation.

**Sequence parallelism (SP)** (Li et al. 2023a; Wang et al. 2025; Wu et al. 2024) like Ulysses is a technique used to accelerate the processing of long input sequences on multiple GPUs. Ulysses achieves parallel computation by splitting along the attention head dimension, with different GPUs processing different attention heads. The computation model of Ulysses is illustrated in Fig. 3(a). After each GPU computes its portion of the sub-sequence’s  $\mathbf{Q}$ ,  $\mathbf{K}$ , and  $\mathbf{V}$ , three rounds of All-to-All communication are used to distribute  $\mathbf{Q}$ ,  $\mathbf{K}$ , and  $\mathbf{V}$  along the attention head dimension. The GPUs then concatenate the gathered  $\mathbf{Q}$ ,  $\mathbf{K}$ , and  $\mathbf{V}$  to form a complete sequence, but with only partial attention heads. After all attention heads have been computed, a final round of All-to-All communication is used to disperse the results along the sequence dimension and collect the data along the attention head dimension, resulting in a hidden state with partial sequence length but full attention heads. However, in the original Ulysses kernel, as illustrated in Fig. 3(a), a single All-to-All operation is issued only after all attention heads have been computed; *during the waiting for this communication, GPUs remain idle, resulting in a waste of computational resources.*

### 3 Methodology

#### Pipelining Computation and Communication in SP

To address the issue of serial communication and computation in Ulysses, we propose a pipelined SP (PipeSP) algorithm that partitions the computation of attention along the head dimension and issues an All-to-All immediately after each head is processed, as illustrated in Fig. 3(b), thus overlapping communication with computation to improve the

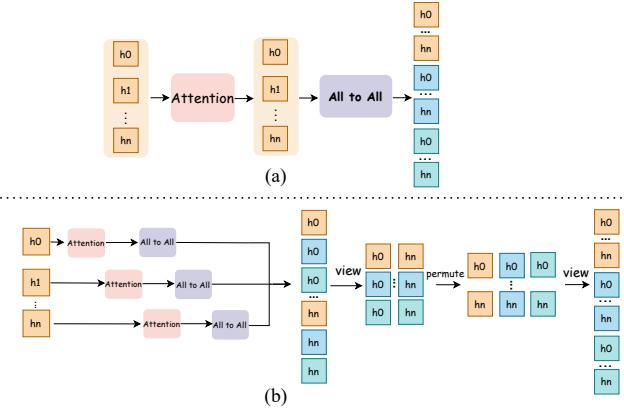


Figure 3: (a) The execution process of Ulysses, where computation and communication are executed sequentially. (b) Our optimized SP (PipeSP) by pipelining communication and computation. The subsequent post-processing resolves the misalignment issue introduced by the pipelining.

Algorithm 1: PipeSP: Overlapping Computation and Communication in SP

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Require:  $Q \in \mathbb{R}^{B \times h \times S \times D}$ ,  $K$ ,  $V$ ,  $\text{attention\_mask}$ 
1: Initialize  $\text{chunks}$ ,  $\text{results}$ ,  $\text{event\_lst}$ 
2: for  $j \leftarrow 0$  to  $h - 1$  do
3:    $\text{result} \leftarrow \text{attention}(Q[:, j, :, :], K[:, j, :, :], V[:, j, :, :], \text{attention\_mask}[:, j, :, :])$ 
4:   Append  $\text{result}$  to  $\text{results}$ 
5:   Record event  $\text{event\_lst}[j]$ 
6:   Wait on CUDA stream for  $\text{event\_lst}[j]$ 
7:    $\text{hidden\_states} \leftarrow \text{All\_to\_All}(\text{results}[j])$ 
8:   Append  $\text{hidden\_states}$  to  $\text{chunks}$ 
9: end for
10:  $\text{hidden\_states} \leftarrow \text{concat}(\text{chunks}, \text{dim} = 1)$ 
11:  $\text{hidden\_states} \leftarrow \text{view}(-1, h, n, D)$ 
12:  $\text{hidden\_states} \leftarrow \text{permute}(0, 2, 1, 3)$ 
13:  $\text{hidden\_states} \leftarrow \text{view}(-1, h \times n, D)$ 

```

computation efficiency. Specifically, in the attention layer that has  $n$  heads, each head is processed independently. Thus, the  $n$  heads can be partitioned into  $n$  independent attention operations, each of which has only one head. After each head has been computed at its attention, its result can be communicated with other GPUs via an All-to-All operation. Thus, the operations of attention (computation) and All-to-All (communication) form a pipeline, which keeps GPU resources be fully utilized during the inference process. After the results of all heads have been gathered, a layout transformation is performed to align the result be identical with that without pipelining.

The PipeSP algorithm is shown in Algorithm 1. In lines 1–9, the  $\mathbf{Q}$ ,  $\mathbf{K}$ , and  $\mathbf{V}$  tensors are partitioned along the attention head dimension, and for each head, attention is computed over the full sequence. An event is recorded to mark the completion of this computation, and once all GPUs have completed the corresponding event, an All-to-All is trig-

gered. In this step, each GPU receives the portion of the attention output corresponding to its local sequence slice for a single head. Lines 10–13 perform post-processing to reorder the collected results. This reordering is necessary because the optimized method collects attention outputs one head at a time, whereas the original method gathered them in a total different way, resulting in a misalignment shown in Fig. 3(b). To resolve this, the tensor must be reshaped and permuted using the sequence `view` → `permute` → `view`. Specifically, `view(-1, h, n, D)` reshapes the head dimension into a 2D layout of  $[h, n]$ , `permute(0, 2, 1, 3)` swaps the GPU and head axes, and the final `view(-1, nh, D)` restores the expected layout. Mathematically, this process ensures the final tensor matches the original layout expected by the attention module, while enabling efficient communication–computation overlap. A formal proof of the correctness of the `view`–`permute`–`view` transformation is provided in the Supplementary Material.

### Memory-Efficient Diffusion–VAE Decoupling

To address the issues of low computational efficiency and poor GPU memory utilization caused by colocating the diffusion model and the VAE decoder, we propose **Diffusion–VAE Module Decoupling** (DeDiVAE) by breaking down the Diffusion module and the VAE module to two disjoint GPU groups: *Denoising Group* and *Decoding Group*. Specifically, for a given  $N$ -GPU system for video generation with DiT, DeDiVAE splits the  $N$  GPUs to  $N_{\text{denoise}}$  GPUs as the *Denoising Group* and the other  $N_{\text{decode}} = N - N_{\text{denoise}}$  GPUs as the *Decoding Group*. Accordingly, full video generation model is split into the Diffusion backbone stored in the *Denoising Group*, and the VAE decoder stored in the *Decoding Group*. The decoupling effectively avoids the OOM problem for large models and high-resolution video generation. The latent outputs of the *Denoising Group* should be sent the *Denoising Group* to generate the video.

At first glance, DeDiVAE might also lead to idle periods due to the data dependency between the two groups, potentially affecting inference efficiency. This issue can be addressed by implementing a pipeline execution with multiple prompts. Given that a video generation service typically handles multiple ongoing queries, multiple prompts (or queries) can be pipelined within our decoupled structure as demonstrated in Fig. 4. The decoding execution with VAE of the first prompt can be overlapped with the denoising execution with diffusion of the second prompt, which allows both GPU groups to keep busy. To maximize the utilization of GPU resources, we provide an effective analysis on how many GPUs should be assigned to the two groups.

**Optimal GPU partitioning.** Given  $N$  GPUs for inference, there are  $N_{\text{denoise}}$  GPUs in the *Denoising Group* and  $N_{\text{decode}}$  GPUs in the *Decoding Group*. Let  $T_{\text{denoise}}$  denote the time of denoising one prompt on a single GPU and  $T_{\text{decode}}$  denote the time of decoding one latent on a single GPU. During inference we accelerate the denoising with SP across  $N_{\text{denoise}}$  GPUs, while the decoder uses data parallelism across  $N_{\text{decode}}$  GPUs. Since the total workloads of inference are unchanged, to enable an maximal overlap is to make the execution time of the groups be identical. Thus,

the first-order balance condition is

$$\left( \frac{T_{\text{denoise}}}{N_{\text{denoise}}} + T_{\text{comm}} \right) N_{\text{decode}} \approx T_{\text{decode}},$$

$$\implies N_{\text{decode}} \approx \left\lceil \frac{T_{\text{decode}}}{T_{\text{decode}} + T_{\text{denoise}}} N \right\rceil,$$

which yields the optimal  $N_{\text{decode}}$  that maximizes GPU utilization: both stages finish a micro-batch in approximately the same time, preventing either group of GPUs from idling while the other is still computing. Since intra-node GPU communication is very fast, and PipeSP overlaps communication with computation to hide most of the communication overhead, omitting  $T_{\text{comm}}$  does not affect the resulting resource allocation.

In practice, though we assign the GPUs in a balance way, the execution time of the diffusion stage may still dominate the overall execution time. To improve the efficiency, we design a new co-processing approach in DeDiVAE as introduced in the following section.

### Attention Co-processing

When denoising process is much slower than a VAE decoding, the Decoding GPUs idle during most of the generation window, and the pipeline cannot achieve a full overlap. Therefore, we propose **Attention Co-processing** (Aco) to utilize the idle time of the *Decoding Group*. We further split the DiT block into two disjoint kernels:

- *Linear projections*:  $\mathbf{Q} = \mathbf{XW}_Q$ ,  $\mathbf{K} = \mathbf{XW}_K$ ,  $\mathbf{V} = \mathbf{XW}_V$ ,
- *Attention kernel*:  $\text{Attn}(\mathbf{Q}, \mathbf{K}, \mathbf{V})$ ,

and assign them to the two GPU groups. The Denoising GPUs keep the DiT weights and compute the linear projections; immediately afterwards they transmit the resulting  $\mathbf{Q}$ ,  $\mathbf{K}$ ,  $\mathbf{V}$  tensors via point-to-point links to the Decoding GPUs, when Decoding GPUs are not decoding latents. Because the attention kernel depends only on  $\mathbf{Q}$ ,  $\mathbf{K}$ ,  $\mathbf{V}$ , and the computations of different attention heads are independent in multi-head attention, the Decoding GPUs can execute it autonomously.

As shown in Fig. 4, in the prompt 1 stage, since there is no latent requiring for decoding, the idle Decoding GPUs can be leveraged to assist with attention computation. Specifically, the Denoising GPUs first perform intra-group All-to-All communication, followed by P2P communication to send the  $\mathbf{Q}$ ,  $\mathbf{K}$ ,  $\mathbf{V}$  tensors to the Decoding GPUs. Both groups then execute attention computations in parallel. Afterward, the Denoising GPUs aggregate the results via intra-group All-to-All and inter-group P2P communication, obtaining latents with partial sequence length but complete attention heads. Afterwards, the Denoising GPUs push the latent outputs into a shared queue that is accessible to all processes. The Decoding GPUs then retrieve them from the queue for subsequent decoding.

In the prompt 2 stage, as the decoding queue becomes non-empty, the Decoding GPUs are occupied with decoding latents from the queue. Consequently, the Denoising GPUs

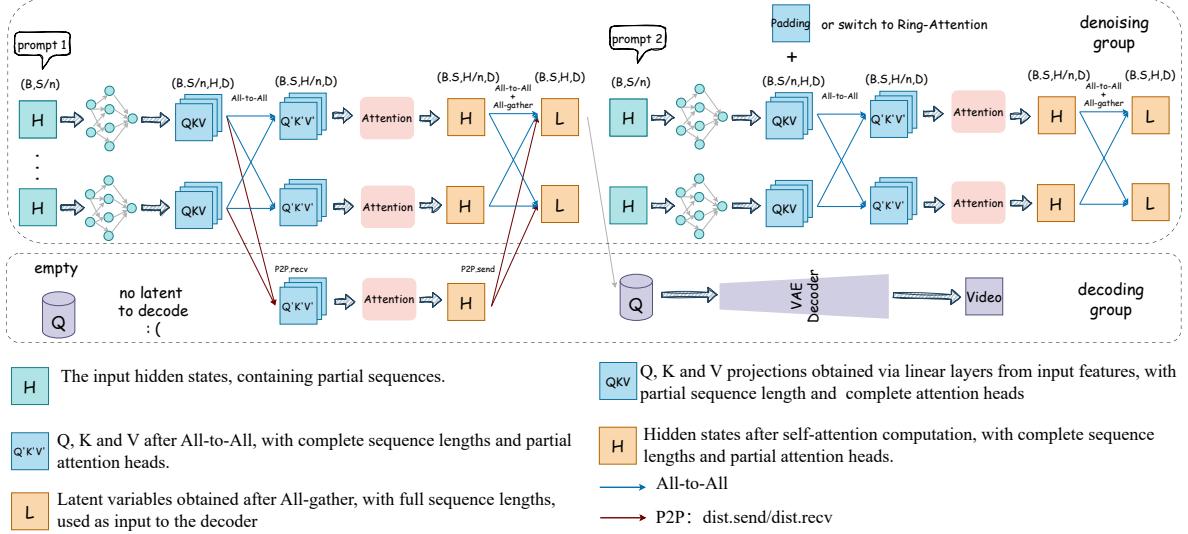


Figure 4: In the prompt 1 stage, the Denoising GPUs transmit the computed  $\mathbf{Q}$ ,  $\mathbf{K}$ , and  $\mathbf{V}$  tensors to the Decoding GPUs, enabling parallel attention computation across both groups. In the prompt 2 stage, the Denoising GPUs perform attention computation independently, while the Decoding GPUs execute decoding in parallel.

must perform attention computation independently. During this stage, denoising and decoding proceed in parallel. It is worth noting that if the number of attention heads is not divisible by the number of Denoising GPUs, there are two possible strategies to handle this. For models that only adopt Ulysses, such as OpenSoraPlan (PKU-YuanGroup 2025), head dimension padding must be introduced to ensure balanced workload distribution. In contrast, models like HunyuanVideo (Tencent-Hunyuan 2025) and Wan (Wan et al. 2025) adopt Unified Sequence Parallelism (USP) (Fang and Zhao 2024), which allows flexible configuration of both the Ulysses degree and the Ring-Attention degree. When the number of heads is not divisible, we can switch Denoising GPUs from Ulysses to Ring-Attention, effectively changing the parallelism from head-wise splitting to sequence-wise splitting, thereby avoiding the overhead of padding and improving GPU utilization.

**Performance Analysis.** Let  $t_L$  and  $t_A$  denote the wall-clock time of one linear-projection and one attention kernel on Denoising GPUs, respectively, and let  $N_{\text{denoise}}$  and  $N_{\text{decode}}$  be the two GPU group sizes ( $N_{\text{denoise}} + N_{\text{decode}} = N$ ). In the baseline decoupling only the denoising group participates:

$$T_{\text{baseline}} = t_L + t_A. \quad (1)$$

With Aco, the linear part still costs  $t_L$ , but the attention time scales inversely with the total number of GPUs that now share the work:

$$T_{\text{coop}} = t_L + t_A \frac{N_{\text{denoise}}}{N_{\text{denoise}} + N_{\text{decode}}}. \quad (2)$$

Hence the theoretical speed-up is

$$S = \frac{T_{\text{baseline}}}{T_{\text{coop}}} = \frac{t_L + t_A}{t_L + t_A \frac{N_{\text{denoise}}}{N}}. \quad (3)$$

Note that the above analysis assumes the number of attention heads  $H$  is divisible by the number of Denoising GPUs  $N_{\text{denoise}}$ . If not divisible, and switching between Ulysses and Ring-Attention as in HunyuanVideo is not supported, then padding is required to balance the workload, leading to wasted GPU resources. For example, if  $H = 24$  and 7 GPUs are used for denoising, padding increases the head count to 28 so that each GPU handles 4 heads. However, only 6 GPUs are effectively needed, and one GPU performs redundant computations. Our Attention Co-processing solves this issue by avoiding padding and ensuring all GPUs perform meaningful work, even when  $H$  is not divisible by  $N_{\text{denoise}}$ .

## 4 Evaluation

### Experimental Setups

**Baselines.** We implement our PipeDiT on two state-of-the-art open-source video generation systems OpenSoraPlan at v1.3.0<sup>1</sup> and HunyuanVideo<sup>2</sup>. As the generation algorithm of PipeDiT is identical with OpenSoraPlan and HunyuanVideo, the generated videos are identical, so we mainly compare the time and memory efficiency. Note that OpenSoraPlan uses Ulysses, while HunyuanVideo integrates USP in xDiT (Fang et al. 2024a). The model sizes for OpenSoraPlan and HunyuanVideo are 2B and 13B parameters, respectively.

**Performance Metrics.** The performance metrics are video generation efficiency and GPU memory consumption. The efficiency metrics consist of two aspects. The first is the latency per timestep, which measures the optimization effect of PipeSP. The second metric is the overall latency for generating multiple videos from consecutive prompts, which measures the overall optimization effect of PipeDiT.

<sup>1</sup><https://github.com/PKU-YuanGroup/Open-Sora-Plan>

<sup>2</sup><https://github.com/Tencent-Hunyuan/HunyuanVideo>

Resolution	OpenSoraPlan (A6000)								OpenSoraPlan (L40)									
	10			30			50		10			30			50			
	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑
480 × 352 × 97	227	107	2.12×	420	304	1.38×	622	502	1.24×	252	154	1.64×	492	<b>407</b>	1.21×	738	<b>657</b>	1.12×
640 × 352 × 97	257	135	1.90×	522	389	1.34×	786	643	1.22×	303	<b>206</b>	1.47×	650	<b>545</b>	1.19×	983	<b>883</b>	1.11×
800 × 592 × 97	520	397	1.31×	1257	<b>1097</b>	1.15×	1994	<b>1766</b>	1.13×	646	<b>517</b>	1.25×	1609	<b>1441</b>	1.12×	2570	<b>2373</b>	1.08×
1024 × 576 × 97	555	430	1.29×	1360	<b>1144</b>	1.19×	2162	<b>1832</b>	1.18×	731	<b>591</b>	1.24×	1836	<b>1639</b>	1.12×	2940	<b>2689</b>	1.09×
HunyuanVideo (A6000)																	HunyuanVideo (L40)	
Resolution	10			30			50		10			30			50			
	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑	base	opt	spd↑
	480 × 352 × 97	540	<b>165</b>	3.27×	767	<b>445</b>	1.72×	965	<b>726</b>	1.33×	676	<b>229</b>	2.95×	992	<b>649</b>	1.53×	1350	<b>1068</b>
640 × 352 × 97	593	<b>191</b>	3.10×	865	<b>531</b>	1.63×	1142	<b>907</b>	1.26×	760	<b>295</b>	2.58×	1231	<b>843</b>	1.46×	1702	<b>1392</b>	1.22%
800 × 592 × 97	1082	<b>506</b>	2.14×	1880	<b>1492</b>	1.26×	2686	<b>2470</b>	1.09×	1694	<b>923</b>	1.84×	3291	<b>2702</b>	1.22×	4898	<b>4482</b>	1.09%
1024 × 576 × 97	1399	<b>729</b>	1.92×	2545	<b>2090</b>	1.22×	3726	<b>3453</b>	1.08×	2237	<b>1333</b>	1.68×	4576	<b>3894</b>	1.18×	6952	<b>6453</b>	1.08%

Table 1: Latency and speedup for generating 10 videos with the baseline system and our optimized PipeDiT. Bold numbers indicate the results obtained with PipeDiT w/ Aco.

OpenSoraPlan (A6000)								
480x352x65 480x352x129 640x352x65 640x352x129 800x592x65 800x592x129 1024x576x65 1024x576x129								
Baseline (s)	1.67	1.30	1.21	2.10	2.21	4.98	2.57	6.86
PipeSP(s)	1.73	1.20	1.69	1.83	2.05	4.74	2.41	6.54
Speedup	0.97×	1.08×	0.72×	1.15×	1.08×	1.05×	1.07×	1.05×
OpenSoraPlan (L40)								
480x352x65 480x352x129 640x352x65 640x352x129 800x592x65 800x592x129 1024x576x65 1024x576x129								
Baseline (s)	1.36	1.66	1.05	2.44	2.87	7.34	3.61	10.30
PipeSP (s)	1.42	1.57	1.01	2.34	2.74	7.05	3.44	9.95
Speedup	0.96×	1.06×	1.04×	1.04×	1.05×	1.04×	1.05×	1.04%

Table 2: Improvement in per-timestep latency with our PipeSP.

**Testbeds.** All experiments are conducted on two 8-GPU systems: 1) eight NVIDIA RTX A6000 48GB GPUs and 2) eight NVIDIA L40 48GB GPUs. More environment information can be found in Supplementary Material.

### End-to-End Performance

We configure different video resolutions, commonly used diffusion timesteps (10, 30, and 50), and 10 prompts<sup>3</sup> to compare generation latency as shown in Table 1, where “base” indicates the baseline using offloading, “opt” indicates our PipeDiT, and “spd” indicates the speedup of PipeDiT over the baseline. Since Aco does not always achieve improvement especially on low workload video generation, bold numbers indicate the results generated using PipeDiT w/ Aco.

From the results in Table 1, our PipeDiT always achieves faster inference speed by 1.08×-3.27× than baseline both OpenSoraPlan and HunyuanVideo. Particularly, PipeDiT yields the most notable speedups under lower resolutions,

<sup>3</sup>Due to the page limit, we put the results with more comprehensive configurations in Supplementary Material.

fewer frames, and shorter timesteps, reaching up to 3.27× (up to 4.02× as shown in Supplementary Material). As the resolution, frame count, and timesteps increase, the benefit diminishes since the computation time dominates and the relative impact of data transfer decreases, making offloading less of a bottleneck. Despite this, our PipeDiT on OpenSoraPlan with the A6000 platform still achieves 1.18× improvement over the baseline in the highest setting.

For different models, HunyuanVideo has more parameters, so its offloading takes longer time, making PipeDiT more effective to HunyuanVideo under lower resolutions and timesteps. In contrast, under higher resolutions and timesteps, the optimizations of PipeDiT in HunyuanVideo bring greater gains to OpenSoraPlan due to its shorter computation time. For different hardware, because the A6000 GPUs are connected with NVLink which delivers higher communication speed than L40. Thus, PipeDiT yields shorter per-timestep computation times compared to L40, and thus it has higher improvement on A6000 than L40.

OpenSoraPlan (A6000)																	
A	B	C	D	480x352x65	480x352x129	640x352x65	640x352x129	800x592x65	800x592x129	1024x576x65	1024x576x129						
T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑
✓ ✗ ✗ ✗	314	1x	529	1x	368	1x	665	1x	777	1x	1875	1x	851	1x	1995	1x	
✗ ✓ ✗ ✗	217	1.45x	452	1.17x	234	1.57x	500	1.33x	649	1.20x	1872	1.00x	702	1.21x	2138	0.93x	
✗ ✓ ✓ ✗	200	1.57x	390	1.36x	250	1.47x	509	1.31x	649	1.20x	1847	1.02x	717	1.19x	1936	1.03x	
✗ ✓ ✓ ✓	261	1.20x	414	1.28x	296	1.24x	507	1.31x	645	1.20x	1652	1.14x	683	1.25x	1690	1.18x	

HunyuanVideo (A6000)																	
A	B	C	D	480x352x65	480x352x129	640x352x65	640x352x129	800x592x65	800x592x129	1024x576x65	1024x576x129						
T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑	T(s)↓	Spd↑
✗ ✗ ✗ ✗	636	1x	911	1x	695	1x	1104	1x	1294	1x	2681	1x	1676	1x	3733	1x	
✗ ✓ ✗ ✗	340	1.87x	681	1.34x	403	1.72x	824	1.34x	984	1.32x	2501	1.07x	1374	1.22x	3680	1.01x	
✗ ✓ ✓ ✗	345	1.84x	701	1.30x	404	1.72x	824	1.34x	983	1.32x	2499	1.07x	1374	1.22x	3675	1.02x	
✗ ✓ ✓ ✓	327	1.94x	595	1.53x	396	1.76x	741	1.49x	942	1.37x	2259	1.19x	1242	1.35x	3090	1.21x	

Table 3: Efficiency improvement of different optimization methods.

Methods	OpenSoraPlan															
	480x352x129		640x352x129		800x592x129		1024x576x129		Mem	↓%	Mem	↓%	Mem	↓%	Mem	↓%
	Mem	↓%	Mem	↓%	Mem	↓%	Mem	↓%								
Baseline	26.5	—	29.4	—	39.8	—	OOM	—								

HunyuanVideo																	
A	B	C	D	480x352x65	480x352x129	640x352x65	640x352x129	800x592x65	800x592x129	1024x576x65	1024x576x129						
Timesteps	5	-82	-38	-16	-58	-19	30	39	190	391	98	279	496				
Baseline	OOM	—	OOM	—	OOM	—	OOM	—	49	-73	-36	-21	-64	-18	16	21	131
Offloading	29.37	38.8%	29.38	38.8%	32.97	31.3%	33.01	31.2%	-61	-35	-25	-46	-26	2	8	78	196
DeDiVAE	41.44	13.6%	41.43	13.7%	41.45	13.6%	42.12	12.2%	-35	-33	-32	-31	-36	-31	-29	-24	1

Table 4: Peak GPU memory usage (GB) and reduction ratio.

### Effectiveness of PipeSP

To evaluate the effectiveness of PipeSP, we use eight representative resolution and frame configurations and measure the per-timestep latency, as shown in Table 2. Notably, PipeSP achieves a 15% performance improvement under the 640x352x129 configuration. The results also indicate that the optimization achieves the best performance under moderate resolutions, as it strikes a balance between overly short and excessively long computation times. When the resolution is low, the computation time is short, and the communication overhead introduced by overlap can offset its benefits. Conversely, at high resolutions, the proportion of communication time becomes less significant relative to the overall computation time, thereby reducing the optimization gains.

### Memory Efficiency of DeDiVAE

For the memory optimization comparison, we compare our DeDiVAE with the original implementation w/o offloading as the baseline. The second row in Table 4 presents the original implementation with offloading, while the third row shows the results of our DeDiVAE approach. As shown in the table, both our method and the offloading strategy significantly reduce memory consumption during inference. The baseline implementation fails with an OOM error under the highest resolution setting, indicating that without any memory optimization strategies, the model is unable to generate videos beyond 1024 × 576 × 129 in OpenSoraPlan and 480 × 352 × 129 in HunyuanVideo.

It should be noted that in HunyuanVideo, our DeDiVAE demonstrates greater peak memory consumption than the offloading method. This occurs because we colocated the text encoder with the VAE decoder. Given the substantial size of the text encoder in HunyuanVideo, colocating it with the DiT module, as done in OpenSoraPlan, is not feasible. This demonstrates that our method allows adaptable management of module positioning based on the attributes of the model.

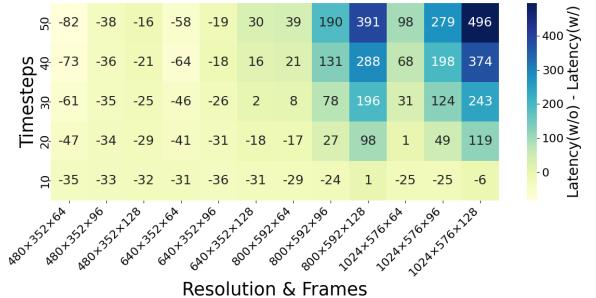


Figure 5: The heatmap of the latency difference between the two methods: (1) PipeDiT w/o Aco and (2) PipeDiT w/ Aco.

### Ablation Study

To evaluate the performance improvements of various optimization methods, we fixed the number of timesteps to 30 and selected eight different resolutions and frame settings for ablation studies. The results are shown in Table 3, where “A” indicates the baseline offloading method, “B” indicates DeDiVAE, “C” indicates PipeSP, and “D” refers to Aco.

The results show that PipeSP demonstrates significant performance improvements on OpenSoraPlan. This is primarily because OpenSoraPlan incurs longer All-to-All communication times, and due to its non-modular design, we were able to partially overlap the computation of  $\mathbf{Q}$ ,  $\mathbf{K}$ , and  $\mathbf{V}$  with the three All-to-All communications that occur before the attention computation.

For DeDiVAE, it achieves substantial efficiency gains under lower resolutions. However, as the resolution increases, the drawback of having fewer GPUs allocated to denoising

becomes more apparent. Introducing Aco helps to address this limitation. Even under the highest resolution setting, the combined approach still delivers considerable performance benefits. The performance difference of PipeDiT w/ Aco and w/o Aco is shown in Fig. 5, which indicates that Aco improves performance on high workload tasks.

## 5 Conclusion

In this study, we proposed a system-level optimization system named PipeDiT for accelerating the video generation with diffusion transformer (DiT) based models. There are three key innovations in PipeDiT: 1) a pipelining algorithm named PipeSP for sequence parallelism (SP) for enable overlapping between communication and computation tasks, 2) a module decoupling method named DeDiVAE by breaking down the diffusion module and VAE module to two GPU groups to reduce the memory consumption, and 3) an attention co-processing approach named Aco, which leverages the idle decoding GPU group to assist with denoising module execution. Our PipeDiT is implemented atop two state-of-the-art video generations frameworks OpenSora-Pland and HunyuanVideo. Extensive experiments were conducted on two GPU systems and the results indicate that our PipeDiT not only significantly reduces memory consumption but also greatly enhances the generation efficiency.

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## Supplementary Material

### Complete End-to-End Performance Results

In the main body, we present a subset of the End-to-End Performance Results, while Table 6 provides the complete results. We evaluate our model under multiple resolutions ranging from  $480 \times 352$  to  $1024 \times 576$ , covering common video qualities such as 480p and 576p. The timestep values are arranged in descending order, where fewer timesteps lead to lower latency but also lower generation quality.

Results demonstrate that PipeDiT achieves notable acceleration across both models and platforms, proving its effectiveness for lightweight frameworks like OpenSoraPlan and large-scale systems like HunyuanVideo. PipeDiT is thus applicable to video generation models of various sizes.

Under low to medium resolutions and shorter timesteps, PipeDiT achieves up to  $4.02\times$  speedup. Even at the highest resolution and timestep, it still delivers  $1.06\times$  to  $1.17\times$  improvement. As the current trend in DiT-based inference optimization moves toward using fewer timesteps and more aggressively compressed VAE decoders to reduce denoising latency, the speedup brought by PipeDiT is expected to increase as the denoising time becomes smaller.

Additionally, some recent video generation models, such as Wan2.2, have adopted Mixture-of-Experts (MoE) architectures that significantly increase model size. In such cases, traditional offloading approaches become less viable, while PipeDiT offers a scalable and efficient alternative well-suited to these future scenarios.

### Complete Results of Ablation Study

In the main text, we only present the ablation results on the A6000 platform. Table 7 shows the full ablation study results across all platforms, where “A” indicates the baseline offloading method, “B” indicates DeDiVAE, “C” indicates PipeSP, and “D” refers to Aco. We observe that PipeDiT achieves more significant performance improvements on the A6000 platform compared to the L40 platform. This is primarily because, under the same model and input configurations, the end-to-end latency on the A6000 is lower than that on the L40 for both the baseline and PipeDiT. As a result, the proportion of offloading time—eliminated by PipeDiT—accounts for a larger share of the total runtime on the A6000 system, leading to a higher relative speedup.

Furthermore, the A6000’s support for high-bandwidth NVLink interconnects allows more efficient inter-GPU communication compared to the PCIe-based L40. This architectural advantage further amplifies the effectiveness of PipeDiT’s PipeSP. These results demonstrate that PipeDiT can adapt well across heterogeneous hardware configurations while achieving especially notable improvements on platforms equipped with high interconnect bandwidth and lower baseline latencies.

### Consistency Proof of PipeSP

As PipeSP generates misordered results which are then transformed to the original layout, we prove that the results of PipeSP is identical with the original SP. **Resulting mis-order** After all heads have been processed, every GPU owns

the hidden state of its sub-sequence, but the global head order is now interleaved: for GPU index  $i \in \{0, \dots, n-1\}$  and local head  $j \in \{0, \dots, h-1\}$

$$k_{\text{orig}}(i, j) = ih + j, \quad k_{\text{mod}}(i, j) = jn + i. \quad (4)$$

The tensor  $T^{\text{mod}} \in \mathbb{R}^{B \times H \times D}$  therefore has head  $k_{\text{mod}}(i, j)$  where the original order expects  $k_{\text{orig}}(i, j)$ ; a reordering is mandatory.

Let  $B$  be the mini-batch,  $n$  the number of GPUs,  $h$  heads per GPU ( $H = nh$ ), and  $D$  the head dimension. Since the sequence dimension  $S$  is not involved in the operations considered in this section, it is omitted for brevity. Define the reshape map  $\varphi_{h,n} : \mathbb{R}^{B \times H \times D} \rightarrow \mathbb{R}^{B \times h \times n \times D}$ ,

$$(\varphi_{h,n} T)[b, j, i, d] = T[b, jn + i, d], \quad (5)$$

and its inverse  $\varphi_{h,n}^{-1}$  that merges  $(i, j)$  back into a linear head index. Let  $\pi : \mathbb{R}^{B \times h \times n \times D} \rightarrow \mathbb{R}^{B \times n \times h \times D}$ ,

$$(\pi X)[b, i, j, d] = X[b, j, i, d]. \quad (6)$$

The code  $\text{sequence view}(-1, h, n, D) \rightarrow \text{permute}(0, 2, 1, 3) \rightarrow \text{view}(-1, nh, D)$  implements the composite map

$$\Psi = \varphi_{h,n}^{-1} \circ \pi \circ \varphi_{h,n} : \mathbb{R}^{B \times H \times D} \rightarrow \mathbb{R}^{B \times H \times D}. \quad (7)$$

**Alignment proof** For any  $b, d, i, j$  one has

$$\begin{aligned} (\Psi T^{\text{mod}})[b, k_{\text{orig}}(i, j), d] &= (\varphi_{h,n}^{-1} \pi \varphi_{h,n} T^{\text{mod}})[b, ih + j, d] \\ &= (\pi \varphi_{h,n} T^{\text{mod}})[b, i, j, d] \\ &= (\varphi_{h,n} T^{\text{mod}})[b, j, i, d] \\ &= T^{\text{mod}}[b, jn + i, d] \\ &= T^{\text{mod}}[b, k_{\text{mod}}(i, j), d]. \end{aligned}$$

Hence  $\Psi T^{\text{mod}} = T^{\text{orig}}$ : after the two view plus one permute, the interleaved tensor is mapped exactly onto the head-contiguous layout expected by the original Ulysses implementation.

### Experimental Environment

Our experiments are conducted entirely on A6000 and L40 GPUs. The hardware configurations of the test platforms are shown in Table 5.

Component	Specification
CPU	Intel® Xeon® Platinum 8358, @2.60 GHz
GPU	8× Nvidia RTX A6000, 48GB GDDR6
NVLink	112.5GB/s (4×)
PCIe	4.0 (x16)
CPU	Intel® Xeon® Platinum 8358, @2.60 GHz
GPU	8× Nvidia L40, 48GB GDDR6
NVLink	-
PCIe	4.0 (x16)

Table 5: Testbed Hardware Specifications.

Resolution	OpenSoraPlan (A6000)															OpenSoraPlan (L40)														
	10			20			30			40			50			10			20			30			40			50		
	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$	base	opt	spd $\dagger$
480x352x65	177	73	2.42x	240	138	1.74x	314	200	1.57x	379	264	1.44x	437	329	1.33x	204	105	1.94x	274	202	1.35x	355	298	1.19x	436	393	1.11x	512	481	1.06x
480x352x70	227	107	2.12x	321	205	1.57x	420	304	1.38x	521	403	1.29x	622	502	1.24x	252	154	1.64x	368	278	1.32x	492	407	1.21x	613	531	1.15x	738	657	1.12x
480x352x129	162	135	1.94x	400	263	1.52x	320	389	1.28x	606	518	1.28x	594	624	1.23x	310	200	1.55x	344	372	1.30x	625	548	1.22x	824	714	1.15x	936	882	1.11x
640x352x65	203	92	2.21x	285	170	1.69x	364	250	1.47x	491	332	1.48x	536	411	1.31x	224	129	1.81x	333	244	1.36x	625	548	1.27	454	416	1.16x	638	562	1.14x
640x352x97	257	135	1.90x	388	262	1.49x	522	389	1.34x	653	521	1.25x	786	643	1.22x	303	206	1.47x	473	373	1.27x	650	545	1.19x	713	653	1.15x	983	883	1.11x
640x352x129	310	176	1.76x	492	342	1.44x	665	507	1.31x	835	660	1.27x	1007	811	1.24x	368	253	1.45x	590	471	1.25x	808	685	1.18x	1030	902	1.14x	1240	1118	1.11x
800x592x65	347	228	1.52x	571	436	1.31x	777	645	1.20x	999	841	1.19x	1037	116x	410	299	555	669	555	1.21x	935	815	1.15x	1201	1073	1.12x	1471	1331	1.11x	
800x592x97	520	397	1.31x	899	758	1.19x	1257	1097	1.15x	1637	1433	1.14x	1994	1766	1.13x	646	517	1.25x	1124	980	1.15x	1609	1441	1.12x	2013	1903	1.06x	2373	208	1.08x
800x592x129	751	621	1.21x	1316	1137	1.16x	1875	1651	1.14x	2447	2174	1.13x	3010	2689	1.12x	959	791	1.21x	1709	1515	1.13x	2464	2239	1.10x	3223	2964	1.09x	3977	3688	1.08x
1024x576x65	376	251	1.50x	614	479	1.28x	851	684	1.24x	1094	888	1.23x	1323	1089	1.21x	476	354	1.34x	801	661	1.21x	1114	970	1.15x	1440	1280	1.13x	1760	1588	1.11x
1024x576x97	555	430	1.29x	959	799	1.20x	1360	1144	1.19x	1762	1491	1.18x	2162	1832	1.18x	731	591	1.24x	1279	1115	1.15x	1836	1639	1.12x	2387	2164	1.10x	2940	2689	1.09x
1024x576x129	797	652	1.22x	1402	1176	1.19x	1995	1698	1.17x	2600	2206	1.18x	3194	2726	1.17x	1094	916	1.19x	1970	1751	1.13x	2848	2582	1.10x	3722	3416	1.09x	4599	4251	1.08x

Table 6: Latency and speedup for generating 10 videos with the baseline system and our optimized PipeDiT. Bold numbers indicate the results obtained with PipeDiT w/ Aco.

Resolution	OpenSoraPlan(A6000)															OpenSoraPlan(L40)																				
	A			B			C			D			480x352x65			480x352x129			640x352x65			640x352x129			800x592x65			800x592x129			1024x576x65			1024x576x129		
	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$	T(s) $\downarrow$	Spd $\uparrow$														
480x352x65	482	120	4.02x	563	219	2.57x	636	327	1.94x	702	431	1.63x	766	520	1.47x	517	157	3.29x	632	298	2.12x	764	437	1.75x	850	579	1.47x	983	718	1.37x						
480x352x70	540	165	3.27x	641	306	2.09x	767	445	1.85x	850	585	1.45x	965	726	1.33x	676	295	3.93x	838	439	1.91x	992	649	1.53x	1163	859	1.35x	1350	1068	1.26x						
480x352x129	630	203	3.06x	767	395	1.84x	911	595	1.53x	1011	791	1.35x	1205	985	1.22x	787	312	2.52x	1038	602	1.72x	1288	892	1.44x	1573	1182	1.32x	1944	1472	1.23x						
640x352x65	518	147	3.65x	596	269	2.22x	695	396	1.76x	791	515	1.54x	882	638	1.38x	601	201	1.41x	749	376	1.99x	749	555	1.43x	1041	738	1.32x	1206	911	1.21x						
640x352x97	593	191	3.11x	733	360	2.04x	865	531	1.63x	1008	501	1.41x	1123	907	1.26x	760	295	2.58x	1021	571	1.71x	1231	843	1.46x	1460	1119	1.30x	1702	1392	1.21x						
640x352x129	710	262	2.71x	899	503	1.79x	1104	511	1.49x	1272	987	1.29x	1456	1253	1.22x	1792	1561	1.15x	1160	527	2.0x	1601	1028	1.56x	2018	1818	1.32x	2487	2027	1.23x						
800x592x65	833	321	2.60x	1075	633	1.70x	1294	942	1.42x	1531	1253	1.22x	1792	1561	1.15x	1160	527	2.0x	1601	1028	1.56x	2018	1818	1.32x	2487	2027	1.16x	2942	2528	1.16x						
800x592x97	1082	506	2.4x	1499	1000	1.56x	1880	1992	1.26x	2381	1985	1.15x	2686	2470	1.09x	1694	923	1.84x	2848	1812	1.37x	3291	2702	1.22x	3515	3592	1.16x	4898	4482	1.09x						
800x592x129	1467	772	1.90x	2062	1514	1.36x	2681	2259	1.19x	3302	3006	1.10x	3920	3756	1.04x	2311	1374	1.68x	3511	2686	1.31x	4717	4001	1.18x	5926	5317	1.11x	7136	6632	1.08x						
1024x576x65	997	430	2.32x	1333	835	1.60x	1676	1242	1.35x	1989	1645	1.21x	2324	2051	1.13x	1486	760	1.96x	2146	1490	1.44x	2817	2223	1.27x	3473	2952	1.18x	4123	3682	1.12x						
1024x576x97	1399	729	1.92x	1987	1425	1.39x	2545	2090	1.22x	3150	2771	1.14x	3726	3453	1.08x	2237	1333	1.68x	3395	2612	1.30x	4576	3894	1.18x	5762	5173	1.11x	6952	6453	1.08x						
1024x576x129	1918	1097	1.75x	2836	2078	1.36x	3733	3090	1.21x	4638	4206	1.10x	5545	5240	1.06x	3187	2024	1.57x	5017	3984	1.26x	6846	5942	1.15x	8658	7899	1.10x	10472	9856	1.06x						

Table 7: Efficiency improvement of different optimization methods.

### Consistency Proof of Generated Results

Since our optimization focuses solely on resource allocation and computational workload balancing, the algorithmic logic remains fully consistent with the original method. As a result, the generated outputs are identical to those of the original algorithm. Fig. 6 presents the outputs from both the original method and our optimized approach under the same prompt, experimental configuration, and sampled frame index. The results clearly demonstrate that the two generations are perfectly identical.



Open-Sora-Plan w/o PipeDiT

Open-Sora-Plan w/ PipeDiT

Figure 6: The generation results show that the outputs produced by PipeDiT are consistent with those of the original algorithm.