

# A Survey of Neuromorphic Computing and Neural Networks in Hardware

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**Abstract**—Neuromorphic computing has come to refer to a variety of brain-inspired computers, devices, and models that contrast the pervasive von Neumann computer architecture. This biologically inspired approach has created highly connected synthetic neurons and synapses that can be used to model neuroscience theories as well as solve challenging machine learning problems. The promise of the technology is to create a brain-like ability to learn and adapt, but the technical challenges are significant, starting with an accurate neuroscience model of how the brain works, to finding materials and engineering breakthroughs to build devices to support these models, to creating a programming framework so the systems can learn, to creating applications with brain-like capabilities. In this work, we provide a comprehensive survey of the research and motivations for neuromorphic computing over its history. We begin with a 35-year review of the motivations and drivers of neuromorphic computing, then look at the major research areas of the field, which we define as neuro-inspired models, algorithms and learning approaches, hardware and devices, supporting systems, and finally applications. We conclude with a broad discussion on the major research topics that need to be addressed in the coming years to see the promise of neuromorphic computing fulfilled. The goals of this work are to provide an exhaustive review of the research conducted in neuromorphic computing since the inception of the term, and to motivate further work by illuminating gaps in the field where new research is needed.

**Index Terms**—neuromorphic computing, neural networks, deep learning, spiking neural networks, materials science, digital, analog, mixed analog/digital

## I. INTRODUCTION

THIS paper provides a comprehensive survey of the neuromorphic computing field, reviewing over 3,000 papers from a 35-year time span looking primarily at the motivations, neuron/synapse models, algorithms and learning, applications, advancements in hardware, and briefly touching on materials and supporting systems. Our goal is to provide a broad and historic perspective of the field to help further ongoing

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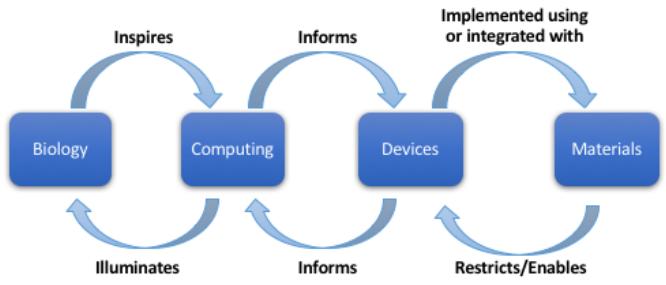


Fig. 1. Areas of research involved in neuromorphic computing, and how they are related.

research, as well as provide a starting point for those new to the field.

Devising a machine that can process information faster than humans has been a driving force in computing for decades, and the von Neumann architecture has become the clear standard for such a machine. However, the inevitable comparisons of this architecture to the human brain highlight significant differences in the organizational structure, power requirements, and processing capabilities between the two. This leads to a natural question regarding the feasibility of creating alternative architectures based on neurological models, that compare favorably to a biological brain.

Neuromorphic computing has emerged in recent years as a complementary architecture to von Neumann systems. The term neuromorphic computing was coined in 1990 by Carver Mead [1]. At the time, Mead referred to very large scale integration (VLSI) with analog components that mimicked biological neural systems as “neuromorphic” systems. More recently, the term has come to encompass implementations that are based on biologically-inspired or artificial neural networks in or using non-von Neumann architectures.

These neuromorphic architectures are notable for being highly connected and parallel, requiring low-power, and collocating memory and processing. While interesting in their own right, neuromorphic architectures have received increased attention due to the approaching end of Moore’s law, the increasing power demands associated with Dennard scaling, and the low bandwidth between CPU and memory known as the von Neumann bottleneck [2]. Neuromorphic computers have the potential to perform complex calculations faster, more power-efficiently, and on a smaller footprint than traditional

von Neumann architectures. These characteristics provide compelling reasons for developing hardware that employs neuromorphic architectures.

Machine learning provides the second important reason for strong interest in neuromorphic computing. The approach shows promise in improving the overall learning performance for certain tasks. This moves away from hardware benefits to understanding potential application benefits of neuromorphic computing, with the promise of developing algorithms that are capable of on-line, real-time learning similar to what is done in biological brains. Neuromorphic architectures appear to be the most appropriate platform for implementing machine learning algorithms in the future.

The neuromorphic computing community is quite broad, including researchers from a variety of fields, such as materials science, neuroscience, electrical engineering, computer engineering, and computer science (Figure 1). Materials scientists study, fabricate, and characterize new materials to use in neuromorphic devices, with a focus on materials that exhibit properties similar to biological neural systems. Neuroscientists provide information about new results from their studies that may be useful in a computational sense, and utilize neuromorphic systems to simulate and study biological neural systems. Electrical and computer engineers work at the device level with analog, digital, mixed analog/digital, and non-traditional circuitry to build new types of devices, while also determining new systems and communication schemes. Computer scientists and computer engineers work to develop new network models inspired by both biology and machine learning, including new algorithms that can allow these models to be trained and/or learn on their own. They also develop the supporting software necessary to enable the use of neuromorphic computing systems in the real world.

The goals of this paper are to give a thirty-year survey of the published works in neuromorphic computing and hardware implementations of neural networks and to discuss open issues for the future of neuromorphic computing. The remainder of the paper is organized as follows: In Section II, we present a historical view of the motivations for developing neuromorphic computing and how they have changed over time. We then break down the discussion of past works in neuromorphic computing into models (Section III), algorithms and learning (Section IV), hardware implementations (Section V), and supporting components, including communication schemes and software systems (Section VI-B). Section VII gives an overview of the types of applications to which neuromorphic computing systems have been applied in the literature. Finally, we conclude with a forward-looking perspective for neuromorphic computing and enumerate some of the major research challenges that are left to tackle.

## II. MOTIVATION

The idea of using custom hardware to implement neurally-inspired systems is as old as computer science and computer engineering itself, with both von Neumann [3] and Turing [4] discussing brain-inspired machines in the 1950's. Computer scientists have long wanted to replicate biological neural

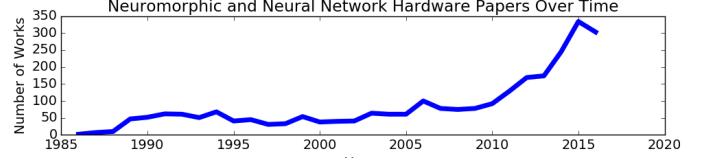


Fig. 2. Neuromorphic and neural network hardware works over time.

systems in computers. This pursuit has led to key discoveries in the fields of artificial neural networks (ANNs), artificial intelligence, and machine learning. The focus of this work, however, is not directly on ANNs or neuroscience itself, but on the development of non-von Neumann hardware for simulating ANNs or biological neural systems. We discuss several reasons why neuromorphic systems have been developed over the years based on motivations described in the literature. Figure 2 shows the number of works over time for neuromorphic computing and indicates that there has been a distinct rise in interest in the field over the last decade. Figure 3 shows ten of the primary motivations for neuromorphic in the literature and how those motivations have changed over time. These ten motivations were chosen because they were the most frequently noted motivations in the literature, each specified by at least fifteen separate works.

Much of the early work in neuromorphic computing was spurred by the development of hardware that could perform parallel operations, inspired by observed parallelism in biological brains, but on a single chip [5]–[9]. Although there were parallel architectures available, neuromorphic systems emphasized many simple processing components (usually in the form of neurons), with relatively dense interconnections between them (usually in the form of synapses), differentiating them from other parallel computing platforms of that time. In works from this early era of neuromorphic computing, the inherent parallelism of neuromorphic systems was the most popular reason for custom hardware implementations.

Another popular reason for early neuromorphic and neural network hardware implementations was speed of computation [10]–[13]. In particular, developers of early systems emphasized that it was possible to achieve much faster neural network computation with custom chips than what was possible with traditional von Neumann architectures, partially by exploiting their natural parallelism as mentioned above, but also by building custom hardware to complete neural-style computations. This early focus on speed foreshadowed a future of utilizing neuromorphic systems as accelerators for machine learning or neural network style tasks.

Real-time performance was also a key motivator of early neuromorphic systems. Enabled by natural parallelism and speed of computation, these devices tended to be able to complete neural network computations faster than implementations on von Neumann architectures for applications such as real-time control [14], real-time digital image reconstruction [15], and autonomous robot control [16]. In these cases, the need for faster computation was not driven by studying the neural network architectures themselves or for training, but

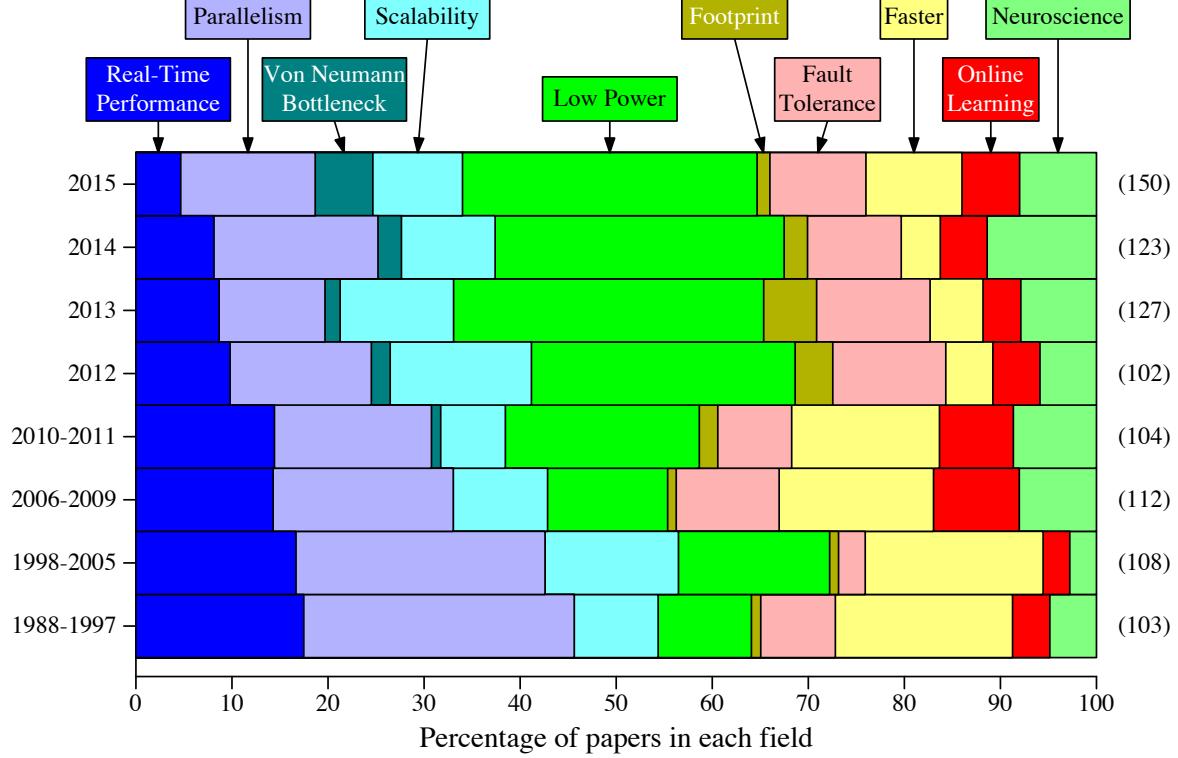


Fig. 3. Ten different motivations for developing neuromorphic systems, and over time, the percentage of the papers in the literature that have indicated that motivation as one of the primary reasons they have pursued the development of neuromorphic systems.

was more driven by application performance. This is why we have differentiated it from speed and parallelism as a motivation for the development of neuromorphic systems.

Early developers also started to recognize that neural networks may be a natural model for hardware implementation because of their inherent fault tolerance, both in the massively parallel representation and in potential adaptation or self-healing capabilities that can be present in artificial neural network representations in software [5], [17]. These were and continue to be relevant characteristics for fabricating new hardware implementations, where device and process variation may lead to imperfect fabricated devices, and where utilized devices may experience hardware errors.

The most popular motivation in present-day literature and discussions of neuromorphic systems in the referenced articles is the emphasis on their potential for extremely low power operation. Our major source of inspiration, the human brain, requires about 20 watts of power and performs extremely complex computations and tasks on that small power budget. The desire to create neuromorphic systems that consume similarly low power has been a driving force for neuromorphic computing from its conception [18], [19], but it became a prominent motivation about a decade into the field's history.

Similarly, creating devices capable of neural network-style computations with a small footprint (in terms of device size) also became a major motivation in this decade of neuromorphic research. Both of these motivations correspond with the rise of the use of embedded systems and microprocessors,

which may require a small footprint and, depending on the application, very low power consumption.

In recent years, the primary motivation for the development of neuromorphic systems is low-power consumption. It is, by far, the most popular motivation for neuromorphic computers, as can be seen in Figure 3. Inherent parallelism, real-time-performance, speed in both operation and training, and small device footprint also continue to be major motivations for the development of neuromorphic implementations. A few other motivations became popular in this period, including a rise of approaches that utilize neural network-style architectures (i.e., architectures made up of neuron and synapse-like components) because of their fault tolerance characteristics or reliability in the face of hardware errors. This has become an increasingly popular motivation in recent years in light of the use of novel materials for implementing neuromorphic systems (see Section V-C).

Another major motivation for building neuromorphic systems in recent years has been to study neuroscience. Custom neuromorphic systems have been developed for several neuroscience-driven projects, including those created as part of the European Union's Human Brain Project [20], because simulating relatively realistic neural behavior on a traditional supercomputer is not feasible, in scale, speed, or power consumption [21]. As such, custom neuromorphic implementations are required in order to perform meaningful neuroscience simulations with reasonable effort. In this same vein, scalability has also become an increasingly popular

motivation for building neuromorphic systems. Most major neuromorphic projects discuss how to cascade their devices together to reach very large numbers of neurons and synapses.

A common motivation not given explicitly in Figure 3 is the end of Moore’s Law, though most of the other listed motivations are related to the consideration of neuromorphic systems as a potential complementary architecture in the beyond Moore’s law computing landscape. Though most researchers do not expect that neuromorphic systems will replace von Neumann architectures, “building a better computer” is one of their motivations for developing neuromorphic devices; though this is a fairly broad motivation, it encompasses issues associated with traditional computers, including the looming end of Moore’s law and the end of Dennard scaling. Another common motivation for neuromorphic computing development is solving the von Neumann bottleneck [22], which arises in von Neumann architectures due to the separation of memory and processing and the gap in performance between processing and memory technologies in current systems. In neuromorphic systems, memory and processing are collocated, mitigating issues that arise with the von Neumann bottleneck.

On-line learning, defined as the ability to adapt to changes in a task as they occur, has been a key motivation for neuromorphic systems in recent years. Though on-line learning mechanisms are still not well understood, there is still potential for the on-line learning mechanisms that are present in many neuromorphic systems to perform learning tasks in an unsupervised, low-power manner. With the tremendous rise of data collection in recent years, systems that are capable of processing and analyzing this data in an unsupervised, on-line way will be integral in future computing platforms. Moreover, as we continue to gain an understanding of biological brains, it is likely that we will be able to build better on-line learning mechanisms and that neuromorphic computing systems will be natural platforms on which to implement those systems.

### III. MODELS

One of the key questions associated with neuromorphic computing is which neural network model to use. The neural network model defines what components make up the network, how those components operate, and how those components interact. For example, common components of a neural network model are neurons and synapses, taking inspiration from biological neural networks. When defining the neural network model, one must also define models for each of the components (e.g., neuron models and synapse models); the component model governs how that component operates.

How is the correct model chosen? In some cases, it may be that the chosen model is motivated by a particular application area. For example, if the goal of the neuromorphic device is to utilize the device to simulate biological brains for a neuroscience study on a faster scale than is possible with traditional von Neumann architectures, then a biologically realistic and/or plausible model is necessary. If the application is an image recognition task that requires high accuracy, then a neuromorphic system that implements convolutional neural networks may be best. The model itself may also be shaped

by the characteristics and/or restrictions of a particular device or material. For example, memristor-based systems (discussed further in Section V-B1) have characteristics that allow for spike-timing dependent plasticity-like mechanisms (a type of learning mechanism discussed further in Section IV) that are most appropriate for spiking neural network models. In many other cases, the choice of the model or the level of complexity for the model is not entirely clear.

A wide variety of model types have been implemented in neuromorphic or neural network hardware systems. The models range from predominantly biologically-inspired to predominantly computationally driven. The latter models are inspired more by artificial neural network models than by biological brains. This section discusses different neuron models, synapse models, and network models that have been utilized in neuromorphic systems, and points to key portions of the literature for each type of model.

#### A. Neuron Models

A biological neuron is usually composed of a cell body, an axon, and dendrites. The axon usually (though not always) transmits information away from the neuron, and is where neurons transmit output. Dendrites usually (though not always) transmit information to the cell body and are typically where neurons receive input. Neurons can receive information through chemical or electrical transmissions from other neurons. The juncture between the end of an axon of one neuron and the dendrite of another neuron that allows information or signals to be transmitted between the two neurons is called a synapse. The typical behavior of a neuron is to accumulate charge through a change in voltage potential across the neuron’s cell membrane, caused by receiving signals from other neurons through synapses. The voltage potential in a neuron may reach a particular threshold, which will cause the neuron to “fire” or, in the biological terminology, generate an action potential that will travel along a neuron’s axon to affect the charge on other neurons through synapses. Most neuron models implemented in neuromorphic systems have some concept of accumulation of charge and firing to affect other neurons, but the mechanisms by which these processes take place can vary significantly from model to model. Similarly, models that are not biologically plausible (i.e. artificial models that are *inspired* by neuroscience rather than *mimicking* neuroscience) typically do not implement axons or dendrites, although there are a few exceptions (as noted below).

Figure 4 gives an overview of the types of neuron models that have been implemented in hardware. The neuron models are given in five broad categories:

- Biologically-plausible: Explicitly model the types of behavior that are seen in biological neural systems.
- Biologically-inspired: Attempt to replicate behavior of biological neural systems but not necessarily in a biologically-plausible way.
- Neuron+Other: Neuron models including other biologically-inspired components that are not usually included in other neuromorphic neuron models, such as axons, dendrites, or glial cells.

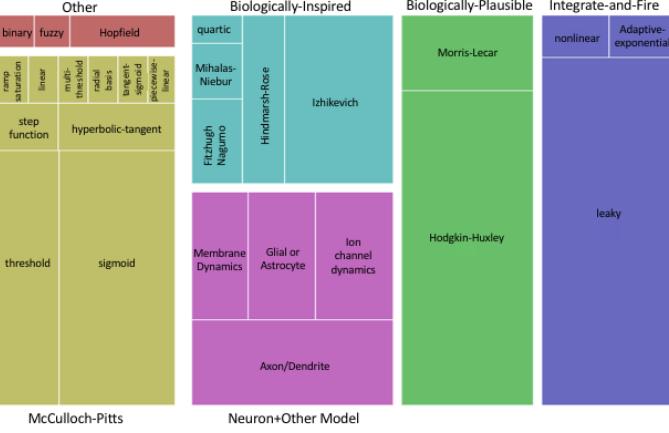


Fig. 4. A hierarchy of neuron models that have hardware implementations. The size of the boxes corresponds to the number of implementations for that model, and the color of the boxes corresponds to the “family” of neuron models, which are labeled either above or below the group of same-colored boxes.

- Integrate-and-fire: A simpler category of biologically-inspired spiking neuron models.
- McCulloch-Pitts: Neuron models that are derivatives of the original McCulloch-Pitts neuron [23] used in most artificial neural network literature. For this model, the output of neuron  $j$  is governed by the following equation:

$$y_j = f \left( \sum_{i=0}^N w_{i,j} x_i \right), \quad (1)$$

where  $y_j$  is the output value,  $f$  is an activation function,  $N$  is the number of inputs into neuron  $j$ ,  $w_{i,j}$  is the weight of the synapse from neuron  $i$  to neuron  $j$  and  $x_i$  is the output value of neuron  $i$ .

A variety of biologically-plausible and biologically-inspired neuron models have been implemented in hardware. Components that may be included in these models may include: cell membrane dynamics, which govern factors such as charge leakage across the neuron’s cell membrane; ion channel dynamics, which govern how ions flow into and out of a neuron, changing the charge level of the neuron; axonal models, which may include delay components; and dendritic models, which govern how many pre- and post-synaptic neurons affect the current neuron. A good overview of these types of spiking neuron models is given by Izhikevich [24].

1) *Biologically-Plausible*: The most popular biologically-plausible neuron model is the Hodgkin-Huxley model [25]. The Hodgkin-Huxley model was first introduced in 1952 and is a relatively complex neuron model, with four-dimensional nonlinear differential equations describing the behavior of the neuron in terms of the transfer of ions into and out of the neuron. Because of their biological plausibility, Hodgkin-Huxley models have been very popular in neuromorphic implementations that are trying to accurately model biological neural systems [26]–[54]. A simpler, but still biologically-plausible model is the Morris Lecar model, which reduces the model to a two-dimensional nonlinear equation [55]. It

is a commonly implemented model in neuroscience and in neuromorphic systems [27], [56]–[61].

2) *Biologically-Inspired*: There are a variety of neuron models that are simplified versions of the Hodgkin-Huxley model that have been implemented in hardware, including Fitzhugh-Nagumo [62]–[64] and Hindmarsh-Rose [65]–[69] models. These models tend to be both simpler computationally and simpler in terms of number of parameters, but they become more biologically-inspired than biologically-plausible because they attempt to model behavior rather than trying to emulate physical activity in biological systems. From the perspective of neuromorphic computing hardware, simpler computation can lead to simpler implementations that are more efficient and can be realized with a smaller footprint. From the algorithms and learning method perspective, a smaller number of parameters can be easier to set and/or train than models with a large number of parameters.

The Izhikevich spiking neuron model was developed to produce similar bursting and spiking behaviors as can be elicited from the Hodgkin-Huxley model, but do so with much simpler computation [70]. The Izhikevich model has been very popular in the neuromorphic literature because of its simultaneous simplicity and ability to reproduce biologically accurate behavior [27], [71]–[82]. The Mihalas-Niebur neuron is another popular neuron model that tries to replicate bursting and spiking behaviors, but it does so with a set of linear differential equations [83]; it also has neuromorphic implementations [84], [85]. The quartic model has two non-linear differential equations that describe its behavior, and also has an implementation for neuromorphic systems [86].

3) *Neuron + Other Biologically-Inspired Mechanism*: Other biologically-inspired models are also prevalent that do not fall into the above categories. They typically contain a much higher level of biological detail than most models from the machine learning and artificial intelligence literature, such as the inclusion of membrane dynamics [87]–[91], modeling ion-channel dynamics [92]–[98], the incorporation of axons and/or dendrite models [99]–[110], and glial cell or astrocyte interactions [111]–[116]. Occasionally, new models are developed specifically with the hardware in mind. For example, a neuron model with equations inspired by the Fitzhugh-Nagumo, Morris Lecar, Hodgkin-Huxley, or other models have been developed, but the equations were updated or the models abstracted in order to allow for ease of implementation in low-power VLSI [117], [118], on FPGA [119], [120], or using static CMOS [121]–[123]. Similarly, other researchers have updated the Hodgkin-Huxley model to account for new hardware developments, such as the MOSFET transistor [124]–[130] or the single-electron transistor [131].

4) *Integrate-and-Fire Neurons*: A simpler set of spiking neuron models belong to the integrate-and-fire family, which is a set of models that vary in complexity from relatively simple (the basic integrate-and-fire) to those approaching complexity levels near that of the Izhikevich model and other more complex biologically-inspired models [132]. In general, integrate-and-fire models are less biologically realistic, but produce enough complexity in behavior to be useful in spiking neural systems. The simplest integrate-and-fire model maintains the

current charge level of the neuron. There is also a leaky integrate-and-fire implementation that expands the simplest implementation by including a leak term to the model, which causes the potential on a neuron to decay over time. It is one of the most popular models used in neuromorphic systems [58], [133]–[164]. The next level of complexity is the general nonlinear integrate-and-fire method, including the quadratic integrate-and-fire model that is used in some neuromorphic systems [165], [166]. Another level of complexity is added with the adaptive exponential integrate-and-fire model, which is similar in complexity to the models discussed above (such as the Izhikevich model). These have also been used in neuromorphic systems [167], [168].

In addition to the previous analog-style spiking neuron models, there are also implementations of digital spiking neuron models. The dynamics in a digital spiking neuron model are usually governed by a cellular automaton, as opposed to a set of nonlinear or linear differential equations. A hybrid analog/digital implementation has been created for neuromorphic implementations [169], as well as implementations of resonate-and-fire [170] and rotate-and-fire [171], [172] digital spiking neurons. A generalized asynchronous digital spiking model has been created in order to allow for exhibition of nonlinear response characteristics [173], [174]. Digital spiking neurons have also been utilized in pulse-coupled networks [175]–[179]. Finally, a neuron for a random neural network has been implemented in hardware [180].

In the following sections, the term spiking neural network will be used to describe full network models. These spiking networks may utilize any of the above neuron models in their implementation; we do not specify which neuron model is being utilized. Moreover, in some hardware implementations, such as SpiNNaker (see Section V-A1), the neuron model is programmable, so different neuron models may be realized in a single neuromorphic implementation.

5) *McCulloch-Pitts Neurons*: Moving to more traditional artificial neural network implementations in hardware, there is a large variety of implementations of the traditional McCulloch-Pitts neuron model [23]. The perceptron is one implementation of the McCulloch-Pitts model, which uses a simple thresholding function as the activation function; because of its simplicity, it is commonly used in hardware implementations [181]–[191]. There has also been significant focus to create implementations of various activation functions for McCulloch-Pitts-style neurons in hardware. Different activation functions have had varying levels of success in neural network literature, and some activation functions can be computationally intensive. This complexity in computation can lead to complexity in hardware, resulting in a variety of different activation functions and implementations that are attempting to trade-off complexity and overall accuracy and computational usefulness of the model. The most popular implementations are the basic sigmoid function [192]–[212] and the hyperbolic tangent function [213]–[216], but other hardware-based activation functions that have been implemented include the ramp-saturation function [194], linear [200], piecewise linear [217], step function [194], [218], multi-threshold [219], radial basis function [208], the tan-

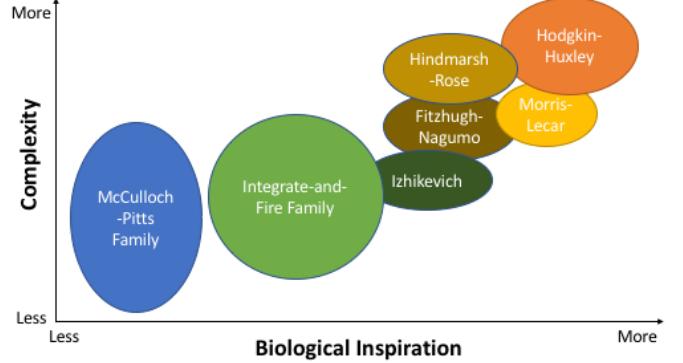


Fig. 5. A qualitative comparison of neuron models in terms of biological inspiration and complexity of the neuron model.

gent sigmoid function [208], and periodic activation functions [220]. Because the derivative of the activation function is utilized in the back-propagation training algorithm [221], some circuits implement both the function itself and its derivative, for both sigmoid [222]–[227] and hyperbolic tangent [224]. A few implementations have focused on creating neurons with programmable activation functions [228] or on creating building blocks to construct neurons [229].

Neuron models for other traditional artificial neural network models have also been implemented in hardware. These neuron models include binary neural network neurons [230], fuzzy neural network neurons [231], and Hopfield neural network neurons [232]–[234]. On the whole, there have been a wide variety of neuron models implemented in hardware, and one of the decisions a user might make is a tradeoff between complexity and biological inspiration. Figure 5 gives a qualitative comparison of different neuron models in terms of those two factors.

## B. Synapse Models

Just as some neuromorphic work has focused particularly on neuron models, which occasionally also encapsulate the synapse implementation, there has also been a focus on developing synapse implementations independent of neuron models for neuromorphic systems. Once again, we may separate the synapse models into two categories: biologically-inspired synapse implementations, which include synapses for spike-based systems, and synapse implementations for traditional artificial neural networks, such as feed-forward neural networks. It is worth noting that synapses are typically going to be the most abundant element in neuromorphic systems, or the element that is going to require the most real estate on a particular chip. For many hardware implementations and especially for the development and use of novel materials for neuromorphic, the focus is typically on optimizing the synapse implementation. As such, synapse models tend to be relatively simple, unless they are attempting to explicitly model biological behavior. One popular inclusion for more complex synapse models is a plasticity mechanism, which causes the neuron's strength or weight value to change over

time. Plasticity mechanisms have been found to be related to learning in biological brains.

For more biologically-inspired neuromorphic networks, synapse implementations that explicitly model the chemical interactions of synapses, such as the ion pumps or neurotransmitter interactions, have been utilized in some neuromorphic systems [67], [235]–[245]. Ion channels have also been implemented in neuromorphic implementations in the form of conductance-based synapse models [246]–[251]. For these implementations, the detail goes above and beyond what one might see with the modeling of ion channels in neuron models such as Hodgkin-Huxley.

Implementations for spiking neuromorphic systems focus on a variety of characteristics of synapses. Neuromorphic synapses that exhibit plasticity and learning mechanisms inspired by both short-term and long-term potentiation and depression in biological synapses have been common in biologically-inspired neuromorphic implementations [252]–[262]. Potentiation and depression rules are specific forms of spike-timing dependent plasticity (STDP) [263] rules. STDP rules and their associated circuitry are extremely common in neuromorphic implementations for synapses [252], [256], [259], [264]–[300]. More information on STDP as a learning algorithm and its implementations in neuromorphic systems is provided in Section IV. Synaptic responses can also be relatively complex in neuromorphic systems. Some neuromorphic synapse implementations focus on synaptic dynamics, such as the shape of the outgoing spike from the synapse or the post-synaptic potential [301]–[305]. Synapses in spiking neuromorphic systems have also been used as homeostasis mechanisms to stabilize the network’s activity, which can be an issue in spiking neural network systems [306], [307].

A variety of neuromorphic synaptic implementations for non-spiking neural networks have also been implemented. These networks include feed-forward multi-layer networks [308]–[314], winner-take-all [315], and convolutional neural networks [316]. A focus on different learning rules for synapses in artificial neural network-based neuromorphic systems is also common, as it is for STDP and potentiation and depression rules in spike-based neuromorphic systems. Common learning rules in artificial neural network-based systems include Hebbian learning [310], [312], [317], [318] and least mean-square [11], [319]. Gaussian synapses have also been implemented in order to help with back-propagation learning rules [320]–[322].

### C. Network Models

Network models describe how different neurons and synapses are connected and how they interact. As may be intuited from the previous sections, there are a wide variety of neural network models that have been developed for neuromorphic systems. Once again, they range from trying to replicate biological behavior closely to much more computationally-driven, non-spiking neural networks. There are a variety of factors to consider when selecting a network model. One of the factors is clearly biological inspiration and complexity of neuron and synapse models, as discussed in previous

sections. Another factor to consider is the topology of the network. Figure 6 shows some examples of network topologies that might be used in various network models, including biologically-inspired networks and spiking networks. Depending on the hardware chosen, the connectivity might be relatively restricted, which would restrict the topologies that can be realistically implemented. A third factor is the feasibility and applicability of existing training or learning algorithms for the chosen network model, which will be discussed in more detail in Section IV. Finally, general applicability of that network model to a set of applications may also play a role in choosing the appropriate network model.

There are a large variety of general spiking neural network implementations in hardware [21], [86], [169], [323]–[570]. These implementations utilize a variety of neuron models such as the various integrate-and-fire neurons listed above or the more biologically-plausible or biologically-inspired models. Spiking neural network implementations also typically include some form of STDP in the synapse implementation. Spiking models have been popular in neuromorphic implementations in part because of their event-drive nature and improved energy efficiency relative to other systems. As such, implementations of other neural network models have been created using spiking neuromorphic systems, including spiking feed-forward networks [571]–[575], spiking recurrent networks [576]–[581], spiking deep neural networks [582]–[592], spiking deep belief networks [593], spiking Hebbian systems [594]–[602], spiking Hopfield networks or associative memories [603]–[605], spiking winner-take-all networks [606]–[611], spiking probabilistic networks [612], [613], and spiking random neural networks [614]. In these implementations a spiking neural network architecture in neuromorphic systems has been utilized for another neural network model type. Typically, the training for these methods is done on the traditional neural network type (such as the feed-forward network), and then the resulting network solution has been adapted to fit the spiking neuromorphic implementation. In these cases, the full properties of the spiking neural network may not be utilized.

A popular biologically-inspired network model that is often implemented using spiking neural networks is central pattern generators (CPGs). CPGs generate oscillatory motion, such as walking gaits or swimming motions in biological systems. A common use of CPGs have been in robotic motion. There are several neuromorphic systems that were built specifically to operate as CPGs [615]–[619], but CPGs are also often an application built on top of existing spiking neuromorphic systems, as is discussed in Section VII.

The most popular implementation by far is feed-forward neural networks, including multi-layer perceptrons [8], [9], [16]–[19], [192], [194], [200], [202], [206], [207], [530], [620]–[1023]. Extreme learning machines are a special case of feed-forward neural networks, where a number of the weights in the network are randomly set and never updated based on a learning or training algorithm; there have been several neuromorphic implementations of extreme learning machines [1024]–[1029]. Another special case of feed-forward neural networks are multi-layer perceptrons with delay, and those have also been implemented in neuromorphic systems [1030]–

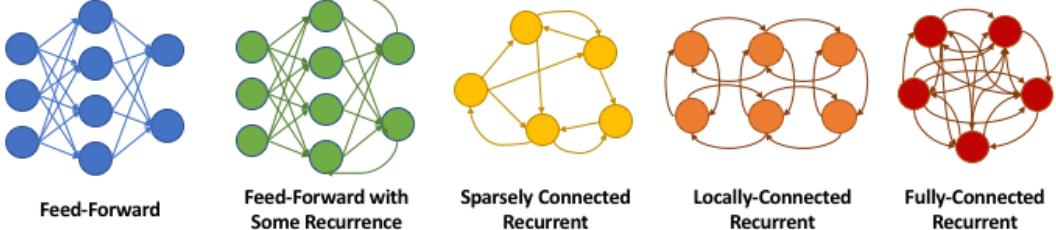


Fig. 6. Different network topologies that might be desired for neuromorphic systems. Determining the level of connectivity that is required for a neuromorphic implementation and then finding the appropriate hardware that can accommodate that level of connectivity is often a non-trivial exercise.

[1034]. Probabilistic neural networks, yet another special-case of feed-forward neural networks that have a particular type of functionality that is related to Bayesian calculations, have several neuromorphic implementations [1035]–[1043]. Single-layer feed-forward networks that utilize radial basis functions as the activation function of the neurons have also been used in neuromorphic implementations [530], [747], [825], [826], [1044]–[1053]. In recent years, with the rise of deep learning, convolutional neural networks have also seen several implementations in neuromorphic systems [1054]–[1075].

Recurrent neural networks are those that allow for cycles in the network, and they can have differing levels of connectivity, including all-to-all connections. Non-spiking recurrent neural networks have also been implemented in neuromorphic systems [7], [813], [829], [857], [1076]–[1099]. Reservoir computing models, including liquid state machines, have become popular in neuromorphic systems [1100]–[1106]. In reservoir computing models, recurrent neural networks are utilized as a “reservoir”, and outputs of the reservoir are fed into simple feed-forward networks. Both spiking and non-spiking implementations exist. Winner-take-all networks, which utilize recurrent inhibitory connections to force a single output, have also been implemented in neuromorphic systems [1107]–[1109]. Hopfield networks were especially common in earlier neuromorphic implementations, as is consistent with neural network research at that time [5], [6], [13], [15], [759], [764], [813], [1110]–[1148], but there are also more recent implementations [838], [1149]–[1159]. Similarly, associative memory based implementations were also significantly more popular in earlier neuromorphic implementations [1053], [1160]–[1182].

Stochastic neural networks, which introduce a notion of randomness into the processing of a network, have been utilized in neuromorphic systems as well [1183]–[1192]. A special case of stochastic neural networks, Boltzmann machines, have also been popular in neuromorphic systems. The general Boltzmann machine was utilized in neuromorphic systems primarily in the early 1990’s [12], [1193]–[1199], but it has seen occasional implementations in more recent publications [1200]–[1203]. A more common use of the Boltzmann model is the restricted Boltzmann machine, because the training time is significantly reduced when compared with a general Boltzmann machine. As such, there are several implementations of the restricted Boltzmann machine in neuromorphic implementations [1201]–[1211]. Restricted Boltzmann machines are

an integral component to deep belief networks, which have become more common with increased interest in deep learning and have been utilized in neuromorphic implementations [1212]–[1214].

Neural network models that focus on unsupervised learning rules have also been popular in neuromorphic implementations, beyond the STDP rules implemented in most spiking neural network systems. Hebbian learning mechanisms, of which STDP is one type in spiking neural networks, are common in non-spiking implementations of neuromorphic networks [1215]–[1231]. Self-organizing maps are another form of artificial neural network that utilize unsupervised learning rules, and they have been utilized in neuromorphic implementations [759], [1053], [1160], [1232]–[1248]. More discussion on unsupervised learning methods such as Hebbian learning or STDP is provided in Section IV.

The visual system has been a common inspiration for artificial neural network types, including convolutional neural networks. Two other visual system-inspired models, cellular neural networks [1249] and pulse-coupled neural networks [1250], have been utilized in neuromorphic systems. In particular, cellular neural networks were common in early neuromorphic implementations [1251]–[1260] and have recently seen a resurgence [1261]–[1268], whereas pulse-coupled networks were popular in the early 2000’s [1269]–[1277].

Other, less common neural network and neural network-adjacent models implemented in neuromorphic systems include cellular automata [1278]–[1282], fuzzy neural networks [1283], which combine fuzzy logic and artificial neural networks, and hierarchical temporal memory [1284], a network model introduced by Hawkins in [1285].

Figure 7 gives an overview of the network models implemented in neuromorphic systems. Figure 8 shows how some of the most frequently used models in neuromorphic implementations have evolved over time. As can be seen in the figures, spiking and feed-forward implementations are by far the most common, with spiking implementations seeing a rise in the last decade. General feed-forward networks had begun to taper off, but the popularity and success of convolutional neural networks in deep learning has increased in activity in the last five years.

#### D. Summary and Discussion

In terms of model selection for neuromorphic implementations, it is clear that there are a wide variety of options, and

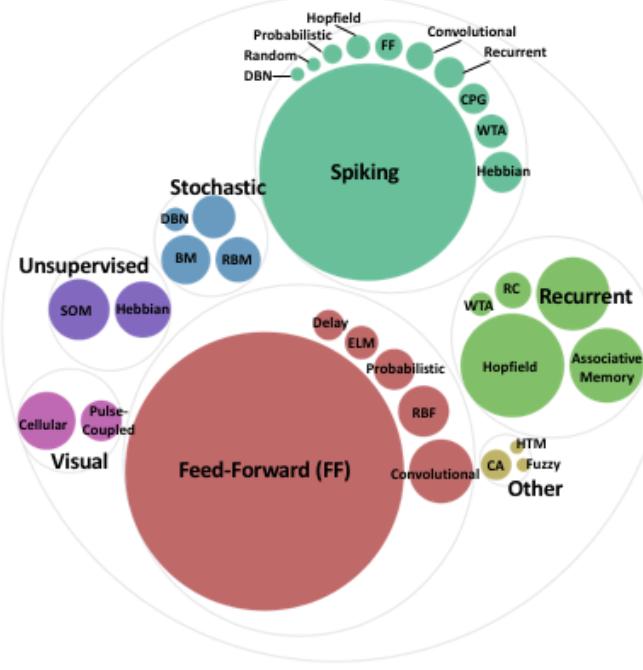


Fig. 7. A breakdown of network models in neuromorphic implementations, grouped by overall type and sized to reflect the number of associates papers.

much of the ground of potential biological and artificial neural network models has been tread at least once by previous work. The choice of model will be heavily dependent on the intent of the neuromorphic system. With projects whose goal it is to produce useful results for neuroscience, the models usually err on the side of biologically-plausible or at least biologically-inspired. For systems that have been moved to hardware for a particular application, such as image processing on a remote sensor or autonomous robots, more artificial neural network-like systems that have proven capabilities in those arenas may be most applicable. It is also the case that the model is chosen or adapted to fit within some particular hardware characteristics (e.g., selecting models that utilize STDP for memristors), or that the model is chosen for efficiency's sake, as is often the case for event-driven spiking neural network systems. On the whole, it is clear that most neural network models have, at some point in their history, been implemented in hardware.

#### IV. ALGORITHMS AND LEARNING

Some of the major open questions for neuromorphic systems revolve around algorithms. The chosen neuron, synapse, and network models have an impact on the algorithm chosen, as certain algorithms are specific to certain network topologies, neuron models, or other network model characteristics. Beyond that, a second issue is whether training or learning for a system should be implemented on chip or if networks should be trained off-chip and then transferred to the neuromorphic implementation. A third issue is whether the algorithms should be on-line and unsupervised (in which case they would necessarily need to be on-chip), whether off-line, supervised methods are sufficient, or whether a combination

of the two should be utilized. One of the key reasons neuromorphic systems are seen as a popular post-Moore's law era complementary architecture is their potential for on-line learning; however, even the most well-funded neuromorphic systems struggle to develop algorithms for programming their hardware, either in an off-line or on-line way. In this section, we focus primarily on on-chip algorithms, chip-in-the-loop algorithms, and algorithms that are tailored directly for the hardware implementation.

##### A. Supervised Learning

The most commonly utilized algorithm for programming neuromorphic systems is back-propagation. Back-propagation is a supervised learning method, and is not typically thought of as an on-line method. Back-propagation and its many variations can be used to program feed-forward neural networks, recurrent neural networks (usually back-propagation through time), spiking neural networks (where often feed-forward neural networks are adapted to spiking systems), and convolutional neural networks. The simplest possible approach is to utilize back-propagation off-line on a traditional host machine, as there are many available software implementations that have been highly optimized. We omit citing these approaches, as they typically utilize basic back-propagation, and that topic has been covered extensively in the neural network literature [1286]. However, there are also a large variety of implementations for on-chip back-propagation in neuromorphic systems [217], [575], [623], [628]–[630], [633], [641]–[644], [646], [647], [650], [657]–[659], [661], [662], [671], [691]–[697], [721], [726]–[728], [730], [738], [741], [745], [746], [759], [764], [775], [778]–[780], [784], [786], [788]–[790], [793], [795], [796], [798]–[803], [840], [843], [857], [872], [877], [896], [902], [941]–[965], [968], [970], [971], [973]–[975], [986], [987], [1010], [1022], [1032], [1034], [1052], [1089], [1128], [1287]–[1296]. There have been several works that adapt or tailor the back-propagation method to their particular hardware implementation, such as coping with memristive characteristics of synapses [634], [689], [1297]–[1299]. Other gradient descent-based optimization methods have also been implemented on neuromorphic systems for training, and they tend to be variations of back-propagation that have been adapted or simplified in some way [639], [645], [709], [716], [718], [719], [723], [792], [812], [844], [1030], [1122], [1300]–[1303]. Back-propagation methods have also been developed in chip-in-the-loop training methods [686], [702], [732], [815], [859]; in this case, most of the learning takes place on a host machine or off-chip, but the evaluation of the solution network is done on the chip. These methods can help to take into account some of the device's characteristics, such as component variation.

There are a variety of issues associated with back-propagation, including that it is relatively restrictive on the type of neuron models, networks models, and network topologies that can be utilized in an efficient way. It can also be difficult or costly to implement in hardware. Other approaches for on-chip supervised weight training have been utilized. These approaches include the least-mean-squares algorithm

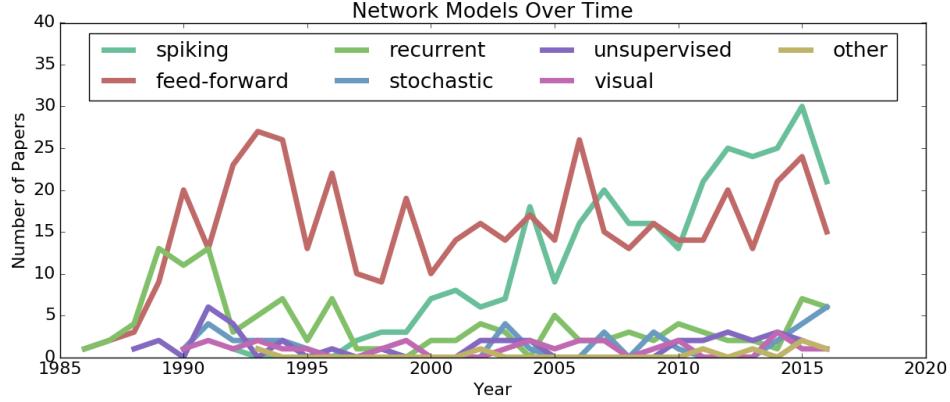


Fig. 8. An overview of how models for neuromorphic implementations have changed over time, in terms of the number of papers published per year.

[750], [787], [1025], [1026], weight perturbation [19], [625], [655], [669], [682], [698], [699], [708], [710], [712], [713], [715], [736], [834], [835], [841], [845]–[847], [856], [1078]–[1080], [1098], [1099], [1148], [1304], training specifically for convolutional neural networks [1305], [1306] and others [169], [220], [465], [714], [804], [864], [865], [1029], [1049], [1307]–[1320]. Other on-chip supervised learning mechanisms are built for particular model types, such as Boltzmann machines, restricted Boltzmann machines, or deep belief networks [12], [627], [1135], [1193], [1196], [1201], [1202], [1207] and hierarchical temporal memory [1284].

A set of nature-based or evolution-inspired algorithms have also been implemented for hardware. These implementations are popular because they do not rely on particular characteristics of a model to be utilized, and off-chip methods can easily utilize the hardware implementations in the loop. They can also be used to optimize within the characteristics and peculiarities of a particular hardware implementation (or even the characteristics and peculiarities of a particular hardware device instance). Off-chip nature-based implementations include differential evolution [1321]–[1324], evolutionary or genetic algorithms [484]–[487], [512], [570], [680], [700], [1076], [1082]–[1085], [1092], [1325]–[1337], and particle swarm optimization [1338]. We explicitly specify these off-chip methods because all of the nature-based implementations rely on evaluations of a current network solution and can utilize the chip during the training process (as a chip-in-the-loop method). There have also been a variety of implementations that include the training mechanisms on the hardware itself or in a companion hardware implementation, including both evolutionary/genetic algorithms [524], [554]–[556], [560], [622], [626], [1339]–[1350] and particle swarm optimization [1351]–[1354].

### B. Unsupervised Learning

There have been several implementations of on-chip, on-line, unsupervised training mechanisms in neuromorphic systems. These self-learning training algorithms will almost certainly be necessary to realize the full potential of neuromorphic implementations. Some early neuromorphic implementations of unsupervised learning were based on self-organizing maps

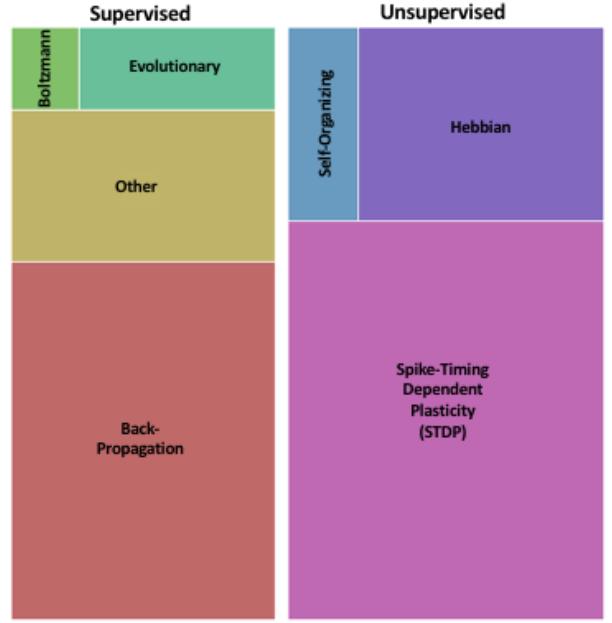


Fig. 9. An overview of on-chip training/learning algorithms. The size of the box corresponds to the number of papers in that category.

or self-organizing learning rules [759], [1022], [1053], [1197], [1198], [1233]–[1235], [1241], [1244], [1245], [1247], [1271], [1273], [1274], though there have been a few implementations in more recent years [1237], [1242], [1248], [1272]. Hebbian-type learning rules, which encompass a broad variety of rules, have been very popular as on-line mechanisms for neuromorphic systems, and there are variations that encompass both supervised and unsupervised learning [323], [334], [341], [342], [355], [362], [366], [385], [426], [427], [496], [573], [576], [580], [594]–[596], [598]–[602], [607], [612], [642], [660], [800], [918], [1053], [1114], [1126], [1143], [1144], [1146], [1149], [1151]–[1154], [1157], [1166], [1181], [1184], [1195], [1215], [1217]–[1219], [1221]–[1223], [1225]–[1231], [1355]–[1363]. Finally, perhaps the most popular on-line, unsupervised learning mechanism in neuromorphic systems is spike-timing dependent plasticity [21], [254], [328], [329], [340], [343], [347], [348], [352], [353], [357], [358], [365],

TABLE I  
ALGORITHMS PROS AND CONS

Algorithm Class	Any Model	Device Quirks	Complex to Implement	On-Line	Fast Time to Solution	Demonstrated Broad Applicability	Biologically-Inspired or Plausible
Back-Propagation	No	No	Yes	No	Yes	Yes	No
Evolutionary	Yes	Yes	No	No	No	Yes	Maybe
Hebbian	No	Yes	No	Yes	Maybe	No	Yes
STDP	No	Yes	Maybe	Yes	Maybe	No	Yes

[368]–[371], [375]–[377], [380], [384], [386], [388], [393], [396]–[399], [402], [406], [407], [410]–[412], [414], [423], [425], [432], [435]–[437], [442], [444], [446]–[449], [452], [456], [458]–[463], [473]–[475], [477], [478], [497], [502], [507], [516], [518], [519], [549], [552], [558], [561], [566], [571], [578], [579], [586], [597], [603], [838], [1036], [1064], [1169], [1307], [1330]–[1333], [1364]–[1453], which is a form of Hebbian-like learning that has been observed in real biological systems [1454]. The rule for STDP is generally that if a pre-synaptic neuron fires shortly before (after) the post-synaptic neuron, the synapse's weight will be increased (decreased) and the less time between the fires, the higher the magnitude of the change. There are also custom circuits for depression [351], [356], [409], [440], [1455], [1456] and potentiation [1457] in synapses in more biologically-inspired implementations. It is worth noting that, especially for STDP, wide applicability to a set of applications has not been fully demonstrated.

### C. Summary and Discussion

Spiking neural network-based neuromorphic systems have been popular for several reasons, including the power and/or energy efficiency of their event-driven computation and their closer biological inspiration relative to artificial neural networks in general. Though there have been proposed methods for training spiking neural networks that usually utilize STDP learning rules for synaptic weight updates, we believe that the full capabilities of spiking neuromorphic systems have not yet been realized by training and learning mechanisms. As noted in Section III-C, spiking neuromorphic systems have been frequently utilized for non-spiking network models. These models are attractive because we typically know how to train them and how to best utilize them, which gives a set of applications for spiking neuromorphic systems. However, we cannot rely on these existing models to realize the full potential of neuromorphic systems. As such, the neuromorphic computing community needs to develop algorithms for spiking neural network systems that can fully realize the characteristics and capabilities of those systems. This will require a paradigm shift in the way we think about training and learning. In particular, we need to understand how to best utilize the hardware itself in training and learning, as neuromorphic hardware systems will likely allow us to explore larger-scale spiking neural networks in a more computationally and resource efficient way than is possible on traditional von Neumann architectures.

An overview of on-chip learning algorithms is given in Figure 9. When choosing the appropriate algorithm for a neuromorphic implementation, one must consider several factors: (1) the chosen model, (2) the chosen material or device

type, (3) whether learning should be on-chip, (4) whether learning should be on-line, (5) how fast learning or training needs to take place, (6) how successful or broadly applicable the results will be, and (7) whether the learning should be biologically-inspired or biologically-plausible. Some of these factors for various algorithms are considered in Table I. For example, back-propagation is a tried and true algorithm, has been applied to a wide variety of applications and can be relatively fast to converge to a solution. However, if a device is particularly restrictive (e.g., in terms of connectivity or weight resolution) or has a variety of other quirks, then back-propagation requires significant adaptation to work correctly and may take significantly longer to converge. Back-propagation is also very restrictive in terms of the types of models on which it can operate. We contrast back-propagation with evolutionary-based methods, which can work with a variety of models, devices, and applications. Evolutionary methods can also be relatively easier to implement than more analytic approaches for different neuromorphic systems. However, they can be slow to converge for complex models or applications. Additionally, both back-propagation and evolutionary methods require feedback, i.e., they are supervised algorithms. Both Hebbian learning and STDP methods can be either supervised or unsupervised; they are also biologically-inspired and biologically-plausible, making them attractive to developers who are building biologically-inspired devices. The downside to choosing Hebbian learning or STDP is that they have not been demonstrated to be widely applicable.

There is still a significant amount of work to be done within the field of algorithms for neuromorphic systems. As can be seen in Figure 8, spiking network models are on the rise. Currently, STDP is the most commonly used algorithm proposed for training spiking systems, and many spiking systems in the literature do not specify a learning or training rule at all. It is worth noting that algorithms such as back-propagation and the associated network models were developed with the von Neumann architecture in mind. Moving forward for neuromorphic systems, algorithm developers need to take into account the devices themselves and have an understanding of how these devices can be utilized most effectively for both learning and training. Moreover, algorithm developers need to work with hardware developers to discover what can be done to integrate training and learning directly into future neuromorphic devices, and to work with neuroscientists in understanding how learning is accomplished in biological systems.

## V. HARDWARE

Here we divide hardware implementations of neuromorphic implementations into three major categories: digital, analog, and mixed analog/digital platforms. These are examined at a high-level with some of the more exotic device-level components utilized in neuromorphic systems explored in greater depth. For the purposes of this survey, we maintain a high-level view of the neuromorphic system hardware considered.

### A. High-Level

There have been many proposed taxonomies for neuromorphic hardware systems [1458], but most of those taxonomies divide the hardware systems at a high-level into analog, digital or mixed analog/digital implementations. Before diving into the neuromorphic systems themselves, it is worthwhile to note the major characteristics of analog and digital systems and how they relate to neuromorphic systems. Analog systems utilize native physical characteristics of electronic devices as part of the computation of the system, while digital systems tend to rely on Boolean logic-based gates, such as AND, OR, and NOT, for building computation. The biological brain is an analog system and relies on physical properties for computation and not on Boolean logic. Many of the computations in neuromorphic hardware lend themselves to the sorts of operations that analog systems naturally perform. Digital systems rely on discrete values while analog systems deal with continuous values. Digital systems are usually (but not always) synchronous or clock-based, while analog systems are usually (but not always) asynchronous; in neuromorphic, however, this rule of thumb is often not true, as even the digital systems tend to be event-driven and analog systems sometimes employ clocks for synchronization. Analog systems tend to be significantly more noisy than digital systems; however, there have been some arguments that because neural networks can be robust to noise and faults, they may be ideal candidates for analog implementation [1459]. Figure 10 gives an overall summary breakdown of high-level breakdown of different neuromorphic hardware implementations.

1) **Digital:** Two broad categories of digital systems are addressed here. The first is field programmable gate arrays or FPGAs. FPGAs have been frequently utilized in neuromorphic systems [86], [169], [192], [194], [200], [202], [206], [207], [217], [481], [489]–[570], [573], [575], [587], [588], [605], [617]–[619], [805], [806], [871]–[940], [966]–[1023], [1029], [1032]–[1034], [1037]–[1043], [1049]–[1053], [1067]–[1075], [1095]–[1099], [1104]–[1106], [1139], [1141]–[1148], [1155]–[1159], [1179]–[1182], [1187]–[1192], [1209]–[1211], [1213], [1214], [1245]–[1248], [1267], [1268], [1277], [1279]–[1282], [1287], [1289], [1293], [1304], [1339]–[1348], [1350]–[1352], [1354], [1360], [1361], [1460]–[1525]. For many of these implementations, the use of the FPGA is often utilized as a stop-gap solution on the way to a custom chip implementation. In this case, the programmability of the FPGA is not utilized as part of the neuromorphic implementation; it is simply utilized to program the device as a neuromorphic system that is then evaluated. However, it is also frequently the case that the

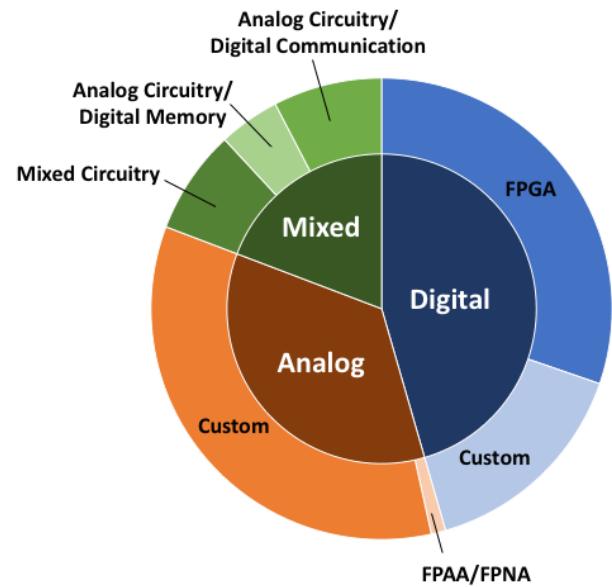


Fig. 10. An overview of hardware implementations in neuromorphic computing. These implementations are relatively basic hardware implementations and do not contain the more unusual device components discussed in Section V-B.

FPGA is utilized as the final implementation, and in this case, the programmability of the device can be leveraged to realize radically different network topologies, models, and algorithms. Because of their relative ubiquity, most researchers have access to at least one FPGA and can work with languages such as VHDL or Verilog (hardware description languages) to implement circuits in FPGAs. If the goal of developing a neuromorphic system is to achieve speed-up over software simulations, then FPGAs can be a great choice. However, if the goal is to achieve a small, low-power system, then FPGAs are probably not the correct approach. Liu and Wang point out several advantages of FPGAs over both digital and analog ASIC implementations, including shorter design and fabrication time, reconfigurability and reusability for different applications, optimization for each problem, and easy interface with a host computer [1526].

Full custom or application specific integrated circuit (ASIC) chips have also been very common for neuromorphic implementations [6], [9], [348], [350], [389]–[404], [438], [477], [677], [683], [749]–[764], [764]–[808], [1047], [1048], [1054]–[1060], [1100], [1101], [1118]–[1130], [1170], [1183]–[1185], [1204], [1205], [1212], [1236]–[1242], [1260], [1275], [1283], [1363], [1410], [1527]–[1561]. IBM's TrueNorth, one of the most popular present-day neuromorphic implementations, is a full custom ASIC design [1562]–[1569]. The TrueNorth chip is partially asynchronous and partially synchronous, in that some activity does not occur with the clock, but the clock governs the basic time step in the system. A core in the TrueNorth system contains a 256x256 crossbar configuration that maps incoming spikes to neurons. The behavior of the system is deterministic, but there is the ability to generate stochastic behavior through pseudo-random source. This stochasticity can be exactly replicated in a software

simulation.

SpiNNaker, another popular neuromorphic implementation, is also a full custom digital, massively parallel system [1570]–[1593]. SpiNNaker is composed of many small integer cores and a custom interconnect communication scheme which is optimized for the communication behavior of a spike-based network architecture. That is, the communication fabric is meant to handle a large number of very small messages (spikes). The processing unit itself is very flexible and not custom for neuromorphic, but the configuration of each SpiNNaker chip includes instruction and data memory in order to minimize access time for frequently used data. Like TrueNorth, SpiNNaker supports the cascading of chips to form larger systems.

TrueNorth and SpiNNaker provide good examples of the extremes one can take with digital hardware implementations. TrueNorth has chosen a fixed spiking neural network model with leaky integrate-and-fire neurons and limited programmable connectivity, and there is no on-chip learning. It is highly optimized for the chosen model and topology of the network. SpiNNaker, on the other hand, is extremely flexible in its chosen neuron model, synapse model, and learning algorithm. All of those features and the topology of the network are extremely flexible. However, this flexibility comes at a cost in terms of energy efficiency. As reported by Furber in [1594], TrueNorth consumes 25 pJ per connection, whereas SpiNNaker consumes 10 nJ per connection.

**2) Analog:** Similar to the breakdown of digital systems, we separate analog systems into programmable and custom chip implementations. As there are FPGAs for digital systems, there are also field programmable analog arrays (FPAs). For many of the same reasons that FPGAs have been utilized for digital neuromorphic implementations, FPAs have also been utilized [481], [483]–[488], [604], [869], [1028], [1595]. There have also been custom FPAs specifically developed for neuromorphic systems, including the field programmable neural array (FPNA) [482] and the NeuroFPA [870]. These circuits contain programmable components for neurons, synapses, and other components, rather than being more general FPAs for general analog circuit design.

It has been pointed out that custom analog integrated circuits and neuromorphic systems have several characteristics that make them well suited for one another. In particular, factors such as conservation of charge, amplification, thresholding and integration are all characteristics that are present in both analog circuitry and biological systems [1]. In fact, the original term neuromorphic was used to refer to analog designs. Moreover, taking inspiration from biological neural systems and how they operate, neuromorphic based implementations have the potential to overcome some of the issues associated with analog circuits that have prevented them from being widely accepted. Some of these issues are dealing with global asynchrony and noisy, unreliable components [1459]. For both of these cases, systems such as spiking neural networks are natural applications for analog circuitry because they can operate asynchronously and can deal with noise and unreliability.

One of the common approaches for analog neuromorphic systems is to utilize circuitry that operates in subthreshold

mode, typically for power efficiency purposes [101], [325], [330], [334], [373], [576], [577], [641], [647], [654], [665], [684], [700], [704], [704], [720], [721], [727], [737], [1045], [1079], [1080], [1084], [1089], [1160]–[1163], [1274], [1394], [1411], [1596]–[1619]. In fact, the original neuromorphic definition by Carver Mead referred to analog circuits that operated in subthreshold mode [1]. There are a large variety of other neuromorphic analog implementations [7], [8], [12], [14], [17]–[19], [99], [100], [323], [324], [326]–[329], [331]–[333], [335]–[372], [374]–[387], [516], [571], [572], [578]–[580], [594]–[603], [606]–[610], [612]–[614], [620]–[640], [642]–[646], [648]–[653], [655]–[664], [666]–[683], [685]–[699], [701]–[703], [705]–[719], [722]–[726], [728]–[736], [738]–[747], [747], [748], [1030], [1031], [1035], [1044], [1046], [1076]–[1078], [1081]–[1083], [1085]–[1088], [1090]–[1093], [1110]–[1117], [1164]–[1169], [1193]–[1196], [1215]–[1220], [1232]–[1235], [1251]–[1259], [1269]–[1273], [1313], [1320], [1324], [1359], [1395], [1419], [1429], [1455], [1457], [1597], [1620]–[1720].

**3) Mixed Analog/Digital:** Mixed analog/digital systems are also very common for neuromorphic systems [5], [15], [16], [21], [408], [409], [428], [430]–[432], [440]–[444], [450], [451], [456], [457], [459]–[467], [471], [473], [477]–[479], [585], [593], [809], [810], [812], [818], [830], [833], [839]–[841], [843], [848], [850], [852], [853], [858], [860], [1061], [1062], [1094], [1102], [1130], [1132], [1135], [1136], [1173]–[1176], [1199], [1203], [1244], [1367], [1434], [1444], [1721]–[1745]. Because of its natural similarity to biological systems, analog circuitry has been commonly utilized in mixed analog/digital neuromorphic systems to implement the processing components of neurons and synapses. However, there are several issues with analog systems that can be overcome by utilizing digital components, including unreliability.

In some neuromorphic systems, it has been the case that synapse weight values or some component of the memory of the system are stored using digital components, which can be less noisy and more reliable than analog-based memory components [405], [410], [411], [413], [422], [425], [445], [458], [814]–[817], [819]–[821], [821], [823], [824], [828], [834], [835], [837], [842], [844]–[846], [849], [851], [856], [857], [859], [861], [1107], [1131], [1137], [1138], [1186], [1202], [1223], [1243], [1746]–[1760]. For example, synaptic weights are frequently stored in digital memory for analog neuromorphic systems. Other neuromorphic platforms are primarily analog, but utilize digital communication, either within the chip itself, to and from the chip, or between neuromorphic chips [13], [133], [406], [412], [413], [415], [417]–[421], [424], [429], [434]–[437], [446]–[449], [452]–[455], [468]–[470], [472], [480], [586], [615], [616], [813], [826], [827], [829], [854], [855], [1024], [1108], [1109], [1133], [1134], [1171], [1172], [1198], [1221], [1276], [1372], [1452], [1453], [1761]–[1776]. Communication within and between neuromorphic chips is usually in the form of digital spikes for these implementations. Using digital components for programmability or learning mechanisms has also been common in mixed analog/digital systems [407], [412], [416], [423], [433], [439], [825], [831], [832], [1197], [1201], [1201], [1261], [1318], [1777]–[1781].

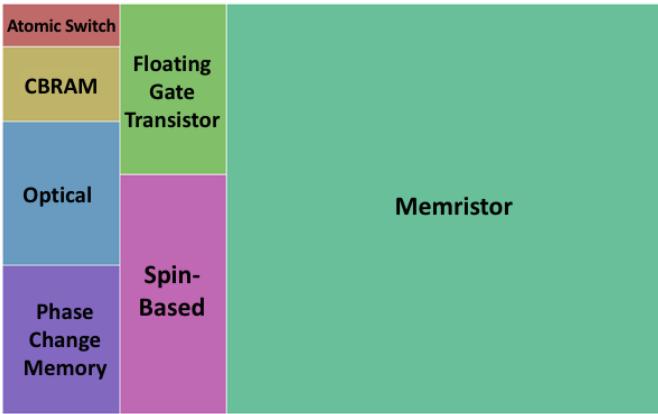


Fig. 11. Device-level components and their relative popularity in neuromorphic systems. The size of the boxes corresponds to the number of works referenced that have included those components.

Two major projects within the mixed analog/digital family are Neurogrid and BrainScaleS. Neurogrid is a primarily analog chip that is probably closest in spirit to the original definition of neuromorphic as coined by Mead [1782]–[1785]. Both of these implementation fall within the mixed analog/digital family because of their digital communication framework. BrainScaleS is a wafer-scale implementation that has analog components [363], [372], [444], [459], [1631], [1770], [1786]. Neurogrid operates in subthreshold mode, and BrainScaleS operates in superthreshold mode. The developers of BrainScaleS chose superthreshold mode because it allows BrainScaleS chips to operate at a much higher rate than is possible with Neurogrid, achieving a 10,000x speed-up [1594].

### B. Device-Level Components

In this section, we cover some of the non-standard device level or circuit level components that are being utilized in neuromorphic systems. These include a variety of components that have traditionally been used as memory technologies, but they also include elements such as optical components. Figure 11 gives an overview of the device-level components and also shows their relative popularity in the neuromorphic literature.

1) **Memristors:** Perhaps the most ubiquitous device-level component in neuromorphic systems is the “memory resistor” or the memristor. Memristors were a theoretical circuit element proposed by Leon Chua in 1971 [1787] and “found” by researchers at HP in 2008 [1788]. The key characteristic of memristive devices is that the resistance value of the memristor is dependent upon its historical activity. One of the major reasons that memristors have become popular in neuromorphic computing is their relationship to synapses; namely, circuits that incorporate memristors can exhibit STDP-like behavior that is very similar to what occurs in biological synapses. In fact, it has been proposed that biological STDP can be explained by memristance [1789]. Memristors can be and have been made from a large variety of materials, some of which will be discussed in Section V-C, and these different materials can exhibit radically different characteristics. Another reason for utilizing memristors in neuromorphic systems is their

potential for building energy efficient circuitry, and this has been studied extensively, with several works focused entirely on evaluating energy consumption of memristive circuitry in neuromorphic systems [1790]–[1797]. It has also been observed that neuromorphic implementations are a good fit for memristors because the inherent fault tolerance of neural network models can help mitigate effects caused by memristor device variation [1798]–[1802].

A common use of memristors in neuromorphic implementations is as part of or the entire synapse implementation (depending on the type of network) [862]–[868], [1025]–[1027], [1036], [1063]–[1065], [1103], [1149]–[1154], [1177], [1178], [1200], [1206]–[1208], [1262]–[1264], [1284], [1356], [1357], [1456], [1803]–[1820]. Sometimes the memristor is simply used as a synaptic weight storage element. In other cases, because of their plasticity-like properties, memristors have been used to implement synaptic systems that include Hebbian learning in general [1224]–[1231] or STDP in particular [254], [1364], [1365], [1369]–[1371], [1373]–[1377], [1381]–[1389], [1391]–[1393], [1397]–[1400], [1403]–[1405], [1409], [1412], [1413], [1416], [1420]–[1422], [1424], [1430]–[1432], [1436]–[1438], [1441]–[1443], [1445], [1450], [1451]. Perhaps the most common use of a memristor in neuromorphic systems is to build a memristor crossbar to represent the synapses in the network [475], [476], [478], [1288], [1294], [1296], [1301], [1302], [1307]–[1312], [1316], [1317], [1319], [1358], [1366], [1368], [1379], [1380], [1401], [1402], [1406], [1407], [1414], [1415], [1417], [1418], [1423], [1425], [1426], [1428], [1435], [1440], [1446]–[1449], [1512], [1513], [1821]–[1882]. Early physical implementations of memristors have been in the crossbar configuration. Crossbar realizations are popular in the literature mainly due to their density advantage by also because physical crossbars have been fabricated and shown to perform well. Because a single memristor cannot represent positive and negative weight values for a synapse (which may be required over the course of training for that synapse), multi-memristor synapses have been proposed, including memristor-bridge synapses, which can realize positive, negative and zero weight values [1883]–[1893]. Memristor-based synapse implementations that include forgetting effects have also been studied [1894], [1895]. Because of their relative ubiquity in neuromorphic systems, a set of training algorithms have been developed specifically with characteristics of memristive systems in mind, such as dealing with non-ideal device characteristics [220], [1295], [1303], [1314], [1329]–[1333], [1362], [1378], [1386], [1388], [1427], [1433], [1896]–[1905].

Memristors have also been utilized in neuron implementations [1416], [1906]–[1913]. For example, memristive circuits have been used to generate complex spiking behavior [1914]–[1916]. In another case, a memristor has been utilized to add stochasticity to an implemented neuron model [1208]. Memristors have also been used to implement Hodgkin-Huxley axons in hardware as part of a neuron implementation [1917], [1918].

It is worth noting that there are a variety of issues associated with using memristors for neuromorphic implementations. These include issues with memristor behavior that can seriously affect the performance of STDP [1919]–[1921], sneak paths [1922], and geometry variations [1923]. It is also

worth noting that a fair amount of theory about memristive neural networks has been established, including stabilization [1924]–[1982], synchronization [1927], [1930], [1947], [1974], [1976], [1981], [1983]–[2046], and passivity [2047]–[2063] criteria for memristive neural networks. However, these works are typically done with respect to ideal memristor models and may not be realistic in fabricated systems.

2) ***CBRAM and Atomic Switches:*** Conductive-bridging RAM (CBRAM) has also been utilized in neuromorphic systems. Similar to resistive RAM (ReRAM), which is implemented using metal-oxide based memristors or memristive materials, CBRAM is a non-volatile memory technology. CBRAM has been used to implement synapses [299], [1027], [1384], [1390], [1408], [1439], [2064]–[2069] and neurons [457], [2070]. CBRAM differs from resistive RAM in that it utilizes electrochemical properties to form and dissolve connections. CBRAM is fast, nanoscale, and has very low power consumption [2064]. Similarly, atomic switches, which are nano-devices related to resistive memory or memristors, control the diffusion of metal ions to create and destroy an atomic bridge between two electrodes [2071]. Atomic switches have been fabricated for neuromorphic systems. Atomic switches are typically utilized to implement synapses and have been shown to implement synaptic plasticity in a similar way to approaches with memristors [2072]–[2079].

3) ***Phase Change Memory:*** Phase change memory elements have been utilized in neuromorphic systems, usually to achieve high density. Phase change memory elements have commonly been used to realize synapses that can exhibit STDP. Phase change memory elements are usually utilized for synapse implementations [261], [2080]–[2099] or synapse weight storage [2100]–[2103], but they have also been used to implement both neurons and synapses [2104]–[2106].

4) ***Spin Devices:*** One of the proposed beyond-CMOS technologies for neuromorphic computing is spintronics (i.e., magnetic devices). Spintronic devices and components have been considered for neuromorphic implementation because they allow for a variety of tunable functionalities, are compatible with CMOS, and can be implemented at nanoscale for high density. The types of spintronic devices utilized in neuromorphic systems include spin-transfer torque devices, spin-wave devices, and magnetic domain walls [2107]–[2111]. Spintronic devices have been used to implement neurons [1853], [1880], [2112]–[2118], synapses that usually incorporate a form of online learning such as STDP [2119]–[2126], and full networks or network modules [2127]–[2144].

5) ***Floating Gate Transistors:*** Floating-gate transistors, commonly used in digital storage elements such as flash memory [2145], have been utilized frequently in neuromorphic systems. As Aunet and Hartmann note, floating-gate transistors can be utilized as analog amplifiers, and can be used in analog, digital, or mixed-signal circuits for neuromorphic implementation [2146]. The most frequent uses for floating-gate transistors in neuromorphic systems have been either as analog memory cells for synaptic weight and/or parameter storage [2147]–[2155] or as a synapse implementation that usually includes a learning mechanism such as STDP [259], [281], [285], [2156]–[2168]. However, floating gate transistors have also

been used to implement a linear threshold element that could be utilized for neurons [2146], a full neuron implementation [2169], dendrite models [2170], and to estimate firing rates of silicon neurons [2171].

6) ***Optical:*** Optical implementations and implementations that include optical or photonic components are popular for neuromorphic implementations [2172]–[2181]. In the early days of neuromorphic computing, optical implementations were considered because they are inherently parallel, but it was also noted that the implementation of storage can be difficult in optical systems [2182], so their implementations became less popular for several decades. In more recent years, optical implementations and photonic platforms have reemerged because of their potential for ultrafast operation, relatively moderate complexity and programmability [2183], [2184]. Over the course of development of neuromorphic systems, optical and/or photonic components have been utilized to build different components within neuromorphic implementations. Optical neuromorphic implementations include optical or opto-electronic synapse implementations in early neuromorphic implementations [2185], [2186] and more recent optical synapses, including using novel materials [2187]–[2191]. There have been several proposed optical or photonic neuron implementations in recent years [150], [2192]–[2197].

### C. Materials for Neuromorphic Systems

One of the key areas of development in neuromorphic computing in recent years have been in the fabrication and characterization of materials for neuromorphic systems. Though we are primarily focused on the computing and system components of neuromorphic computing, we also want to emphasize the variety of new materials and nano-scale devices being fabricated and characterized for neuromorphic systems by the materials science community.

Atomic switches and CBRAM are two of the common nano-scale devices that have been fabricated with different materials that can produce different behaviors. A review of different types of atomic switches for neuromorphic systems is given in [2078], but common materials for atomic switches are  $\text{Ag}_2\text{S}$  [2072], [2073], [2076],  $\text{Cu}_2\text{S}$  [2074],  $\text{Ta}_2\text{O}_5$  [2077], and  $\text{WO}_{3-x}$  [2079]. Different materials for atomic switches can exhibit different switching behavior under different conditions. As such, the selection of the appropriate material can govern how the atomic switch will behave and will likely be application-dependent. CBRAM has been implemented using  $\text{GeS}_2/\text{Ag}$  [299], [457], [1027], [1384], [1439], [2066], [2068],  $\text{HfO}_2/\text{GeS}_2$  [2067],  $\text{Cu}/\text{Ti}/\text{Al}_2\text{O}_3$  [2070],  $\text{Ag}/\text{Ge}_{0.3}\text{Se}_{0.7}$  [1408], [2069], [2198],  $\text{Ag}_2\text{S}$  [2199]–[2201] and  $\text{Cu}/\text{SiO}_2$  [2069]. Similar to atomic switches, the switching behavior of CBRAM devices is also dependent upon the material selected; the stability and reliability of the device is also dependent upon the material chosen.

There are a large variety of implementations of memristors. Perhaps the most popular memristor implementations are based on transition metal-oxides (TMOs). For metal-oxide memristors, a large variety of different materials are used, including  $\text{HfO}_x$  [2202]–[2210],  $\text{TiO}_x$  [2211]–[2216],  $\text{WO}_x$  [2217]–[2221],  $\text{SiO}_x$  [2222], [2223],  $\text{TaO}_x/\text{TiO}_x$

[2224], [2225],  $\text{NiO}_x$  [2226]–[2228],  $\text{TaO}_x$  [2229]–[2231],  $\text{FeO}_x$  [2232],  $\text{AlO}_x$  [2233], [2234],  $\text{TaO}_x/\text{TiO}_x$  [2224], [2225],  $\text{HfO}_x/\text{ZnO}_x$  [2235], and PCMO [2236]–[2241]. Different metal oxide memristor types can produce different numbers and types of resistance states, which govern the weight values that can be “stored” on the memristor. They also have different endurance, stability, and reliability characteristics.

A variety of other materials for memristors have also been proposed. For example, spin-based magnetic tunnel junction memristors based on  $\text{MgO}$  have been proposed for implementations of both neurons and synapses [2242], though it has been noted that they have a limited range of resistance levels that make them less applicable to store synaptic weights [2231]. Chalcogenide memristors [2243]–[2245] have also been used to implement synapses; one of the reasons given for utilizing chalcogenide-based memristors is ultra-fast switching speeds, which allow for processes like STDP to take place at nanosecond scale [2243]. Polymer-based memristors have been utilized because of their low cost and tunable performance [2211], [2246]–[2254]. Organic memristors (which include organic polymers) have also been proposed [2211], [2255]–[2266].

Ferroelectric materials have been considered for building analog memory for synaptic weights [2267]–[2272], and synaptic devices [2273]–[2276], including those based on ferroelectric memristors [2277]–[2279]. They have primarily been investigated as three-terminal synaptic devices (as opposed other implementations that may be two-terminal). Three-terminal synaptic devices can realize learning processes such as STDP in the device itself [2273], [2278], rather than requiring additional circuitry to implement STDP.

Graphene has more recently been incorporated in neuromorphic systems in order to achieve more compact circuits. It has been utilized for both transistors [2280]–[2282] and resistors [2283] for neuromorphic implementations and in full synapse implementations [2284], [2285].

Another material considered for some neuromorphic implementations is the carbon nanotube. Carbon nanotubes have been proposed for use in a variety of neuromorphic components, including dendrites on neurons [2286]–[2290], synapses [235], [2291]–[2307], and spiking neurons [139], [2308]–[2310]. The reasons that carbon nanotubes have been utilized are that they can produce both the scale of neuromorphic systems (number of neurons and synapses) and density (in terms of synapses) that may be required for emulating or simulating biological neural systems. They have also been used to interact with living tissue, indicating that carbon-nanotube based systems may be useful in prosthetic applications of neuromorphic systems [2297].

A variety of synaptic transistors have also been fabricated for neuromorphic implementations, including silicon-based synaptic transistors [2311], [2312] and oxide-based synaptic transistors [2313]–[2325]. Organic electrochemical transistors [2326]–[2331] and organic nanoparticle transistors [2332]–[2335] have also been utilized to build neuromorphic components such as synapses. Similar to organic memristors, organic transistors are being pursued because of their low-cost processing and flexibility. Moreover, they are natural for

implementations of brain-machine interfaces or any kind of chemical or biological sensor [2326]. Interestingly, groups are pursuing the development of transistors within polymer based membranes that can be used in neuromorphic applications such as biosensors [2336]–[2340].

There is a very large amount of fascinating work being done in the materials science community to develop devices for neuromorphic systems out of novel materials in order to build smaller, faster, and more efficient neuromorphic devices. Different materials for even a single device implementation can have wildly different characteristics. These differences will propagate effects through the rest of the community, up through the device, high-level hardware, supporting software, model and algorithms levels of neuromorphic systems. Thus, as a community, it is important that we understand what implications different materials may have on functionality, which will almost certainly require close collaborations with the materials science community moving forward.

#### D. Summary and Discussion

In this section, we have looked at hardware implementations at the full device level, at the device component level, and at the materials level. There is a significant body of work in each of these areas. At the system level, there are fully functional neuromorphic systems, including both programmable architectures such as FPGAs and FPAs, as well as custom chip implementations that are digital, analog, or mixed analog/digital. A wide variety of novel device components beyond the basic circuit elements used in most device development have been utilized in neuromorphic systems. The most popular new component that is utilized is the memristor, but other device components are becoming popular, including other memory technologies such as CBRAM and phase change memory, as well as spin-based components, optical components, and floating gate transistors. There are also a large variety of materials being used to develop device components, and the properties of these materials will have fundamental effects on the way future neuromorphic systems will operate.

## VI. SUPPORTING SYSTEMS

In order for neuromorphic systems to be feasible as a complementary architecture for future computing, we must consider the supporting tools required for usability. Two of the key supporting systems for neuromorphic devices are communication frameworks and supporting software. In this section, we briefly discuss some of the work in these two areas.

#### A. Communication

Communication for neuromorphic systems includes both intra-chip and inter-chip communication. Perhaps the most common implementation of inter-chip communication is address event representation (AER) [1785], [2343]–[2350]. In AER communication, each neuron has a unique address, and when a spike is generated that will traverse between chips, the address specifies to which chip it will go. Custom PCI

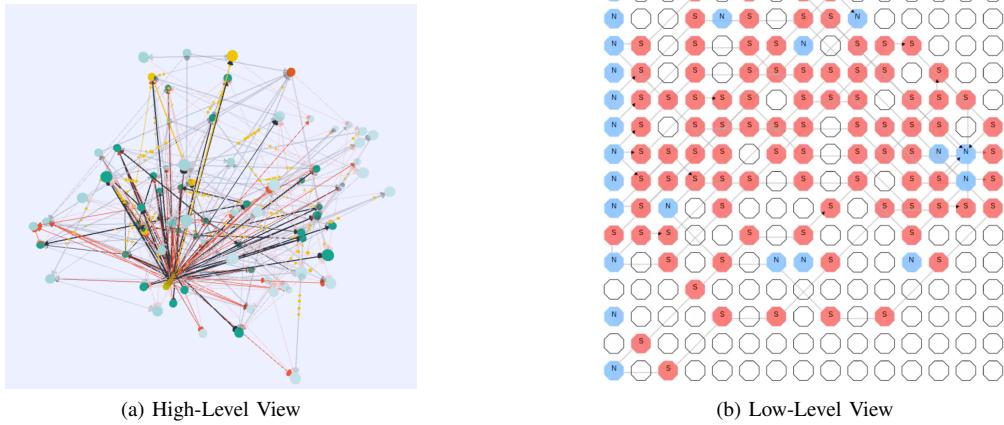


Fig. 12. Example neuromorphic visualization tools, giving a high-level view of a spiking neural network model [2341] and a low-level view of a network layout on a particular neuromorphic implementation [2342].

boards for AER have been implemented to optimize performance [2351], [2352]. Occasionally, inter-chip communication interfaces will have their own hardware implementations, usually in the form of FPGAs [2353]–[2357]. SpiNNaker’s interconnect system is one of its most innovative components; the SpiNNaker chips are interconnected in a toroidal mesh, and an AER communication strategy for inter-chip communication is used [1585], [1587], [2358]–[2366]. It is the communication framework for SpiNNaker that enables scalability, allowing tens of thousands of chips to be utilized together to simulate activity in a single network. A hierarchical version of AER utilizing a tree structure has also been implemented [2367], [2368]. One of the key components of AER communication is that it is asynchronous. In contrast, BrainScaleS utilizes an isynchronous inter-chip communication network, which means that events occur regularly [2369], [2370].

AER communication has also been utilized for on-chip communication [2371], [2372], but it has been noted that there are limits of AER for on-chip communication [2373]. As such, there are several other approaches that have been used to optimize intra-chip communication. For example, in early work with neuromorphic systems, buses were utilized for some on-chip communication systems [2374], [2375]. In a later work, one on-chip communication optimization removed buses as part of the communication framework to improve performance [879]. Vainbrand and Ginosaur examined different network-on-chip architectures for neural networks, including mesh, shared bus, tree, and point-to-point, and found network-on-chip multicast to give the highest performance [2376], [2377]. Ring-based communication for on-chip communication has also been utilized successfully [2378], [2379]. Communication systems specifically for feed-forward networks have also been studied [2380]–[2382].

One of the common beyond Moore's law era technologies to improve performance in communication that is being utilized across a variety of computing platforms (including traditional von Neumann computer systems) is three-dimensional (3D) integration. 3D integration has been utilized in neuromorphic systems even from the early days of neuromorphic, especially

for pattern recognition and object recognition tasks [2383], [2384]. In more recent applications, 3D integration has been used in a similar way as it would be for von Neumann architectures, where memory is stacked with processing [1058]. It has also been utilized to stack neuromorphic chips. Through silicon vias (TSVs) are commonly used to physically implement 3D integration approaches for neuromorphic systems [1058], [2066], [2385]–[2387], partially because utilizing TSVs in neuromorphic systems help mitigate some of the issues that arise with using TSVs, such as parasitic capacitance [2388]; however, other technologies have also been utilized in 3D integration, such as microbumps [2389]. 3D integration is commonly used in neuromorphic systems with a variety of other technologies, such as memristors [866], [2390]–[2393], phase change memory [2093], and CMOS-molecular (CMOL) systems [2394].

### *B. Supporting Software*

Supporting software will be a vital component in order for neuromorphic systems to be truly successful and accepted both within and outside the computing community. However, there has not been much focus on developing the appropriate tools for these systems. In this section, we discuss some efforts in developing supporting software systems for different neuromorphic implementations and use-cases.

One important set of software tools consist of custom hardware synthesis tools [628], [871], [2395]–[2401]. These synthesis tools typically take a relatively high level description and convert it to very low level representations of neural circuitry that can be used to implement neuromorphic systems. They tend to generate application specific circuits. That is, these tools are meant to work within the confines of a particular neuromorphic system, but also generate neuromorphic systems for particular applications.

A second set of software tools for neuromorphic systems are tools that are meant for programming existing neuromorphic systems. These fall into two primary categories: mapping and programming. Mapping tools are usually meant to take an existing neural network model representation, probably trained

offline using existing methods such as back-propagation, and convert or map that neural network model to a particular neuromorphic architecture [414], [1588], [1589], [2402]–[2413]. These tools typically take into account restrictions associated with the hardware, such as connectivity restrictions or parameter value bounds, and make appropriate adaptations to the network representation to work within those restrictions.

Programming tools, in contrast to mapping tools, are built so that a user can explicitly program a particular neuromorphic architecture [566], [1515], [2342], [2414]–[2424]. These can allow the user to program at a low level by setting different parameter and topology configurations, or by utilizing custom training methods built specifically for a particular neuromorphic architecture. The Corelet paradigm used in TrueNorth programming fits into this category [2425]. Corelets are pre-programmed modules that accomplish different tasks. Corelets can be used as building blocks to program networks for TrueNorth that solve more complex tasks. There have also been some programming languages for neuromorphic systems such as PyNN [2426], [2427], PyNCS [2428], and even a neuromorphic instruction set architecture [2429]. These languages have been developed to allow users to describe and program neuromorphic systems at a high-level.

Software simulators have also been key in developing usable neuromorphic systems [1515], [1587], [2065], [2342], [2407], [2417], [2430]–[2440]. Software-based simulators are vital for verifying hardware performance, testing new potential hardware changes, and for development and use of training algorithms. If the hardware has not been widely deployed or distributed, software simulators can be key to developing a user base, even if the hardware has not been fabricated beyond simple prototypes. Visualization tools that show what is happening in neuromorphic systems can also be key to allowing users to understand how neuromorphic systems solve problems and to inspire further development within the field [2341], [2342], [2416], [2419], [2441]. These visualization tools are often used in combination with software simulations, and they can provide detailed information about what might be occurring at a low-level in the hardware. Figure 12 provides two examples of visualizations for neuromorphic systems.

### C. Summary

When building a neuromorphic system, it is extremely important to think about how the neuromorphic system will actually be used in real computing systems and with real users. Supporting systems, including communication on-chip and between chips and supporting software, will be necessary to enable real utilization of neuromorphic systems. Compared to the number of hardware implementations of neuromorphic systems there are very few works that focus on the development of supporting software that will enable ease-of-use for these systems. There is significantly more work to be done, especially on the supporting software side, within the field of neuromorphic computing. It is absolutely necessary that the community develop software tools alongside hardware moving forward.

## VII. APPLICATIONS

The “killer” applications for neuromorphic computing, or the applications that best showcase the capabilities of neuromorphic computers and devices, have yet to be determined. Obviously, various neural network types have been applied to a wide variety of applications, including image [2442], speech [2443], and data classification [2444], control [2445], and anomaly detection [2446]. Implementing neural networks for these types of applications directly in hardware can potentially produce lower power, faster computation, and a smaller footprint than can be delivered on a von Neumann architecture. However, many of the application spaces that we will discuss in this section do not actually require any of those characteristics. In addition, spiking neural networks have not been studied to their full potential in the way that artificial neural networks have been, and it may be that physical neuromorphic hardware is required in order to determine what the killer applications for spiking neuromorphic systems will be moving forward. This goes hand-in-hand with the appropriate algorithms being developed for neuromorphic systems, as discussed in Section IV. Here, we discuss a variety of applications of neuromorphic systems. We omit one of the major application areas, which is utilizing neuromorphic systems in order to study neuroscience via faster, more efficient simulation than is possible on traditional computing platforms. Instead, we focus on other real-world applications to which neuromorphic systems have been applied. The goal of this section is to provide a scope of the types of problems neuromorphic systems have successfully tackled, and to provide inspiration to the reader to apply neuromorphic systems to their own set of applications. Figure 13 gives an overview of the types of applications of neuromorphic systems and how popular they have been.

There are a broad set of neuromorphic systems that have been developed entirely based on particular sensory systems, and applied to those particular application areas. The most popular of these “sensing” style implementations are vision-based systems, which often have architectures that are entirely based on replicating various characteristics of biological visual systems [299], [324], [344]–[346], [416], [469], [510], [584], [1054], [1057], [1161], [1179], [1186], [1432], [1439], [1456], [1459], [1521]–[1525], [1597], [1598], [1607], [1608], [1612], [1613], [1615], [1643], [1644], [1710], [1711], [1715], [1717], [1718], [1723], [1725], [1727], [1738], [1762], [1767], [1774], [1881], [2160], [2165], [2292], [2351], [2371], [2447]–[2513]. Though vision-based systems are by far the most popular sensory-based systems, there are also neuromorphic auditory systems [127], [299], [335], [374], [1269], [1283], [1418], [1434], [1439], [1460]–[1462], [1649], [1744], [2393], [2441], [2463], [2514]–[2521], olfactory systems [720], [1514], [1515], [2522]–[2531], and somatosensory or touch-based systems [1520], [2532]–[2537].

Another class of applications for neuromorphic systems are those that either interface directly with biological systems or are implanted or worn as part of other objects that are usually used for medical treatment or monitoring [2538]. A key feature of all of these applications is that they require devices that can be made very small and require very low-

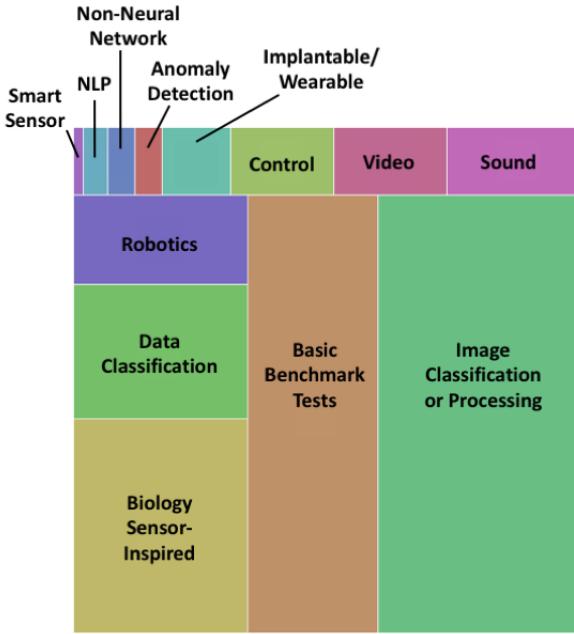


Fig. 13. Breakdown of applications to which neuromorphic systems have been applied. The size of the boxes corresponds to the number of works in which a neuromorphic system was developed for that application.

power. Neuromorphic systems have become more popular in recent years in brain-machine interfaces [237], [412], [590], [1625], [2538]–[2545]. By their very nature, spike-based neuromorphic models communicate using the same type of communication as biological systems, so they are a natural choice for brain-machine or brain-computer interfaces. Other wearable or implantable neuromorphic systems have been developed for pacemakers or defibrillator systems [18], [602], [651]–[653], retina implants [2546], wearable fall detectors for elderly users [1019], and prosthetics [2547].

Robotics applications are also very common for neuromorphic systems. Very small and power efficient systems are often required for autonomous robots. Many of the requirements for robotics, including motor control, are applications that have been successfully demonstrated in neural networks. Some of the common applications of neuromorphic systems for robotics include learning a particular behavior [2548], [2549], locomotion control or control of particular joints to achieve a certain motion [67]–[69], [361], [663], [1082], [1083], [1261], [1279], [1527], [1784], [1885], [2550], [2551], social learning [2552], [2553], and target or wall following [498], [606], [1576], [1682], [2554]. Thus far, in terms of robotics, the most common use of neuromorphic implementations is for autonomous navigation tasks [16], [195], [393], [486], [532], [547], [735], [1077], [1329]–[1333], [1339], [1503], [1539], [1563], [1671], [1716], [2379], [2555]–[2560]. In the same application space as robotics is the generation of motion through central pattern generators (CPGs). CPGs generate oscillatory motions, such as those used to generate swimming motions in lampreys or walking gaits. There are a variety of implementations of CPGs in neuromorphic systems [615]–[619], [1084], [1313], [1335], [1561], [1609], [1622], [1637], [1647], [1729], [1731]–[1734], [1739], [1775].

Control tasks have been popular for neuromorphic systems because they typically require real-time performance, are often deployed in real systems that require small volume and low power, and have a temporal processing component, so they benefit from models that utilize recurrent connections or delays on synapses. A large variety of different control applications have utilized neuromorphic systems [466], [687], [688], [863], [872], [895], [902], [903], [920], [932], [962], [1017], [1051], [1085], [1660], [2561], [2562], but by far the most common control test case is the cart-pole problem or the inverted pendulum task [487], [512], [792], [902], [903], [1008], [1045], [1337], [1340], [2563]. Neuromorphic systems have also been applied to video games, such as Pong [1563], PACMAN [2405], and Flappy Bird [1337].

An extremely common use of both neural networks and neuromorphic implementations has been on various image-based applications, including edge detection [220], [339], [520], [783], [829], [922], [1260], [1873], [2107], [2118], [2141], [2287], [2564], image compression [641], [721], [875], [960], [1243], [1263], image filtering [15], [338], [1112], [1255], [1267], [1492], [1516], [1551], [1779], [1886], [1887], [2565], [2566], image segmentation [141], [490], [541], [921], [1272]–[1274], [1277], [1278], [1679], [1712], [1713], [2567]–[2569], and feature extraction [388], [392], [608], [827], [854], [1165], [1269], [1270], [1502], [1606], [1611], [1658], [1719], [2065], [2132], [2570]–[2572]. Image classification, detection, or recognition is an extremely popular application for neural networks and neuromorphic systems. The MNIST data set, subsets of the data set, and variations of the data set has been used to evaluate many neuromorphic implementations [211], [264], [267], [290], [297], [316], [395], [491], [557], [584], [585], [593], [790], [862], [936], [941], [967], [1055], [1061], [1063]–[1065], [1183], [1184], [1205], [1207], [1208], [1212]–[1214], [1296]–[1298], [1301], [1305]–[1307], [1371], [1378], [1379], [1390], [1427], [1433], [1563], [1567], [1593], [1796], [1797], [1800], [1801], [1818], [1827], [1829], [1831], [1833], [1835], [1840], [1842], [1845], [1846], [1848], [1852], [1853], [1855], [1856], [1870], [1873], [1877], [1903], [1904], [1906], [1907], [1922], [2080], [2086], [2100]–[2103], [2115], [2116], [2122], [2126], [2130], [2137], [2143], [2209], [2215], [2224], [2241], [2300], [2342], [2389], [2407], [2413], [2418], [2429], [2433], [2568], [2573]–[2594]. Other digit recognition tasks [448], [706], [731], [788], [798], [813], [852], [853], [1130], [1149], [1380], [1415], [1446], [1798], [1819], [1852], [1878], [1895], [2283], [2395], [2396], [2593], [2595]–[2599] and general character recognition tasks [197], [231], [438], [478], [545], [559], [665], [670], [714], [730], [757], [758], [768], [831], [832], [888], [899], [946], [989], [991], [992], [1022], [1157], [1158], [1172], [1304], [1312], [1316], [1317], [1349], [1356], [1381], [1401], [1402], [1435], [1543], [1552], [1558], [1714], [1830], [1858], [1860], [1891], [1892], [1902], [1923], [2070], [2128], [2135], [2140], [2141], [2144], [2350], [2411], [2585], [2600]–[2612] have also been very popular. Recognition of other patterns such as simple shapes or pixel patterns have also been used as applications for neuromorphic systems [119], [191], [217], [308], [375], [446], [528], [533], [549], [580], [586], [598], [599], [603], [689], [765], [785], [805]–[808], [821], [953], [955], [1113], [1152], [1153],

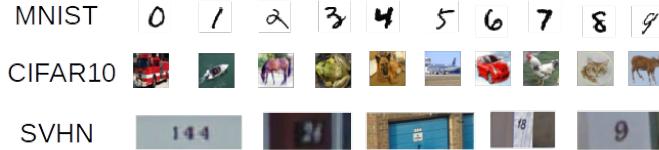


Fig. 14. Examples from different image data sets (MNIST [2618], CIFAR10 [2619], and SVHN [2620]) to which neuromorphic systems have been applied for classification purposes.

[1167], [1180], [1257], [1287], [1289], [1318], [1398], [1399], [1420], [1423], [1426], [1441], [1445], [1455], [1702], [1795], [1839], [1851], [1857], [1867], [1868], [1879], [1880], [1957], [2085], [2093], [2096], [2097], [2112], [2202], [2277], [2392], [2613], [2614].

Other image classification tasks that have been demonstrated on neuromorphic systems include classifying real world images such as traffic signs [1018], [1065], [1305], face recognition or detection [582], [1067], [1204], [1284], [1885], [2130], [2585], [2591], [2615], car recognition or detection [1883], detecting air pollution in images [2616], detection of manufacturing defects or defaults [1692], hand gesture recognition [558], [1038], human recognition [1422], object texture analysis [2617], and other real world image recognition tasks [825], [1037], [1058], [2127]. There are several common real-world image data sets that have been evaluated on neuromorphic systems, including the CalTech-101 data set [867], [1068], the Google Street-View House Number (SVHN) data set [316], [2580], [2585], [2590], [2591], the CIFAR10 data set [587], [592], [1066], [1069], [2130], [2590], [2591], and ImageNet [1827]. Evaluations of how well neuromorphic systems implement AlexNet, a popular convolutional neural network architecture for image classification, have also been conducted [1056], [1074]. Examples of images from the MNIST data set, the CIFAR10, and the SVHN data set are given in Figure 14 to demonstrate the variety of images that neuromorphic systems have been used to successfully classify or recognize.

A variety of sound-based recognition tasks have also been considered with neuromorphic systems. Speech recognition, for example, has been a common application for neuromorphic systems [502], [591], [628], [754], [755], [812], [868], [976], [978], [984], [1004]–[1006], [1030], [1031], [1048], [1104], [1105], [1206], [1463], [1546], [1665], [1859], [1861], [2448], [2621]–[2624]. Neuromorphic systems have also been applied to music recognition tasks [584], [588], [2425]. Both speech and music recognition tasks may require the ability to process temporal components, and may have real-time constraints. As such, neuromorphic systems that are based on recurrent or spiking neural networks that have an inherent temporal processing component are natural fits for these applications. Neuromorphic systems have also been used for other sound-based tasks, including speaker recognition [584], distinguishing voice activity from noise [592], and analyzing sound for identification purposes [336], [337]. Neuromorphic systems have also been applied to noise filtering applications as well

to translate noisy speech or other signals into clean versions of the signal [624], [644], [648], [649].

Applications that utilize video have also been common uses of neuromorphic systems. The most common example for video is object recognition within video frames [794], [1073], [1242], [1439], [1562], [1565], [1568], [2082], [2088]–[2090], [2416], [2625]–[2631]. This application does not necessarily require a temporal component, as it can analyze video frames as images. However, some of the other applications in video do require a temporal component, including motion detection [383], [572], [1768], [1769], [2632], motion estimation [1031], [1704], [2633], motion tracking [905], [917], [2634], [2635], and activity recognition [916], [2636].

Neuromorphic systems have also been applied to natural language processing (NLP) tasks, many of which require recurrent networks. Example applications in NLP that have been demonstrated using neuromorphic systems include sentence construction [388], sentence completion [1097], [2411], [2637], question subject classification [581], sentiment analysis [583], and document similarity [1239].

Tasks that require real-time performance, ability to deploy into an environment with a small footprint, and/or low power are common use cases for neuromorphic systems. Smart sensors are one area of interest, including humidity sensors [756], light intensity sensors [1009], and sensors on mobile devices that can be used to classify and authenticate users [2638]. Similarly, anomaly detectors are also applications for neuromorphic systems, including detecting anomalies in traffic [1825], biological data [2639], and industrial data [2639], applications in cyber security [1807], [2640], and fault detection in diesel engines [931] and analog chips [1686], [1687].

General data classification using neuromorphic systems has also been popular. There are a variety of different and diverse application areas in this space to which neuromorphic systems have been applied, including accident diagnosis [1015], cereal grain identification [657], [659], computer user analysis [2641], [2642], driver drowsiness detection [2434], gas recognition or detection [622], [943], [972], product classification [781], hyperspectral data classification [750], stock price prediction [1537], wind velocity estimation [939], solder joint classification [1050], solar radiation detection [929], climate prediction [966], and applications within high energy physics [982], [1018]. Applications within the medical domain have also been popular, including coronary disease diagnosis [954], pulmonary disease diagnosis [887], deep brain sensor monitoring [404], DNA analysis [1146], heart arrhythmia detection [2434], analysis of electrocardiogram (ECG) [900], [922], [965], [1007], electroencephalogram (EEG) [403], [1100], [1103], [1850], and electromyogram (EMG) [1039], [1103] results, and pharmacology applications [2643]. A set of benchmarks from the UCI machine learning repository [2644] and/or the Proben1 data set [710], [908], [974], [2444] have been popular in both neural network and neuromorphic systems, including the following data sets: building [998], [1840], connect4 [1842], [1845], gene [998], [1840], [1842], [1845], glass [951], [1055], [1338], heart [998], [2645], ionosphere [1029], [1055], [2645], iris [215], [305], [530], [573], [575], [612], [952], [959], [983], [1050], [1055], [1295], [1303], [1336],

[1342], [1345], [1346], [1504], [2646], [2647], lymphography [1842], [1845], mushroom [1840], [1842], [1845], phoneme [952], Pima Indian diabetes [998], [1027], [1336], [1338], [1504], [2648], semeion [983], thyroid [998], [1840], [1842], [1845], wine [1055], [1303], [1336], [2646], and Wisconsin breast cancer [305], [573], [612], [959], [998], [1029], [1288], [1295], [1303], [1336], [1338], [1340], [1842], [1845], [2645]. These data sets are especially useful because they have been widely used in the literature and can serve as points of comparison across both neuromorphic systems and neuromorphic models.

There are a set of relatively simple testing tasks that have been utilized in evaluating neuromorphic system behaviors, especially in the early development of new devices or architectures. In the early years of development, the two spirals problem was a common benchmark [1315], [2641], [2642], [2649], [2650].  $N$ -bit parity tasks have also been commonly used [209], [217], [625], [657]–[659], [661], [680], [696], [697], [737], [855], [1092], [1193], [1346], [1349], [1883]–[1885], [2640], [2650], [2651]. Basic function approximation has also been a common task for neuromorphic systems, where a mathematical function is specified and the neuromorphic system is trained to replicate its output behavior [196], [419]–[421], [514], [518], [519], [614], [628], [643], [715], [819], [873], [874], [971], [983], [984], [1024], [1053], [1078], [1079], [1098], [1148], [1304], [1354], [1538], [2214], [2397], [2652]–[2657]. Temporal pattern recall or classification [341], [351], [355], [390], [407], [411], [584], [595], [605], [1377], [1622], [2104], [2401], [2658], [2659] and spatiotemporal pattern classification [104], [382], [447], [473], [561], [1101], [1370], [1416], [1661], [1771], [1899], [2294], [2416], [2419], [2660]–[2666] have also been popular with neuromorphic systems, because they demonstrate the temporal processing characteristics of networks with recurrent connections and/or delays on the synapses. Finally, implementing various simple logic gates have been common tests for neural networks and neuromorphic systems, including AND [746], [834], [835], [896], [1224], [1289], [1400], [1805], [1902], [2255], [2295], [2667], [2668], OR [910], [1289], [1805], [1862], [1902], [2255], [2295], [2668], NAND [181], [864], [910], [1902], [1909], [1912], [2211], [2255], [2295], [2301], [2669], [2670], NOR [181], [864], [910], [1400], [1902], [1909], [1912], [2211], [2255], [2295], [2301], [2669], [2670], NOT [2667], [2670], and XNOR [712], [1400], [1902], [1912], [2671]. XOR has been especially popular because the results are not linearly separable, which makes it a good test case for more complex neural network topologies [97], [223], [227], [234], [276], [304], [536], [620], [628], [629], [633], [642], [647], [655], [670], [679], [682], [693], [698], [699], [702]–[704], [712], [713], [723], [726], [737], [741], [746], [799], [834], [835], [841], [844]–[848], [865], [928], [946], [949], [952], [954], [956], [957], [959], [1012], [1026], [1052], [1089], [1128], [1271], [1289], [1291], [1304], [1310], [1334], [1340], [1343], [1347], [1348], [1362], [1387], [1400], [1504], [1507], [1517], [1614], [1805], [1902], [1912], [2163], [2278], [2379], [2395], [2396], [2434], [2624], [2640]–[2642], [2668], [2671]–[2681].

In all of the applications discussed above, neuromorphic

architectures are utilized primarily as neural networks. However, there are some works that propose utilizing neuromorphic systems for non-neural network applications. Graph algorithms have been one common area of application, as most neuromorphic architectures can be represented as graphs. Example graph algorithms include maximum cut [1200], minimum graph coloring [1156], [1698], traveling salesman [1147], [2682], and shortest path [1131]. Neuromorphic systems have also been used to simulate motion in flocks of birds [1570] and for optimization problems [1697]. Moving forward, we expect to see many more use cases of neuromorphic architectures in non-neural network applications, as neuromorphic computers become more widely available and are considered simply as a new type of computer with specific characteristics that are radically different from the characteristics traditional von Neumann architecture.

## VIII. DISCUSSION: NEUROMORPHIC COMPUTING MOVING FORWARD

In this work, we have discussed a variety of components of neuromorphic systems: models, algorithms, hardware in terms of full hardware systems, device-level components, new materials, supporting systems such as communication infrastructure and supporting software systems, and applications of neuromorphic systems. There has clearly been a tremendous amount of work up until this point in the field of neuromorphic computing and neural networks in hardware. Moving forward, there are several exciting research directions in a variety of fields that can help revolutionize how and why we will use neuromorphic computers in the future (Figure 15).

From the machine learning perspective, the most intriguing question is what the appropriate training and/or learning algorithms are for neuromorphic systems. Neuromorphic computing systems provide a platform for exploring different training and learning mechanisms on an accelerated scale. If utilized properly, we expect that neuromorphic computing devices could have a similar effect on increasing spiking neural network performance as GPUs had for deep learning networks. In other words, when the algorithm developer is not reliant on a slow simulation of the network and/or training method, there is much faster turn around in developing effective methods. However, in order for this innovation to take place, algorithm developers will need to be willing to look beyond traditional algorithms such as back-propagation and to think outside the von Neumann box. This will not be an easy task, but if successful, it will potentially revolutionize the way we think about machine learning and the types of applications to which neuromorphic computers can be applied.

From the device level perspective, the use of new and emerging technologies and materials for neuromorphic devices is one of the most exciting components of current neuromorphic computing research. With today's capabilities in fabrication of nanoscale materials, many novel device components are certain to be developed. Neuromorphic computing researchers at all levels, including models and algorithms, should be collaborating with materials scientists as these new materials are developed in order to customize them for use in a variety

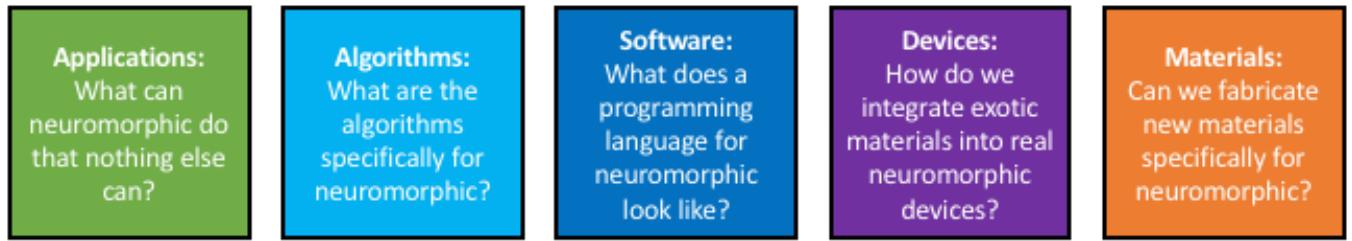


Fig. 15. Major neuromorphic computing research challenges in different fields.

of neuromorphic use cases. Not only is there potential for extremely small, ultra-fast neuromorphic computers with new technologies, but we may be able to collaborate to build new composite materials that elicit behaviors that are specifically tailored for neuromorphic computation.

From the software engineering perspective, neuromorphic computers represent a new challenge in how to develop the supporting software systems that will be required for neuromorphic computers to be usable by non-experts in the future. The neuromorphic computing community would greatly benefit from the inclusion of more software engineers as we continue to develop new neuromorphic devices moving forward, both to build supporting software for those systems, but also to inform the design themselves. Once again, neuromorphic computers require a totally different way of thinking than traditional von Neumann architectures. Building out programming languages specifically for neuromorphic devices wherein the device is not utilized as a neural network simulator but as a special type of computer with certain characteristics (e.g., massive parallelism and collocated memory and computation elements) is one way to begin to attract new users, and we believe such languages will be extremely beneficial moving forward.

From the end-user and applications perspective, there is much work that the neuromorphic community needs to do to develop and communicate use cases for neuromorphic systems. Some of those use cases include as a neuromorphic co-processor in a future heterogeneous computer, as smart sensors or anomaly detectors in Internet of Things applications, as extremely low power and small footprint intelligent controllers in autonomous vehicles, as *in situ* data analysis platforms on deployed systems such as satellites, and many other application areas. The potential to utilize neuromorphic systems for real-time spatiotemporal data analysis or real-time control in a very efficient way needs to be communicated to the community at large, so that those that have these types of applications will think of neuromorphic computers as one solution to their computing needs.

There are clearly many exciting areas of development for neuromorphic computing. It is also clear that neuromorphic computers could play a major role in the future computing landscape if we continue to ramp up research at all levels of neuromorphic computing, from materials all the way up to algorithms and models. Neuromorphic computing research would benefit from coordination across all levels, and as a

community, we should encourage that coordination to drive innovation in the field moving forward.

## IX. CONCLUSION

In this work, we have given an overview of past work in neuromorphic computing. The motivations for building neuromorphic computers have changed over the years, but the need for a non-von Neumann architecture that is low-power, massively parallel, can perform in real time, and has the potential to train or learn in an on-line fashion is clear. We discussed the variety of neuron, synapse and network models that have been used in neuromorphic and neural network hardware in the past, emphasizing the wide variety of selections that can be made in determining how the neuromorphic system will function at an abstract level. It is not clear that this wide variety of models will ever be narrowed down to one all encompassing model in the future, as each model has its own strengths and weaknesses. As such, the neuromorphic computing landscape will likely continue to encompass everything from feed-forward neural networks to highly-detailed biological neural network emulators.

We discussed the variety of training and learning algorithms that have been implemented on and for neuromorphic systems. Moving forward, we will need to address building training and learning algorithms specifically for neuromorphic systems, rather than adapting existing algorithms that were designed with an entirely different architecture in mind. There is great potential for innovation in this particular area of neuromorphic computing, and we believe that it is one of the areas for which innovation will have the most impact. We discussed high-level hardware views of neuromorphic systems, as well as the novel device-level components and materials that are being used to implement them. There is also significant room for continued development in this area moving forward. We briefly discussed some of the supporting systems for neuromorphic computers, such as supporting software, of which there is relatively little and from which the community would greatly benefit. Finally, we discuss some of the applications to which neuromorphic computing systems have been successfully applied.

The goal of this paper was to give the reader a full view of the types of research that has been done in neuromorphic computing across a variety of fields. As such, we have included all of the references in this version. We hope that this work will inspire others to develop new and innovative systems to

fill in the gaps with their own research in the field and to consider neuromorphic computers for their own applications.

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