The Impact of New Technology on Soft Error Rates

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***Abstract*—This paper presents the impact of new microprocessor technology on microprocessor soft error rate (SER). The results are based on Oracle's (formerly Sun Microsystems) neutron beam testing over the past several years. We describe how the tests were conducted and how the test results are used to influence microprocessor design. As microprocessor feature sizes decreased from 180nm to 65nm, memory error rates per bit decreased, but our data indicates a reversal of this trend at 40nm. Flop error rates still appear to be decreasing, even at a 28nm feature size We measure SER as a function of power supply voltage (Vdd) over a range of 1.2V down to 0.5V, and the data shows SER significantly increases as Vdd decreases. This result implies that dynamic voltage frequency scaling (DVFS), a commonly used microprocessor energy reduction technique, could cause a significant decrease in microprocessor reliability. The data also show that more energy-efficient transistors using back bias technique do not appear to significantly impact microprocessor reliability.**

Keywords-soft error; single-event upset; neutron beam testing; bit error rates

I. INTRODUCTION

Reliability has always been one of the key requirements in microprocessor designs at Oracle (formerly Sun Microsystems). With shrinking cell geometries, neutron-induced soft errors have become a greater concern. We conduct accelerated tests at the LANSCE test facility in Los Alamos [1] to characterize cell upsets, usually called single-event upsets (SEUs), in our microprocessors. We measure the SEU rate of unprotected memory cells and logic blocks of flops and/or latches in a neutron beam to determine the raw SEU rate of SRAM cells and flip flops on microprocessors. These data are used to help define appropriate error detection and correction in microprocessor designs.

This paper presents some of the trends and lessons learned from our accelerated test experiments over the past ten years, ranging from 250nm through 28nm technology nodes. In particular, we describe how the test results are used to influence microprocessor design. Our results show that:

- The SEU rate for individual SRAM cells increased at a 40nm feature size compared to a 65nm feature size. This reverses a long-term trend of SEU rate decline with technology scaling that had been true from the 250nm node to the 65nm node. In the past, the reduction in critical charge caused by declining power supply voltage has been more than offset by cell area reduction and technology improvement, but this no longer appears to be true for SRAMs. However, there is still a reduction in latch/flop SEU when moving from 65nm to 40nm to 28nm, which may be caused by flops being larger than SRAMS and/or by flop design having a big impact on SEU sensitivity.
- Flop SEU rate increases significantly as Vdd decreases due to the reduction in critical charge of the storage nodes. The SEU rate approximately doubles when dropping from 1.25V to 0.7V and doubles again when dropping from 0.7V to 0.5V. This result implies that dynamic voltage frequency scaling (DVFS), a commonly used microprocessor energy reduction technique, could cause a significant decrease in microprocessor reliability.
- Flop SEU rates do not seem to vary much with new circuit designs that trade off device speed with leakage current, hence improving energy-efficiency. The new designs usually involve back-bias transistors, in which a bias voltage is applied to the "back gate" or "body" terminal of a transistor - thus changing the effective threshold voltage of the device. However, forward bias does seem to decrease SEU rates at the 28nm node.
- Shrinking feature sizes have made multi-cell upsets more prominent, requiring that ECC be supplemented by appropriate spacing between bits belonging to the same logical word to minimize the system level effect of soft errors in microprocessor memory cells.
- Flop SEU rates are approximately the same as SRAM cell SEU rates for recent technology nodes. Flop SEU rates are expected to play a greater role in defining the system level soft error rates for future technologies.
- As feature sizes decrease, the apparent neutron beam attenuation due to the beam passing through a device and package material increases, perhaps because of greater sensitivity to lower energy neutrons. This limits the number of devices that can be simultaneously tested.

II. TEST SETUP

Accelerated testing is necessary to provide data for microprocessor designers because cell upset events due to neutrons are relatively rare events in a terrestrial environment. Although neutron flux is higher at higher altitudes and we have performed testing at high altitudes with hundreds of units in the past, we have found that a neutron beam is the most practical

way to get sufficient neutron flux rates for accelerated testing. The LANSCE facility at Los Alamos [1] provides an energy distribution very close to the cosmic neutron flux at the earth's surface at approximately 10^8 times the intensity, and we have performed neutron beam testing at that facility once or twice every year for the past ten years.

Our test methodology is fairly standard for beam testing. We begin by initializing memory and logic to a known state, turn on the beam, and monitor errors while the beam is on. We generally initialize to all zeros for symmetric memory cells but have also experimented with checkerboard patterns. For SRAM cells, we sweep through memory while the beam is on and record the location and time (to within one sweep) of bit flips. For flops we only check for bit flips at the end of the test because the number of flops on a microprocessor is small compared to the number of memory cells, meaning that the total number of logic cell errors is relatively small compared to the total number of memory cell errors.

After the test, we analyze the data to determine the number of single and multi-cell upset events. We use time and spatial correlation to determine if a single neutron has upset multiple SRAM cells. If, during a single sweep through memory, we record bit flips for cells within a few microns of each other, we consider those events as multi-cell upset events. Otherwise, we consider them as single cell upset events.

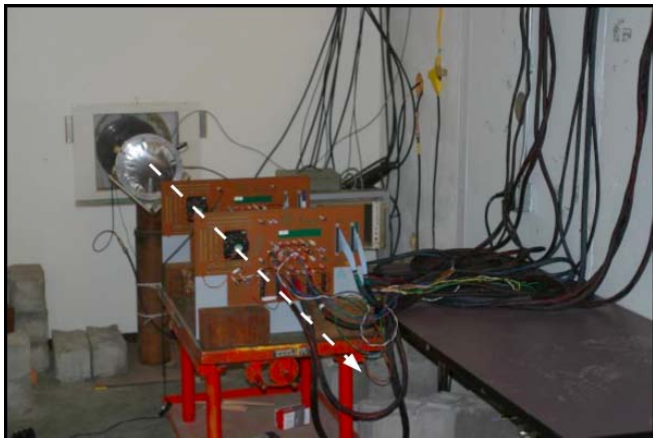

Figure 1. Test setup using a special tester [12]

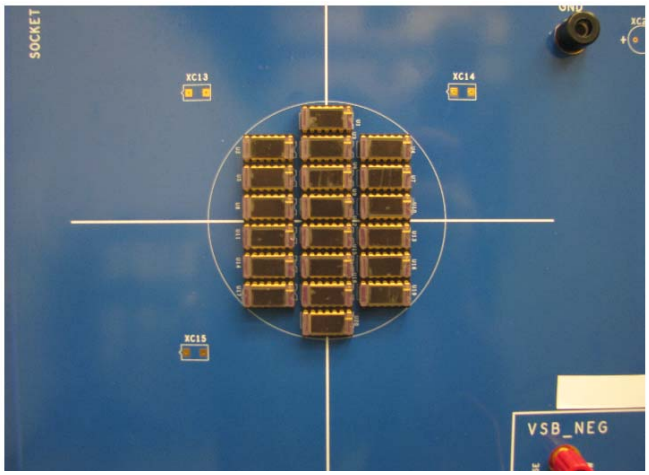

Figure 2. Test board containing 40nm test chips

Figure 1 shows our test setup. The beam direction is shown by the arrow as it travels through the neutron counter and two microprocessor boards. We use a portable tester [12], not shown in Fig. 1, for neutron beam testing (see [2] for the benefits of using this approach instead of testing complete systems). We test both microprocessors and specially designed test chips using the arrangement shown in Fig. 1. Using test chips allows us to test and compare various types of flops, as well as to vary voltages and other parameters. An example of a board with 20 test chips is shown in Fig. 2. The beam diameter and distance to the beam are carefully selected so that the transmitted beam flux is approximately the same for all the test chips on the board. Each test chip for these latest experiments contains approximately 55,000 flops, so there are more than a millions flops on the test board. At the current time, we have 28nm results only for flop test chips.

As can be seen in Fig. 1, multiple microprocessors are placed in the neutron beam path. This allows us to gather more data in a single experiment as long as the neutron beam attenuation, caused by neutron absorption and the spreading of the beam cross-section with distance, is reasonable. We can measure the attenuation by analyzing the total number of upset events for each microprocessor position in the beam path. It has been observed that the attenuation has increased from about 10% per microprocessor position in 180nm to 40% per microprocessor position in 65nm technology. This has direct impact on the number of boards that can give meaningful results when placed in series in the neutron beam. In 180nm technology, we would place 4-5 boards with microprocessors in the beam path. In 65nm and smaller technology nodes, we only place 2 microprocessors or test boards in the beam path.

To further investigate the beam attenuation, the neutron energy spectrum was captured before and after the neutron beam passed through a single board. The beam radius was collimated to approximately 1 inch in diameter to ensure that the entire beam passed through the board material, package lid, and silicon die. Figure 3 shows the beam transmitted flux as a

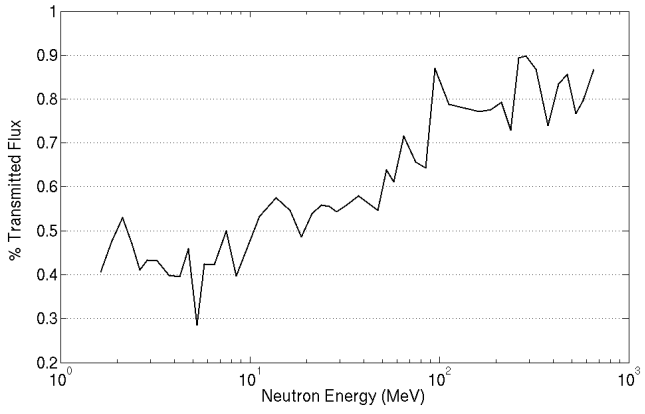

Figure 3. Neutron beam transmission spectrum through a circuit board and microprocessor

function of the neutron beam energy. Beam attenuation is the inverse of beam transmitted flux (attenuation = 1 – normalized transmitted flux). The apparent attenuation in Fig. 3 is due to absorption of neutrons by the circuit board and beam spreading. The data in Fig. 3 is noisy due to the narrow beam diameter required for this test and the limited test time that we were able to devote to it. However, it does show the correct trend for transmitted flux as a function of neutron energy. Lower energy neutrons are more attenuated (around 50%) than the higher energy neutrons (0-20%). The increase in attenuation as technology has scaled mentioned in the previous paragraph, together with the change in beam attenuation observed in the measurements, could be indicative of memories being more sensitive to lower energy neutrons as the technology has scaled. Due to the attenuation, it is important to compare the test results from each board independently to see if there are differences.

In all beam testing, it is important to avoid contaminating the data with secondary particles originating from neutron interactions on the first board and propagating to the second board. For all our beam testing, the spacing between the boards was 12 to 18 inches to allow the secondary particles to decay and disperse.

III. Technology Trend Test Results

Figure 4 shows the microprocessor SRAM single-event upset (SEU) rate and voltage as a function of the technology node, normalized to a value of 1 at the 90nm technology node for ease of comparison and to protect proprietary data. (SEU rate is reported in FITs/kbit, equivalent to cell upset events per bit per million hours.) The nominal power supply voltage (Vdd) has been slowly decreasing, which decreases the critical charge necessary for a cell upset event, thus making the cells more vulnerable to bit flips. However, cell size reduction and the corresponding sensitive area reduction with technology scaling has led to a reduction in SRAM cell SEU, even as the voltage has decreased, until the 40nm technology node. The large reduction in SRAM cell SEU rate from 130nm technology to 90nm technology was most likely the result of an SRAM design change. The layout of the SRAM cell changed from the traditional one to a lithographically friendly one with uni-directional poly orientation [3]. As a result, 90nm SRAMs have a significantly reduced amount of NMOS active area - over and above what just technology shrink would indicate, thus significantly reducing the sensitive area most contributing to SEUs.

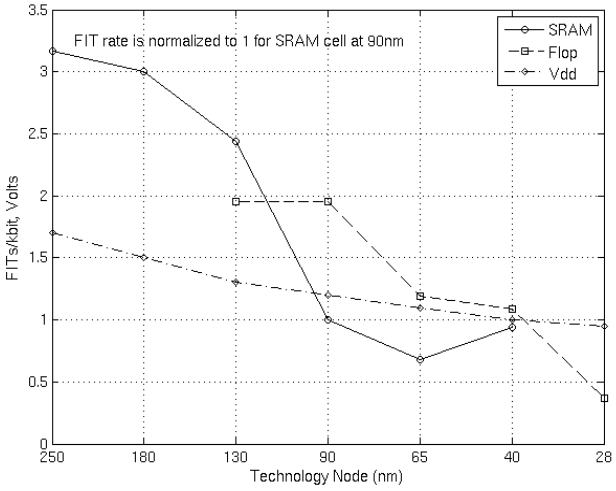

Figure 4. SRAM and Flop SEUs as a function of technology node

Because soft error susceptibility increases exponentially as voltage decreases and decreases linearly as area decrease (quadratically as feature size decreases), it has long been expected that the voltage reduction that has accompanied feature size reduction would eventually cause SEU rates to increase. Our data for 40nm SRAMs appear to be the first evidence of this affect. The 40nm SRAM SEU rate is 30% higher than the 65nm SRAM and nearly the same as the 90nm SRAM. One sigma error bars for SRAM FIT rate (not shown in Fig. 4) are less than 3%, so the results are not due to uncertainty. However, there was a foundry change between 65nm and 40nm that may have impacted the results. When we have data for 28nm SRAM SEU rates, we will be able to determine the relative contributions of the technology node and foundry changes.

Kobayashi et al [5] have recently published an analysis on how various particles generated in the nuclear reactions of neutron and silicon nuclei contribute to the final SEU rate of a 45nm SRAM. Their analysis indicates a sharp increase in SEU rate as a function of critical charge when the cell critical charge drops below than ~0.6fC. For cell critical charge less than 0.6fC, the contribution from protons (with average energy of ~5MeV for all interactions) becomes the dominant term. Since these relatively low energy particles are much more abundant than heavier ions like He, Al and Mg, this may explain the sharp increase in SEU rate. This sharp increase in SEU rate as a function of critical charge has been noted by others as well [6] [10]. Another recent result [7] adds more evidence to the SRAM cells being sensitive to low energy particles. In Section II, we reported on the change in apparent beam transmission while stacking and testing multiple boards in the neutron beam. Our results indicate that SRAM cells are becoming more sensitive to reaction products from low energy neutrons as they are being scaled in each technology node. However, SEU rate depends on the balance of critical charge and critical volume, and other authors [11] predict that SRAM cell SEU rate will continue to decline to the 22nm technology node, so our results may not be generic.

Figure 4 also shows how flop SEU rates compare to SRAM SEU rates as a function of technology. Flop data presented here is averaged over all the different drive strengths and different flop design families in the product. Flop data also has higher error bars because the total number of flops is smaller compared to the total number of memory cells on the same die. As shown in Fig. 4, the SEU rate for flops in 130nm product is similar to flops in 90nm product, while flops in 65nm product show a reduction in SEU rate.

Unlike SRAMs, flops in 40nm technology show a reduction in SEU rate compared to 65nm, although not as big a reduction as predicted by our simulations [4]. Flops in 28nm technology show a significant reduction in SEU rate compared to 40nm.

One reason that the trend may not yet have appeared in the flop data is that flops are bigger than SRAMs, so the sensitive area reduction may have more relative importance. However, it should be noted that due to the special treatment by fabs, SRAM cells get close to the expected area shrink entitled by the feature size reduction. Flops don't enjoy the same treatment, and hence, the sensitive area reduction for flops is more modest. Another contributing factor to the flop trend is that flop design style plays a big role in determining the flop SEU rate. Due to the manufacturing and design dependencies, some difference can be expected in the SEU rate versus technology trend for memory cells and flops. This will be especially true when comparing trend results from different vendors.

In the past, designers have not been greatly concerned about soft errors in microprocessor logic because the number of flops/latches on a microprocessor is much fewer than the number of SRAM cells, and flop SEU rates were lower than SRAM SEU rates. In 90nm, 65nm, and 40nm technology, flop SEU rates are larger than SRAM SEU rates. Because flop protection mechanisms such as state machine encoding and invariant checking are more difficult to implement than simple parity and ECC, flops are quickly becoming the major contributor to system soft error rate as technology scales to smaller feature sizes.

While SEU rates per memory cell have been decreasing, the amount of memory on a microprocessor has been increasing. Table 1 shows the raw SEU rate per microprocessor as a function of the technology node for representative microprocessors built in that technology. The example microprocessor in 180nm was a simple die shrink of the 250nm microprocessor, so the amount of memory did not change. However, for later technology generations, the amount of on-chip microprocessor SRAM has been significantly increased to create larger caches and improve performance. Due to the larger caches, the total uncorrected SEU rate per microprocessor has increased with technology generation even though the SEU rate per bit has decreased. The uncorrected rates in Table 1 are input into error correction code (ECC) design to determine the appropriate protection for each memory structure. With ECC, the corrected memory array failure rate on a microprocessor is orders of magnitude smaller than the numbers in Table 1.

Table 1 also shows how the microprocessor designs have evolved over the years. Early designs were done in a way to ease production in the next technology generation via optical scaling when moving from the 250nm node to the 180nm node. This was abandoned in favor of using additional silicon real estate on the scaled chip for multiple copies of the device when moving from the 180nm to the 130nm node. Technological complexity also dictated that porting a design to the next node was no longer a relatively simple optical process but required significant engineering resources. Larger cache sizes were deemed necessary to bridge the widening speed gap between microprocessor and memory I/O. This explains the almost 10x increase in memory capacity when moving from 130nm to 90nm node. The next node (65nm) was the first multi-core architecture with high-speed serial I/O links and shared level-2 caches and hence shows only a modest increase in the total number of bits. The current node (40nm) continues the trend in multi-core architecture with extra chip real estate being used to increase on-chip memory by close to 50% while doubling the number of cores on the die.

TABLE I. RAW SEU RATE PER MICROPROCESSOR

Tech. (nm)	***Relative SEU rate in FITs/kbit***	**Approx. Mbits per microprocessor**	**Relative uncorrected SEU rate per microprocessor (kFIT)**
250	3.2	1.52	5.0
180	3.0	1.52	4.3
130	2.4	3.28	7.9
90	1.0	33.6	33.6
65	0.7	44.3	30.5
40	0.94	71.0	67.0

IV. VOLTAGE TEST RESULTS

As shown in Fig. 5 for the 40nm technology node, the average flop SEU rate increases significantly as Vdd decreases. This is expected because the critical charge decreases linearly as Vdd decreases and SEU rate has an exponential dependence on critical charge. The SEU rate increases by approximately 30% per 0.1V as the voltage decreases from 1.25V to 0.5V as shown by the exponential fit in Fig. 5. The error bars in this paper indicate +/- 1 standard deviation range around the average value. The SEU rate approximately doubles when the voltage decreases from 0.7V to 0.5V. The 28nm technology node is also shown in Fig. 5 and indicates the same trend, albeit with fewer data points. Note that the data in figures 5, 6, and 7 is normalized to a SEU rate of 1 for the 40nm node data at 0.95V for ease of trend comparison and to protect proprietary data.

Because the dynamic power consumption of transistors is proportional to V^2F, where V is the voltage (usually Vdd) and F is the frequency, microprocessor designers would like to reduce Vdd as much as possible to make the microprocessor more energy-efficient. These test results provide an indication of the SEU rate impact of that Vdd reduction.

Dynamic voltage frequency scaling (DVFS) is the (usually simultaneous) reduction of both voltage and frequency to reduce microprocessor power consumption. Many modern microprocessors use this technique to reduce power consumption during periods of light utilization or during periods when external conditions require that the system reduce its power consumption. If the microprocessor is idle while the voltage is reduced, the increase in flop SEU rate may not matter, but if the microprocessor is operating at a reduced rate, the increase in flop SEU rate may negatively impact reliability based on our test results.

Figure 6 shows the trend of SEU rate increasing as voltage decreases for four different flop design topologies: master slave, dynamic [8] and two different flavors of sense amplifier based flops [9]. As shown in the figure, all flops show similar

trends for SER as a function of supply voltage. While this is true for these particular flop designs tested, it should not be taken for granted for all designs. A counterexample is shown in Fig. 7, where a different master slave design on our 40nm test chip shows a very different slope for SER as a function of supply voltage. The second master slave flop shows 2.3x more sensitivity to voltage compared to first – its SEU rate increases ~3x for each 100mV drop in supply voltage. Please note that our data for the second master slave flop has large error bars at higher voltages but the difference in slope and its higher SEU rate at lower voltages is clearly visible. Its higher SEU rate at 0.86V compared to 0.73V is believed to be an artifact of these large error bars.

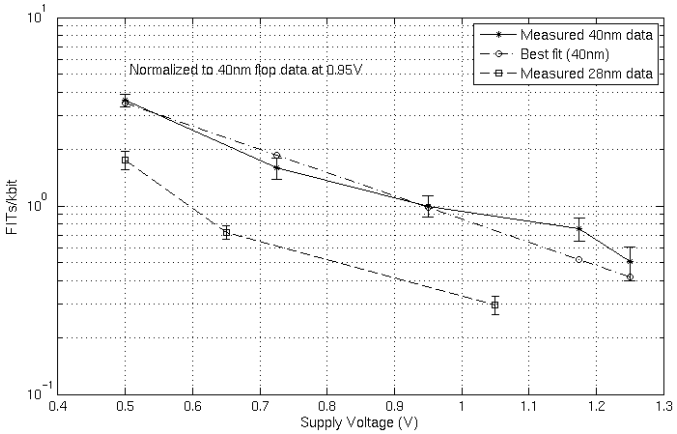

Figure 5. Flop SEU rates as a function of Vdd

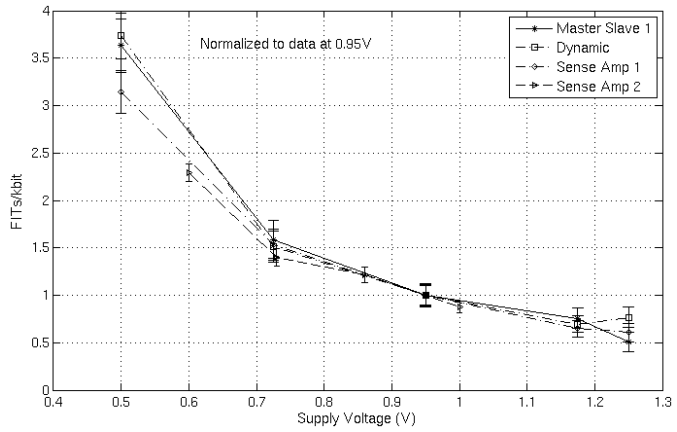

Figure 6. SEU rates as a function of VDD for various flops
Note that all flop families show similar trends.

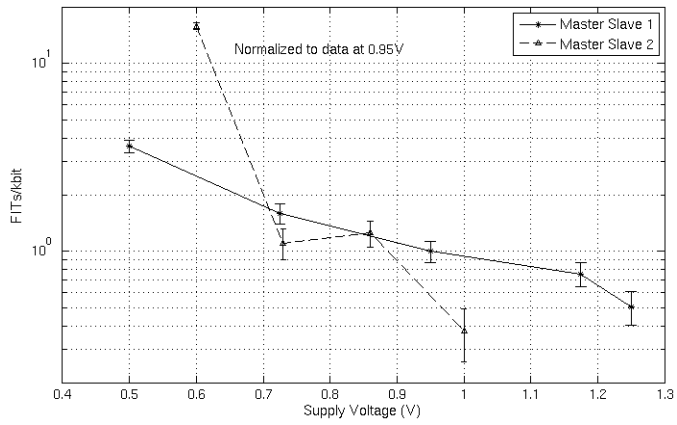

Figure 7. SEU rates for two different master slave flops on 40nm test chip
Note the very different slopes for the two designs.

Clearly, for designs using DVFS, comprehending such differences in SEU sensitivity is of great importance. It would be highly desirable to exclude extremely sensitive flops from the design. The master slave flops in Fig. 7 are different circuit designs and follow different layout styles. Master Slave 1 follows all DFM (Design For Manufacturing) guidelines with only straight poly while Master Slave 2 uses the minimum design rules and allows for poly bends in order to reduce the circuit area as much as possible. For SEU sensitivity reduction in this application, the Master Slave 1 design approach would be preferred.

To reduce microprocessor power consumption, designers are creating more energy-efficient circuits. One example is the use of back-bias transistors, in which a bias voltage is applied to the "back gate" or the "body" terminal of a transistor. This can be used to increase the effective threshold voltage of an extremely leaky device, thus reducing leakage current and making the device usable in a system that would have otherwise rejected it due to power consumption. Back bias can also be used to reduce the threshold voltages of the devices. A reduction in threshold voltage increases the operating speed of the device and allows it to be used in a system for which it originally would have been too slow at the cost of added leakage current as noted above. SEU rate implications as a function of both forward bias and reverse bias for the complementary NMOS and PMOS transistors need to be understood before this scheme can be qualified for field usage.

For an NMOS transistor, the substrate voltage (Vsb) or the p-well voltage can be varied, and for a PMOS transistor, the n-well voltage (Vnw) can be varied. Changing the back bias (Vsb or Vnw) affects both the charge collection volume and the feedback dynamics of the storage nodes. Forward bias (+Vsb, -Vnw) reduces the charge collection area due to lower applied voltage across the p-n junction area and increases feedback speed, while reverse bias has the opposite effect. Table II shows the results of varying the substrate voltage (Vsb) and the n-well voltage (Vnw) for a flop on a 65nm test chip. Typical operating ranges of interest are +/-300mV. No statistically significant trend in SEU rate as a function of bias is evident even when testing up to +/-500mV, well beyond the expected range. All measured results are within 10% of nominal. This indicates that SEU rate is insensitive to this transistor energy-reduction technique in these circuits. The circuits tested are twin well circuits manufactured in a triple-well capable process.

TABLE II. NORMALIZED FLOP SEU RATE FOR DIFFERENT TRANSISTOR BIAS VOLTAGE FOR 65NM PARTS

Vnw	Vsb = +0.5V	Vsb = 0V	Vsb = -0.5V
	Part A, 65nm, Vdd = 1.0V		
1.5	1.50	1.35	1.36
1	1.47	1.37	1.43
0.7	1.42	1.35	1.25
	Part B, 65nm, Vdd = 1.2V		
1.7	1.11	1.04	1.15
1.2	1.15	1.06	1.1
0.9	1.13	1.1	1.14

Values are FITs/kbits, normalized to a value of 1 for 90nm technology and 1.2V Vdd.

Vsb is the substrate voltage, and Vnw is the n-well voltage. Forward/reverse bias is +/-500mV for Vsb and -300/+500mV for Vnw.

TABLE III. NORMALIZED FLOP SEU RATE FOR DIFFERENT TRANSISTOR BIAS VOLTAGE FOR 40NM AND 28NM PARTS

Vnw	Vsb = +0.3V	Vsb = 0V	Vsb = -0.3V
	Part C, 40nm, Vdd = 1.0V		
1.3	1.10	-	1.23
1	-	1.09	-
0.7	0.96	-	1.22
	Part D, 28nm, Vdd = 0.65V		
0.95	0.96	-	1.02
0.65	-	0.80	-
0.35	0.77	-	0.95

Values are FITs/kbits, normalized to a value of 1 for 90nm technology and 1.2V Vdd.

Vsb is the substrate voltage, and Vnw is the n-well voltage. Forward/reverse bias is +/-300mV for Vsb and -/+300mV for Vnw.

Table III shows the results of varying Vsb and Vnw for flops on a 40nm test chip and a 28nm test chip. Due to lack of test time, data was only gathered for the corner cases in the table. Although some evidence of SEU rate reduction with forward bias (+Vsb, -Vnw) appears, the trend is minimal and not statistically significant. Note that testing was done with a nominal Vdd of 0.65V for the 28nm test chip in an attempt to accelerate the results.

V. MULTI-CELL UPSETS – DESIGN IMPLICATIONS

As shown in Fig. 8, SRAM multi-cell upsets are much more common in newer technology nodes, and microprocessor designs need to protect against them. Standard ECC can detect up to two bit errors per word and correct one, but the prevalence of single neutron events that upset 3 or more bits means that designers need to appropriately physically separate bits that appear in the same protected word.

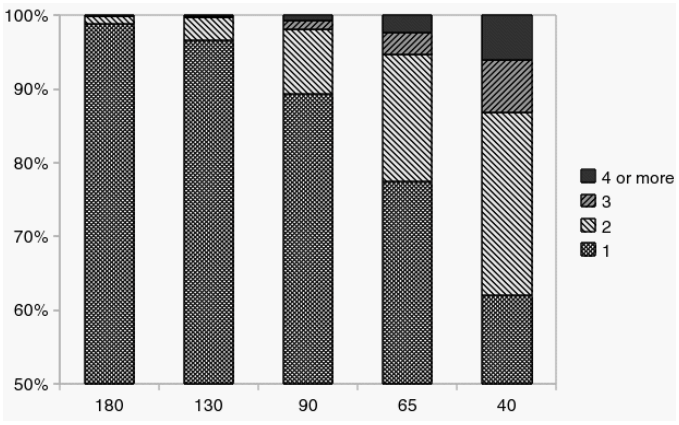

Figure 8. Multi-cell error percentages by technology node

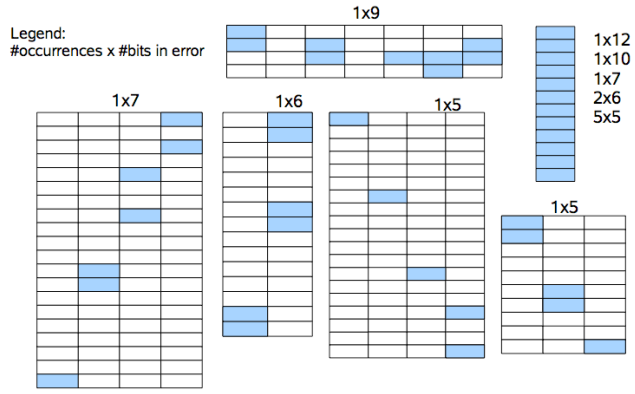

Figure 9. Multi-cell upset patterns

Multi-cell upset events that impact different rows of an array are not a concern because a single word only uses cells in the same row. The concern is a multi-cell upset event that flips multiple bits in the same row. Many of the double, triple, and quadruple cell upset events are exactly of this nature. From our study of these event patterns, bits in the same word must be separated by a number of cells to avoid multi-cell upsets in the same word.

The cell upset patterns for the events that upset 5 or more cells are a bit more complex and problematic as shown in Fig. 9. These events come from a recent experiment that obtained over 36,000 SEUs from a 90nm part. Fig. 9 shows the number of occurrences for each pattern and the number of bits in the pattern. The "1x9" pattern at the top middle of Fig. 9 means that there was one event that upset 9 cells. It was spread over 4 rows and 7 columns as shown in the figure. Similarly, the "1x7" pattern on the left was one event that upset 7 cells, spread over 4 rows and 20 columns. The "1x7" event was about the maximum cell separation we would consider as a single event; events with larger separation would be considered as separate upsets (recall that an event is recorded during a single sweep through memory, so the upsets are correlated in time as well as space). There were a number of events indicated on the top right of Fig. 9 that impacted several rows in a

column, but these are not an obvious concern for a design because each upset would be in a different word.

However, cell upsets events are spatially random. In the "1x7" pattern, it appears as though a charged particle traveled from the top right corner to the bottom left (or vice versa), leaving a trail of cell upsets in its wake. In the "1x5" pattern, it appears that the trail was upper left to lower right or vice versa. In either of these events, there is no reason the charged particle could not have travelled along a row rather than diagonally. The SRAM cell size in Fig. 9 is 2.1 microns by 0.7 microns. The maximum distance between cells upset in a multi-cell upset event is 16 microns from corner to corner in the "1x7" event. Thus, if a designer wanted to protect against the worst possible event, they would protect against events that were 16 microns or 8 cells apart in the same row. For example, if simple parity is used for protection, bits in the same word should be separated by at least 8 cells in order to guard against such errors. In other words, there needs to be at least a 9-word interleave in each row or a design rule that states that cells in the same word must be on at least an 18 micron center-to-center pitch.

The approach described in the previous paragraph is very conservative. It assumes the worst case multi-cell upset event at the worst case geometry. A more reasonable approach is to compare the protection mechanisms against the upset data to determine the probability of an event that would defeat the protection. For example, if double error detection, single error correction ECC is used with a 2-word interleave, there would have to be 3 upsets within 5 cells in a row to cause an undetectable error. This occurs once in 36,000 events - in the third row of the "1x9" configuration. With an event rate of around 30 kFITs per Table 1, this is an undetected error rate of 1 FIT, something that the microprocessor designers may decide is acceptable. It is also possible to create a probability vs. distance distribution using the test data and do a more conservative calculation by assuming worst-case geometry for the multi-cell upset events.

VI. Conclusion

The Oracle design teams have found the accelerated test data from our experimentation at LANSCE to be very valuable. We have used them to guide error detection and correction in our microprocessor designs. Our data shows trends that will make system error protection even more important:

- SEU rates per SRAM cell have reversed a long-term trend and show an increase at the 40nm technology nodes. Data from the 28nm node is needed to confirm the trend.
- SEU rates per flop continue to show an improvement trend, although a trend reversal is expected in the next few technology nodes. Flop design and manufacturing appears to be more important factors for SEU rate than charge collection volume reduction and increased voltage sensitivity.
- Multi-cell upsets have become much more frequent due to shrinking feature sizes. Designers of memory structures on microprocessors need to consider multi-cell upset protection techniques.
- Microprocessor energy reduction techniques can negatively impact SEU rate, e.g., reducing Vdd to reduce energy consumption.
- The use of back-bias transistors to improve energy-efficiency does not seem to significantly impact SEU rate.

We intend to continue our accelerated test program to track these trends and guide our microprocessor design.

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