Selective Hardening Methodology for Combinational Logic

Samuel N. Pagliarini, Lirida A. de B. Naviner and Jean-François Naviner
Institut TELECOM, TELECOM-ParisTech, LTCI-CNRS
46, rue Barrault, 75634 - Paris Cedex 13, France
E-mail: {samuel.pagliarini, lirida.naviner, jean-francois.naviner}@telecom-paristech.fr

***Abstract*—Defects as well as soft errors are a growing concern in micro and nanoelectronics. Multiple faults induced by single event effects are expected to be seen more often. Thus, reliability has become an important design criterion. In this context we introduce a cost-aware methodology for selective hardening of combinational logic cells. The methodology is based on the SPRA algorithm for calculating logical masking, and it is capable to automatically perform a trade-off between reliability improvements and associated costs, providing a list of the most effective candidates for hardening. The methodology is applied to a set of benchmark circuits using costs extracted from an actual standard cell library. The results then show that the methodology is able to diminish the unreliability of circuits in a cost-effective manner.**

***Index Terms*—Reliability, Single Event Effects, Selective Hardening, Logic Masking.**

I. Introduction

The amount of defects as well as the number of soft errors (i.e., transient errors) in electronic circuits are expected to increase, becoming a major concern in current and future technologies [1]. Thus, there is a current trend in the design of these circuits in which reliability related criterion are more and more common in the design flows.

Transient errors have many different sources. The transient faults that originate the errors can be caused by different physical phenomena, such as high-energy particle hits originating from cosmic rays, capacitive coupling, electromagnetic interference, or power transients [2]. Transient errors induced by the strikes of energetic particles at the devices are of great concern, specially for dependable systems and circuits [1, 3]. In the past, transient errors used to be a concern only in the design of memories, thus resulting in the now widely used error correcting codes and other mitigation techniques such as nodal interleaving. On the other hand, at 90 nm and beyond, the reduced dimensions of the devices and also reduced operating voltage levels lead to more common radiation-induced faults in logic, with resulting error rates approaching those of memories [4, 5].

Therefore, transient errors in logic circuits are becoming an important reliability concern for current and future technology. Furthermore, the critical charge and the distance between sensitive junctions are decreasing with scaling. Thus, the energy of radiation particles that is required to cause multiple transient faults is also decreasing. The probability that a single high energetic particle affects the output of more than one circuit node, causing multiple faults, is no longer negligible [6].

On the ocasion of a transient fault, one or multiple electrical pulses may be created. These pulses, typically current spikes, are able to change the current output value of a node from one to zero or vice-versa. Yet, not all transients are able to reach the outputs of the combinational logic since there are natural masking properties against transient errors. These are:

- *Electrical masking*, which accounts for the attenuation of the current pulses as they propagate through the logic.
- *Temporal masking*, or latch-window masking, which defines a time interval in which the transients that reach the memory elements of the circuit will or will not be registered.
- *Logical masking*, which accounts for the lack of sensitized paths (from the erroneous node) to a primary output or memory element.

Among the masking phenomena that render immunity to combinational logic circuits from soft errors, logical masking is the hardest to model and characterize [7]. Also, logical masking is technology-independent. Thus, in this work we focus on calculating the reliability of a circuit considering only the logical masking. The other masking properties can be interpreted as derating factors, i.e., by calculating only the logical masking we are providing a underestimate of the actual circuit reliability. Electrical and latching-window masking computations may actually filter out some of the errors that logical masking does not filter.

Hardening techniques are applied in order to mitigate transient errors. Traditional hardening consumes too much area and/or energy to be cost-effective in commercial applications. Selective hardening, applied only to a design's most error-sensitive parts, offers an attractive alternative [8, 9]. Thus, considering logical masking, the main idea is to classify the composing blocks (i.e., standard cells) of a circuit according to their relative significance with respect to the reliability of the circuit. With the classified list of blocks it is possible to apply selective hardening either by using hardening by design techniques or by more generic fault tolerance techniques like Triple Modular Redundancy (TMR). By using an additional hardening affinity parameter, a trade-off between the hardening cost of a block and the reliability gain is then clearly stablished.

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A. Related work

In [9] we have studied the same problem of selective hardening but considering only single faults and by applying a different simulation/emulation model for obtaining the reliability figures. Such reliability methodology is referred as Probabilistic Binomial Reliability (PBR) [10]. The main drawback of the PBR methodology is the need for fault simulation or fault emulation, tasks that are inherently time consuming.

In [11] the authors have described a very similar approach for selective hardening. They have chosen an algorithm with linear complexity and accept the fact that innacurate values will be used for estimating the relative reliability gains of hardening a given cell in a circuit. We have used the same premise in our work. Yet, they are only concerned with single faults. Also, they propose a cost target such that the number of hardened cells does not exceed a cost limit *L*. All nodes have the same weight if this hypothesis is used while in our approach each type of node has a different cost. For instance, it is quite less costy to triplicate an inverter than to triplicate an or gate with several inputs.

B. Contribution

Our contribution is to provide an efficient methodology for selective hardening of the most critical blocks of a digital circuit. This methodology takes into account the effects of multiple faults since these are more prone to happen nowadays. Our methodology is also scalable since it relies in an algorithm with linear complexity to calculate the logical masking effect. A parameter similar to a hardening cost is also introduced, which allows the designer to drive the methodology using accurate cost values for the hardening of each block.

C. Overview

This paper is organized as follows: Section II contains the basic definitions used by our reliability estimation method. Section III describes the steps used to build the methodology to classify the blocks. It also contains a comparison among an accurate reliability estimation method and the approach we have used. Finnaly, in Section IV we have applied the proposed methodology in a series of circuits of different types, while in Section V we present our final remarks.

II. Preliminaries

The reliability of a given circuit is the degree of confidence observed in the outputs of this circuit, given a certain scenario in which faults are expected to occur with a given probability. In this work we obtain the reliability figures of a circuit by applying the Signal Probability Reliability Analysis (SPRA) algorithm [12]. Based on a straightforward signal reliability computation and propagation algorithm, SPRA allows the evaluation of the logical masking capability of combinational logic circuits. Let us then define signal reliability.

A. Signal reliability

We consider the *signal reliability* of a given signal as the probability that this signal carries a correct value [12]. So, it is assumed that a binary signal x can also carry incorrect information. This results in the fact that x can take four different values: correct zero (0_c), correct one (1_c), incorrect zero (0_i) and incorrect one (1_i). Then, the probabilities for occurrence of each one of these four values are represented in matrices, as shown bellow:

$$\begin{bmatrix} P(x=0_c) & P(x=1_i) \\ P(x=0_i) & P(x=1_c) \end{bmatrix} = \begin{bmatrix} x_0 & x_1 \\ x_2 & x_3 \end{bmatrix} \quad (1)$$

The signal reliability for x, noted R_x, comes directly from expression (2), where $P(.)$ stands for the probability function:

$$R_x = P(x=0_c) + P(x=1_c) = x_0 + x_3 \quad (2)$$

B. Reliability of a block

Digital circuits are composed of many connected blocks, typically standard cells. Let us consider one of these blocks which performs a function on a signal x in order to produce a signal y, i.e., y is the output of the block. The probability that this block fails is given by p, such that ($0 \leq p \leq 1$). Thus, $q = (1-p)$ is the probability it works properly. We can obtain the reliability of the signal y as:

$$R_y = (x_0 + x_3).q + (x_1 + x_2).p \quad (3)$$

Equation (3) shows that, when the input signal is reliable, the output signal reliability is given by q. This implies that for fault-free inputs, the reliability of the output signal is given by the inherent reliability of the block that produces this signal. More complex scenarios are evaluated by also taking into account the truth table of the logic blocks.

SPRA uses both the reliability of the blocks as well as signal reliability to determine the cumulative effect of multiple simultaneous faults in the reliability of a circuit. To each signal in the circuit a signal reliability matrix is attributed. The propagation of these signals through the logic blocks is done by performing operations (tensoring and multiplying) in these matrices to calculate the actual reliability of the entire circuit. The basis for the SPRA algorithm comes from the Probabilistic Transfer Matrices algorithm (PTM) [13, 14]. The main difference is that the PTM approach does not scale well, while the SPRA approach has a linear complexity.

III. Selective Hardening Methodology

The reliability of a circuit consisting of several blocks depends on the reliabilities of these individual blocks. This is shown in equation (4) for a circuit consisting of K blocks, where R is the circuit's reliability and q_i, q_j stand for the reliabilities of the blocks b_i, b_j respectively ($1 \leq i, j \leq K$).

$$R = f(q_1, q_2, ...q_i, ...q_j, ...q_K) \quad (4)$$

Assume that the blocks are independent in the sense that changing the reliability of a given block b_i has no impact on the reliability of another block b_j with $i \neq j$.

If we consider that a reliability change of a single block b_i brings in its new reliability q_i^*, the circuit's reliability becomes R_i^*. Because different blocks b_i and b_j make different contributions to the reliability of a circuit, changes of different blocks may produce different values R_i^* and R_j^* [9].

In our methodology we assume that there is a hardening technique that is able to improve the reliability of a given block b_i, such that $q_i^* = 1$. This is not a restriction, it is just a simplification, other values are also possible. Then, for all blocks of the circuit we perform an evaluation run of the SPRA algorithm. In each evaluation run we select a node b_i, allow q_i^* to be 1, and obtain the new reliability value R_i^*. This effort is possible since the complexity of the SPRA algorithm is linear.

After all initial evaluation runs are performed, we obtain a list of all R_i^* values. At this point, one could sort the list and elect the block with the highest R_i^* to be hardened. This is the approach followed in [9]. Yet, we are interested in stablishing a trade-off between the cost of hardening this block against the cost of hardening any other block. In order to do so, we introduce a new parameter to express the hardening affinity of such block, given by Ha_i.

The parameter Ha_i of each type of cell is defined by the user. It must be constrained in the interval [0,1]. This parameter is generic and can be used to express any type of hardening trade-off: area, delay, power or combinations of the previous.

It can also be used to model other situation of particular interest: assume that a certain cell is available in two versions in the same standard cell library, let us say INV_t and INV_h. The former is a traditional design while the latter is a hardened by design version of an inverter. Assume that the hardening by design, once is already done, has no additional cost to be implemented. Thus, to model this situation one should say that this particular cell has the highest hardening affinity, i.e., the Ha_i of INV_h is 1. Since the other types of cells have no hardened versions available, they will require a technique such as TMR to be applied. This technique is expected to have a larger cost and therefore any cell requiring TMR will have a $Ha_i < 1$.

In Tab. I we show the values that were used in our experiments for some cells. These values are extracted from an actual 90nm standard cell library provided by Synopsys [15]. In our analysis we considered that only the dynamic power of the blocks would be considered to calculate the hardening affinity. So, for each cell in the library, we have divided the dynamic power of the smallest inverter in the library by the given cell actual dynamic power. It is possible to notice that negated cells (like NOR and NAND) benefit from the CMOS natural inversion and have a higher hardening affinity. It is also possible to notice that inverters have the smallest dynamic power of all cells. All the other Ha_i values are normalized.

After each cell's affinity is known it is necessary to apply this value to decide wich block should be selected for hardening. This step of the methodology introduces a new value, the reliability gain or reliability difference, given by Rg_i. This is the difference from the circuit reliability before and after a single block was hardened. For each evaluation run this value is calculated as follows:

TABLE I: Hardware affinity (Ha_i) parameters for several blocks.

Block	**Power** (nW/MHz)	**Hardening affinity**
INVX0	10	1
NAND2X0	3583	0.002790957
NOR2X0	4211	0.002374733
AND2X1	6545	0.001527884
OR2X1	6859	0.001457938
OR4X1	7698	0.001299039
MUX21X1	8639	0.001157541
XOR2X1	8702	0.001149161
AOI21X1	13912	0.000718804

$$Rg_i = R_i^* - R \quad (5)$$

The value of (5) is then used to calculate the reliability-affinity product as follows:

$$Prh_i = Rg_i^{w1} \times Ha_i^{w2} \quad (6)$$

where $w1$ and $w2$ are the weigths to be applied. I.e., the user may choose if reliability should be more important than power or vice-versa, and by which amount. In the experiments that are presented in Section IV, these values were set as $w1 = 2$ and $w2 = 1$.

Once the value of (6) has been calculated for all cells, these are sorted and the highest value is picked. This block is then assumed to be hardened and the new circuit reliability (R_i^*) is obtained. This reliability is then compared against a user-given reliability target. If it is lower than the target the methodology algorithm starts again and all cells still not hardened are considered as candidates. Otherwise, if the target is met, the algorithm ends and outputs the ordered lists of cells to be hardened.

A. Comparison with an accurate reliability analysis algorithm

Our methodology uses the SPRA algorithm which is not accurate. The sources of inaccuracies come from incorrect evaluation of multiple fanout branches. An accurate analysis is possible using the multi-pass algorithm described in [12], here referred as SPRMP. It is well known that both algorithms produce different values for the reliability of a circuit. Yet, we are interested in comparing how well SPRA estimates the critical node in comparison with SPRMP.

Let us first consider a simple circuit, *c17*, which has only 6 nodes. By applying both algorithms just once, i.e., neglecting a reliability target given by the user, two lists of b_i nodes are

created. These lists are sorted according to the R_i^* of each node and are referred as L_b. These lists are showed in Tab. II.

The meaning of each column of Tab. II is as follows:

- **Position** is the ranking of the nodes according to R_i^*.
- **SPRMP's** L_b is the list of nodes generated by the SPRMP algorithm, i.e., the accurate list.
- **SPRA's** L_b is the list of nodes generated by the SPRA algorithm, i.e., the inaccurate list.
- **Position difference** is the difference in the ranking from column 3 with respect to column 2. E.g., block 4 is ranked first in the SPRA's L_b list while it is ranked second in the SPRMP's L_b list, thus the difference is 1 position.
- **Normalized difference** is the position difference divided by the maximum position error possible. In this example it is 5 since the circuit has 6 blocks.

According to the analysis of the circuit *c17* presented in Tab. II, the average error introduced by the SPRA algorithm is 13.3%. Yet, we have performed this same analysis for other circuits with different profiles, all containing multiple fanouts branches. The selected circuits are very limited in size since the execution time of the SPRMP algorithm is very high even for medium-sized circuits. The details of the chosen circuits are as follows:

- *74283*, a 4 bit adder.
- *AOI*, which contains an and-or-inverter logic and 2 multiple fanouts.
- *AOIX2*, which contains a larger and-or-inverter logic followed by a buffer network with many multiple fanouts.
- *decoder*, which contains a large or-like logic to decode 8 inputs. Each input feeds many gates so multiple fanouts appear already in the inputs.
- *chain*, which contains a chain of inverters and or gates.

Table III summarizes the comparison of all the presented circuits plus the already presented *c17* one.

The results in Tab. III clearly show that for some circuits both algorithms produce the same list of blocks to be hardened. Yet, for the circuits *c17*, *74283* and *AOIX2* the maximum error is quite high. A deeper analysis is performed for such circuits, where the error distribution is analysed.

The error distribution for the *74283* circuit is shown in Fig. 1, where the nodes in the **x** axis are sorted according to R_i^* (the actual labels are the ids of the blocks in the circuit).

TABLE II: Comparison of the SPRA and SPRMP algorithms.

Position	SPRMP's L_b	SPRA's L_b	Position difference	Normalized difference
1	2	4	1	0.2
2	4	5	1	0.2
3	5	2	2	0.4
4	1	1	0	0
5	0	0	0	0
6	3	3	0	0
			Average error:	0.133

TABLE III: Comparison of the methodology using the SPRA and SPRMP algorithms.

Circuit	Minimum error	Average error	Maximum error
c17	0	0.133	0.4
74283	0	0.07	0.28
AOI	0	0	0
AOIX2	0	0.35	0.85
decoder	0	0	0
chain	0	0	0

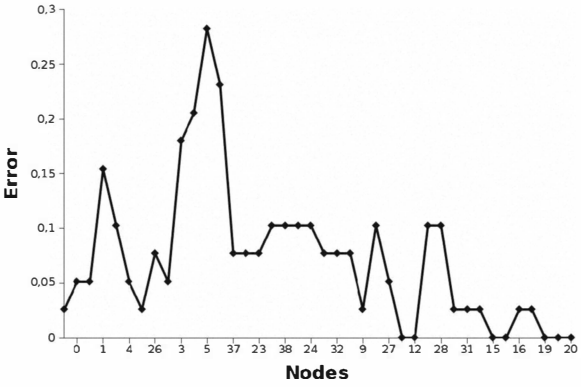

Fig. 1: Error distribution for the circuit *74283*.

It is possible to notice that some blocks have a higher error probability. Yet, that is not the case for the blocks that are closer to the **y** axis (which are exactly the best candidates for hardening). This same profile, where the error is not that high in the elected block, is also seen in the error distribution of the other circuits. The same profile is also observed after some cells have already been elected for hardening. Thus, our results are presented using the SPRA algorithm only.

In the particular case of the *AOIX2* circuit, the higher error values are due to the large number of multiple fanouts in the buffer network. Regarding the circuit *c17*, it only has 6 cells. So any small difference is very meaningful, even in relative terms.

IV. Experimental Results

The methodology described in Section III was applied to several ISCAS benchmark circuits [16]. Each block from each circuit was set using $q_i = 0.9999$. The reliability target was adjusted so a decrease of the unreliability would be reached for each circuit. The results are presented in tables IV and V. The former table contains the results for a reduction of at least 20% (w.r.t. the original unreliability) while the latter contains the results for a reduction of at least 40%. The original unreliability of each circuit is given in the second column of the aforementioned tables.

The column entitled "Original Power" contains the sum of the dynamic power of all cells of each circuit. The columns entitled "Hardened Cells" contain the amount of cells that

TABLE IV: Results for decreasing the unreliability by at least 20%.

Circuit	Original Unreliability	Original Power (nW/MHz)	No hardening affinity		With hardening affinity	
			Hardened cells	Power (nW/MHz)	Hardened cells	Power (nW/MHz)
c17	0.000562	21498	1	21498	1	21498
74283	0.003848	189244	4	222932	8	**189404**
c432	0.013466	624686	9	624866	9	624866
c499	0.013611	1321460	20	1669540	41	**1322280**
c1355	0.021905	1907300	38	2179608	38	2179608
c1908	0.031668	2146539	58	2147699	58	2147699
c3540	0.062635	5.90419e+06	54	5.90527e+06	54	5.90527e+06
c2670	0.064015	4.07731e+06	41	4.12503e+06	42	**4.08044e+06**
c5315	0.085614	8.89708e+06	59	8.96576e+06	60	**8.90057e+06**

TABLE V: Results for decreasing the unreliability by at least 40%.

Circuit	Original Unreliability	Original Power (nW/MHz)	No hardening affinity		With hardening affinity	
			Hardened cells	Power (nW/MHz)	Hardened cells	Power (nW/MHz)
c17	0.000562	21498	2	35830	2	35830
74283	0.003848	189244	10	273464	16	**189564**
c432	0.013466	624686	26	625206	26	625206
c499	0.013611	1.32146e+06	48	2.15685e+06	80	**1.42736e+06**
c1355	0.021905	1.90730e+06	83	2.50208e+06	83	2.50208e+06
c1908	0.031668	2.14653e+06	132	2.14918e+06	132	2.14918e+06
c3540	0.062635	5.90419e+06	175	5.90769e+06	175	5.90769e+06
c2670	0.064015	4.07731e+06	128	4.22630e+06	128	**4.08444e+06**
c5315	0.085614	8.89708e+06	205	9.13570e+06	207	**8.90465e+06**

are elected for hardening. By using the hardening affinity parameter this number tends to increase. Then, the columns entitled "Power" contain the sum of the dynamic power of all cells of the new version of the circuit. A fairly simple assumption was made: on hardening a given node we should add three times the value of the power of that node to the overall circuit power.

Thus the additional power that would be consumed by a voter is not considered. Once again, this is a simplification. A voter should be considered for a group of cells and not for a single cell, otherwise the costs can become unfeasible. Assuming one voter for each hardened cell would create a large cost both in terms of area and power. Therefore the power figures given in the tables are a minimum value estimate. Voter placement (i.e., TMR granularity) is not the scope of this work.

In tables IV and V some power figures are highlighted in bold. It is clear that applying the methodology considering the hardening affinity is an effective trade-off between power and reliability in these cases. This does not mean that the methodology is not appropriate for the other circuits. In fact, it means that the current choice of parameters $w1$ and $w2$ is not a good one for the circuits that are not highlighted.

A. Comparison

A straightforward comparison with other methodologies is not simple since the goals are different. The results presented in [9] are in alignment with the results presented in this work, which is a strong suggestion that multiple faults do not have a large impact on the decision of which node to harden. Yet, they have a considerable effect on the actual reliability of the circuit. Thus, they are important when determining the trade-offs between cost and reliability.

A radiation hardening technique for combinational logic is proposed in [17]. The hardening is achieved by increasing the gate size of some critical nodes in the circuit but no hardening against defects is mentioned. Thus the technique presented here is more of a general solution since it is technology-independent. The overheads mentioned in [17] are not directly comparable.

Nevertheless, in qualitative terms it is easily observed that certain cells have a larger impact in the reliability of the circuit than others. This observation is highlighted in [9, 11, 17]. In our exeperiments this was also observed. There are some particular cases, like the one illustrated in Fig. 2, where choosing the correct node to harden has a large impact in the overall circuit reliability. The analysis depicted in Fig. 2 is from the circuit *c1355*.

Regarding Fig. 2, it contains the R_i^* values related to the hardening of all possible cells. The nodes in the **x** axis are ordered by the reliability gain that hardening that node would produce. The circuit was evaluated given the parameter $q_i = 0.9999$ for each cell. In absolute terms the difference from the

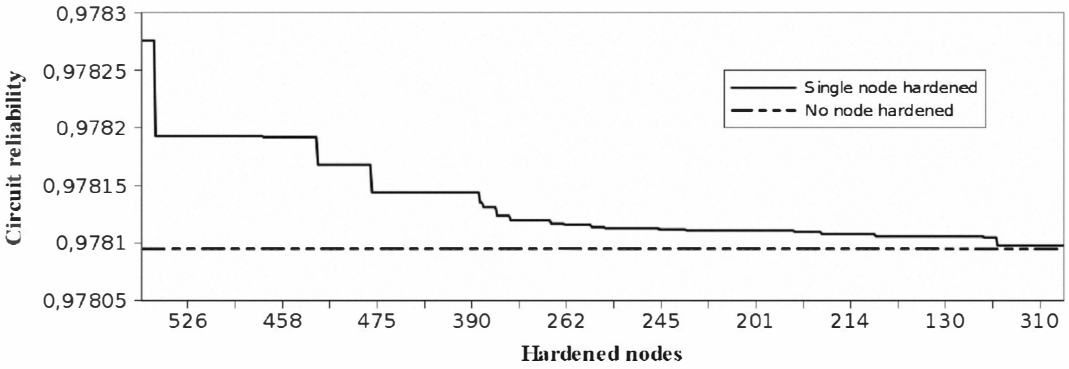

Fig. 2: Reliability gain versus chosen node to be hardened.

best to the worst candidate is not large. Yet, usually several cells are selected for hardening (as in Tab. V), so these values accumulate. Thus choosing the best candidate for hardening is critical.

V. Conclusion

In a context where defects and soft errors are a growing concern, we have proposed a selective hardening methodology for combinational logic nodes. Furthermore, we have also concerned multiple faults to determine the actual reliability of the circuits.

Our results present the use of the methodology in conjunction with a standard cell library from an actual vendor, where the trade-off between power and reliability gain is highlighted. Thus, the methodology can be integrated in commercial design flows in a very straightforward manner. Other cost-effective schemes are also possible since the methodology contains a generic parameter to define the hardening affinity of a node.

In our future works we plan to investigate the effects of multiple faults in the reliability of a circuit by limiting the effect of multiple faults locally in the circuit. The study of the relationship between parameters $w1$ and $w2$ is also a matter for a future work.

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