Comparison of Alpha-particle and Neutron-induced Combinational and Sequential Logic Error Rates at the 32nm Technology Node

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***Abstract*— We report on particle induced upset rates of combinational and sequential logic. A novel test chip has been designed in a 32nm process to study the effects of single event transients (SET) and to verify the accuracy of our simulation models. The test chip has been tested under neutron and alpha particle radiation. Our measured data verify simulation-based projections that while static logic at the 32nm technology node is sensitive to both alpha particle and neutron radiation, it is not a dominant contributor at the chip-level.**

Neutron; Alpha particle; combinational logic; single event effects; SEE; SET; single-event transient; soft errors, SE

I. INTRODUCTION

Radiation-induced upset rates in memory type devices such as SRAM and sequential devices are well understood and can be accurately predicted for terrestrial environments [1-9]. The radiation response of small devices has been successfully simulated using physical device simulators [4, 10, 11]. Circuit-level simulation tools are frequently applied for larger circuits where device or mixed mode simulations are not feasible [1].

A single event upset (SEU) of a memory cell is stable in time until the upset cell is re-written or the state is re-stored by a subsequent particle strike. An entirely different class of upsets is formed by so-called single event transients (SETs). SETs occur in combinational logic where the node voltage is always restored in the case of a particle strike. The amount of time it takes to restore the original state depends on the charge collection dynamics, the load capacitance and on the driver strength which all determine the width and amplitude of the radiation-induced voltage glitch. Combinational logic is different in that radiation induced glitches per se do not constitute single event upsets, but radiation-induced noise. However, if the glitch is captured by a receiving storage element it becomes a SEU. SETs can only be captured by storage elements if they are not masked by any of the following masking effects [12, 13]. 1) Electrical Masking: SETs are electrically attenuated before they reach the receiver, 2) Logical Masking: SETs propagation is blocked by a logic device and 3) Timing Masking: The propagated pulse at the combinational circuit output will not be captured by the storage element if it doesn't arrive during the data latching window of the receiving element. It is because of these masking effects, and in particular because of the high degree of electrical attenuation of SETs in older technologies, that combinational logic in data paths has not been a dominant soft error rate (SER) contributor in the past despite the vast numbers of combinatorial gates in products [14].

Shivakumar et al. predicted a nine orders of magnitude increase in SER per chip due to neutron strikes in combinational logic between 600nm and 50nm technologies [15]. At the 50nm node the authors projected that upsets in combinational logic are of equal or larger significance than upsets in sequential devices. In contrast, the authors of [16] concluded that combinational logic is not of a large significance at the 65nm node. The issue with both studies is that they are based on simulations rather than on measured data. Shivakumar et al. assumed a quadratic reduction in critical charge (Qcrit) of combinational logic nodes with scaling. Seifert et al's work questions the validity of these key assumptions in the presence of less aggressive clock frequency and voltage scaling [16]. Unfortunately, little experimental data have been published that could shed more light on whether combinational SER can be neglected for deep submicron technologies for terrestrial applications. One of the few experimental studies is the work by Gadlage et al. who designed test chips in a 180nm technology with a) different number of inverters in simple data paths, and b) either implemented hardened or unhardened latches to investigate the relative importance of combinational to sequential SER [17]. Their results show that under proton irradiation the combinational SER increases with clock frequency. Gadlage et al. found that at the highest investigated clock speed (300 MHz), the error rate due to strikes in the combinatorial logic equaled about 10% of the nominal unhardened flip flop (FF) SER. Narasimham has directly measured the SET temporal width distribution for static logic designed and manufactured in a 90nm and 130nm bulk CMOS process [18, 19]. The authors conclude that static combinational logic cannot be neglected for modern technologies, even for terrestrial applications. SETs widths are in general expected to increase with scaling [19]. This observation combined with the fact that with process scaling the logic gate switching speed of transistors increases indicates that the degree of electrical masking will decrease in future technologies[1]. Whether this translates into a significant increase in SER depends, however, on the scaling of critical charges to generate sufficiently wide SETs and whether decreasing strike cross-sections per gate will be able to compensate those trends.

Please note that in most circuit-level SER simulations reported in the literature ([15], [16]) voltage independent current sources are used, i.e., the current injection is independent of the node voltage. For large amounts of collected charge the electric field at the junction might collapse temporarily, however, and the effective current pulse and the voltage pulse widths can be much wider than when using independent current sources [20]. Recent investigations have shown

[1] Investigations by Baze and Buchner [14] provide the rule of thumb that pulses wider than the logic transition time will propagate through the gate without any significant attenuation.

that most neutron events in fact yield low amplitude and wide current pulses [3]. The question arises whether circuit-level simulations based on independent current sources are adequate to accurately predict soft error rates of devices in scaled modern technologies. It is well known that this is true for memory type [1]. However, the work by Mavis et al. indicates that SER simulations utilizing voltage independent current sources might yield optimistic results, at least for space environments.

The primary purpose of this work is to investigate the significance of neutron and alpha-particle induced upset rates in combinational logic relative to upset rates in sequential devices and to estimate their relative contribution on the chip-level for the investigated technology. The second objective of this study is to test the accuracy of the SER simulation methodology introduced in [16].

The rest of the paper is organized as follows. Section II describes the design of our test chip. The experimental setup and results are summarized in section III. Our simulation methodology is briefly introduced in section IV along with key simulation results. Finally, in section V simulated and measured data are compared and the importance of combinational SER on the chip-level is discussed.

II. TESTCHIP DESIGN

Latch upset rates are typically measured with simple shift-register type test chips [21]. During beam exposure the clocks are stopped and the latches are in store mode. It is well known that combinational upset rates are proportional to clock frequency and therefore high clock speeds are required to capture statistically significant numbers of upsets [22, 13]. Supporting high clock frequencies on wire-bonded test chips tremendously complicates the test chip design. The analysis of upset rates detected for test chips that contain both combinational and sequential logic is further complicated by the fact that soft error rates of sequentials depend on the clock frequency [9]. To simplify the analysis and test the susceptibility of realistic data paths we designed a test chip that can be run at clock speeds up to 2 GHz. Sequential upset rates are guaranteed to be independent of the clock frequency in our design[2]. The susceptibility of clock generators and error detection logic is minimized in by implementing hardened devices. Local clock node strikes do not impact the sequential SER significantly, since the data at the input of the receiving FF and the state stored in the FF are identical. Radiation-induced race [23] is not contributing significantly since the probability that a SET is propagating to the receiver just when the receiving FF is hit by another particle strike is extremely low. Since regular data are not propagating in our design (first inverter in inverter chain connected to ground), radiation-induced jitter is not an issue [23].

The key functional blocks of our test chip (see Figs. 1 and 2), manufactured in a 32nm process, are [24]: clock configuration registers, clock generator, data paths, and a scan chain. The on chip clock generator can provide 16 different clock frequencies from 80MHz to 2GHz. The desired clock frequency is generated by writing appropriate bits to the clock configuration registers which are radiation hardened. The clock provided by the clock generator, MCLK, is distributed to the data paths of the entire die through a shielded clock network. For MCLK clock speed validation purposes, the clock signal is divided by 1E6 and fed out through an I/O pin which can be monitored by an oscilloscope. Each data path contains 12 chains of inverters connected to flip-flops through the logic network of XNOR, NAND and NOR gates. The data path flip-flops (FFs) are controlled MCLK and output of each flip-flop is connected to an asynchronous 3-bit binary up counter constructed from hardened FFs. Please note that it is the asynchronous nature of the counter that guarantees FF upset rates that are independent of MCLK [9]. We believe that this approach is superior to using hardened receivers as implemented by Gadlage et al. [17]. Our simulation results indicate that SET capture probabilities (i.e., latch masking) of hardened FFs are significantly different from non-hardened FFs which would have complicated extracting the pure combinational SER contribution for realistic data paths.

We implemented four different types of data paths: N6, N10, S6, S10. N6 is a nominal inverter chain with a length of 6 inverters. Similarly, N10 has 10 nominal inverters in the chain. S6 has 6 skewed inverters in the chain, and S10 has 10 skewed inverters. The inverters in the skewed paths are skewed by adjusting the P/N ratio to allow for better SET propagation. The P/N (or N/P alternating scheme[3]) ratio is about 4x higher for the skewed devices when compared to the nominal ones. The nominal inverters have close to equal low and high transition times and the corresponding P/N ratios are much closer to devices typically implemented in products. All inverters in the data path sections are minimum sized inverters to maximize SET generation rates. The P/N ratio of the complex gates has not been skewed. Fig. 1 shows the micrograph of the test chip.

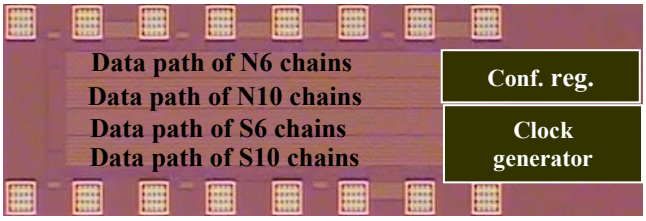

Figure 1: Micrograph of the combination logic test chip.

Fig. 2 is a schematic representation of the data path block. 12 inverter chains feed the flip-flop running at the MCLK frequency through the logic network of XNOR, NAND, and NOR gates. These complex combinatorial devices have been scaled such that radiation-induced SET formation is very unlikely relative to the skewed inverters but the SET propagation properties are excellent. Simulated and experimental data verify this design objective as will be demonstrated in subsequent sections. A SET generated in any of the inverters chain has a propagation path to the receiving FF. SETs propagating to the FF with sufficient width and amplitude will be latched and the hardened asynchronous counter is updated. The counters are read out from the test chip by using a scan chain. Our test chip is designed in such a way that an unlimited number of test chips can be connected in daisy chain fashion to maximize the number of upsets observed, improving the counting statistics.

[2] Data presented in this publication are only up to 1.4 GHz though.

[3] Since the first inverter is grounded its N/P ratio is about 4x that of the balanced inverter. The 2nd inverter then has a P/N ratio of 4x the balanced one.

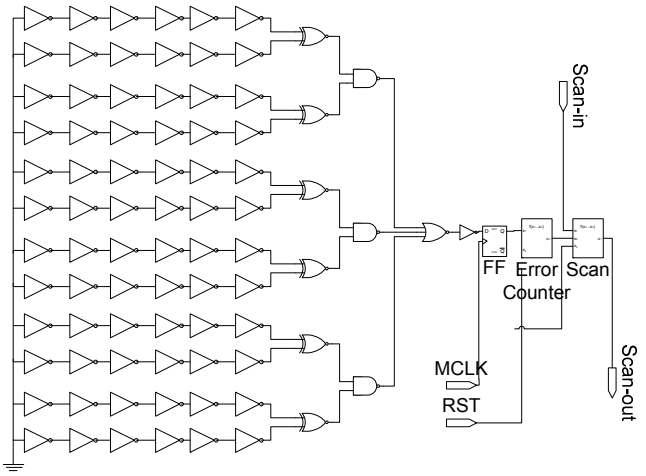

Figure 2: Schematic representation of data path and SER count logic.

III. Experimental Setup and Results

Collecting sufficient numbers of upsets to warrant good SEU counting statistics was a challenge particularly for the neutron beam experiments where beamtime was very limited. Therefore, neutron-induced combinational SER data were taken at one power supply voltage only. Shown clock frequencies depend on voltage settings and reflect measured values.

A. Experimental Setup

Accelerated radiation experiments have been performed. The sensitivity of the combinational and sequential test structures to alpha-particle radiation was studied by placing Thorium-232 foils on the wire bonded test chips described above. Alpha-particle induced upset rates are corrected for geometry effects and alpha-particle absorption as described in [27] and normalized to a 0.001 alpha-particles/cm^2/hr flux.

Neutron SER data were collected at the the Los Alamos Labarotory Weapons Neutrons Research (WNR) facility, New Mexico.

B. Alpha-particle SER Results

Fig. 3 shows alpha-particle induced upset rates (aSER) as a function of clock frequency at 0.75V. S10 denotes 10 inverters long skewed paths, N10 nominal (balanced) paths and S6 and N6 the corresponding 6 inverter deep versions. The solid line reflects the simulated soft error rate of the FF receiver using calibrated soft error compact models as described in [1]. All upset rates have been divided by the number of receiving FFs and therefore reflect the upset rates of one combinational logic block as shown in Fig. 2.

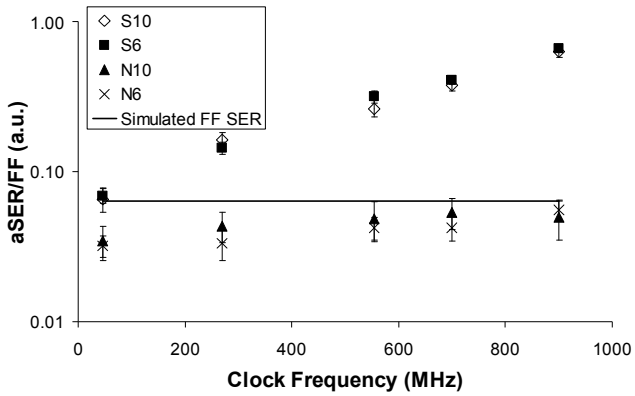

Figure 3: Measured alpha-particle induced upset rates per receiving FF are plotted as a function of clock frequency[4].

In the case of Fig. 4 the sequential SER has been subtracted from the measured upset rates/FF to derive the "pure" combinational SER per FF receiver. This approach assumes that the nominal SER at the lowest frequency reflects best the measured FF SER rather then using simulated results which would have yielded slightly negative upset rates in some cases (particularly in cases with poor counting statistics).

Four key observations can be made in Figs. 3 and 4: SER increases approximately linearly with clock speed, b) Paths with skewed devices show a much higher combinational SER than balanced paths (~10x at 1GHz), c) Both, S10 and S6, show the same comb. SER/FF, and finally, d) Combinational and sequential SER exhibit similar slopes as a function of supply voltage. The latter point is not obvious from Figs. 3 and 4, but our measured FF aSER and simulated FF aSER both increase by ~2-3x when reducing Vcc from 0.95V to 0.75V.

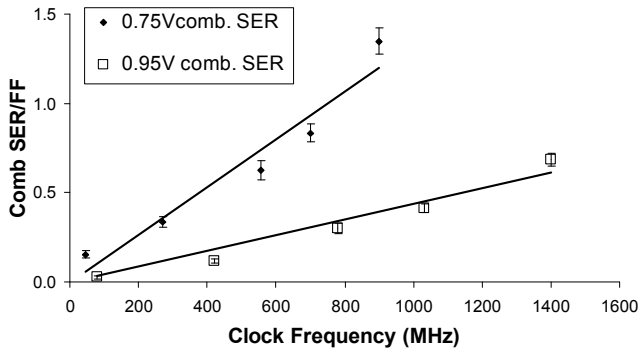

Figure 4: Measured combinational aSER for skewed paths is plotted as a function of clock frequency for two different power supply voltages.

C. Neutron SER Results

Because of poor counting statistics N10 and N6 upsets are combined into the "Balanced Paths" SER bin and similarly the S6 and S10 upsets are added to the "Skewed Paths" bin. Neutron upset rates/FF show a similar increase with clock frequency as the alpha-particle data (Fig. 5). The solid line in Fig. 5 reflects the simulated upset rate of the receiving FF at 0.95V.

[4] Throughout this document error bars denote one standard deviation.

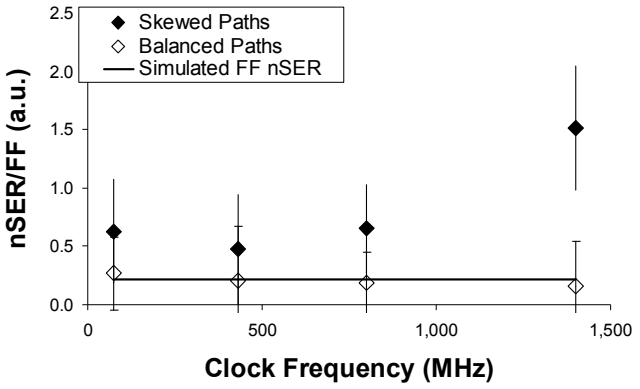

Figure 5: Measured neutron induced soft error rates of skewed and balanced data paths are plotted as a function of clock speed. Upset rates reflect a power supply voltage of 0.95V.

In contrast to the alpha-particle SER, no frequency dependence is observed in the neutron SER data for balanced paths. Further, neutron-induced upset rates for S10 paths are almost 2x those of S6 paths, but this is well within the error of the measurement (and consequently ignored).

The ratio of neutron to alpha combinational SER assuming an alpha flux of 0.001 counts/cm^2/hr is about 2.5x at 0.95V. In both cases the ratio of the skewed to balanced (FF) SER is of the order of 10x at 1400MHz.

IV. Simulation Setup and Results

The simulation methodology applied in this study, which is called TIDEST, is described in detail in [9, 16, 23]. In the following, the main features of this methodology are summarized. The average combinational or sequential upset rates <SER> are calculated using (1) [9]

$$< SER >_{\alpha,n} = \sum_{Node\ i} \sum_{Time\ j} SER_{\alpha,n}(Qcrit_{\alpha,n}^{i;j}) \frac{\Delta t}{T_{cycle}} \quad (1)$$

where Tcycle denotes the clock cycle, α and n the alpha-particle or neutron induced failure rates. The first sum in equation 1 is over all circuit nodes (Node – i) of interest (can be either combinational or sequential nodes).

To compute the average derated SER of a circuit, a clock cycle is divided into N time-steps of length Δt. At each time-step Qcrit is determined and the nominal SER is computed. The monitor node for the derated SER computations in this work is the output node of the asynchronous counter (see Fig. 2). Qcrit values are determined as a function of current injection time by inserting voltage independent current sources into the netlist of the circuit depicted in Fig. 2. Particle-specific current waveforms as are applied and the soft error rates are calculated using a compact model as described in [1][5].

Our methodology accounts for timing vulnerability factors [12, 13]. However, only particle strikes at local clock nodes were simulated in this study. It is known that the susceptibility of upstream clock nodes and drivers is low in a terrestrial radiation environment [23]. Further, global clock node drivers and registers that store clock frequency parameters needed for the correct functional operation of the test chip were hardened (by implementing SEUT devices; see [25, 26]). Since the computational methodology is Spice based, radiation-induced SET propagation, electrical and logical masking, and latching-window masking are automatically included in this approach.

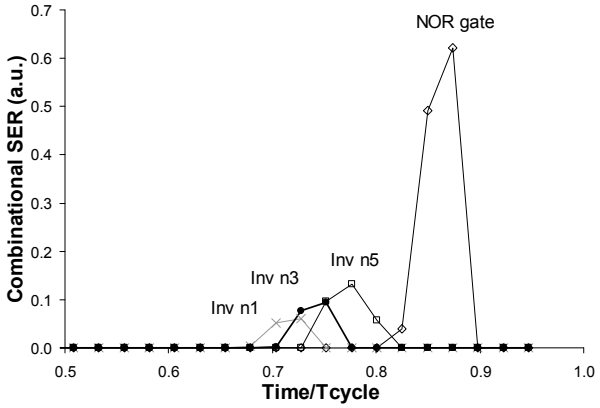

Figure: 6: Simulated aSER of selected combinational N10 nodes as a function of charge injection time.

In Fig. 6, simulated alpha-particle upset rates of combinatorial nodes along the balanced paths are plotted as a function of charge injection time. “Inv n1” to “inv n5” denote the first three odd inverter nodes in consecutive order counting from the gate after the grounded inverter (most upstream device in Fig. 2). The “complex gate node” denotes the NOR node closest to the FF receiver. Inverter chain nodes are located farther away from the receiving FF than complex gate nodes and their combinational SER therefore peaks earlier during the cycle due to longer SET propagation times.

TABLE 1: Ratio of measured to simulated combinational and sequential upset rates.

Freq (MHz)	Vcc (V)	Type	S10 Ratio	S6 Ratio	N10 Ratio	N6 Ratio	FF Ratio
1400	0.95	aSER	0.7	0.6	1.9	4.8	0.6
1400	0.95	nSER	0.4		2.4		0.8
900	0.75	aSER	0.8	0.9	0.8	1.7	0.5

Table 1 compares combinational and sequential SER simulation results with measured data. Simulated and measured results are within 2-3x with one single exception, where the uncertainty in the measured data is known to be large.

V. Discussion

One of the key objectives of our test chip design is to determine the susceptibility of combinational logic manufactured in an advanced bulk CMOS process to alpha-particle and neutron radiation.

[5] SER is assumed to be a function of the critical charge, diffusion area, transistor type and particle type

The results shown in Fig. 4 demonstrate a linear increase in upset rate in skewed paths with clock speed, which is the trademark of combinational SER [13, 14]. Further, upset rates of balanced (nominal) paths show only shallow slopes as a function of clock frequency, which is consistent with sequential SER dominating over the combinational one and the sequential SER being independent of clock frequency. Timing vulnerability factors of receiving data path FFs are independent of the clock frequency as discussed above. Error counters register the sequential SEU whenever it arrives at the counter input gate and SEU propagation times are consequently irrelevant. This conclusion is also supported by our sequential simulation results which are within ~50% of the measured upset rates and show no clock frequency dependence.

The fact that measured and simulated sequential SER results agree well is not very surprising since SER compact models have been calibrated specifically for memory devices manufactured in this 32nm process as described in [1]. However, the results listed in Table 1 also support the conclusion that applying voltage independent current sources yields combinational upset rates with a reasonable degree of accuracy. This indicates that small amplitude but wide voltage SETs, that according to [3] are the most frequently occurring ones, are electrically masked before reaching the FF receivers in circuits built in this 32nm technology. Further, radiation-induced collected charge is efficiently compensated by node drivers and keepers, such that SET widening by a field collapse is not relevant either[6]. Our experimental findings provide direct evidence that SETs only propagate a finite number of gates before they are electrically masked (S10 and S6 combinational SER are identical within error bars; Fig. 3). Because only two different data path lengths have been implemented in our test chip, we are not able to quantify the exact logic cone depth <d> in gates under the tested conditions for this technology. However, the fact that our simulation results are in agreement with our experimental data enables us to simulate this distance from the clocked receiver. The (SER-) weighted averages of the combinational SER fanin cone depth <d> as defined in (2) are about 3.5 for alpha particles and 4.0 gates for neutrons.

$$< d >= \int_1^{pd} SER(x)xdx \,/\, \int_1^{pd} SER(x)dx \qquad (2)$$

where SER(x) denotes the dependence of the combinational SER on distance x in gates from the receiver derived from SER simulations as shown in Fig. 6. pd equals the total number of gates in a data path (data path depth), which equals 10 or 14 in the case of our test chip (N6 or N10).

Shivakumar et al. [15] projected that at the 50nm technology node, combinational SER of a logic chain will be equal or higher than the receiving latch SER. Fig. 7 directly addresses this statement for circuits manufactured in a 32nm bulk CMOS process and demonstrates that the SER of one single logic chain is less than 10% of the nominal latch SER[7] at 1 GHz[8]. It is worth mentioning that upset rates for skewed logic is about 10x higher and indeed of similar magnitude as the nominal latch SER at typical product clock speeds. However, these extreme P/N ratios are not representative of actual circuits on real products. Their sole purpose is to maximize combinational SER and enable us to quantitatively compare our SER simulation results to measured upset rates.

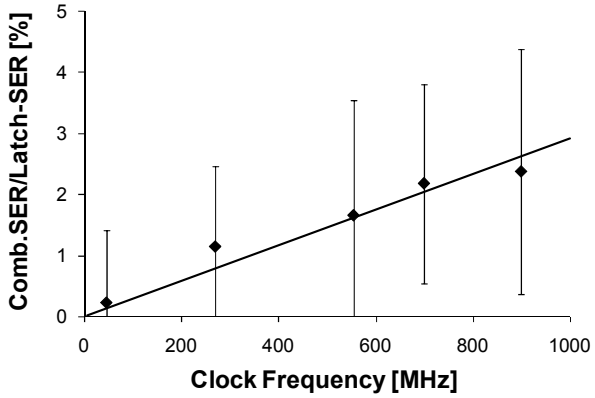

Figure: 7: Total (i.e., alpha-particle + neutron) combinational SER of a single data path chain (balanced N/P) as implemented on our test chip in per cent of the nominal latch[7] SER is plotted as a function of clock frequency.

Product Level SER Extrapolation

The chip-level significance of combinational SER can be determined by two different approaches:

1) Because the circuit-level simulation accuracy has been validated, one can run circuit-level TIDEST type simulations of representative logic circuits and extrapolate to the chip-level. Exhaustive chip-level simulations are impossible due to runtime constraints and spice convergence issues. It is worth mentioning that TIDEST simulations on one data path block as shown in Fig. 2 can take several hours on a modern system cluster for simulating the error rate of one combinational node.

2) Or use the figure of merit (FOM) shown in Fig. 7 to determine an upper bound of the combinational SER expressed as a fraction of the total chip-level sequential SER.

We selected the 2nd method and applied the following equation to derive at an upper estimate of the combinational SER in modern microprocessors expressed as a percentage of the nominal latch SER at the same use conditions

$$\frac{SER_{comb}}{SER_{Latch}}[\%] \approx LD_{comb} * f_{clock}[GHz] * \left(0.6\% * \begin{cases} \dfrac{\left(Fanin^{<d>+1} - 1\right)}{(Fanin - 1)}; Fanin > 1 \\ < d >; Fanin = 1 \end{cases} \right) \qquad (3)$$

where 0.6% reflects an upper bound of the combinational SER per gate at 1GHz relative to the unhardened nominal latch SER[7,9]. It is worth mentioning that the data pattern dependence of combinational

[6] We suspect that the situation is very different for space environments where high values in stopping power (LET) and correspondingly large amounts of generated charge are much more common.

[7] Latch SER is assumed to equal ½ of FF SER

[8] This figure of merit derived from measured N10 and N6 SER data applies a simulated neutron to alpha particle comb. SER ratio because the measured neutron balanced path SER statistics are not sufficient to extract a slope with clock speed.

[9] valid for P/N ratios typically found in products

SER has been accounted for in the 0.6% FOM in (3). Preventing to write a new value into a latch is characterized by a different upset rate than writing an incorrect value. The combinational SER therefore depends on whether the data inside and outside the sequential logic are different or identical[10]. The parameter Fanin reflects the average product fan-in of logic gates. The higher the fan-in the wider is the logic cone and the larger is the number of susceptible logic at a fixed depth <d> feeding into one equivalent latch receiver[11]. Please note that the expression containing the parameter Fanin after the left brace in (2) is only a rough estimate of the number of gates within the sensitive logic cone that is strictly valid only if all gates have the same average fanin. Finally, LD_{comb} accounts for the fact that in many cases SETs are logically blocked by logic upstream to the receiving sequential (logical masking). For consistency reasons with [15] LD_{comb} is set to equal one in this study.

Applying typical clock speeds and fan-in statistics for modern microprocessors, we get an upper bound of about 30% for the relative contribution of combinational logic SER relative to the nominal latch SER on the chip-level (under the conservative assumption that LD_{comb} = 1). Please note that LD_{comb} is not equal to LD (aka Architectural Vulnerability Factor (AVF) [12, 13, 28]. LD (AVF) denotes the probability of a latched fault in a sequential to be important to the correct execution and output of a program (i..e, whether the fault becomes an observable error). LD_{comb} in contrast denotes the probability that a SET is not blocked on its path to a receiving sequential. However, even when a conservative LD_{comb} = 1 is applied, combinational SER is clearly not a dominant SER contributor on the chip-level for the process studied, assuming that most implemented sequential devices are not SEU hardened [29].

Equation (3) is only applicable to static combinatorial logic in data paths but not to SETs induced in control logic. However, the fact that our simulation methodology works well for static logic in data paths indicates that it can be applied to project the sensitivity of static logic in control paths as well. Simulation results of the impact of clock node strikes have been reported in [23].

It is important to remember that other manufacturers might arrive at a different conclusion, similarly to the wide variety of SER trends observed for logic devices [16]. More aggressive scaling of Qcrit, or less scaling in charge collection efficiency, or a strong bipolar parasitic effect all have the potential to dramatically increase the significance of combinational logic SER in modern technologies [19]. Gadlage et al. [17] estimated that combinational SER induced by 200 MeV protons is of the order of 10% of unhardened FFs at 300 MHz for test chips manufactured in an 180nm process. The average number of logic gates per pipeline stage is on the order of 4 in their tested design [17], suggesting a ~8% combinational SER per static logic gate at 1GHz, which is ~25x higher than our FOM (~0.3% per FF[7]). It is worth mentioning that a direct comparison of the SER performance is not straightforward because the absolute soft error rates of the receiving sequential devices are not known[12].

[10] The experimentally tested setup (Fig.2) addresses only one combination: Data stored inside and outside the receiver are identical. Simulation results have been applied in (3) to extrapolate to a 50% data pattern distribution.

[11] Equivalent, because the receiver could be a FF instead a latch or any other clocked device. We chose to compare the combinational SER to the nominal latch SER since that is what Shivakumar et al. seems to have done.

[12] One can still conclude that combinational SER is of greater significance in the investigated 180nm technology than in our 32nm one.

Narasimham et al. have observed very large SET widths that show similar distributions for alpha-particle, neutron or heavy ion radiation in test chips built in 130 and 90nm bulk technologies [19]. It is speculated that SET widths in the investigated technologies are dominated by a bipolar effect rather than by drift and diffusion [19]. We believe that the successful suppression of bipolar effects in the tested 32nm technology contributes to the observed low combinational error rates.

VI. CONCLUSIONS

This paper addresses the importance of combinational SER in modern 32nm CMOS circuits and products in terrestrial radiation environments. To quantitatively estimate the contribution of combinational SER relative to sequential SER, a test chip has been designed and exposed to alpha-particle and neutron radiation. The test chip implements four different types of data paths feeding into non-hardened sequentials. Balanced (nominal) paths reflect P/N ratios that are close to those implemented in products, whereas skewed paths maximize SET generation and propagation to test the accuracy of our simulation methodology against measured data. The design strategy chosen ensures a sequential SER that is independent of clock speed and minimal contributions due to clock nodes strikes.

Our results are consistent with combinational SER increasing linearly with clock frequency. For the test chip analyzed, the neutron combinational SER is about 2x higher than the alpha-particle induced one. Further, the combinational SER contribution per sensitive static logic gate is less than 1% of the nominal latch SER at 1GHz at 0.75V.

Sequential soft error simulation results based on calibrated SER models are within ~2x of the measured error rates whereas simulated combinational SER projections are within 2-3x of our test chip data, which is surprisingly accurate. The latter result indicates that applying voltage independent current sources to mimic particle strikes yields sufficiently accurate estimates for terrestrial radiation environments.

Based on measured and simulated soft error rates, chip-level conservative estimates are derived by factoring in product P/N and logic depth distributions and typical use conditions. Our results indicate that the chip-level SER contribution of combinational logic is well below 30% of the chip-level nominal latch SER in the investigated 32nm process technology.

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