# Single Event Transient Mitigation Through Pulse Quenching: Effectiveness at Circuit Level

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***Abstract*—This paper exploits the pulse quenching effect in order to reduce circuit error rates due to single event transients in combinational logic. Although the effect allows for substantial reduction in the sensitive area of a single cell, logical masking at circuit level has to be also considered. Our results show that pulse quenching has a limited effectiveness at circuit level. The results of the proposed approach can be used to drive a reliability-aware design flow.**

## I. Introduction

Technology scaling has led to a number of worth noting improvements in current CMOS based circuits, such as higher operating frequencies and lower operating voltages. The same reduced distance between transistors that has allowed for these and other improvements has also enhanced circuit's sensitivity to single-event effects (SEEs).

One particular kind of SEE, termed single-event transient (SET), occurs when an ion hits the combinational logic of a circuit. These hits lead to shifts in the legitimate logic signals being propagated and, in some scenarios, may propagate long enough through downstream logic until reaching a memorizing element like a flip-flop. The erroneous value from this flip-flop can reach one of the primary outputs of the circuit then effectively causing an error.

It has been acknowledged that multiple transistors can collect charge from a single ion hit in a process referred as charge sharing [1]. As a matter of fact, these multiples SETs might occur between nodes that are not electrically related, potentially increasing the circuit error rate. Many studies have been performed with the sole goal of characterizing the charge sharing profile [1, 2, 3]. Factors such as particle's energy, angle of incidence and the type of the device that was struck (i.e., NMOS or PMOS) should be considered.

Furthermore, when the affected nodes are indeed electrically related, a secondary mechanism may take place, in which the induced transient pulses might be reduced or quenched. Thus, the term pulse quenching (PQ). The work of Ahlbin et al. [4] has described PQ thoroughly.

However, the analysis in [4] has been made at gate-level. No actual circuit-level analysis was performed. Thus, the goal of this paper is to extend such analysis to larger circuits and to evaluate if the mechanism still plays an important role in error rate reduction at circuit-level. Also, a secondary analysis is performed using the layout technique described by Atkinson et al. in [5], which intentionally promotes PQ by introducing additional circuit area.

This paper is organized as follows: foundations of charge sharing and quenching mechanisms are discussed in Section II. A detailed description of our analysis is given in Section III. Results are presented in Section IV while our conclusions are drawn in Section V.

## II. Background: SETs, Charge Sharing and Pulse Quenching

When a particle strikes a microelectronic device, the most sensitive regions are usually reverse-biased p/n junctions. The high field present in a reverse-biased junction depletion region can very efficiently collect the particle-induced charge through drift processes, leading to a transient current at the junction contact [1]. SETs are usually characterized by the width of such generated transient current.

While the size of the ion track generated by an incident ion on a silicon surface remains relatively constant, the distance between adjacent devices has been significantly reduced with technology scaling. In fact, multiple transients due to a single ion hit (i.e., due to charge sharing) have been measured for currently in use technology nodes such as 90nm [6] and 65nm [7].

Charge sharing is a big concern because it has the potential of making hardening techniques ineffective, thus many works have aimed at reducing charge sharing. For instance, Black et al. [8] made use of guard contacts to reduce charge sharing in PMOS devices. Other works try to explore/promote the charge sharing mechanism to reduce error rates. For instance, Entrena et. al [9] identified pairs of cells that, if struck at the same time, would produce transients that would be masked, i.e., would cancel each other. In other words, such work promotes charge sharing between cells that, when struck, will have their transients logically masked.

Analogously, PQ can be used to promote charge sharing and reduce error rates. Nevertheless, it has a different behavior since it is not linked to logical masking. Due to a dynamic interplay of charges, SETs can be masked "electrically" if two adjacent transistors have similar time constants for (delayed) charge sharing and actual signal propagation. The concurrency of these two effects may cause shorter than expected transients, thus partially masking the transient. The effect is prominent in inverter-like structures (actual inverters or larger cells that

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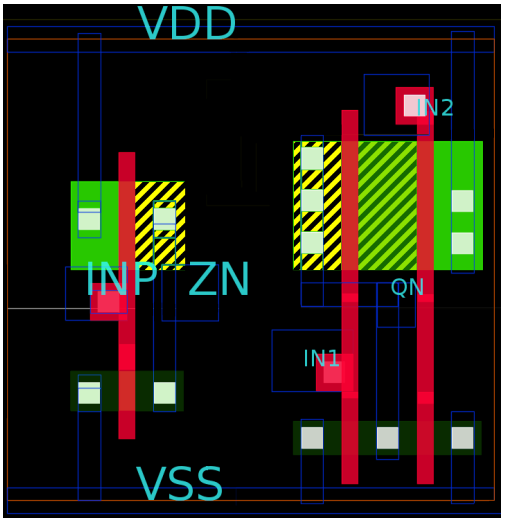


Fig. 1: Layout of an inverter and a NOR2 cell from a 90nm ASIC library.

have an inverting stage). Details concerning the delayed charge collection mechanism are explained in [4].

## III. Methodology and Error Rate Analysis

Since the PQ effect is prominent in inverter-like structures, our analysis begins by identifying such structures. First, it should be mentioned that several CMOS gates already have an internal inverter stage (ORs and ANDs, for example). Such gates already have the potential of quenching pulses, a phenomenon we term *intra-cell PQ*.

Nevertheless, some cells that do not have an inverter stage can benefit from *inter-cell PQ*, which can be achieved by rearranging the circuit layout. Some pair of cells might be brought together during placement to make them effectively quench pulses. The trade-off here is that routing will not be optimal. In this work, the interest is focused on those pairs of cells that promote inter-cell PQ. The first cell in the pair is termed primary while the other cell is termed secondary. Those cells must match the following criteria to be considered in our analysis:

- The primary cell must have (at least) one 'exploitable' output. The drain region of the PMOS transistor connected to that output must be near the cell's boundary. Thus, charge sharing with a neighboring cell can be exploited.
- The secondary cell must have one input that is connected to an inverter-like structure.
- The secondary cell's input node (i.e., the drain region to which the input is connected) must also be near the cell's boundary region.

That being said, we proceeded with an analysis of a 90nm standard cell library [10], in order to identify which cells are fit for being primary and/or secondary cells. Figure 1 depicts a layout containing two cells from the referred library: a NOR2 on the right-hand side and an inverter on the left-hand side.

TABLE I: Average reduction in sensitive area due to pulse quenching.

| Cell | Factor | PMOS transistors |
|---|---|---|
| INVX0 | 100% | 1 |
| NOR2X1 | 50% | 2 |
| AND3X1 | 30% | 4 |
| XNOR2X1 | 16.6% | 7 |

The NOR2 cell in Fig. 1 is a good candidate for being a primary cell since it matches the previously mentioned criteria. The portion of the image highlighted in yellow corresponds to the sensitive drain area that has the potential of sharing charge with a neighboring cell. Bringing the inverter close to the NOR2 cell thus effectively promotes PQ (it is assumed both cells are connected through a higher layer metal, which is not represented in the image).

After a full analysis of the library, 16 cells that can act as the primary cell were identified. Only two cells can act as the secondary cell (inverters and buffers). Obviously, since all those cells implement different logic functions and have different sizes (i.e., drive strengths), they do not quench pulses with the same efficiency. We have defined average quenching efficiency factors for all cells. Some of those factors are given in Tab. I. They are directly related to the size of the secondary cell of the pair. It is assumed the charge sharing area will always comprise the whole primary cell and a portion of the secondary cell.

The factors defined in Tab. I are intentionally overestimated. For instance, let us take the NOR2X1 cell, which has 2 PMOS transistors (as depicted in Fig. 1). We consider that the drain region associated to the leftmost transistor can always share charge with a neighboring cell, while the region in the center of the image can share charge 50% of the time (because its distance to the neighboring cell is higher). Thus, the reduction in sensitive area is of 50%. Yet that value does not take input patterns into account. Analogously, cell AND3X1 has 4 PMOS transistors, from which 2 are considered able to share charge. Yet not all drain regions are equally sized in the layout of that cell. Once again, we assumed all nodes to be equally important, which is also a source of overestimation. For a detailed discussion regarding the reductions in sensitive area, the reader is referred to [5].

It was also assumed that a cell can be flipped whenever necessary to meet the defined criteria. Flipping can and usually will add some additional wiring due to less optimal routing.

The circuits from the ISCAS'85 benchmark suite [11] were chosen as our case study. After an analysis of each circuit's topology, we have identified two possible scenarios in Tab. II. An inter-cell pair is a pair similar to the one depicted in Fig. 1. The unpaired candidates are cells that fit the profile of a primary cell but are not electrically connected to any inverter-like structure, thus PQ cannot be promoted by pairing.

Nevertheless, a hardening by design technique proposed in [5] can be used to make those cells more robust to SEEs.

TABLE II: Number of pairs.

| Circuit | Number of gates | Inter-cell pairs | Unpaired candidates |
|---|---|---|---|
| *c432* | 160 | 3 | 42 |
| *c499* | 202 | 0 | 98 |
| *c1355* | 546 | 0 | 130 |
| *c1908* | 880 | 214 | 289 |
| *c2670* | 1269 | 309 | 694 |
| *c3540* | 1669 | 279 | 1041 |
| *c5315* | 2307 | 461 | 1365 |
| *c6288* | 2416 | 31 | 257 |

This technique comes with a considerable cost in area, while bringing together pairs of cells that are already supposed to be connected is of minimal cost, if any, since many of those pairs might already be side by side after placement.

From Tab. II it is already possible to conclude that many circuits will not have a significant reduction in error rate due to the small number of inter-cell pairs. This and other factors are explored in the next section when our results are presented.

## IV. Results

In order to evaluate how the reduction in sensitive area translates into reduction in error rate, we have made use of the SPRA method [12]. Its original purpose is to calculate circuit reliability by taking into account logical masking. One positive aspect of using such method is that it is not simulation-based (i.e., it is analytical), thus all possible input scenarios can be taken into account in a linear execution time. More details about the method can be found in [12].

During our analysis we have slightly modified the use of SPRA. First, it should be mentioned that each gate is characterized in SPRA by a $q$ value. This value determines how reliable each cell is, in a range of [0,1] (where 1 means the cell does not produce faults and zero means it always produces faults). For each gate $g$ in the circuit, we have performed one SPRA run in which that gate (and that gate only) is set with $q = 0$. All the others are set with $q = 1$. Each run would then produce a reliability result $R(g)$, between 0 and 1. Such result can be interpreted as the circuit error rate due to an error in gate $g$ (averaged by all possible input scenarios). Such effort is only possible due to the analytical approach of SPRA.

If we sum all $R(g)$ values, for all gates, and divide by the number $N$ of gates in the circuit, we get the averaged circuit error rate. Such analysis was performed for the circuit *c432* and is shown in Fig. 2, in which the black solid line shows $R(g)$ per gate while the dashed line shows the average $R(g)$ value. The gates in the $x$ axis are ordered by their $R(g)$ value.

Now, let us suppose a hardening technique is to be applied to a gate $g$ such that the gate still implements the same logic function but it is less sensitive to SETs. An increase in its $R(g)$ value is expected, but the improvement $I(g)$ is limited by:

$$I(g) \leq 1 - R(g) \tag{1}$$

TABLE III: Reliability improvements due to inter-cell and intra-cell PQ.

| Circuit | Inter-cell PQ | Combined with intra-cell PQ [5] |
|---|---|---|
| *c432* | 0.196% | 0.453% |
| *c499* | 0.000% | 9.932% |
| *c1355* | 0.000% | 1.580% |
| *c1908* | 3.731% | 4.199% |
| *c2670* | 3.691% | 7.150% |
| *c3540* | 2.356% | 6.211% |
| *c5315* | 2.245% | 7.841% |
| *c6288* | 0.941% | 5.368% |

since logical masking will still take place. At the circuit level, improving one gate's $R(g)$ will not change the $R(g)$ values of other gates. Thus, the improvement $I_c$ at the circuit level becomes limited by:

$$I_c \leq I(g)/N \tag{2}$$

According to Tab. II, only 3 gates from the *c432* circuit might benefit from inter-cell PQ, which are shown in Fig. 2 as red diamond shaped points. All 3 improvements are the same: $R(g)$ values change from 0 to 0.105. Thus, $I(g) = 0.105$ for all 3 gates. Those improvements are, nevertheless, very small. Those improvements combined represent an average increase of 0.19% in circuit reliability, which increases from 48.16% to 48.35%.

Then we proceeded into applying the intra-cell PQ technique described in [5]. Such technique consists in adding extra inverters to the layout of a cell. Not all cells can benefit from that technique (the cell must have an internal inverter stage that can be duplicated) and not all cells benefit from it in the same way. The best case scenario is the OR2 gate, which becomes symmetrical after layout modifications (one inverter on each layout extremity). By doing so, the sensitive area of the OR2 gate becomes zero for 3-out-of-4 input patterns. The reader is referred to [5] for more details concerning the technique and its associated cost.

In the particular case of the circuit *c432*, only two gates can benefit from intra-cell PQ. They are represented in Fig. 2 by blue circles. Once again, even when considering both techniques at the same time, the increase in circuit reliability is quite small: 0.453%. The results for all the other studied circuits are given in Tab. III.

Results concerning the area increase figures due to applying the layout technique proposed in [5] are shown in Fig. 3. The circuit *c5315* has the largest area increase among the studied circuits (an increase that is equivalent to 307 OR2 cells). It must be highlighted that the same circuit has 2300 cells, thus such increase is not negligible. And, at the same time, the reduction in the error rate is of only 7.8%.

## V. Conclusion

The results given in Tab. III state that PQ cannot reduce circuit-level error rates by significant amounts. Even if the

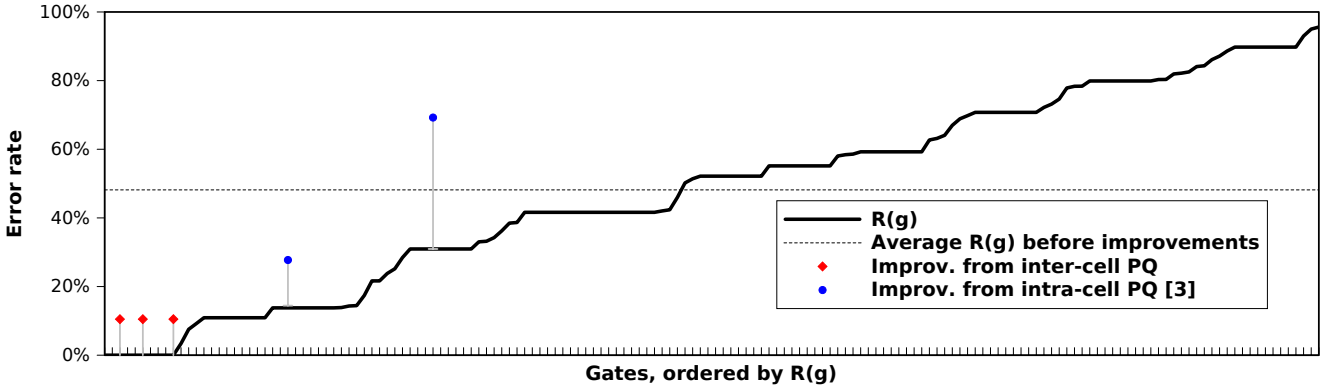


Fig. 2: Circuit error rates for the circuit *c432*.

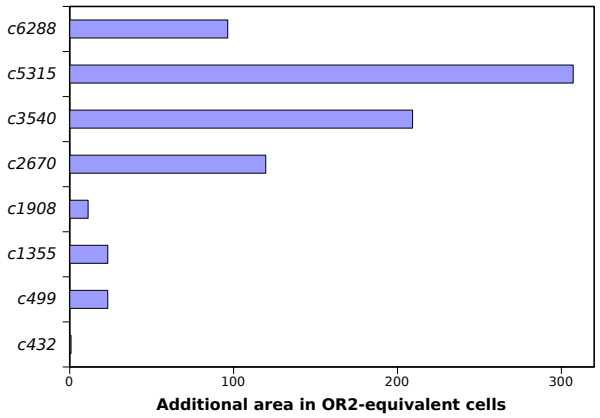


Fig. 3: Area increase due to the layout technique presented in [5].

simplifications described in Section III tend to overestimate the potential of PQ, the results are not expressive. There are several reasons for that:

- Logical masking plays an important role in circuit reliability. Hardening gates that are not capable of producing errors in the circuit output is meaningless.
- Not all circuit topologies are prone for inter-cell PQ, i.e., many circuit have a low number of suitable pairs, as highlighted in Tab. II.
- Even for the gates that are paired, the reliability $R(g)$ does not become 100%. This is highlighted in Fig. 2, especially for the paired gates (drawn as red diamonds).

Moreover, a detailed analysis of how small/large the improvements shown in Fig. 2 are has been made for multiple ISCAS'85 circuits. It shows that 44% of the improvements give marginal gains (smaller or equal to 10%).

Since the improvements from pairing come with almost zero cost, those are suitable for mostly all circuits and the analysis described in this work can easily be integrated in a design flow. Nevertheless, if the technique described in [5] is to be applied, is must be reasoned if the increase in area is worth the reduction in the error rate. In other words, a trade-off is created.

## ACKNOWLEDGMENT

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