Comparison of Error Rates in Combinational and Sequential Logic[a]

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Abstract

A pulsed laser was used to demonstrate that, for transients much shorter than the clock period, error rates in sequential logic were independent of frequency, whereas error rates in combinational logic were linearly dependent on frequency. In addition, by measuring the error rate as a function of laser pulse energy for fixed clock frequency, the logarithmic dependence of the SEU vulnerable time period prior to the clock edge in combinational logic was established. A mixed mode circuit simulator program was used to successfully model the dynamic response of the logic circuit to pulses of laser light.

I. INTRODUCTION

Recent experiments have demonstrated that the occurrence of single event upsets (SEU's) in logic circuits increases with increasing circuit clock frequency.[1-7] In fact, there is some evidence that at high frequencies the dynamic SEU rate may be dominated by errors generated in combinational logic, such as NAND gates, rather than in sequential logic, such as flip-flops.[2] With circuit clock frequencies constantly increasing, the threat to system reliability from dynamic SEU's is expected to become more of a concern for circuit designers. It is, therefore, important to understand the mechanisms responsible for SEU's in logic circuits, as well as their dependence on clock frequency.

Until recently, relatively few articles have been published in this area, primarily because of the difficulty of isolating dynamic SEU's in logic circuits exposed to unfocussed ion beams at accelerators. Without detailed temporal and spatial information, it is difficult to study the mechanisms responsible for dynamic SEU's. Modeling the effects with circuit and device simulator programs can provide some insight, but experimental verification is essential given the complicated nature of the problem.

Pulsed lasers are powerful tools for probing the origins of dynamic SEU's because i) the technique is nondestructive, ii) the laser light can be focused to a small spot for identifying areas sensitive to SEU, and iii) the arrival time of a light pulse can be synchronized to the circuit clock for measuring the time interval during which a node is sensitive to SEU. Two major limitations are the inability of light to probe sensitive areas covered with metal and the measured upset threshold cannot be converted to an equivalent one for ions.[8] Neither of these played a role in our experiments because (a) we did not measure upset thresholds and (b) all the circuits had some open area on the sensitive drains through which the laser light could reach the sensitive junctions.

Some results on both ion- and laser-induced dynamic SEU's in logic circuits have previously been published.[1-6] However, a detailed study comparing the frequency dependence of SEU's in both sequential and combinational logic has not yet been done. In some cases, measurements were taken at either one [1] or two frequencies [6] in GaAs circuits. It was shown that in a circuit employing majority voting and scrubbing at each clock cycle, the error rate at high frequencies was dominated by errors in combinational logic. In addition, the "window of vulnerability," defined as the time around a clock edge during which a logic element is sensitive to SEU, was measured by synchronizing the firing of the laser with the circuit clock and progressively delaying the one relative to the other.[2] A recent publication reported that the SEU rate in bipolar level shifters exhibited a linear dependence on frequency[3], but that a nonlinear behavior was observed in some proprietary clocked circuits with SEU's in logic circuits.

We show that, when the clock period is much longer than the setup times (the time just before a clock or enable pulse during which data must be kept at the input to guarantee recognition). the SEU error rate in combinational logic depends linearly on frequency whereas in sequential logic it is independent of frequency. [In combinational logic, the output of the logic element is determined by the inputs at that time, whereas in sequential logic, the output depends on the switching of a clock.] From the error rate dependence on laser pulse energy for the combinational element (inverter), we were able to calculate the SEU-sensitive time around the clock edge and its dependence on laser pulse energy. A circuit simulator program (SPICE) was used to model the response of the circuit to SEU's in the combinational

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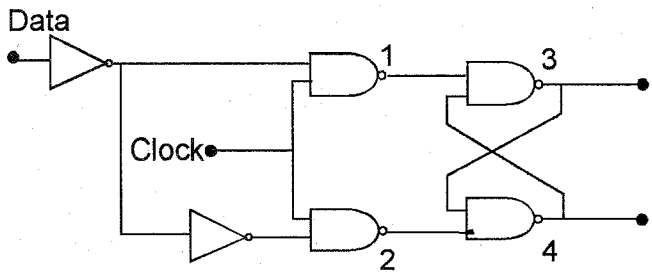

Fig. 1. D-type flip/flop containing six NAND gates and an input inverter.

element. The modeling results exhibited qualitative, though not quantitative agreement with the experimental data.

II. ORIGINS OF FREQUENCY DEPENDENCE

Standard SEU testing of memories such as SRAM's involves writing a test pattern into the entire memory, irradiating the part to a predetermined fluence with ions having the required linear energy transfer (LET), and then reading the memory to determine the number of SEU's. Obviously, clock frequency has no effect on static measurements of this kind. However, if the memory is continuously written to and read during irradiation, clock frequency does affect the measured SEU cross section, because the memory cell is essentially immune to SEU's when the pass transistors are turned on during the writing and reading operations.[9]

Clock frequency is an important factor that must be considered when measuring dynamic SEU's in logic circuits, and its effects are different for combinational and sequential logic. To illustrate, we consider a D-latch with an inverter on the input data line. The inverter is a simple combinational logic element, and the D-latch a simple sequential element. Fig. 1 shows the circuit. When the voltage on the clock line is low, the input is "disabled", and data stored in the D-latch is isolated from the input. Under these conditions, nodes 3 and 4 in the D-latch are sensitive to SEU's. When the clock voltage is high, the input to the D-latch is enabled, which forces a fixed state onto the D-latch and renders it immune to SEU's. However, if an ion deposits a sufficient amount of charge to disturb the output of the inverter just prior to the clock transitioning from high to low voltage, the disturbed voltage transient may be latched into the D-latch, and an upset will be registered. It has been shown that the time extent of a voltage transient, generated by an ion at the drain of a sensitive transistor, has a short rise time of about 50 ps and a decay time of a few hundred picoseconds, depending on the LET of the incident ion.[10] If the ion strike occurs at a finite time prior to the clock edge, an upset may still occur, provided sufficient charge has been deposited by the ion so that the voltage transient will still be beyond the threshold for upset when the clock pulse arrives If the ion strike occurs well before the clock edge, the transient will have decayed

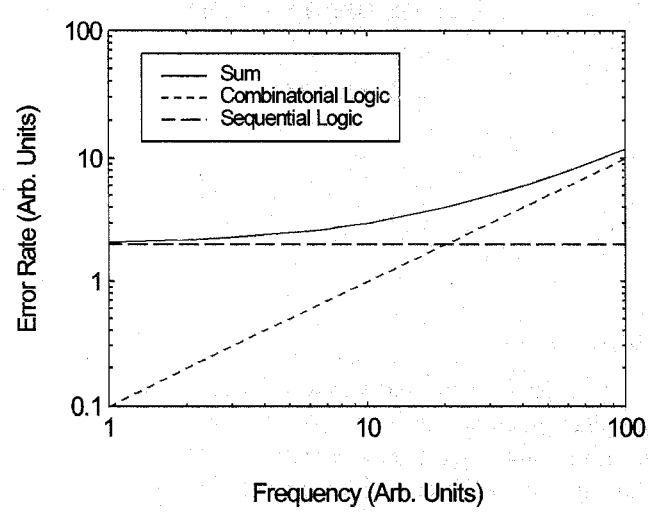

Fig. 2. Error rate as a function of frequency for combinational and sequential logic elements as well as their sum.

by the time the clock transitions, and no SEU will be registered. In summary, SEU's originate in sequential logic if the clock voltage is low, and in combinational logic if the ion strike occurs in a period just prior to the clock transitioning from high to low, where the period depends on the amount of charge deposited by the ion.

Frequency effects can be observed when a square wave voltage signal having a variable frequency is applied to the clock line. Because SEU's that originate in the D-latch only occur when the voltage on the clock line is low (50% of the time at all frequencies), they will not exhibit any frequency dependence, provided the setup time for the node is much less than the clock period. However, for SEU's that originate in the inverter just prior to the clock edge, changing the clock frequency (the number of clock edges per second) by a given factor will change the error rate by the same factor. Based on this simple analysis, the SEU rate for sequential logic should be largely independent of frequency at low frequencies, and should decrease at frequencies where the setup time becomes comparable to the clock period. For combinational logic, it should be linearly dependent on frequency. Fig. 2 shows the individual contributions from the inverter and the D-latch to the overall error rate for this "gedanken" experiment. At low frequencies, the SEU rate is dominated by those originating in the D-latch and at high frequency by those in the inverter. Obviously, the relative amounts will also depend on the relative sizes of the sensitive areas of the logic and D-latches, as well as their thresholds.

Another factor affecting the error rate is the amount of energy deposited by an ion. Static measurements with ion beams reveal that the SEU cross section increases with increasing linear energy transfer (LET), eventually reaching a saturation level at high LET's. The gradual increase in

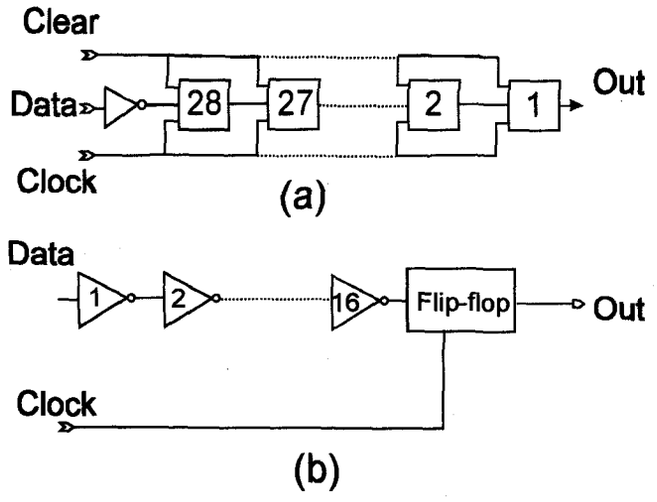

Fig. 3. a) Circuit SRWOTDCN consisting of a string of flip/flops with a single input inverter, and b) circuit EDGE consisting of a single flip/flop and a string of inverters.

cross section has been attributed to the varying SEU threshold across the sensitive area, such that at low LET's only a small fraction of the total sensitive area contributes to SEU's, whereas at high LET's most of the sensitive area contributes. For combinational logic circuits, the dependence of the dynamic SEU rate on laser energy (or ion LET) stems from two sources - the varying sensitive area and the varying sensitive time. The sensitive time around a clock edge increases as the amount of energy deposited increases. This effect can be explained by noting that, for an SEU to occur, the voltage on the node must be disturbed by an amount sufficient to cause subsequent nodes to switch. If the disturbance occurs just prior to the clock transition, less charge will be needed than if it occurs at an earlier time. It is the goal of this paper to demonstrate that the vulnerable time depends logarithmically on laser pulse energy because it is related to the exponential decay of the voltage transient on the struck node.

Measurements of SEU cross sections for logic circuits will include both effects. For instance, if the amount of energy deposited just exceeds the threshold for upset, the time interval prior to the clock edge during which an error can occur will be short and the sensitive area will be small, resulting in low error rates. Conversely, for large deposited energies, both the SEU sensitive time and area will increase, resulting in high error rates. An ion beam could, in principle, separate out the contribution from timing effects, but only at high LET's for which the SEU-sensitive area is saturated but the "window of vulnerability" is not. During pulsed laser measurements, the location of the focused spot does not move, so that the SEU dependence on pulse energy is due entirely to variations in timing sensitivity with deposited energy and not to variations in sensitive area.

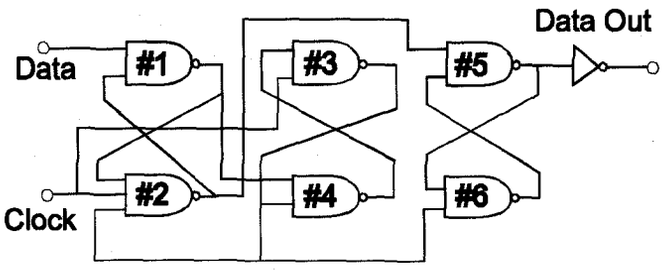

Fig. 4. Circuit diagram of flip/flop both tested with the laser beam and modeled with circuit and device simulator programs.

III. Test Circuits

Two test circuits - SRWOTDCN and EDGE - were used to study the effects of frequency on error rate. Fig. 3a shows SRWOTDCN and Fig. 3b shows EDGE. Both circuits consist of inverters (combinational logic) connected to flip-flops (sequential logic). The flip-flops are basically similar but differ in the following ways; circuit "SRWOTDCN" has a gate length of 1μm and gate widths of a 7 μm, whereas circuit "EDGE" has gate lengths of 0.7 μm and gate widths of about 3 μm; SRWOTDCN has a "clear" function which, for these experiments, is disabled and which is lacking in EDGE; one circuit consists of a single inverter connected to a string of 28 shift registers (SRWOTDCN), whereas the other consists of 16 inverters connected to a single register; and, finally, SRWOTDCN is relatively sensitive to single event latchup (SEL) with a threshold comparable to that for SEU, whereas EDGE, having a different layout, has a SEL threshold considerably higher than that for SEU. In both cases, error rates originating in the inverters were compared with those originating in the latches. Two circuits with different transistor sizes were compared to ascertain whether they differed in their response to dynamic SEU's.

Fig. 4 shows the circuit diagram for the flip-flop. Its operation differs from that of the simple D-latch primarily in that its input is only enabled when the clock transitions from low to high voltage, in contrast to the D-latch whose input is enabled when the clock is at high voltage. A circuit simulator program (SPICE) was used to identify which nodes were sensitive to SEU and when. Nodes 2, 5 and 6 were sensitive to SEU when the clock was at low voltage and nodes 1 and 4 when the clock voltage was high. Just as for the case of the D-latch, voltage transients on the data line caused by ion strikes to the input inverter will only be latched into the flip-flop if they are present when the clock transitions from low to high voltage.

IV. Experiment

The pulsed laser system for SEU measurements has been described in detail in previous publications [7] so that only the briefest description will be included here. The laser had a

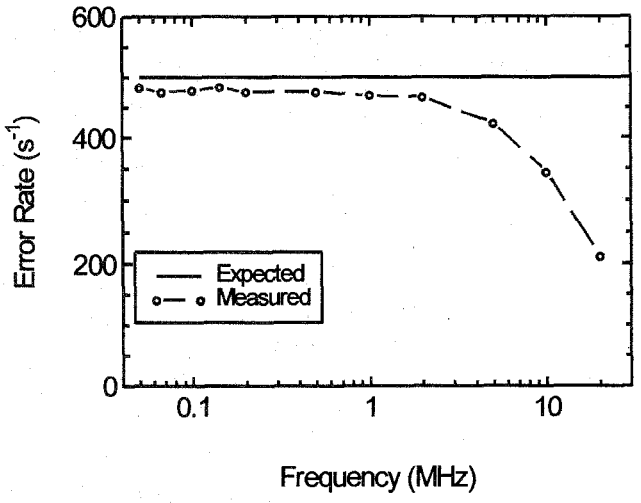

Fig. 5. Error rate as a function of frequency for SRWOTDCN. The straight line is the expected error rate calculated assuming the flip/flop is sensitive 50% of the time.

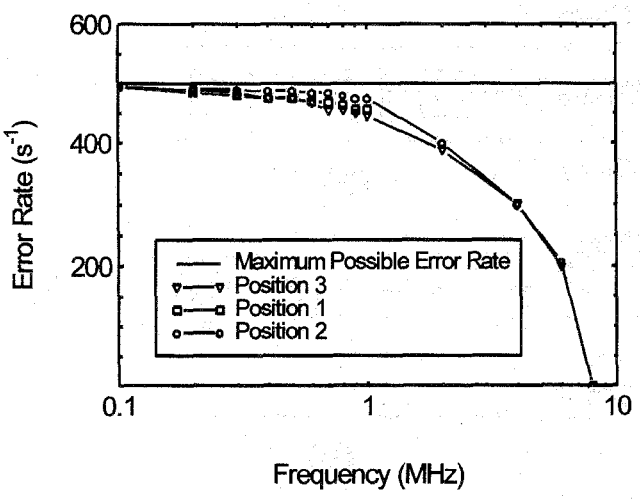

Fig. 6. Error rate as a function of frequency for circuit EDGE at three different locations in the circuit.

pulsed rate of 1 kHz and emitted light with a pulse length of 7 ps and a wavelength of 700 nm, resulting in a penetration depth in silicon of 5 μm. During measurements, "clear" was inactive for circuit SRWOTDCN. Errors in both flip-flops could, in theory, be generated at a number of different nodes, but the occurrence of SEL in SRWOTDCN limited the number of nodes that could be probed. A square wave voltage signal with frequency from DC to 50 MHz was applied to the clock line. No attempt was made to synchronize the pulsing of the laser with the circuit clock because, for these experiments, we found a simpler method - the laser and circuit clock were run asynchronously and the upset rate was measured with a ratemeter. (The ratemeter had a discriminator level of 0.1 V and dead time of 15 ns). This is a relatively straightforward procedure that facilitates the calculation of error rates as a function of frequency, as will be shown in the next section. The output was also connected to an oscilloscope with a bandwidth of 500 MHz used to monitor the time evolution of the output signal. Laser pulse energy was measured by splitting of a portion of the beam and directing it at a photodiode connected to a boxcar integrator.

V. Results and Discussion

Dynamic SEU measurements were made for both circuits in order to compare their SEU responses.

A. Flip-flop

Figs. 5 and 6 show the error rates measured for the flip-flops in both circuits. Results are for node 5 in flip-flop 1, the flip-flop closest to the output in circuit SRWOTDCN, and for nodes 2, 5, and 6 in EDGE. During the measurements of SRWOTDCN, "clear" was inactive and data was kept at 5 V. With a laser pulse rate of 1 kHz, and given that the node is sensitive to SEU's only 50% of the time, the maximum number of errors generated by the laser is 500 counts per second (cps). The actual rates, measured with a ratemeter, fall slightly below the expected values at low frequencies. Above 1 MHz, however, the error rates drop off rapidly with increasing frequency, and above 9 MHz for EDGE and 20 MHz for SRWOTDCN, no more errors are registered on the counter.

These measurements confirm that the error rate in sequential logic is essentially independent of frequency at low frequencies. The rapid falloff at higher frequencies is due to long transients on the data output lines. Evidently, the circuit was not ideal for demonstrating the frequency independence of error rates in sequential logic at frequencies above 1 Mhz. The long time constants are associated with the large capacitances on the output nodes of both circuits. When an upset occurs, the output voltage drops from 5 V to 0 V and remains there until it is reset at the next rising clock edge. Fig. 7 shows the oscilloscope traces for the output transients. If an upset occurs at the beginning of the sensitive time, i.e., when the clock voltage transitions from high to low, the register remains upset for half a clock cycle (500 ns). If the upset occurs just prior to the clock transitioning from low to high voltage, the output begins to upset but then, almost immediately, it recovers. The set of traces observed in the figure are due to the random arrival time of the pulses relative to the clock edge. The slow fall time (500 ns) observed on the oscilloscope accounts for the measured error rate being less than the expected error rate, i.e., if an internal node is upset just prior to the clock edge, there is insufficient time before the clock restores the voltage on the upset node, for the relatively slow transient to fall below the threshold value for which the ratemeter registers an upset. Therefore, upsets that occur just prior to the clock edge will not be counted, and the measured rate will fall below 500 cps. As the frequency increases, the fall time of the output voltage becomes comparable to the time during which the node is

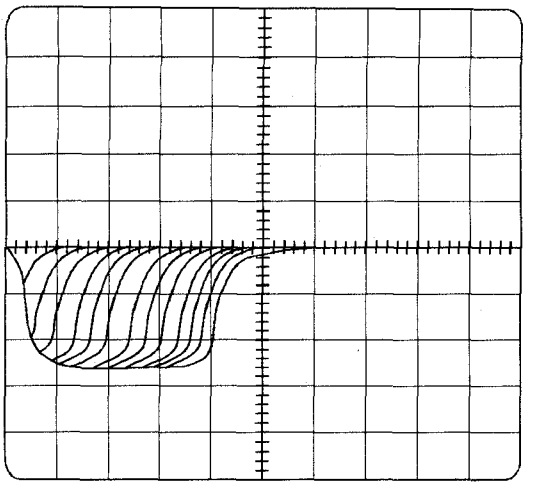

Fig. 7. Oscilloscope traces of the output of circuit EDGE. The vertical scale is 2 V/div and the horizontal scale is 100 ns/div.

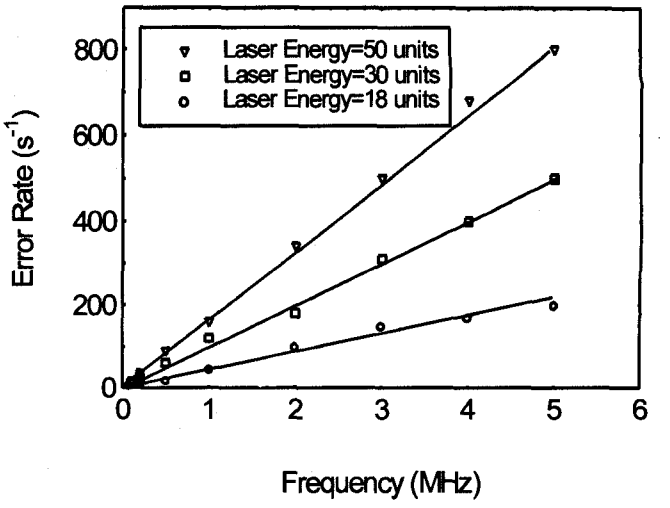

Fig. 8. Error rate as a function of frequency for three different laser pulse energies. The straight lines are best fits to the data. From their slopes one can calculate the window of vulnerability.

sensitive. When this occurs, a larger fraction of the upsets generated at an internal node will not be registered by the ratemeter, and the measured rate will fall far below 500 cps. Above 9 MHz for EDGE and 20 MHz for SRWOTDCN, the sensitive time is shorter than the fall time of the respective outputs, and no upsets are registered by the ratemeter. In summary, the measured error rates in sequential logic are independent of frequency, provided the voltage transients are much shorter than the clock period.

B. Inverter

Figs. 8 and 9 show the error rates measured as a function of frequency for the inverters in the two circuits. The solid lines are best fits to the data and show that, as predicted, the error rate depends linearly on frequency. Based on the discussion in Section II, these measurements confirm that transients in combinational logic can only be latched into registers (resulting in an errors) if they occur when the clock transitions from low to high voltage. Fig. 8 also shows that the slope of the straight line increases with increasing laser pulse energy. The following simple equation shows that the slope of the straight line is related to the time period (T) prior to the clock edge during which the node is vulnerable to upsets:

$$T = \frac{\nu_{error}}{\nu_{clock}} \frac{1}{\nu_{laser}} \qquad (1)$$

where ν_{clock} is the clock frequency, ν_{laser} is the laser pulse rate, and ν_{error} is the measured error rate. Equation 1 shows that, if the error rate increases with increasing laser pulse energy, so does the vulnerable time, T.

Fig. 9 shows that at frequencies above 16 MHz the data for the inverter in EDGE deviates drastically from the straight line. In fact, above 19 MHz errors were no longer registered by the ratemeter. [The relatively small deviations from linear behavior at frequencies below 16 MHz are due to instabilities in the laser, resulting in short-term drift in the laser pulse energy output. The data were not corrected for these variations in energy.] The fact that the circuit ceases to function at 20 MHz, twice the maximum frequency for the register, is also related to the slow changes in the output voltage following an upset. Upsets originating in the inverter are detected up to a frequency twice that for the flip-flop. This can be explained by noting that both upsets in the inverter are reset at the next rising clock edge, which occurs a full clock period later. This was confirmed by observing the oscilloscope which showed a single transient with a width

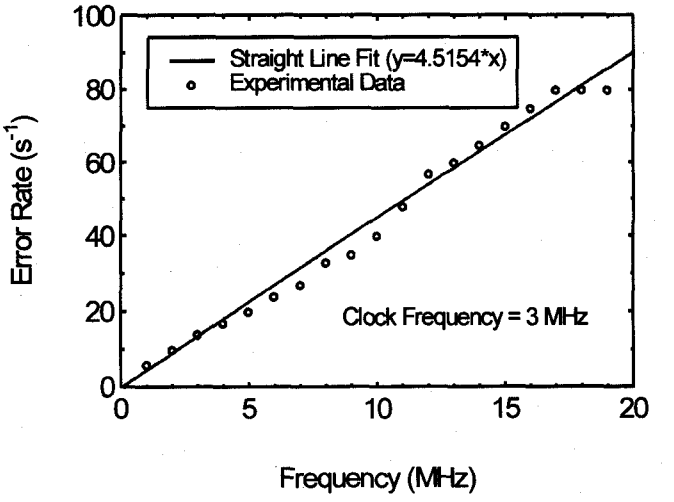

Fig. 9. Error rate for inverter in circuit EDGE. The straight line is a best fit to the data. The data was not corrected for variations in laser power that lead to the deviations from straight line behavior.

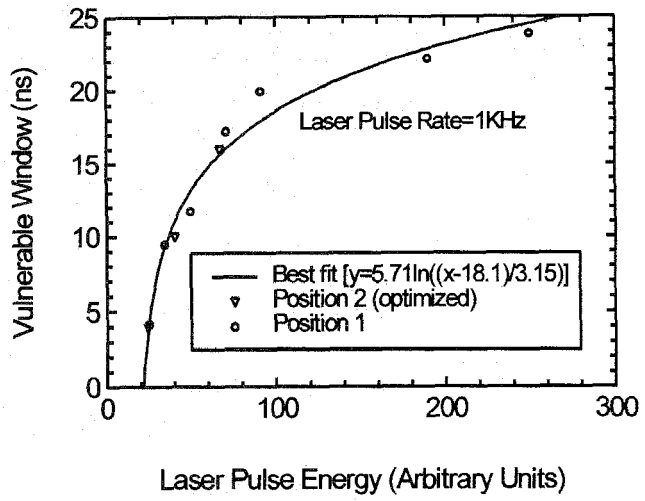

Fig. 10. The window of vulnerability, calculated from equation 1 as a function of laser pulse energy for two different positions near the drain of the "off" n-channel transistor in the inverter of SRWOTDCN.

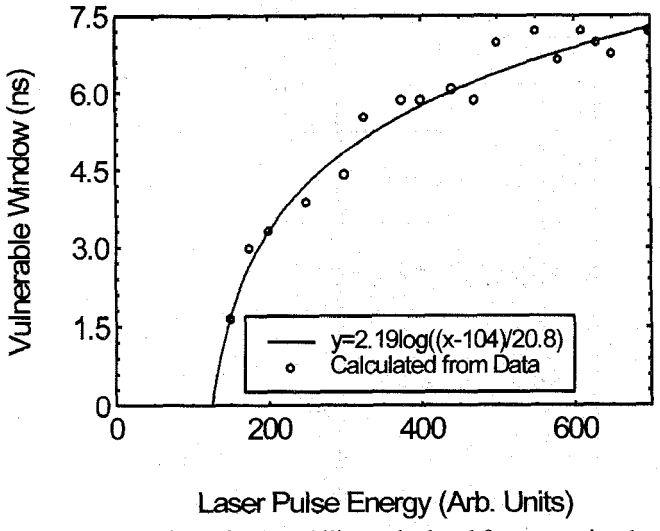

Fig. 11. The window of vulnerability, calculated from equation 1, as a function of laser pulse energy for the "off" n-channel transistor in circuit EDGE.

equal to the full clock period. The full clock period is twice the maximum time interval between upset and reset observed for the flip-flop, which means that the circuit can be run at twice the frequency before the slow decay time prevents the ratemeter from detecting upsets.

Additional measurements were taken on the dependence of error rate on laser pulse energy at low clock frequencies where the results would not skewed by the long time constants of the data output signals. [This is roughly equivalent to measuring the error rate as a function of LET for heavy ions.] The SEU vulnerable time (T) was calculated, using equation 1, as a function of laser pulse energy at a fixed clock frequency and a fixed pulse rate for the laser. Figs.10 and 11 show the dependence of SEU vulnerable time on laser pulse energy. The solid lines are best fits to the data using a logarithmic function. The data for both circuits show that the vulnerable times increase rapidly with laser pulse energy for low energies, but very slowly at high laser pulse energies.

The logarithmic dependence of the vulnerable time on laser pulse energy is a direct consequence of the exponential decay of the voltage on the node being irradiated. From the fits to the data in Figs. 10 and 11, decay times of 5.7 ns and 2.19 ns were obtained for SRWOTDCN and EDGE, respectively. These long decay times are not surprising because the p-n junction, across which charge is being collected, remains reverse biased the entire time. This is different from the case of a latch where the voltage on the irradiated node switches, removing the reverse bias from the p-n junction and resulting in reduced charge collection times.[11] The smaller charge collection time for EDGE is consistent with the circuit having smaller dimensions.

These results lead to an important conclusion: two different circuits containing combinational logic should both exhibit a linear dependence on frequency, but the rate of increase of SEU's with frequency will depend on the "window of vulnerability" which, in turn, depends on the charge collection times at the upset node. The two circuits investigated show vastly different charge collection times. EDGE was designed to operate at higher clock speeds than SRWOTDCN by making its gate lengths shorter. Operating both circuits at the same frequency should result in fewer errors in EDGE for two reasons - the sensitive areas are smaller, and the sensitive times are also smaller. Therefore, neglecting the effects of sensitive area, it is not automatically the case that a faster circuit will have a higher error rate - it will depend partly on the charge collection times.

VI. Modeling Results

A. *Circuit Simulation*

A circuit simulator program (SPICE) was used to confirm the logarithmic dependence on laser pulse energy of the inverter's vulnerable time period around a clock edge. Essential for running the simulations were the SPICE parameters provided by the circuit designers. An SEU was simulated with a current generator connected between the output of the inverter and ground with the input to the inverter held at low voltage. The current generator was characterized by a rapid (0.2 ns) exponential rise time and an exponential decay time obtained from the experiments described in the previous section. The current generator was applied at various times prior to the rising clock edge, and the current amplitude was adjusted to determine the upset threshold. Fig. 12 is a comparison of the experimental data and the calculated results from SPICE. In this figure, we have plotted the vulnerable time along the x-axis, the laser

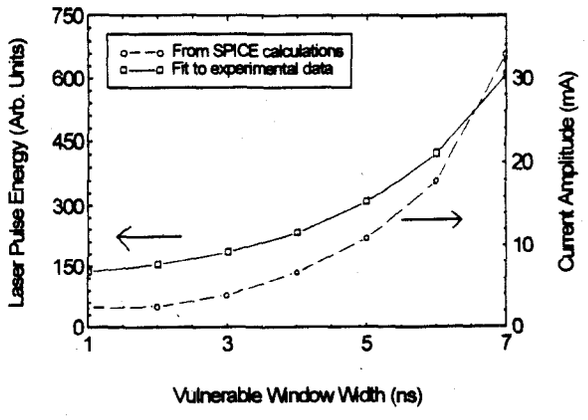

Fig. 12. Comparison of laser pulse energy (experiment) and current amplitude (simulation) necessary for a particular SEU vulnerable window time interval.

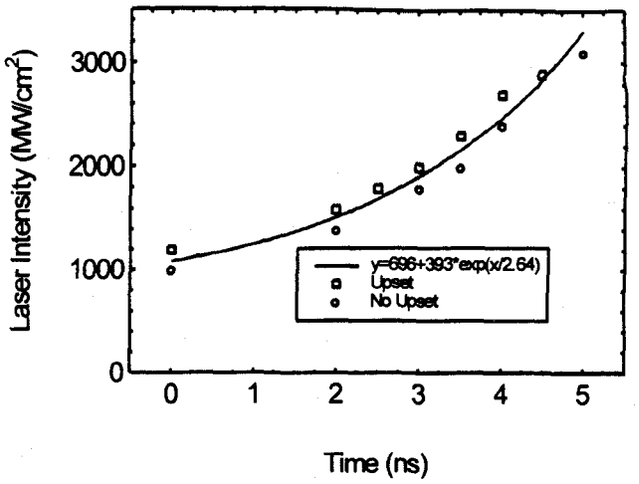

Fig. 13. Laser intensity required to produce an upset as a function of the time between the laser and the clock edge. The solid line is an exponential fit to the threshold values and gives a time constant of 2.64 ns.

pulse energy (experiment) along the left y-axis and the current amplitude (used in SPICE) along the right y-axis. [We make the reasonable assumption that current amplitude is directly proportional to laser pulse energy.] For greater clarity, we have taken the data for the experimental points from the "best-fit" curve rather than the actual data. From the figure, it is obvious that the results obtained from the SPICE simulation do not agree with the experimental data, i.e., even though both curves are based on the same decay time, there are other factors that determine the actual magnitude of the charge collection. This should not be too surprising given the large differences between the simple current model and the actual data obtained using the pulsed laser.

B. *Device and Circuit Simulation*

Another approach that avoids having to use the experimentally obtained charge collection time for SEU's in dynamic logic circuits involves using a computer program "ATLAS" (obtained from SILVACO). It is a "mixed mode" program that includes a 2-dimensional device simulator for modeling the struck transistor, and a circuit simulator (SPICE) for determining, during the course of the upset, the dynamic voltage levels in the remaining circuit elements in circuit EDGE. The physical dimensions of the actual n-channel transistor in the input inverter in circuit EDGE were used. The light beam had a constant intensity both across its 0.4 μm diameter and its 5.5 μm depth. Its rise and fall times were 0.5 ps, which is much shorter than the response time of the circuit.

To obtain the charge-collection time, the arrival time of the laser pulse was varied with respect to the clock edge and the laser intensity was adjusted until the upset threshold could be determined. Fig. 13 shows the dependence of laser pulse energy on the time interval between the arrival of the laser light and the clock edge. The threshold lies between the highest light intensity for upset and the lowest light intensity for no upset. An exponential fit to the upset threshold as a function of $t_{clock} - t_{laser}$ gives excellent agreement, as can be seen in the figure. From the constant in the exponential we obtained a charge collection time of 2.61 ns, which is very close to the experimental value of 2.19 ns obtained with the laser. Therefore, from knowledge of the device and circuit parameters, one can quite accurately predict the charge collection time. That time then gives the width of the SEU-vulnerable window, useful information for predicting the SEU sensitivity of logic circuits. The major disadvantage of the mixed mode program over the simple circuit simulator program is the much longer time required to do the calculation - hours versus seconds.

VII CONCLUSIONS

Using the unique features of a pulsed laser, we have measured error rates in individual elements in logic circuits. The results demonstrate that, at sufficiently low frequencies where the transients are much shorter than clock period, error rates in sequential logic are independent of frequency and in combinational logic are linearly dependent on frequency. The frequency range over which these measurements could be performed was limited by the large capacitances associated with the drive transistors on the data output lines.

From the dependence of the upset rates on the laser pulse energy, it is possible to calculate the time, prior to the clock edge, during which the combinational logic element was sensitive to upsets. That time, which is related to the decay time for the transient voltage on the irradiated node, is shorter for the circuit with smaller dimensions. A circuit simulation program (SPICE) alone was used to model the response of the circuit to a current pulse with exponentially rising and decaying transients. The decay time used in the simulation was obtained from the experimental data.

Although the experimental and calculated results agree qualitatively - both vulnerable times depend logarithmically on deposited energy - there are significant quantitative differences, suggesting that the circuit simulator program alone cannot be used for accurately modeling dynamic SEU's in logic circuits. However, results from a computer simulation of a mixed device and circuit simulators gave very good agreement between calculated and experimental values for the charge collection time.

VIII. REFERENCES

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