Automatic Selective Hardening Against Soft Errors: a Cost-based and Regularity-aware Approach

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***Abstract*—This paper proposes a methodology to automatically apply selective hardening into a circuit based on the *net hardening* concept. Analysis is performed in the profile of a hardening cost function, in order to automatically determine a stop point for the hardening process. Such analysis can be, sometimes, very time consuming, and even intractable for large circuits. In order to overcome such limitation, two approaches are presented and combined in this paper. The first one takes advantage of circuit regularity, while the second limits the scope of the analysis. A set of circuits from the ISCAS85 benchmarks is used as case study. Simulation results demonstrate the effectiveness of the proposed methodology, where substantial reductions of the required computation time are achieved.**

***Index Terms*—Automatic selective hardening, single event effects, soft errors, reliability analysis, fault tolerance.**

I. Introduction

Transient errors in integrated circuits, or soft errors, are an increasing concern due to downscaling-related shifts in circuit's design, such as reduced device feature sizes and lower supply voltages. Soft errors can be caused by different physical phenomena, such as radiation effects, capacitive coupling, electromagnetic interference, or power transients. Radiation-induced soft errors are of great interest, particularly for dependable systems and circuits [1]–[3]. They occur when a radiation event generates enough charge disturbance to cause a switch of the current value in a circuit's element.

In the case of combinational logic, radiation events may lead to the appearance of single event transients (SETs) that, if propagated and latched into a memory element, become errors. In the past, soft errors used to be a concern only in the design of memories, leading to the appearance of error mitigation techniques such as nodal interleaving and error correcting codes. However, the reduced dimensions of the devices together with the reduced operating voltage levels have increased the sensitivity of semiconductor devices to radiation, with resulting error rates approaching those of memories [4]. Further, the probability of multiple transient faults is no longer negligible (due to the reduction of the critical charge and the distance between sensitive junctions, among another factors). Indeed, a single high energetic particle may affect the output of more than one circuit node, causing multiple faults [5], [6].

Several masking phenomena, e.g., electrical masking, logical masking and timing masking, render immunity to combinational logic circuits. Among them, logical masking is the hardest to model and characterize [7]. However, it has the advantage of technology independence. Thus, in this work we focus on calculating the reliability of a circuit by considering only logical masking. Notice that this calculation provides an underestimation of the reliability of a circuit (but never an overestimation). Indeed, errors that are not logically masked may still be filtered out by other masking phenomena.

Soft errors can be mitigated by the properly use of hardening techniques, which are generally redundancy-based. Traditional hardening techniques may require too much area/effort in order to be suitable for commercial use. An attractive alternative is to protect only the most sensitive parts of a design. This alternative, known as *selective hardening*, offers an interesting trade-off between reliability and overhead [7], [8]. Thus, considering logical masking, this work proposes a methodology to automatically apply selective hardening into a circuit based on the concept of *net hardening* [9].

This paper is organized as follows: Section II details the reliability analysis method we have used. Section III explains how candidates are selected for hardening by using cost-based analysis and locality bias. In Section IV we show our results with and without the use of a regularity-aware optimization. Finally, in Section V final remarks and prospects are provided.

II. Signal Probability Reliability Analysis

The reliability of a given circuit is the degree of confidence observed in the outputs of this circuit, considering a scenario in which faults are expected to occur with a given probability [9]. It can be analyzed by many different methods, depending on the type of faults we are interested in. The Signal Probability Reliability Analysis (SPRA) is a method that examines the failure rate of a circuit (i.e., to its ability to mask faults) concerning transient faults [11]. In SPRA, the signal reliability concept is considered, i.e., a given signal is assumed to have a probability to take four different values: correct 0, correct 1, incorrect 0 or incorrect 1. These values are then arranged in probability matrices, which are used to propagate the cumulative effects of faults to the outputs of the circuit. By performing this task, the SPRA method embeds the probability of occurrence of multiple simultaneous faults as well.

The SPRA algorithm is based on the Probabilistic Transfer Matrix approach (PTM) [10]. The main difference being that SPRA has a linear complexity instead of the exponential complexity of PTM. On the other hand, SPRA provides an approximated result for the reliability. The linear complexity

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is fundamental for allowing the analysis later described in this paper. More details of the algorithm can be found in [11].

III. Selective hardening methodology

Typically, digital circuits are designed using standard cells. The circuit is synthesized and later placed. Since one of the goals of placement algorithms is to reduce wirelength, cells that are logically connected have a fair probability of being actually physically adjacent. And, since these cells are close enough to each other, they are susceptible to charge sharing effects. In other words, a single energetic particle is able to cause a strike in two (or more) nearby logic cells [9].

When it comes to assessing the effect of multiple faults in a circuit, a simplistic approach is to perform completely random multiple fault injection. For defect-based analysis such approach might be appropriate, but it is not suitable for single event related multiple faults. Some form of *locality bias* must be applied to limit the faults to certain regions in the circuit. In fact, using random multiple faults may lead to an overestimation of the error rate of a circuit [12].

In this work, the locality bias is given by the concept of *net hardening*, introduced in [9]. Instead of assuming faults in a set of random cells, only cells in the same net are considered. Hardening a net means hardening all the cells that are logically connected to it. This approach is an heuristic, since it simplifies the profile of a real circuit. Nevertheless, such heuristic allows the analysis of synthesized circuits, having no need to analyze the actual layout of the circuit.

That being sad, it is now necessary to perform a correct modeling using SPRA. Such modeling will then allow for choosing the candidates for hardening. First, if we consider that a reliability change of a single cell b_i brings its new reliability to q_i^*, the circuit's reliability R then becomes R_i^*. Because different cells b_i and b_j make different contributions to the reliability of a circuit, changes of different cells may produce different values R_i^* and R_j^* [13].

In our analysis we assume that there is a technique that is able to improve the reliability of a given block b_i, such that $q_i^* = 1$. This is not restrictive since other values are also possible. Selective hardening can be applied by the use of Hardening by Design (HBD) techniques or generic fault tolerance techniques such as Triple Modular Redundancy (TMR). In our experiments we do not define the hardening technique being used, but we assume that a hardened cell is 3 times larger than before. Such value is inspired by classical TMR, given the voter's area is ignored.

Then, for each net of the circuit, we perform a SPRA evaluation run (only possible since the SPRA's complexity is linear). In each run, we select all gates that are connected to the current net, allow q_i^* of each gate to be 1, and obtain the new R value R_i^*. All other gates of the circuit have a q_i value smaller than one, so they introduce faults in the analysis. After all runs are performed, we obtain a list of all R_i^* values (list size is equal to the number of nets). A graphical representation of this is given in Fig. 1, in which it is possible to observe that some nets (the ones in the left portion of the image) are better

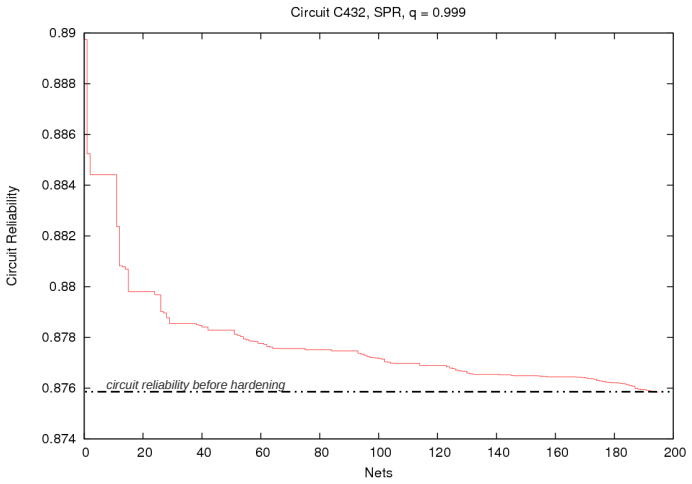

Fig. 1. Reliability gain versus chosen net to be hardened.

candidates for hardening than others. At this point, one could apply a naive approach: sort the list and select the net with the highest R_i^* to be hardened. Nevertheless, we are interested in establishing a trade-off between the cost of hardening these nets instead of any other net. In order to do so, we make use of two parameters to express hardening affinities from both cells and nets: Cha_i and Nha_i. The parameter Cha_i of each type of cell can be used to express any type of hardening trade-off: area, delay, power or combinations of the previous. In Tab. I we show some of the area values that were used in our experiments, which are from an actual 90nm standard cell library [14]. In our analysis, only area was taken into account to calculate the hardening affinity. For each cell we have divided the area of the smallest inverter in the library (INVX0) by the given cell actual area, in order to normalize all the Cha_i values, as shown in Tab. I. The parameter Nha_i defines the affinity of the nets, and is given by the sum of all the Cha_j values, given that j is a cell connected to a net i:

$$Nha_i = \sum Cha_j \quad (1)$$

In order to have a clear trade-off between reliability improvements and hardening efforts, a cost function is used, which takes into account the reliability gain given by Rg_i^*, as well as the net affinity parameter Nha_i:

$$Rg_i^* = R_i^* - R \quad (2)$$

TABLE I
Hardware affinity (Cha_i) parameters for some cells.

Cell	**Area** (μm^2)	Cha_i
INVX0	5.5296	1
NAND2X0	5.5296	1
NOR2X0	5.5296	1
AND2X1	7.3728	0.75
OR4X1	10.1376	0.55
XOR3X1	22.1184	0.25

$$C_i = (Rg_i^*)^{w1}/(Nha_i)^{w2} \quad (3)$$

where $w1$ and $w2$ are weights that allow to choose if reliability should be more important than the hardening effort (or vice-versa), and by which amount. Finally, the net with the highest value of C_i is selected for hardening. When a target reliability improvement has not been reached, then another round is performed to choose the next net for hardening. In our experiments, since the goal is to fully characterize the circuit, net by net, no target is given: the hardening process is repeated until all nets are hardened.

IV. Results

In recent works we have shown how our methodology is effective when it comes to hardening under a certain circuit hardening budget. For instance, in [8] we have obtained improvements in the reliability of a circuit by a fixed target of 20% or 40% and, at the same time, trying to reduce the power consumption. In another recent work [9] we have applied the same *net hardening* bias to obtain savings in circuit area.

The two aforementioned works have a point in common: they require the user intervention to determine the reliability increase target. In order to avoid that, in this work we have analyzed the progressive profile of the cost function, so an automatic stop point of the hardening process can be determined. Our case study circuits are a set of circuits from the ISCAS85 benchmarks [15].

When analyzing the results, two different profiles have emerged. The first profile has a *high peak* near the beginning of the analysis and is represented in Fig. 2. The second profile is more *step-shaped* and is represented in Fig. 3. The illustrations in both figures were obtained using the parameters $q_i = 0.999$ and $q_i^* = 1$. Other combination of values cause slight changes in the plots, i.e., the profile of the function remains the same. In other words, the profile of the function is highly related to the logic masking capabilities and the affinity of nets. The closer a net is to the **y** axis, the better candidate for hardening it is. Both $w1$ and $w2$ were set as 1.

Generating the plots of the cost function requires a long computation time. Every time a net is selected as the best candidate, the order must be re-evaluated since shifts in the selection order are possible and often seen. If we take SPRA alone, it has a linear complexity ($O(n)$) with respect to the number of gates, which is a very positive property of the algorithm. Nevertheless, when we apply it as described in Section III, the execution time also becomes proportional to the number of nets in the circuit ($O(n^2)$, roughly assuming the number of gates and nets is the same, given by n). And since we must re-evaluate all nets once a net is selected, its complexity then becomes bounded by $O(n^3)$.

In order to reduce the execution time we propose two approaches: the first approach is an optimization based on the analysis of the regularity of the circuit and it is described in Subsection IV-A. The second approach is to limit the scope of the analysis to the first elements of the cost function, which

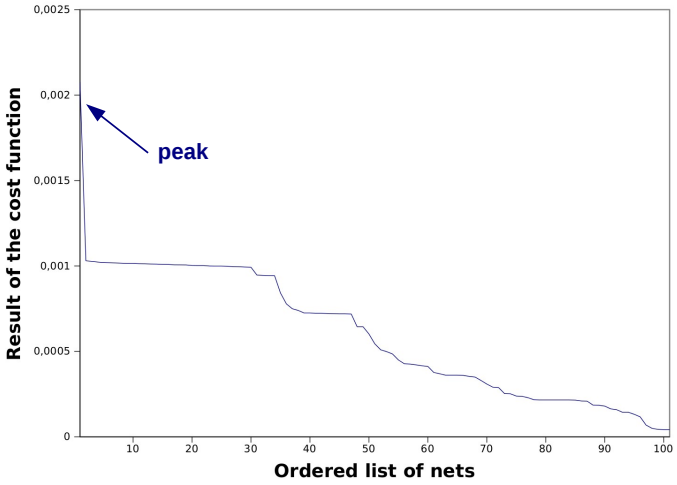

Fig. 2. Reliability gain versus chosen net to be hardened, circuit *c432*.

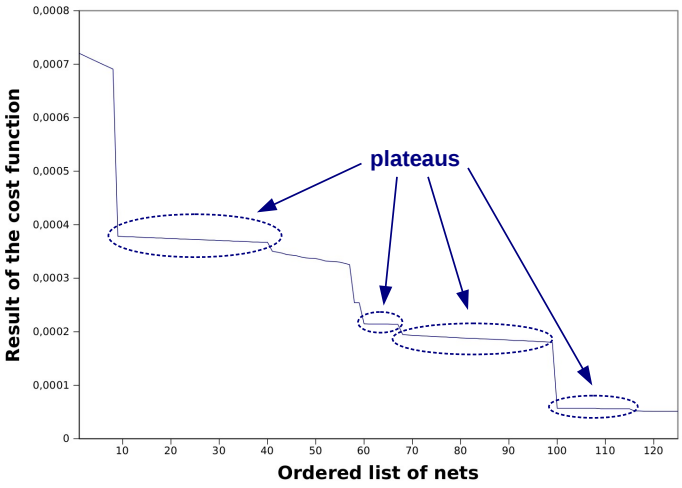

Fig. 3. Reliability gain versus chosen net to be hardened, circuit *c499*.

are the ones that are in fact interesting for selective hardening. This scope limitation is given by a heuristic explained in Subsection IV-B.

A. Optimization

Both analysis in figures 2 and 3 have some *plateaus*, i.e., some areas in which the cost function has a linear decreasing trend. This happens because all the nets that are part of the same plateau are equivalent in terms of both reliability and cost. As a matter of fact, the order in which they are elected for hardening is irrelevant. Thus, we work under the fair assumption that those nets have a similar purpose in the circuit and therefore represent a certain degree of regularity of the given circuit.

From this assumption, once one of these plateaus has been detected, we do not proceed with the analysis of all nets in it. It is possible to save some execution time by estimating the profile of that plateau. Given the number of nets in a plateau is known, as well as the value of the cost function for the first

element outside (after) the plateau, it is possible to plot the corresponding profile.

We applied this optimization to some of the ISCAS'85 circuits. The results are given in Tab. II, in which it is possible to see that some circuits require a long execution time, even with this optimization. In particular, the analysis of the circuit *c1908* has an execution time of more than 9 hours. As predicted by Fig. 3, the analysis of the circuit *c499* is much faster when the optimization is applied.

B. Automatic stop heuristic

Since the first optimization we proposed is still not able to cope with large circuits, we have proposed a second one. This heuristic was defined to create a stop point when the sum of the elements already evaluated reaches a threshold.

Let C_1 be the cost function value of the best hardening candidate. Then, the goal is to find a value j such that $\sum_{i=2}^{j} C_i \leq K \times C_1$, where K is an arbitrary constant. In other words, the threshold is defined as K times the value of C_1. This heuristic can be interpreted as an integral which calculates the area under a curve.

Using a K value of 10, we performed the same analysis as before to the largest circuits in the ISCAS'85 set. The results are given in Tab. III. Notice that the column entitled 'Exec. time' is given in hours and, when a circuit required more than a day to be analyzed, we assumed it to be completely unfeasible and canceled the execution.

V. Conclusions and Future Work

This work presented a selective hardening methodology, which was adapted to *automatically* apply selective hardening into a circuit, based on the concept of *net hardening*. This concept is of great interest because cells that are close to each other are susceptible to charge sharing effects. Thus, by hardening a net, we are protecting the circuit against multiple faults caused by single-event induced charge sharing.

TABLE II
Execution time for determining the cost function profile with a target of 100%.

Circuit	Exec. time (s)	Exec. time with optimization (s)
c17	0.26	0.23
74283	4.78	4.48
c432	1058.71	611.76
c499	263.75	27.33
c1355	5907.91	709.14
c1908	56621.25	33898.49

TABLE III
Execution times for determining the partial cost function profile.

Circuit	Exec. time (h)	Exec. time with optimization (s)
c1355	1.64	15.06
c1908	> 19	477.49
c3540	> 24	2109.85
c2670	> 24	523.56
c5315	> 24	2555.74

However, the computation required can be very time consuming. Because of that, two different approaches were also proposed. The first approach is based on the analysis of the regularity of the circuit, and has achieved reductions in the computation time of up to 89.6% for the case studied circuits. The second approach is based on limiting the scope of the analysis, and has obtained even more substantial results, reducing the computation time from the order of days to minutes for some of the circuits.

As future work we intend to evaluate larger circuits, a task which will require more heuristics and optimizations as the ones already described in this work.

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