From an Analytic NBTI Device Model to Reliability Assessment of Complex Digital Circuits

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***Abstract*—In safety critical applications precise characterization of circuits to predict the lifetime reliability is a key challenge. This paper proposes a reliability assessment tool to model and simulate the NBTI degradation including its recovery effect during the design phase of digital circuits. The model is based on single device models and the corresponding measurement data. The circuits under test can be custom designed on transistor level and/or designed on gate level. The toolset is applied to a test circuit to evaluate its reliability within the lifetime. Considering not only the permanent component of NBTI but also the recoverable part, the tool provides a useful means to prevent an early circuit failure at minimum costs. Our studies support the applicability of the proposed method to efficiently estimate application specific reliability requirements over lifetime.**

I. Introduction

Non-constant field scaling elevated the Negative Bias Temperature Instability (NBTI) to a detrimental concern in modern technologies. Since the 90nm node, it is considered as the predominant cause of device reliability degradation and lifetime limitation. To deal with reliability concerns, state of the art design introduces generous safety margins arising from the worst-case scenario. However, systems used in space, avionic, and biomedical applications require high reliability levels. Therefore, in such applications very conservative safety margins are used, where drift-related parameters severely impact the circuit performance. This results in high waste of power, area and performance [1]. Nevertheless, device degradation is strongly dependent on the circuit structure and workload. Therefore, all devices within a circuit are not aged to the same level. Moreover, for reliability issues with a recovery effect such as NBTI, after the stress is removed, the drift in parameters is partly recovered [2], [3], [4]. As many guard banding approaches consider only the permanent component of degraded parameters under worst case stress, they underestimate the recoverable component of NBTI.

Therefore, accurate prediction of the NBTI effect is still challenging due to its strong recovery characteristic and not only the workload and structure of the circuit, but also the stress and recovery behavior of aging effects need to be taken into account. To encounter the increasing reliability costs and tighten the guard-bands while ensuring reliable operation, a reliability analysis in the early design phase becomes inevitable to predict the timing degradation over the lifetime.

Despite of the known existence of the reliability challenges, there is still a lack of flexible and yet sufficiently accurate analyzing methods on circuit level for digital circuits. Therefore, we propose to predict the timing degradation due to NBTI induced aging with a novel sufficiently accurate model that is capable of analyzing even complex digital circuits when considering both NBTI stress and recovery.

Our proposed approach combines gate level and transistor level approaches to accurately characterize digital circuits with low computational effort compared to transistor level approaches. The approach performs an evaluation of the timing behavior of the digital circuit over the lifetime. The delay and output slope calculations result from a SPICE simulation of an aged netlist. As the physical model is separated from the circuit analysis, integration of updated models for new technologies is highly efficient. Our aging analysis toolset utilizes the NBTI device model and measurement data of [5], in which both NBTI stress and relaxation are regarded. Therefore, the toolset is more accurate than current approaches for aging analysis of digital circuits are considered. In our approach the effect of the recoverable component of NBTI is carefully evaluated. Moreover, the presented approach is applicable on circuit level and can handle even complex digital circuits.

There are several approaches which analyze the impact of aging effects both on transistor and gate level [7], [8]. Commercially available tools on transistor level such as BERT or RelXpert simulate the virgin circuit and store the current and voltage waveforms at the transistor terminals to determine the workload for each transistor. Utilizing those, degraded transistor models are generated and a second simulation with the aged circuit is accomplished. However, such models are only accurate if they describe the degradation of the transistors precisely. Moreover, they are proprietary and not interchangeable by the user. More importantly, such tools are mainly built for the analysis of small analog circuits and are not capable of verifying the timing constraints of more complex digital circuits with thousands of transistors and very different possible stress scenarios.

Modeling approaches on gate level commonly estimate the aged gate delay due to a threshold voltage shift as the sum of the delay of the virgin circuit and the aged delay. However, these models are inaccurate compared to device level models as only one threshold voltage shift per gate is considered and no equation for the aged output slope is provided. Gate level approaches such as [6] use a canonical gate model which provides the aged gate performance for parameter drifts of individual transistors. However, with gate level approaches analysis of custom designed circuits is not possible. Moreover, to efficiently update the aging analysis for new technologies it is advantageous to have interchangeable parameter models. This necessitates separating the physics behind the aging model from the aging analysis toolset. Separating physical model from the aging framework enables to integrate effects

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such as recovery of aging mechanisms into the aging analysis tool. Moreover, it speeds up integrating new developed models for scaled technologies into the aging toolset.

Our proposed approach utilizes the device model of [5] to characterize the digital circuit. It combines both gate and transistor level approaches to provide accurate data regarding the transient behavior of the circuit while decreasing the computational effort compared to transistor level models.
The paper is organized as follows: section II discusses the physical model behind the aging tool. In section III the developed tool is explained in detail. Section IV shows the reliability analysis utilizing the developed aging for a test circuit. Finally, the paper is concluded in section V.

II. The physical NBTI Model

A. Charge Trapping Model and CET Maps

NBTI is nowadays understood as a charge trapping mechanism of defects in the gate stack when a transistor is under stress. In a PMOS transistor where NBTI occures, a captured positively charged defect increases the absolute value of transistor threshold voltage with time. This results in a temporal performance degradation of a gate.
Every defect can exist in two states, a charged (positive) and an uncharged (neutral) state with stochastic transitions between them determined by two time constants. To describe more than one individual defect the Capture Emission Time (CET) map modeling from [5] can be utilized. A CET map describes the distribution of capture and emission times of traps in the gate oxide. Experimentally gathered CET maps for most nitrided gates show that NBTI in general consists of two distinctly different components: A recoverable component *R* and a permanent component *P*. Thereby, we conclude that not only the permanent component is the crucial degradation mechanism determining the lifetime [11], but also the recoverable part is highly crucial in transient reliability assessment. The reason is that in low activity nodes within the circuit toggling with much lower frequencies than the system clock, a temporal (recoverable) increase of $V_{th} - shift$ can be present. As this ΔV_{th} is not recovered to a great extent within the interval of few clock periods, both the frequency dependency and the recoverable component of NBTI has to be considered.
The overall degradation *S* arises from adding the recoverable and the permanent components [9]. Eventually the threshold voltage shift results from integration over all defect energies. The parameter shift increases with time under negative gate bias and at elevated temperature.
The model of [5] distinguishes DC- and AC-stress scenarios. In case of a DC-stress a constant stress voltage is applied to the transistor for a certain time t_{stress} after which the transistor enters recovery for the relaxation time t_{relax}. On the other hand, for AC-stress a periodic pulsed gate source voltage with a constant frequency f_{AC} and duty factor (DUF) is applied to the transistor. The area of integration to determine the threshold voltage shift for an AC-stress scenario is then dependent on the duty factor as well as the period $T_{AC} = \frac{1}{f_{AC}}$.
Compared to a pure DC-stress, a shorter stress time is applied in the AC case and a number of defects can recover. This results in a lower threshold voltage shift depending on the duty factor. Hence, considering AC-stress instead of the worst-case DC-stress will result in a substantially lower prediction of the delay degradation.
However, this assumed periodic stress with a certain frequency and DUF cannot represent signals in digital circuits. Instead, a model is required that deals with diverse aperiodic patterns. This is due to different activity rates of the nodes within the circuit discussed in detail in section III.
Since it is not feasible to track the signal for every PMOS to gather information about this aperiodic behavior, we approximate the workload of a transistor with a statistical approach and adapt therewith aperiodic signal patterns to periodic patterns such that the proposed AC NBTI model of [5] can be applied to estimate the threshold shift.

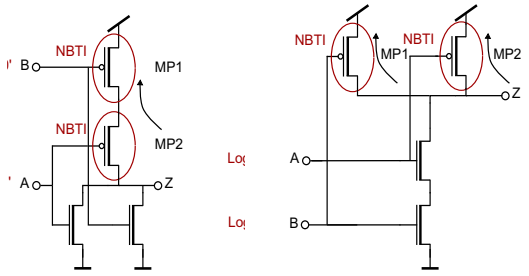

Fig. 1. NBTI degradation of the a) 2-input NOR gate and b) 2-input NAND gate

III. The developed aging toolset

NBTI is strongly dependent on the circuit structure and applied stress pattern and thus workload. Therefore, transistors in the same circuit do not experience the similar stress due to a varying stress pattern. The stress is dependent on the applied inputs and the structure of the circuit, e.g. if PMOS stacking is present. The following describes the developed tool based on the physical device model when considering the circuit structure and the defined use profile.

A. Structural Dependence of Stress Pattern

For multiple input gates the applied input pattern determines if a PMOS transistor experiences NBTI stress or not. This is the case if a multi-input gate contains transistors connected in series, i.e. in a stack. As an example, Fig. 1a shows a simple 2-input NOR gate where two PMOS transistors are in a stack. For transistor MP1, similar to an inverter, if a logic “0” is applied at input A, the PMOS is under stress. However, for transistor MP2 to enter the stress condition, both inputs need to be “0”. As a consequence, either both PMOS transistors are experiencing NBTI stress or just the one connected directly to V_{DD}. Hence, whether the second transistor in series is under stress depends on the input combination [13], [6]. For gates with more transistors in a stack even more cases have to be considered.
However, not for all multi-input gates the states of other transistors need to be regarded. In comparison to the NOR gate, in a 2-input NAND gate (see Fig. 1b) the sources of

all PMOS transistors are tied to the supply voltage V_{DD} and hence V_{GS} is always either $-V_{DD}$ or 0. Therefore, if the input signals are independent, the stress condition for each PMOS is also independent of others.
A varying workload results in a different increase in delay for different gates. This asymmetric delay degradation leads to parts of a circuit being more prone to aging than others.

B. AC NBTI Model for Digital Circuit

Different nodes within a digital circuit might have considerably different activity rates. In other words, not all nodes operate with high frequencies relative to the (high) clock frequency. Therefore, if the gate terminal of a PMOS transistor toggles rarely, the stress pattern applied to this node must be mapped to a much lower frequency than the clock frequency. At lower frequencies the induced ΔV_{th} is increased compared to higher frequencies [14], [15]. Extreme case would be similar to the DC stress pattern. It should be noted that for such low active nodes the recoverable component of ΔV_{th} is the crucial degradation mechanism and plays an important role in determining the transient performance degradation. This can be understood when considering short clock periods in practical applications (frequency in the range of several hundreds of MHz to GHz) compared to time constants of the NBTI recovery phenomena. Fig. 2 shows the ΔV_{th} degradation when applying stress/recovery sequences [16]. Therefore, besides DUF, we propose to consider the activity rate of each node to be able to take the recovery component of ΔV_{th} into account.
For the proposed approximate AC NBTI model, the stress toggle rate at each PMOS gate terminal as well as the duty factor of stress is collected. This information about the activities of all transistors is gathered for a statistically significant number of inputs by the aging tool and is used to map aperiodic input patterns to periodic patterns as expected from the proposed AC model. For large circuits the information about the activities of all transistors is gathered by applying a set of most likely patterns to the circuit.

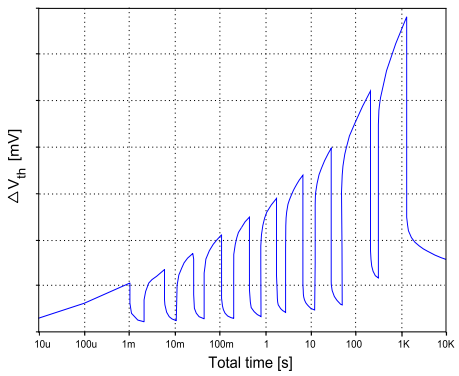

Fig. 2. a) NBTI degradation with an alternating stress-recovery pattern. The stress/recovery sequence is with increasing times [16]

Therefore, the average duty factor DUF_{AV} and the average period T_{AV} over the applied stress pattern seen at a PMOS are calculated. The average duty factor is defined by

$$DUF_{AV} = \frac{NBTI_{stress}}{t_{AC}} \tag{1}$$

where $NBTI_{stress}$ denotes how often the stress condition was fulfilled for a transistor. $t_{AC} = n \cdot T_{clk}$ is the overall stress time where n is the number of applied clock cycles.
As mentioned above, although the frequency dependence vanishes at relatively moderate frequencies [12], it is crucial to consider both frequency dependency and the recoverable component of ΔV_{th} for nodes with low activity within the circuit. For that reason, it is additionally possible to differentiate between different stress shapes which would result in the same duty factor. It is then assumed that one period consists of a stress phase followed by a relaxation phase. The average over all these periods results in

$$T_{AV} = \frac{n \cdot T_{clk}}{n_{stress-relax}} \tag{2}$$

in which $n_{stress-relax}$ specifies the number of stress relaxation cycles and can easily be calculated as half of the number of stress toggles on a certain gate terminal net.
After collecting the statistics for every PMOS and performing the average of these values over the given number of clock cycles constant values are gained for the originally variable stress and relaxation times. With these constant values for DUF_{AV} and T_{AV} the model for a single transistor is applied and an individual constant threshold voltage shift is calculated for every PMOS. This shift is then added to the SPICE netlist as a voltage source in a subcircuit by the proposed aging tool. The clock frequency determines the order of recovery interval after stress for the ΔV_{th}. This enables a transient reliability assessment, preventing an underestimation of the guardbands.

C. Aging Analysis Toolset

To integrate the AC NBTI model into the design flow, a novel aging tool applicable on circuit level was developed (see Fig. 3). The core of the aging tool is the modified analytic AC NBTI model. The aging tool reads in the structural information of a circuit from a SPICE netlist. Two inputs are provided including a fresh netlist and a set of input patterns. The gate level description enables propagating signal values within the circuit which decreases the computational effort. The set of input patterns is chosen either completely random for small modules or is a set of more likely ones for large circuits. The aging tool scans the netlist and establishes two superior levels. First one is the gate level where information about the connections between different logic gates is included, and if the component belongs to a standard library propagates the logic values. This is accomplished by a VHDL description of logic gates. Otherwise, if the component is custom designed the logic propagation is performed on transistor level. By applying the set of input patterns and simulating the logic values on gate level the activity rate at each input pin of each cell is gathered. The second superior level is the transistor level where the device level implementation of the components is listed. In the next step, the desired inputs are applied and propagated through the circuit where the statistics for NBTI stress for the gate terminal and the stress toggle rate for every PMOS transistor are gathered.
Subsequently, the aged netlist will be prepared with parameters for the aging subfunction. For every subcircuit where a transistor experiences a ΔV_{th}, a new equivalent aged subcircuit is written into the netlist. This subcircuit comprises a voltage

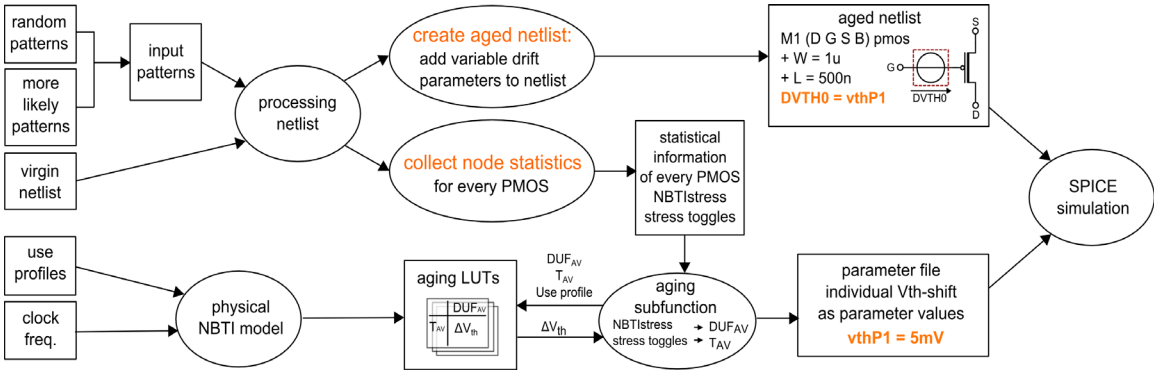

Fig. 3. Data flow diagram of the proposed tool extrapolating aging for circuit lifetime

source at the gate terminal to incorporate the PMOS threshold voltage shift. The ΔV_{th} is then set as an individual parameter for each transistor at the corresponding voltage source. The parameter value of this voltage source is stored in a separate parameter file according to the parameter variable added in the netlist.

Next, a function with the NBTI model for a single transistor reads out the statistical information and calculates the DUF_{AV} and T_{AV} for every PMOS. The corresponding individual ΔV_{th} for every PMOS is obtained from a look-up table (LUT) containing all possible threshold voltage shifts. These threshold voltage shifts are calculated and stored from the approximate AC NBTI model by a sweep over all possible T_{AV} and DUF_{AV} for a certain clock and use profile. For every transistor, the obtained statistical values for NBTI stress and toggle rates result in a specific DUF_{AV} and T_{AV} for which the closest corresponding ΔV_{th} is taken from the table. The table is dependent on T_{clk} and the defined use profile. The defined use profile includes the temperature, V_{stress} and the time span for which a circuit is aged. It is possible to create LUTs for different desired use profiles.

An extrapolation over the desired lifetime is performed and the ΔV_{th} is written into a separate file containing all parameter values. Both the aged netlist and the parameter files are directly taken into an SPICE simulation, with the benefit that the statistics are gathered only once for a statistically reasonable amount of inputs. This is computationally feasible even for big circuits. For other aging scenarios with different use profiles only the parameter file is changed. Furthermore, the simulations retain their simulation speed due to the constant ΔV_{th} and hence no further computational effort is added.

In other words, the developed tool enables reliability assessment of a circuit considering NBTI with a low computational effort and thereby provides a valuable means to predict the lifetime constraints of a circuit. Moreover, the proposed aging tool is able to handle netlists with high level, gate and transistor level components. As an additional feature clock and power gating as used in state-of-the-art low power technologies are included.

As an example, to mimic dangerous scenarios within digital circuits we characterized chains of standard core elements in a 65nm technology. Assume an inverter chain with low activity rate, i.e. the elements are in a steady state for long intervals. With high operating frequencies, the relaxation time would be short and the recoverable part of NBTI has the dominant effect. Thus, for high activity nodes permanent NBTI and for low activity nodes both permanent and recoverable NBTI are considered. A mobile use profile is defined, with accelerated voltage of 105% of $V_{DD} = 1.3$V, temperature $Temp = 85\,^{\circ}$C and 4 years of operation. Table I summarizes the delay increase after this use profile for slow corner with peak $Temp = 125\,^{\circ}$C. The difference between NAND and NOR chain is due to the serial connection of NMOS or PMOS transistors.

In the next section the aging analysis toolset is applied to a safety critical application and the reliability analysis is performed. Here, instead of the mobile phone use case a typical automotive use profile is considered.

TABLE I. DELAY INCREASE IN STANDARD CORE COMPONENTS

	Considering permanent NBTI with periodic AC stress and frequency of 500MHz	Permanent and recoverable NBTI with short recovery time, shortly after steady state of 1h
Inverter Chain	2.3%	7.8%
NOR Chain	2.6%	8.9%
NAND Chain	2.2%	4.6%

IV. TEST CIRCUIT: SHA-1 ALGORITHM

In case of safety critical applications, such as in automotive electronics, system errors due to performance failures are not acceptable as human lives are in stake. Automotive products are designed to operate in harsh environments at high temperatures and for long life cycles. Typical are temperatures of $85\,^{\circ}$C-$175\,^{\circ}$C for a time frame of 10-15 years [17]. Thus, especially long-term parametric variations due to aging become relevant and aging is amplified significantly.

To investigate the possibility of nonuniform aging which results from structural dependence of NBTI, an algorithm heavily used in the automotive sector was synthesized, resulting in a complex digital circuit with several high-level components. This so called Secure Hash Algorithm (SHA-1) was synthesized in an industrial design flow and evaluated in terms of aging. Here, nonuniform degrading paths are detected which can lead to a violation of the timing specifications if the safety margins were underestimated.

SHA-1 is a cryptographic algorithm used to ensure confidential communication between several electronic control units (ECUs) in a bus system to assure that only authentic controllers can be a part of those closed communication

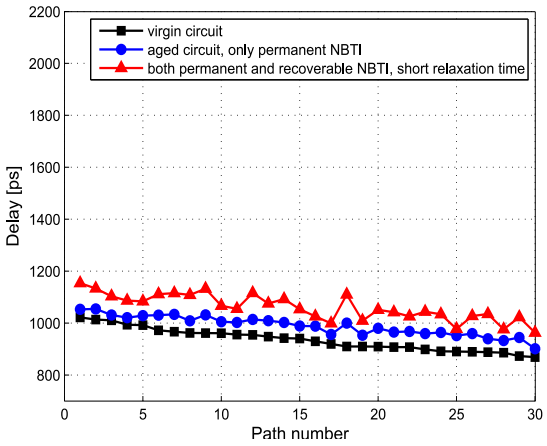

Fig. 4. Delays of the most critical paths for the virgin and the aged SHA-1 circuit, 10 years operation. Performance simulation in nominal process, $V_{DD} = 1.20$V and $T = 125\,°$C

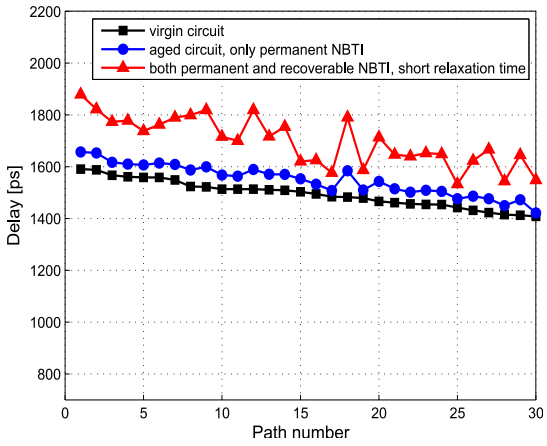

Fig. 5. Delays of the most critical paths for the virgin and the aged SHA-1 circuit, 10 years operation. Performance simulation in slow process, $V_{DD} = 1.05$V and $T = 175\,°$C

groups. Therewith, all vehicular data transmission is encrypted. Any changes in the message will most likely result in a different hash value and the authentication will fail to verify. Hence, only a small change in the message will produce a completely different message digest.

Due to the different components and the algorithm itself, some parts of the circuit are in a steady state for a large number of clock cycles since some signals are constant for these times. Furthermore, the algorithm includes different functionality such that gates can experience a strongly varying workload and hence an asymmetric delay increase. The SHA-1 algorithm was synthesized in a 65nm technology and a clock frequency of 500MHz ($T_{clock} = 2$ns). Clock gating was inherently introduced during the synthesis to reduce the operating power consumption. In this circuit clock gating appears for several registers which have a particularly low switching activity and retain the same value for most of the clock cycles. This also increases highly nonuniform degradation inside the circuit due to inhomogeneous degrading clock buffers.

A. Reliability Assessment of SHA-1

To evaluate the synthesized SHA-1 circuit a typical automotive use profile was chosen. Supply voltage and temperature within the life span are considered 105% of an enhanced $V_{DD} = 1.3$V and $T = 125\,°$C, respectively. The circuit is considered to be under operation for 10 years. The simulations of the virgin and aged netlist are executed at nominal and slow corners. Figure 4 shows the worst case delays of the 30 most critical paths with the highest delay for the virgin circuit. Here, the results of two aging regimes are depicted. In the first regime only the permanent component of NBTI is considered. In the second regime both permanent and recoverable part of NBTI are present. As in the second regime the relaxation time is of the same order of magnitude as the clock period, larger ΔV_{th}s and thus bigger performance change is observed. As can be seen in Fig. 4 assigning different recoverable NBTI shifts for gates with very different activity rates results in nonuniform aging. However, in nominal corner aging does not result in critical operation.

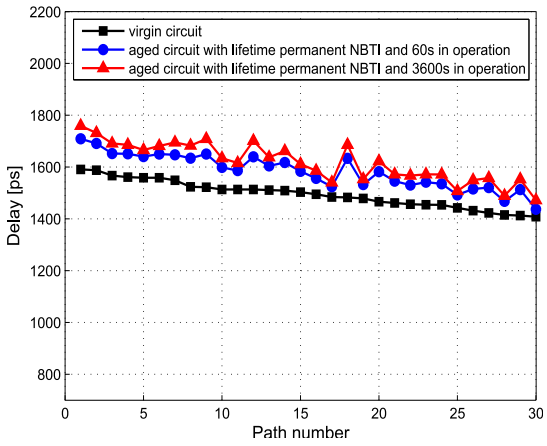

Fig. 6. Delays of the most critical paths for the virgin and the aged SHA-1 circuit, permanent NBTI $NBTI_P$ over 10 years, recoverable and permanent NBTI $NBTI_{P,R}$ for operation times of 60s and 3600s. Performance simulation in slow process, $V_{DD} = 1.05$V and $T = 175\,°$C

Therefore, to take into account PVT variations simulations are repeated for slow corner (Fig. 5). A voltage drop of 150mV and a short time peak temperature of $T = 175\,°$C is considered. Here, large performance degradation is observed. Regarding the setup time of an aged commonly used scan flip-flop at slow corner, a setup time violation occurs resulting in errors at the output of the flip-flop. However, assuming full time circuit operation is not realistic and another regime needs to be evaluated to take care of permanent NBTI over the life span of the circuit and both recoverable and permanent effects under short current operation times after a huge recovery time (Fig. 6). Here, two operating times (60s and 3600s) are considered. The delay degradations are smaller than Fig. 5 but yet considerably larger than only permanent NBTI. The slack is very small and does not provide reliable operation. Table II) summarizes the resulting data for permanent NBTI $NBTI_P$, recoverable and permanent NBTI $NBTI_{P,R}$ after over 10 years. Moreover, it summarizes the simulation results for permanent NBTI $NBTI_P$, recoverable and permanent NBTI $NBTI_{P,R}$ after over 10 years and operation times of 60s and 3600s, respectively.

TABLE II. PERFORMANCE DEGRADATION FOR NBTI, PERMANENT NBTI $NBTI_P$ OVER 10 YEARS, RECOVERABLE AND PERMANENT NBTI $NBTI_{P,R}$ FOR OPERATION TIMES OF 60S AND 3600S

Aging regime	Delay increase
Virgin circuit slow corner	-
$NBTI_P$ 10 years operation	6.9%
$NBTI_{P,R}$ 10 years operation	20.7%
$NBTI_P$ in 10 years operation and $NBTI_{P,R}$ in 60s	10.2%
$NBTI_P$ 10 years operation and $NBTI_{P,R}$ in 3600s	13.7%

To summarize, an accurate evaluation of reliability over lifetime is possible with the developed aging analysis tool. While the delays of the virgin circuit were displayed in a decreasing order, due to the strong asymmetric aging of different paths this is no longer the case for the aged circuit. The recoverable NBTI also needs to be evaluated to identify the potential reliability threats. In our toolset, utilizing a physical NBTI model individual threshold voltage drifts were determined for each transistor. By updating the physical NBTI model for new technologies it is possible to easily update the toolset for scaled circuits and thus integrating new device models for new technologies is highly efficient.. Moreover, by combining gate level and transistor level approaches, the tool gathers activity information on every node within the circuit on gate level and afterwrads utilizes the physical NBTI model on transistor level to determine the threshold voltage drifts. Therefore, the tool is more accurate than the gate level approaches and is capable of handling both custom designed and complex synthesized digital circuits with low computational effort compared to the transistor level approaches.

V. CONCLUSIONS

A novel aging tool was developed which is applicable on circuit level and able to extrapolate the aging induced ΔV_{th} over the lifetime of a digital circuit. The tool considers state-of-the-art design techniques like clock or power gating. Besides the NBTI permanent parameter shift, recovery and frequency dependence of the NBTI are modeled. Thus, the tool is able to detect momentarily performance degradation due to the recoverable component of NBTI. As a test case, the aging toolset is used to analyze the reliability of a safety critical circuit during its lifetime. With the developed tool, it is possible to detect asymmetrically aging paths which experience a different amount of stress and thus age with different speeds. Therefore, the proposed aging tool provides a useful means to encounter generous guard-bands as determined by a worst-case approach while preventing an early circuit failure. Moreover, the elaborated aging tool can be used to determine the weak spots of the circuit to be used for reliability methods such as in-situ monitoring or component replacements.

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REFERENCES

[1] N. Pour Aryan, G. Georgakos, and D. Schmitt-Landsiedel “Reliability monitoring of digital circuits by in situ timing measurement,” in International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2013.

[2] C. Yilmaz, L. Heiss, C. Werner, and D. Schmitt-Landsiedel ,”Modeling of NBTI-recovery effects in analog CMOS circuits,” in IEEE International Reliability Physics Symposium (IRPS), pp. 2A.4.1-2A.4.4, 2013.

[3] C. Ma, H. Mattausch, M. Miyake, T. Iizuka, M. Miura-Mattausch, K. Matsuzawa, S. Yamaguchi, T. Hoshida, M. Imade, R. Koh, T. Arakawa, and J. He, “Compact reliability model for degradation of advanced p-MOSFETs due to NBTI and hot-carrier effects in the circuit simulation,” in Reliability Physics Symposium (IRPS), 2013 IEEE International, pp. 2A.3.1-2A.3.6, 2013.

[4] A. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. Alam, “Recent issues in negative-bias temperature instability: Initial degradation, field dependence of interface trap generation, hole trapping effects, and relaxation,” in Electron Devices, IEEE Transactions on, 54(9):2143-2154, 2007.

[5] T. Grasser, P.-J. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, and B. Kaczer, “Analytic modeling of the bias temperature instability using capture/emission time maps,” in Proceedings of the IEEE International Electron Devices Meeting (IEDM), pp. 618-621, 2011.

[6] D. Lorenz, G. Georgakos, and U. Schlichtmann, “ Aging analysis of circuit timing considering NBTI and HCI,” in Proceedings of the IEEE On-Line Testing Symposium (IOLTS), pp. 3-8, 2009.

[7] S. Khan, S. Hamdioui, “Modeling and mitigating NBTI in nanoscale circuits,” in IEEE 17th International On-Line Testing Symposium (IOLTS), pp.1,6, 2011.

[8] H. Luo, X. Chen, J. Velamala, Y. Wang, Y. Cao, V. Chandra, Y. Ma, H. Yang, “Circuit-level delay modeling considering both TDDB and NBTI,” in 12th International Symposium on Quality Electronic Design (ISQED), pp.1, 2011.

[9] T. Grasser, B. Kaczer, P. Hehenberger, W. Goes, R. O’Connor, H. Resinger, C. Gustin, and C. Schluender, “ Simultaneous extraction of recoverable and permanent components contributing to Bias-Temperature Instability,” in International Electron Devices Meeting (IEDM), pp. 801-804, 2007.

[10] T. Grasser, “ Stochastic charge trapping in oxides: from random telegraph noise to bias temperature instabilities,” in International Reliability Physics Symposium (IRPS), pp. 39-70, 2011.

[11] T. Grasser, T. Aichinger, G. Pobegen, H. Reisinger, P. Wagner, J. Franco, M. Nelhiebel, and B. Kaczer, “The permanent component of NBTI: composition and annealing,” in Proceedings of the IEEE International Reliability Physics Symposium (IRPS), pp. 605-613, 2011.

[12] H. Reisinger, T. Grasser, K. Ermisch, H. Nielen, C. Gustin, and C. Schluender, “Understanding and modeling AC BTI,” in Proceedings of the IEEE International Reliability Physics Symposium (IRPS), pp. 597-604, 2011.

[13] S. Kumar, K. C., and S. Sapatnekar, “ NBTI-aware synthesis of digital circuits,” in Proc. IEEE Design Automation Conference (DAC), pp. 370-375, 2007.

[14] C. Liu, P. Ren, R. Wang, R. Huang, J. Ou, Q. Huang, J. Zou, J. Wang, J. Wu, S. Yu, H. Wu, S.-W. Lee, and Y. Wang, “ New observations on ac NBTI induced dynamic variability in scaled high-k metal-gate MOSFETs: Characterization, origin of frequency dependence, and impacts on circuits,” in Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 19.5.1-19.5.4, 2012.

[15] S. Desai, S. Mukhopadhyay, N. Goel, N. Nanaware, B. Jose, K. Joshi, and S. Mahapatra, “ A comprehensive ac / dc nbti model: Stress, recovery, frequency, duty cycle and process dependence,” in Reliability Physics Symposium (IRPS), 2013 IEEE International, pp. XT.2.1-XT.2.11, 2013.

[16] H. Reisinger, T. Grasser, W. Gustin, and C. Schluender, “ The Statistical Analysis of Individual Defects constituting NBTI and its Implications for Modeling DC- and AC-Stress,” in Proceedings of the IEEE International Reliability Physics Symposium (IRPS), pp. 7-15, 2010.

[17] M. Wolf and C. Weimerskirch, A. Paar. Secure in-vehicle communication. Springer, 2006.