Soft Error Susceptibilities of 22 nm Tri-Gate Devices

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***Abstract*—We report on measured radiation-induced soft error rates (SER) of memory and logic devices built in a 22 nm high-k+metal gate bulk Tri-Gate technology. Our results demonstrate excellent single event upset (SEU) scaling benefits of tri-gate devices. For cosmic radiation, SEU SER reduction levels of the order of $1.5\times - 4\times$ are observed relative to 32 nm planar devices, while for alpha-particles, the measured SEU SER benefit is in excess of $10\times$. Similar improvements are observed for Tri-Gate combinational logic and memory array multi-cell upset (MCU) rates. Reduced SER (RSER) device SER performances (relative to standard, non -RSER devices) are on par or better than that of tested 32 nm planar devices. Finally, a novel, efficient SER reduction design called RTS is introduced.**

***Index Terms*—FinFET, radiation, soft error, soft error rate (SER), single event effect (SEE), Tri-Gate.**

I. Introduction

MULTI-GATE FETs, such as FinFETs and Tri-Gate FETs have long been advertised as the most promising candidates to extend CMOS scaling [1], [2]. It is well known that these non-planar device architectures are characterized by better short channel behaviors due to enhanced electrostatic control from the multiple gates. However, little is known on the single event (SE) sensitivities of these novel multi-gate devices. Recently, El-Mamouni *et al.* [3], and Fang and Oates [4] have reported on measured charge-collection efficiencies of bulk tri-gate devices compared to those of Si on insulator (SOI) devices and on simulated soft error rates (SER) compared to those of planar devices, respectively. Laser and heavy-ion testing of Tri-Gate devices manufactured at IMEC indicated that the sensitive area (i.e., sensitive volume SV) for charge collection in bulk FinFETs is significantly larger than the actual fin's structure, increasing the probability of single event upsets in the cell [3] (see Fig. 1). The tested devices are characterized by large drain areas that explained the increased charge collection. In contrast, Fang and Oates' TCAD simulations indicated that bulk Tri-Gate devices might show soft error rates that are $\sim 15\times$ lower in terrestrial radiation environments than those of planar bulk devices manufactured in a planar CMOS process [4]. The main objective of this paper is to demonstrate the real, measured SER benefit of memory and logic devices built in a high volume manufacturing (HVM) Tri-Gate technology. Specifically, we are comparing measured soft error rates of SRAMs, latches and combinational logic manufactured in a 22 nm, high-k and metal gate (HKMG), bulk CMOS Tri-Gate technology to results of equivalent devices built in 32 nm and older planar technologies [5], [6].

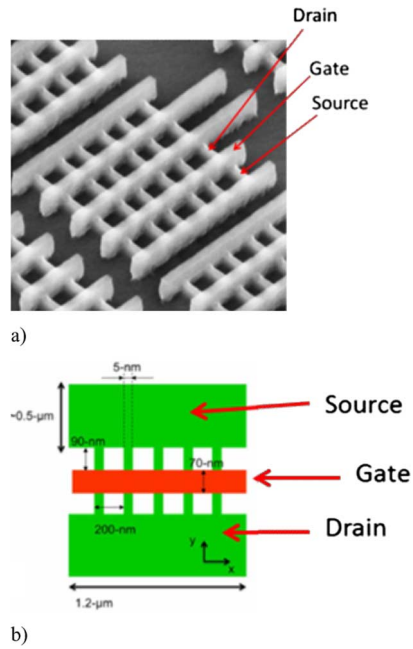

Fig. 1. (a) Intel Tri-Gate transistor [6] (b) FinFETs tested and characterized in [3]. Note the large difference in relative source and drain junction areas.

II. Experimental Setup and Test Structures

A. Experimental Setup

Accelerated high-energy proton beam testing was conducted at the Indiana University Cyclotron Facility (IUCF) and broad beam neutron testing at LANSCE (flight path ICE2-4FP30R). Accelerated alpha-particle upset rates were collected in-house using thorium-232 foils. All accelerated testing was conducted on flip-chip packaged SRAMs (proton testing), or on wire-bonded logic devices (alpha-particle testing). For alpha-particle testing, the full interconnect stack was not processed in order to increase the number of upsets observed in accelerated Th-232 testing (see discussion below). Further, never more than 1 board was exposed to the beam to preclude any changes in the beam flux energy distribution. All testing was conducted in compliance with JEDEC JESD89A [7].

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TABLE I
SUMMARY OF TESTED DEVICES AND RADIATION ENVIRONMENTS REPORTED ON IN THIS WORK

Test Chip	Radiation Environment			Description
	IUCF	LANSCE	Th-232	
SERSL	32+22nm	32+22nm	32+22nm	Latches: Diff.A & Qcrit dependence
SERSM	22nm	22nm	22nm	Selected library elements (FFs and latches)
SERRC	22nm	22nm	None	RSER latches (SEUT, RCC and RTS)
SRAM	32+22nm	32+22nm	None	6T SRAM array; SBU and MCU
SERCL	32+22nm	22nm	None	Combinational Logic

B. Test Structures

An overview of all investigated test structures and collected data reported on in this work is given in Table I. The test chips (TC) listed in Table I are described at a high level below.

SRAM Test Structures: High density flip-chip 6T SRAM devices, each consisting of many tens of millions of bits, were exposed. Single-bit upset (SBU) and multi-cell upset (MCU) statistics were collected and results are summarized in this work. SRAMs were continuously read out[1] to be able to differentiate between 2 or more SBU and MCU.

Sequential Structures: Each test chip contains tens of thousands of instantiations of several flavors of sequential elements each, all chained together in a shift register fashion [8]. Up to 22 chips per board were tested per experiment. Similarly, on the design reported in [8], standard and reduced SER (RSER) latches and flip flops (FFs)[2] were tested under static testing conditions. The tested nominal standard latches (SERSL and SERSM; Table I), whose SER has not been reduced by design, cover a wide design parameter range in terms of critical charges (Qcrit) and junction areas (diff.A). In the case of SERSL, additional reverse biased NMOS and PMOS diffusion is added to state nodes to calibrate the diffusion area dependence of our compact SER models [8]. Great care has been taken to equalize the critical charges among the different flavors of SERSL. This simplified characterization (and model fitting) of the different NMOS and PMOS charge collection properties (at the same Qcrit and same junction areas).

SER benefits of RCC (Reinforcing Charge Collection) and SEUT (Single Event Upset Tolerant) devices (for a detailed description, see [9]), and a novel design we call RTS (Reverse TriState), were characterized under various radiation environments (RSER; Table I). In RTS devices the clock and data input signals of the clock gated feedback tristate gate are swapped such that the clock inputs connect to the transistors closest to the power rails (see Fig. 2). This configuration eliminates both of the internal tristate nodes from contributing to the device SER. SEUT devices utilize local redundancy schemes (interlocked node duplication) as described in detail in [9]. In the case of RCC, Qcrit is increased by minimizing the separation of node pairs that reinforce the state of a cell by simultaneously collecting charge deposited by a single event (SE) [9].

[1]Reading out 1 full TC content takes about 10 sec.

[2]In the remainder of this extended abstract we do not differentiate between latches and FFs and refer to all sequential elements as latches.

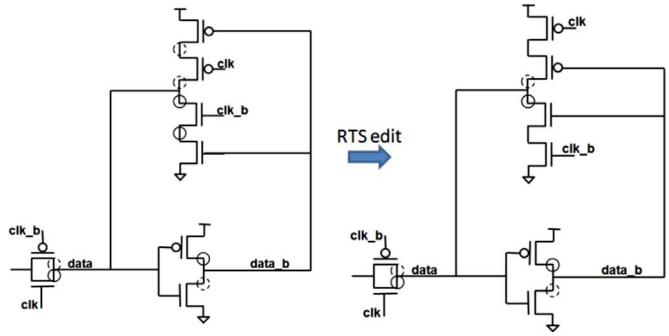

Fig. 2. Schematic change for RTS device is shown. Circles show vulnerable diffusions before and after the RTS edit.

Combinational SER Test Vehicles: These structures were tested at speed. Minimum and maximum clock frequencies depended on power supply voltage conditions and were approximately 50 MHz up to 2 GHz. Our 22 nm test chip design is very similar to the 32 nm version described in [10], and consists of data path blocks, error detection and counter logic, clock generators (ring oscillators) and shift registers for shifting out upset counts after irradiation. In the 22 nm version of this test chip we implemented the capability to stop the clock entirely, which enabled us to measure and subtract out errors that occurred due to strikes of non-combinatorial data path nodes.

III. RESULTS AND DISCUSSION

In the first section the correlation of neutron soft error rates versus high energy proton cross sections (CS) is discussed. Detailed testing results and trends are discussed next. All error bars shown in this work reflect 90% confidence intervals. Alpha-particle SER data are normalized to an effective alpha-particle flux of 0.001 a/cm^2/hr. Please note that this value is applied for comparison purposes only (32 nm to 22 nm results). The effective flux in actual products is estimated to be much smaller than this value [11].

A. High Energy Neutron SER vs. Proton Cross Sections

Proton facilities such as IUCF are more accessible[3] and offer higher beam fluxes than most high energy neutron facilities. Collecting all SER data needed for verification and model calibration purposes can easily take several months of testing in case of a broad neutron beam facility such as LANSCE for instance. That is particularly true for RSER devices. Our strategy therefore is to collect neutron data for a limited set of selected devices and for a limited set of operating conditions and use those results together with proton CS taken on the same parts to establish a proton CS to neutron broad beam SER correlation factor. This is typically done once or twice for each technology generation. Fig. 3 depicts the normalized correlation factor results for one particular study on 22 nm devices. Going forward, the weighted average correlation factor is applied to all proton cross section results. The weighted average of the correlation factor (CF) is computed using

[3]In terms of beam availability.

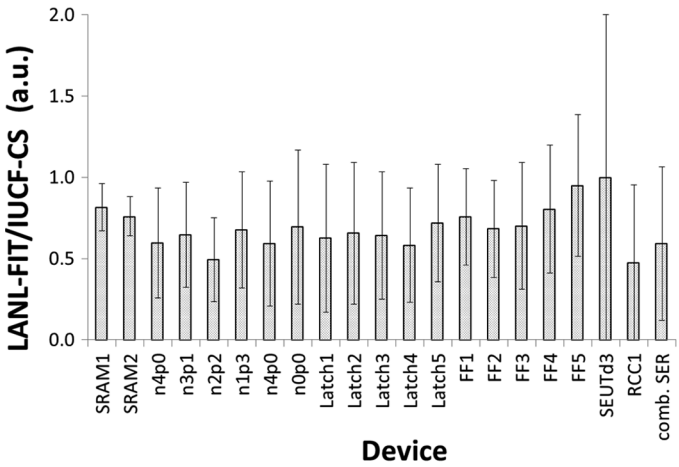

Fig. 3. Calculated correlation factors (CF) and the corresponding 90% confidence intervals for various measured devices. Correlation factor CF corresponds to LANSCE neutron FIT divided by 198 MeV proton cross sections collected at IUCF. Dotted line denotes the weighted average CF.

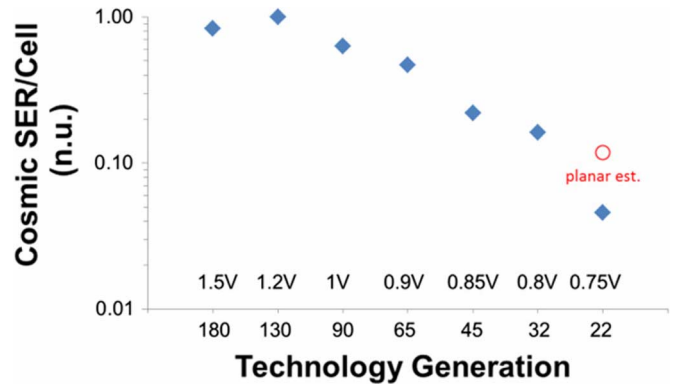

Fig. 4. Measured upset rates of 6T SRAM cells induced by high-energy cosmic radiation, plotted as a function of technology generation. SER of planar 22 nm SRAM cell shown is estimated by simple extrapolation from the 45 nm to 32 nm trend.

$$\mathrm{CF} = \frac{\sum_{k=0}^{n}\left[\frac{\left(\frac{\mathrm{LANL-SER}}{\mathrm{IUCF-CS}}\right)}{\sigma_{\mathrm{CF}}}\right]_k}{\sum_{k=0}^{n}\left[\frac{1}{\sigma_{\mathrm{CF}}}\right]_k} \qquad \text{(eq.1)}$$

where σ_{CF} denotes the 90% confidence interval of the calculated correlation factors.

The average CF is within the 90% confidence intervals of all measured devices, which includes a very broad range of device types: 6T SRAM cells, latches, FFs, nominal and reduced SER devices and combinational test structures (Fig. 3). Not surprisingly, devices with low upset rates (such as SEUT devices) have the largest correlation factor uncertainties.

While Fig. 3 only refers to SBU results, a good correlation between proton and neutron-induced MCU has been demonstrated by the authors in a previous publication (45 nm SRAMs; [12]). Our 22 nm measured data are consistent with our published 45 nm results and conclusions.

It is important to note that LET spectra and the corresponding device responses cannot be expected to be perfectly identical for a broad neutron beam and 198 MeV protons. Any actual differences in conversion factor CF are most probably masked by statistical uncertainties involved in the data collection process.

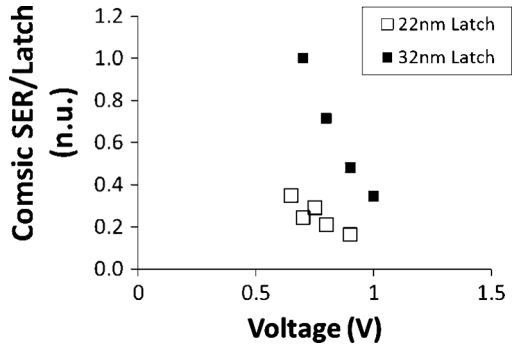

Fig. 5. Voltage dependence of upset rates of 32 nm planar and 22 nm Tri-Gate latches.

However, our detailed study underlines that for the broad class of investigated devices and within the given experimental uncertainties (which are mainly limited by the count statistics of the neutron broad beam results), proton cross sections and neutron induced FIT rates can be described by a consistent conversion factor CF. Consequently, in the remainder of this work we do not differentiate between proton CS or neutron FITs[4] and refer to upset rates induced by either 198 MeV protons or LANSCE neutrons as "Cosmic SER". In all cases a combination of neutron and proton results have been applied in the analysis (typically neutron data are collected for a subset of conditions and proton data cover the whole set). Please note that no testing was performed at proton energies other than 198 MeV.

B. SRAM and Non-RSER Sequential Results

Fig. 4 demonstrates that Tri-Gate technology provides a significant reduction in SE sensitivity. For the bit-level SRAM Cosmic SER trend shown, Tri-Gate devices at the 22 nm node yield a $\sim 3.5\times$ reduction in SER compared to SRAM devices built in a 32 nm bulk, planar CMOS technology. The marker labeled "planar estimate" reflects the estimated upset rate of a planar 22 nm 6T SRAM device. We estimate the Tri-Gate technology SER benefit equals about 2–$2.5\times$ relative to a planar SRAM device at the same technology node. Please note that this estimate is highly speculative. The 45 nm $->$ 32 nm SER scaling factor was applied to the measured 32 nm SRAM upset rates.

Since memory arrays built with 6T SRAM devices are typically protected by parity or error correcting codes (ECC), the Tri-Gate SER performance of frequently used sequential elements is more important. Fig. 4 depicts the voltage dependence of the SER of a typical standard latch built in a 32 nm planar process and 22 nm Tri-Gate process, respectively. Voltage slopes of 22 nm devices and 32 nm devices are very similar[5].

While 22 nm SRAM cells show a $3.5\times$ reduction relative to 32 nm cells, Tri-Gate SER performance of latches and other logic devices varies. Fig. 6 plots latch cosmic SER ratios of 32 nm to 22 nm for $1- > 0$ transitions (NMOS dominated) and $0- > 1$ state transitions (PMOS dominated) as a function of reverse biased junction area. Each pair of chart bars in Fig. 6 reflects results for one latch flavor implemented in our

[4]FIT: Failure In Time, which equals number of upsets per 1 billion hours of operation.

[5]Scaled to the same maximum value, both curves are almost perfectly on top of each other.

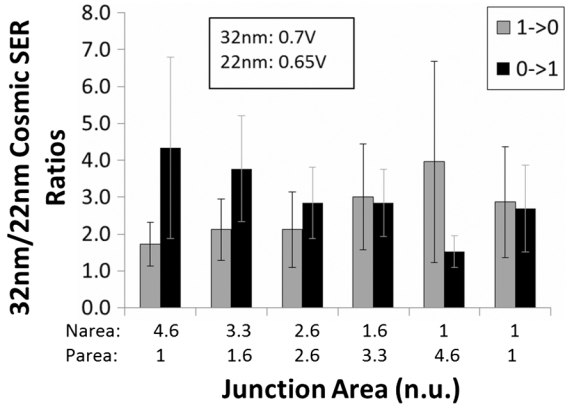

Fig. 6. Ratio of measured cosmic SER of 32 nm planar devices to equivalent 22 nm Tri-Gate ones. Narea and Parea denote normalized relative reverse biased junction areas of various latch types tested (SERSL; see Table I).

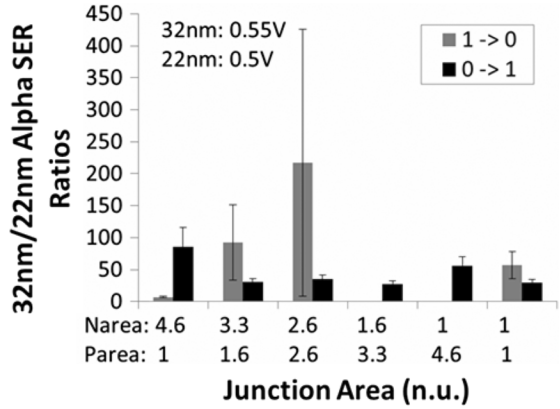

Fig. 7. Ratio of measured alpha-particle induced SER of 32 nm planar devices to equivalent 22 nm ones.

SERSL test chip. For instance, the leftmost device has a relative Narea (reversed biased NMOS junction area) of 4.6 and Parea (PMOS junction area) of 1, implying maximum NMOS and minimal PMOS junction areas. The latches implemented on SERSL are simple D-type transmission gate latches where additional reverse biased diffusion (NMOS or PMOS) was added on the feedback node [8]. Critical charges across latches within one technology generation are approximately the same with the exception of $(\mathrm{Narea},\ \mathrm{Parea}) = (1,1)$ latches, which have a $\sim$40% lower Qcrit than the other flavors. It is worth mentioning that the results of the (1, 1) latch are very characteristic of the soft error response of production latches.

Fig. 6 results demonstrate[6] that latches show 32 nm to 22 nm SER improvement values ranging between $\sim 1.5\times$ up to $\sim 4\times$ on average (per transition). In general and independent of the junction type (NMOS or PMOS), the larger the junction area, the smaller the SER benefit when compared to equivalent 32 nm devices[7]. In other words, the more fins, the higher the charge collection efficiency and the smaller the SER benefit. Most devices implemented in products have areas well below 4.6 area units and the overall cosmic SER benefit in components is expected to be of the order of $2-3\times$ relative to 32 nm planar devices. The root cause of this fact as well as the impact of the fin topology are subject to future investigations.

Fig. 7 depicts alpha-particle induced upset rate ratios for the same 32 nm and 22 nm SERSL devices whose cosmic SER ratios are shown in Fig. 6. We would like to emphasize again, that with the exception of the $(\mathrm{Narea},\ \mathrm{Parea}) = (1,1)$ device, Qcrit values of all device flavors are identical within $\sim$10% for the same state nodes as confirmed by circuit simulations on extracted netlists. The first key observation from these results is that SER benefits for alpha particles are significantly larger than the benefits for cosmic radiation (compare Figs. 6 and 7). 22 nm Tri-Gate devices show a $\sim 10-300\times$ lower SER than those of equivalent 32 nm planar devices. For a typical latch $(\mathrm{Narea},\ \mathrm{Parea} = 1,1)$ the SER reduction equals about $50\times$. It is important to note that the observed difference in soft error sensitivity is an intrinsic transistor property since the BEOL thicknesses of both tested technologies are approximately the same (difference not significant in our accelerated testing), and the Th-232 foils were the same in all experiments.

As mentioned above, only a partial metal stack was used for accelerated alpha particle testing in order to maximize the alpha-particle induced upset rates[8]. Testing on full stacks was performed, but even after weeks of testing no upsets were detected in many cases. For the very same reason accelerated alpha-particle testing was conducted at lower voltages than in case when the 32 nm to 22 nm cosmic SER ratio was investigated.

Fig. 7 underlines that no clear trend in alpha-particle SER ratios with reverse biased junction area is observed, in contrast to ratio results induced by cosmic radiation as shown in Fig. 6. The root cause for this observation is currently being investigated. Please note that in all cases (for 22 nm and 32 nm NMOS and PMOS reverse biased junction areas), SER increases approximately linearly with diffusion junction area.

The findings by Fang and Oates are consistent with alpha-particle SER but clearly too optimistic for the dominating contribution due to cosmic rays [4].

Accounting for measured low susceptibility of 22 nm Tri-Gate devices to alpha particles relative to 32 nm planar devices, and the fact that 45 nm SRAM devices show an alpha-particle SER of well below 10% of the neutron SER at the sea-level [11], we conclude that alpha-particle SER has become negligible in the tested 22 nm Tri-Gate technology[9]. Therefore, in the remainder of this paper solely cosmic SER is discussed.

If a radiation event deposits sufficient charge, more than a single device or bit may be affected, creating a so-called multi-cell upset (MCU) as opposed to a single bit upset (SBU). Scaling is known to increase the fraction of MCU clusters relative to SBU, with important implications for future memory architectures in systems utilizing ECC. If the size of a radiation-induced multi-cell cluster is larger than the memory interleaving distance, detected unrecoverable errors (DUE), or even silent data corruption (SDC) can occur. This is why it is important to fully

[6]22 nm accelerated testing was conducted at 50 mV lower power supply voltages to account for the fact that products designed and manufactured in this technology would be operating at a lower voltage than equivalent 32 nm parts.

[7]The error bars in Fig. 6 account for the uncertainties involved in CF (Fig. 3), which is conservative. Just looking at proton cross sections or LANSCE soft error rates alone gives equivalent trends with error bars smaller than the observed differences in cross sections or SER for different junction area flavors. We therefore believe the trend is real.

[8]Th-232 foil is placed on top of the interconnect stack for accelerated SER testing [7].

[9]This conclusion is based on simulation results that take into account the full stack thickness and material composition.

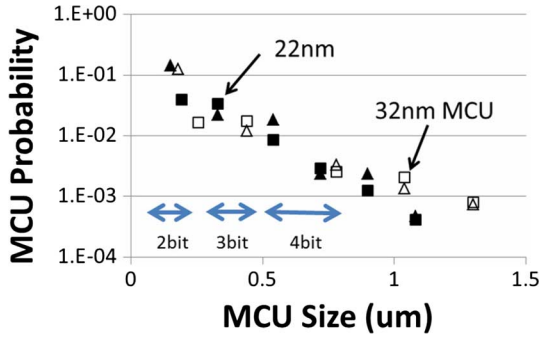

Fig. 8. Measured cosmic radiation-induced MCU probabilities are plotted as a function of maximum MCU cluster size. Triangles denote solid data patterns and squares checkerboard patterns. Bit sizes refer to maximum 22 nm MCU clusters sizes in bits (along BL or WL).

TABLE II
SER REDUCTION AT 0.7 V FOR VARIOUS RSER TYPES. SEUT DENOTES SEUT DEVICES WITH SAME SEPARATION OF SUSCEPTIBLE STATE NODES IN 32 nm AND 22 nm TECHNOLOGIES

	SER Reduction	
RSER Type	**22nm**	**32nm**
RTS	1.9x ± 0.2x	NA
RCC (tested cell includes RTS in case of 22nm)	6.3x ± 1.9x	3.8x ± 1.1x
SEUT	37x ± 23x	17x ±10x

characterize MCU probabilities for the radiation environments of interest.

While SRAM SBU shows a clear impact of Tri-Gate technology, relative MCU probabilities are approximately in line with 32 nm planar results (Fig. 8). Data plotted in Fig. 8 equal the conditional probability that a MCU cluster of size x in micron is formed by the 198 MeV proton beam[10], given that a SBU occurred during the same run[11]. It is worth mentioning that MCU probabilities denote MCU event probabilities and not the fraction of upset bits in MCU clusters relative to SBU bits (which may be larger). MCU cluster sizes reflect maximum sizes in any direction (maximum dimension in BL, WL or diagonal[12]). Runtimes were sufficiently short such that neighboring upsets[13] due to more than one proton or neutron strike are negligible. For more details on our MCU data collection methodology please see [12]. Tri-Gate devices collect less charge than planar ones, but the probability to share charge across nodes and devices is apparently not impacted by the new technology and mainly depends on physical separation. However, it is important to emphasize that overall MCU probabilities remain low at 22 nm when compared to 32 nm and even older technologies [13]. On an absolute SER scale, 22 nm 6T SRAM MCU soft error rates for the same arrays size and cell pitches are $\sim 3.5\times$ lower than equivalent 32 nm ones. This is because MCU probabilities are conditional ones specified relative to SBU probabilities and upset rates.

[10]Reference [12] shows that for 45 nm SRAMs MCU upset rates are equivalent for LANSCE neutrons and 198 MeV protons.

[11]In other words, the plotted MCU probabilities approximately equal the MCU cluster rate (as a function of size x) divided by the (pure) SBU one measured in the same run. Plotted data summarize results collected during many runs.

[12]In the investigated technologies MCU upset probabilities are very symmetrical along BL or WL directions (for the same distances or sizes).

[13]Neighboring is defined as upsets within a radius of 1.5 micron (in either WL or BL direction). The total number of SBU detected equals less than 0.001% of the total number of exposed bits on our SRAM test chips. The 2 bit MCU probability is less than 20% of the SBU one (see Fig. 8).

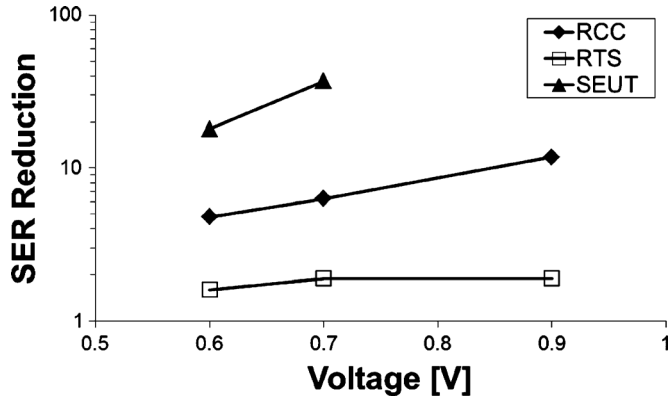

Fig. 9. 22 nm RSER device voltage trends. SEUT at 0.9 V not available due to poor statistics.

TABLE III
POWER, AREA AND TIMING COST OF EACH OF THE RSER TYPES AT THE CELL LEVEL

	Power	Area	Delay
Std. Latch	1	1	0ps
RTS	1.05	1	+2ps
RCC	1.15	1.15	+5ps
SEUT	2	2	+10ps

C. RSER. Results

Without ECC or parity error detection schemes in logic portions of a chip, a reduction in SER can be achieved with the use of more robust cells (in this work called RSER devices). In some cases, simple design modifications can change the sensitivity to soft errors by making the total susceptible node area smaller (RTS) or by increasing Qcrit on sensitive nodes (RCC).

The results listed in Table II demonstrate that 22 nm RSER devices show equal or better SER improvements[14] compared to 32 nm planar technology. Table II specifies RSER SER reduction values in comparison to upset rates of standard latches of the same drive strengths.

Clearly, SEUT and RCC schemes are still viable mitigation schemes at the 22 nm technology node. We observe similar or even better SER performances at comparable cost relative to 32 nm devices. Fig. 9 shows the voltage dependence of the SER reduction of RCC and RTS latches. RTS latches are less sensitive to voltage changes. The fact that SER benefits diminish with reduced power supply voltages for SEUT and RCC devices is consistent with our observation reported on in [9]. State weakening node pairs typically have large separations in space (to reduce cell SER), but at lower voltages (i.e., lower Qcrit), the probability to collect sufficient charge at these state weakening node combinations increases and, therefore, SER are higher too [9].

Table III Summarizes power, area, and delay increase of each of the RSER types at the cell level. As expected, increased SER reduction incurs higher costs.

[14]Reduction in SER relative to non-RSER reference devices (i.e., to a "standard" latch).

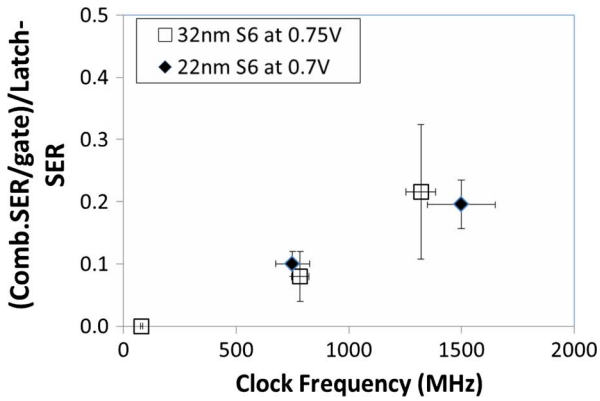

Fig. 10. Measured 32 nm and 22 nm combinational cosmic SER per logic gate expressed as a fraction of latch SER is plotted as a function of clock frequency. Data shown are for paths with skewed, not balanced, N/P ratio devices.

D. Combinational Circuit Results

Combinational logic is different in that radiation induced glitches do not constitute single event upsets, but radiation-induced noise, or single event transients (SETs). However, if the glitch is captured by a receiving storage element it becomes a SEU.

As mentioned in the Section II.B, an improved version of the combinational test chip described in detail in [10] was implemented on a 22 nm test chip (SERCL) to investigate the susceptibility to SETs. The test chip contains several flavors of data paths: N0, N2, N6, S0, S2, S6. This is different from the 32 nm version, which implemented S10, S6, N10 and N6 paths. N6 is a nominal P/N transistor width ratio inverter chain with a length of 6 inverters. Similarly, N2 has 2 nominal inverters in the chain and N0 data paths consist of only the collecting logic network of XNOR, NAND, and NOR gates [10]. S6 has 6 skewed P/N ratio inverters in the chain, and S2 has 2 skewed inverters, and S0 has no inverters. The inverters in the skewed paths are skewed by adjusting the P/N ratio to allow for better SET propagation. The P/N (or N/P, alternating scheme) transistor width ratio is about $4\times$ higher for the skewed devices when compared to the balanced ones. The balanced inverters have close to equal low and high transition times and the corresponding P/N ratios are much closer to devices typically implemented in products. All inverters in the data path sections are minimum sized inverters to maximize SET generation rates. 10 inverter paths were dropped in the 22 nm version of the combinational TC, mainly because our 32 nm data strongly indicated that SETs do not propagate more than 4–5 gates at the investigated conditions.

In contrast to the 32 nm version, the 22 nm implementation allows for running experiments with the clock completely turned off. This makes subtracting out errors not induced in logic gates along the data paths much easier. For neutron or proton irradiation this turns out to be an important correction factor. For instance, $\sim$430 upsets were observed in S6 for a total fluence of 5×10^{12} 198 MeV protons at 1400 MHz and 0.7 V. At the same fluence and conditions, $\sim$110 upsets were detected when the clock was turned off. These upsets originated in the receiving FFs and RSER counters. S0, which contains no additional inverters, yielded at 1400 MHz $\sim$90 upsets and with the clock turned off $\sim$100 detected errors. Therefore, the clock tree seems to be very robust[15]. Our TIDEST[16] simulations [14] confirm that the counter combinational SER and receiver FFs contribute the most upsets besides the data path inverters. In the 32 nm analysis [10], the non-data path contribution was estimated by extrapolating the SER to 0 clock frequency. This is the main reason for the large error bars in the 32 nm data (Fig. 10).

TABLE IV
RATIO OF MEASURED TO SIMULATED (TIDEST) COSMIC SOFT ERROR RATES

Vcc (V)	Frequency (MHz)	S6-Errors	S2-Errors	S0-Errors
0.7	60	0.45	1.00	2.13
0.7	700	0.37	0.58	1.60
0.7	1350	0.32	0.69	0.69
0.95	90	0.87	1.58	1.68
0.95	1020	0.53	0.91	1.12
0.95	2000	0.46	1.20	1.00

The SER performance per logic gate (with skewed N/P ratios), expressed as a fraction of the SER of a typical latch is shown in Fig. 10 for the investigated 32 and 22 nm technologies. Clock frequency dependence is, as expected, linear. For skewed paths, 32 nm and 22 nm show similar susceptibilities. Similarly to MCU results, this means that in terms of absolute upset rates, combinational SER of 22 nm logic devices (with skewed P/N ratios) is in average $2-3\times$ lower than that of equivalent devices implemented in a 32 nm bulk, planar technology.

Balanced N/P ratio data path upset rates are in the noise margin of our experiments for the 22 nm test chip. In the 32 nm version a non-zero result was obtained, but it is not clear whether those are real and indeed above the noise floor. Therefore, similarly to the 32 nm work, we rely on simulations to estimate the 22 nm combinational SER susceptibility of devices with balanced N/P ratios. 22 nm accelerated testing results of skewed paths serve as a verification tool that TIDEST simulations [14] are a suitable replacement of measured results. Table IV compares measured 22 nm SERCL SER results for skewed paths to TIDEST simulation results. Calibrated 22 nm compact models[17] have been used in the simulations. On average TIDEST simulations are $\sim 2\times$ overestimating combinational SER. Please recall that 90% confidence intervals of measured S6 path results are of the same order of magnitude ($\sim$50%) and even larger for paths with fewer inverters (i.e., S2 and S0). We conclude that TIDEST results are a good metric and suitable replacement of measurement results of balanced paths.

Next we would like to shed some light on the combinational SER trend with respect to sequential SER for more realistic, N/P-balanced paths. As mentioned above, we entirely rely on TIDEST type simulations to estimate this trend. Table V summarizes SERCL path simulation results relative to receiver soft error rates (in %). For a 6 inverter balanced path, the total cosmic

[15]This is not a surprise given the large devices and node capacitances attached to the clock tree.

[16]TIDEST stands for TIme DEpendent Softerror Tool. All simulations are conducted on the circuit level as outlined and explained in great detail in [10] and [14].

[17]Calibrated using measured SER results from a large number of memory elements (FFs, latches, RFs, SRAM cells).

TABLE V
SIMULATED (TIDEST) COSMIC SOFT ERROR RATES OF INVERTER CHAIN PATHS (BALANCED N/P DEVICES), EXPRESSED AS A PERCENTAGE OF SIMULATED RECEIVER LATCH SER

Fclk (MHz)	Vcc (V)	N2 SER/Latch (%)	N6 SER/Latch(%)
61	0.7	0.31	0.53
694	0.7	3.57	6.01
1366	0.7	7.02	11.83
88.6	0.95	0.18	0.28
1016	0.95	2.05	3.25
2000	0.95	4.03	6.40

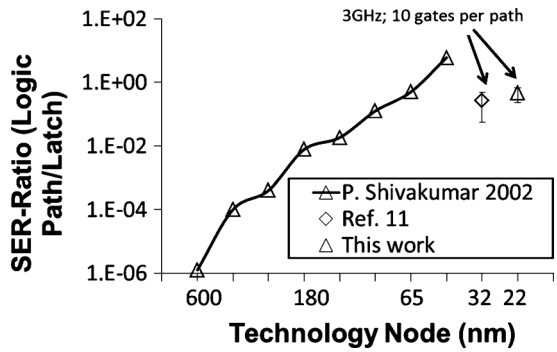

Fig. 11. Comparison of 22 nm Tri-Gate cosmic combinational logic SER to published results and projections.

combinational SER equals about 10% at 1400 MHz (including the SER of the collecting circuitry; see Fig. 2 in [10]).

For a 10 inverter chain, our simulations project a total combinational SER contribution that equals approximately 45% of the receiving sequential SER at 3 GHz and 0.7 V. This is slightly higher than the value we estimated for 32 nm ($<\sim 30\%$ at a 50 mV higher voltage), but within the error bars of both results. We conclude that in the worst case 22 nm Tri-Gate technology shows a very modest increase in combinational SER relative to sequential SER, but in terms of absolute FIT, the combinational SER for the same path length decreases significantly. Overall, 22 nm combinational SER remains well below what Shivakumar and Co. projected more than 10 years ago [15] (Fig. 11).

IV. CONCLUSION

Alpha-particle and cosmic ray induced SER benefits of 22 nm high-K and metal-gate bulk Tri-Gate devices have been measured and compared against equivalent devices manufactured in a 32 nm, planar bulk CMOS technology.

Our key findings are:

1) For high energy neutrons and protons a SER reduction of the order of $1.5\times$ to $4\times$ is observed for SRAMs and sequential elements. 22 nm MCU probabilities are consistent with 32 nm ones and in terms of absolute upset rates decrease by $\sim 3.5\times$.
2) Alpha-particle SER benefits are even higher (in excess of $10\times$). These results and real-time testing results of 45 nm devices lead us to conclude that alpha-particle SER has become negligible in the investigated technologies.
3) Combinational SER per sequential receiver SER might show a modest increase for 22 nm paths, although the difference to 32 nm results is within error bars. Similarly to MCU results, in terms of absolute upset rates, combinational SER is decreasing in 22 nm.
4) 22 nm RSER devices show similar or larger SER benefits relative to non-RSER ones than 32 nm ones. Since non-RSER upset rates are decreasing in terms of absolute SER, RSER device SER is also decreasing correspondingly. A novel design technique called RTS is introduced that shows SER benefits of the order of $2\times$ with extremely low area and power overheads.

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REFERENCES

[1] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, and R. Chau, "Tri-gate fully-depleted CMOS transistors: Fabrication, design and layout," in *Proc. IEEE Symp. VLSI Technol. Dig. Tech. Papers*, 2003, pp. 133–134.

[2] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," in *Proc. IEEE Symp. VLSI Technol. Dig. Tech. Papers*, 2006, pp. 50–51.

[3] F. El-Mamouni, E. X. Zhang, N. D. Pate, R. D. Schrimpf, R. A. Reed, K. F. Galloway, D. McMorrow, J. Warner, E. Simoen, C. Claeys, A. Griffoni, D. Linten, and G. Vizkelethy, "Laser- and heavy ion-induced charge collection in bulk finFETs," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2563–2569, Dec. 2011.

[4] Y. Fang and A. S. Oates, "Neutron-induced charge collection simulation of bulk finFET SRAMs compared with conventional planar SRAMs," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 4, pp. 551–554, Dec. 2011.

[5] P. Packan *et al.*, "High performance 32 nm logic technology featuring 2nd generation high-k+metal gate transistors," in *Proc. IEEE Int. Electron Devices Meeting Tech. Dig.*, 2009, pp. 1–4.

[6] C. Auth *et al.*, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. IEEE Symp. VLSI Technol. Dig. Tech. Papers*, 2012, pp. 131–132.

[7] *Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices*, JEDEC Test Standard 89A, Sep. 2006.

[8] P. Hazucha, T. Karnik, S. Walstra, B. Bloechel, J. Tschanz, J. Maiz, K. Soumyanath, G. Dermer, S. Narendra, V. De, and S. Borkar, "Measurements and analysis of SER tolerant latch in a 90 nm dual-Vt CMOS process," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2003, pp. 617–620.

[9] N. Seifert, V. Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, and A. Balasubramanian, "On the radiation-induced soft error performance of hardened sequential elements in advanced bulk CMOS technologies," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2010, pp. 188–197.

[10] B. Gill, N. Seifert, and V. Zia, "Comparison of alpha-particle and neutron-induced combinational and sequential logic error rates at the 32 nm technology node," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2009, pp. 199–205.

[11] N. Seifert and M. Kirsch, "Real-time soft-error testing results of 45 nm, high-K metal gate, bulk CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, Dec. 2012, presented at NSREC 2012, submitted for publication.

[12] N. Seifert, B. Gill, K. Foley, and P. Relangi, "Multi-cell upset probabilities of 45 nm high-k+metal gate SRAM devices in terrestrial and space environments," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2008, pp. 181–186.

[13] F. X. Ruckerbauer and G. Georgakos, "Soft error rates in 65 nm SRAMs-analysis of new phenomena," in *Proc. IEEE Int. On-Line Testing Symp.*, 2007, pp. 203–204.

[14] N. Seifert, "Radiation-induced soft errors: A chip-level modeling perspective," *Foundat. Trends® in Electron. Design Autom.*, vol. 4, no. 2–3, pp. 99–221, 2010.

[15] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Proc. IEEE Depend. Syst. Netw. Conf.*, Jun. 2002, pp. 389–398.