Neutron-Induced Multiple Bit Upsets on Dynamically-Stressed Commercial SRAM Arrays

P. Rech, J-M. Galliere, P. Girard, A. Griffoni, J. Boch, F. Wrobel, F. Saigné, and L. Dilillo

***Abstract*—We investigate the occurrence of Multiple Bit Upsets in commercial SRAMs of 4Mbits and 32Mbits when irradiated with neutrons. The devices were irradiated at TSL facility with QMN beams of energies from 50MeV to 180MeV. Experimental data demonstrate that the dynamic-stress increases SRAMs sensitivity as well as MBUs occurrence for both the memory types. We also show that both SEU and MBU cross section may depend on memory architecture and memory utilization.**

***Index Terms*—SRAM, Soft Error Rate, Multiple Bit Upset**

I. Introduction

IONIZING particles may produce different kind of errors in any electronic device even at sea-level. High-energy and thermal neutrons generated by the interaction of cosmic rays with terrestrial atmosphere and alpha particles emitted by chip package materials may affect the correct functionality of commercial electronic devices [1-3].

In this scenario, memory density is approaching over 90% of System on Chip (SoC) silicon area in the next few years as confirmed by the SIA Roadmap [4]. Therefore, memories are becoming the main responsible of the overall SoC error rate.

Some hardening techniques have been designed in order to reduce the impact of radiation-induced errors in SRAMs. For example, the physical structure of bit-cell transistors can be strengthened against radiation enlarging the critical nodes capacitances, adding a lightly doped epitaxial layer on the wafer or putting a triple-well underneath the n- and p-well tubs [1]. Although these hardening strategies may significantly reduce the sensitivity of SRAM cells, some of them may also affect the device performances and definitely increase the chip manufacturing cost. On the other hand, system-level or software strategies can be used to reduce the impact of cells corruption in the system functionality. These strategies include Parity Check, Cyclic Redundancy Check (CRC), Error Detection and Correction Code (EDAC), etc. The efficiency of these codes is usually strictly related to the redundancy that they introduce. In fact, both area and computational overheads may be necessary to generate a code that meets the requested reliability in terms of detected or corrected errors.

The codes applied to memory arrays are able often to detect and/or correct no more than one error per word. This choice is made to limit the introduced overhead and it is commonly considered as an acceptable trade-off between costs and benefits. If the memory is exposed to a sufficient high flux of ionizing particles for a sufficient time, two particles may corrupt different bits inside a word. To prevent errors accumulation from corrupting more bits then the code is capable of detecting/correcting, memory scrubbing (i.e., content refresh) can be performed [5]. The scrubbing frequency is dictated by the expected radiation-induced error rate of the device in its particular application.

With the continuous shrinking of transistor dimensions, it may be possible, for one single particle, to interact with more than one cell. Thus, the probability of having more bits simultaneously corrupted by the same particle is increasing, as demonstrated for technology nodes under 130nm [6][7]. In the occurrence of Multiple Bit Upsets, memory scrubbing or single error detection/correction codes may result ineffective, and the memory unreliable particularly for safety critical applications like the biomedical, automotive or avionic ones. The latter is of particular interest for the radiation community as aircrafts normally fly at altitude close to 12 km over sea level, where a maximum of ionization was measured [8].

In this contest, we performed this study in the framework of the HAMLET project. The target of this project is the measure of the radiation-induced error rate on electronics, at high altitudes. This paper intends to analyze the occurrence of MBUs due to neutrons in memory arrays and to evaluate the impact of the array architecture in the radiation-induced error rate. To do so, we performed experiments at TSL facility in Uppsala, Sweden, with neutron beams of energies ranging from 50MeV to 180MeV. We analyze MBU occurrences in 4Mbit and 32Mbit commercial SRAMs. This, on one side, allows us to evaluate which device architecture is more prone to experience MBU and, on the other, demonstrates that traditional static and dynamic tests may not be sufficient to measure an accurate MBU cross section. In fact, as we will detail, defects or asymmetries introduced in the device fabrication stages may increase the sensitivity of the SRAMs especially when stressed. In a previous study, based on SPICE

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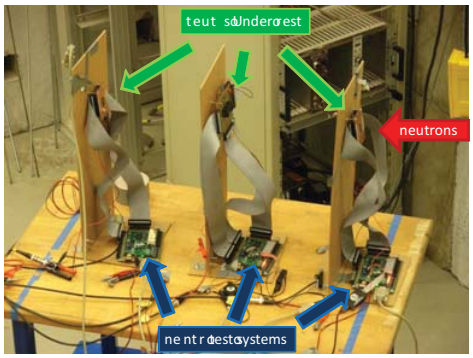

Fig. 1: Test setup used at TSL facility in Uppsala, Sweden.

simulations, we have demonstrated how resistive-open defects may increase the Soft Error Rate (SER) of defective cells when read/write or Read Equivalent Stress (RES) operations are performed [9]. Moreover, in [10] we have experimentally shown how the neutron-induced error rate of SRAM arrays can increase if operations are continuously applied at cell-level to the irradiated memory.

The contribution of this paper is twofold. On one side, we will compare two different SRAM structures to identify which memory (4Mbit or 32 Mbit) is more prone to MBUs. On the other side, we will give experimental evidence that MBU occurrence is increased when the memory is continuously stressed.

The rest of the paper is organized as follows. Section II describes the devices we tested and the experiments we performed, Section III introduces our test methodology, while in Section IV irradiation experiments results are reported and discussed. Finally, Section V concludes the paper.

II. Devices and Experiments

We tested commercially available SRAMs of 4Mbit (512K x 8bit) and 32Mbit (2M x 16bit or 4M x 8bit) built in a 90nm technology with a nominal supply voltage of 3.3V. The 32Mbit array has a more complex structure than the 4Mbit one. The 32Mbit SRAM is divided into two layers (top and bottom layer) and each layer is divided into 4 blocks, each of which is composed of 4Mbit. Every block of the 32Mbit device is similar to the 4Mbit device. The 32Mbit SRAM can be accessed using 16bit or 8bit wide words. We chose the latter configuration in order to have the same access type as the 4 Mbit SRAM. This also eased MBU count comparison as the words have the same number of bits.

Radiation experiments were performed at The Svedberg Laboratory (TSL) neutron facility in Uppsala, Sweden. We irradiated the devices with Quasi-Monoenergetic Neutron (QMN) fluxes with energies of 50, 80, 114, 150, and 180 MeV, during two different test campaigns. Details on neutrons measurements and QMN energy precision can be found in [11]. We performed experiments at room temperature.

Each memory was stimulated by a test controller named Built On Board Self Test (BOBST) implemented through an FPGA. This controller continuously applies the proper write or read operation to the array and eventually detects radiation-induced errors. The memories were stimulated with a frequency of 20MHz, close to the maximum frequency of operation of the irradiated devices.

As can be seen from Fig. 1, the SRAMs were aligned with the accelerated neutron beam. On the contrary, the FPGAs were placed far enough from the beam focus to consider any radiation-induced corruption on the test system to be very unlikely to occur. The beam had a circular spot with a diameter of about 6 cm. The memories were centered with the beam while the FPGAs were placed about 20 cm below (see Fig. 1). Moreover, we applied Triple Modular Redundancy (TMR) features in the implementation of the controller in the FPGA in order to ensure the integrity of the experimental data.

To maximize the number of detected events, we tested 3 memories in parallel. When measuring the cross section of each memory, a conversion factor based on the distance from the neutron source was used. Moreover, to limit the inaccuracy introduced by the experimental error, we regularly swapped the position of the memories. For the same reason, we tested two memories of one type and one of the other in parallel. We tested three different devices for each memory type and perform runs for almost 8 hour for each available energy.

III. Test Methodology

We performed both static and dynamic-stress test on the SRAMs. During the static test, a known pattern is written in the whole memory and the array is read back after a predefined amount of time in order to detect mismatches. We set the interval between write and read operation at 1s to be sure that eventual detected errors are produced by no more than one impinging neutron. This ensures that if two errors were detected during the time between two read back (accumulation time), they were produced by a single impinging neutron. During the accumulation time the memory was left in standby mode, as the test controller is not giving any stimulus. Conversely, in the dynamic-stress mode the array was continuously accessed, and the memory-bit cells were stimulated at speed.

```
⇕ (0)
↑ (0, 1, 1, 1, 1, 1, 1)
↑ (1, 0, 0, 0, 0, 0, 0)
↑ (0, 1, 1, 1, 1, 1, 1)
↑ (1, 0, 0, 0, 0, 0, 0)
↓ (0, 1, 1, 1, 1, 1, 1)
↓ (1, 0, 0, 0, 0, 0, 0)⇕
```

Fig. 2: DS-March algorithm that performs the dynamic-stress test.

Fig. 2 depicts the scheme of the test algorithm March DS that performs the dynamic-stress. In the figure, *r0* (*r1*) is a read 0 (1) operation and *w0* (*w1*) is a write 0 (1) operation. The first element of the March algorithm in Fig. 2 is used for initializing the array, and it is just executed at the beginning of each experiment. The following elements contain the operation to apply at-speed to each location in the memory array. When all the operations of each March element have been applied, the following location is stressed and so on, until the whole array has been scanned. The next element is then executed. Elements are continuously applied to the memory while dynamic-stress test is performed. The main difference

TABLE I
4MBIT AND 32MBIT STATIC AND DYNAMIC-STRESS CROSS SECTIONS

	4Mbit σ [10^{-13}cm^2]			32Mbit σ [10^{-13}cm^2]		
Energy [MeV]	**50**	**80**	**180**	**50**	**80**	**180**
Static	*1.79*	*2.63*	*2.74*	*0.20*	*0.43*	*0.60*
Dyn-Stress	*2.30*	*3.39*	*3.01*	*0.35*	*0.55*	*0.84*
Increment	*28%*	*29%*	*10%*	*75%*	*28%*	*40%*

4Mbit and 32Mbit cross sections under Static (first row) and Dynamic-Stress (second row) conditions. The last row reports the cross section increment due to the applied dynamic-stress

TABLE II
4MBIT SRAM SEU AND MBU DYNAMIC-STRESS CROSS SECTIONS

	Cross Section [10^{-13}cm^2]				
	50MeV	**80MeV**	**114MeV**	**150MeV**	**180MeV**
SEU	*2.30*	*3.39*	*5.02*	*5.52*	*3.01*
MBU	*0.40*	*0.49*	*0.46*	*0.59*	*0.45*
Diff	*17.4%*	*14.6%*	*9.2%*	*10.7%*	*14.9%*

4Mbit SRAM SEU and MBU dynamic-stress cross sections for the available QMN energies. The last line reports the percentage of SEUs that was found to be double MBUs.

between a traditional dynamic test and the dynamic-stress test is that in the former operation are applied at array level, so a cell is accessed just after all the others have been stimulated. In the latter, the single cell is accessed at speed when a March element is applied.

All the March elements, a part from the initialization one, start with a read operation. This is needed, on one side, to detect errors accumulated while the element is applied to other memory locations from the current one. On the other side, the first read operation begins the stress sequence on the cell. In fact, just after the first read, the opposite value is written in the current location, and this value is read 5 times at-speed. If an error appears in one of these read operations, it will also be detected by the remaining read operations in that March element. However, when such a situation occurs, we consider just one error in the cross section measurement.

The changing of the stored value followed by several read operations is a very critical stress for SRAM cells [12]. It is worth to notice that this sequence of operations realistically describes the typical use of memories. For instance, in the case of microprocessors cache or memory cores integrated in a System on Chip, the same location may be read or modified very frequently.

The effectiveness of this sequence of operations in increasing the memory radiation sensitivity has already been demonstrated both analytically [8] and experimentally [10]. These results attest that for realistically evaluating the SER of SRAMs in operation it is not sufficient to perform static or traditional dynamic tests. The novelty of this work is the application of the dynamic-stress test to different memory types in order to evaluate in which terms its efficiency is higher. Moreover, we will measure the occurrence of Multiple Bit Upsets in the array under operating conditions. The next section describes the experimental results we have obtained in the irradiation campaign with the described test setup and methodologies.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. 4Mbit vs 32Mbit SEU cross sections

Tab. I reports the results obtained with the static and dynamic-stress tests for three different QMN energies. It is worth to notice that MBU was counted as a single error in the SEU cross section measurement, thus any multiple error produced by a single impinging neutron was counted like single event.

From the reported data it is clear that both the memory types have a higher cross section when the dynamic-stress test is applied. In particular, in the case of 4Mbit the increment ranges from 10% at 180MeV to 29% at 80MeV. The increment is even more remarkable in the 32Mbit memory, and reaches a maximum of 75% at 50MeV.

The sensitivity of the 32Mbit memory is almost one order of magnitude lower with respect to the 4Mbit device, even if both SRAMs are built by the same manufacturer with a 90nm CMOS technology. The gap between 4Mbit and 32Mbit static cross sections may be due to different realization processes and internal architectures. The goal of this study is to test Commercially available Off-The-Shelf (COTS) devices. Unfortunately, this limits the information we can gather on the physical implementation of the core cell, as the producer does not share those details. Thus, we cannot further investigate the impact of the realization processes in the sensitivities of the devices. In any case, knowing that the technology node is the same (both devices are built in a 90nm CMOS technology), we may assume that the core cell static cross section of the 4Mit and 32Mbit cells should be comparable. In fact, the devices were both in standby mode during the accumulation time, so there is no impact of the architecture or control circuitry corruption in the observed error rate. Moreover, as the cells are not dynamically stressed, the effects of resistive-open or other kind of defects eventually introduced in the manufacturing are not stimulated and do not affect the radiation induced error rate. Thus, the differences in the cross sections are probably due to silicon implementation processes that are part of the Intellectual Property (IP) of the producer.

This lack of information does not limit the discussion on the results that is object of this paper. Here, we focus on the difference between static and dynamic stress test radiation sensitivities of the two devices. This difference is relative and is related to the different response of the two memories to the applied stress and not to the static error rate.

As can be deduced from Tab. I, the dynamic stress cross section of the 4Mbit device is at most 29% higher with respect to the static one, while in the case of the 32Mbit device, the dynamic stress cross section can be even 75% higher with respect to the static one (e.g. when the device is irradiated with 50MeV QMN flux). The applied stress is then definitely more effective in increasing the radiation-induced error rate of the 32Mbit array. This can be explained with the following considerations:

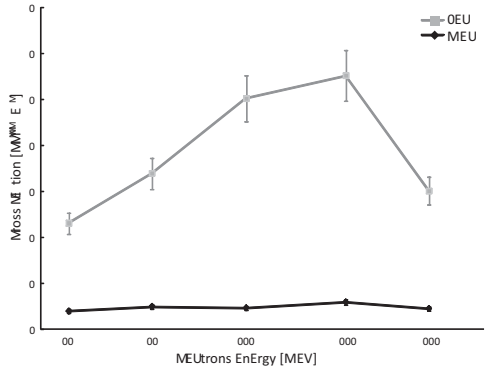

Fig. 3: SEU and MBU cross sections of the 4Mbit SRAMs as a function of the energy of the QMN beam. These results were obtained applying the dynamic-stress test to the irradiated memory.

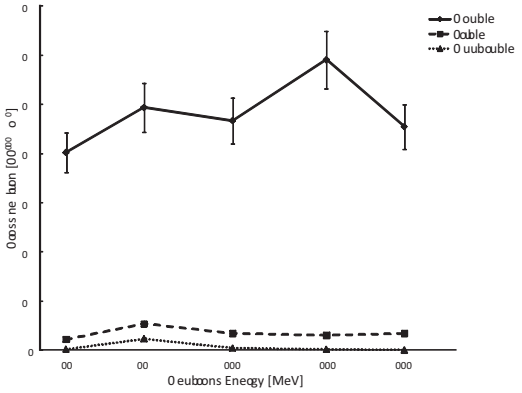

Fig. 4: Double, triple, and quadruple MBUs cross sections of the 4Mbit SRAMs as a function of the energy of the QMN beam. These results were obtained applying the dynamic-stress test to the irradiated memory.

- Firstly, the different structures of the arrays strongly affect the impact of the applied dynamic stress on the device radiation sensitivity. In fact, the bit lines (BLs) and Word lines (WLs) have different lengths in the two arrays and we believe to be longer in the 32Mbit device. The longer the Word lines are, the higher is the number of cells connected together in the same WL and thus the higher the number of cells that experience Read Equivalent Stress (RES) during the dynamic stress test. We have already demonstrated in [9] that when a cell is accessed, even all the cells connected to the same word line are stressed. This kind of stress is very efficient in reducing the voltage level of the internal nodes of non-ideal cells. RESs are very likely to occur when multiple locations are scanned or modified quickly. This which is very common in real applications. It is worth to notice that, in a traditional dynamic test, RESs are not taken into account, as normally just one operation is applied to a location and then the next one is accessed. On the contrary, with the March-DS algorithm, 7 operations are applied to the same location, thus all the cells connected to the WL experience 7 RESs at speed at each March-DS element execution.

- Secondly, the structure of the 32Mbit device is more complex and probably dense. This fact may have forced the designers to choose implementation solutions that introduce a higher probability of asymmetry within the core cell. This kind of problems, as we have already studied and demonstrated in [9] and [10], does not prevent the device from working properly in normal conditions but may increase its radiation sensitivity when stressed at speed. In the presence of defects, the nominal setup time imposed by the producer may not be sufficient to fully recover the node voltage after an operation execution. The stress induced by the March-DS limits the recovery time that a cell has to the minimum period of access (operations are applied at 20MHz, close to the maximum allowed frequency of operation). On the contrary, if all the cells are accessed one after the other (e.g. in a typical dynamic test), the next access to a cell will be performed just when the entire array has been completely scanned. Thus, even the defective cells may have enough time to recover (which is definitely longer than the nominal one). To prevent the critical node voltage to recover completely it is then necessary to apply multiple operations at speed to the same location. The higher the number of consecutive accesses is on a certain cell and the closer to the swap threshold is the voltage level of the internal nodes of the cell, thus the higher is the radiation sensitivity.

- Finally, the 32Mbit architecture may require longer power rails, thus more prone to experience defects. It is well known that even a slight decrease in the sensitive node voltage has the side effect of exponentially increasing the soft error rate of the cell [17]. In [10] we have seen that when the dynamic stress is applied, the radiation-induced error rate increases. As already said, the presence of silent defects increases the recovery time necessary for the cell nodes to restore their voltage after any read access. If operations are applied at speed to a cell, as it happens if the dynamic-stress test is executed, such a voltage restoration will not be fully achieved. This combined with the lowered voltage caused by un-idealities in the power rails makes the cell extremely sensitive to radiation. This thesis is also supported by the fact that the cells that are far from the array power rails were found to be more prone to be corrupted by radiation.

With the experimental data we have obtained and the analysis made, we can conclude that a more complex array structure, the more effective the dynamic stress we are applying.

B. 4Mbit vs 32Mbit MBU cross sections

We further analyze the sensitivity of the 4Mbit device taking advantage of all the available energies at TSL facility. The first row in Tab. II and the grey curve in Fig. 3 report the

TABLE III
DOUBLE MBU CROSS SECTIONS

	2-MBU Cross Section [10^{-14}cm^2]		
	50MeV	**80MeV**	**180MeV**
4Mbit Static	*2.65*	*3.96*	*4.52*
4Mbit Dyn-Stress	*4.02*	*6.94*	*5.95*
32Mbit Static	*0.16*	*0.47*	*0.78*
32Mbit Dyn-Stress	*0.57*	*1.44*	*1.39*

Double MBU Cross Sections for the 4Mbit and 32Mbit SRAM under static and dynamic-stress test condition. In all the considered energies and cases, the observed MBU number is higher when the dynamic-stress test is applied.

cross section of 4Mbit SRAMs under static conditions for 50, 80, 114, 150, and 180 MeV QMN fluxes. As can be seen, the values are slightly greater than the ones presented in literature for similar devices [13-15]. This may be due to difference in the manufacturing processes or to the effects of thermal neutrons in the available beam. Moreover, data show how the memory is more sensible to neutrons of 114 and 150MeV with respect to the other energies. Unfortunately, with the limited information provided by the producer it is not possible to further analyze this trend.

The second line of Tab. II and the black curve in Fig. 3 report the probability of double MBUs occurrence. A double MBU is detected when a single impinging neutron corrupts two bits in the same word. As expected from previous experiments [16], the MBUs cross section is about one order of magnitude lower with respect to the SEUs In this case, as reported in the last row of Tab. II, the percentage of SEUs that was found to be double MBUs ranges from 9.2% at 114MeV to 17.4% at 50MeV. Fig. 4 shows the variation of double, triple (three bits of a word corrupted by a single impinging neutron), and quadruple (four bits of a word corrupted by a single impinging neutron) MBUs cross section as a function of the QMN flux energy. An MBU with more than 4 bits corrupted in the same word was never found during our experiments. As for SEUs, even for MBUs the higher cross section is found at 150MeV. Again, no further investigation is possible with the information provided so, we are not able to physically explain this phenomenon. Again, the scope of this work is to study the impact of the stress we are dynamically introducing in our test in commercially available devices with different architectures. We are aware of the limits of the analysis that can be performed at physical level when dealing with COSTS devices. On the other side, the choice of testing commercial devices gives a realistic idea of the behavior of a device in real life applications. As already demonstrated in [9][10], such a behavior cannot be simulated by testing the device just with a static or a classic dynamic test.

Many works in literature showed that a static test gives just a rough idea of the radiation sensitivity of the irradiated SRAM. In fact, as in a static test the array is left in hold mode without any applied stimulus, errors in the logic circuitry cannot be detected. The introduction of dynamic test overcomes this issue. In a dynamic test operations are

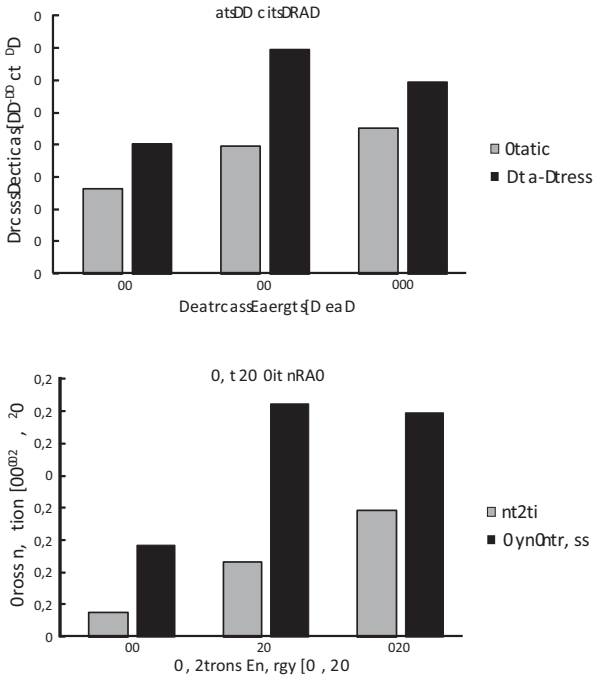

Fig. 5: Double MBU Cross Sections for 4Mbit (a) and 32Mbit (b) SRAMs under static conditions (in grey) and dynamic-stress test (in black)

continuously applied to the irradiated SRAM, allowing the detection of radiation-induced errors in the array logic circuitry. In this paper, we are showing how the introduction of dynamic-stress test increases the accuracy of experimental results, rendering them closer to the realistic utilization of the memory The addressing order is chosen 'row after row' in order to maximize the applied stress. The effectiveness of dynamic-stress test with March-DS in increasing the memory sensitivity to radiation has already been analytically demonstrated in [12]. The results reported here prove the effects of the applied stress even in the MBU cross section. In the follow, we will focus our attention just on 50, 80, and 180MeV energy levels.

Tab. III reports the cross sections of double MBUs for the 4Mbit and 32Mbit SRAMs under static and dynamic-stress conditions irradiated with three different QMN energies. The reported values show that the 32Mbit memory is more resilient to MBUs than the 4Mbit memory. In fact, the number of detected MBUs is almost an order of magnitude lower in the case of the 32Mbit SRAM with respect to the 4Mbit. These values are consistent with the diverse SEU cross sections reported in Tab. I, and the same considerations made in the previous subsection could be applied here.

Experimental data in Tab. III as well as the graphs in Fig. 5a and 5b show that for both types of memory the number of detected MBUs is higher when the SRAM is stressed. In the case of the 4Mbit SRAM, the increased number of detected MBUs by dynamic-stress test with respect to the static test ranges from 51% at 50MeV to 75% at 80MeV. The difference

is definitely more remarkable in the case of the 32Mbit memory. As shown in Fig. 5b, at 80MeV the number of radiation-induced MBUs is almost tripled when the irradiated SRAM is stressed. These experimental data demonstrate that the increment in the MBU cross section due to the applied stress is even higher than the SEU cross section. As we will see, the increment of MBU sensitivity may have even worse repercussions than for SEUs' on the system reliability. It is fundamental to accurately evaluate the impact of the applied stress in the irradiated SRAMs MBU cross sections.

To explain the different impacts of the March-DS in the 4Mbit and 32Mbit MBU cross section we have to consider, firstly, that the array structures of the two arrays are different. As we have said, when a cell is accessed, all the cells connected to the same World Line can undergo a stress called Read Equivalent Stress (RES) [11]. The 32Mbit is likely to have longer word lines (WL) and bit lines (BL) than the 4Mbit, thus a more remarkable stress action (due to RESs) is expected. As in the chosen configuration both memories words are 8bits wide, the addressing needs 19bits for the 4Mbits and 22bits for the 32Mbit. Consequently, when a March element is applied to a location, the number of cells that undergo RESs is definitely higher in the 32Mbit than in the 4Mbit, thus the former may be more sensible to neutrons. It is likely to believe that all the bits of the same word are placed on the same word line. This may be a possible explanation for the observed higher number of MBUs.

As told above, the higher number of cells and the higher level of integration needed to implement the 32Mbit array may have also increased the probability of silent defects or process variations introduction. It is possible that some defects affect particularly a certain region of the array. Thus, those cells are more susceptible to be corrupted if stressed and are likely to belong to the same word. The combination of these two factors may effectively have repercussions also on the amount of MBUs the SRAM experience under radiation.

A second explanation for the higher impact of dynamic-stress test on the 32Mbit MBU cross section relies on the physical process used for implementing the two kinds of SRAMs. Even though the memories are both built by the same vendor in a 90nm CMOS technology, some variations in the physical manufacturing process may have been introduced. The two types of device have very probably been produced on different lines and different times. The design of a 32Mbit memory array may be a harder challenge with respect to the 4Mbit one. The different cross sections of the two devices and the more remarkable impact of the dynamic-stress test in the 32Mbit error rate reported in Tab. I support this thesis. In fact, on one side, process variations may result in different static radiation sensitivities and, on the other, may lead to cells less reliable to the applied stress. The same considerations could be applied to explain the higher increase of the MBU cross section with respect to the SEU one in both the SRAMs.

Experimental data demonstrates that MBUs issue can be exacerbate if the array is continuously stimulated. In particular, the 32Mbit MBU cross section can be roughly underestimated if just traditional dynamic or static test are performed.

These results are of great interest when safety critical applications are concerned, as the applied Error Detection And Correction Code may not be sufficient to ensure the required level of reliability. In fact, when an EDAC code (or other kind of memory protection systems) is designed, a trade-off between overhead and benefits is normally necessary [18][19]. Such a trade-off is principally based on the maximum amount of bits that are accepted to be corrupted by a single impinging neutron. Tuning the EDAC with data obtained with static or traditional dynamic tests may result in an underestimation of the MBUs rate, and thus may lead to sever repercussion on the reliability of the system. On the contrary, using data known to be not precise may force the designer to oversize the protection system, uselessly increasing costs and overheads. The March-DS we have applied during our experiments has been demonstrated to generate a worst case (and realistic, at same time) stress on the memory under radiation. In this paper, we have showed that this is particularly true when MBUs are taken into account. In fact, the MBUs occurrence is drastically increased especially in complex devices like the 32Mbit we have tested. The proposed test methodology is likely to provide an upper bound of the MBU cross section. The memory protection system can then be optimized using this data, avoiding both errors underestimation and minimizing costs.

V. Conclusion

We have tested 4Mbit and 32Mbit commercially available SRAMs under accelerated neutrons beams. We have measured the memories sensitivity to different QMN energies under static (hold mode) condition and when the dynamic-stress test is applied. We have analyzed the MBUs occurrences in both devices and we found out that when the cells are continuously accessed, the percentage of neutrons that generates MBUs is increased. This is particularly an issue for the 32Mbit SRAMs, probably due to longer word lines and bit lines or variation issues introduced in the fabrication processes. It is then important to take into account also stress tests that mimic the real memory operation, as the one we propose here, to have an accurate estimation of the sensitivity of the SRAM, particularly when complex architectures or high density devices are considered.

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