Attenuation of Single Event Induced Pulses in CMOS Combinational Logic

M. P. Baze
Boeing Defense & Space Group
Seattle, WA 98124

S. P. Buchner
SFA Inc
Landover, MD 20785

Abstract

Results are presented of a study of SEU generated transient pulse attenuation in combinational logic structures built using common digital CMOS design practices. SPICE circuit analysis, heavy ion tests, and pulsed, focused laser simulations were used to examine the response characteristics of transient pulse behavior in long logic strings. Results show that while there is an observable effect, it cannot be generally assumed that attenuation will significantly reduce observed circuit bit error rates.

I. INTRODUCTION

Estimating error rates in complex VLSI designs is often addressed by methods which first perform detailed SEU tests and analyses on simple logic gates and then use these gate level results in algorithms that yield reasonable conservative estimates of the VLSI circuit response. Various techniques using different forms of this general method have been described. [1, 2, 3, 4]

An important aspect of these methods is their treatment of short transient upset pulses in combinational logic. Short transient upset pulses occur when charges generated by a single event 'hit' are collected at the logic nodes of non-storing circuit elements. (i.e. NAND and NOR gates, buffers, etc.) These charges may produce a transient logic upset that lasts until they are conducted away via open current paths to power and ground, returning the logic node to its original state. The result is an upset pulse of short duration, typically much shorter than the clock period of the circuit. Because the duration is so short, these pulses are not observed as logic bit errors. However, they can propagate throughout combinational logic and, if they reach register cells, can cause those registers to store erroneous logic states, creating logic bit errors that contribute to the observed bit error rate of the circuit. Analyses of errors that result from direct ion 'hits' to registers can often be performed by considering the storage circuit of the register alone. In contrast, the observed effects of transients involve both combinational logic and registers so that analysis of transient effects must consider a circuit consisting of the cell that is 'hit' and all subsequent cells to the next register.

Whether a pulse will result in a bit error is governed by three important factors. First, the path of logic gates between the gate in which the pulse originates and the next register must be a sensitive path that will allow the pulse to propagate. For an example of sensitive and insensitive paths consider an AND gate with inputs A and B in the states A=0 and B=1. The path from A to the output is sensitive since a change in A will change the output. The path from B to the output is insensitive since a change in B will not change the output.

Second, the pulse must have sufficient amplitude and (more importantly) width to propagate through combinational logic and to a register without excessive attenuation. As a general rule, pulses wider than the logic transition time of a gate will propagate through the gate without attenuation, pulses less than half the transition

0018-9499/97$10.00

time will terminate, and pulses in the range between these will propagate with varying degrees of attenuation. This generality is subject to common design practices and not valid for all design methods. An example where it does not apply would be gate arrays. This is because gate arrays can have widely variable rise and fall times that make the attenuation effect harder to predict.

Third, on arriving at the register the pulse must satisfy the input requirements of the register so that an erroneous state is stored. The most critical of these requirements is the pulse width, expressed as 'set-up and hold time' for synchronous inputs and 'minimum switching time' for asynchronous inputs.

This paper presents the results of a study of the second factor, SEU transient pulse attenuation in combinational logic. Particular attention was paid to the responses of circuit structures built using common digital CMOS design practices. The responses of test circuits were modeled using SPICE circuit analysis and experimentally measured in heavy ion and pulsed laser tests. The goal was to develop a conservative estimate of how important this effect might be in reducing bit error rates. The results reveal characteristics of SEU pulse attenuation and logic error cross-sections in typical digital CMOS circuits that are useful for estimating chip error rates and provide indications for situations in which pulse attenuation may be significant.

II. Test Circuits

Two test circuits were used for this study. Both were designed for SEU response characterization of fabrication processes and are part of a larger radiation test set. The first circuit is a string of inverters that leads to a latch formed by a pair of cross coupled NAND gates. This test circuit is called 'FASTLATCH' and its schematic is shown in figure 1. The inverters serve as both heavy ion 'targets' for pulse generation and as the pulse attenuation line. Two intermediate NOR gates are included to control the flow of pulses from the inverters to the latch and to perform circuit diagnostics. The cross coupled NAND latch was used because it has a shorter input pulse switching time (400 ps) than any of the standard registers (including RAM) in the IC CAD cell library used by Boeing. This allows us to study shorter pulses than would be possible with the standard registers. Inverters were chosen because we wished to use the data to make conservative estimates of logic attenuation and an inverter string has less attenuation than other logic structures. The result is that bit error rate estimates based on inverter attenuation will be an upper bound compared to other logic gate attenuation.

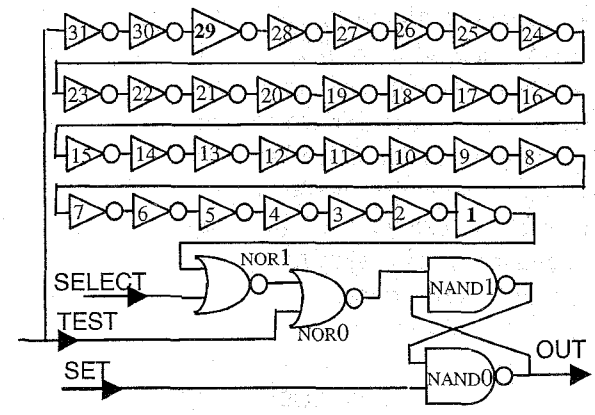

Figure 1. FASTLATCH test circuit.

The second circuit (figure 2) is a string of 62 inverters connected at various points to the PRESET inputs of 5 D FLIP/FLOPS. The PRESET input was chosen instead of D because it is an asynchronous input and avoids the complications of clock edge to error pulse synchronization that occur on the normal D input. Also the minimum switching time on PRESET is 500 ps which is shorter than the 700 ps set-up and hold time for D. This circuit was also designed to provide data for standard library registers as opposed to the custom latch in FASTLATCH.

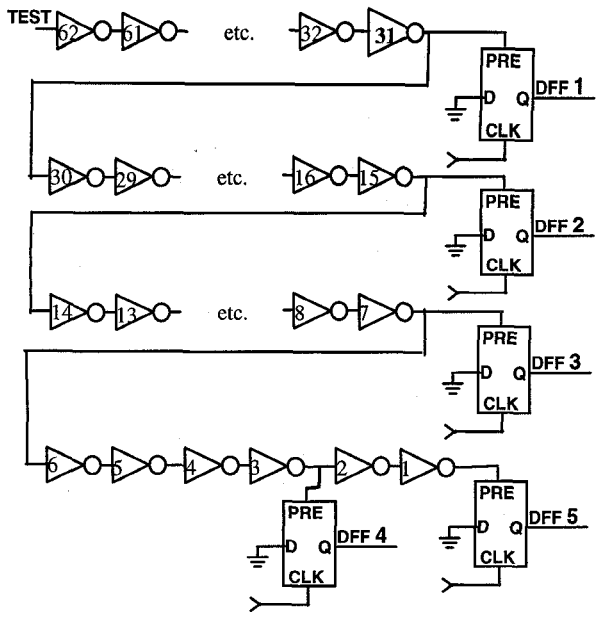

Figure 2. D FLIP/FLOP & inverters test circuit.

All combinational logic gates in these circuits have transistors sized to provide 1.3 mA of drive. This is a minimum drive utilized by the IC CAD system for low capacitive loads. Larger drive values are automatically invoked to maintain combinational logic speed whenever the system encounters larger loads. Transistors within the D FLIP/FLOPs are sized somewhat smaller to conserve power. The internal structure of the FLIP/FLOPs is functionally equivalent to 3 sets of cross-coupled NANDs but because of their smaller transistor size, the internal rise and fall times are slower than the standard library NANDs used for FASTLATCH.

The design practice of reducing register transistor sizes to conserve power is fairly common. In some cases it may result in register set-up and hold or minimum switching times which are longer than the transition times of combinational logic. In these cases the only pulses that will cause an erroneous register state are those which are wide enough to propagate through logic without any attenuation and attenuation will have no observable effect on the bit error rate.

The process used for this study was a commercial, low cost, 5 volt, 1 micron, epi-bulk CMOS process. The epi thickness was 3.0 microns. It could be described as 'typical' in that it has no special, high speed, low power, high temperature, etc. features.

III. Circuit Simulations

Circuit responses to transient pulses were simulated using SPICE. A SPICE 'hit model' developed by Rabe and Golke [5] was used to simulate the pulse on a circuit node that would be produced by a direct heavy ion hit. These simulations give an estimate of the minimum collected critical charge required to produce an upset.

Charge collection was estimated using known process parameters in the HCREM SEU model software. Sensitive volumes were assumed to have the length and width of the drain and gate areas of the sensitive transistors and to have a depletion depth of 1 micron. The funnel length was assumed to be 3 microns (equal to the epi thickness). Due to the number of structures and test conditions, detailed charge collection simulations, (i.e. PISCES) were not performed.

IV. Test Methods

Upset tests were performed using both heavy ions at the Berkeley Cyclotron and laser simulations performed at NRL. Details of the laser facility can be found in reference 6. Propagation delays of the circuits were approximately 10 ns for FASTLATCH and 20 ns for the D FLIP/FLOP string. Devices were clocked at a relatively slow rate of 100 kHz during both tests so that nearly all errors would propagate through the circuit. Errors in the D-FLIP/FLOPs were automatically reset by the clock. Errors in the coupled NAND latch were reset by external error 'sense-and-reset' circuitry at one half the clock rate.

Heavy Ions

Error rates and cross-sections as a function of LET were measured for both circuits. The effect of attenuation should be an increase in the

observed error cross-section as the LET is increased, producing wider pulses that can propagate through a larger number of inverters. At lower LETs, the narrow pulses will attenuate and only the inverters closest to a register will successfully contribute to the observable bit error rate. The results below show that this effect was difficult to observe because charge diffusion in the inverter strings had a much greater impact on the observed cross-section than did attenuation effects.

In addition to cross-sections, coincident errors on the 5 D FLIP/FLOPs were determined using a data logging technique which records the errors that occur within specified time intervals.[7] The interval size was chosen such that the number of ion hits capable of producing errors within any interval was statistically much less than one. In this way bit errors occurring on more than one D FLIP/FLOP within a single interval could be assumed to have resulted from a single ion hit to an inverter producing a pulse that reaches multiple FLIP/FLOP inputs. This technique was more successful for observing pulse attenuation than measurements of the circuit cross-sections.

Laser

SEU Pulse attenuation was determined with the laser by targeting different locations in the inverter strings and measuring the minimum laser energy needed to produce observable bit errors in the latches. (coupled NANDs or D FLIP/FLOPs) The effect of attenuation in these tests is an increase in the minimum laser energy as the number of inverters between the laser 'target' and latch cell increases.

During laser tests care was taken to ensure that shielding of the beam by overlying circuit structures was not a factor. This was accomplished by using structures with identical geometry in terms of cell layout and local metal routing when taking data for comparative results. In addition, the procedures of laser alignment and data acquisition were repeated several times with repeatable results to verify that no alignment uncertainties were effecting the data.

V. RESULTS

General Attenuation Model

Figure 3 shows the results of SPICE modeling to calculate the attenuation/propagation versus pulse width for an inverter string. Pulse widths were taken at the SPICE determined logic switching threshold of 2.5 volts and pulses were defined as absent when they failed to cross that threshold. The lines at 400 and 500 ps are the switching requirements for the coupled NANDs and the D-FLIP/FLOP PRESET respectively and give a qualitative indication of the pulse width 'windows' and logic string lengths over which one can expect attenuation to occur. For example an initial pulse of 600 ps can travel through 15 inverters (25 to 10) and still maintain the 500 ps needed to 'upset' a FLIP/FLOP through its PRESET. Pulses greater than 680 ps propagate with no attenuation in this simulation. 680 ps is in fact the transition time, 'rail-to-rail', for inverters in this process.

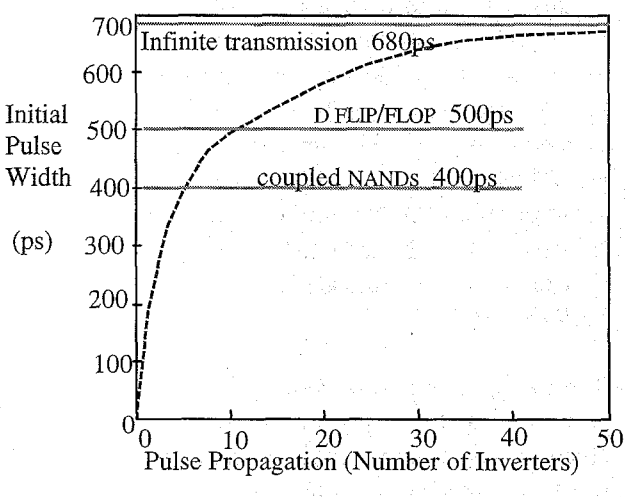

Figure 3. Results of SPICE modeling. Pulse width required (y axis) for propagation through N (x axis) inverters.

FASTLATCH

Using SPICE and the Rabe and Golke hit model, the charge required to induce an output error at various nodes was calculated. Results of this

calculation are plotted in figure 4. The sharp initial rise compared to figure 3 is due to substantial attenuation in the NOR gates which have slower transition times than the inverters.

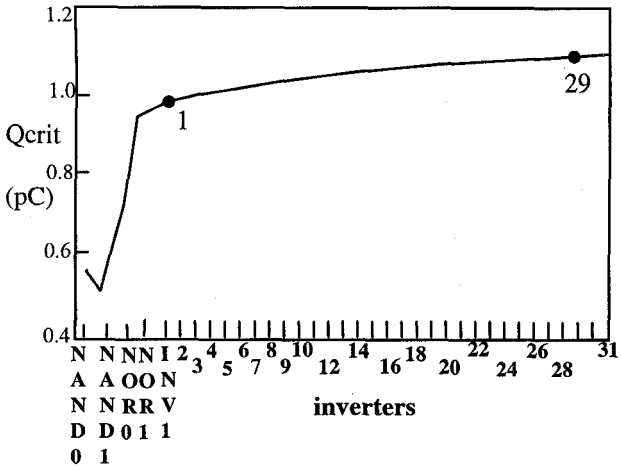

Figure 4. SPICE simulation results for FASTLATCH

Laser tests were performed on two identical inverters to determine the relative energy required for upset at two positions in the string. A comparison of the laser and SPICE results is given in table 1. Points for the SPICE simulations for inverters #1 and #29 are also drawn in figure 4. Even though this circuit was designed for minimum attenuation, some attenuation was predicted by SPICE and observed with the laser. The agreement between the two is good considering that SPICE is a calculation of collected charge and the laser results represent incident energy.

Table 1
Laser and SPICE comparison of FASTLATCH upset thresholds.

	SPICE (pC)	LASER (relative energy)
inverter # 1	0.98	120
inverter # 29	1.04	140
Ratio INV1/INV29	0.94	0.86

Heavy ion data, along with estimates of LETs for the upset thresholds at NAND0, INV1 and INV31 are plotted in figure 5. The shape of this curve is not what one would expect from a simple attenuation model. Rather than rising between 'inv1' and 'inv31' and then saturating, the cross-section curve is nearly linear. In addition, the largest cross-section is nearly 6 times the sensitive area one would calculate from the 'as drawn' layout dimensions of the upset sensitive structures in this circuit. In laser tests to investigate the inverter cross-sections, it was found that doubling the laser energy increased the sensitive area around an inverter from twice to four times the 'as drawn' sensitive area. This is an indication that the error cross-section for the inverters is increasing with heavy ion LET, perhaps due to charge diffusion. Data on the D-FLIP/FLOPs below support this.

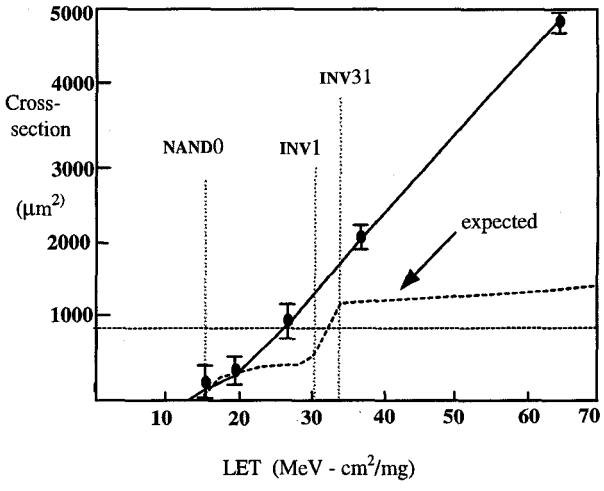

Figure 5. Heavy Ion data for FASTLATCH

D FLIP/FLOPs & INVERTER String

Laser simulations were performed using a single inverter (#31) and observing the number of 'downstream' FLIP/FLOPs displaying upsets. In these tests the attenuation changed so rapidly that the thresholds were very closely grouped and it was not possible to resolve all five error thresholds. For this reason only the data for DFF1 and DFF5 are presented. Table 2 shows a comparison of SPICE simulations and laser upset data for this circuit. Again there is good

agreement between the laser data and SPICE simulations.

Table 2
Laser and SPICE comparison of D-FLIP/FLOP & inverters upset thresholds.

	SPICE (pC)	LASER (relative energy)
DFF1 (only)	1.07	182
DFF 5 (& DFF 1)	1.14	192
Ratio DFF 1 : DFF 5	0.94	0.95

The heavy ion data for FLIP/FLOPs 1 and 5 of this circuit are plotted in figure 6. Again there is a nearly linear increase in cross-section clear up to the highest LET measured and the cross-sections at LET 64 are many times greater than the 'as drawn' sensitive areas. However one can see in this graph that at low LETs the curves nearly coincide and then split around LET 27 eventually reaching a nearly two to one ratio. One explanation for this would be that for the narrower pulses that are generated below an LET 27, pulse attenuation limits the number of inverters that can contribute to the total circuit bit error rate and hence the observed error cross section. In this case DFF1 and DFF5 will have nearly the same cross-sections because the number of inverters that can contribute to the bit error rate in each case is the same. DFF5 may be slightly less due to the capacitive loading of 'upstream' FLIP/FLOPs. Above LET 27, attenuation decreases to the point where DFF5 now 'sees' more upstream inverters than DFF1.

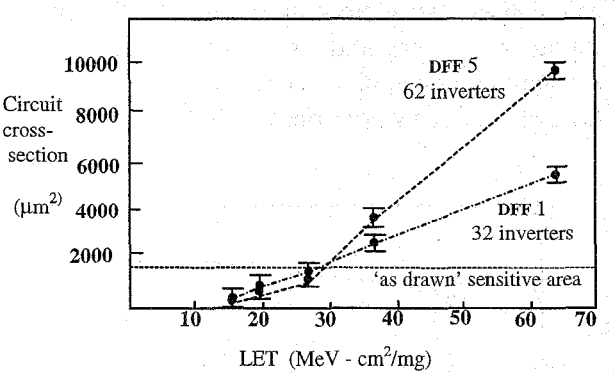

Figure 6. Heavy Ion data for D-FLIP/FLOP & inverters

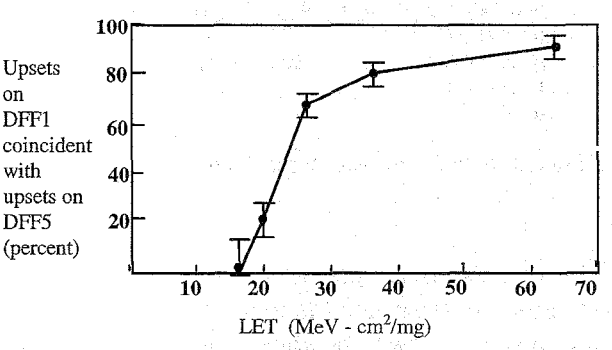

Figure 7. Heavy ion error coincidence results. Percent of errors on DFF1 that are coincident with errors on DFF5

Figure 7 shows the percent of errors on DFF1 that coincide, within a data logging interval, with errors on DFF5. This coincidence measurement was far more effective for observing attenuation than were cross-section measurements. The coincidence data shows a rapid increase from LET 20 to 27. This implies that by LET 27 the majority of ion hits produce pulses wide enough to propagate without attenuation. A more gradual increase up to LET 64 could be due to ion hits toward the fringes of the sensitive areas for which charge collection is less efficient and pulses are narrower. Of additional interest is the fact that the attenuation is varying in a range not far from the 38 MeV-cm^2/mg fall-off point in the natural space LET spectrum. The relative positions of these curves can have a significant effect on the logic induced error rate.

VI. CONCLUSIONS

The data presented here show that even in circuits designed to have minimum attenuation, there is sufficient pulse attenuation to have an observable effect on bit error rates. While attenuation in this case was not large enough to merit the use of an attenuation bit error reduction factor, one implication of the results is that attenuation may have a significant effect when 'slower' combinational logic gates, such as 4 input NORs, are used. The extent of this effect in a VLSI design can vary according to the relative number of registers versus combinational logic cells, clock operating frequency, and pulse widths for attenuation versus pulse widths near the LET spectrum fall-off. In some cases attenuation may be significant with respect to SEU design margin and merit a careful calculation.

The comparisons between laser data and SPICE simulations were quite good and suggest that SPICE can be used to obtain reasonable simulations of heavy ion pulse attenuation.

While the effects reported here are based on a single design cell library and process, one would expect to observe similar effects in other IC CAD systems that follow similar practices.

REFERENCES

[1] Diehl-Nagle, S. E. and Vinson, J. E.,"Single Event Upset Rate Predictions for Complex LogicSystems", *IEEE Trans. Nucl. Sci.*, NS-31, No. 6, 1132 (1984)

[2] Newberry, "Single Event Induced Errors in VLSI Logic Circuits", presented at *IEEE NSREC*, July, (1986).

[3] Baze, M. P. and Bartholet,W. G., "Single Event Test Structures for Digital CMOS ASICs", *IEEE Trans. Nucl. Sci.*, NS-40, No. 6, 1703 (1993)

[4] Kaul, N., Bhuva, B. L., and Kerns, S. E., "Simulation of SEU Transients in CMOS ICs", *IEEE Trans Nucl. Sci.* NS-38, No. 6 1514 (1991)

[5] Silver, John J, "Circuit Designs for Reliable Operation in Hazardous Environments", *IEEE NSREC Short Course Notes.* , pp 59-65 (1987)

[6] Buchner, S., et al, "Laboratory Tests for Single Event Effrects", *IEEE Trans. Nucl,. Sci.,* , NS-43, No. 6, 678 (1996)

[7] Normand, E., et al, "Single Event Upset and Latchup Measurements in Avionics Devices", *IEEE Radiation Effects Data Workshop Record,* Cat # 95TH8149, p 33 (1995)