Alpha-Induced Multiple Cell Upsets in Standard and Radiation Hardened SRAMs Manufactured in a 65 nm CMOS Technology

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***Abstract*—Accelerated alpha-Soft Error Rate (SER) measurements are carried out on regular and radiation-hardened SRAMs in a 65 nm CMOS technology. Results are first compared to previous experimental radiation data in 130 nm and 90 nm. Second, the SER increase measured in 65 nm is investigated through (i) Multiple Cell Upsets (MCU) counting and classification from experimental bitmap errors and (ii) full 3-D device simulations on SRAM bitcells to assess the PMOS-off sensitivity and the NMOS SEU threshold LET (LET_{th}) of each tested technologies. Finally, process changes are also scanned to shed light on the 65 nm SRAM response to alpha particles.**

***Index Terms*—Alpha experiments, CMOS 65 nm, full 3-D device simulation, multiple cell upset, robust SRAM, soft error rate.**

I. Introduction

SOFT Errors, also referred to as Single Event Upsets, are non destructive loss of information in an electronic system. Such failures occur when energetic particles interact with a memory cell. Soft errors are a key reliability concern for today's consumer applications often responsible for the highest failure rate of all the hard reliability mechanism, such as Negative Bias Temperature Instability (NBTI), electromigration or soft breakdown. After a continuous increase of the SER per Mbit over the past decade, a saturation and even a slight reduction has been recently reported in the literature from either the 130 nm or the 90 nm technological node. This behavior is noticed for both neutron [1], [2] and alpha [3]–[5] SER. Note that even if the SER per bit tends to saturate or decrease, from the 130 or 90 nm node, the SER per System on Chip keeps on growing with the technology shrinking due to the amount of transistors per mm2 doubling at each generation [6].

In this work, alpha testing is performed on regular and radiation-hardened SRAMs in a 65 nm CMOS technology. Results are compared to previous experimental data in 130 nm and 90 nm. The impact on SER of different phenomena is quantified in order to understand the SER variation from the 90 to 65 nm technological node.

— First, the 65 nm experiments are analyzed to count the alpha-induced multiple events. The so-called Multiple Cell Upsets (MCU) are topological multiple upsets which can be corrected by classical Error Correction Codes. A new formula is proposed to differentiate multiple errors due to a single ion from multiple errors due to multiple ions to ensure the relevance of the MCU recorded.

— Second, device simulations are performed on full 3-D structures built using a new methodology developed for the 65nm node. These simulations are used: (i) to compare the sensitivity between the NMOS-off and the PMOS-off, (ii) to compare the NMOS-off sensitivity of the 3 tested technologies, (iii) to investigate the current-response of the 65nm bitcell after an ion strike.

Device simulations outcomes are then correlated to process changes in 65 nm. Their effects on charge collection are also appraised. Finally, the alpha testing results are used to extrapolate the sensitivity of 65 nm devices to neutrons.

II. Experiments

A. Experimental Details

1) Alpha Source: Experiments results presented hereafter are performed with an Americium 241 alpha source whose activity is 100 μCi. The design-of-experiments included different test patterns and supply voltages. The test procedure is compliant with the JEDEC SER test standard labeled JESD89 [7].

2) Tested SRAMs: SRAM devices were manufactured with two commercial 130 and 90 nm processes and a 65 nm development process. For comparison purpose, the 90 and 65 nm SRAMs were processed with exactly the same Low Power (LP) process option and with triple-well structures. These triple-wells consist in either an N+ or P+ buried layer in respectively a P or N-doped substrate [8]. As most actual devices are processed in a P-substrate, triple well are also usually designated as Deep N-Well (DNW) or N+ buried layer. DNW structures are well known to reduce the SER [8]. Main features of the tested devices are summarized in Table I.

Each tested SRAM was processed in a hardened version by adding two Metal-Insulator Metal (MIM) capacitors just above the cell footprint. The radiation and electrical performances for this original mitigation technique are described in details elsewhere [9].

The robust SRAM cell is built in the third dimension (3-D) of a standard 6 transistor High Density SRAM cell above which two stacked eDRAM capacitors are symmetrically added (Fig. 1). The SRAM cell layout and footprint are rigorously identical to the non-hardened version with only the 3 additional

Manuscript received July 14, 2006; revised August 11, 2006.

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Digital Object Identifier 10.1109/TNS.2006.885007

TABLE I
MAIN FEATURES OF TESTED SRAMS

Technological node	Nominal Voltage [V]	Bitcell area	Technology Option
130 nm	1.2	2.50 µm²	General Purpose
90 nm	1.2	1.15 µm²	Low Power
65 nm	1.2	0.525 µm²	Low Power

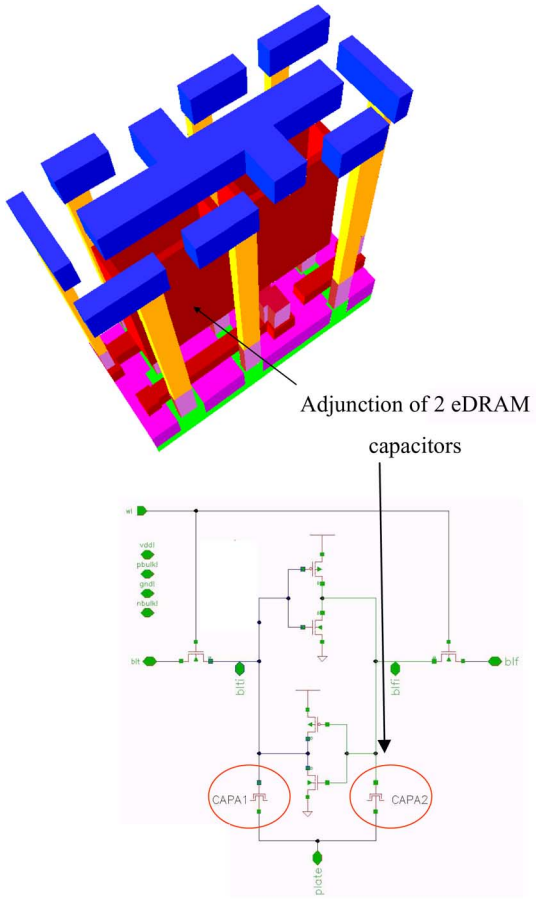


Fig. 1. Overview of a robust SRAM (rSRAM) cell composed of 6 standard transistors plus 2 eDRAM capacitors (6T + 2C). The common electrode is biased at $V_{DD}/2$ to ensure the 15-year life product.

layers for the capacitor definition. This device can be processed with and without the capacitor steps resulting respectively in a hardened or non-hardened SRAM.

With this stacked MIM capacitor, the internal node capacitance can be increased without any area penalty up to 36 fF/unit in 130 nm, 14 fF/unit in 90 nm and 8 fF/unit in 65 nm.

B. Alpha-SER Experimental Results

Fig. 2 shows the SER from alpha particles measured on non-hardened SRAMs in arbitrary units. The Failure-In-Time (1 FIT = 1 soft error in 10^9 device-hours) rates are extrapolated from the accelerated measurements with the radioactive sources assuming a natural alpha emission rate of 10^{-3} α/cm^2/h.

Between the 130 nm and 90 nm technological nodes, the SER/bit is decreased by 37%. This value is comparable to the 30% decrease claimed by Cannon *et al.* [10] but opposite to the 8% increase reported by Hazucha *et al.* [11].

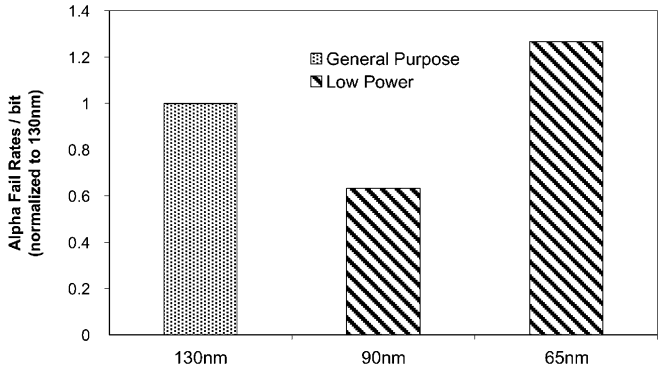


Fig. 2. Experimental alpha SER in arbitrary unit as a function of technological node for non-hardened SRAMs. Failure rates compared at the same nominal power supply voltage: 1.2 V. Identical nominal supply voltages for the 3 technologies are due to processes option change.

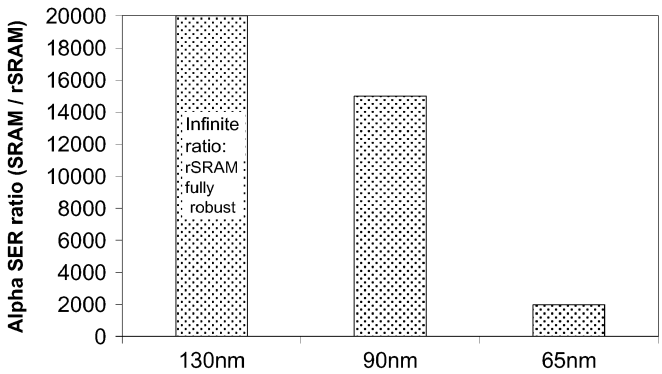


Fig. 3. Experimental alpha SER ratio between SRAM and rSRAM as a function of technological node.

From the 90 nm to 65 nm technological nodes the SER/bit is doubled. This experimental SER increase is stronger than the 20% increase measured on latch [12] and opposite to the saturation or decrease trends extrapolated by several research teams [10], [13], [14].

For the first time, the effectiveness of the rSRAM is plotted in Fig. 3, together with the alpha SER ratio between SRAM and rSRAM for the three technologies. At the 130 nm node, this ratio is infinite since the rSRAM is fully immune to alpha particles thanks to the added 36 fF. From the 90 nm technological node, the bitcell area shrinking has reduced the added capacitors value and some rare errors are recorded when testing the 90 nm rSRAMs. At this node, the rSRAM is 15000 times less sensitive than its non-hardened counterpart; this ratio is 2000 for the 65 nm node. However, the 65 nm rSRAM has still a very low sensitivity to alpha particles as its SER is well below 1 FIT/Mb, which translates into a Mean-Time-To-Failure (MTTF) superior to 100 000 years.

These experiments show a potential limitation of hardening SRAMs with eDRAM capacitors while keeping the bitcell area unchanged (the amount of added fF per cell is directly proportional to the bit cell area). This mitigation technique might also have another limitation in 65 nm related to its capability to diminish the neutron-SER. The critical charge threshold for the device immunity is indeed much higher for neutrons than for

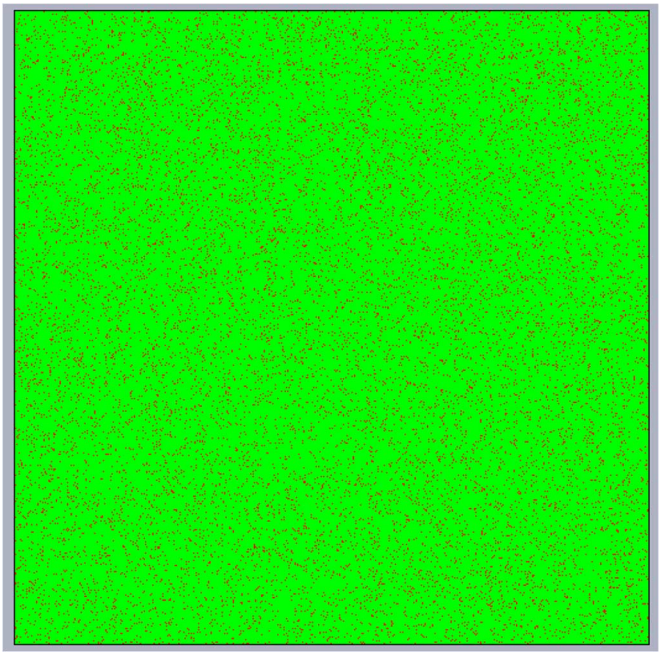


Fig. 4. Example of error bitmap after intense alpha bombing. Bit in errors are displayed as points.

alpha particles. However, the neutron SER of rSRAM 90 nm is successfully reduced down to 10 FIT/Mb [8].

III. Investigating the SER Increase Between 90 and 65 nm Technologies

The SER evolution between the 130 and 90 nm is perfectly consistent. As a matter of fact, the technology option is changed from general purpose to low power which has induced a constant supply voltage between the 130 nm and 90 nm technology. Since, the bitcell area is reduced (Table I), the SER is reduced accordingly.

A SER reduction is also expected from the 90 to 65 nm since the nominal supply voltage is still kept constant and the bitcell area decreased. However, the experiments have shown a large SER increase. To understand this behavior, the following analyzes are carried out:

— Multiple Cell Events counting and classification from experimental bitmap errors.
— Linear Energy Transfer threshold (LETth) computations through full 3-D device simulation on SRAM bitcells.

A. Multiple Cell Events

MCU phenomenon is often presented as a bottleneck for technologies below the 130 nm node [15], [16]. Analyzing the experimental bitmap errors for MCU is therefore mandatory when investigating the reasons for the alpha-SER increase in 65 nm.

An illustration for the bitmap error on the standard 65 nm SRAM is given in Fig. 4 where the errors are displayed as red points. With such a high density of SEUs (thousands of SEUs) the key question is therefore: how many upsets are "true" MCU

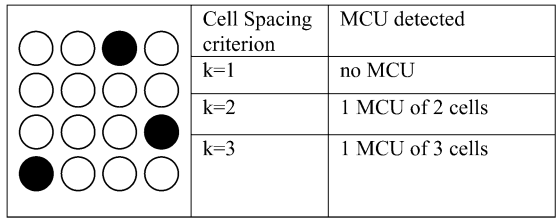


Fig. 5. Illustration of the impact of Cell Spacing criterion on the MCU detection efficiency.

(cf. [1] for the MCU definition) i.e., several SEUs simultaneously created by a single ion, and how many are "false" MCU i.e., sequentially created in the same vicinity by different ion strikes?

1) Cell Spacing Criterion Effect on Counting "False" MCU: MCU rates and shapes depend on the test pattern filling the memory. It was experimentally verified that checkerboard, All1 and All0 test patterns have similar MCU rates. The following analyzes and MCU counting are given for CKB pattern. A cell spacing criterion (k) is chosen when analyzing a post-irradiation error bitmap for MCU detection. This criterion corresponds to the upset-to-upset spacing (maximum number of cells between two SEUs in the X and Y directions to count a MCU). The effect of this criterion on the number of counted MCU is illustrated in Fig. 5. This figure points out that the MCU number (zero or one bitflip) and type (2 or 3 cells) is function of the cell spacing (CS) criterion value: the larger this value $(5, 6\ldots)$, the higher the MCU number. However, large k value would lead to count as an MCU two single SEU in neighboring cells created by two different events i.e., not simultaneously generated. This would lead to a large overestimation of the MCU rates.

For this reason, formula (1) is proposed for quantifying the rates of "false" MCU in order to correct raw experimental data to count only the "true" MCUs. The formula is further detailed in annex 1. We believe that this result should be useful in hardness assurance processes: for the total number of fails to target before stopping the irradiation and for the choice of the radiation source intensity (here a radioactive alpha source).

$$\text{false}MCU\% = 1 - e^{-E_{\text{SRP}} \times \frac{\text{AdjCell}}{N\text{bit}}} \tag{1}$$

where E_{SRP} is the number of SEU recorded after irradiation; AdjCell is the number of cells around each SEU which are inspected to detect a MCU; and N_{bit} is the size of the memory array.

2) Percentages of MCU Measured in 65 nm: During the alpha SER experiments on the standard 65 nm SRAM, Multiple Cell Upsets are recorded but no MBU were ever detected. The reason for this total lack of MBU is the physical bit interleaving within the tested memory arrays. MCUs are carefully counted from the alpha experiments performed on the standard 65 nm SRAM. The results are reported in Table II for different

[1]Definitions given in JEDEC JESD89 standard for multiple upsets [7]: • **Multiple-bit upset (MBU)**: MCU in which two or more bits are involved in the same word, which cannot be corrected by a simple Error Code Correction. This term is used in some cases only to express MCU, so that care must be paid in the usage of this term • **Multiple-cell upset (MCU):**An event that induces several bits to fail at one time. MCU consists of multiple-cell error bits which are usually but not always adjacent

TABLE II
MEASURED MCU PERCENTAGES ON 65 NM SRAM FOR SEVERAL TESTS CONDITIONS. "FALSE" MCU ARE SUBSTRACTED TO RAW DATA TO COUNT ONLY "TRUE" MCU % (REPORTED AS CORRECTED MCU%)

	V_{DDnom}	V_{DDnom} -20%	CS value
Raw MCU%	9.4%	8.8%	1
Corrected MCU%	4.0%	3.7%	1
Raw MCU%	32.0%	31.1%	3
Corrected MCU%	3.9%	3.8%	3

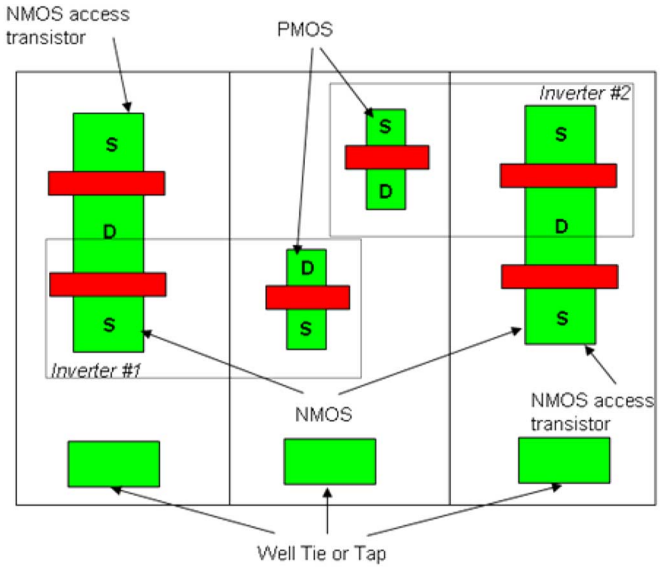


Fig. 6. Cell layout of a 6T SRAM with three wells (p-n-p).

cell spacing criteria (cf. Fig. 5) and supply voltage conditions. Raw MCU rates are presented along with corrected ones (which are obtained by subtracting false MCU rates calculated with formula (1) from raw experimental data). Table II shows that the MCU percentage is constant with the supply voltage and the cell spacing criterion. Additionally, another important point to notice from Table II is that raw MCU rates (uncorrected) have large values especially for large CS criterion $(\sim 30\%)$. Uncorrected MCU rates would thus have lead to erroneous conclusion about the strong effect of MCU on 65 nm alpha-SER.

Compared to 130 nm and 90 nm, the 65 nm MCU rate is constant for alpha. Consequently, MCU phenomenon can not explain the alpha SER increase observed in 65 nm. However, as the charge deposition and collection mechanisms are different with alpha particles and neutrons, the MCU rates from neutron experiments will probably increase from 90 to 65 nm.

B. Full 3-D Device Simulations

Simulations are performed using device simulator Devise [17]. SEU threshold calculations are performed using Devise mixed-level device/circuit capabilities [18]. Physical models used in the simulations included carrier concentration-dependent minority carrier lifetimes, Auger recombination, and mobility models which included doping, electric field, and carrier--carrier scattering dependence. The cell layout is first depicted in Fig. 6. The polysilicon layer is arbitrary truncated to the MOSFET gate definitions.

This layout is used to build the 3-D structures. Shape, dimensions of processed and simulated transistors are thus strictly equal. Wire connections between the different cell electrodes are indeed modeled in a contiguous SPICE domain (mixed-mode TCAD simulations) to save a significant number of finite elements and lighten the CPU burden. Fig. 7 shows the 65 nm 3-D SRAM bit cells having 6 transistors (2 P and 4 N MOSFETs) and 3 well contacts (one per well). Note that the doping profiles are precisely modeled from SIMS (Secondary Ion Mass Spectrometry) profiles. The complex procedure to build such a 3-D device, with more than 100 000 finite individual elements, is described elsewhere [19]. It may be worth noting that short channel effects in 65 nm, leading to important leakage currents, are extremely difficult to tackle in these 3-D TCAD device buildings.

1) PMOS-off Sensitivity Assessment by 3-D Device Simulation: Another possible cause of the 65 nm alpha-SER sensitivity enhancement is an increased sensitive area due to upset not only from NMOS-off strikes but also from PMOS-off. To further check for this assumption, computation of the SEU thresholds are performed for ion strikes centered both on the drain diffusion areas for the NMOS-off and the PMOS-off. Results are synthesized in Table III which shows that PMOS-off threshold LET is 4 times higher than the NMOS-off. This implies that in 65 nm the PMOS is still far less sensitive than the NMOS and cannot be responsible for the whole alpha-SER increase experimentally measured.

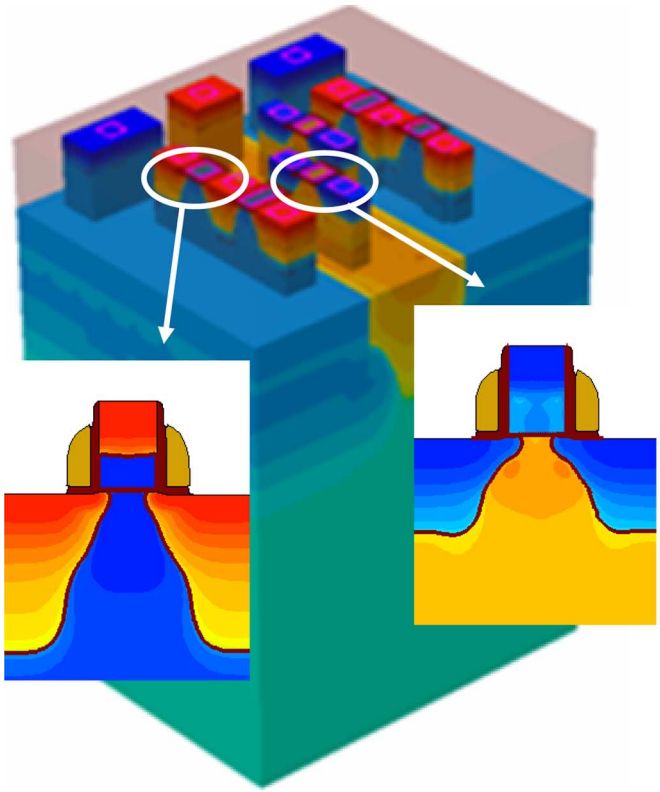
2) Effect of the LET_{th} on Alpha Sensitivity: At first order, the SER is often described as a direct function of critical charge and sensitive volume [20]. From the 90 to 65 nm node, the critical charge is slightly decreased since the supply voltage is kept constant at 1.2 V while sensitive area is decreased by almost a factor x2. SER variation from the 90 to 65 nm is expected to be identical with the 130 to 90 nm one which has decreased of 40%. However, this would be ignoring the specificity of alpha particles and the impact of a third parameter on alpha SER: the threshold LET.

Many publications have differentiated particles crossing the drain from tracks not crossing the drain [21], [22]. However, these publications have not highlighted enough the importance of this difference when dealing with alpha particles. For alpha-SER, diffusion mechanism plays a little role in the upset as well as particles not crossing the drain since:

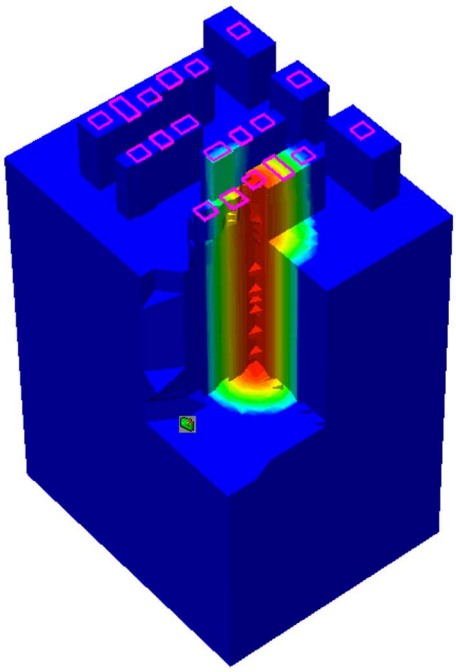
i) Alpha particles are emitted through radioactive decay by heavy atoms and have an energy comprised between 2 and 8 MeV. Americium 241 has an alpha energy of 5.4 MeV and a LET of 6 fC/μm. This LET corresponds to a small amount of deposited charge once compared to a critical charge (few fC) collected through diffusion.

ii) Alpha particles have a limited range in silicon (~ 30 μm) and during alpha SER experiments the alpha source is located above the silicon chip (Fig. 8). This implies that most of the alpha particles reaching the active silicon do not have grazing angles. However, it is known that for particles not crossing the drain, the most effective tracks to induce SEUs are located beneath the source/drain diffusion and parallel to the surface [23]. During alpha experiments, most effective conditions to upset a cell by diffusion are not likely to occur.

To additionally verify the predominance of drift over diffusion, 3-D device simulations were used to compute the collected charge after alpha-particle strikes. Two different particles local-



(a)



(b)

Fig. 7. Full 3-D structures of the 65 nm 6T SRAM showing (a) doping profiles (inserts are 2D MOSFETs doping) and (b) ion strike in the drain of the NMOS-off. This SRAM cell has three wells (p-n-p).

TABLE III
SEU THRESHOLD LET FROM 3-D DEVICE SIMULATIONS

Ion strike centered on	SEU threshold LET
NMOS-off drain	(5.5<SEU_{th}<6) fC/µm
PMOS-off drain	(21<SEU_{th}<22) fC/µm

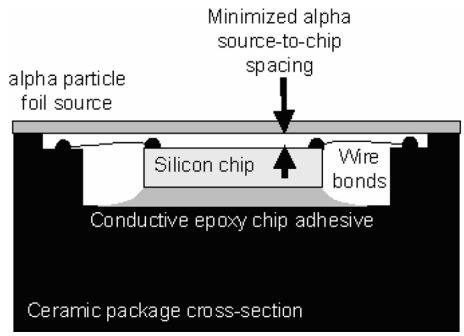


Fig. 8. Cross section of die and radioactive source during alpha SER experiments (from JEDEC standard JESD89 [7]).

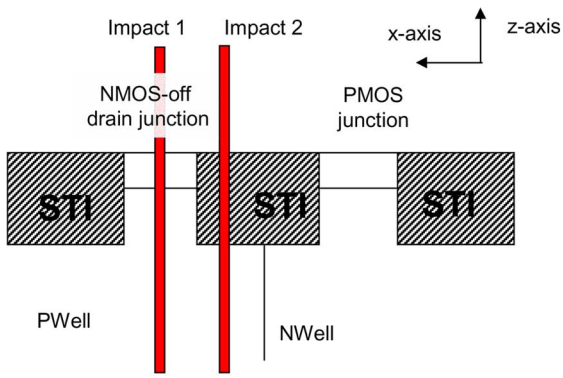


Fig. 9. Cross sections of Fig. 7 to illustrate the alpha track position of two different simulations: (i) centered on the NMOS-off drain (ii) position slightly shifted compared to previous one. Vertical particle tracks are simulated in both cases.

izations are simulated: one centered in the NMOS-off drain (impact 1 schematized on Fig. 9), the other shifted by 0.1 μm along the x-axis (impact 2 in Fig. 9). Collected charge from impact number 2 is much lower than for impact 1. Because e^-/h^+ pairs are not collected from the first 0.3 μm due to the STI (Shallow Trench Isolation) and few drift is possible since the track did not cross the NMOS-off drain junction. These last points highlight that alpha SER is driven by alpha particles crossing the drain and that the main collection mechanism is drift and not diffusion.

It was demonstrated that for a particle track crossing the drain, the drain current is mainly determined by the LET of the incident particle [24]. The particle LET value is the key parameter to (i) state if a particle can induce an upset or not (ii) determine the alpha SER sensitivity of the chip. Consequently, full-3-D structures were simulated to calculate $\mathrm{LET_{th}}$ value for the 3 tested technologies (Fig. 10). This figure shows that from the 130 to 90 nm node, the $\mathrm{LET_{th}}$ has increased which has induced a strong SER decrease (jointly with the moderate $\mathrm{Q_{crit}}$ and strong bitcell area decrease). Fig. 10 also points out that from the 90 to 65 nm, the $\mathrm{LET_{th}}$ is divided by a factor x2. This decrease may explain the 65 nm alpha SER large variation.

In order to quantify the effect of $\mathrm{LET_{th}}$ on alpha SER additional simulations are performed using a proprietary Monte-Carlo simulator. This code is presented elsewhere as well as its ability to predict alpha and neutron SER [8], [25]. To synthesize its main features, when a track doesn't intersect the drain

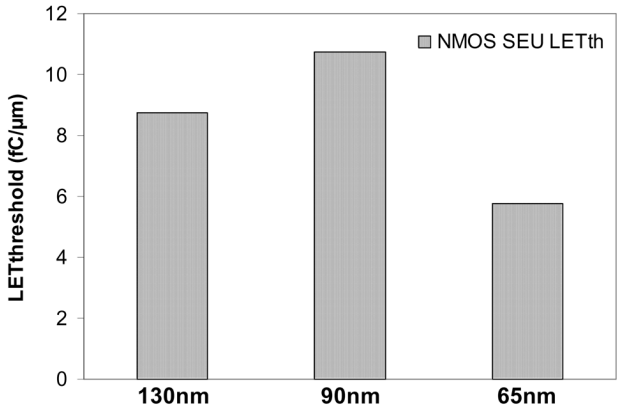


Fig. 10. SEU LET_{th} for strike in NMOS-off drain at nominal voltage for the 3 tested technologies.

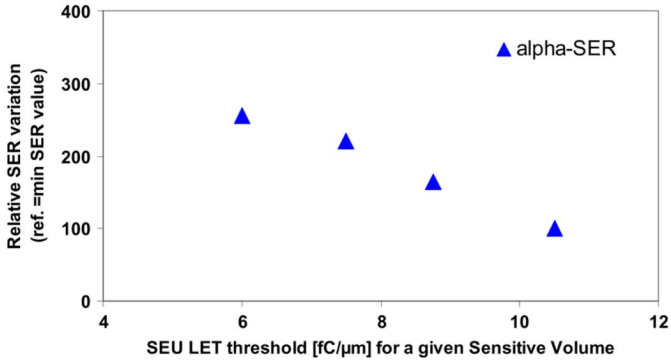


Fig. 11. Alpha SER variation as a function of the threshold LET. SER data are computed from Monte Carlo simulations and are normalized to their minimum value.

junction, drain current pulse is computed thanks to the numbers of carriers collected at the drain junction by diffusion. When a track crosses the drain junction, critical LET criterion is used instead of the diffusion model. Alpha and neutron SER are computed as a function of threshold LET for a 90 nm LP technology. The results are reported in Fig. 11. At the time of the writing of this paper, Monte-Carlo simulations on the 65 nm were still on-going. Fig. 11 shows that alpha-SER is strongly impacted by LET_{th} variation. When the LET_{th} is decreased by a factor x2, the alpha SER is increased by a factor x2.5. The simulated SER variation matches the experimental one. The LET_{th} variation justifies that the 65 nm alpha-SER not even decrease compared to the 90 nm but increase by a factor x2.

3) Charge Collection Enhancement in 65 nm: 3-D device simulations have shown that the LET_{th} in 65 nm is divided by a factor x2 compared to the 90 nm. This decrease is the main reason for the 65 nm alpha SER increase compared to 90 nm. The last remaining question to shed light on is the reason for the LET_{th} decrease.

The main process change between each tested technologies is the well resistance. The N-Well and P-Well sheet resistance for the 3 technologies is reported on Table IV. It shows that both N- and P-Wells resistance have decreased from the 130 nm to 90 nm node but also that they have increased and almost doubled from the 90 to 65 nm node.

TABLE IV
NWELL AND PWELL RESISTANCE FOR THE 3 TESTED TECHNOLOGIES ALL NORMALIZED AT THEIR VALUES IN 130 NM

Technological node	N-Well sheet Resistance	P-Well sheet Resistance
130nm	100	100
90nm	73	71
65nm	120	135

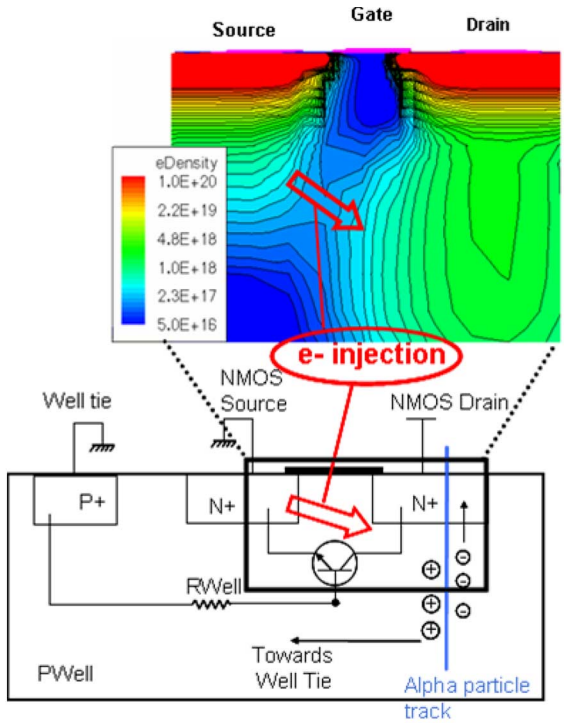


Fig. 12. Illustration of the carrier injected by the source and triggering of the parasitic bipolar transistor after an alpha particle strike in the drain. Insert is from device simulation of the 65 nm 3-D structure.

The main effect of well resistance increase is related to parasitic bipolar transistor inherent to each MOSFET [26]. Majority carriers deposited by particle diffuse towards well tie. A higher well resistance will induce a higher voltage drop beneath source diffusion. The source-well junction will therefore be turned-on more easily and additional carriers will be injected in the well (Fig. 12). Most of these additional carriers will be collected at the drain junction and increase the collected charge at the drain since:

i) The lower the well doping, the weaker the recombination process: this will increase the number of minority carrier that will reach the drain junction.
ii) The gate length of MOS transistors corresponds to the source-drain distance and is the base width of bipolar transistors. From 90 to 65 nm, this distance is consequently reduced by 30%. This assumption was verified thanks to 3-D device simulations, the amount of injected charge by the source of the NMOS is compared in Table V for the 90 nm and 65 nm node. This table shows that in 65 nm the amount of injected charge has almost doubled.

The source injected carriers are also forerunners of the bipolar transistor triggering. Jointly with these carriers, the base width diminution and the recombination diminution in the base lead to

TABLE V
CHARGE INJECTED BY THE NMOS SOURCE (NORMALIZED TO THE 90 NM VALUE) FROM 3-D DEVICE SIMULATIONS

Technological node	90nm	65nm
Normalized source-injected charge	100	180

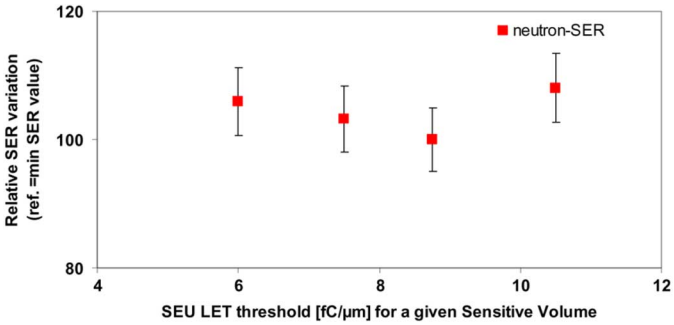


Fig. 13. Neutron SER variation as a function of the threshold LET. SER data are computed from Monte Carlo simulations and are normalized to their minimum value.

a parasitic bipolar transistor more easily triggered. We believe that the additional charge collection due to the source injection and to the parasitic bipolar action is responsible for the $\mathrm{LET_{th}}$ decrease and alpha-SER increase observed in 65 nm.

4) Neutron SER Assessment in 65 nm: The alpha-SER is driven by the NMOS-off $\mathrm{LET_{th}}$ value. In order to assess the influence of the $\mathrm{LET_{th}}$ on neutron-SER, Monte Carlo simulations are performed for atmospheric neutrons. The neutron-SER variation as a function of the $\mathrm{LET_{th}}$ is plotted in Fig. 13. This figure highlights that neutron-SER is not driven by $\mathrm{LET_{th}}$ value as SER variations remain within simulation uncertainty. This concurs with previous works which have shown that neutron-SER main collection mechanism is diffusion from charges generated by particles tracks not crossing the drain [22]. The $\mathrm{LET_{th}}$ decrease observed in 65 nm will not influence the neutron-SER. With the additional assumption that the MCU rate and PMOS sensitivity are equal to their 90 nm value: the 65 nm neutron-SER will be smaller than the 90 nm one.

IV. CONCLUSION

Accelerated alpha SER measurements were carried out on regular and robust SRAMs in a 65 nm technology. The hardening effectiveness for an SRAM cell protected by eDRAM capacitors is again demonstrated: the fail rate is reduced by up to x2000 compared to the standard SRAM. However, compared to the 90 nm node, the measured 65 nm alpha-SER is doubled for standard SRAM. Since the sensitive drain area and critical charge variation were not able to justify this SER increase, the following studies were performed.

The analysis of the 65nm radiation tests on the standard SRAM has revealed that the MCU% is kept steady compared to the 90 nm node and cannot account for the SER increase measured. Besides, we have pointed out that MCU, defined as multiple cell upsets, can either result from several SEUs randomly created in the same vicinity (false MCU) or multiple Upsets simultaneously created by a unique ion strike (true MCU). Counting criteria have been proposed to quantify the different type of MCUs from a classical radiation bitmap error. A formula has then been proposed to easily calculate the amount of false MCU.

TABLE VI
NUMBER OF ADJACENT CELLS INSPECTED FOR MCU AROUND EACH SEUS AS A FUNCTION OF THE CELL SPACING CRITERION

Cell Spacing criterion	k=1	k=3	k=5	k=8
# of Adjacent Cells = AdjCell	8	48	120	288

Full 3-D device simulations were then set-up to further explore the radiation response of the 65 nm technology. First, it was verified that PMOS-off transistor was still far less sensitive than the NMOS (SEU $\mathrm{LET_{th}}$ 4 times higher). Second, NMOS $\mathrm{LET_{th}}$ values were calculated for 3 successive technologies. Between the 90 and 65 nm node, $\mathrm{LET_{th}}$ is decreased by a factor x2. 3-D Monte Carlo simulations have shown that this $\mathrm{LET_{th}}$ variation account for the SER experimental increase.

Compared to 90 nm, the 65 nm well sheet resistance variation has induced additional charge collection at the drain (due to source injection and to the parasitic bipolar action) which in turn was responsible for the $\mathrm{LET_{th}}$ decrease and the alpha-SER increase.

APPENDIX I
ANNEX 1

The probability to count a "false" MCU is given by:

$$P = E_{\mathrm{SRP}} \times \frac{\mathrm{AdjCell}}{N\mathrm{bit}} \tag{1}$$

where $\mathrm{E_{SRP}}$ is the number of SEU recorded after irradiation (from a single readout period); AdjCell is the number of cells around each SEU which are inspected to detect a MCU, this number is function of the CS criterion (Table VI); and N_{bit} is the total number of bits in the memory array.

The probability that a MCU occurred is the complementary probability that no MCU occurred $(\mathrm{n} = 0)$ and is given using the cumulative Poisson probability by:

$$\begin{aligned} \mathrm{MCU_{proba}} &= 1 - \sum_{i=0}^{n} \frac{e^{-P} \times P^i}{i!} \\ &= 1 - e^{-P} \quad \text{for } n = 0 \end{aligned} \tag{2}$$

Multiplying this probability by the total number of SEU gives the number of Multiple Cell Upsets. This number divided by the total number of SEU is the percentage of MCU. Using formulas (1) and (2), the percentage of "false" MCU (SEUs from 2 different events are counted as a MCU) is:

$$\text{false MCU } \% = 1 - e^{-E_{\mathrm{SRP}} \times \frac{\mathrm{AdjCell}}{N\mathrm{bit}}} \tag{3}$$

In order to double check the relevance of this model, MCU percentages obtained from formula (1) are compared to MCU percentages counted from randomly generated error bipmaps

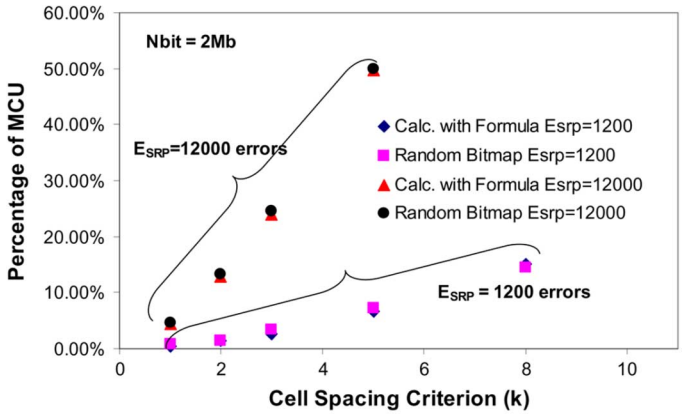


Fig. 14. Comparison of MCU percentages obtained from either a randomly generated bitmap or from formula (1) for a 2 Mb memory array ($Nbit = 2\ \mathrm{Mb}$).

(Fig. 14). This figure shows that whatever the CS criterion, the MCU percentages match perfectly.

Formula (1) is very convenient as it is easy to use and it can be used for different devices (SRAM, DRAM, etc.) and many radiation sources (alpha, neutron, heavy ions, etc).

ACKNOWLEDGMENT

The authors would like to thank their colleagues H. Tupin, C. Prunier, and O. Guillermin for their work on test engineering. The authors would also like to extend their gratitude to B. Borot and F. Jacquet for their involvement in test-chip design.

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