Altitude SEE Test European Platform (ASTEP) and First Results in CMOS 130 nm SRAM

Jean-Luc Autran, *Senior Member, IEEE*, Philippe Roche, Joseph Borel, *Senior Member, IEEE*, Christophe Sudre, Karine Castellani-Coulié, Daniela Munteanu, *Member, IEEE*, Thierry Parrassin, Gilles Gasiot, and Jean-Pierre Schoellkopf

***Abstract*—The "Altitude SEE Test European Platform" (ASTEP) is dedicated to real-time soft-error rate (SER) testing of semiconductor memories. The platform, located in the French Alps on the "Plateau de Bure" at 2552 m, has been operational since March 2006. This test facility includes a proprietary automatic test equipment specially designed for static memory (SRAM) testing and secured remote control operation via internet. First real-time SER measurements on 3.6 Gbit of SRAMs manufactured in CMOS 130 nm technology are reported, as well as the comparison between real-time and accelerated SER. Project perspectives for CMOS 65 nm SRAMs are finally reported.**

***Index Terms*—Accelerated tests, alpha-SER, atmospheric neutrons, neutron-SER, real-time testing, SER simulation, single-event effects (SEE), single-event rate (SER), static memory, terrestrial radiation environment.**

I. Introduction

SINCE terrestrial cosmic-rays have been identified to be at the origin of soft errors in modern integrated circuits, the estimation of soft error rates (SER) is rapidly becoming a major consideration for reliability aspects at device, circuit and system levels [1]. For deep submicron technologies, SER of chips is becoming a vital customer issue and its determination is still an open challenge, not only to investigate and understand technology sensitivity but also to extrapolate the trends for future generations of circuits.

Different experimental and simulation approaches are known to estimate SER: accelerated testing using alpha, neutron or proton source/beam, life testing under natural environments, modeling and software simulation at device or circuit level, combination of experimental/simulation approaches [1]–[6]. In contrast with accelerated testing which is relatively easy to conduct, cheaper and fast (a few hours/days is generally sufficient to obtain confident results), life testing is clearly time consuming and expensive. But it appears as the unique experimental solution to accurately estimate SER, ensuring that the test does not introduce artificial results due, for example, to beam uniformity/fluctuations, dosimetry errors, chip disorientation or difference in spectrum (largely introduced by the cut-off energy of the accelerator which is always well below cosmic ray energies). Life testing can also address SER at system level for complex electronic solutions and, installed in an underground site, provide an efficient method of monitoring for radioactive contamination. On the contrary, when based at altitude to increase the flux of particles (primarily neutrons, but also pions and protons), SER by life testing can be accelerated by a factor $\sim$2–15 depending on the earth location of the test site.

The project of an "Altitude SEE Test European Platform," located in the French Alps and simultaneously opened to industrials and laboratories to conduct, in the same place, qualification tests or research works, was initiated by STMicroelectronics and JB R&D in 2001. The ASTEP consortium was created in 2003 and operated by the CNRS and L2MP laboratory in 2004, in the framework of a multi-partner European-national funding program (the preliminary project was presented during the RADECS'05 industrial exhibition at the booth L2MP-CNRS). At the end of 2004, Bertin Technology (Aix-en-Provence, France) was selected as the industrial integrator of the automatic tester equipment. The construction of the machine was conducted in 2005, including one trimester of tests and qualifications and the preparation of the test area on the Plateau de Bure. Finally, the equipment was installed in altitude, on the Plateau de Bure, in February/March 2006 and the first campaign of SER life testing officially began on March 2006. The aim of this paper is precisely to present a brief overview of this project and to report the first experimental results obtained during this initial 5-month operation period. The paper is organized as follows: Section II briefly describes the test platform and gives some experimental detail concerning the platform location and its environment (Subsection II.A), the automatic test equipment constructed in the framework of the ASTEP project (Subsection II.B) and the tested devices (Subsection II.D). Experimental results are presented in Section III: real-time data (Subsection III.A) as well as their comparison with accelerated (Subsection III.B) and simulated (Subsection III.C) SER results. Finally, Subsection III.D presents some project perspectives for a near-term (2007–2008) period

Manuscript received October 6, 2006; revised December 12, 2006. This work was supported by the European Commission, the Provence Alpes Côte d'Azur Regional Council, the Hautes Alpes Department Council, the City of Saint-Etienne en Dévoluy, STMicroelectronics, the Centre National de la Recherche Scientifique, the Université de Provence, and the Institut Universitaire de France. The ASTEP Project (www.astep.eu) is operated by L2MP-CNRS, in collaboration with STMicroelectronics, JB R&D and with the technical support of IRAM.

J.-L. Autran is with L2MP, UMR CNRS 6137, Bât. IRPHE, BP 146, F-13394 Marseille Cedex 13, France and also with the Institut Universitaire de France, F-13394 Marseille Cedex 13, France (e-mail: jean-luc.autran@up.univ-mrs.fr).

P. Roche, T. Parrassin, G. Gasiot, and J.-P. Schoellkopf are with STMicroelectronics, 38926 Crolles Cedex, France (e-mail: philippe.roche@st.com).

J. Borel is with JB R&D, Ferrière, 05250 Saint-Etienne en Dévoluy, France.

C. Sudre was with L2MP, UMR CNRS 6137, Bât. IRPHE, BP 146, 13384 Marseille Cedex 13, France. He is now with INSEET, 84400 Rustrel, France.

K. Castellani-Coulié and D. Munteanu are with L2MP, UMR CNRS 6137, Bât. IRPHE, BP 146, 13384 Marseille Cedex 13, France.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2007.891398

Fig. 1. General view of the Observatory on the Plateau de Bure. The ASTEP platform is hosted in Building POM2 indicated in the figure (Photo courtesy of IRAM).

TABLE I
LOCATION AND MAIN ENVIRONMENT CHARACTERISTICS OF THE ASTEP PLATFORM (AFTER [7])

ASTEP, Plateau de Bure, France		
Latitude (°N)		44.6
Longitude (°E)		5.9
Elevation (m)		2550
Atm. depth (g/cm^2)		757
Cutoff rigidity y (Gy)		5.0
Relative neutron flux	Active Sun low	5.76
	Quiet Sun peak	6.66
	Average	**6.21**

concerning the real-time characterization of CMOS 65 nm SRAMs and the development of an *in situ* neutron monitor station installed close to the test equipment.

II. TEST PLATFORM AND EXPERIMENTAL DETAILS

A. Location and Environment

The ASTEP platform is located in the French Alps at 2 552 m of elevation. The installation is hosted by the Institute for Radio-astronomy at Millimeter Wavelengths (IRAM) on the Plateau de Bure in the Dévoluy Mountains. Fig. 1 shows a general aerial view of the observatory on the Plateau: the ASTEP platform is installed in an ancient radio-telescope building reconverted into an altitude laboratory platform (one floor standard concrete slab building). The main environment characteristics of the ASTEP platform are summarized in Table I. Since 2006, this test location has been referenced in the latest release of JEDEC Standard JESD89A [7]. Data of Table I corresponds to values of Table A3.B in [7].

B. The Automatic Test Equipment (ATE)

The ASTEP masterpiece is a specially designed and universal SRAM automatic test equipment (ATE), capable of monitoring several thousands of synchronous/asynchronous SRAM memories and performing all requested operations such as writing/reading data to the chips, comparing the output data to the written data and recording details on the different detected errors. The ATE hardware and software have been designed and developed by BERTIN Technologies (Aix-en-Provence, France), in collaboration with L2MP-CNRS and STMicroelectronics. The design of both the hardware and software components of the system follows all the specifications of the JEDEC SER test standard [7]. Table II lists the main features

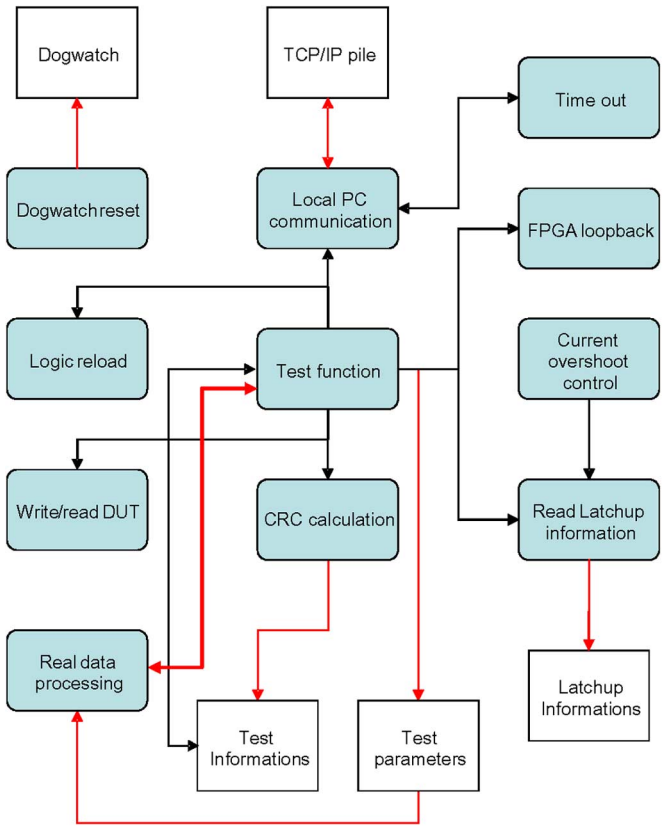

Fig. 2. Block diagram of the test processor function subsystems, showing the implemented functions (blue), the action flux (black lines) and the data flux (red lines).

of the constructed equipment with some indications about ATE capabilities. In addition, Fig. 2 gives a block diagram representation of the ATE test processor, showing the different subsystem modules, action and data flux. Higher level functions, such as test flow selection, data processing and log file writing are performed by the test software; lower level functions (in particular the scanning through the memory array and the comparison of read data with expected data) are performed by hardware controllers mounted on the boards. Particular precautions were taken to minimize digital noise sources at different levels: filtered and UPS-protected power supplies, ground and power supply plans optimization for all mother and daughterboards, electromagnetic shielding of the test processor box, special test procedure to verify written data and to discriminate transient errors possibly induced by the system itself (cf. II.C). Fig. 3 shows a schematic representation of the whole test equipment. This system is divided in two identical subsystems, Astep1 and Astep2, capable of independently performing an automatic survey of two racks of memories placed into temperature-controlled ovens (RT-125°C). Each rack contains 8 motherboards; each motherboard connects 40 daughtercards and each daughtercard drives 2 test chips. The daughterboards (and consequently the chips) are oriented face horizontally. The current consumption of each daughtercard, i.e., of each pair of devices, is real-time monitored on 4 supply lines on a total of 5 for Single Event Latchup (SEL) detection. This explains the relative complexity of the electronic circuitry developed

TABLE II
MAIN TECHNICAL CHARACTERISTICS OF THE ASTEP AUTOMATIC TEST EQUIPMENT (INSPIRED FROM TABLE 7.2 IN [1])

ASTEP Automatic Test Equipment (ATE) characteristics		Comments
Data-logging and error monitor		
Continuous verification of device date vs. expected data	Yes	Automatic sequences
Timestamp of the detection of the error event	Yes	Send an email + log file
Identification of failing device	Yes	Graphic human-machine interface
Failing memory address	Yes	Logical and physical addresses
Background data pattern generation		
Basic (solid 0, 1, checkboard, etc.)	Yes	
Advanced (vector list, conditioned by address, etc.)	Yes	Logical or physical pattern (entry file)
Memory content-dependent	No	Possible upgrade
Test		
Initialization and basic functional test	Yes	
Static (W/R, wait, R/W/R,…)	Yes	Configurable sequences and patterns
Dynamic	Yes	Configurable sequences, patterns and test frequency
Identify and correct errors based on the selected test conditions	Yes	Exclude failed circuits
Selectable address counting scheme	No	Possible upgrade
Other hardware/software features		
Low noise design	Yes	Ground and shielding optimized ATE powered via stabilized UPS
Current monitoring of every device	Yes	Current monitoring (4 supply channels on 5) of each daughtercard (2 chips)
Device disconnect (fuse)	Yes	Automatic latchup monitoring with adjustable threshold current
Device disconnect (FET switch)	Yes	Configurable by soft (entry file)
Device reconnect (FET switch)	Yes	Configurable by soft (entry file)
Reusability of tester for different chips	Yes	High modularity (daughterboard, motherboard, test processor, control software, power supplies, etc.)
Temperature monitoring	Yes	Use of controlled drying and heating ovens (RT-125°C)
Bit-error mapping and data processing	Yes	Graphic human-machine interface
Real-time data display capability	Yes	Email alert system
Remote control	Yes	Total secured remote control of the ATE using an internet connection

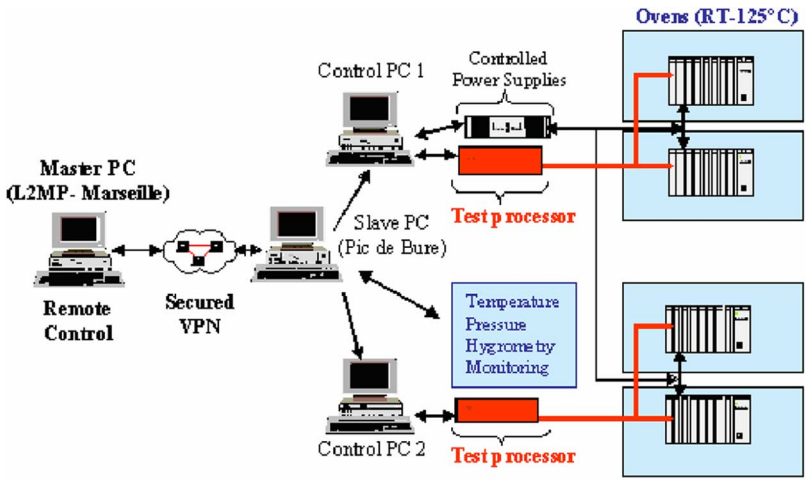

Fig. 3. Schematic description of the automatic test equipment (ATE) designed and built to perform real-time SER tests on static memories. The ATE is divided in two networked subsystems (Astep1 and Astep2), capable of monitoring two memory racks (640 test chip per rack) placed in temperature-controlled ovens.

at the level of each daughtercard (current monitoring) and for each motherboard (the system is able to disconnect a given daughtercard in case of abnormal power consumption; the current intensity threshold is directly controlled by the software interface as an input parameter of the test). Fig. 4 shows a zoom of a motherboard with its daughtercards and test chips. The maximum capacity of the ATE in the current configuration is 1280 test chips. Of course, the system is modular and it will be able to received additional racks for future experiments. The ATE can be completely controlled in remote control mode via a

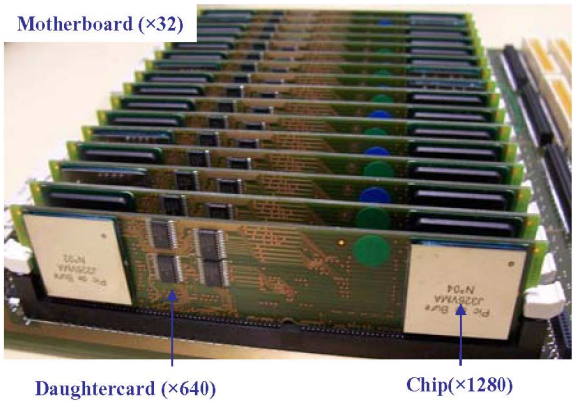

Fig. 4. Detail of one motherboard containing 40 daughtercards and 80 test chips (2 per daughtercard). The complete ATE system is designed to test a maximum of 1280 chips dispatched on 32 motherboards and 640 daughtercards.

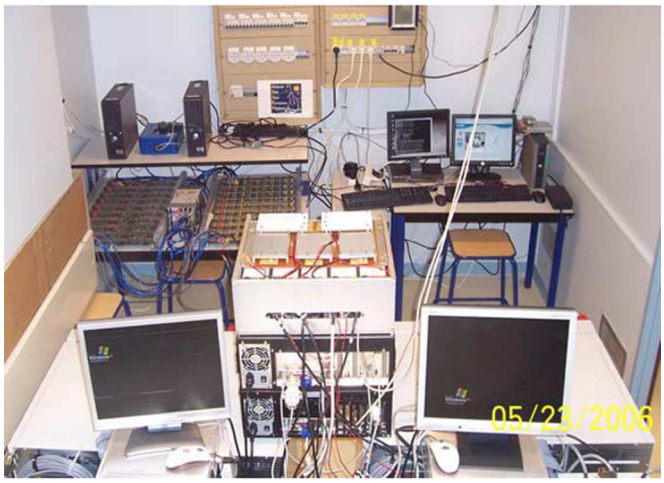

Fig. 5. General view of the equipments installed in the ASTEP test room. The ATE system is visible on the first plan. The Xilinx "Rosetta" experiment boards [10], hosted by ASTEP, are visible on the second plan (left).

virtual private network (VPN) on internet. This allows the users to perform all control operations during a real-time experiment and to access all the data in real-time. Fig. 5 shows a general view of the ASTEP installation (main test room).

C. Test Procedure

The test procedure implemented in the ATE control software is summarized in Fig. 6. This procedure allows the discrimination of the following error types as a function write/read and rewrite/reread operation results:

- "*Transient Soft Error*" (TSE), sometimes called dynamic read error;
- "*Static Soft Error*" (SSE), i.e., classical bit flip;
- "*Single-Event Hard Error*" (SHE), sometimes referred as stuck bit.

When an error is detected, the software increments the data-log file with all information concerning the fail:

- Date and time;
- Type of error (TSE, SSE or SHE);
- Written pattern and read pattern;
- Round number (i.e., scan number of all memories from the beginning of the experiment);

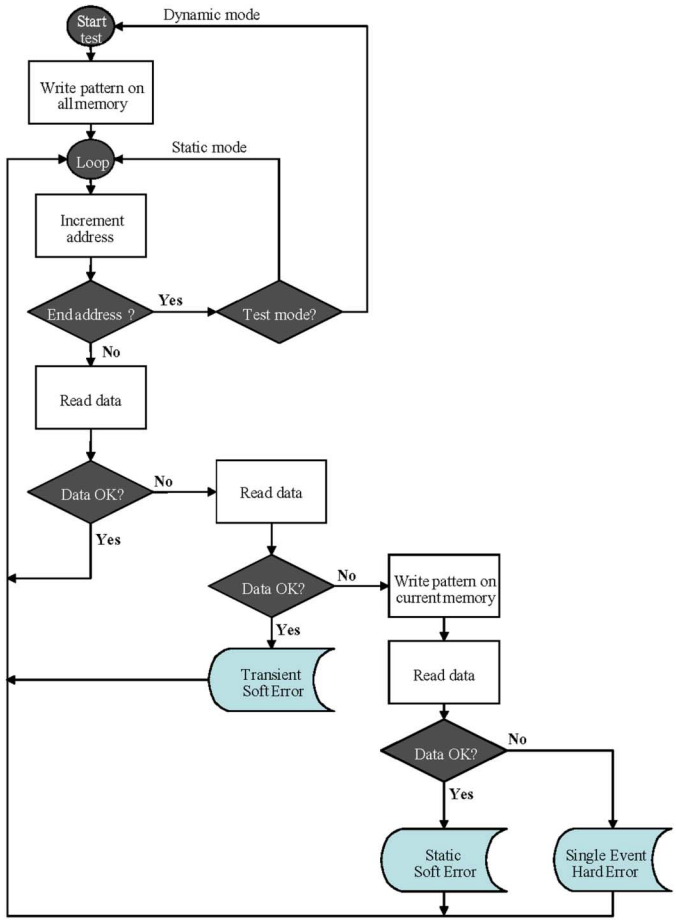

Fig. 6. Flowchart of the test procedure implemented in the ATE control software.

- Testchip identification (rack, board, slot and chip numbers);
- Logical address.

An additional software is used to perform a physical mapping of the bit flips. This mapping is used to discriminate logical multi-bit upsets (MBU) from physical multi-cell upsets (MCU), as recently recommended by JEDEC specifications [7].

D. Devices Under Test

The first real-time testing campaign has been currently performed on bulk static memories (SRAM) fabricated by STMicroelectronics using a CMOS 130 nm commercial technology (PBSG-free) process. This technology was extensively characterized in previous works using alpha irradiations (with both ST and L2MP setups) and neutron accelerated SER tests performed with two continuous neutron sources available in North-America (TRIUMF and LANSCE facilities). The use of a mature and well-characterized technology is important for the validation of ATE functionalities and data comparison between accelerated and life time testing.

Fig. 7 shows the schematic and the layout of the elementary memory point: it corresponds to a 6-transistor cell with a bit cell area of 2.50 μm^2. The layout of the complete test chip is shown in Fig. 8. This test chip is composed of different memory cuts; only cut #9 (4 MBit) has been used (i.e., connected) for the

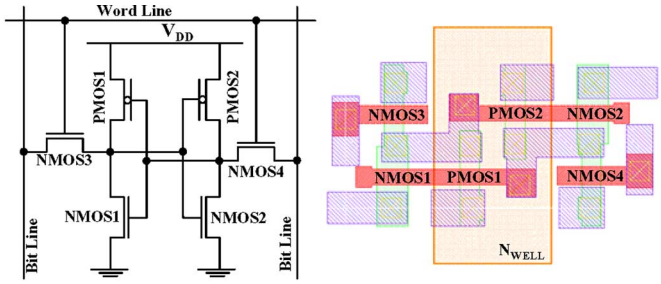

Fig. 7. Schematic and layout of the 6T SRAM memory cell manufactured by STMicroelectronics in CMOS 130 nm technology. The bitcell area is 2.50 μm^2.

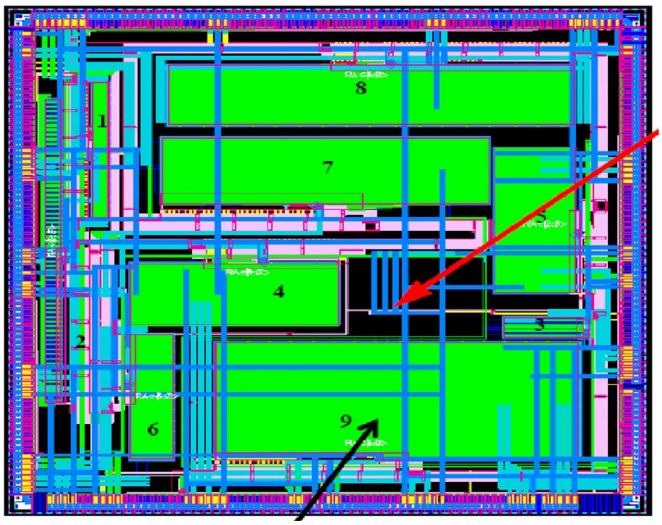

Fig. 8. Layout of the complete memory test chip. Only cut #9 (4 MBit) was used for real-time testing. The location of the laser fuses for cut selection is also indicated (red arrow).

present measurement campaign. The ATE was initially loaded at 72% of its maximal capacity with 492 test chips in the Astep1 subsystem and 424 chips in Astep2, respectively. This represents a total of 912 chips, i.e., 3 664 MBit under test.

III. Experimental Results

A. Real-Time Testing Results

Fig. 9 shows the cumulative fail number versus test hours for the two subsystems Astep1 and Astep2 during the period March 31–September 6, 2006. These events correspond to Static Soft Errors (SSE) detected under nominal test conditions (V_{DD} = 1.2 V, room temperature and checkerboard pattern for all devices). Because of several maintenance operations in the test room, the two subsystems were subjected to interruptions during this period. However, the number of MBit×h cumulated during these five months approaches 10^7 MBit×h, which gives an excellent confidence interval on the extrapolated SER, as shown in the following. A total of 44 fails was detected, including 38 single event upsets and 3 MBU. These later involved 2 physical adjacent bit cells in all cases.

Experimental data consistency was checked in terms of statistical distribution of $0 \rightarrow 1$ and $1 \rightarrow 0$ bit flips (Fig. 10) and error bitmap (Fig. 11). These results show satisfactory distributions compliant with a "random process" in so far as the frequency of bit flips is close to 50% for each transition and there is no flagrant accumulation of errors in a particular area of the

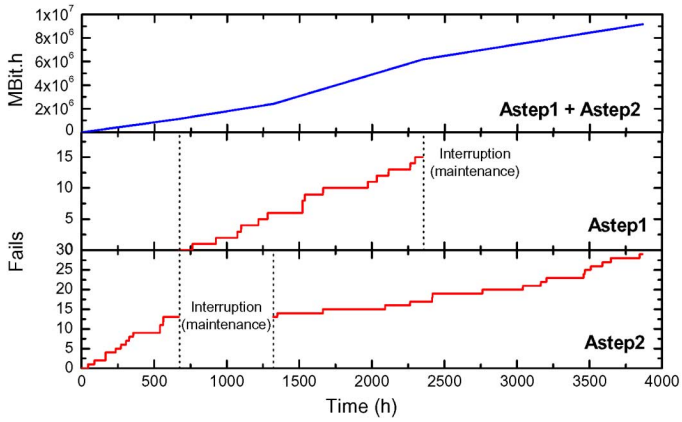

Fig. 9. Cumulative fail numbers versus test hours for the two boards Astep1 and Astep2 of the ATE. The experiment started on March 31, 2006 and finished on September 6, 2006 under nominal test conditions (V_{DD} = 1.2 V, room temperature, checkerboard). The cumulated number of MBit×h versus test hours is also indicated (approaching 10^7 MBit×h at the end of the present test period).

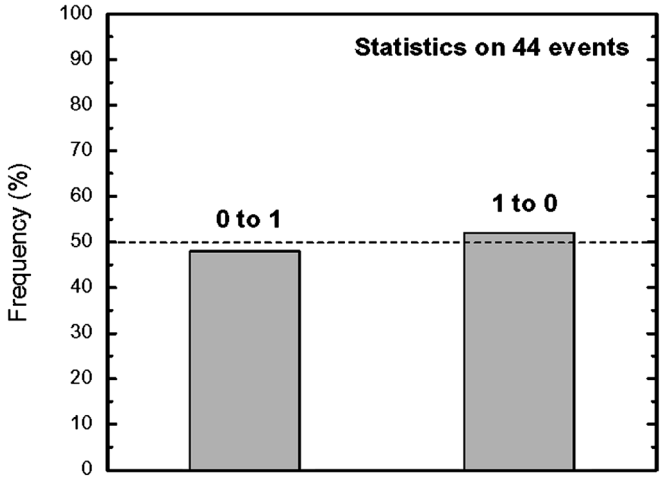

Fig. 10. Frequency distribution of $0 \rightarrow 1$ and $1 \rightarrow 0$ bit flips corresponding to the 44 Static Soft Errors (SSE) reported in Fig. 9.

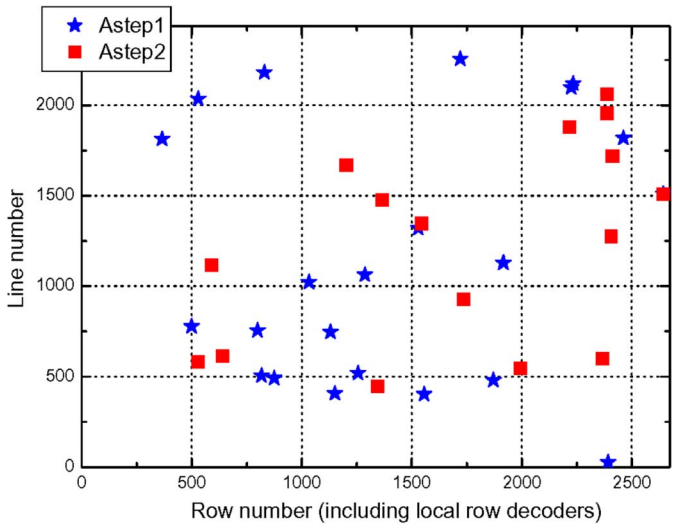

Fig. 11. Cumulative error bitmap corresponding to data of Fig. 9. The memory plan (2048 × 2048) corresponds to the 4 MBit cut #9 (see Fig. 8). It includes in this figure the local row decoders.

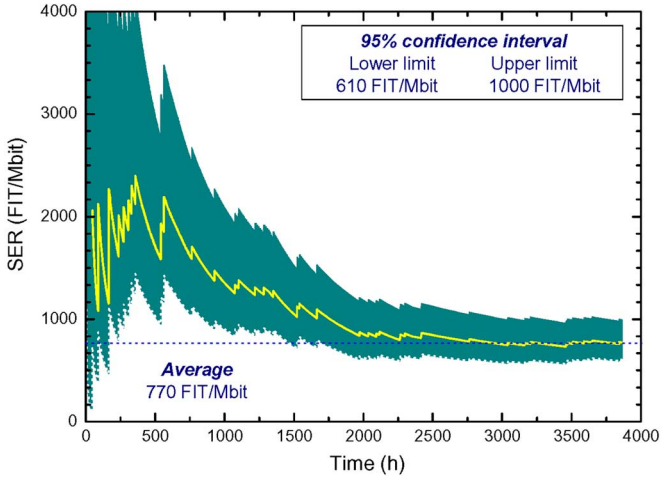

Fig. 12. Estimated real-time SER (FIT/MBit) versus test hours calculated from data of Fig. 9. 95% confidence intervals are also indicated. The average acceleration factor value of 6.21, given in [1], was used to estimate this real-time SER. The erratic character and high value of the SER in the first ~ 1000 hours are due to the very low number of cumulated fails during this initial period, introducing a large error in the evaluation of the ratio $\mathrm{N_r}/\Sigma_\mathrm{r}$ in (1).

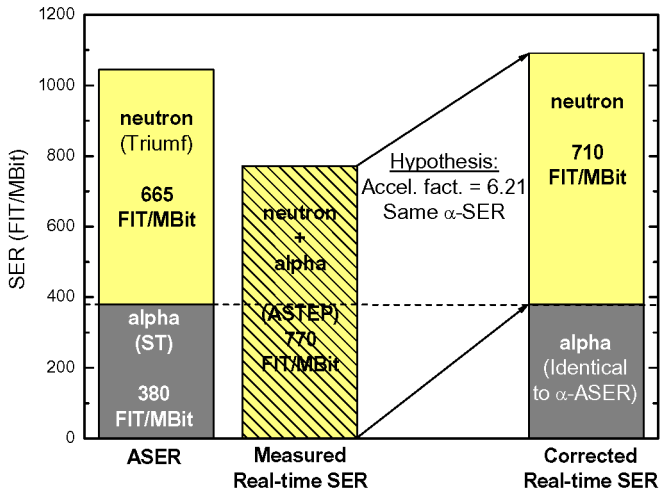

Fig. 13. Comparison between the accelerated (ASER) and the real-time SER estimated in Fig. 12. Accelerated tests were performed at Triumf facility for neutron-ASER and at both ST-Crolles and L2MP-Marseille for alpha-ASER characterization, respectively. Real-time SER data of Fig. 12 is corrected from the contribution of alpha disintegrations, considering a same alpha-SER for both accelerated and real-time experiments.

memory plan. Such verification is not sufficient but necessary to ensure that the ATE is correctly working.

From data of Fig. 9, we estimated real-time SER, shown in Fig. 12, using the following expression:

$$\mathrm{SER} = \frac{\mathrm{N_r}}{\mathrm{AF} \times \Sigma_\mathrm{r}} \times 10^9 \ (\mathrm{FIT/MBit}) \tag{1}$$

where $\mathrm{N_r}$ is the number of errors observed at time $\mathrm{T_r}$, AF is the acceleration factor of the test location and Σ_r is the number of MBit×h cumulated at time $\mathrm{T_r}$ given by:

$$\Sigma_\mathrm{r} = \int_0^{\mathrm{Tr}} 4 \times \mathrm{N(t)}\, dt. \tag{2}$$

In (2), the factor 4 accounts for 4 MBit per device and $\mathrm{N(t)}$ represents the number of test chips under test at time t.

The acceleration factor value is considered equal to $\mathrm{AF} = 6.21$ for the ASTEP platform. It corresponds to the estimated relative neutron flux (average value) of the Plateau de Bure with respect to the reference flux of New York City, as reported in Table A.3-B of [7].

Ninety-five percent confidence interval upper and lower limits [7] are also indicated in Fig. 12. An average value of 770 FIT/MBit is obtained, with lower and upper confidence limits equal to 610 and 1000 FIT/MBit, respectively. In addition, Fig. 12 shows that the convergence of SER vs. test hours is reached in approximately 2000–2500 h, i.e., for 4–6 $\times 10^6$ MBit×h. Beyond this duration, the SER remains constant around 770 FIT/MBit.

B. Accelerated Versus Real-Time SER

In complement to real-time characterization, both neutrons and alpha irradiations (under nominal test conditions) were performed on several test chips issued from the same technological lot. This data allows us to directly compare accelerated versus real-time SER. Neutron experiments were performed using the continuous spectrum sources available at both the Los Alamos Neutron Science Center (LANSCE) and at the Tri-University Meson Facility at Vancouver, (TRIUMF). At LANSCE, as at TRIUMF, the neutron spectrum closely matches the terrestrial environment for energies ranging from 1 MeV to 800 MeV (few meV to 400 MeV at TRIUMF). The acceleration factor at LANSCE is 1.33×10^8 times higher than the natural ground level flux. Thus, one hour of neutron bombardment under this intense source is equivalent to 15 753 years at sea-level. Alpha experiments were conducted with an intense Am^{241} alpha source at the main STMicroelectronics Front-End Technology and Manufacturing site located at Crolles, France. The acceleration factor is 3×10^{12} at 1.0 mm from this source, at room temperature and in the air. Additional measurements were also performed using a less intense Am^{241} source at the L2MP laboratory. SER values obtained with these two setups agreed within $\pm 10\%$. Fig. 13 shows the normalized accelerated results for this commercial CMOS 130 nm SRAM. Average values of 380 FIT/Mbit and 665 FIT/Mbit have been obtained for alpha-SER and neutron-SER, respectively. It is noteworthy that the orders of magnitude for these failure-in-time rates are realistic, reminding that one FIT corresponds to one soft error every billon chip-hours. The accelerated measurements are extrapolated assuming: i) for the semiconductor processing and packaging materials a natural alpha emissivity of 10^{-3} alpha/cm^2/h and ii) a reference neutron flux equal to 14 particles/cm^2/h at sea level (New York City).

If we try now to compare, as in [11], these accelerated and real-time test results, one have to reminder that the SER given by the altitude experiment (i.e., 770 FIT/MBit) must be corrected from the impact of alpha contamination affecting all tested devices. In other words, this signifies that a certain number of fails detected by the ATE during the test period have been induced by alpha particles and not by neutron interactions. Supposing a real-time alpha-SER equal to the value given by accelerated tests (i.e., 380 FIT/Mbit) and taking into account the acceler-

TABLE III
COMPARISON OF SERS ACQUIRED BY THE THREE DIFFERENT METHODS ON 130 NM SRAMS: ACCELERATED TEST, REAL-TIME AND MONTE CARLO SIMULATION

	Neutron-SER (FIT/Mbit)
Accelerated-test (Triumf)	**665**
Real-time test (corrected)	**710**
Monte-Carlo simulation	**700**

ation factor $(\mathrm{AF} = 6.21)$ of the test location only for neutron-induced fails, we obtain a corrected neutron failure-in-time of 710 FIT/Mbit. This corrected value is very close to the accelerated neutron-SER equal to 665 FIT/Mbit, demonstrating, in this case, a very good agreement between the two estimation methods within the experimental error margins.

C. Simulated Versus Real-Time SER

Three Dimensional (3D) Monte Carlo simulations used to predict neutron-SER were also performed for this SRAM circuit, using a proprietary radiation simulator developed by STMicroelectronics [6], [8], [9]. This simulation code considers the exact layout of the memory cell and calibrated TCAD results as inputs. Simulation results for nominal conditions ($\mathrm{V_{DD}} = 1.2$ V, room temperature) give a typical neutron failure-in-time of 700 FIT/Mbit. This value is very close to those corresponding to both accelerated and real-time experiments. In conclusion, as summarized in Table III, we can consider that the three SER values, respectively obtained by accelerated test, real-time experiment and Monte Carlo simulations, give the same order of magnitude for the neutron failure-in-time of the 130 nm SRAM, within a typical error domain estimated to be $\sim$20%. At this level of our investigations, we explain this result not only by the deep and accurate knowledge of the technological process, device architecture and circuit configuration for this mature 130 nm technology but also by the great number of experimental tests (involving numerous samples) conducted these last years in terms of alpha and neutron characterization.

D. Future Works

Since September 9, 2006, a new measurement campaign has been started with the same 130 nm SRAM circuits. The objective is now to quantify the impact of several key-parameters, i.e., the power supply voltage, the test temperature (up to 125°C) and the configuration of the written pattern, on the real-time SER. Another objective is also to further compare real-time and accelerated tests for which data is already available on this test vehicle.

Beyond this work currently in progress, STMicroelectronics (Crolles), with its partners NXP (formerly Philips Semiconductor) and Freescale (formerly Motorola), is envisaging to test a new circuit on the ASTEP platform within the following months. This circuit is a CMOS 65 nm test vehicle for library qualification and process monitoring. It contains 8.5 Mb of single port SRAM (bit cell area of 0.525 $\mu\mathrm{m}^2$) already characterized this year from an accelerated-test point-of-view with neutrons at LANSCE and TRIUMF, as well as with alphas at STMicroelectronics. About 1000 test chips, representing a memory capacity up to 8 Gbit, is envisaged to be mounted in the automatic test equipment by the beginning of 2007.

The last near-term perspective for the ASTEP platform is the development, in 2007, of an *in situ* neutron monitor, installed close to the test equipment (directly in the test room) to try to correlate the observed circuit fails with the total neutron flux incident on the experimental area. This equipment, based on high pressure He^3 neutron proportional counters, should be completed by a high sensitivity neutron spectrometer in 2008–2009 for a more accurate characterization of the ASTEP radiation environment. This point is crucial for a better understanding of circuit response to neutrons and for the study of SER fluctuations, primarily induced by the modulation of cosmic ray flux, solar cycle, latitude and altitude, etc. [12], [13].

IV. CONCLUSION

In conclusion, the present work represents the first experimental validation of the "Altitude SEE Test European Platform" as a technical installation capable of performing real-time characterization of semiconductor memories with a non negligible (estimated) acceleration factor of $\sim$6.2 with respect to sea level. Real-time SER estimation on 3.6 Gbit of SRAMs manufactured in CMOS 130 nm technology has been successfully conducted during five months, which represents not far from $\sim 10^7$ MBit$\times$h. The estimated failure-in-time has been found to very reasonably agree (within $\sim$20%) with values obtained during accelerated tests and with numerical SER simulations. We explain this result by the accumulation of numerous experimental works, TCAD and SER simulations performed these last years on such a very mature 130 nm technology which strongly reduced statistical dispersions from sample-to-sample and error intervals on the knowledge of some physical, technological and electrical key-parameters.

ACKNOWLEDGMENT

The authors would like to thank their colleagues J.-M. Drevon, G. Wauters, and D. Delhom from BERTIN Technologies (Aix-en-Provence) for their major technical contribution to the development and construction of the automatic test equipment. The logistical support of the Institute for Radioastronomy at Millimeter Wavelengths (IRAM) is also gratefully acknowledged. Special thanks are due to B. Gautier (IRAM, Station Manager of the Plateau de Bure Observatory), B. Saint-Cricq (CNRS, Délégation de Provence, Marseille), P. Nguyen (formerly L2MP-CNRS), and J.-M. Bec (Univ. Montpellier II) for their assistance and support. Finally, the authors would like to acknowledge A. Lesea (Xilinx, San Jose) and J. Le Mauff (Xilinx France) for their collaboration in the framework of the "Rosetta" experiment [10].

REFERENCES

[1] J. F. Ziegler and H. Puchner, SER—History, Trends and Challenges, Cypress Semiconductor. San Jose, CA, 2004.
[2] E. Normand, "Single event upset at ground level," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2742–2750, Dec. 1996.
[3] T. J. O'Gorman, J. M. Ross, A. H. Taber, J. F. Ziegler, H. P. Muhlfeld, I. C. J. Montrose, H. W. Curtis, and J. L. Walsh, "Field testing for cosmic ray soft errors in semiconductor memories," *IBM J. Res. Develop.*, vol. 40, no. 1, pp. 41–50, 1996.

[4] P. E. Dodd, "Device simulation of charge collection and single-event upset," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 561–574, Apr. 1996.

[5] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, 2005.

[6] P. Roche, "Year-in-review on radiation-induced soft error rate," in *Proc. IEEE Int. Reliability Physics Symp. Tutorial*, San Jose, CA, Mar. 2006.

[7] JEDEC Standard Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices, JESD89 Arlington, VA: JEDEC Solid State Technology Association [Online]. Available: http://www.jedec.org/download/search/JESD89A.pdf

[8] P. Roche and G. Gasiot, "Impacts of front-end and middle-end process modifications on terrestrial soft error rate," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 382–396, 2005.

[9] P. Roche, "Comparisons of soft error rate for SRAMs in commercial SOI and bulk below the 130 nm technology node," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2046–2054, Dec. 2003.

[10] A. Lesea, S. Drimer, J. J. Fabula, C. Carmichael, and P. Alfke, "The Rosetta experiment: Atmospheric soft error rate testing in differing technology FPGAs," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 317–328, 2005.

[11] H. Kobayashi, H. Usuki, K. Shiraishi, H. Tsuchiya, N. Kawamoto, G. Merchant, and J. Kase, "Comparison between neutron-induced system-SER and accelerated-SER in SRAMs," in *Proc. IEEE Int. Reliability Physics Symp.*, Phoenix, AZ, 2004, pp. 288–293.

[12] E. Normand and T. J. Baker, "Altitude and latitude variations in avionics SEU and atmospheric neutron flux," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1484–1490, Dec. 1993.

[13] E. Normand, "Correlation of inflight neutron dosimeter and SEU measurements with atmospheric neutron model," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1996–2003, Dec. 2001.