Design and Fabrication of Pockels Effect EO Polymer Modulators as Novice Designers.

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***Abstract* — Our goal is to understand and document the process of designing and fabricating silicon photonic devices from scratch as new designers. Throughout the design process, we study the Mach-Zehnder Interferometer (MZI) and specifically a length-mismatched polymer-modulator MZI which we then fabricate in-house. This is an example of how quickly one can get accustomed to the design process and with access to tooling and training, can produce electro-optic (EO) modulators that rival currently available commercial options.**

I. Introduction

As an introductory undergraduate course at the University of British Columbia, ELEC 463: Micro/Nanofabrication Laboratory provides students with little or no background in the emerging field of silicon photonics or VLSI fabrication the opportunity to learn the theory of a fundamental device, then fabricate it in a small-scale lab with access to cutting edge equipment and processes.

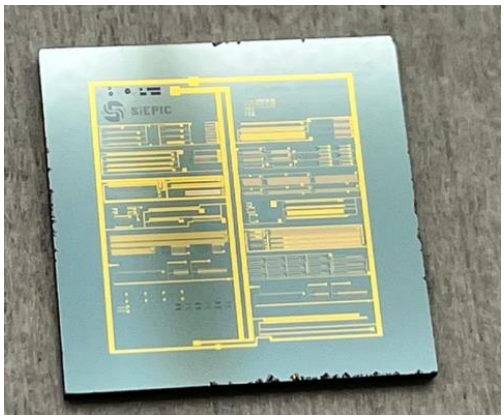


Figure 1: Completed fabricated silicon-photonic chip produced in the Steward Blussom Quantum Matter Institute laboratory with classmates in ELEC463.

This is an opportunity to study polymer based electro-optic effect interferometer modulators using state of the art chemistry with the potential to achieve over 100gbit/s modulation [1]. Not only is the data transfer rate attractive, but EO modulators are an energy-efficient solution with low propagation losses, and are soon likely to be integrated in various datacenters that currently spend significant portions of their energy budget on heating and cooling [2]

We first model a basic Mach-Zehnder Interferometer (MZI) and study the effects of length mismatch in the interferometer arms. This is a static example of how modulating works. As we study the fundamental physics of the devices to fabricate, we also study the workings and physics of the manufacturing tooling and processes to understand how manufacturing variations affect how the device is fabricated and how it differs from what we design.

We then actually manufacture the devices we design in CAD, going through the design process from a wafer of Silicon on Insulator through lithography and metallization in the laboratory facilities located on-campus in the Stewart Blussom Quantum Matter Institute (QMI). Here we not only manufacture but validate our designs and empirically measure and see our working designs outside of computer modelling and simulation using the Laboratory's suite of optical signal processing equipment.

Our major intentions for this project are to measure our devices nominally throughout the manufacturing process to understand said process variations, and to validate our interferometer process by successfully recording expected effects when we modulate our interferometers. Validating our small-scale process also legitimizes the ability to rapidly prototype silicon photonic circuits and optimize designs over multiple processes in time frames shorter than typical large scale fabs.

II. Modelling and Theory

A. *Mach-Zehnder Interferometer*

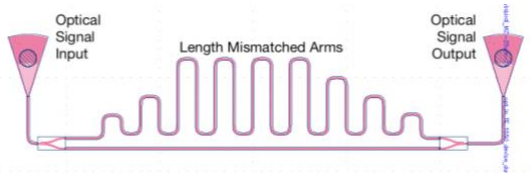


Figure 2: Example of Length Mismatched MZI designed with the SiEPIC-EBeam-PDK

A Mach-Zehnder Interferometer operates the principle of a traveling pulse of light in a waveguide being split and recombined. Below is the transfer function (1) derived by Dr. Chrostowski [3], and the lossless case below (2):

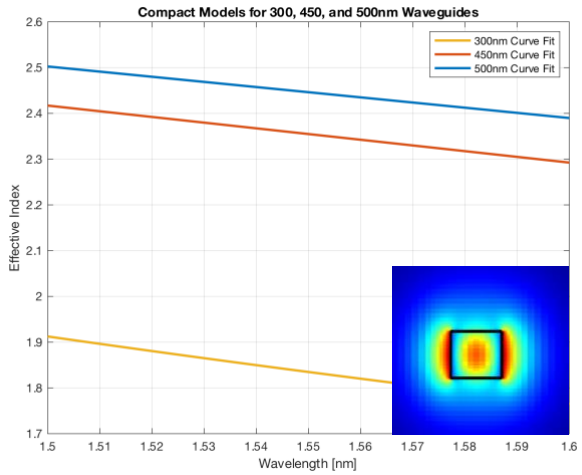
$$H(\lambda) = \frac{I_O}{I_I} = \frac{1}{4}\left|e^{-i\beta(\lambda)L_1} + e^{-i\beta(\lambda)L_2}\right|^2, \quad (1)$$

$$\frac{I_O}{I_{I\ lossless}} = \frac{1}{2}(1 + \cos(\Delta\beta\Delta L)) \quad (2)$$

Where the term β is the complex propagation constant including the propagation loss that is dependent on the n_{eff} of the waveguide material.

$$\beta = \frac{2\pi n_{eff}(\lambda)}{\lambda} - i\frac{\alpha}{2}\lambda, \quad (3)$$

The term n_{eff} is the comprehensive index that considers the mode solution to the waveguide. It considers geometry of the waveguide, the impact of varying the wavelength of our input sweep, and polarization of the signal. For this investigation we only focus on the first quasi-TE mode of the waveguide. We use a 2nd order Taylor Series expansion for simplicity and we see how it changes for example with waveguide width.



300nm	$n_{eff} = 1.8348 - 1.4801(\lambda - 1.55) - 1.4423(\lambda - 1.55)\text{^}2$
450nm	$n_{eff} = 2.3548 - 1.2457(\lambda - 1.55) - 0.0355(\lambda - 1.55)\text{^}2$
500nm	$n_{eff} = 2.4462 - 1.1262(\lambda - 1.55) - 0.0405(\lambda - 1.55)\text{^}2$

Figure 3: Different effective indices for varied waveguide widths and wavelength sweep, with respective Waveguide Compact Models below. Compact models are derived from Palik using Lumerical MODE with instruction from Dr. Chrostowski [3]. Inset: 220nm by 300nm waveguide signal intensity for TE polarized wave simulated in Lumerical MODE.

In an interferometer with identical arms, we get the nominal loss for all wavelengths of optical signal we input. In cases where we have non-identical beta terms or lengths, we observe a sinusoidal pattern that converted into a logarithmic gain looks like as below:

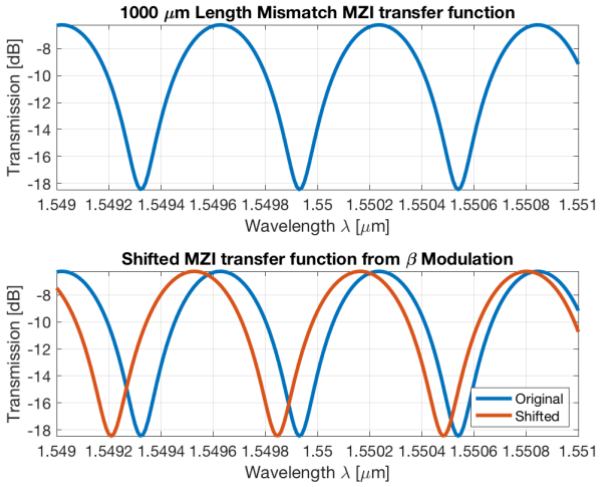


Figure 4: Example of sinusoidal gain in decibels for (top) 1000μm length mismatched MZI, and (bottom) estimated shift of spectrum for an example change in effective index coefficients in waveguide compact model. Both use a 100pm wavelength sweep resolution. [need to update with proper effective model for modulation]

We measure the distance between subsequent maxima or minima known as our interferometer's Free Spectral Range. It can be measured but also calculated as a function of our device's group velocity as derived in [4]:

$$\text{FSR} = \Delta\lambda = \frac{\lambda^2}{\Delta L\left(n - \lambda\frac{dn}{d\lambda}\right)} = \frac{\lambda^2}{\Delta L n_g}$$

B. *Pockels Effect:*

To modulate this interferometer, we can use the Pockels Effect on the material surrounding the waveguide to vary the effective index of the waveguide. The relationship of the changing index of refraction is derived [4]:

$$\Delta n_{eop} = -\frac{1}{2}n_{eop}^3 r_{33} E = \frac{1}{n_{eop}}\chi^{(2)}E, \quad (3)$$

Where n_{eop} is the refractive index of the polymer and the r_{33} is the electro-optic coefficient, representing how well the chromophores within the polymer are aligned based on polling. We are using a 2:1 ratio of HLD1:HLD2 and can expect the following values given a polling voltage:

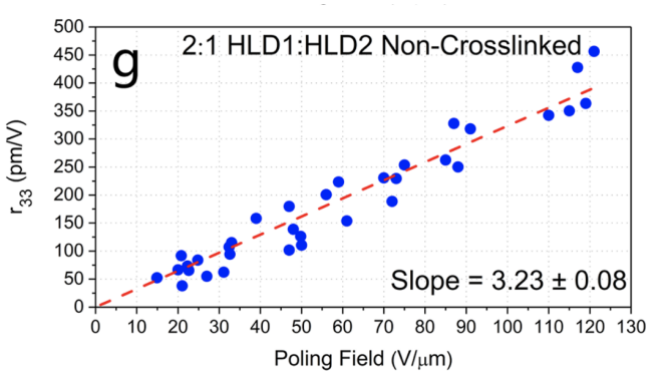


Figure 5: Fitted relationship between Electro-optic Coefficient, r33, and Polling Field by Xu et al [1].

We can find the relationship to our waveguide's effective index using a Finite Differential Eigenmode Solver such as Lumerical MODE. We can then simulate our MZI to find the anticipated result of modulation, providing us with information on our

Effective Index of waveguides – need to use Lumerical MODE to get the effective index model with maximum polymer effect

Empirical n_{eop} is ~1.8

r_{33} determined from polling: 200V/25μm = 8pm/V???

After Polling, the chromophores in the polymerare aligned in a common direction. Once aligned, we can apply a modulating electric field across the polled region to slightly shift the alignment in the polymer. This slight change in alignment causes the change in effective index.

The r33 relationship

Effective index changes

V_π modelling

Evaluation criteria – Good model grounded in correct understanding; accurate and relevant results.

C. Simulation Results

Show graphs and tables. Include waveguide mode profiles, plots of the waveguide effective index versus wavelength, transmission spectrum of your device, etc.

III. Design

A. Design objective

For this course, we are attempting to utilize the polymer-optic effect to create a working modulator for the first time as new designers. Our *Figure of Merit* is to design an interferometer that optimizes the Pockels effect and although we do not know the yield for this new process, we'd like to maximize the effect if we were to obtain a functioning device. This can prove to us the benefit of the polymer-optic effect over one manufacturing cycle we undergo during a 12-week university semester.

B. Design Methodology

As new designers, we adopted a simple design flow of translating our basic MZI theory into a layout with only the idea to optimize the Pockels effect. Knowing that effect increases with a longer interaction period [3], we designed the effected arms to be as lengthy as possible. Also knowing the Pockels effect creates a small perturbation in the effective index, we want to be able to see the effect as obviously as possible [3]. For this reason, we choose an imbalanced MZI layout with a very small FSR to view any excitations we may see on a similar scale.

C. Design of Experiment

Below in Table 1 we list 6 devices to fabricate and run our polymer-optic effect experiment on. To add further redundancy of having visible polymer-optic effects, we added a 350nm wide waveguide configuration. In Figure 7**,** it's visible that with a smaller width waveguide there is a larger portion of stable optical signal existing outside the waveguide in the surrounding material. When our polymer's effective index is modulated, the more signal we have interacting with the polymer would affect our response.

Design of Polymer-Optic MZI Devices				
Design #		**Wave Guide Width**	**ΔL**	**Max L**
Short	1	350 nm	1000 µm	2312 µm
	2	500 nm	1000 µm	2332 µm
Long	3	350 nm	1500 µm	15012 µm
	4	350 nm	2200 µm	15712 µm
	5	500 nm	2200 µm	15732 µm
Big	6	350 nm	3000 µm	~30000 µm

Table 1: Variations of Polymer-Optic Modulators to fabricate and Test. All are in unbalanced MZI configurations with length mismatch of ΔL and longer length arm of Max L. They are to be injected with 1550nm wavelength TE optical signal.

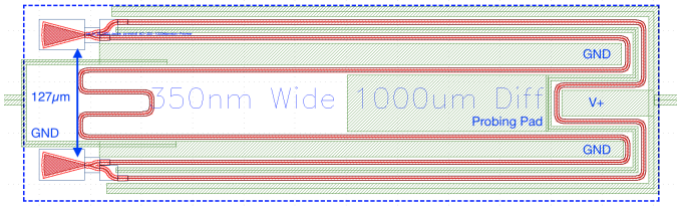


Figure 6: Short-1 Device with labelled electrical connections. Both arms of the interferometer are polled, but only from the Probing Terminal to Ground is modulated and affected. This Design can easily create variants with different lengths and mismatches.

Test Measurement Structures		
Design #	**Wave Guide width**	**Measurement**
7	350 nm	Decoupling
8	500 nm	Decoupling
9	500 nm	Decoupling with Y-Branch

Table 2: Test Structures on or nearby devices under test used for determining insertion loss and to validate any noise added by fiber array and grating coupler during measurement.

Listed in Table 2 are our Test Structures that characterize noise that is generated in our signal from the grating couplers. It was specified to keep these as close as possible to our devices to ensure they accurately represent the losses we see when we measure our devices.

Polling Distance	25µm
Modulating Distance	10µm
Polling Voltage	200V or 1000V
r33 value	8V/µm or 40V/µm

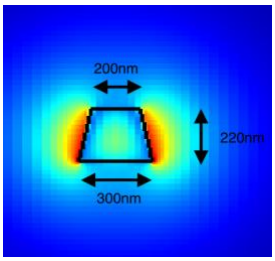


Figure 7: Left: Intensity of 1550nm signal in first TE Mode injected into 300nm wide by 220nm tall Si on SiO2 waveguide, showing amount of signal outside Silicon waveguide in surrounding material (air) useful for polymer-optic effect. Right: Changes of confinement factor when manufacturing variation such as sloped walls occurs and how this variation can be an advantage with polymer-optic effect.

D. Manufacturing variability

As noted in Figure 7 we can see the potential effect of variations on our signal. One way to note potential outcomes and to better understand our fabricated device is to corner analysis and Monte Carlo simulations to our designs which we can then compare with our simulations. With this comparison, we can better estimate dimensions of our devices that we cannot accurately measure, such as the actual width of our devices, without destructive techniques.

E. Mask Layout

To manufacture these devices, we first design the mask layout we will use for our specified process using the SiEPICfab EBeam ZEP PDK [4] in the KLayout GDS Layout

Tool. To achieve best yield, we followed the following design rules provided [5] and as specified in the appendix.

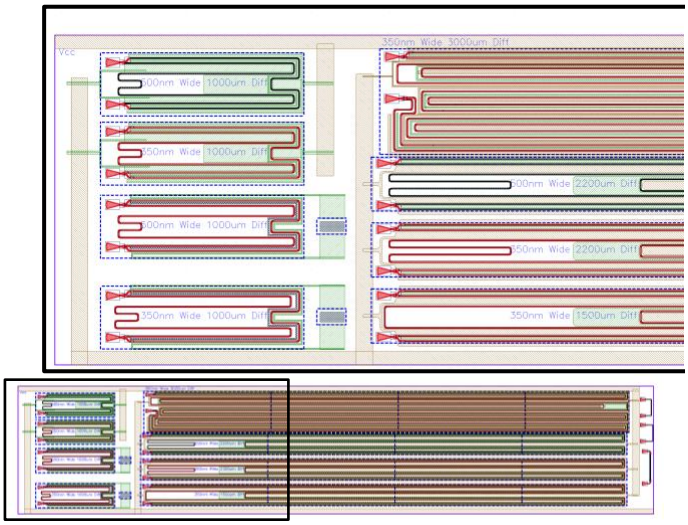


Figure 8: Full Mask Layout with zoomed area of interest above. Six Polymer-Modulators connected to global Polling Electrodes (top and bottommost metals) and two backup Thermo-Optic Effect Modulators (bottom-left) along with three decoupling test structures (right). Designs optimized for long lengths and small FSRs with variation in waveguide width.

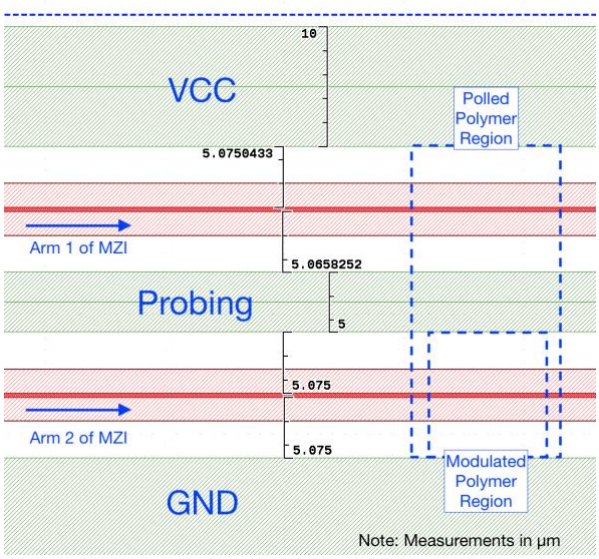


Figure 9: Enlarged view of Short-1 MZI (350 Wide, 1000 ΔL). Annotations denote distances between metal and Silicon features, regions of polling and modulation, and metal connections. Polling occurs in the electric field between VCC and GND, and the modulation only affects polymer between Probing and GND metal connections. All measurements are in micro-meters.

A major rule involved keeping our electrical probing pads 500 µm away from our correctly oriented grating couplers to allow us to measure and modulate our devices at the same time. Other rules involved preventative design to avoid overlap and bleeding between areas of fine geometry that have been learned in previous process yields [3]. A large design constraint was to utilize global polling pads to poll the entire chip rather than individual devices.

IV. Manufacturing and Test Procedure

A. Fabrication

To manufacture our chips, we had our Teaching Assistant (TA) Donald Witt who was trained for the Clean Room Lab equipment prepare, etch, and clean our chips. It is very important to cut multiple chips as we use some to set-up processes as well have redundancy in the event of process variations and defects. We marked the underside of the 6 chips that we began our process with and stored in a clean gel pack.

Our manufacturing steps include:

Stage	Steps	Figure
Prep	Dicing of Wafer Cleaning of Wafer	Figure 11
Silicon Etching	EB Resist Spin + Baking BEAMER Electron Beam Lithography EB Resist Development Plasma Etch Post-Etch Cleaning	Figure 11
Validation	Microscope Imaging Automated Testing	
Metal-ization	PhotoResist Spin + Bake Photolithography PhotoResist Development Metal Evaporation/Deposition Lift-off	Figure 13
Validation	Microscope Imaging Automated Testing	
Adding Polymer	Plasma Etch Cleaning Polymer Mixing Polymer spinning	Figure 14
Polling	Polling of Polymer	
Data Collection	Microscope Imaging Manual Probing Testing	

1) Dicing of Wafer

We begin with procuring a Silicon on Insulator (SOI) wafer from our supplier [?]. Using the DISCO DAD3240 Dicing Saw [6] we can cut the size of wafer we need, then clean our silicon surface using acetone and isopropyl.

2) Electron Beam Resist:

We are doing a **Negative EB-Resist** using the ZEP Process. As in Figure 10, this allows us to cost- and time-effectively etch away portions of Silicon on the top layer of our SOI wafer *around* our devices instead of over the entire chip which is unique for our ZEP Process.

With one of our diced chips as a test chip, we place it on 180°C hot plate for 30min while cleaning the 200mm Headway Spinner with acetone and drying with N_2 gas [7]. After timer expires apply Zep520A Resist covering 60% of the wafer. Spin using ramped program as in Appendix on the 200mm Headway Spinner. Immediately return to hot-plate and bake at 180°C for 2min. Using the FILMETRIX F20 Thin Film thickness measurement system [8] we can measure the amount of resist we apply ensuring we achieve 530 to 560nm of resist [7]. We can take this measurement in several locations on the test chip to verify we have an even spread. If needed we can clean, adjust our steps, and re-apply until we verify our process and proceed to apply resist to the other chips.

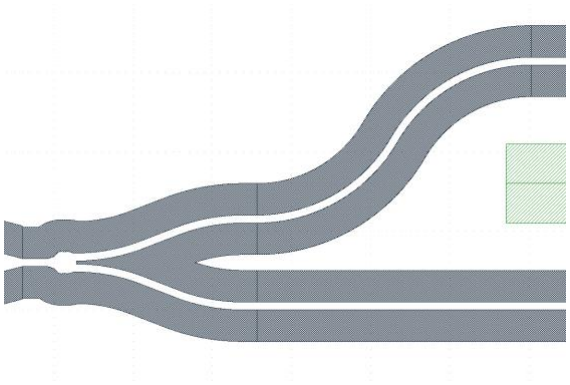


Figure 10: ZEP-EBeam-Process where white is Silicon to keep and grey is Silicon to be etched. The surrounding Silicon has no effect on our devices performance wise and is usually etched away when using a Photolithography process.

Figure 11: Process Cross Sections per procedure that were used to develop a waveguide using the ZEP-E-Beam-Process using the on-site tooling and equipment in Dr. Chrostowski's lab.

3) Electron Beam Lithography

Prior to lithography, we used the BEAMER Software [9] to map out which parts of our designs would have the highest Electron Beam current, focus, and time of exposure onto the EBL-Resist. For rough edges we can go faster with less focus and a higher current but on our waveguide edges, where we want smooth sidewalls, we increase the focus and ensure that there is no scattering of our beam. This allows the resist on top of our waveguide to be as untouched as possible by the electron beam leaving a very distinct difference from etched and non-etched areas after the etching process.

The UBC SiEPIC Lab has access to a Jeol JBX-8100FS Electron Beam Lithography System [10] that Donald will run to weaken the EBL-resist overtop of our etch regions.

Before applying the various dosages of electron beam to our chip that we calculated using BEAMER, we spend multiple steps aligning and calibrating the machine to our chip's height and area to ensure the beam is in focus on each part of our chip following our Runsheet [11, 12]. Due to

material variations in our SOI wafer, the machine creates a heightmap of our chip, so in areas that are taller/shorter the beam can be focussed appropriately to properly react with the EBL-Resists that are at different heights.

4) Resist Development

Shortly after lithography, Donald developed the chips in ZED-N50 and washed with IPA on the isothermal plate at 20°C [13]. We do this in a very controlled process where we rinsed out the beakers with the chemicals to prevent any contaminants from entering the reaction. We place the chip in the ZED-N50 for 1minute slowly agitating vertically before precisely removing at the 57 second mark and immersing in the IPA solution at the 60 second mark.

5) Plasma Etch and Residue Removal:

We have access to an Oxford Instruments PlasmaPro 100 Cobra ICP RIE Etching machine. This machine allows us to do a highly selective dry etching in a plasma environment, as well as highly directional physical etching using Reactive Ion Etching all in the same process.

Our first step in the etching process is cleaning the etching chamber. This clears any residue left by previous processes that may introduce impurities into our process. Now with a clean etching environment, we run our etching program on an empty wafer **without** our chip present. This allows the environment of our first etch to be as like the environments of the etches afterwards. In our lab we have empirically found that running 5 etches serially is our general limit for keeping the etching chamber consistent.

After setting our environment we attach our chips onto the empty holding wafer with vacuum grease and proceed with the etching program. Our etching program runs with the following parameters:

Parameter	Value	Units
Chamber Pressure	10	[mTorr]
SF_6 Gas Flow	25	[sccm]
C_4H_8 Gas Flow	35	[sccm]
ICP Power	600	[W]
Table HF Power	30	[W]

Figure 12: Machine settings for PlasmaPro 100 Cobra ICP RIE Etching Machine used for our ZEP-EBeam-Process to dry etch our silicon and electron beam resist.

We turn the gasses sulfur hexafluoride, SF_6, and isobutylene, C_4H_6, into plasma by fluctuating a magnetic field from the inductor in the chamber to induce electric fields that supply energy to the atoms [14]. This leads to the atoms in the gas to undergo most commonly the dissociation and ionization chemical reactions that create species that participate and enhance the etching process [15].

Once etched, we use chemicals Remover PG along with EKC265 to remove any leftover debris after etching. These are done at very specific temperatures and times and before doing we must remove any remaining vacuum grease from the backside of the chip with ethyl acetate and clean our tools, specifically our custom-designed Teflon sample holder, with Acetone, IPA, and N_2 gas specifically in that order to prevent leftover residue. [16]

We use one beaker of Remover PG on the stirring hotplate at 80°C, one beaker of EKC265 on another hotplate also at 80°C, another beaker of PG Remover at room temperature, and 5x beakers of IPA. [16]

We do 15 minutes in the hot Remover PG, then place in the room-temperature Remover PG for 5 minutes. After this timer, we dunk rinse in the two IPA beakers one at a time before placing in our EKC265 for 30 minutes. After this we do the same dunk rinsing with 3 beakers of IPA to remove any leftover chemical. [16]

6) Photoresist Spinning, Photolithography, and Development

To add our probing and polling metals to our chip, we apply a similar process but use photolithography on our resist rather than electron beam lithography to take advantage of its fast write-time that blankets the whole chip instead of serially writing the layout.

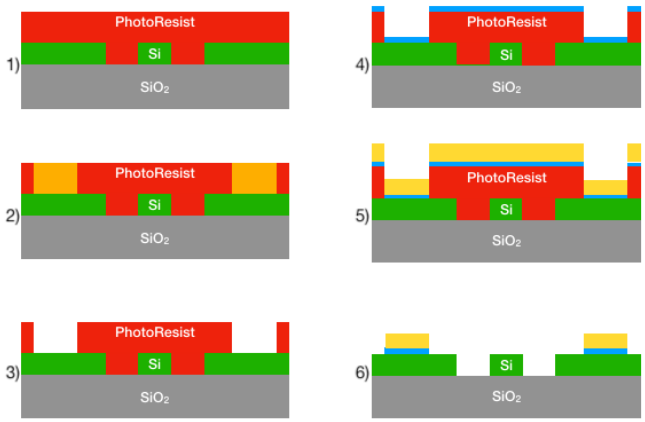


Figure 13: Metallization Process, starting with high amount of (1) photoresist, (2) lithography, (3) development, (4) Titanium Evaporation Deposition, (5) Gold Evaporation Deposition, (6) and Liftoff Etching. All processes were conducted in SBQMI Clean Room (not to scale).

Before spinning our photoresist, we very quickly clean our chip in a O_2 Plasma Etch for 5-minutes in the small dry etcher in the lab [17]. As that finishes we clean and program the spinner then we first apply LOR2A, baking for 5 minutes at 200°C on a hotplate. After baking, we use our second photoresist and program our second spinner program to apply the AZ5214 photoresist, which we then bake for 1 minute at 98°C. We can use the FILMETRIX F20 Thin Film Measurement System to obtain the height of resist we apply which needs to be significantly higher than 105nm to ensure proper lift-off.

After baking we transfer to a carrier wafer and place our chip in the MLA-150 Maskless Lithography System [18]. After lithography, we develop in MIF300 for 45 seconds, quickly transferring and rinsing for 10 seconds in de-ionized water, completing our photoresist mask.

7) Metal Evaporation

To deposit metal on our chip, we use the process of metal evaporation using the AJA Hybrid Evaporator System to chemically bond our metal to our silicon [19]. After securing our chip with Kapton tape, we first deposit 5nm of Titanium,

then 100nm of Gold. If you're reading this, make sure you take the tape as a souvenir as Bruce did and it was very cool to see him have a piece of tape covered in <1mm of gold. Lukas also mentioned he had to go into the back room of a jewelry store to purchase the gold nugget that we evaporated [3].

8) Metal Lift-off

Using Remover 1165 [17], we leave the chip overnight in a beaker for the resist under the metal to break apart and lift-off. We did require some ultrasonication the day after to agitate some of the metal that did not lift off initially. This is a step where yield can be affected as due to non-removed metal, metals joining from ineffective mask distance between metals, and too much metal removed during ultrasonication.

9) Polymer Application

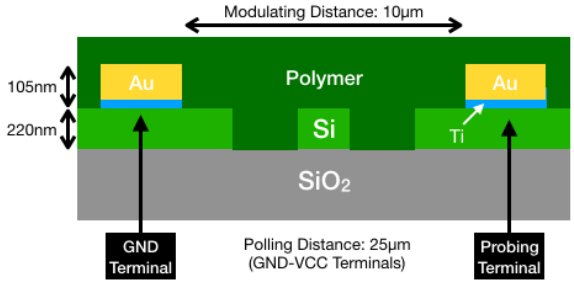


Figure 14: Completed Fabrication Cross Sectional schematic of EO Modulator, viewing modulated arm of MZI (not to scale).

Our last step in manufacturing is spreading our polymer. We do this by bringing our HLD1 and HLD2 mixtures to room temperature from refrigerated storage and mixing a 2:1 weight ratio of HLD1:HLD2 which we then add TCE solvent to create a 9% weight liquid solution [20]. For thinner films a 5% weight solution can be used. We do not have the ability to predict our variables of interest from this manufacturing stage but attempt to cover our chip completely ensuring that the space between our metal and waveguide is filled.

B. Measurement Procedure

For the following, please contact the author of this paper or fellow classmates until updated at a later date.

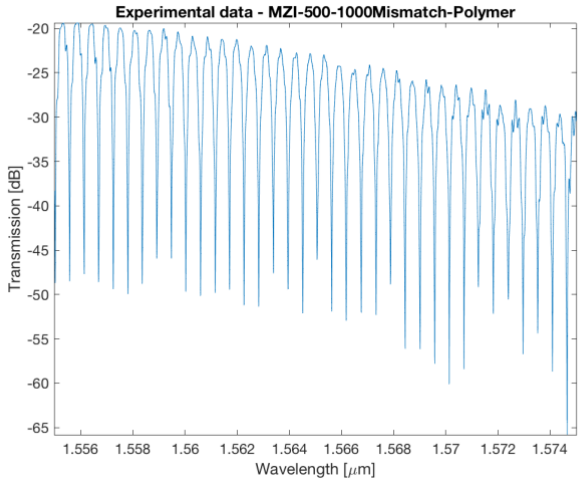
1) Fibre Array and Automated Testing
2) Polling
3) Polymer Modulation

V. Analysis

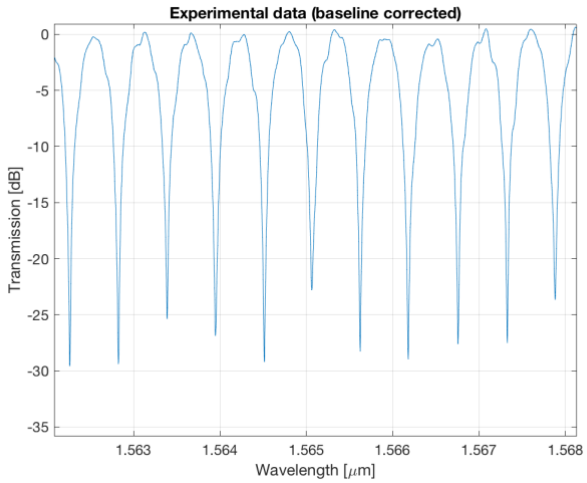
A. Devices Under Study

Note: During measurement of other devices on the chip, a short had suspected to occur which had raised the temperature of the chip far above it's temperature to de-align polymers.

Using the laboratory optical signal tools [write name] we can sweep input wavelength and find our results.



We can see our interferometer's transfer function in the data but need to remove the offset and any noise. We can do this by method of linear interpolation in MATLAB. We attempt to curve fit this data but have some difficulty with our datasets. Once curve fitted, we can extract various parameters of our device and work backwards to discover any variations in dimensions and performance caused by fabrication.



B. Example Devices:

Analyze experimental data and report – using tables, graphs, and in the text. Curve fitting of the optical spectra is performed to extract parameters. Show how this is performed. The analysis includes data extracted from the experiments:

- Tables of the group index (say at 1550 nm) and FSR
- Plot of the free spectral range (FSR) vs. wavelength for both air and oxide cladding
- Plot of the group index (air, oxide) vs. wavelength
- Switch performance. Extract the central wavelength and plot it's variation with power – Δlambda / Δpower
- Calculate the switch efficiency (e.g., mW/FSR).
- Calculate the resistance
- Determine the max % tuned before the device died.
- Plot, tabulate, or report on T vs. mW. T can be found either by numerical thermal models, or by using a combination of experimental data and simulations (dneff/dT).

Analyze the performance of your different designs. Tabulate the Δlambda/ΔT slope for the different designs; both experimental and model.

C. Comparison of experimental results with simulations.

There are many ways to compare your experimental results with simulations. I describe two methods here:

1) Corner analysis simulations vs. experimental data

This is perhaps the easiest method. You take into account the anticipated manufacturing variations during your design, and generate figures that show your expected variations in the parameter of interest (e.g., waveguide group index, or FSR). Then you extract the same parameter from the experimental results. You plot all these on the same figure. If your experimental results lie within your simulation corner analysis, you are successful! If not, re-think why you have a difference: Is the fabrication error is larger than anticipated? Do you have a simulation / model / theory error?

You can also plot your results using histograms or box plots.

2) Matching a model to experimental data

This is more involved. The idea is to try to find the physical parameters that give you a good agreement with the experimental results. This usually involved some detective work and parameter sweeps in simulations. You are hunting for the value of the parameters, e.g., waveguide width and height. This was well done in Figure 4 of Reference **Error! Reference source not found.**. Specifically, the experimental results and simulations were plotted on the same graph; simulation parameters were varied (this can be done manually or by a script) so that the curves match.

Update simulation parameters to match experimental results. Describe the procedure. Include a table of new parameters.

Update the simulation plots to overlap the experimental results. Don't show all the results. But include a summary of the results in a table.

VI. Discussion

It

The discussions section should include:

- Main points from the results are discussed
- Theories are developed; insight into what is going on and how it works, is provided
- Why did one design work better than another other?
- Are these results and conclusions statistically significant, or is it just experimental variations?
- What trends were observed?
- Provide insight into the design trade-offs. For example, does changing the path length difference, ΔL, change the switch efficiency?
- How can you improve upon your design? Speculations and future work are described and well grounded
- Are there any limitations to your design, simulations, approach, etc.?
    - Our Polling distance is 25µm, limited by global polling setup
    - Did not know the big picture until after submitting design for fabrication

Why use metal to carry the polling field? Lecture where we discussed rib waveguide. Also in Midterm. What about parallel Silicon "Terminal" to increase r33 as we don't require metal to be so close.

VII. Conclusion

The conclusion should not be a summary, though conclusions will often be written this way. Having some summary material is ok. But don't just repeat the Abstract. A conclusion should provide some further insight. What recommendations can you make? How do your results compare to other peoples' work?

Acknowledgement

Thank you to Iman Taghavi who aided in performing measurements, Donald Witt who aided in the fabrication, CMC Microsystems for providing the design tools, Dr. Lukas Chrostowski for the theory and insight during lecture. I would also like to thank my lab-mates pictured below who I worked with this semester for their collective help and questioning to further understand this design and fabrication process.

Figure 15: ELEC463 Tuesday Laboratory Section after completing fabrication

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VIII. Appendix

A. Design Rules for Mask Layout:

1. Use Strip TE 1550nm Waveguide specification
2. Grating Couplers on Left pointing right
3. Electrical Probing Pads minimum 500 µm from Grating Couplers
4. Minimum Feature Sizes:
    a. Silicon: 100 nm
    b. Metal: 5 µm
5. Minimum Space between layers:
    a. Silicon-Silicon: 100 µm
    b. Metal-Metal: 5 µm
    c. Metal-Silicon: 4 µm

B. Headway Spinner Ramp Program:

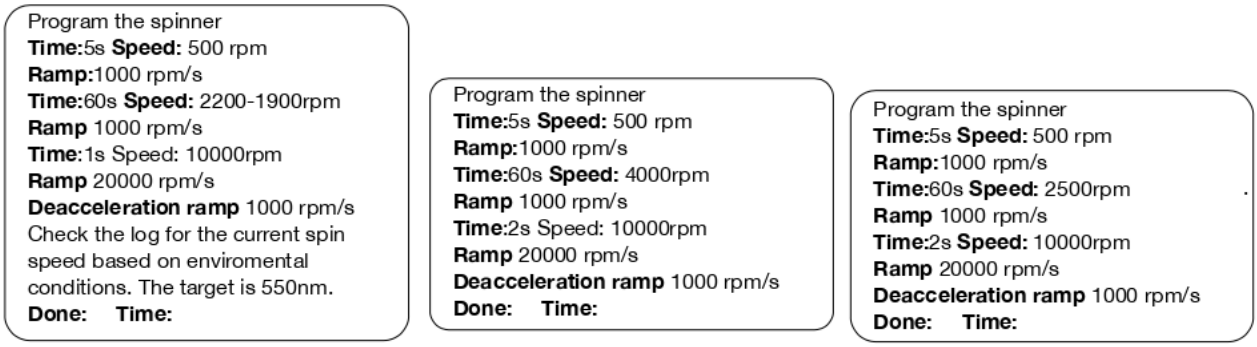

Figure 16: Programming steps when applying (left) Zep520A EBeam Resists to SOI [7], (center) LOR2A PhotoResist [17], and (right)AZ5214 PhotoResist [17].

IX. Table of Figures: