mux_4_to_1 Project Status (12/13/2020 - 13:10:16)			
Project File:	mux_4_to_1.xise	**Parser Errors:**	No Errors
Module Name:	mux_4_to_1	**Implementation State:**	Programming File Generated
Target Device:	xc3s50a-4tq144	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2	1,408	1%	
Number of occupied Slices	1	704	1%	
Number of Slices containing only related logic	1	1	100%	
Number of Slices containing unrelated logic	0	1	0%	
Total Number of 4 input LUTs	2	1,408	1%	
Number of bonded IOBs	7	108	6%	
Average Fanout of Non-Clock Nets	1.14			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:				

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Dec 13 11:05:24 2020	0	0	0
Translation Report	Current	Sun Dec 13 13:08:29 2020	0	0	0
Map Report	Current	Sun Dec 13 13:08:33 2020	0	0	2 Infos (0 new)
Place and Route Report	Current	Sun Dec 13 13:08:39 2020	0	0	1 Info (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Sun Dec 13 13:08:43 2020	0	0	6 Infos (0 new)
Bitgen Report	Current	Sun Dec 13 13:10:14 2020	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Sat Dec 12 17:07:47 2020	
WebTalk Report	Current	Sun Dec 13 13:10:14 2020	
WebTalk Log File	Current	Sun Dec 13 13:10:16 2020	

Date Generated: 12/13/2020 - 13:10:16