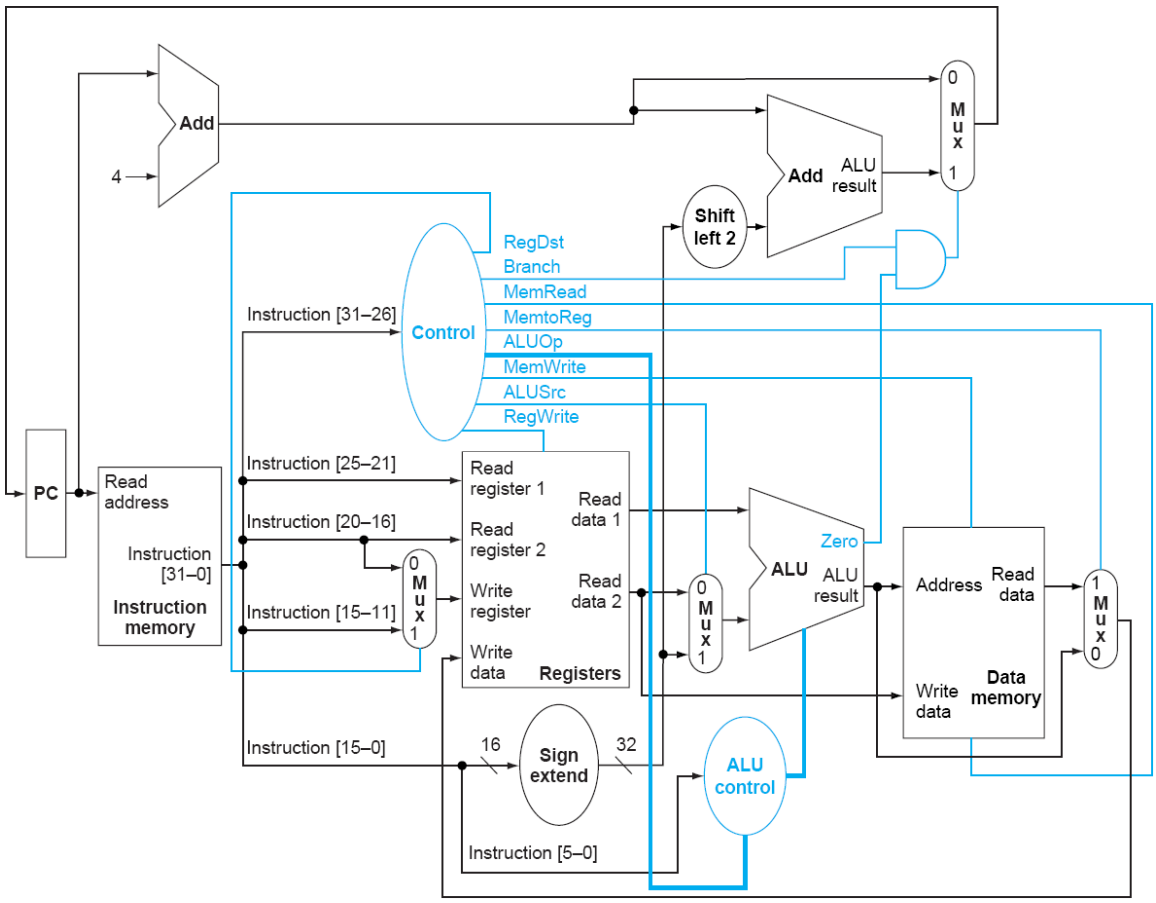
CSCE 212: Quiz 5 **Fall 2009**

Name (please print):_____ **Total points: ___/30**

Instructions

This is a CLOSED BOOK and CLOSED NOTES quiz. However, you may use calculators, scratch paper, and the green MIPS reference card from your textbook. Ask the instructor if you have any questions. Good luck!

1. (10 points) Provide all control signals for the ADDI instruction using the following processor design. Assume ALUOp is 10 for interpretation of instruction function code, 00 for add, and 01 for subtract.



RegDst	0	MemWrite	0
Branch	0	ALUSrc	1
MemRead	0	RegWrite	1
MemtoReg	0		
ALUOp	00		

2. (10 points) Describe how the above design would need to be modified in order to add the **BEQAL rs, rt, label** (branch if equal and link) instruction, which performs the following register transactions:

```
if R[rs] == R[rt] {
        R [31] <= PC+4
        PC <= PC+4+BranchAddr
}
```

Need a path from the “PC+4” signal back to the register file. This can be done by expanding the “MemtoReg” mux to add PC+4 as an option for the write data input to the RegFile.

The RegDst mux must be expanded to include an option for a hard wired “31”.

The “write” signal on the RegFile must be modified to implement control. The easiest way to do this is to add a new control signal called “Link” which is asserted whenever the CPU is executing a BEQAL instruction. The register file “write” can then be evaluated as:

RegWrite OR (Link AND Zero)

...which would cause a register write when the instruction is BEQAL and the branch is taken.

3. (10 points) Briefly describe the disadvantages of the single-cycle processor design.

Clock cycle must be adjusted to accommodate the instruction having the longest datapath (the LW instruction).